

MC33567

Advance Information

Dual Linear Controller for High Current Voltage Regulation

The MC33567 Dual Linear Controller is designed for motherboard/mainboard applications requiring reliable regulation of high current supply planes. This advanced linear IC provides the necessary drive, sense, and control signals to interface two separate N-channel MOSFETs as individual series pass elements regulating two different supply planes.

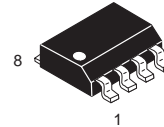
Use of this device lowers costs as well as ameliorates layout problems on pc motherboard products. Additionally, an under voltage-based short circuit detection and protection feature is provided which places system operation into a protected mode pending removal of the short.

Features

- Detects under voltage condition (short circuit condition) and places regulation into a protective “hiccup” mode, thus preventing damage and permitting recovery after short circuit condition is corrected
- Drive capability for SOT-223, DPAK, and D2PAK MOSFETs
- MC33567-1 controls two separate series pass transistors to provide regulation for separate 1.5V and a 1.8V supply planes. MC33567-2 controls two separate series pass transistors to provide regulation for separate 2.5V supply planes

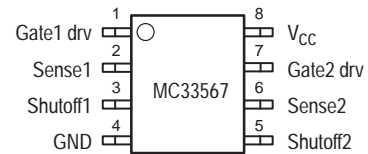


ON Semiconductor
Formerly a Division of Motorola
<http://onsemi.com>

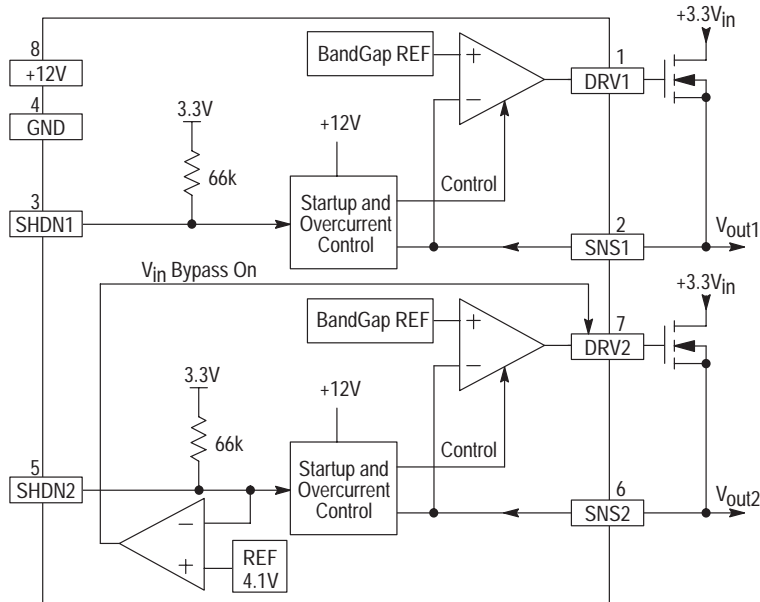


**SO-8
D SUFFIX
CASE 751**

PIN CONNECTIONS



Simplified Functional Block Diagram



This document contains information on a new product. Specifications and information herein are subject to change without notice.

ORDERING INFORMATION

Device	Output Voltage	Shipping
MC33567D-1	1.8V, 1.5/3.3V	98 Units/Rail
MC33567D-1R2	1.8V, 1.5/3.3V	2500 Tape&Reel
MC33567D-2	2.5V, 2.5V	98 Units/Rail
MC33567D-2R2	2.5V, 2.5V	2500 Tape&Reel

MC33567

MAXIMUM RATINGS

Parameter	Symbol	Max Value	Unit
Supply Voltage	V_{CC}	12.5	Vdc
Operating Ambient Temperature	T_a	0 to +80	°C
Operating Junction Temperature	T_J	-5 to +125	°C
Lead Temperature (Soldering, 10 seconds)	T_L	300	°C
Storage Temperature Range	T_{stg}	-55 to +150	°C
Package Thermal Resistance, Junction to Ambient	$R_{\theta JA}^1$	180	°C/W

DEVICE MARKING

Device	Type	Package	Marking (1st Line)
MC33567-1	1.818 V, 1.515 V	SO-8	M5671
MC33567-2	2.525 V, 2.525 V	SO-8	M5672

PIN ASSIGNMENTS AND FUNCTIONS

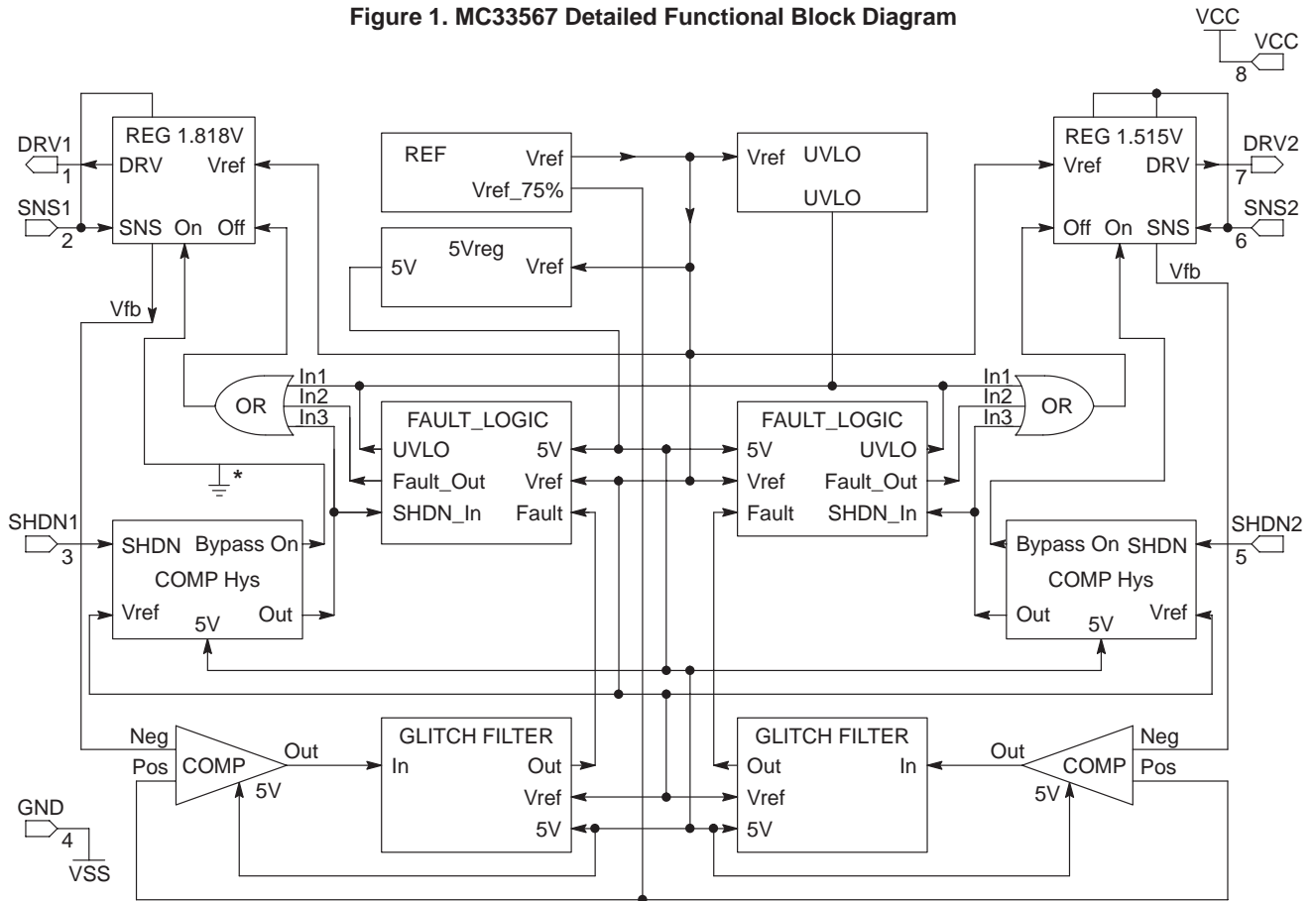
PIN #	PIN NAME	PIN DESCRIPTION
1	Gate 1 drive	Drives mosfet in linear region. Is internally clamped to ground in power down mode.
2	Sense 1 line	Returns regulated output from mosfet.
3	Shutoff 1	At TTL high level turns off regulation for gate 1. Effectively grounds gate 1. (Internal pullup to 3.3V)
4	Ground	
5	Shutoff 2	At TTL high level turns off regulation for gate 2. Effectively grounds gate 2. (Internal pullup to 3.3V)
6	Sense 2 line	Returns regulated output from mosfet.
7	Gate 2 drive	Drives mosfet in linear region. Is internally clamped to ground in power down mode.
8	12 volt input	Supply voltage for operation and gate drive output.

ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Min	Typ	Max	Unit
Output Voltage Regulation (Full-load to no-load @ 25 – 70°C)	$V_{reg}\%$	-2.5	—	+2.5	%
Peak Gate Drive Output (pin 1, pin 7)	I_{pkdrv}	10	20	30	mA
Drive Sink Current (steady state)	I_{sink}	5.0	7.0	10	mA
Short Circuit / Undervoltage Detect (load current increased until output drops)	ss/uvd	70	—	80	% V_o
Quiescent Current	I_q	—	7	10	mA
Under Voltage Lock Out	UVLO	7.0	8.5	9.0	V
Hysteresis	hys	0.2	0.5	0.9	V
Shutoff Threshold (Lower)	SHDN	0.8	1.13	1.29	V
Shutoff Hysteresis	$SHDN_{hys}$	—	130	—	mV
Short Circuit Response Time	SC_{td}	—	250	—	μS
Short Circuit Off Time	SC_{toff}	20	40	60	mS
Short Circuit On Time	SC_{ton}	0.5	0.8	1.5	mS
Shutoff Disable Time	$SHDN_{tdis}$	—	0.5	2.0	μS

MC33567

Figure 1. MC33567 Detailed Functional Block Diagram



* Internal ground disables Bypass On Function on the 1.8V regulator in the MC33567-1 and on the 2.5V regulators of the MC33567-2.

FUNCTIONAL DESCRIPTION

Overcurrent Protection – Hiccup Mode

On detection of overcurrent, output goes into hiccup mode where on period is 40 times shorter than off time. I.e., 1.0 msec ON, 40 msec OFF. When an overcurrent condition exists, the output voltage will drop below the threshold. The

output is then turned on and off in a 1:40 duty cycle. Each transition low to high of the enable input restarts the hiccup mode holdoff period.

Shutoff (Shutdown) Function

Each internal regulator has an active high enable input. If the input is held above the minimum threshold, the regulator

will operate normally. If the input is held low, the regulator is turned off.

Logic table for Shutoff (Pin 3) on the 1.5V regulator:*

Shutoff Pin	1.5V Regulator Output
No Connect	1.5V
< 0.8V	Shutoff
2.0V < SHDN < 4.2V	1.5V
> 4.1V	3.3V – Full ON

Logic table for Shutoff (Pin 3) on the 1.8V regulator:

Shutoff Pin	1.8V Regulator Output
No Connect	1.8V
< 0.8V	Shutoff
> 2.0V	1.8V

*See Figure 4, 1.5V / 3.3V AGP card detection

NOTE: MC33567-2 does not have full-on bypass feature

This part has under voltage detection that uses the channel resistance of an internal N-channel FET to put the regulator into “hiccup mode” when a short is present on the regulated

voltage plane. Under voltage detection is set to ~75% of regulation set point.

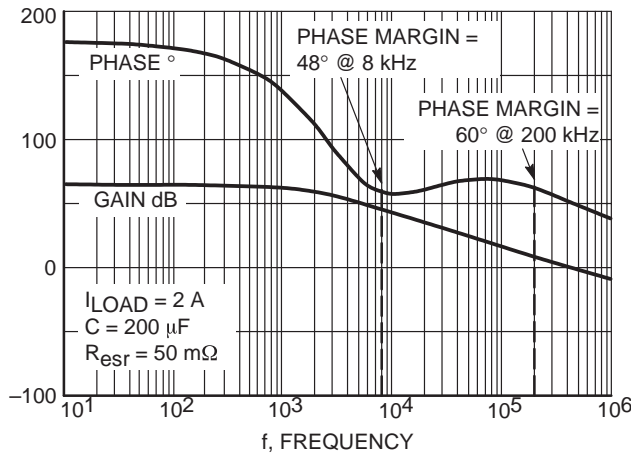


Figure 2. Gain-Phase Plot @ 50 mΩ

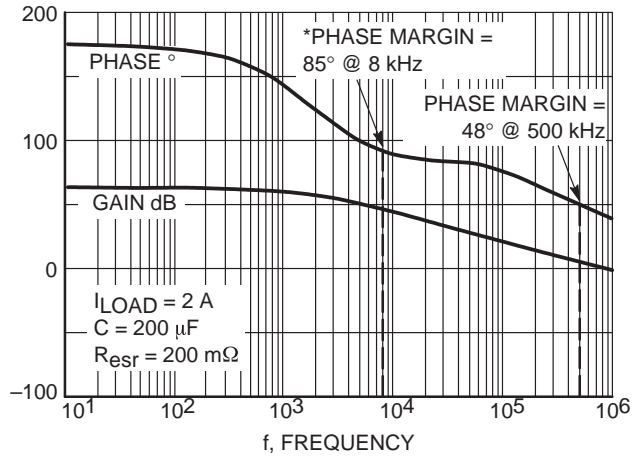


Figure 3. Gain-Phase Plot @ 200 mΩ

*NOTE: For adequate phase margin, $C \times R \geq 10 \times 10^{-6}$.
 E.g. $200 \mu\text{F} \times 50 \text{ m}\Omega = 10 \times 10^{-6}$,
 $400 \mu\text{F} \times 25 \text{ m}\Omega = 10 \times 10^{-6}$,
 $800 \mu\text{F} \times 12.5 \text{ m}\Omega = 10 \times 10^{-6}$.

Capacitor Selection Guidelines

The goal here is to preserve adequate phase margin for stable operation. For adequate phase margin, the load capacitance ESR value multiplied by the load capacitance must be greater than 10×10^{-6} . For example, if the load capacitance is $400 \mu\text{F}$, then the ESR value of the capacitor would need to be no less than 25 milliOhms, ($400 \mu\text{F} \times 25 \text{ m}\Omega = 10 \times 10^{-6}$). Similarly, if the load capacitance was $200 \mu\text{F}$, then the ESR value of the capacitance would need to be at least 50 milliOhms, ($200 \mu\text{F} \times 50 \text{ m}\Omega = 10 \times 10^{-6}$). **(Important Note:** The foregoing rule assumes that all capacitors across the load are of the same type and value. If different types and values of capacitors are used in parallel across the load, then each individual capacitors must meet the $C \times \text{ESR} > 10 \times 10^{-6}$ rule).

PCB Layout Guidelines

The goal here is to minimize extraneous signals from being either magnetically or electrostatically induced on the sense lines or drive lines. As much as practical, the LDO control ic should be physically close (short traces) to the external series pass transistors; the layout of the sense trace should parallel, go in the same direction, and be on the same plane as the power trace going from the series pass transistor source lead to the load; routing the sense lead near the load current return path should be avoided; unterminated runs of the sense lead should be avoided (if options on sense lead destinations are desired on the board, then use zero ohm resistor jumpers to make the alternate sense lead connections near the sense pin itself).

PIN 5 TRUTH TABLE

- Pin 5 No connect = 1.5V LDO drive out active
- Pin 5 < 0.8V = shutoff (drive out 0V)
- 2.5V < pin 5 < 4.1V = 1.5V LDO drive out active
- Pin 5 > 4.1V = 3.3V bypass mode (drive out = V_{CC})

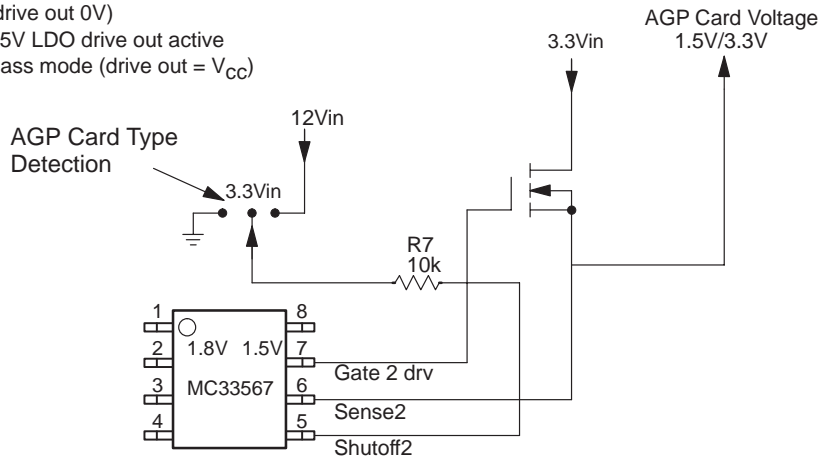
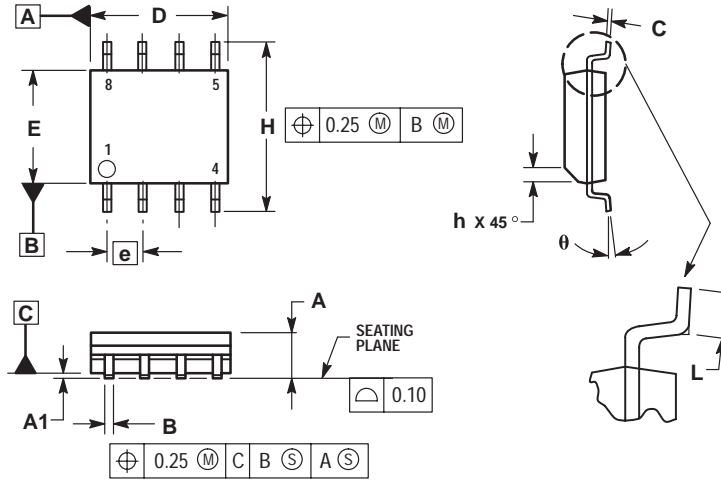


Figure 4. 1.5V/3.3V AGP card detection

MC33567

PACKAGE DIMENSIONS

SO-8
D SUFFIX
PLASTIC SOIC PACKAGE
CASE 751-06
ISSUE T




NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. DIMENSIONS ARE IN MILLIMETER.
3. DIMENSION D AND E DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 PER SIDE.
5. DIMENSION B DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 TOTAL IN EXCESS OF THE B DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS	
	MIN	MAX
A	1.35	1.75
A1	0.10	0.25
B	0.35	0.49
C	0.19	0.25
D	4.80	5.00
E	3.80	4.00
e	1.27 BSC	
H	5.80	6.20
h	0.25	0.50
L	0.40	1.25
θ	0°	7°

Notes

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer.

PUBLICATION ORDERING INFORMATION

North America Literature Fulfillment:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: ONlit@hibbertco.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada

EUROPE: LDC for ON Semiconductor – European Support

German Phone: (+1) 303-308-7140 (M-F 2:30pm to 5:00pm Munich Time)
Email: ONlit-german@hibbertco.com
French Phone: (+1) 303-308-7141 (M-F 2:30pm to 5:00pm Toulouse Time)
Email: ONlit-french@hibbertco.com
English Phone: (+1) 303-308-7142 (M-F 1:30pm to 5:00pm UK Time)
Email: ONlit@hibbertco.com

ASIA/PACIFIC: LDC for ON Semiconductor – Asia Support

Phone: 303-675-2121 (Tue-Fri 9:00am to 1:00pm, Hong Kong Time)
Toll Free from Hong Kong 800-4422-3781
Email: ONlit-asia@hibbertco.com

JAPAN: ON Semiconductor, Japan Customer Focus Center
4-32-1 Nishi-Gotanda, Shinagawa-ku, Tokyo, Japan 141-8549

Phone: 81-3-5740-2745
Email: r14525@onsemi.com

Fax Response Line: 303-675-2167
800-344-3810 Toll Free USA/Canada

ON Semiconductor Website: <http://onsemi.com>

For additional information, please contact your local
Sales Representative.