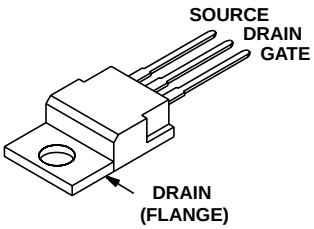
Data Sheet | March 2000 | File Number 4843

# 22A, 100V, 0.064 Ohm, N-Channel Power MOSFET

## Packaging

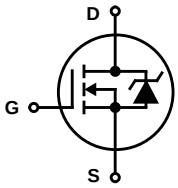
JEDEC TO-220AB




## Features

- Ultra Low On-Resistance
  - $r_{DS(ON)} = 0.064\Omega$, $V_{GS} = 10V$
- Simulation Models
  - Temperature Compensated PSPICE™ and SABER© Electrical Models
  - Spice and SABER© Thermal Impedance Models
  - www.intersil.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve

## Symbol




## Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| IRF530N | TO-220AB | IRF530N |

## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | IRF530N | UNITS |
|---|---|---|---|
| Drain to Source Voltage (Note 1) | $V_{DSS}$ | 100 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ) (Note 1) | $V_{DGR}$ | 100 | V |
| Gate to Source Voltage | $V_{GS}$ | ±20 | V |
| Drain Current | | | |
| Continuous ($T_C$= 25°C, $V_{GS}$ = 10V) (Figure 2) | $I_D$ | 22 | A |
| Continuous ($T_C$= 100°C, $V_{GS}$ = 10V) (Figure 2) | $I_D$ | 15 | A |
| Pulsed Drain Current | $I_{DM}$ | Figure 4 | |
| Pulsed Avalanche Rating | UIS | Figures 6, 14, 15 | |
| Power Dissipation | $P_D$ | 85 | W |
| Derate Above 25°C | | 0.57 | W/°C |
| Operating and Storage Temperature | $T_J$, $T_{STG}$ | -55 to 175 | °C |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | °C |
| Package Body for 10s, See Techbrief TB334 | $T_{pkg}$ | 260 | °C |

NOTES:

1. $T_J$ = 25°C to 150°C.

***CAUTION:*** *Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| **OFF STATE SPECIFICATIONS** | | | | | | | |
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 250µA, $V_{GS}$ = 0V (Figure 11) | | 100 | - | - | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 95V, $V_{GS}$ = 0V | | - | - | 1 | µA |
| | | $V_{DS}$ = 90V, $V_{GS}$ = 0V, $T_C = 150^oC$ | | - | - | 250 | µA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20V | | - | - | ±100 | nA |
| **ON STATE SPECIFICATIONS** | | | | | | | |
| Gate to Source Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250µA (Figure 10) | | 2 | - | 4 | V |
| Drain to Source On Resistance | $r_{DS(ON)}$ | $I_D$ = 22A, $V_{GS}$ = 10V (Figure 9) | | - | 0.054 | 0.064 | Ω |
| **THERMAL SPECIFICATIONS** | | | | | | | |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | TO-220 | | - | - | 1.76 | $^oC/W$ |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | | | - | - | 62 | $^oC/W$ |
| **SWITCHING SPECIFICATIONS** ($V_{GS}$ = 10V) | | | | | | | |
| Turn-On Time | $t_{ON}$ | $V_{DD}$ = 50V, $I_D$ = 22A<br>$V_{GS}$ = 10V,<br>$R_{GS}$ = 13Ω<br>(Figures 18, 19) | | - | - | 75 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | | - | 7.9 | - | ns |
| Rise Time | $t_r$ | | | - | 42 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 47 | - | ns |
| Fall Time | $t_f$ | | | - | 39 | - | ns |
| Turn-Off Time | $t_{OFF}$ | | | - | - | 130 | ns |
| **GATE CHARGE SPECIFICATIONS** | | | | | | | |
| Total Gate Charge | $Q_{g(TOT)}$ | $V_{GS}$ = 0V to 20V | $V_{DD}$ = 50V,<br>$I_D$ = 22A,<br>$I_{g(REF)}$ = 1.0mA<br>(Figures 13, 16, 17) | - | 43 | 52 | nC |
| Gate Charge at 10V | $Q_{g(10)}$ | $V_{GS}$ = 0V to 10V | | - | 23 | 28 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS}$ = 0V to 2V | | - | 1.7 | 2 | nC |
| Gate to Source Gate Charge | $Q_{gs}$ | | | - | 3.5 | - | nC |
| Gate to Drain "Miller" Charge | $Q_{gd}$ | | | - | 8.7 | - | nC |
| **CAPACITANCE SPECIFICATIONS** | | | | | | | |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = 25V, $V_{GS}$ = 0V,<br>f = 1MHz<br>(Figure 12) | | - | 790 | - | pF |
| Output Capacitance | $C_{OSS}$ | | | - | 215 | - | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | - | 70 | - | pF |

## Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Source to Drain Diode Voltage | $V_{SD}$ | $I_{SD}$ = 22A | - | - | 1.25 | V |
| | | $I_{SD}$ = 11A | - | - | 1.00 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_{SD}$ = 22A, $dI_{SD}/dt$ = 100A/µs | - | - | 100 | ns |
| Reverse Recovered Charge | $Q_{RR}$ | $I_{SD}$ = 22A, $dI_{SD}/dt$ = 100A/µs | - | - | 313 | nC |

## Typical Performance Curves

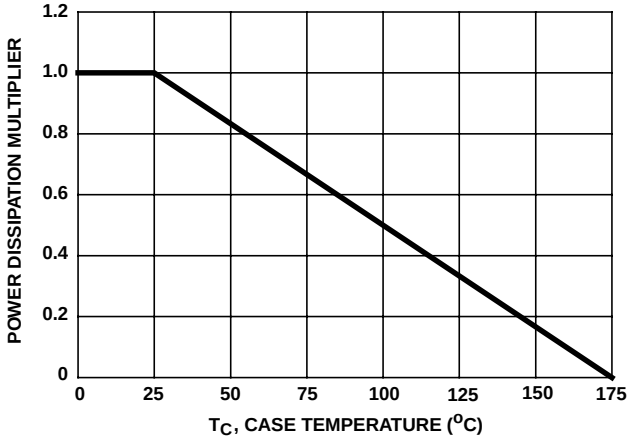



FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

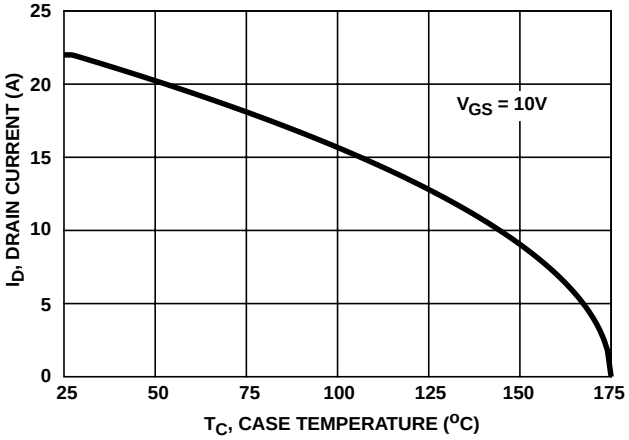



FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

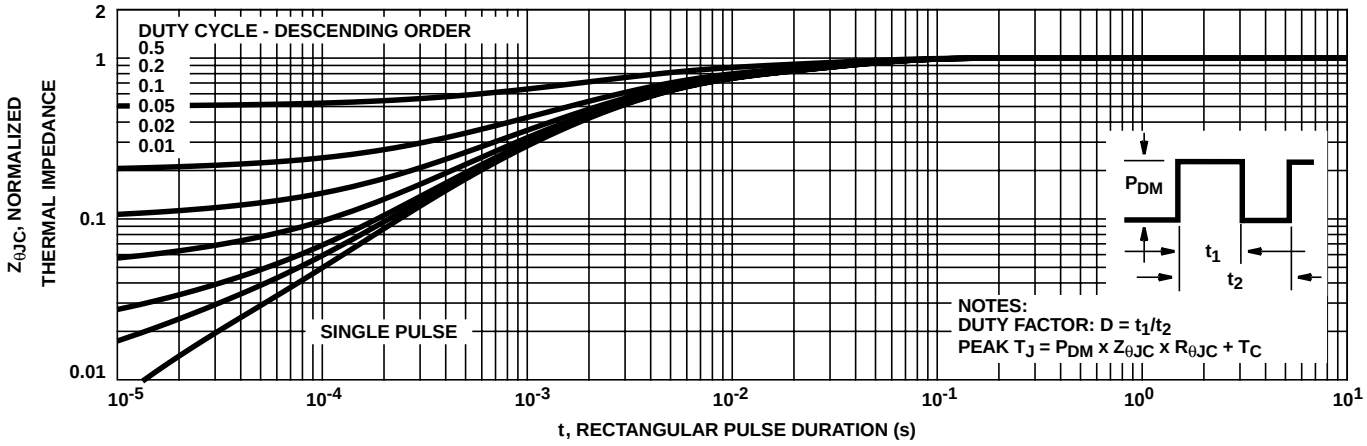



FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

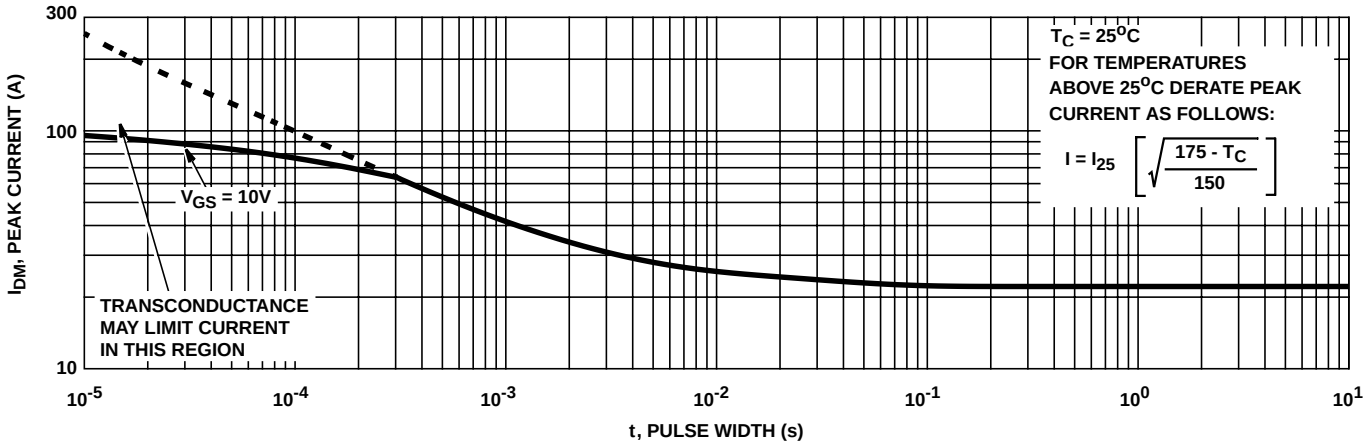



FIGURE 4. PEAK CURRENT CAPABILITY

## Typical Performance Curves (Continued)

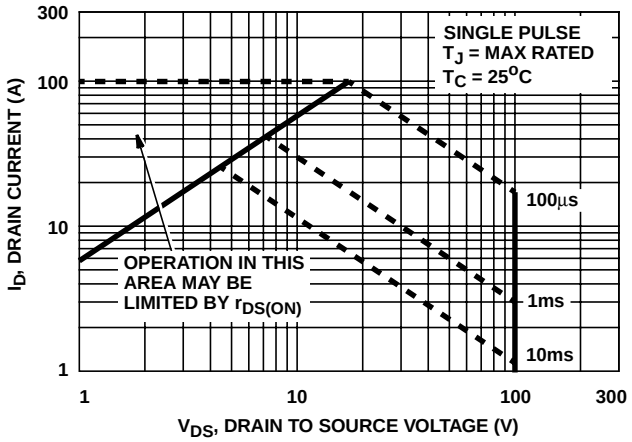
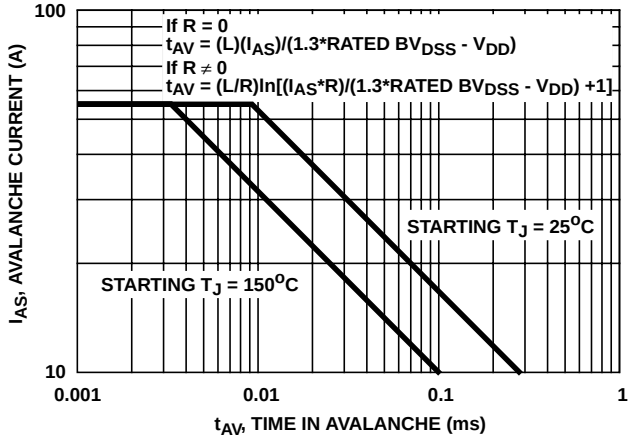



FIGURE 5. FORWARD BIAS SAFE OPERATING AREA




NOTE: Refer to Intersil Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

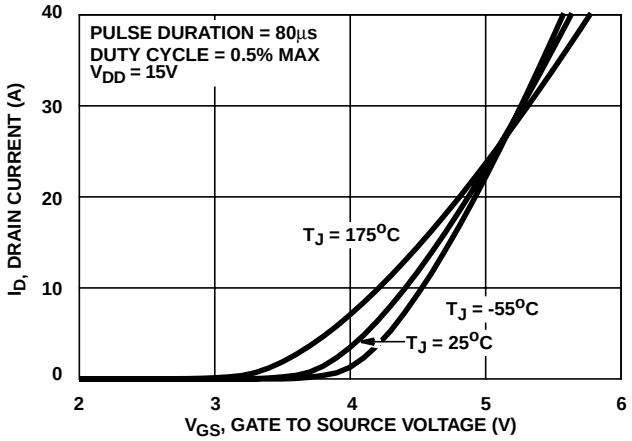



FIGURE 7. TRANSFER CHARACTERISTICS

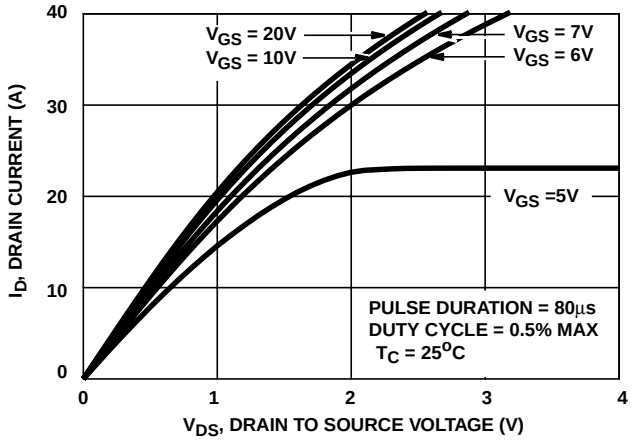



FIGURE 8. SATURATION CHARACTERISTICS

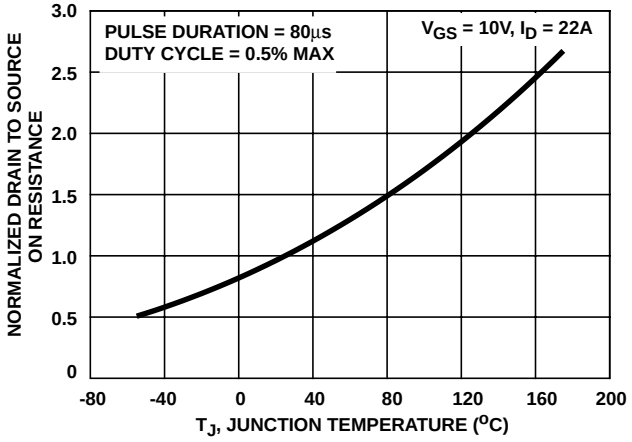



FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

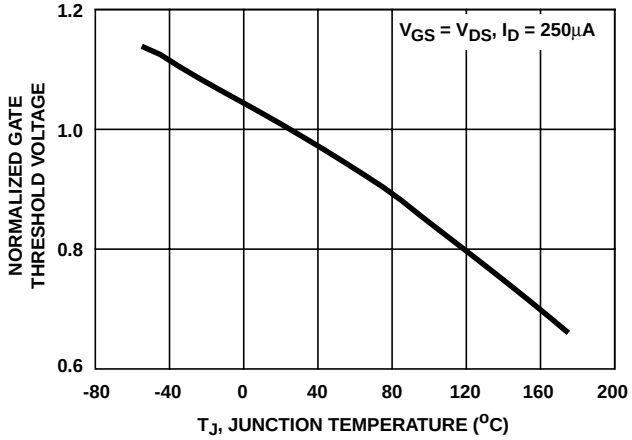



FIGURE 10. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

## Typical Performance Curves (Continued)

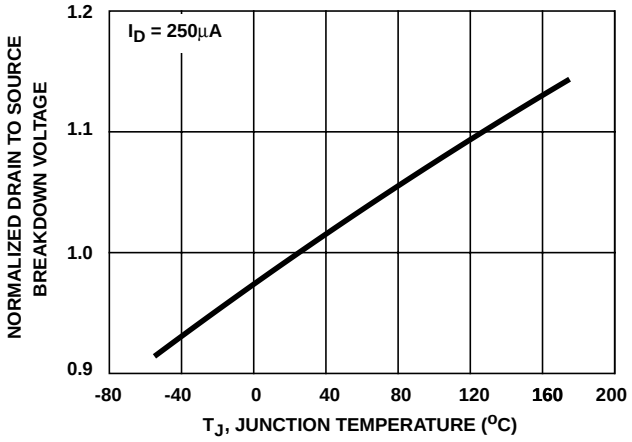



FIGURE 11. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

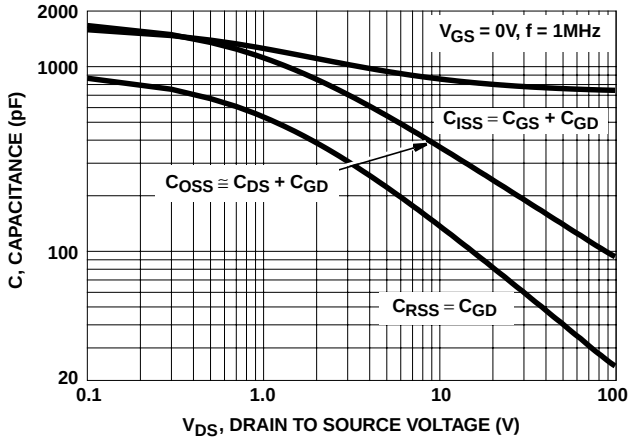
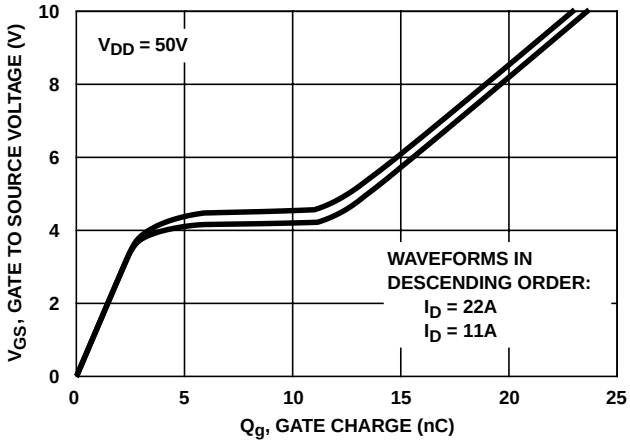



FIGURE 12. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE




NOTE: Refer to Intersil Application Notes AN7254 and AN7260.

FIGURE 13. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

## Test Circuits and Waveforms

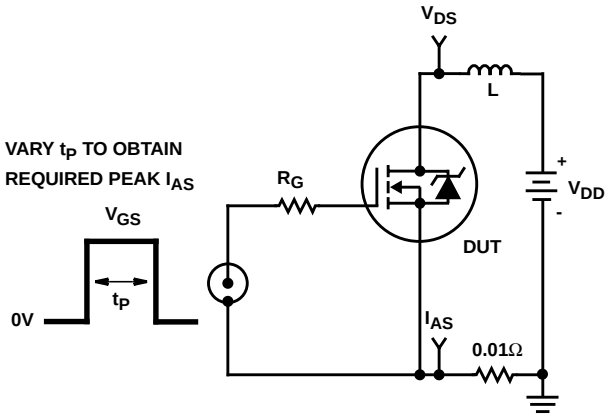



FIGURE 14. UNCLAMPED ENERGY TEST CIRCUIT

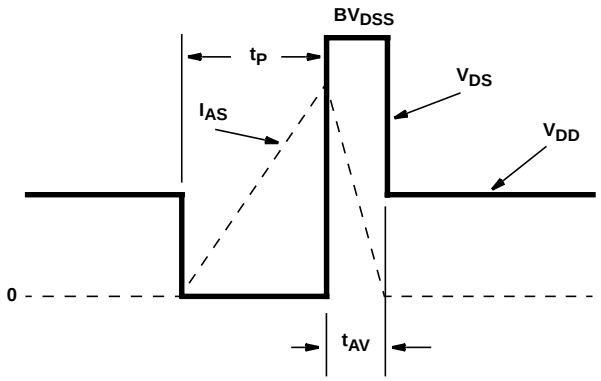



FIGURE 15. UNCLAMPED ENERGY WAVEFORMS

## Test Circuits and Waveforms (Continued)

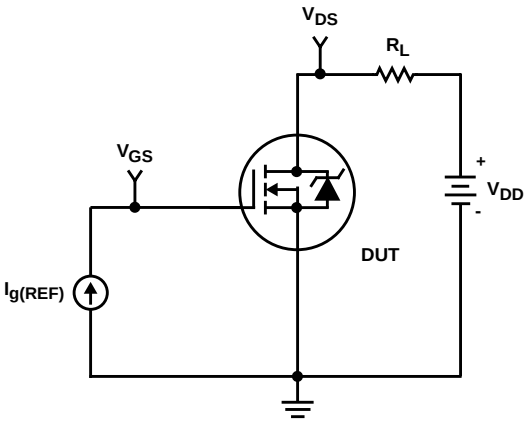



FIGURE 16. GATE CHARGE TEST CIRCUIT

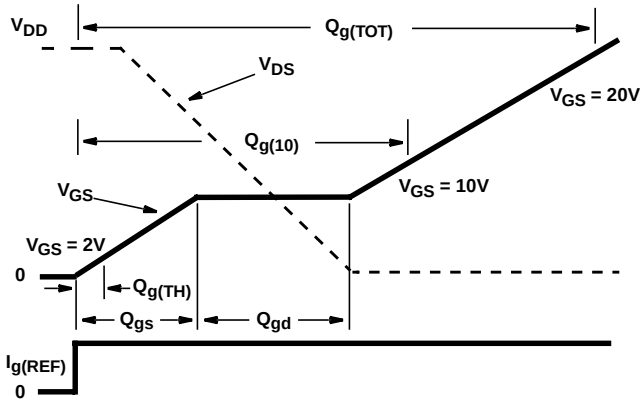



FIGURE 17. GATE CHARGE WAVEFORMS

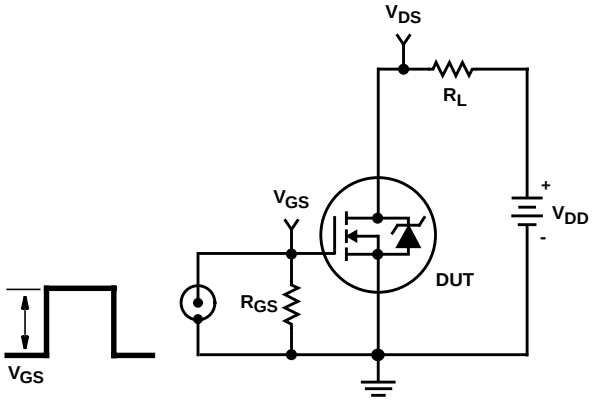



FIGURE 18. SWITCHING TIME TEST CIRCUIT

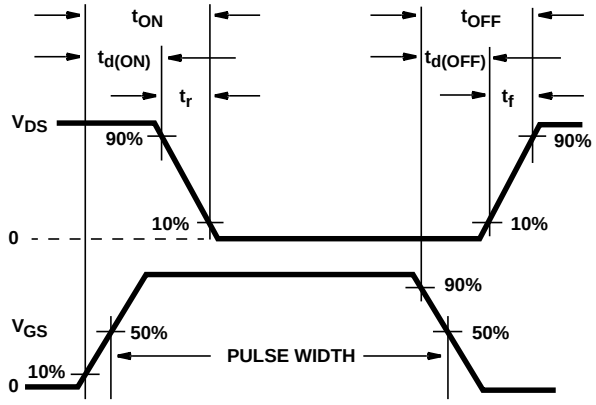



FIGURE 19. SWITCHING TIME WAVEFORM

## PSPICE Electrical Model

.SUBCKT IRF530N 2 1 3 ;  rev 15 Jan 2000

CA 12 8 1.27e-9
CB 15 14 1.27e-9
CIN 6 8 7.20e-10

DBODY 7 5 DBODYMOD
DBREAK 5 11 DBREAKMOD
DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 117.8
EDS 14 8 5 8 1
EGS 13 8 6 8 1
ESG 6 10 6 8 1
EVTHRES 6 21 19 8 1
EVTEMP 20 6 18 22 1

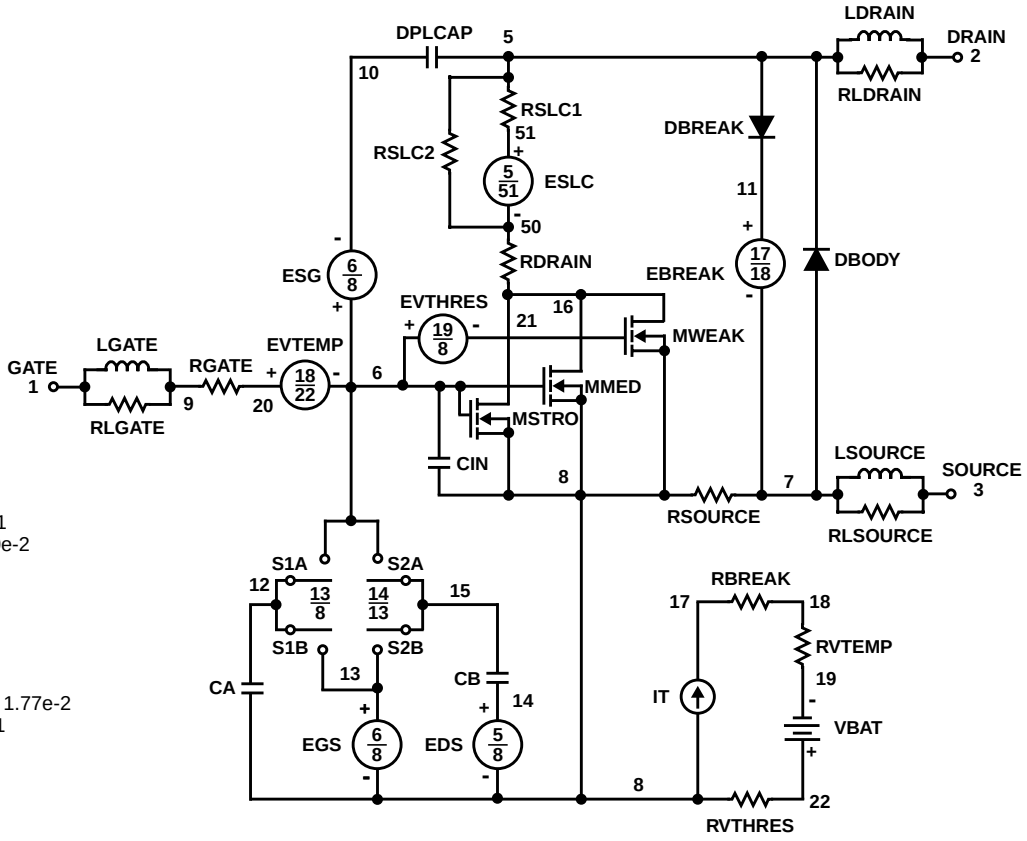
IT 8 17 1

LDRAIN 2 5 1.0e-9
LGATE 1 9 5.53e-9
LSOURCE 3 7 4.35e-9

MMED 16 6 8 8 MMEDMOD
MSTRO 16 6 8 8 MSTROMOD
MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1
RDRAIN 50 16 RDRAINMOD 2.70e-2
RGATE 9 20 2.50
RLDRAIN 2 5 10
RLGATE 1 9 55.3
RLSOURCE 3 7 43.5
RSLC1 5 51 RSLCMOD 1e-6
RSLC2 5 50 1e3
RSOURCE 8 7 RSOURCEMOD 1.77e-2
RVTHRES 22 8 RVTHRESMOD 1
RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD
S1B 13 12 13 8 S1BMOD
S2A 6 15 14 13 S2AMOD
S2B 13 15 14 13 S2BMOD




VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))*(PWR(V(5,51)/(1e-6*43.5),3.5))}

.MODEL DBODYMOD D (IS = 6.0e-13 RS = 6.2e-3 XTI = 5.5 TRS1 = 2.1e-3 TRS2 = 2.0e-6 CJO = 8.50e-10 TT = 6.30e-8 M = 0.54)
.MODEL DBREAKMOD D (RS = 5.6e-1 TRS1 = 8e-4 TRS2 = 3e-6)
.MODEL DPLCAPMOD D (CJO = 9.29e-10 IS = 1e-30 M = 0.79)
.MODEL MMEDMOD NMOS (VTO = 3.21 KP = 5 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 2.50)
.MODEL MSTROMOD NMOS (VTO = 3.60 KP = 37 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)
.MODEL MWEAKMOD NMOS (VTO = 2.77 KP = 0.09 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 25.0 )
.MODEL RBREAKMOD RES (TC1 =1.05e-3 TC2 = -5e-7)
.MODEL RDRAINMOD RES (TC1 = 1.20e-2 TC2 = 3.00e-5)
.MODEL RSLCMOD RES (TC1 = 3.20e-3 TC2 = 3.00e-6)
.MODEL RSOURCEMOD RES (TC1 = 1e-3 TC2 = 1e-6)
.MODEL RVTHRESMOD RES (TC1 = -2.20e-3 TC2 = -9.00e-6)
.MODEL RVTEMPMOD RES (TC1 = -2.40e-3 TC2 =1.80e-6)

.MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.2 VOFF= -3.1)
.MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -3.1 VOFF= -6.2)
.MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.0 VOFF= 0.5)
.MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF= -1.0)

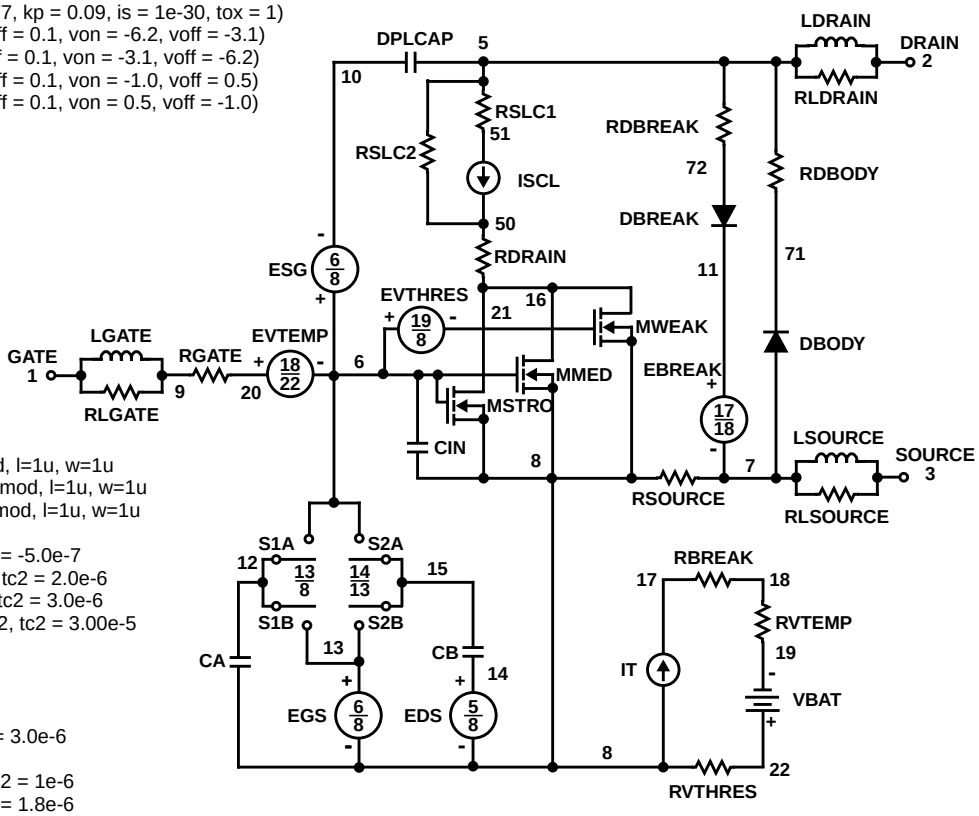
.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.

## SABER Electrical Model

REV 15 Jan 2000

```
template IRF530N n2,n1,n3
electrical n2,n1,n3
{
var i iscl
d..model dbodymod =  (is = 6.00e-13, cjo = 8.50e-10, tt = 6.30e-8, xti = 5.5, m = 0.54)
d..model dbreakmod = ()
d..model dplcapmod =  (cjo = 9.29e-10, is = 1e-30, m = 0.79)
m..model mmedmod = (type=_n, vto = 3.21, kp = 5, is = 1e-30, tox = 1)
m..model mstrongmod = (type=_n, vto = 3.60, kp = 37, is = 1e-30, tox = 1)
m..model mweakmod = (type=_n, vto = 2.77, kp = 0.09, is = 1e-30, tox = 1)
sw_vcsp..model s1amod =  (ron = 1e-5, roff = 0.1, von = -6.2, voff = -3.1)
sw_vcsp..model s1bmod =  (ron =1e-5, roff = 0.1, von = -3.1, voff = -6.2)
sw_vcsp..model s2amod =  (ron = 1e-5, roff = 0.1, von = -1.0, voff = 0.5)
sw_vcsp..model s2bmod =  (ron = 1e-5, roff = 0.1, von = 0.5, voff = -1.0)

c.ca n12 n8 = 1.27e-9
c.cb n15 n14 = 1.27e-9
c.cin n6 n8 = 7.20e-10

d.dbody n7 n71 = model=dbodymod
d.dbreak n72 n11 = model=dbreakmod
d.dplcap n10 n5 = model=dplcapmod

i.it n8 n17 = 1

l.ldrain n2 n5 = 1e-9
l.lgate n1 n9 = 5.53e-9
l.lsource n3 n7 = 4.35e-9

m.mmed n16 n6 n8 n8 = model=mmedmod, l=1u, w=1u
m.mstrong n16 n6 n8 n8 = model=mstrongmod, l=1u, w=1u
m.mweak n16 n21 n8 n8 = model=mweakmod, l=1u, w=1u

res.rbreak n17 n18  = 1, tc1 = 1.05e-3, tc2 = -5.0e-7
res.rdbody n71 n5 = 6.2e-3, tc1 = 2.10e-3, tc2 = 2.0e-6
res.rdbreak n72 n5 = 5.6e-1, tc1 = 8.0e-4, tc2 = 3.0e-6
res.rdrain n50 n16  = 2.70e-2, tc1 = 1.20e-2, tc2 = 3.00e-5
res.rgate n9 n20 = 2.50
res.rldrain n2 n5 = 10
res.rlgate n1 n9 = 55.3
res.rlsource n3 n7 = 43.5
res.rslc1 n5 n51  = 1e-6, tc1 = 3.2e-3, tc2 = 3.0e-6
res.rslc2 n5 n50 = 1e3
res.rsource n8 n7  = 1.77e-2, tc1 = 1e-3, tc2 = 1e-6
res.rvtemp n18 n19  = 1, tc1 = -2.4e-3, tc2 = 1.8e-6
res.rvthres n22 n8  = 1, tc1 = -2.2e-3, tc2 = -9.0e-6

spe.ebreak n11 n7 n17 n18 = 117.8
spe.eds n14 n8 n5 n8 = 1
spe.egs n13 n8 n6 n8 = 1
spe.esg n6 n10 n6 n8 = 1
spe.evtemp n20 n6 n18 n22 = 1
spe.evthres n6 n21 n19 n8 = 1

sw_vcsp.s1a n6 n12 n13 n8 = model=s1amod
sw_vcsp.s1b n13 n12 n13 n8 = model=s1bmod
sw_vcsp.s2a n6 n15 n14 n13 = model=s2amod
sw_vcsp.s2b n13 n15 n14 n13 = model=s2bmod

v.vbat n22 n19 = dc=1

equations {
i (n51->n50) +=iscl
iscl: v(n51,n50) = ((v(n5,n51)/(1e-9+abs(v(n5,n51))))*((abs(v(n5,n51)*1e6/43.5))** 3.5))
}
}
```



## SPICE Thermal Model

REV 15 Jan 2000

IRF530NT

CTHERM1 th 6 1.40e-3
CTHERM2 6 5 5.55e-3
CTHERM3 5 4 5.65e-3
CTHERM4 4 3 6.10e-3
CTHERM5 3 2 9.80e-3
CTHERM6 2 tl 7.70e-2

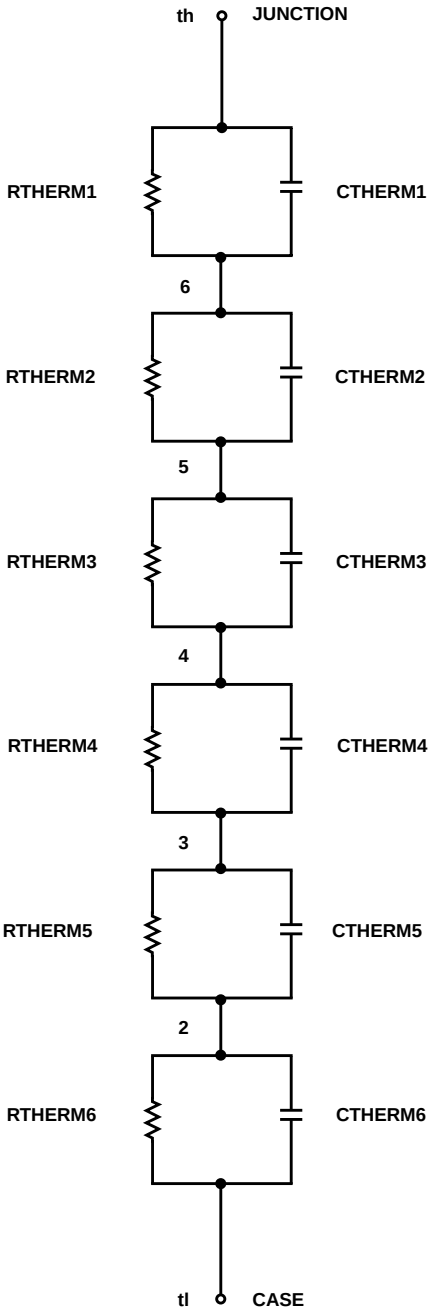
RTHERM1 th 6 1.10e-2
RTHERM2 6 5 5.80e-2
RTHERM3 5 4 1.35e-1
RTHERM4 4 3 3.60e-1
RTHERM5 3 2 4.13e-1
RTHERM6 2 tl 4.30e-1

## SABER Thermal Model

SABER thermal model IRF530NT

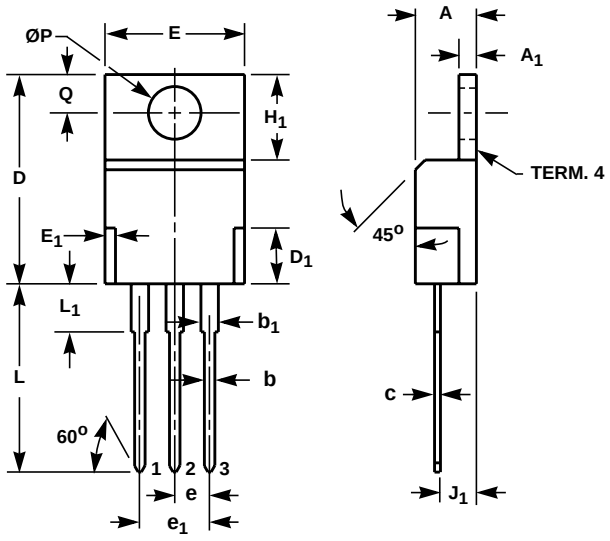
template thermal_model th tl
thermal_c th, tl
{
ctherm.ctherm1 th 6 = 1.40e-3
ctherm.ctherm2 6 5 = 5.55e-3
ctherm.ctherm3 5 4 = 5.65e-3
ctherm.ctherm4 4 3 = 6.10e-3
ctherm.ctherm5 3 2 = 9.80e-3
ctherm.ctherm6 2 tl = 7.70e-2

rtherm.rtherm1 th 6 = 1.10e-2
rtherm.rtherm2 6 5 = 5.80e-2
rtherm.rtherm3 5 4 = 1.35e-1
rtherm.rtherm4 4 3 = 3.60e-1
rtherm.rtherm5 3 2 = 4.13e-1
rtherm.rtherm6 2 tl = 4.30e-1
}



## TO-220AB

**3 LEAD JEDEC TO-220AB PLASTIC PACKAGE**




| SYMBOL | INCHES | | MILLIMETERS | | NOTES |
|---|---|---|---|---|---|
| | MIN | MAX | MIN | MAX | |
| A | 0.170 | 0.180 | 4.32 | 4.57 | - |
| $A_1$ | 0.048 | 0.052 | 1.22 | 1.32 | - |
| b | 0.030 | 0.034 | 0.77 | 0.86 | 3, 4 |
| $b_1$ | 0.045 | 0.055 | 1.15 | 1.39 | 2, 3 |
| c | 0.014 | 0.019 | 0.36 | 0.48 | 2, 3, 4 |
| D | 0.590 | 0.610 | 14.99 | 15.49 | - |
| $D_1$ | - | 0.160 | - | 4.06 | - |
| E | 0.395 | 0.410 | 10.04 | 10.41 | - |
| $E_1$ | - | 0.030 | - | 0.76 | - |
| e | 0.100 TYP | | 2.54 TYP | | 5 |
| $e_1$ | 0.200 BSC | | 5.08 BSC | | 5 |
| $H_1$ | 0.235 | 0.255 | 5.97 | 6.47 | - |
| $J_1$ | 0.100 | 0.110 | 2.54 | 2.79 | 6 |
| L | 0.530 | 0.550 | 13.47 | 13.97 | - |
| $L_1$ | 0.130 | 0.150 | 3.31 | 3.81 | 2 |
| ØP | 0.149 | 0.153 | 3.79 | 3.88 | - |
| Q | 0.102 | 0.112 | 2.60 | 2.84 | - |

NOTES:

1. These dimensions are within allowable dimensions of Rev. J of JEDEC TO-220AB outline dated 3-24-87.
2. Lead dimension and finish uncontrolled in $L_1$.
3. Lead dimension (without solder).
4. Add typically 0.002 inches (0.05mm) for solder coating.
5. Position of lead to be measured 0.250 inches (6.35mm) from bottom of dimension D.
6. Position of lead to be measured 0.100 inches (2.54mm) from bottom of dimension D.
7. Controlling dimension: Inch.
8. Revision 2 dated 7-97.



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