1 PRODUCT OVERVIEW

OVERVIEW

The S3C72N8/C72N5 single-chip CMOS microcontroller has been designed for high performance using Samsung's newest 4-bit CPU core, SAM47 (Samsung Arrangeable Microcontrollers).

With features such as LCD direct drive capability, 8-bit timer/counter, and serial I/O, the S3C72N8/C72N5 offer an excellent design solution for a wide variety of applications that require LCD functions.

Up to 40 pins of the 80-pin QFP package can be dedicated to I/O. Six vectored interrupts provide fast response to internal and external events. In addition, the S3C72N8/C72N5's advanced CMOS technology provides for low power consumption and a wide operating voltage range.

OTP

The S3C72N8/C72N5 microcontroller is also available in OTP (One Time Programmable) version, S3P72N8/P72N5. S3P72N8/P72N5 microcontroller has an on-chip 8/16-Kbyte one-time-programmable EPROM instead of masked ROM. The S3P72N8/P72N5 is comparable to S3C72N8/C72N5, both in function and in pin configuration.

FEATURES

Memory

- 512 × 4-bit RAM
- 8 K × 8-bit ROM (S3C72N8/P72N8)
- 16 K × 8-bit ROM (S3C72N5/P72N5)

I/O Pins

- Input only: 8 pins
- I/O: 24 pins
- Output: 8 pins sharing with segment driver outputs

LCD Controller/Driver

- Maximum 16-digit LCD direct drive capability
- 32 segment, 4 common pins
- Display modes: Static, 1/2 duty (1/2 bias), 1/3 duty (1/2 or 1/3 bias), 1/4 duty (1/3 bias)

8-Bit Basic Timer

- Programmable interval timer
- Watchdog timer

8-Bit Timer/Counter 0

- Programmable 8-bit timer
- External event counter
- Arbitrary clock frequency output
- Serial I/O interface clock generator

Watch Timer

- Real-time and interval time measurement
- Four frequency outputs to BUZ pin
- Clock source generation for LCD

8-Bit Serial I/O Interface

- 8-bit transmit/receive mode
- 8-bit receive only mode
- LSB-first or MSB-first transmission selectable
- Internal or external clock source

Bit Sequential Carrier

- Support 16-bit serial data transfer in arbitrary format

Interrupts

- Three internal vectored interrupts
- Three external vectored interrupts
- Two quasi-interrupts

Memory-Mapped I/O Structure

- Data memory bank 15

Two Power-Down Modes

- Idle mode (only CPU clock stops)
- Stop mode (main or sub system oscillation stops)

Oscillation Sources

- Crystal, ceramic, or RC for main system clock
- Crystal or external oscillator for subsystem clock
- Main system clock frequency: 4.19 MHz (typical)
- Subsystem clock frequency: 32.768 kHz
- CPU clock divider circuit (by 4, 8, or 64)

Instruction Execution Times

- 0.95, 1.91, 15.3 μs at 4.19 MHz (main)
- 122 μs at 32.768 kHz (subsystem)

Operating Temperature

- – 40 °C to 85 °C

Operating Voltage Range

- 1.8 V to 5.5 V

Package Type

- 80-pin QFP

BLOCK DIAGRAM

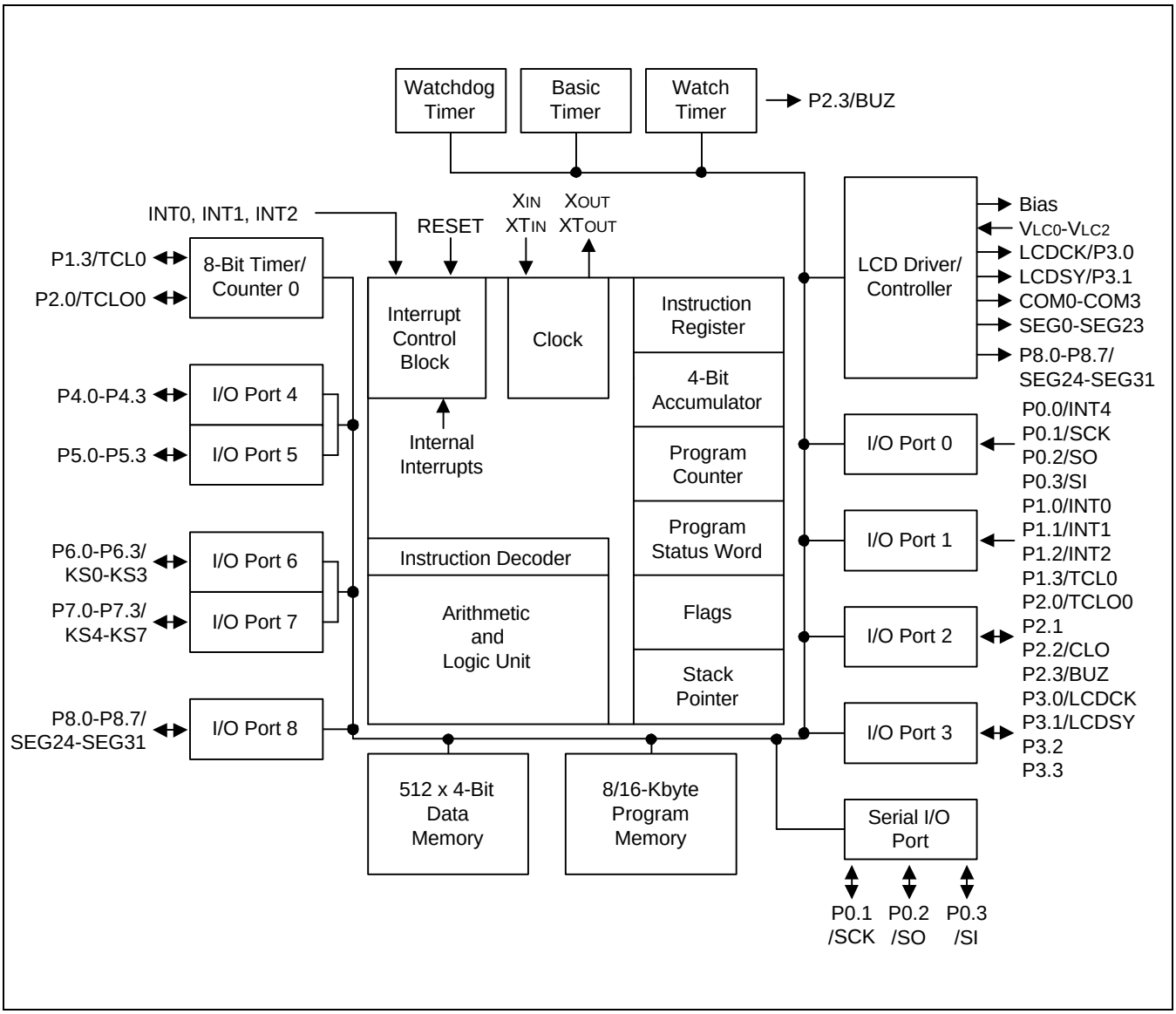


Figure 1-1. S3C72N8/C72N5 Simplified Block Diagram

PIN ASSIGNMENTS

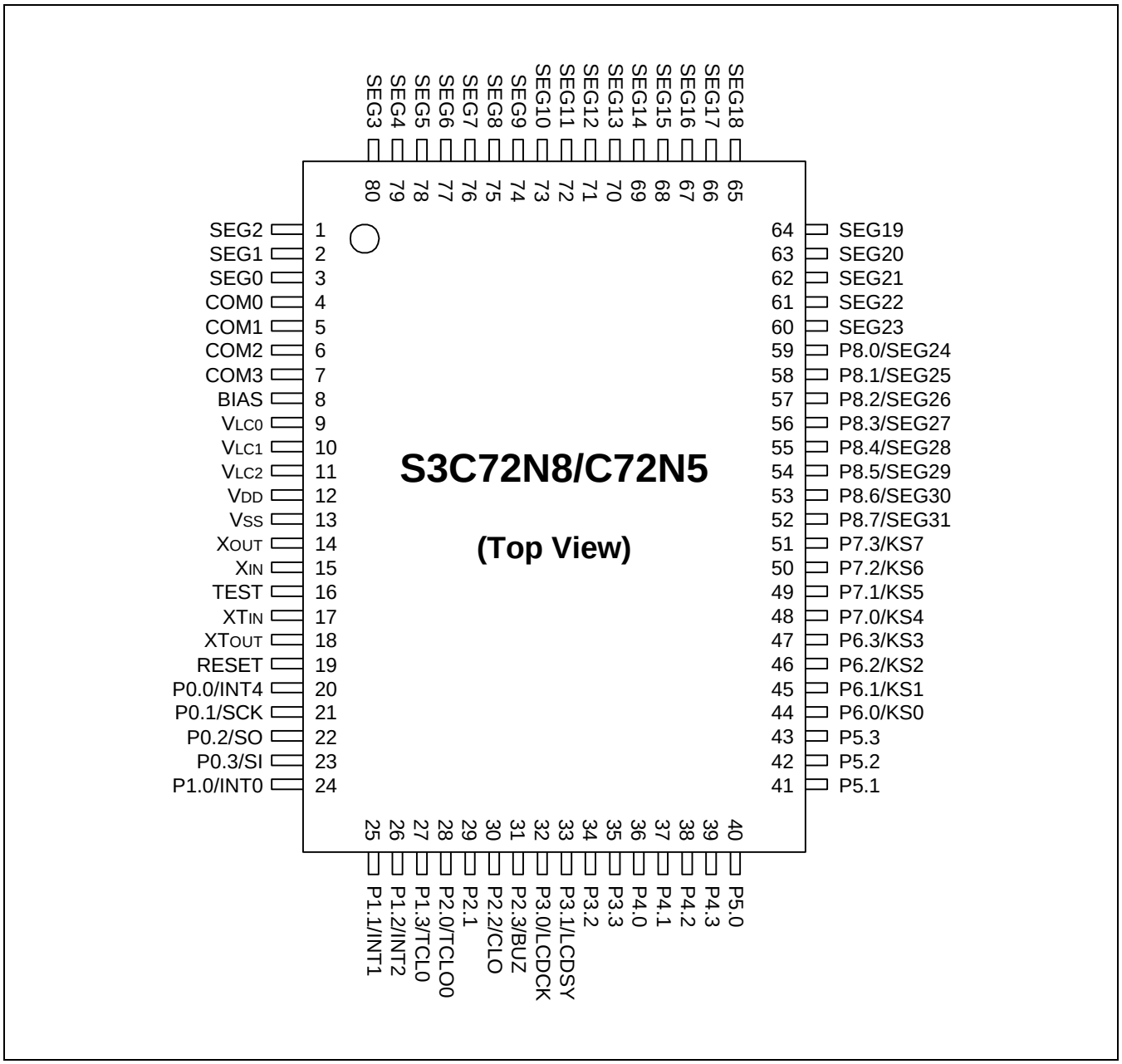


Figure 1-2. S3C72N8/C72N5 80-QFP Pin Assignment Diagram

PIN DESCRIPTIONS

Table 1-1. S3C72N8/C72N5 Pin Descriptions

Pin Name	Pin Type	Description	Number	Share Pin	Reset Value	Circuit Type
P0.0 P0.1 P0.2 P0.3	I I/O I/O I	4-bit input port. 1-bit and 4-bit read and test are possible. 4-bit pull-up resistors are software assignable.	20 21 22 23	INT4 SCK SO SI	Input	A-1 D * D * A-1
P1.0 P1.1 P1.2 P1.3	I	4-bit input port. 1-bit and 4-bit read and test are possible. 4-bit pull-up resistors are software assignable.	24 25 26 27	INT0 INT1 INT2 TCL0	Input	A-1
P2.0 P2.1 P2.2 P2.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test are possible. 4-bit pull-up resistors are software assignable.	28 29 30 31	TCLO0 – CLO BUZ	Input	D
P3.0 P3.1 P3.2 P3.3	I/O	4-bit I/O port. 1-bit and 4-bit read/write and test are possible. Each individual pin can be specified as input or output. 4-bit pull-up resistors are software assignable.	32 33 34 35	LCDCK LCDSY	Input	D
P4.0– P4.3 P5.0– P5.3	I/O	4-bit I/O ports. N-channel open-drain output up to 5 V. 1-, 4-, and 8-bit read/write and test are possible. Ports 4 and 5 can be paired to support 8-bit data transfer. 4-bit pull-up resistors are software assignable.	36–43	–	Input	E
P6.0– P6.3 P7.0– P7.3	I/O	4-bit I/O ports. Port 6 pins are individually software configurable as input or output. 1-bit and 4-bit read/write and test are possible. 4-bit pull-up resistors are software assignable. Ports 6 and 7 can be paired to enable 8-bit data transfer.	44–51	KS0–KS3 KS4–KS7	Input	D *
P8.0– P8.7	O	Output port for 1-bit data (for use as CMOS driver only)	59–52	SEG24– SEG31	Output	H-16
SEG0– SEG23	O	LCD segment signal output	3–1, 80–60	–	Output	H-15
SEG24– SEG31	O	LCD segment signal output	59–52	P8.0–P8.7	Output	H-16
COM0– COM3	O	LCD common signal output	4–7	–	Output	H-15
V_{LC0}–V_{LC2}	–	LCD power supply. Voltage dividing resistors are assignable by mask option	9–11	SCLK SDAT	–	–
BIAS	–	LCD power control	8	–	–	–
LCDCK	I/O	LCD clock output for display expansion	32	P3.0	Input	D

Table 1-1. S3C72N8/C72N5 Pin Descriptions (Continued)

Pin Name	Pin Type	Description	Number	Share Pin	Reset Value	Circuit Type
LCDSY	I/O	LCD synchronization clock output for LCD display expansion	33	P3.1	Input	D
TCL0	I/O	External clock input for timer/counter 0	27	P1.3	Input	A-1
TCLO0	I/O	Timer/counter 0 clock output	28	P2.0	Input	D
SI	I	Serial interface data input	23	P0.3	Input	A-1
SO	I/O	Serial interface data output	22	P0.2	Input	D *
SCK	I/O	Serial I/O interface clock signal	21	P0.1	Input	D *
INT0 INT1	I	External interrupts. The triggering edge for INT0 and INT1 is selectable. Only INT0 is synchronized with the system clock.	24 25	P1.0 P1.1	Input	A-1
INT2	I	Quasi-interrupt with detection of rising edge signals.	26	P1.2	Input	A-1
INT4	I	External interrupt input with detection of rising or falling edge	20	P0.0	Input	A-1
KS0–KS7	I/O	Quasi-interrupt inputs with falling edge detection.	44–51	P6.0–P7.3	Input	D *
CLO	I/O	CPU clock output	30	P2.2	Input	D
BUZ	I/O	2, 4, 8 or 16 kHz frequency output for buzzer sound with 4.19 MHz main system clock or 32.768 kHz subsystem clock.	31	P2.3	Input	D
X_{IN}, X_{OUT}	–	Crystal, ceramic or RC oscillator pins for main system clock. (For external clock input, use X_{IN} and input X_{IN}'s reverse phase to X_{OUT})	15,14	–	–	–
XT_{IN}, XT_{OUT}	–	Crystal oscillator pins for subsystem clock. (For external clock input, use XT_{IN} and input XT_{IN}'s reverse phase to XT_{OUT})	17,18	–	–	–
V_{DD}	–	Main power supply	12	–	–	–
V_{SS}	–	Ground	13	–	–	–
RESET	–	Reset signal	19	–	Input	B
TEST	–	Test signal input (must be connected to V_{SS})	16	–	–	–

NOTES:

1. Pull-up resistors for all I/O ports are automatically disabled if they are configured to output mode.
2. D * Type has a schmitt trigger circuit at input.

PIN CIRCUIT DIAGRAMS

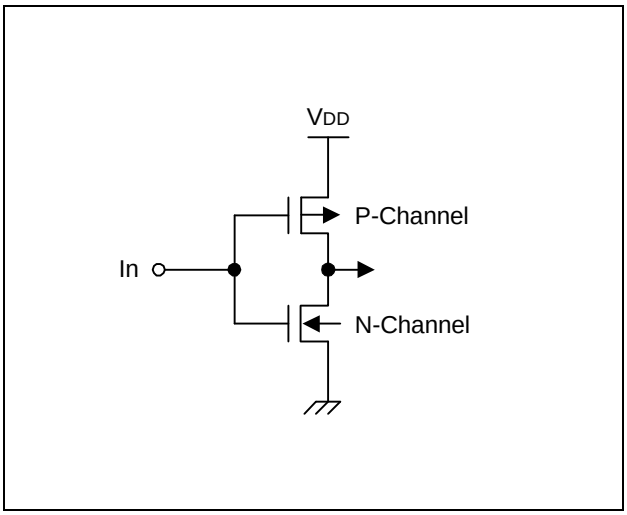


Figure 1-3. Pin Circuit Type A

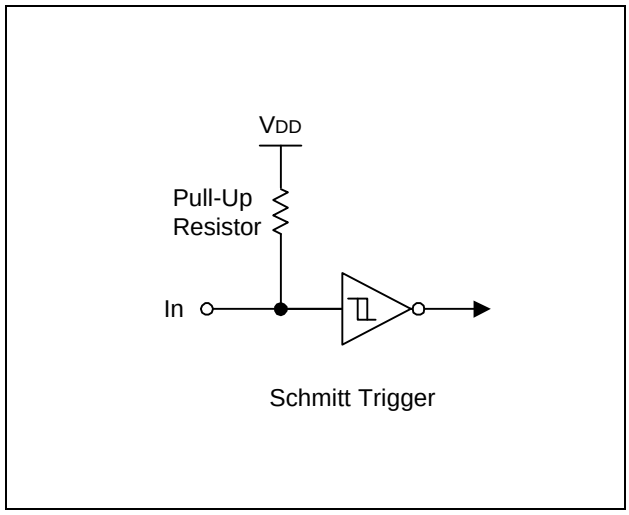


Figure 1-5. Pin Circuit Type B (RESET)

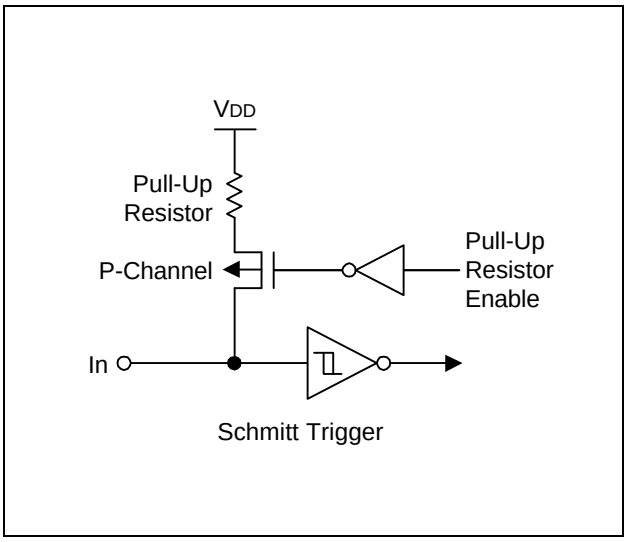


Figure 1-4. Pin Circuit Type A-1 (P1, P0.0, P0.3)

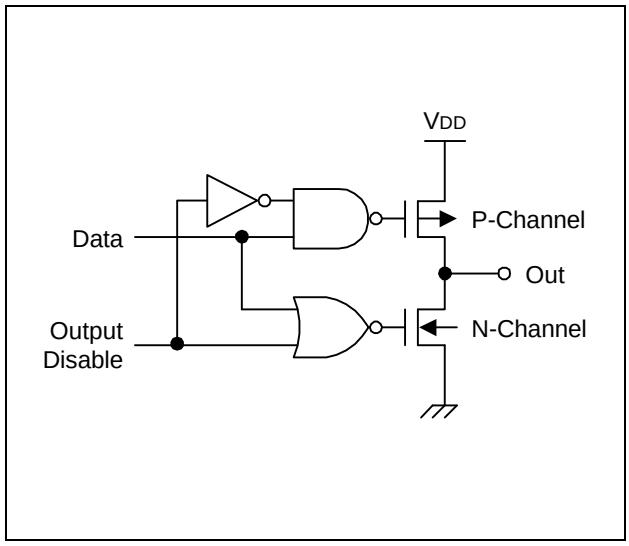


Figure 1-6. Pin Circuit Type C

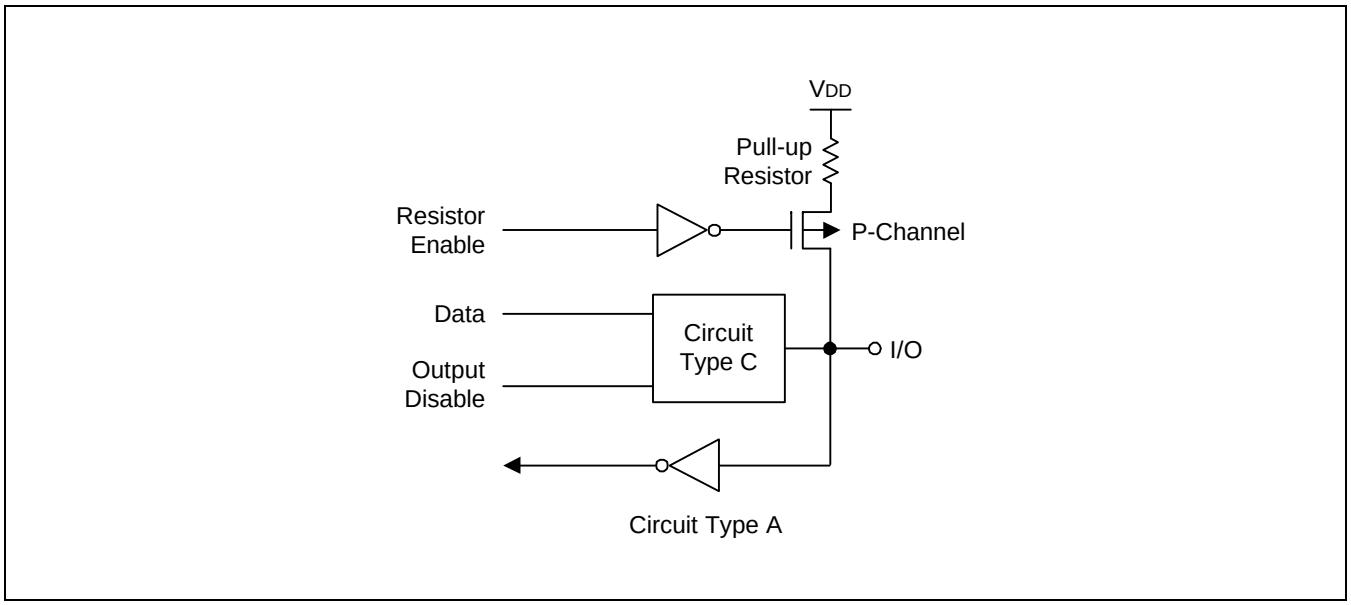


Figure 1-7. Pin Circuit Type D (P0.1, P0.2, P2, P3, P6, P7)

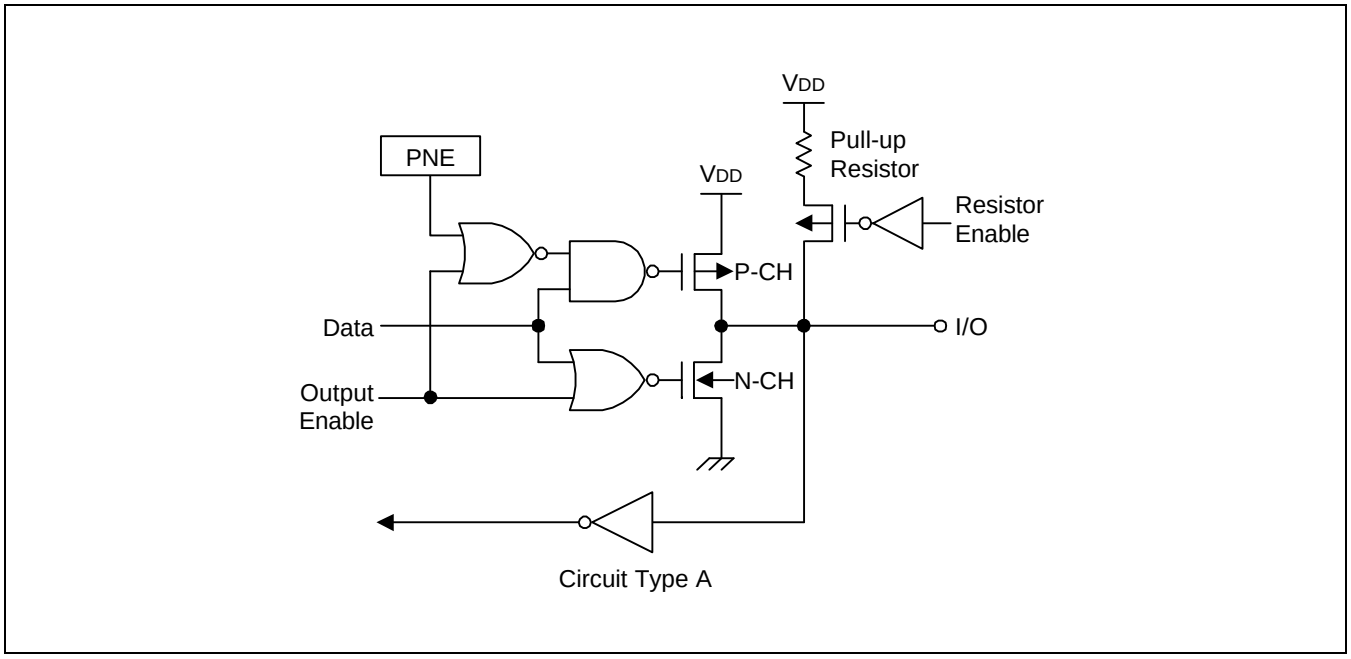


Figure 1-8. Pin Circuit Type E (P4, P5)

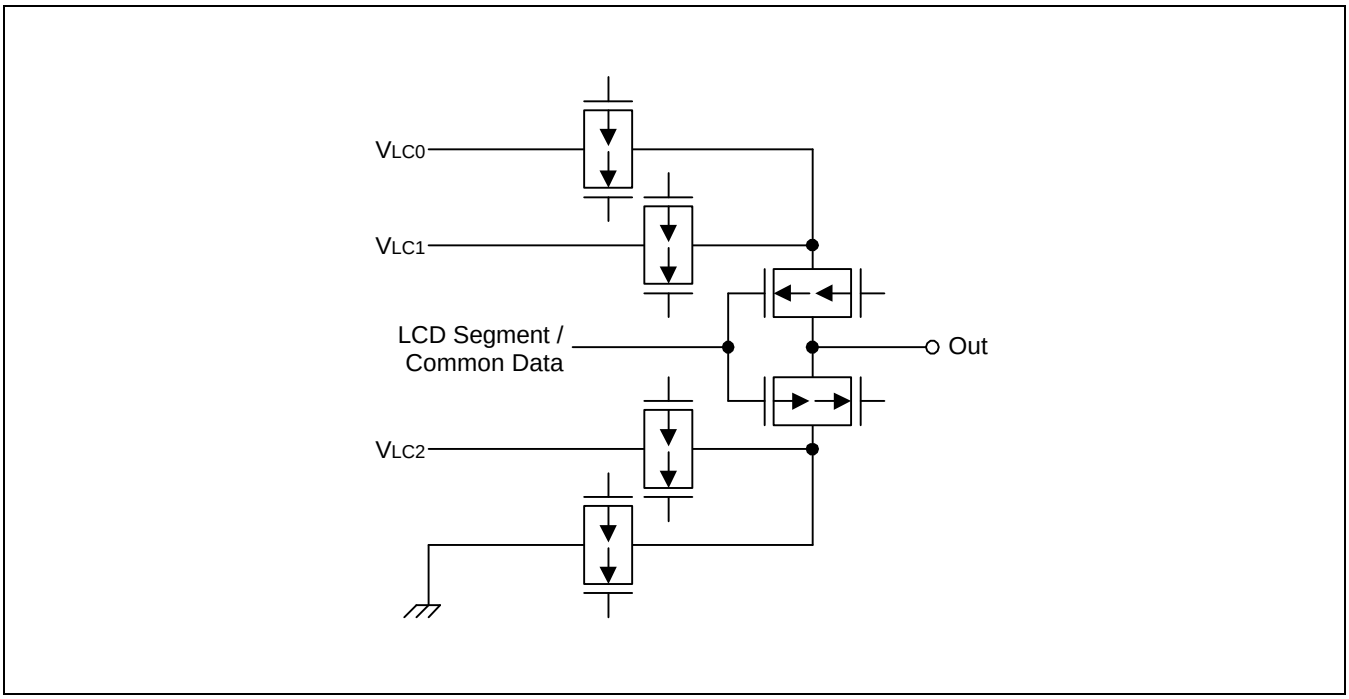


Figure 1-9. Pin Circuit Type H-15 (SEG/COM)

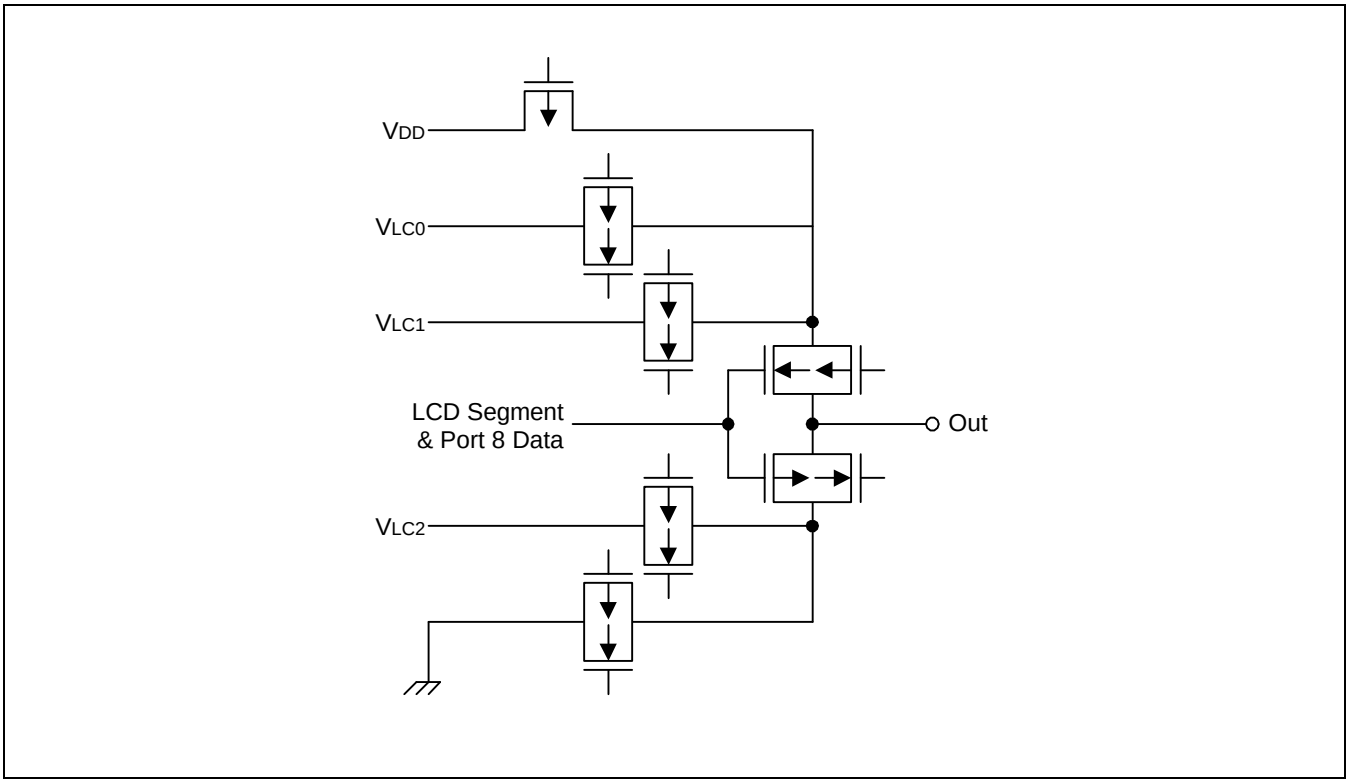


Figure 1-10. Pin Circuit Type H-16 (P8)

NOTES

14 ELECTRICAL DATA

OVERVIEW

In this section, information on S3C72N8/C72N5 electrical characteristics is presented as tables and graphics. The information is arranged in the following order:

Standard Electrical Characteristics

— Absolute maximum ratings
— D.C. electrical characteristics
— Main system clock oscillator characteristics
— Subsystem clock oscillator characteristics
— I/O capacitance
— A.C. electrical characteristics
— Operating voltage range

Miscellaneous Timing Waveforms

— A.C timing measurement point
— Clock timing measurement at X_{IN}
— Clock timing measurement at XT_{IN}
— TCL timing
— Input timing for RESET
— Input timing for external interrupts
— Serial data transfer timing

Stop Mode Characteristics and Timing Waveforms

— RAM data retention supply voltage in stop mode
— Stop mode release timing when initiated by RESET
— Stop mode release timing when initiated by an interrupt request

Table 14-1. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_I	All I/O ports	– 0.3 to V_{DD} + 0.3	
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	
Output Current High	I_{OH}	One I/O pin active	– 15	mA
		All I/O ports active	– 35	
Output Current Low	I_{OL}	One I/O pin active	+ 30 (Peak value)	
			+ 15 (note)	
		Total value for ports 0, 2, 3, and 5	+ 100 (Peak value)	
			+ 60 (note)	
		Total value for ports 4, 6, and 7	+ 100	
			+ 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 14-2. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH1}	All input pins except those specified below for V_{IH2}, V_{IH3}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7 and RESET	0.8 V_{DD}	–	V_{DD}	
	V_{IH3}	X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}	V_{DD} – 0.1	–	V_{DD}	
Input low voltage	V_{IL1}	Ports 2, 3, 4 and 5	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7 and RESET	–	–	0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}	–	–	0.1	
Output high voltage	V_{OH1}	V_{DD} = 4.5 V to 5.5 V Ports 0, 2, 3, 4, 5, 6, 7 and BIAS I_{OH} = – 1 mA	V_{DD} – 1.0	–	–	V
	V_{OH2}	V_{DD} = 4.5 V to 5.5 V Port 8 ONLY I_{OH} = – 100 µA	V_{DD} – 2.0	–	–	

Table 14-2. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output low voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V, Ports 0, 2–7 I_{OL} = 15 mA	–	0.4	2	V
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V, Port 8 only I_{OL} = 100 µA	–	–	1	
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}	–	–	20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}	–	–	– 3	
	I_{LIL2}	V_{IN} = 0 V X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}			– 20	
Output high leakage current	I_{LOH1}	V_{OUT} = V_{DD} All output pins	–	–	3	µA
Output low leakage current	I_{LOL}	V_{OUT} = 0 V All output pins			– 3	
Pull-up resistor	R_{L1}	Ports 0–7 V_{IN} = 0 V; V_{DD} = 5 V	25	47	100	KΩ
		V_{DD} = 3 V	50	95	200	
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V, RESET	100	220	400	
		V_{DD} = 3 V	200	450	800	
LCD voltage dividing resistor	R_{LCD}	T_A = 25 °C	50	93	140	
COM output impedance	R_{COM}	V_{DD} = 5 V	–	3	6	
		V_{DD} = 3 V		5	15	
SEG output impedance	R_{SEG}	V_{DD} = 5 V		3	6	
		V_{DD} = 3 V		5	15	
COM output voltage deviation	VDC	V_{DD} = 5 V (V_{LC0} – COMi) Io = ± 15uA (I = 0–3)	–	± 45	± 90	mV
SEG output voltage deviation	VDS	V_{DD} = 5 V (V_{LC0}-SEGi) Io = ± 15µA (I = 0–31)	–	ñ 45	ñ 90	mV

Table 14-2. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

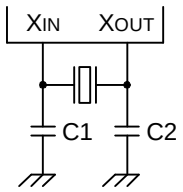
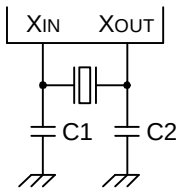
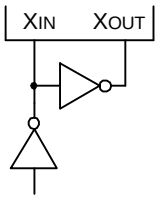
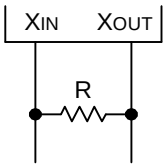
Parameter	Symbol	Conditions		Min	Typ	Max	Units
V_{LC0} Output voltage	V_{LC0}	T_A = 25 øC		0.6 V_{DD} _ 0.2	0.6 V_{DD}	0.6 V_{DD} + 0.2	V
V_{LC1} Output voltage	V_{LC1}	T_A = 25 øC		0.4 V_{DD} – 0.2	0.4 V_{DD}	0.4 V_{DD} + 0.2	
V_{LC2} Output voltage	V_{LC2}	T_A = 25 øC		0.2 V_{DD} – 0.2	0.2 V_{DD}	0.2 V_{DD} + 0.2	
Supply Current (1)	I_{DD1} (2)	Main operating: V_{DD} = 5 V ± 10% CPU = fx/4 SCMOD = 0000B crystal oscillator C1 = C2 = 22pF	6.0 MHz 4.19 MHz	–	3.5 2.5	8 5.5	mA
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		1.6 1.2	4 3	
	I_{DD2} (2)	Main Idle mode; V_{DD} = 5 V ± 10% CPU = fx/4 SCMOD = 0000B crystal oscillator C1 = C2 = 22pF	6.0 MHz 4.19 MHz	–	1.0 0.9	2.5 2.0	
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		0.5 0.4	1.0 0.8	
	I_{DD3}	Sub operating: V_{DD} = 3 V ± 10% CPU = fxt/4 SCMOD = 1001B 32 kHz crystal oscillator		–	15	30	µA
	I_{DD4}	Sub Idle mode; V_{DD} = 3 V ± 10% CPU = fxt/4, SCMOD = 1001B 32 kHz crystal oscillator		–	6	15	
	I_{DD5}	Stop mode; V_{DD} = 5 V ± 10%, XT_{IN} = 0 V CPU = fxt/4, SCMOD = 0000B		–	2.5	5	
	I_{DD6} (3)	Stop mode; V_{DD} = 5 V ± 10% CPU = fx/4, SCMOD = 0100B		–	0.5	3	

NOTES:

1. D.C. electrical values for supply current (I_{DD1} to I_{DD6}) do not include current drawn through internal pull-up resistors and through LCD voltage dividing resistors.
2. Data includes the power consumption for sub-system clock oscillation.
3. When the system clock mode register, SCMOD, is set to 0100B, the sub-system clock oscillation stops. The main-system clock oscillation stops by the STOP instruction.

Table 14-3. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

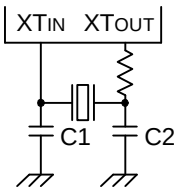
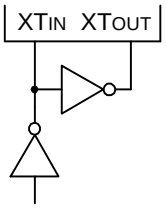
Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	V_{DD} = 4.5 V to 5.5 V	–	–	10	ms
			V_{DD} = 1.8 V to 4.5 V	–	–	30	
External Clock		X_{IN} input frequency (1)	–	0.4	–	6.0	MHz
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	–	ns
RC Oscillator		Frequency (1)	V_{DD} = 5 V R = 20 KΩ, V_{DD} = 5 V R = 38 KΩ, V_{DD} = 3 V	0.4	– 2.0 1.0	2	MHz

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when stop mode is terminated.

Table 14-4. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 4.5 V to 5.5 V	–	1.0	2	s
			V_{DD} = 1.8 V to 4.5 V	–	–	10	
External Clock		XT_{IN} input frequency (1)	–	32	–	100	kHz
		XT_{IN} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	µs

NOTES:
1. Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

Table 14-5. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output capacitance	C_{OUT}		–	–	15	pF
I/O capacitance	C_{IO}		–	–	15	pF

Table 14-6. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction cycle time (1)	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	0.95	–	64	
		With subsystem clock (fxt)	114	122	125	
TCL0 input frequency	f_{TI0}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5V			1	MHz
TCL0 input high, low width	t_{TIH0}, t_{TIL0}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8 V to 5.5 V	1.8			
SCK cycle time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	ns
		Internal SCK source	650			
		V_{DD} = 1.8 V to 5.5 V External SCK source	3200			
		Internal SCK source	3800			
SCK high, low width	t_{KH}, t_{KL}	V_{DD} = 1.8 V to 5.5 V External SCK source	400	–	–	ns
		Internal SCK source	$t_{KCY}/2 – 50$			
		V_{DD} = 1.8 V to 5.5 V External SCK source	1600			
		Internal SCK source	$t_{KCY}/2 – 150$			
SI setup time to SCK high	t_{SIK}	External SCK source	100	–	–	ns
		Internal SCK source	150			
SI hold time to SCK high	t_{KSI}	External SCK source	400	–	–	ns
		Internal SCK source	400			
Output delay for SCK to SO	t_{KSO}	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	ns
		Internal SCK source			250	
		V_{DD} = 1.8 V to 5.5 V External SCK source			1000	
		Internal SCK source			1000	
Interrupt input high, low width	t_{INTH}, t_{INTL}	INT0	(2)	–	–	µs
		INT1, INT2, INT4, KS0–KS7	10			
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTES:

1. Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fx as assigned by the IMOD0 register setting.

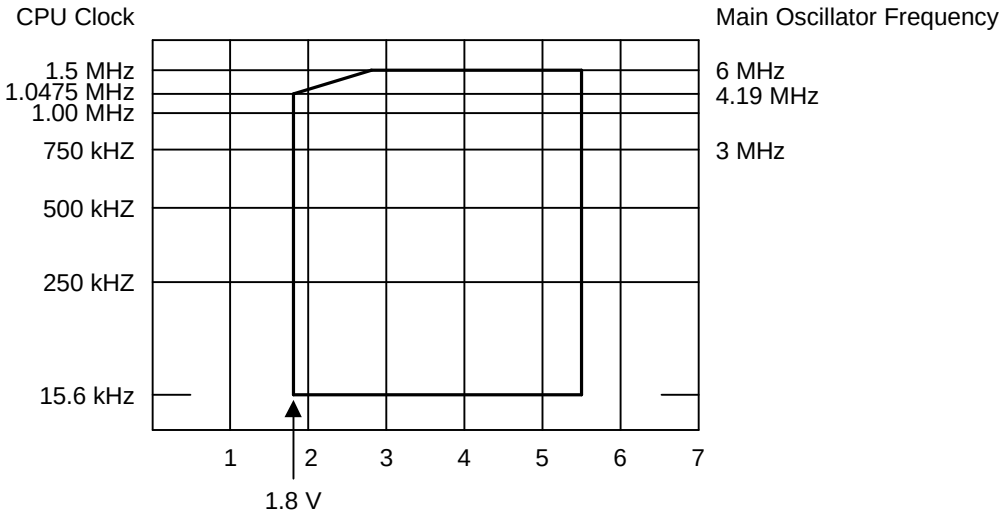


Figure 14-1. Standard Operating Voltage Range

Table 14-7. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	Normal operation	1.8	–	6.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	10	µA
Release signal set time	t_{SREL}	Normal operation	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17}/fx	–	ms
		Released by interrupt	–	(2)	–	

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

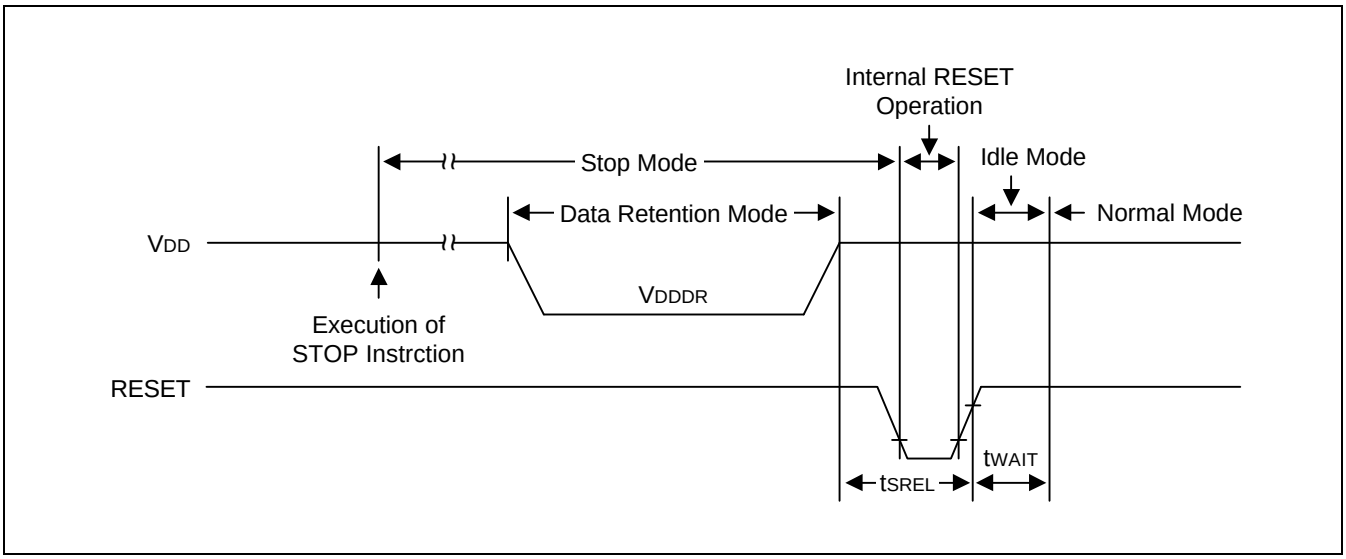


Figure 14-2. Stop Mode Release Timing When Initiated By RESET

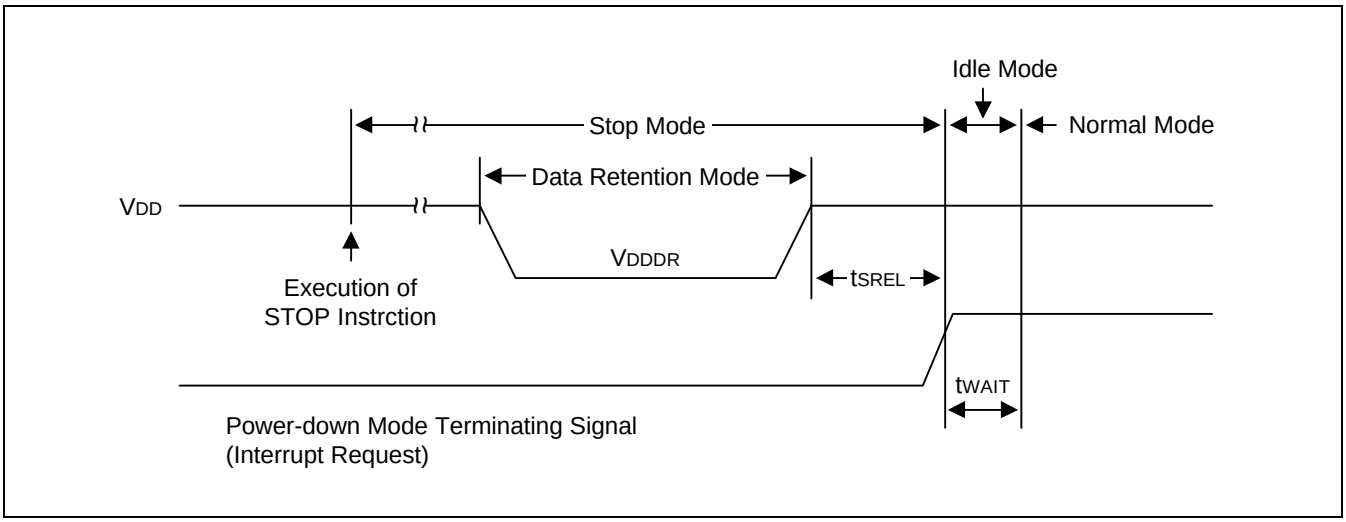


Figure 14-3. Stop Mode Release Timing When Initiated By Interrupt Request

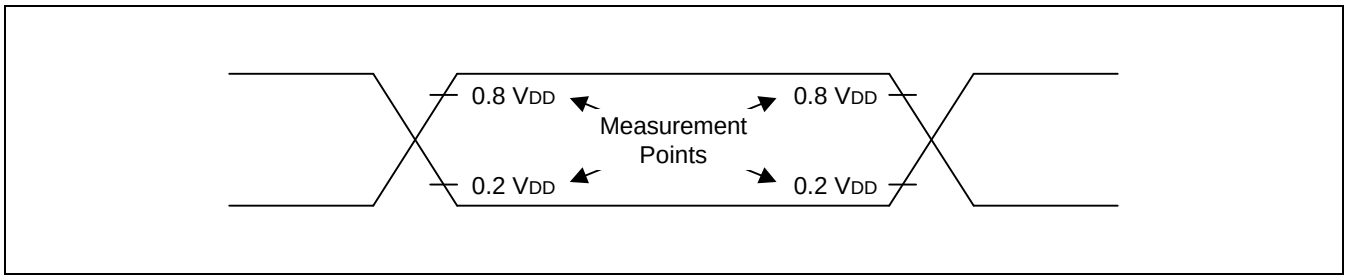


Figure 14-4. A.C. Timing Measurement Points (Except for X_{IN} and XT_{IN})

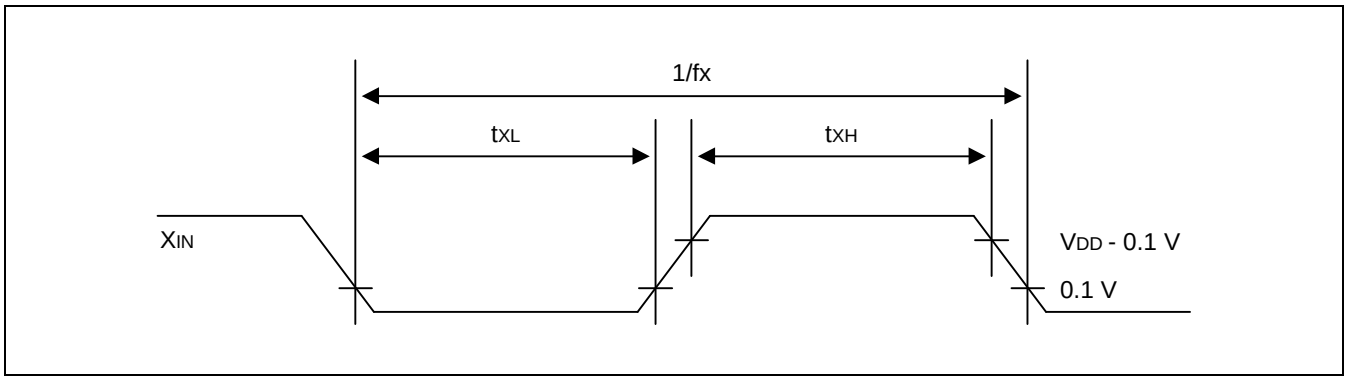


Figure 14-5. Clock Timing Measurement at X_{IN}

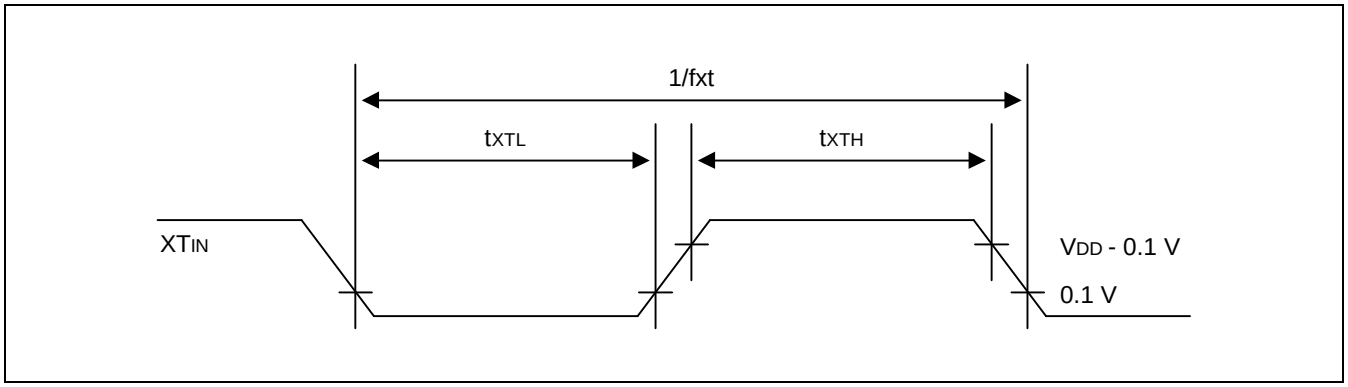


Figure 14-6. Clock Timing Measurement at XT_{IN}

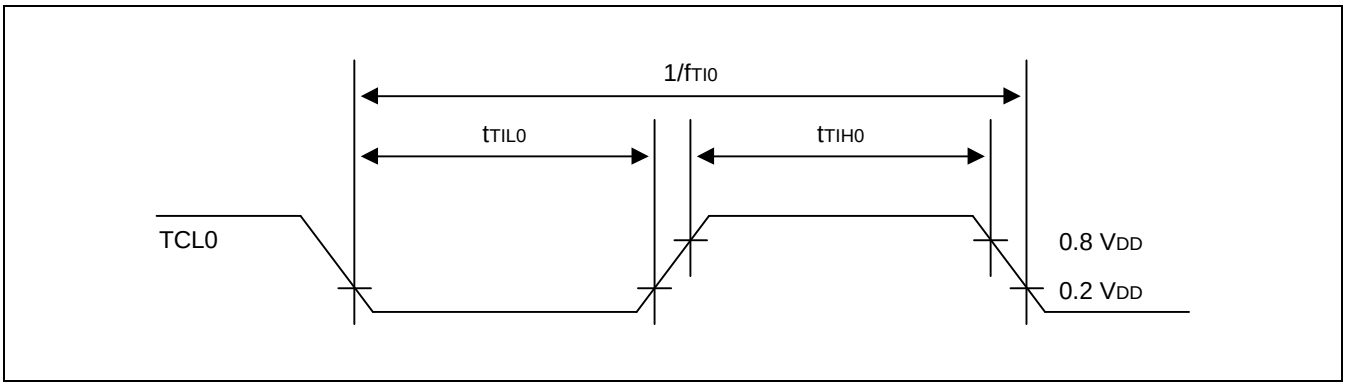


Figure 14-7. TCL0 Timing

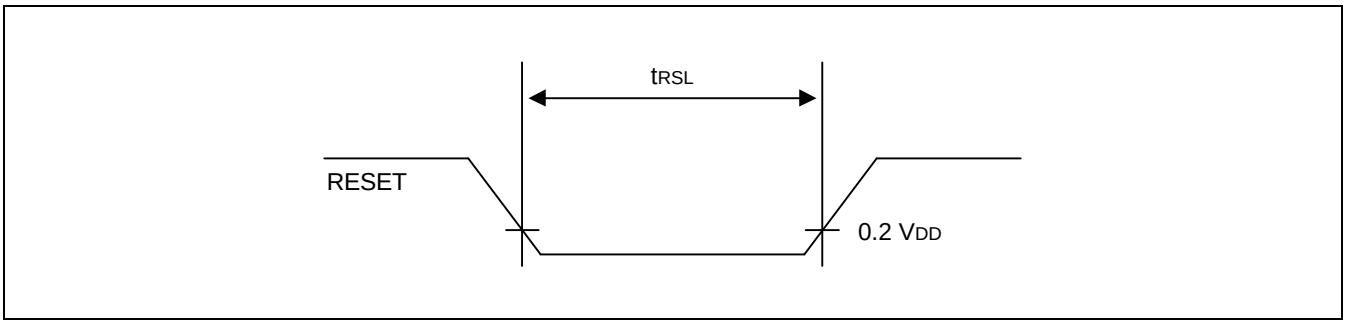


Figure 14-8. Input Timing for RESET Signal

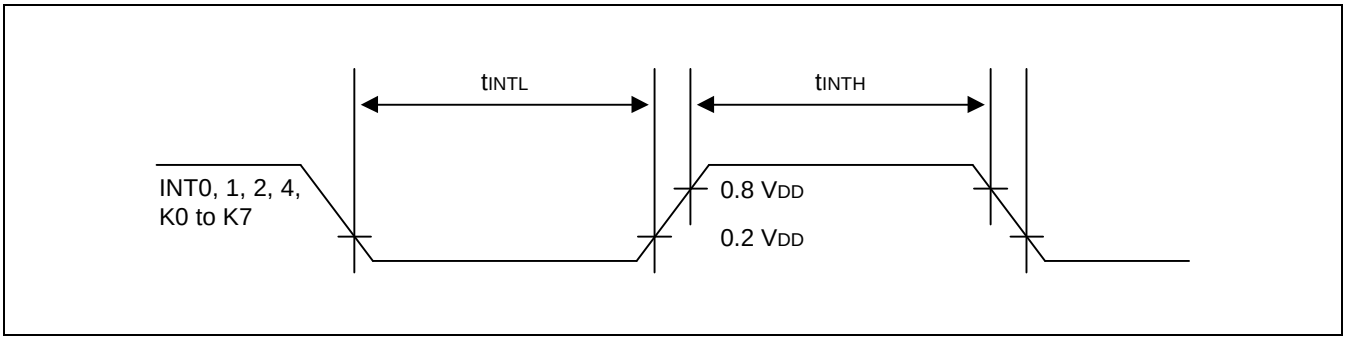


Figure 14-9. Input Timing for External Interrupts and Quasi-Interrupts

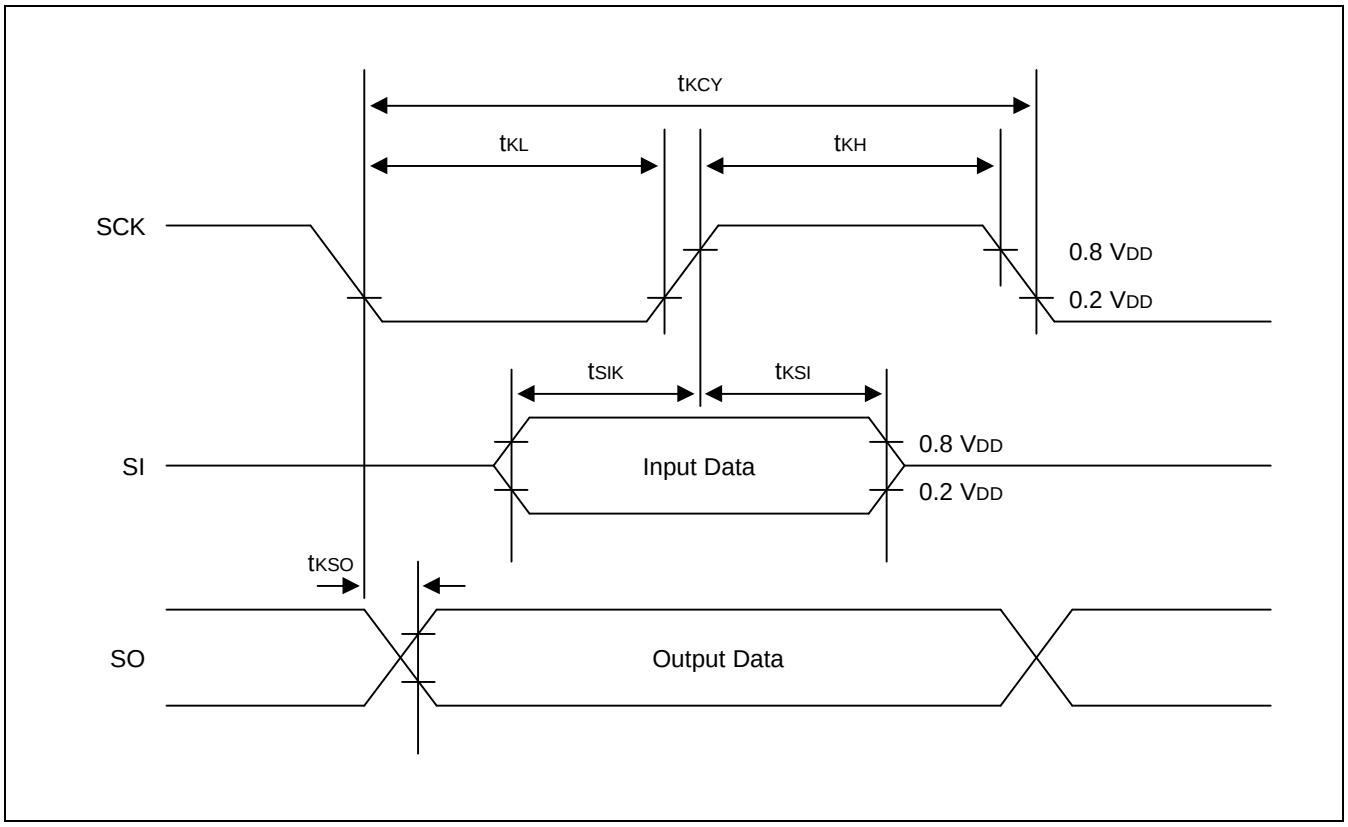


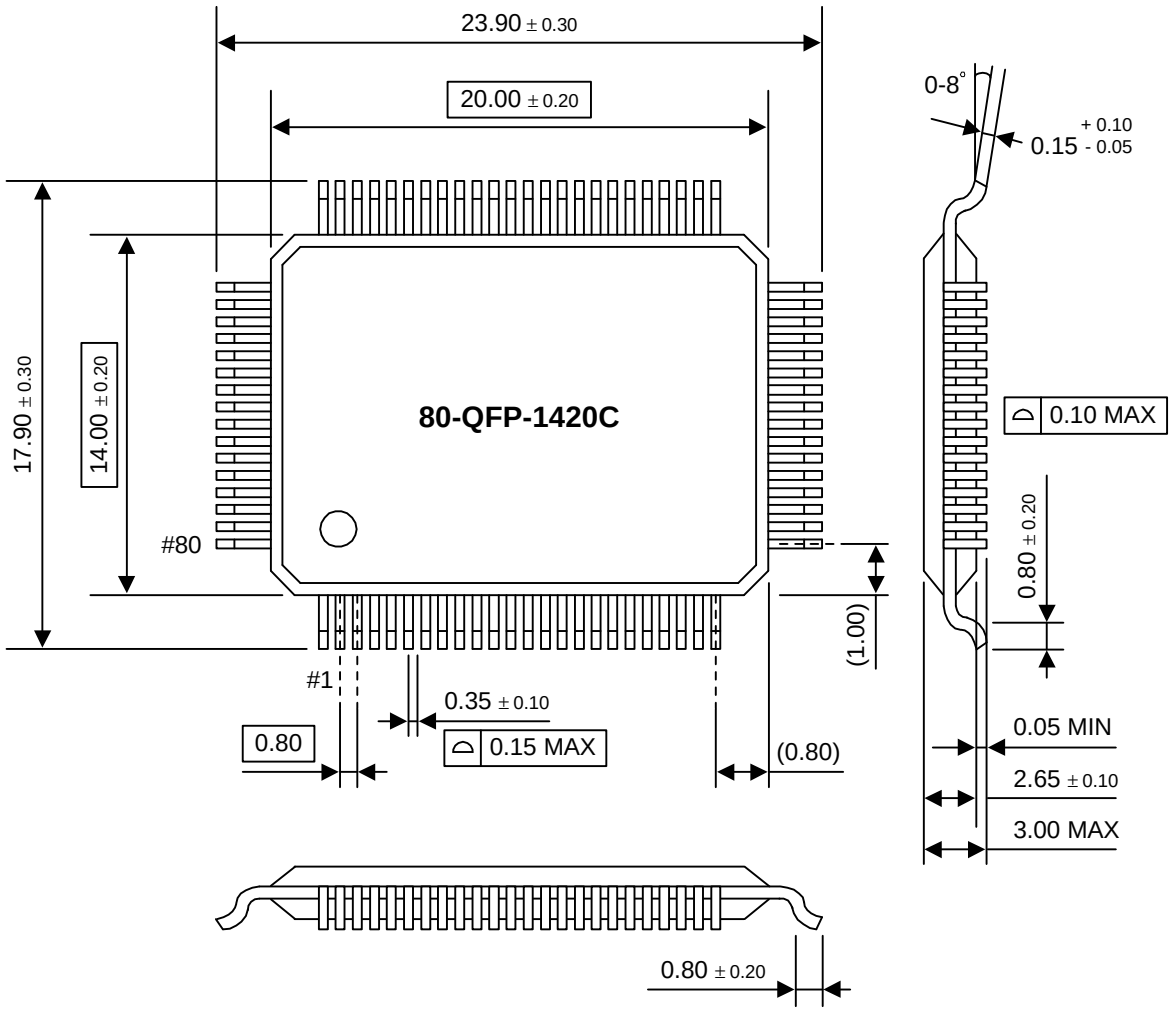
Figure 14-10. Serial Data Transfer Timing

15 MECHANICAL DATA

OVERVIEW

This section contains the following information about the device package:

— Package dimensions in millimeters
— Pad diagram
— Pad/pin coordinate data table



NOTE: Dimensions are in millimeters.

Figure 15-1. 80-QFP-1420C Package Dimensions

16 S3P72N8/P72N5 OTP

OVERVIEW

The S3P72N8/P72N5 single-chip CMOS microcontroller is the OTP (One Time Programmable) version of the S3C72N8/C72N5 microcontroller. It has an on-chip EPROM instead of masked ROM. The EPROM is accessed by a serial data format.

The S3P72N8/P72N5 is fully compatible with the S3C72N8/C72N5, both in function and in pin configuration. Because of its simple programming requirements, the S3P72N8/P72N5 is ideal for use as an evaluation chip for the S3C72N8/C72N5.

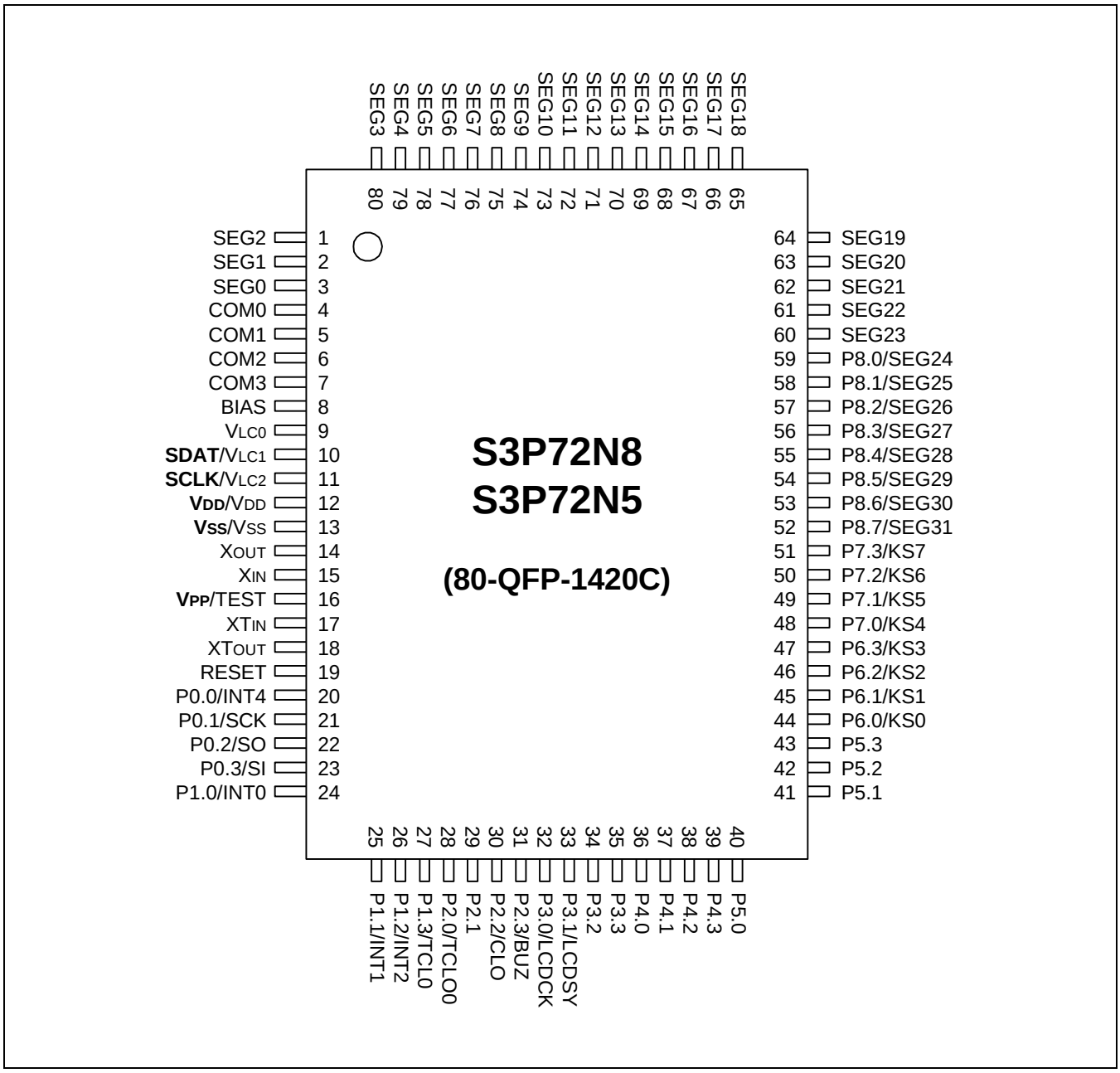


Figure 16-1. S3P72N8/P72N5 Pin Assignments (80-QFP)

Table 16-1. Pin Descriptions Used to Read/Write the EPROM

Main Chip	During Programming			
Pin Name	**Pin Name**	**Pin No.**	**I/O**	**Function**
V_{LC1}	SDAT	10	I/O	Serial data pin. Output port when reading and input port when writing can be assigned as Input/push-pull output port respectively.
V_{LC2}	SCLK	11	I/O	Serial clock pin. Input only pin.
TEST	V_{PP} (TEST)	16	I	Power supply pin for EPROM cell writing (indicates that OTP enters into the writing mode). When 12.5 V is applied, OTP is in writing mode and when 5 V is applied, OTP is in reading mode. (Option)
RESET	RESET	19	I	Chip initialization
V_{DD} / V_{SS}	V_{DD} / V_{SS}	12/13	I	Logic power supply pin. V_{DD} should be tied to +5 V during programming.

Table 16-2. Comparison of S3P72N8/P72N5 and S3C72N8/C72N5 Features

Characteristic	S3P72N8/P72N5	S3C72N8/C72N5
Program Memory	8 K/16 K-byte EPROM	8 K/16-Kbyte mask ROM
Operating Voltage (V_{DD})	1.8 V to 5.5 V	1.8 V to 5.5 V
OTP Programming Mode	V_{DD} = 5 V, V_{PP} (TEST) = 12.5 V	–
Pin Configuration	80 QFP	80 QFP
EPROM Programmability	User Program 1 time	Programmed at the factory

OPERATING MODE CHARACTERISTICS

When 12.5 V is supplied to the V_{PP} (TEST) pin of the S3P72N8/P72N5, the EPROM programming mode is entered. The operating mode (read, write, or read protection) is selected according to the input signals to the pins listed in Table 16-3 below.

Table 16-3. Operating Mode Selection Criteria

V_{DD}	V_{PP} (TEST)	REG/ MEM	Address (A15-A0)	R/W	Mode
5 V	5 V	0	0000H	1	EPROM read
	12.5V	0	0000H	0	EPROM program
	12.5V	0	0000H	1	EPROM verify
	12.5V	1	0E3FH	0	EPROM read protection

NOTE: "0" means low level; "1" means high level.

Table 16-4. Absolute Maximum Ratings

(T_A = 25 °C)

Parameter	Symbol	Conditions	Rating	Units
Supply Voltage	V_{DD}	–	– 0.3 to + 6.5	V
Input Voltage	V_{I1}	All I/O ports	– 0.3 to V_{DD} + 0.3	
Output Voltage	V_O	–	– 0.3 to V_{DD} + 0.3	
Output Current High	I_{OH}	One I/O pin active	– 15	mA
		All I/O ports active	– 35	
Output Current Low	I_{OL}	One I/O pin active	+ 30 (Peak value)	
			+ 15 (note)	
		Total value for ports 0, 2, 3, and 5	+ 100 (Peak value)	
			+ 60 (note)	
		Total value for ports 4, 6, and 7	+ 100	
			+ 60 (note)	
Operating Temperature	T_A	–	– 40 to + 85	°C
Storage Temperature	T_{stg}	–	– 65 to + 150	

NOTE: The values for Output Current Low (I_{OL}) are calculated as Peak Value $\times \sqrt{\text{Duty}}$.

Table 16-5. D.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Input high voltage	V_{IH1}	All input pins except those specified below for V_{IH2}, V_{IH3}	0.7 V_{DD}	–	V_{DD}	V
	V_{IH2}	Ports 0, 1, 6, 7 and RESET	0.8 V_{DD}	–	V_{DD}	
	V_{IH3}	X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}	V_{DD} – 0.1	–	V_{DD}	
Input low voltage	V_{IL1}	Ports 2, 3, 4 and 5	–	–	0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, 7 and RESET	–	–	0.2 V_{DD}	
	V_{IL3}	X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}	–	–	0.1	
Output high voltage	V_{OH1}	V_{DD} = 4.5 V to 5.5 V Ports 0, 2, 3, 4, 5, 6, 7 and BIAS I_{OH} = – 1 mA	V_{DD} – 1.0	–	–	V
	V_{OH2}	V_{DD} = 4.5 V to 5.5 V Port 8 ONLY I_{OH} = – 100 µA	V_{DD} – 2.0	–	–	

Table 16-5. D.C. Electrical Characteristics (Continued)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Output low voltage	V_{OL1}	V_{DD} = 4.5 V to 5.5 V, Ports 0, 2–7 I_{OL} = 15 mA	–	0.4	2	V
	V_{OL2}	V_{DD} = 4.5 V to 5.5 V, Port 8 only I_{OL} = 100 µA	–	–	1	
Input high leakage current	I_{LIH1}	V_{IN} = V_{DD} All input pins except those specified below for I_{LIH2}	–	–	3	µA
	I_{LIH2}	V_{IN} = V_{DD} X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}	–	–	20	
Input low leakage current	I_{LIL1}	V_{IN} = 0 V All input pins except X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}	–	–	– 3	
	I_{LIL2}	V_{IN} = 0 V X_{IN}, X_{OUT}, XT_{IN} and XT_{OUT}			– 20	
Output high leakage current	I_{LOH1}	V_{OUT} = V_{DD} All output pins	–	–	3	µA
Output low leakage current	I_{LOL}	V_{OUT} = 0 V All output pins			– 3	
Pull-up resistor	R_{L1}	Ports 0-7 V_{IN} = 0 V; V_{DD} = 5 V	25	47	100	KΩ
		V_{DD} = 3 V	50	95	200	
	R_{L2}	V_{IN} = 0 V; V_{DD} = 5 V, RESET	100	220	400	
		V_{DD} = 3 V	200	450	800	
LCD voltage dividing resistor	R_{LCD}	T_A = 25 °C	50	93	140	
COM output impedance	R_{COM}	V_{DD} = 5 V	–	3	6	
		V_{DD} = 3 V		5	15	
SEG output impedance	R_{SEG}	V_{DD} = 5 V		3	6	
		V_{DD} = 3 V		5	15	
COM output voltage deviation	VDC	V_{DD} = 5 V (V_{LC0}-COMi) Io = ± 15uA (I = 0–3)	–	± 45	± 90	mV
SEG output voltage deviation	VDS	V_{DD} = 5 V (V_{LC0}-SEGi) Io = ± 15µA (I = 0–31)	–	ñ 45	ñ 90	mV

Table 16-5. D.C. Electrical Characteristics (Concluded)

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

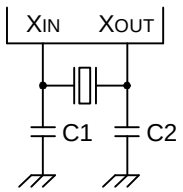
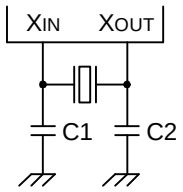
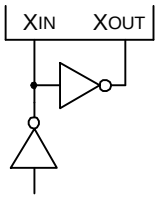
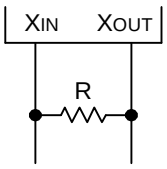
Parameter	Symbol	Conditions		Min	Typ	Max	Units
V_{LC0} Output voltage	V_{LC0}	T_A = 25 øC		0.6 V_{DD} – 0.2	0.6 V_{DD}	0.6 V_{DD} + 0.2	V
V_{LC1} Output voltage	V_{LC1}	T_A = 25 øC		0.4 V_{DD} – 0.2	0.4 V_{DD}	0.4 V_{DD} + 0.2	
V_{LC2} Output voltage	V_{LC2}	T_A = 25 øC		0.2 V_{DD} – 0.2	0.2 V_{DD}	0.2 V_{DD} + 0.2	
Supply Current (1)	I_{DD1} (2)	Main operating: V_{DD} = 5 V ± 10% CPU = fx/4 SCMOD = 0000B crystal oscillator C1 = C2 = 22pF	6.0 MHz 4.19 MHz	–	3.5 2.5	8 5.5	mA
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		1.6 1.2	4 3	
	I_{DD2} (2)	Main Idle mode; V_{DD} = 5 V ± 10% CPU = fx/4 SCMOD = 0000B crystal oscillator C1 = C2 = 22pF	6.0 MHz 4.19 MHz	–	1.0 0.9	2.5 2.0	
		V_{DD} = 3 V ± 10%	6.0 MHz 4.19 MHz		0.5 0.4	1.0 0.8	
	I_{DD3}	Sub operating: V_{DD} = 3 V ± 10% CPU = fxt/4 SCMOD = 1001B 32 kHz crystal oscillator		–	15	30	µA
	I_{DD4}	Sub Idle mode; V_{DD} = 3 V ± 10% CPU = fxt/4, SCMOD = 1001B 32 kHz crystal oscillator		–	6	15	
	I_{DD5}	Stop mode; V_{DD} = 5 V ± 10%, XT_{IN} = 0 V CPU = fxt/4, SCMOD = 0000B		–	2.5	5	
	I_{DD6} (3)	Stop mode; V_{DD} = 5 V ± 10% CPU = fx/4, SCMOD = 0100B		–	0.5	3	

NOTES:

1. D.C. electrical values for supply current (I_{DD1} to I_{DD6}) do not include current drawn through internal pull-up resistors and through LCD voltage dividing resistors.
2. Data includes the power consumption for sub-system clock oscillation.
3. When the system clock mode register, SCMOD, is set to 0100B, the sub-system clock oscillation stops. The main-system clock oscillation stops by the STOP instruction.

Table 16-6. Main System Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

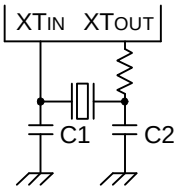
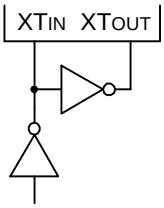
Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Ceramic Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	Stabilization occurs when V_{DD} is equal to the minimum oscillator voltage range.	–	–	4	ms
Crystal Oscillator		Oscillation frequency (1)	–	0.4	–	6.0	MHz
		Stabilization time (2)	V_{DD} = 4.5 V to 5.5 V	–	–	10	ms
			V_{DD} = 1.8 V to 4.5 V	–	–	30	
External Clock		X_{IN} input frequency (1)	–	0.4	–	6.0	MHz
		X_{IN} input high and low level width (t_{XH}, t_{XL})	–	83.3	–	–	ns
RC Oscillator		Frequency (1)	V_{DD} = 5 V R = 20 KΩ, V_{DD} = 5 V R = 38 KΩ, V_{DD} = 3 V	0.4	– 2.0 1.0	2	MHz

NOTES:

1. Oscillation frequency and X_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillator stabilization after a power-on occurs, or when stop mode is terminated.

Table 16-7. Subsystem Clock Oscillator Characteristics

(T_A = – 40 °C + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Oscillator	Clock Configuration	Parameter	Test Condition	Min	Typ	Max	Units
Crystal Oscillator		Oscillation frequency (1)	–	32	32.768	35	kHz
		Stabilization time (2)	V_{DD} = 4.5 V to 5.5 V	–	1.0	2	s
			V_{DD} = 1.8 V to 4.5 V	–	–	10	
External Clock		XT_{IN} input frequency (1)	–	32	–	100	kHz
		XT_{IN} input high and low level width (t_{XTL}, t_{XTH})	–	5	–	15	µs

NOTES:
1. Oscillation frequency and XT_{IN} input frequency data are for oscillator characteristics only.
2. Stabilization time is the interval required for oscillating stabilization after a power-on occurs.

Table 16-8. Input/Output Capacitance

(T_A = 25 °C, V_{DD} = 0 V)

Parameter	Symbol	Condition	Min	Typ	Max	Units
Input capacitance	C_{IN}	f = 1 MHz; Unmeasured pins are returned to V_{SS}	–	–	15	pF
Output capacitance	C_{OUT}		–	–	15	pF
I/O capacitance	C_{IO}		–	–	15	pF

Table 16-9. A.C. Electrical Characteristics

(T_A = – 40 °C to + 85 °C, V_{DD} = 1.8 V to 5.5 V)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
Instruction cycle time (1)	t_{CY}	V_{DD} = 2.7 V to 5.5 V	0.67	–	64	µs
		V_{DD} = 1.8 V to 5.5 V	0.95	–	64	
		With subsystem clock (fxt)	114	122	125	
TCL0 input frequency	f_{TI0}	V_{DD} = 2.7 V to 5.5 V	0	–	1.5	MHz
		V_{DD} = 1.8 V to 5.5V			1	MHz
TCL0 input high, low width	t_{TIH0}, t_{TIL0}	V_{DD} = 2.7 V to 5.5 V	0.48	–	–	µs
		V_{DD} = 1.8 V to 5.5 V	1.8			
SCK cycle time	t_{KCY}	V_{DD} = 2.7 V to 5.5 V External SCK source	800	–	–	ns
		Internal SCK source	650			
		V_{DD} = 1.8 V to 5.5 V External SCK source	3200			
		Internal SCK source	3800			
SCK high, low width	t_{KH}, t_{KL}	V_{DD} = 1.8 V to 5.5 V External SCK source	400	–	–	ns
		Internal SCK source	$t_{KCY}/2 – 50$			
		V_{DD} = 1.8 V to 5.5 V External SCK source	1600			
		Internal SCK source	$t_{KCY}/2 – 150$			
SI setup time to SCK high	t_{SIK}	External SCK source	100	–	–	ns
		Internal SCK source	150			
SI hold time to SCK high	t_{KSI}	External SCK source	400	–	–	ns
		Internal SCK source	400			
Output delay for SCK to SO	t_{KSO}	V_{DD} = 2.7 V to 5.5 V External SCK source	–	–	300	ns
		Internal SCK source			250	
		V_{DD} = 1.8 V to 5.5 V External SCK source			1000	
		Internal SCK source			1000	
Interrupt input high, low width	t_{INTH}, t_{INTL}	INT0	(2)	–	–	µs
		INT1, INT2, INT4, KS0-KS7	10			
RESET Input Low Width	t_{RSL}	Input	10	–	–	µs

NOTES:

1. Unless otherwise specified, Instruction Cycle Time condition values assume a main system clock (fx) source.
2. Minimum value for INT0 is based on a clock of $2t_{CY}$ or 128/fx as assigned by the IMOD0 register setting.

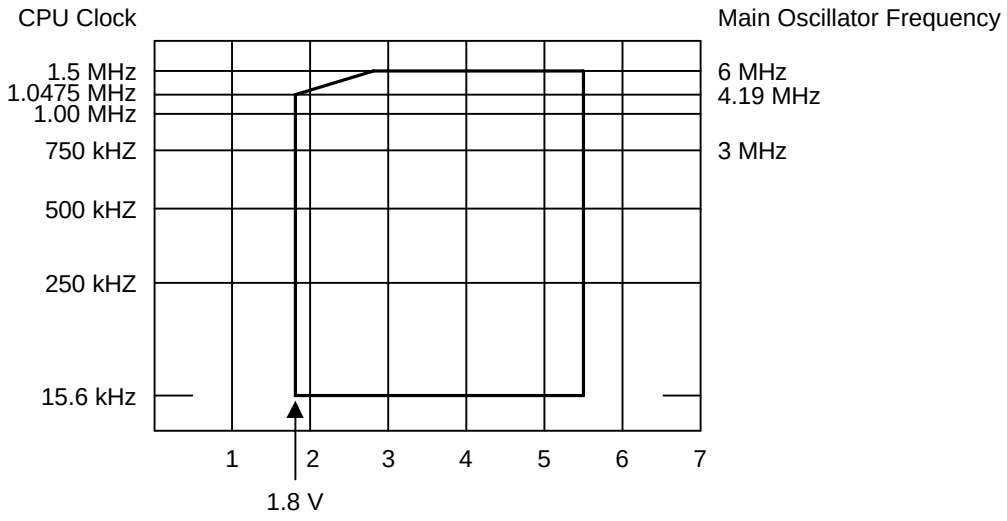


Figure 16-2. Standard Operating Voltage Range

Table 16-10. RAM Data Retention Supply Voltage in Stop Mode

(T_A = – 40 °C to + 85 °C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Data retention supply voltage	V_{DDDR}	Normal operation	1.8	–	6.5	V
Data retention supply current	I_{DDDR}	V_{DDDR} = 1.8 V	–	0.1	10	µs
Release signal set time	t_{SREL}	Normal operation	0	–	–	µs
Oscillator stabilization wait time (1)	t_{WAIT}	Released by RESET	–	2^{17}/fx	–	ms
		Released by interrupt	–	(2)	–	

NOTES:
1. During oscillator stabilization wait time, all CPU operations must be stopped to avoid instability during oscillator start-up.
2. Use the basic timer mode register (BMOD) interval timer to delay execution of CPU instructions during the wait time.

TIMING WAVEFORMS

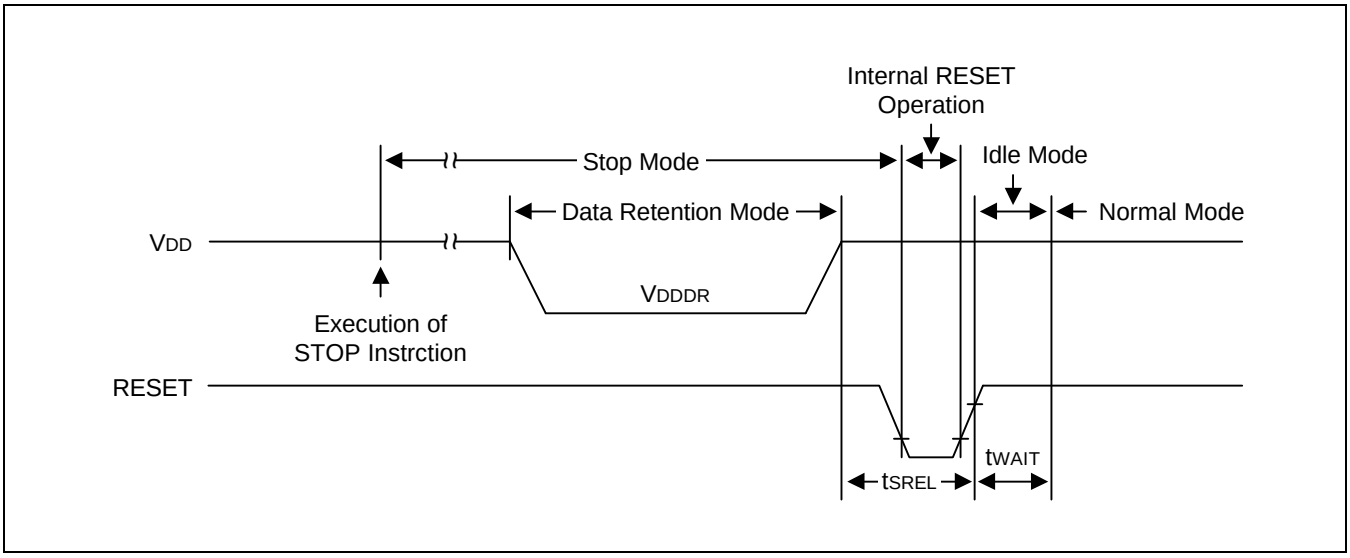


Figure 16-3. Stop Mode Release Timing When Initiated By RESET

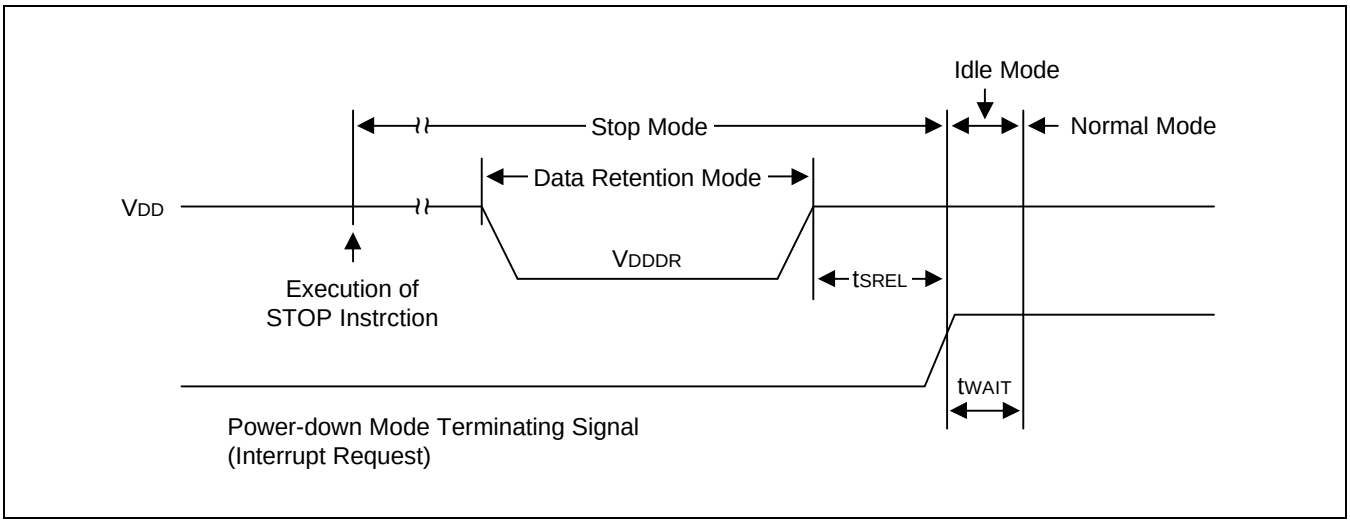


Figure 16-4. Stop Mode Release Timing When Initiated By Interrupt Request

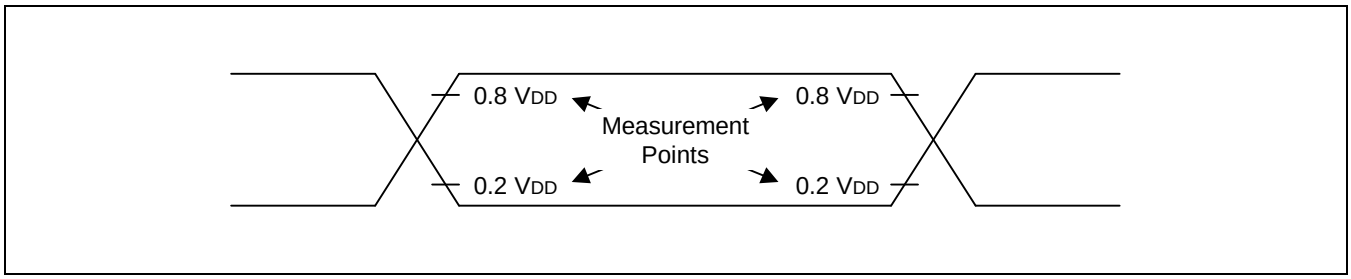


Figure 16-5. A.C. Timing Measurement Points (Except for X_{IN} and XT_{IN})

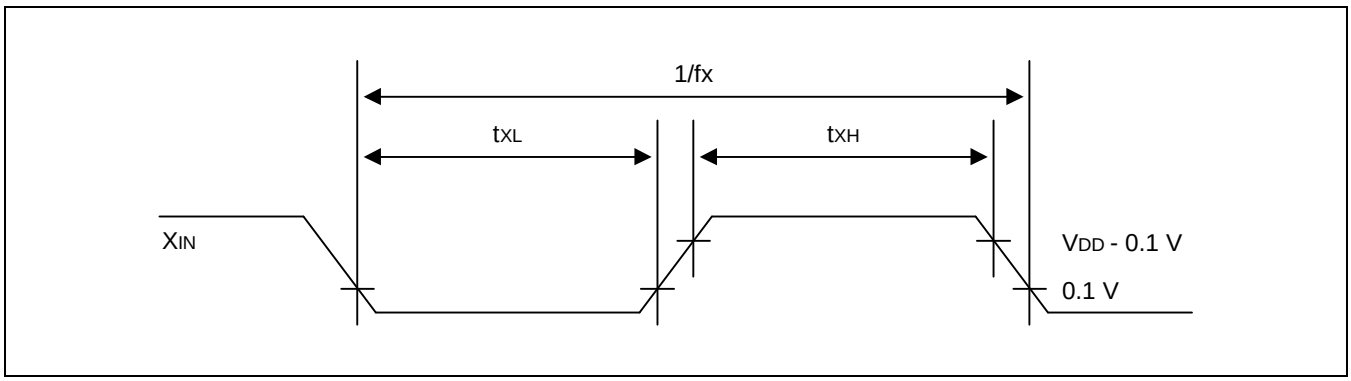


Figure 16-6. Clock Timing Measurement at X_{IN}

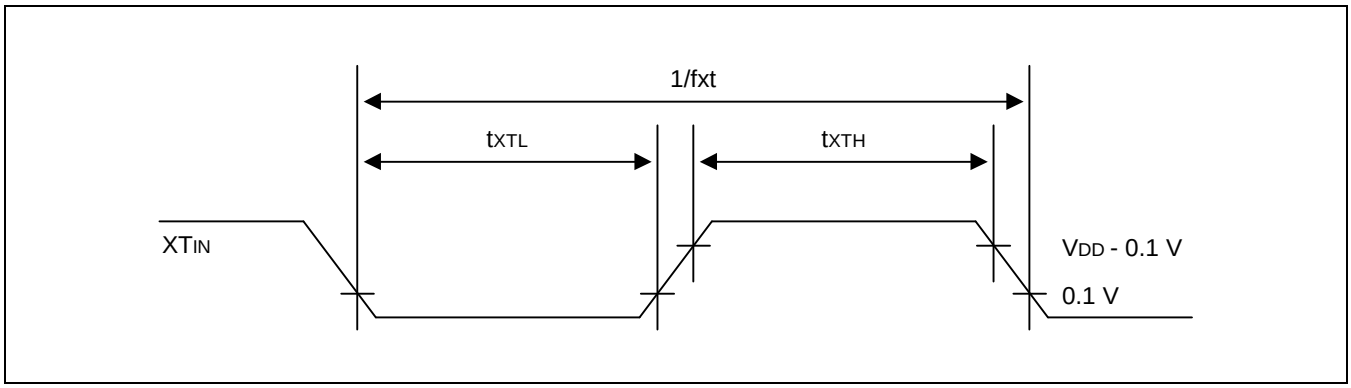


Figure 16-7. Clock Timing Measurement at XT_{IN}

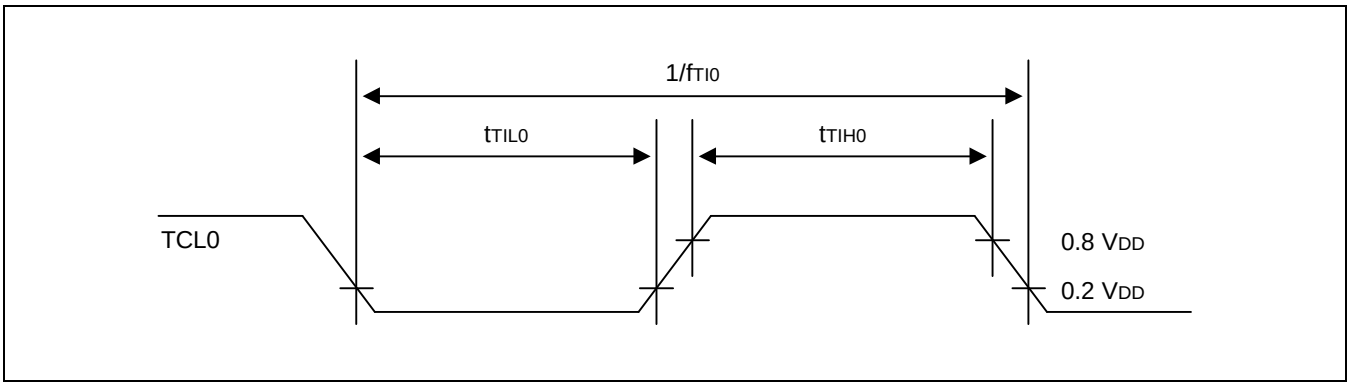


Figure 16-8. TCL0 Timing

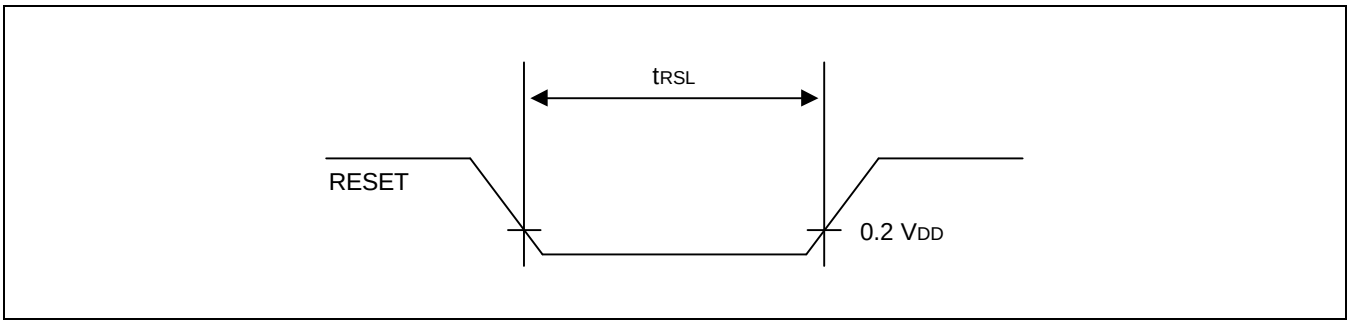


Figure 16-9. Input Timing for RESET Signal

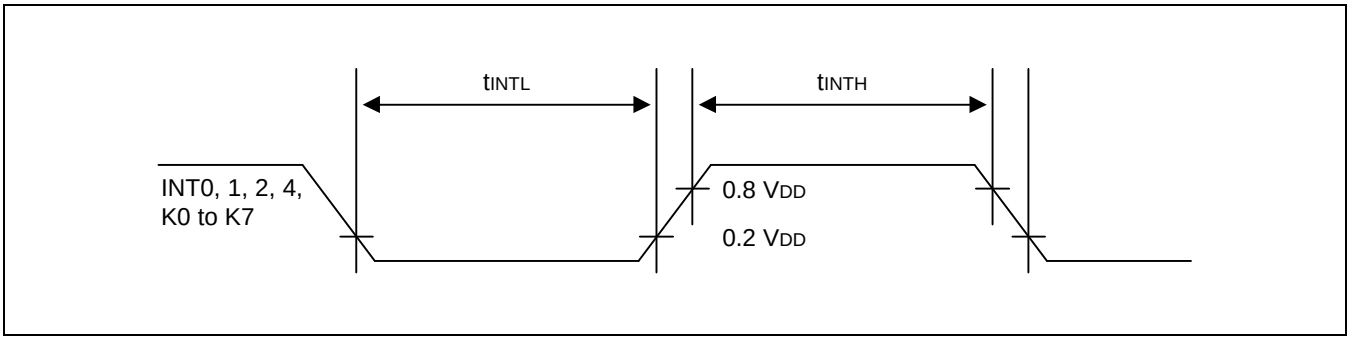


Figure 16-10. Input Timing for External Interrupts and Quasi-Interrupts

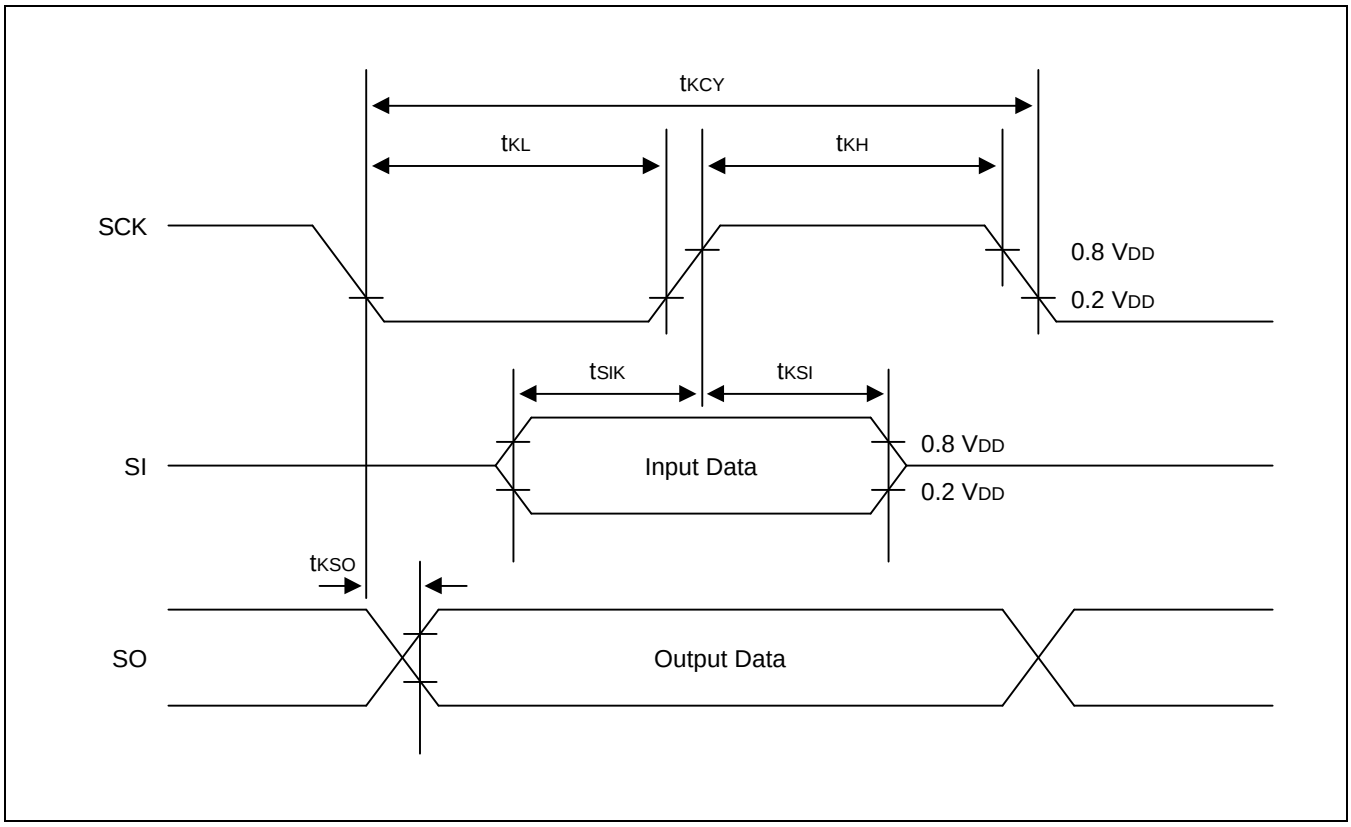


Figure 16-11. Serial Data Transfer Timing

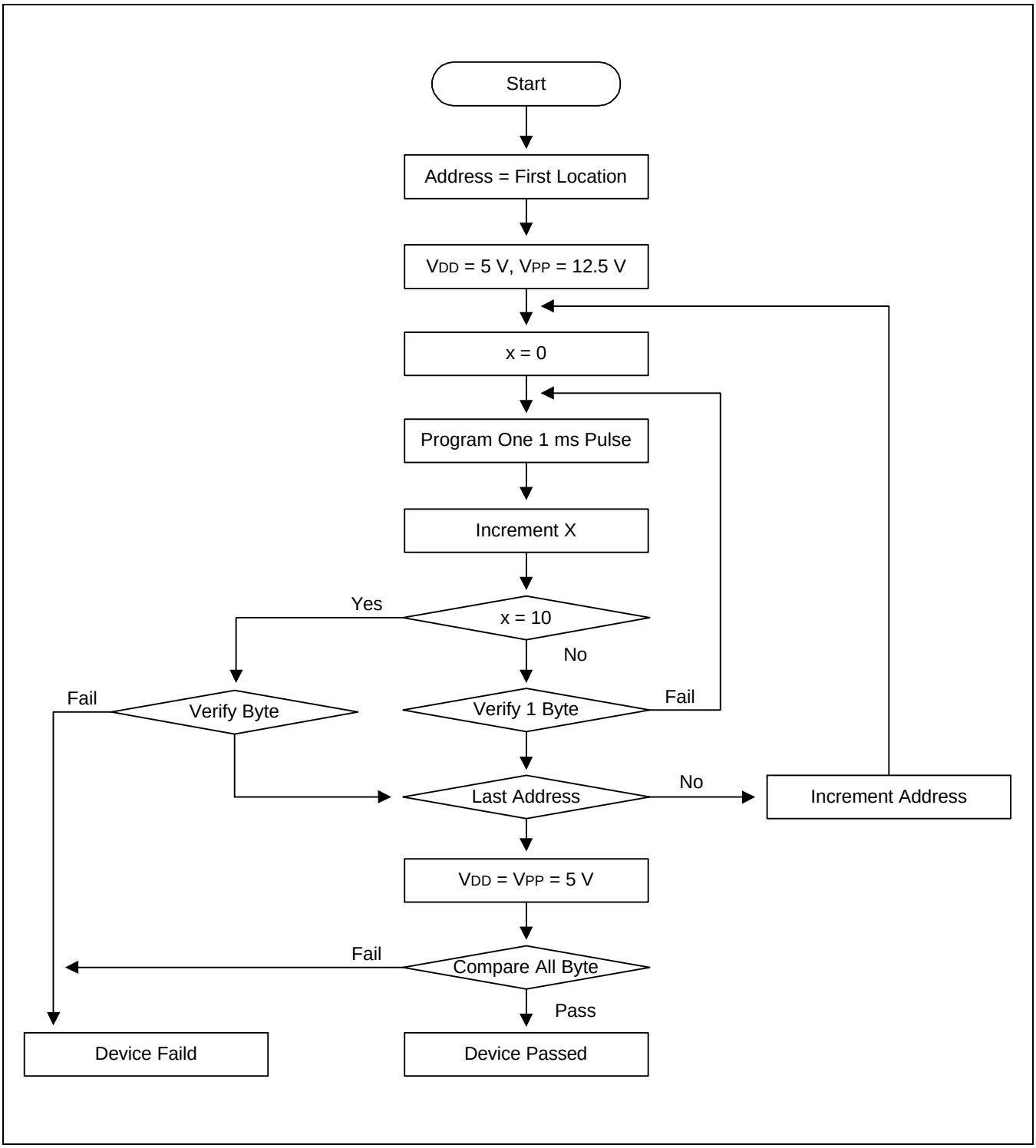


Figure 16-12. OTP Programming Algorithm

NOTES