## TOSHIBA BIPOLAR DIGITAL INTEGRATED CIRCUIT  SILICON MONOLITHIC

# TD62650F, TD62651F, TD62652F

# 5V POWER SUPPLY & SUPPLY MONITORING + COMMUNICATIONS IC

The TD6265xF series covers products developed for use in microcomputer systems applicable to automatic vending machines. They produce an output voltage of 5V±0.5V without need for adjustment, through their accurate reference voltage and amplifier circuit.

The 5V section can reset the system by outputting reset signals at power-on, and also output a reset signal when the 5V output voltage drops below the specified 92% (TD62650F／652F) or 85% (TD62651F) because of external disturbances or other problem.

It also incorporates a watchdog timer for self-diagnosing the system. When the system malfunctions, the IC generates reset pulses intermittently to prevent the system from running away.

The interface section incorporates three serial ports corresponding to the typical 24-V 4800bps system in microcomputers.
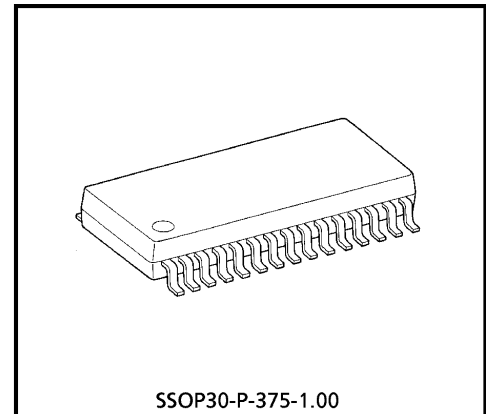


SSOP30-P-375-1.00

Weight : 0.63g (Typ.)

## FEATURES

- Accurate output                         : 5V±0.25V

- Output PNP Tr incorporated              : Current capacity ; 300mA (max)

- Power-on Reset timer incorporated

- Watchdog timer incorporated

- Small flat package sealing              : MFP30 pin (1mm pitch)

- Difference 1

| CHARACTERISTIC | TD62650 / 652F | TD62651F |
|---|---|---|
| Reset Detecting Voltage | 5V / 92% | 5V / 85% |

- Difference 2

  Time setting resistance 22kΩ for power-on reset / watchdog timer, and PULL resistance of 4.7kΩ for $\overline{RESET}$ pin.

| TD62650F | TD62651F | TD62652F |
|---|---|---|
| Built-in | None | None |

**PIN CONNECTION**

| | | |
|---|---|---|
| GND | 1 | 30 | ADJ |
| COMP | 2 | 29 | $\overline{RESET}$ |
| V$_{CCIN}$ | 3 | 28 | TC |
| V$_{CCOUT}$ | 4 | 27 | MSCK |
| OUT | 5 | 26 | CK |
| BIAS | 6 | 25 | CCK |
| V$_{CC2}$ | 7 | 24 | HNSYN |
| SLSYN | 8 | 23 | SYN |
| 50 / 60 | 9 | 22 | SL50 / 60 |
| MSSYN | 10 | 21 | MS50 / 60 |
| CPUOUT | 11 | 20 | SYNIN |
| LED | 12 | 19 | TXDOUT |
| TXD | 13 | 18 | MSTXD |
| RXD | 14 | 17 | MSRXD |
| PG | 15 | 16 | SLTXD |
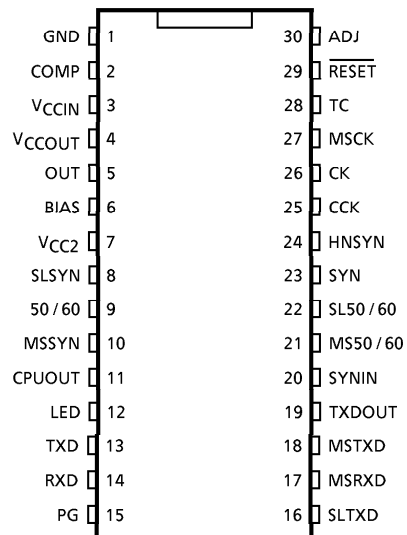
## TD62650F BLOCK DIAGRAM

### 5V POWER SUPPLY + SUPPLY MONITORING



### INTERFACE

## TD62651F / TD62652F BLOCK DIAGRAM

### 5V POWER SUPPLY + SUPPLY MONITORING
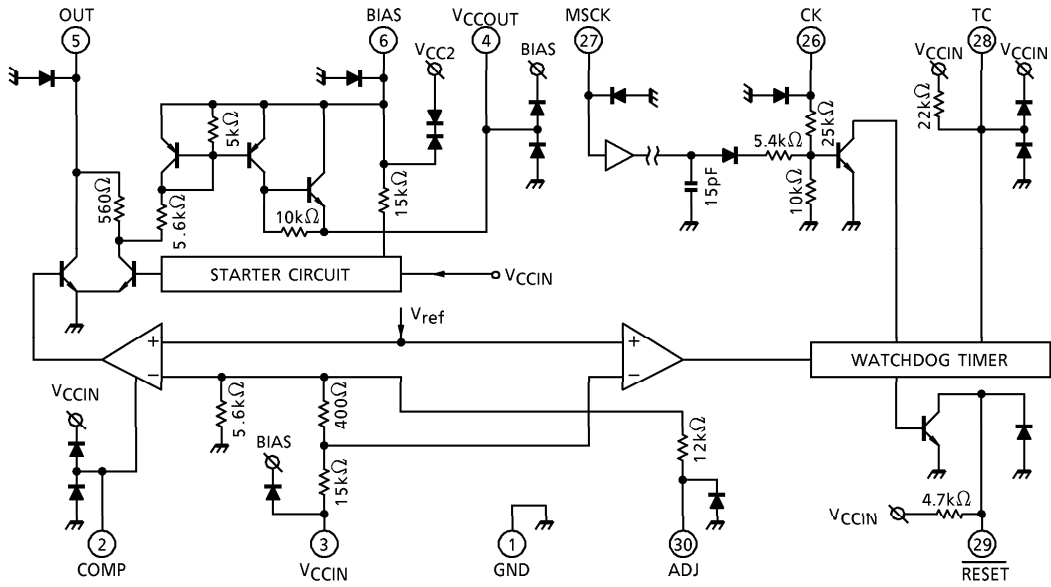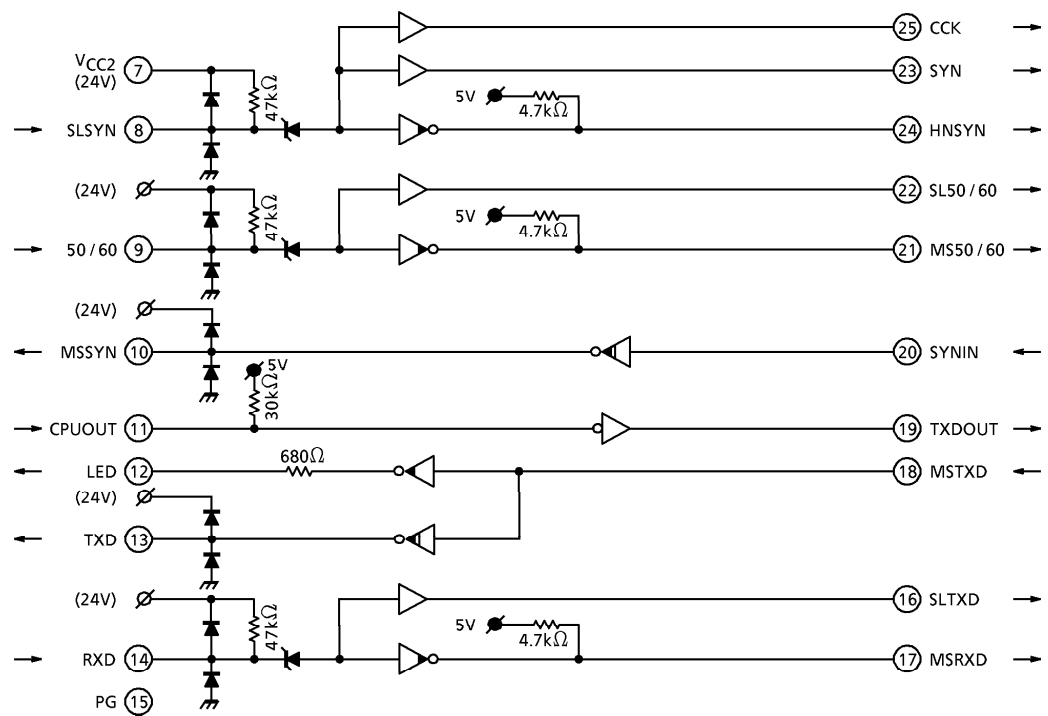


### INTERFACE



▷o : 5-V System Push Pull INV  ▷▶o : 5-V System Open Collector  ▷▶o : 24-V System Open Collector  ▷ : 5-V System Push Pull Buffer

## INTERFACE INPUT / OUTPUT CIRCUITS

## PIN FUNCTION

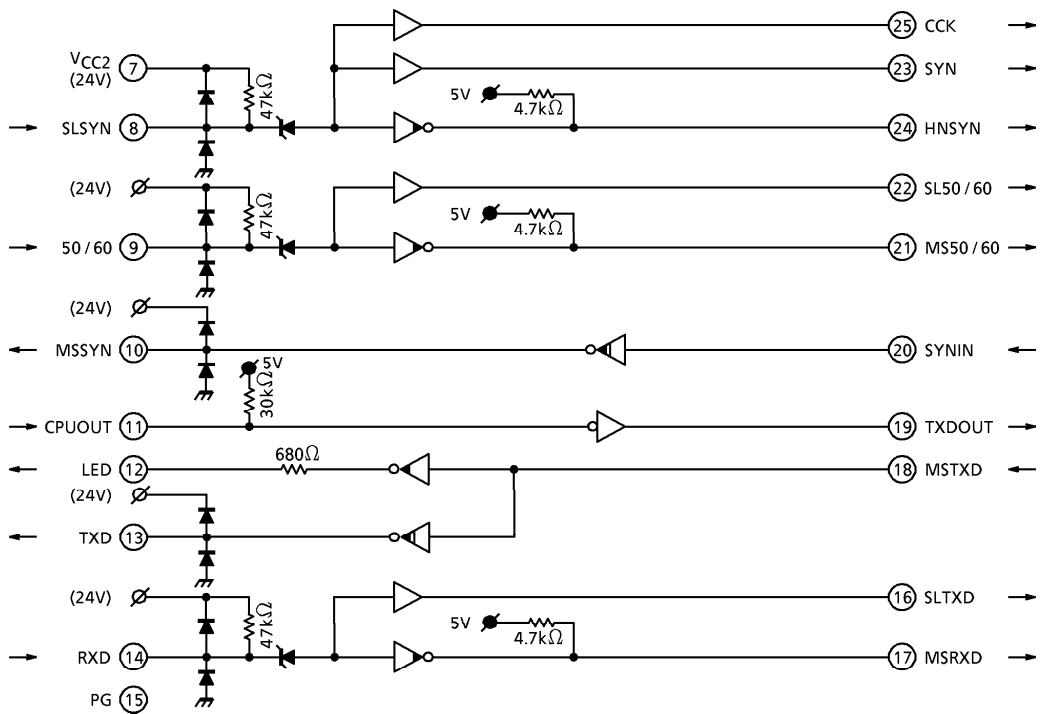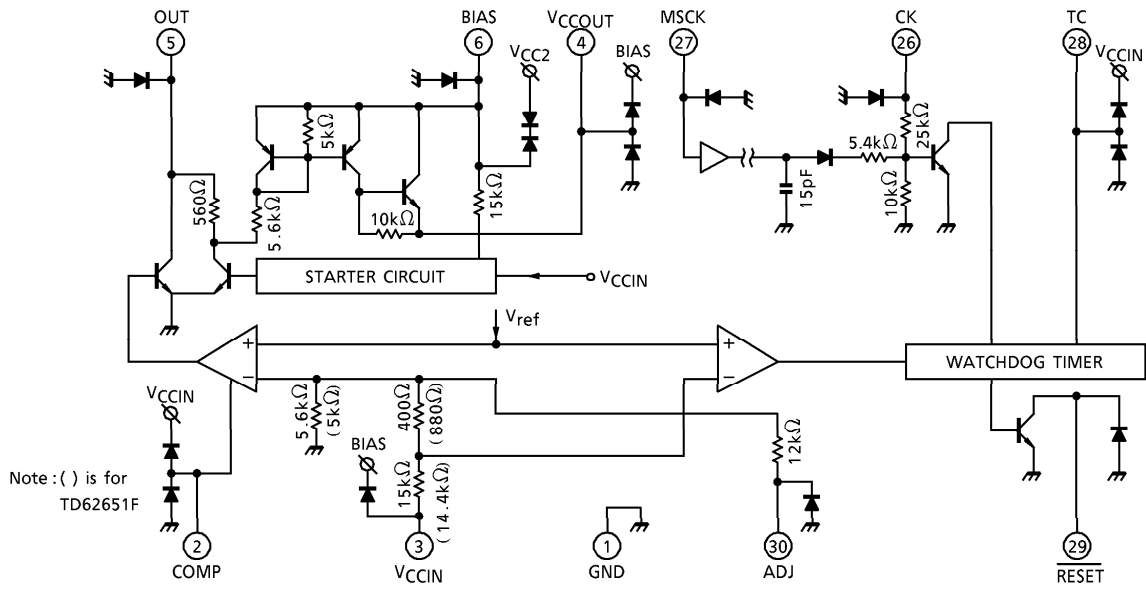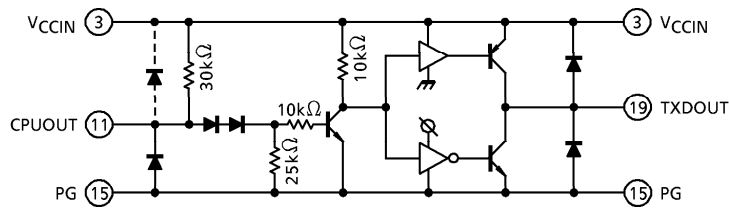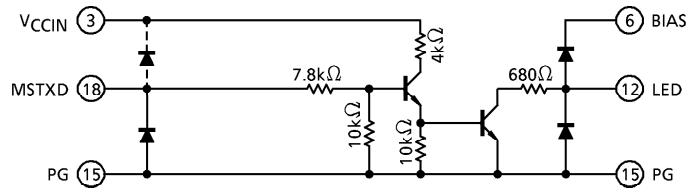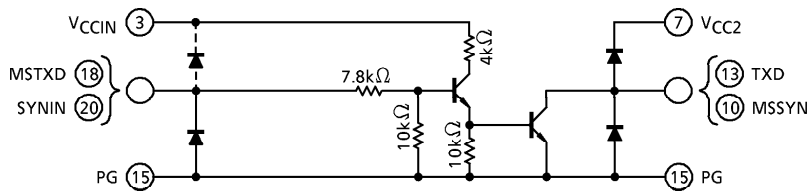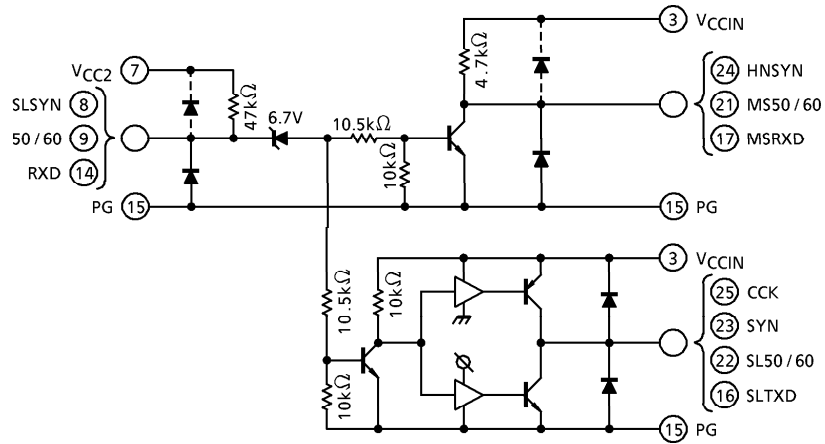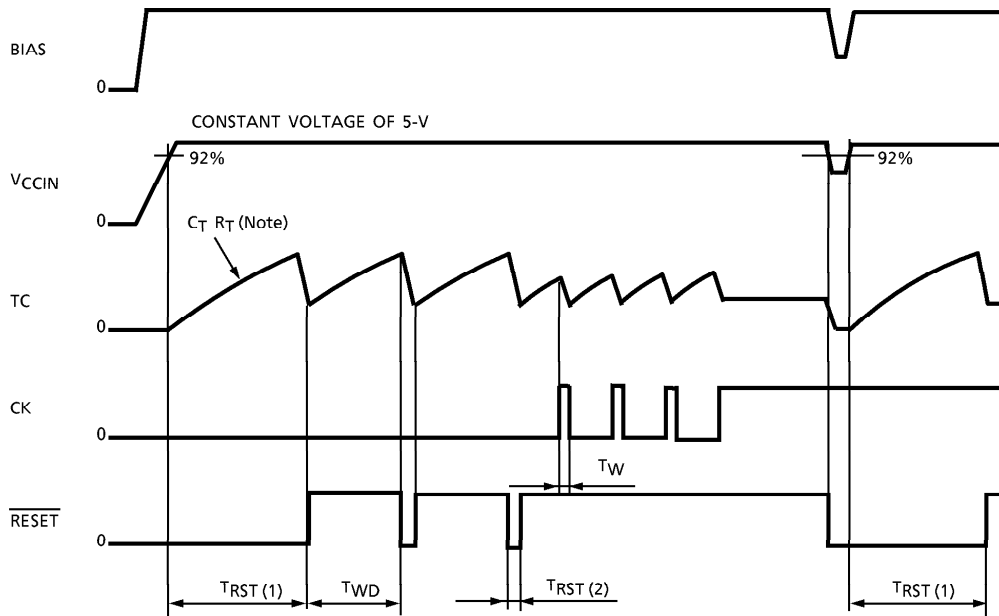| PIN No. | PIN NAME | PIN FUNCTION |
|---|---|---|
| 1 | GND | GND pin for 5V power supply and supply monitoring. |
| 2 | COMP | Phase compensation pin for output stabilization. |
| 3 | $V_{CCIN}$ | Power supply pin for internal circuit. The output voltage can also be detected at this pin. |
| 4 | $V_{CCOUT}$ | Output pin for built-in Power Tr, having a current capacitance of 300mA (max). It is also used as an output pin for 5V constant power supply through shorting with $V_{CCIN}$ pin. |
| 5 | OUT | Connected to the base of an external PNP transistor so that the output voltage is stabilized. Current design suitable for load capacities is thus possible. Since the recommended $I_{OUT}$ current is 5mA, an output current of 300mA is assured if the external transistor has an hFE of 60. When the internal transistor is used, it can be opened. |
| 6 | BIAS | Power supply starting pin. The starting current is supplied through a resistor to which the input voltage is applied. When $V_{CCIN}$ rises above 3.0V, the starting current is absorbed in the internal circuit ; instead, $I_{OUT}$ is supplied via $V_{CCIN}$. |
| 7 | $V_{CC2}$ | Power supply pin for the 24-V system. |
| 8 | SLSYN | Input pin for the 24-V system interface. Pull-up resistor 47kΩ is incorporated at $V_{CC2}$ pin. |
| 9 | 50 / 60 | Input pin for 24-V system interface. Pull-up resistor 47kΩ is incorporated at $V_{CC2}$ pin. |
| 10 | MSSYN | Output pin for the 24-V system open collector. |
| 11 | CPUOUT | Input pin for the 5-V system Push/Pull inverter. Pull-up resistor 30kΩ is incorporated at $V_{CCIN}$ pin. |
| 12 | LED | LED lighting pin for the 8 system open collector. 680Ω limiting resistor is incorporated. |
| 13 | TXD | Output pin for the 24-V system open collector. |
| 14 | RXD | Input pin for the 24-V system interface. Pull-up resistor 47kΩ is incorporated at the $V_{CC2}$ pin. |
| 15 | PG | GND pin for the 5-V / 24-V system interfaces. |
| 16 | SLTXD | Output pin for the 5-V system open collector. Pull-up resistor 4.7kΩ is incorporated at the $V_{CCIN}$ pin. |
| 17 | MSRXD | Output pin for the 5-V system Push-Pull buffer. |
| 18 | MSTXD | Input pin for the 5-V system interface, for input at LED (12 pin) and TXD (13 pin) pins. |
| 19 | TXDOUT | Output pin for the 5-V system Push / Pull inverter (CPUOUT : 11 pin). |
| 20 | SYNIN | Input pin for the 5-V system interface. |
| 21 | MS50 / 60 | Output pin for the 5-V system open collector. Pull-up resistor 4.7kΩ is incorporated at $V_{CCIN}$ pin. |
| 22 | SL50 / 60 | Output pin for the 5-V system Push/Pull buffer. |
| 23 | SYN | Output pin for the 5-V system Push-Pull buffer. |
| 24 | HNSYN | Output pin for the 5-V system open collector. Pull-up resistor 4.7kΩ incorporated at $V_{CCIN}$ pin. |
| 25 | CCK | Output pin for the 5-V system Push-Pull buffer. |

| PIN No. | PIN NAME | PIN FUNCTION |
|---------|----------|--------------|
| 26 | CK | Input pin for watchdog timer. The pin is pulled up to $V_{CCIN}$ if the IC is used only as a power-on reset timer. |
| 27 | MSCK | To input clock pulses, one-shot pulses can be generated for CK (26 pin) inputs at the rise edge. When the pin is not used, short it with GND. |
| 28 | TC | Time setting pin for the reset and watchdog timers. |
| 29 | $\overline{RESET}$ | NPN transistor open-collector output.<br>(1) The signal goes low when the output voltage drops below the specified 92% (TD62650 / 652) or 85% (651F) level.<br>(2) The pin generates a reset signal that is determined by the external condenser connected to the TC pin.<br>(3) The pin generates reset pulses intermittently if no clock is attached to the CK pin.<br>This function can be used as a watchdog timer for microcomputers. |
| 30 | ADJ | Output voltage adjusting pin. The voltage will increase when a resistor is connected between ADJ and GND (1 pin). It can reduce the voltage when the resistor is inserted between ADJ and $V_{CCIN}$ (3 pin). The voltage can be changed by a maximum of ± 1V. |

**TIMING CHART** (TD62650F, TD62652F)

BIAS

0

CONSTANT VOLTAGE OF 5-V

$V_{CCIN}$

92%

0

$C_T$ $R_T$ (Note)

TC

0

CK

0

$T_W$

$\overline{RESET}$

0

$T_{RST\,(1)}$  $T_{WD}$  $T_{RST\,(2)}$  $T_{RST\,(1)}$

92%

(Note) TD62650F incorporates RT (22kΩ (Typ.) only for $C_T$.)

**TIMING CHART** (TD62651F)

BIAS

0

CONSTANT VOLTAGE OF 5-V

$V_{CCIN}$

85%

0

$C_T$ $R_T$

TC

0

CK

0

$T_W$

$\overline{RESET}$

0

$T_{RST\,(1)}$  $T_{WD}$  $T_{RST\,(2)}$  $T_{RST\,(1)}$

85%
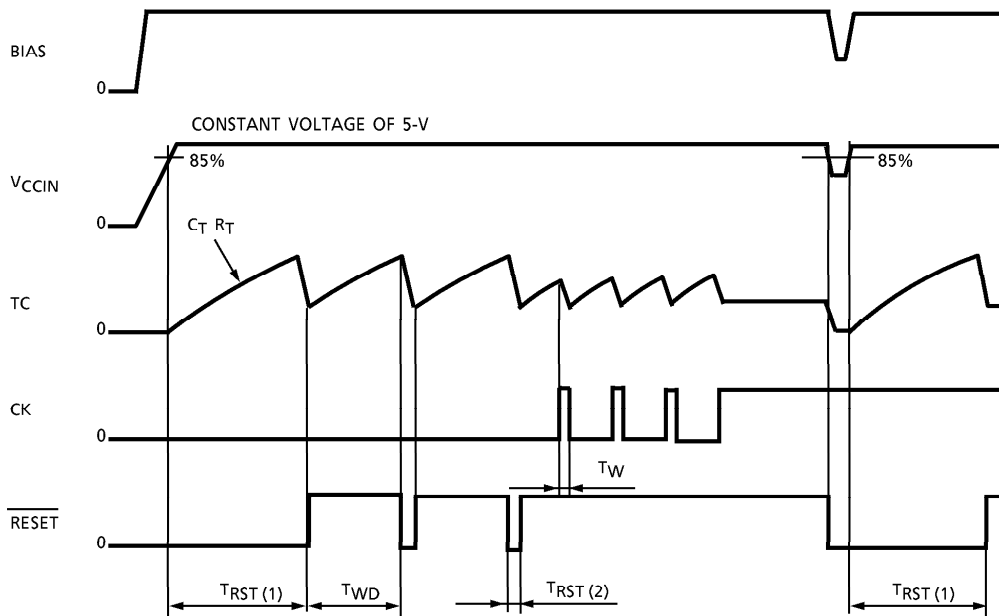
**MAXIMUM RATINGS** (Ta = 25°C)

| CHARACTERISTIC | SYMBOL | RATING | UNIT | PIN |
|---|---|---|---|---|
| Input Voltage | $VV_{CC24}$ | $-0.4\sim35$ | V | $V_{CC2}$, BIAS |
| | $VV_{CCIN}$ | $-0.4\sim7$ | V | $V_{CCIN}$ |
| | $V_{IN24}$ (Condition 1) (Condition 2) | $-0.4\sim VV_{CC2}+0.4$ $-0.4\sim30$ | V | SLSYN, 50/60, RXD |
| | $V_{IN5}$ | $-0.4\sim VV_{CCIN}+0.4$ | V | CPUOUT, MSCK, ADJ, COMP, CK, TC, SYNIN, MSTXD |
| Output Voltage | $V_{OUT24}$ | $-0.4\sim VV_{CC2}+0.4$ | V | MSSYN, TXD |
| | $VV_{CCOUT}$ | $-0.4\sim V_{BIAS}+0.4$ | V | $V_{CCOUT}$, OUT |
| | $V_{LED}$ (Condition 3) (Condition 4) | $-0.4\sim V_{BIAS}+0.4$ $-0.4\sim10$ | V | LED |
| | $V_{OUT5}$ | $-0.4\sim VV_{CCIN}+0.4$ | V | $\overline{RESET}$, CCK, HNSYN, SYN, SL50/60, MS50/60, TXDOUT, MSRXD, SLTXD |
| Output Current | $I_{OUT}$ | 10 | mA | OUT |
| | $I_{RESET}$ | 4 | mA | $\overline{RESET}$ |
| | $I_{OUT}$ Push/Pull | $\pm4$ | mA/ch | CCK, SYN, SL50/60, TXDOUT, SLTXD |
| | $I_{OUT5}$ | 10 | mA/ch | HNSYN, MS50/60, LED, MSRXD |
| | $I_{OUT24}$ | 24 | mA/ch | MSSYN, TXD |
| | $IV_{CCOUT}$ | 300 | mA | $V_{CCOUT}$ |
| Power Dissipation | $P_D$ (Note 5) | 1.47 | W | |
| Operating Temperature | $T_{opr}$ | $-40\sim85$ | °C | |
| Storage Temperature | $T_{stg}$ | $-55\sim150$ | °C | |

(Condition 1)   $VV_{CC2} \leqq 29.6V$
(Condition 2)   $VV_{CC2} > 29.6V$
(Condition 3)   $V_{BIAS} \leqq 9.6V$
(Condition 4)   $V_{BIAS} > 9.6V$
(Note 5)        Board mounting time (50 × 50 × 1.6mm, Cu = 30%)

## DC ELECTRICAL CHARACTERISTICS (Ta = 25°C, $V_{CCIN}$ = 5V)
### Interface Section

| CHARACTERISTIC | SYMBOL | PIN | TEST CIRCUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Input Voltage | $V_{IH5}$ | (Note 1) | — | | $V_{CCIN} \times 70\%$ | — | — | V |
| | $V_{IL5}$ | | | | — | — | $V_{CCIN} \times 30\%$ | |
| | $V_{IH24}$ | (Note 2) | | | 13 | — | $V_{CC2} + 0.4$ | |
| | $V_{IL24}$ | | | | − 0.4 | — | 7 | |
| Input Current | $I_{IH5-1}$ | (Note 3) | — | $V_{IN} = 5V$ | 320 | 462 | 600 | μA / ch |
| | $I_{IL5-1}$ | | | $V_{IN} = 0V$ | — | 0 | 10 | |
| | $I_{IH5-2}$ | (Note 7) | | $V_{IN} = 5V$ | 480 | 690 | 940 | μA |
| | $I_{IL5-2}$ | | | $V_{IN} = 0V$ | 115 | 170 | 240 | |
| | $I_{IH24}$ | (Note 2) | | $V_{IN} = 24V$ | 1.1 | 1.6 | 2.1 | mA / ch |
| | $I_{IL24}$ | | | $V_{IN} = 0V$ | 350 | 510 | 690 | μA |
| Output Voltage | $V_{OH5-1}$ | (Note 4) | — | $I_{OH} = -20 \mu A$ | $V_{CC} - 0.1$ | — | — | V |
| | $V_{OH5-2}$ | | | $I_{OH} = -4mA$ | $V_{CCIN} \times 70\%$ | — | — | |
| | $V_{OL5-1}$ | | | $I_{OL} = 20 \mu A$ | — | — | 0.1 | |
| | $V_{OL5-2}$ | | | $I_{OL} = 4mA$ | — | — | $V_{CCIN} \times 30\%$ | |
| | $V_{OL5-3}$ | (Note 5) | | $I_{IN} = 500 \mu A$ $I_{OL} = 10mA$ | — | — | 0.5 | |
| | $V_{OL}$ LED | LED | | $I_{IN} = 200 \mu A$ $I_{OL} = 1mA$ | — | — | 1.4 | |
| | $V_{OL24}$ | (Note 6) | | $I_{IN} = 200 \mu A$ $I_{OL} = 24mA$ | — | — | 0.5 | |
| Output Impedance | $R_{OL}$ LED | LED | — | (Note 8) | 540 | 680 | 1000 | Ω |
| | $R_{OH5}$ | (Note 5) | | (Note 9) | 3.2 | 4.7 | 6.2 | kΩ |
| Current Consumption 24 | $I_{VCC2}$ | | — | $V_{VCC2} = 24V$ | — | 1.6 | 2.1 | mA |
| Leakage Current | $I_{LEAK24}$ | (Note 6) | — | $V_{OH} = 24.0V$ | — | — | 10 | μA |
| | $I_{LEAK5}$ | (Note 4) | | $V_{OH} = 5V$ | — | — | 10 | |
| Output Shorting Current | $I_{OS}$ (*) | (Note 4) | — | $V_{CCIN} = 5.25V$ $V_{OH} = 0V$ | — | 17.5 | — | mA |

(*)　Two outputs or more must not be shorted at the same time.
　　　Shorting duration must be limited to less than 1 second.

(Note 1) CPUOUT, SYNIN, MSTXD　　　　　　(Note 5) HNSYN, MS50 / 60, MSRXD
(Note 2) SLSYN, 50 / 60, RXD　　　　　　　　(Note 6) MSSYN, TXD
(Note 3) SYNIN, MSTXD　　　　　　　　　　　(Note 7) CPUOUT
(Note 4) CCK, SYN, SL50 / 60, TXDOUT, SLTXD　(Note 8) ($V_{OL}$ (@$I_{OL}$ = 5mA) − $V_{OL}$ (@$I_{OL}$ = 1mA) )
　　　　　　　　　　　　　　　　　　　　　　　　　　　　÷ 4mA
　　　　　　　　　　　　　　　　　　　　　　(Note 9) 4V ÷ (@$I_{OH}$ ($V_{OH}$ = 0V) − @$I_{OH}$ ($V_{OH}$ = 4V) )

**DC ELECTRICAL CHARACTERISTICS** (Unless otherwise specified, $V_{BIAS}$ = 7 to 17V, Ta = − 40 to 85°C)
5V power supply, supply monitoring section

| CHARACTERISTIC | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Output Voltage | $V_{CCOUT}$ | — | $IV_{CCOUT}$ = 0.1A | 4.75 | 5.0 | 5.25 | V |
| Input Stability | $V_{CCOUT}$ LINE | — | $V_{BIAS}$ = 7~35V | — | 0.1 | 0.5 | % |
| Load Stability | $V_{CCOUT}$ LOAD | — | $IV_{CCOUT}$ = 1~150mA | — | 0.1 | 0.5 | % |
| Temperature Coefficient | $V_{CCOUT}$ t | — | | — | 0.01 | — | % / °C |
| Output Voltage | $V_{OL}$ $\overline{RESET}$ | — | $I_{OL}$ = 2mA | — | — | 0.5 | V |
| Output Leakage Current | $I_{LEAK}$ $\overline{RESET}$ | — | $V_{RESET}$ = 7V | — | — | 5 | $\mu$A |
| Input Current | $I_{TC}$ | — | $V_{TC}$ = 0 to 3.5V (Note 8) | − 3 | — | 3 | $\mu$A |
| Threshold Voltage | $V_{TC}$ H | — | $\overline{RESET}$ "High" to "Low" | — | 80% × $V_{CCIN}$ | — | V |
| | $V_{TC}$ L | | $\overline{RESET}$ "Low" to "High" | — | 40% × $V_{CCIN}$ | — | |
| Input Current | $I_{CK}$ | — | $V_{IN}$ = 5V (Note 8) | — | 0.3 | 0.7 | mA |
| Input Voltage | $V_{IH}$ | — | (Note 4) | $V_{CCIN}$ ×70% | — | — | V |
| | $V_{IL}$ | | | — | — | $V_{CCIN}$ ×30% | |
| Reset Detecting Voltage | $V_{CC}$ $\overline{RESET}$ | — | TD62650 / 652F | 89% × $V_{CCIN}$ | 92% × $V_{CCIN}$ | 95% × $V_{CCIN}$ | V |
| | | | TD62651F | 82% × $V_{CCIN}$ | 85% × $V_{CCIN}$ | 88% × $V_{CCIN}$ | |
| Output Impedance | $R_{OH}$ $\overline{RESET}$ | — | TD62650F (Note 1) | 3.2 | 4.7 | 6.2 | k$\Omega$ |
| | $R_{OH}$ TC | — | TD62650F (Note 1) | 15 | 22 | 29 | |
| Current Consumption 5 | $IV_{CCIN}$ | — | (Note 2) | — | 5 | 6.5 | mA |
| | | | (Note 5) | — | 11.5 | 15.0 | |
| Bias Current Consumption | $I_{BIAS}$ | — | $V_{BIAS}$ = 8V (Note 7) | — | 1.73 | 2.25 | mA |
| Watchdog Timer | $T_{WD}$ | — | TD62650F (Note 6) | 15.4 × CT | 24.2 × CT | 33.0 × CT | ms |
| | | | TD62651 / 2F | 0.9 × CTRT | 1.1 × CTRT | 1.3 × CTRT | s |
| Reset Timer (1) (Note 3) | $T_{RST (1)}$ | — | TD62650F (Note 6) | 24.2 × CT | 35.2 × CT | 48.4 × CT | ms |
| | | | TD62651 / 2F | 1.3 × CTRT | 1.6 × CTRT | 1.9 × CTRT | s |
| Reset Timer (Note 3) | $T_{RST (2)}$ | — | (Note 6) | 300 × CT | 600 × CT | 900 × CT | ms |

| CHARACTERISTIC | SYMBOL | TEST CIR-CUIT | TEST CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| Clock Input Pulse width | TW CK | — | | 3 | — | — | $\mu s$ |
| Maximum Response Frequency 1 | $f_{MAX}$ MSCK | — | | 2 | — | — | kHz |
| Maximum Response Frequency 2 | $f_{MAX}$ CK | — | | 10 | — | — | kHz |
| Msck Pin Input Signal Rise Time | tr MSCK | — | (Note 9) | — | — | 500 | ns |
| Minimum Input / Output Voltage Difference | $V_{OH}$ $V_{CCOUT}$ | — | $IV_{CCOUT} = 0.1A$ | — | — | 1.5 | V |

(Note 1)   $4V \div (@I_{OH} (V_{OH} = 0V) - @I_{OH} (V_{OH} = 4V)$

(Note 2)   $V_{BIAS} = 8V$, $V_{CCIN} - V_{CCOUT}$ Short
            Open Collector I/O    : Open
            Push-Pull I/O         : Open
            MSCK Input            : Open

(Note 3)   Reset Timer (1)       : Power On Reset Time
            Reset Timer (2)       : Watchdog Reset Time

(Note 4)   MSCK, CK Pins

(Note 5)   HNSYN, MS50/60, MSRXD Pull/UP Resistance + CCK, SYN, SL50/60, TXDOUT, SLTXD
            Driving Current

(Note 6)   CT Unit ($\mu$F)

(Note 7)   $V_{CCIN}$, $V_{CCOUT}$ Open

(Note 8)   Only TD62651F, TD62652F

(Note 9)   Input Condition 5V : 0 to 100%

## AC ELECTRICAL CHARACTERISTICS (Ta = 25°C)

| CHARACTERISTIC | CHARACTERISTIC / INPUT CONDITION | SYMBOL | TEST CIR-CUIT | OUTPUT CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Propagation Delay Time (tpLH : 50%-50%, tpHL : 50%-50%) | SLSYN-CCK (Note 1) | tpLH | — | (Note 4) | — | 0.6 | — | $\mu s$ |
| | | tpHL | | | — | 1.5 | — | |
| | SLSYN-SYN (Note 1) | tpLH | | (Note 4) | — | 0.6 | — | |
| | | tpHL | | | — | 1.5 | — | |
| | SLSYN-HNSYN (Note 1) | tpLH | | (Note 5) | — | 0.5 | — | |
| | | tpHL | | | — | 0.1 | — | |
| | 50 / 60-MS50 / 60 (Note 1) | tpLH | | (Note 5) | — | 0.5 | — | |
| | | tpHL | | | — | 0.1 | — | |
| | 50 / 60-SL50 / 60 (Note 1) | tpLH | | (Note 4) | — | 0.6 | — | |
| | | tpHL | | | — | 1.5 | — | |
| | SYNIN-MSSYN (Note 2) | tpLH | | (Note 3) | — | 1.0 | — | |
| | | tpHL | | | — | 0.1 | — | |
| | CPUOUT-TXDOUT (Note 2) | tpLH | | (Note 4) | — | 1.0 | — | |
| | | tpHL | | | — | 1.2 | — | |
| | MSTXD-LED (Note 2) | tpLH | | (Note 5) | — | 0.5 | — | |
| | | tpHL | | | — | 0.1 | — | |
| | MSTXD-TXD (Note 2) | tpLH | | (Note 3) | — | 1.0 | — | |
| | | tpHL | | | — | 0.1 | — | |
| | RXD-SLTXD (Note 1) | tpLH | | (Note 4) | — | 0.6 | — | |
| | | tpHL | | | — | 1.5 | — | |
| | RXD-MSRXD (Note 1) | tpLH | | (Note 5) | — | 0.5 | — | |
| | | tpHL | | | — | 0.1 | — | |
| Rise Time (tr : 10%-90%) | MS50 / 60 | tr | — | | — | 0.3 | — | $\mu s$ |
| | SL50 / 60 | | | | — | 0.2 | — | |
| | LED | | | | — | 0.2 | — | |
| | MSSYN | | | | — | 1.1 | — | |
| | TXDOUT | | | | — | 0.2 | — | |
| | TXD | | | | — | 1.1 | — | |
| | SYN | | | | — | 0.2 | — | |
| | CCK | | | | — | 0.2 | — | |
| | HNSYN | | | | — | 0.3 | — | |
| | SLTXD | | | | — | 0.2 | — | |
| | MSRXD | | | | — | 0.3 | — | |

| CHARACTERISTIC | CHARACTERISTIC / INPUT CONDITION | SYMBOL | TEST CIR-CUIT | OUTPUT CONDITION | MIN | TYP. | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| Fall Time (tf : 90%-10%) | MS50 / 60 | tf | — | | — | 0.1 | — | $\mu$s |
| | SL50 / 60 | | | | — | 0.5 | — | |
| | LED | | | | — | 0.1 | — | |
| | MSSYN | | | | — | 0.1 | — | |
| | TXDOUT | | | | — | 0.5 | — | |
| | TXD | | | | — | 0.1 | — | |
| | SYN | | | | — | 0.5 | — | |
| | CCK | | | | — | 0.5 | — | |
| | HNSYN | | | | — | 0.1 | — | |
| | SLTXD | | | | — | 0.5 | — | |
| | MSRXD | | | | — | 0.1 | — | |

Input / Output Conditions

- Input Condition

    (Note 1) 24-V System    :    0.2$\mu$s at 2 to 22-V

    (Note 2) 5-V System    :    0.1$\mu$s at 30 to 70%

- Output Conditions

    (Note 3) 24-V System    :    $C_L = 50pF$

    (Note 4) 5-V System    :    $C_L = 50pF$
    
    $R_L = 5k\Omega$

    (Note 5) 5-V System    :    $C_L = 50pF$

## APPLICATION CIRCUIT

When using an external PNP transistor :
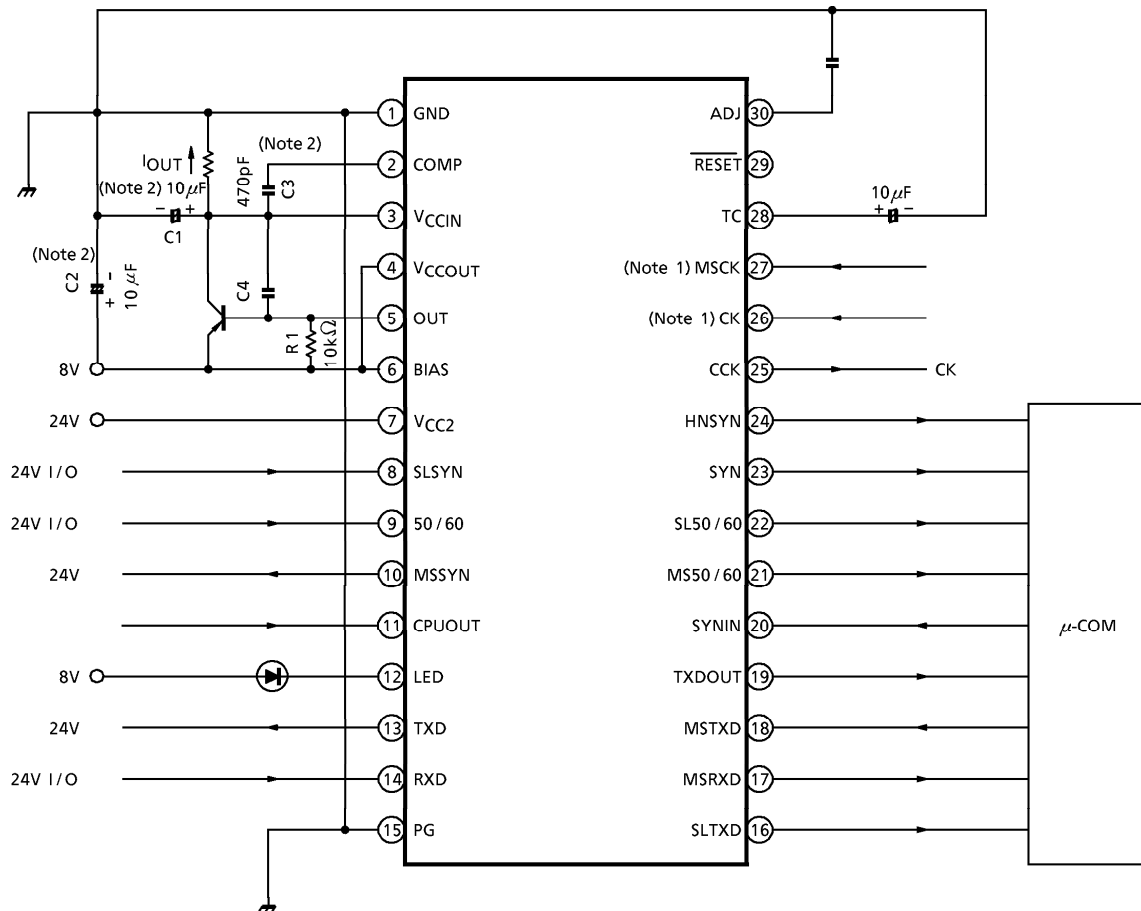


(Note 1) When using the MSCK pin, short circuit the CK pin with GND.

When using the CK pin, short circuit the MSCK pin with GND.

(Note 2) C1 and C2 are necessary to absorb external noise, etc. Connect them as close to the IC as possible.

C3 is used for phase correction, but this also must be connected as close to the IC as possible.

We recommend that C4 be connected between OUT and $V_{CCIN}$.

## PRECAUTIONS for USING

Utmost care is necessary in the design of the output line, $V_{CC}$ ($V_{CCIN}$, $V_{CCOUT}$, BIAS, $V_{CC2}$) and GND line since IC may be destroyed due to short-circuit between outputs, air contamination fault, or fault by improper grounding.

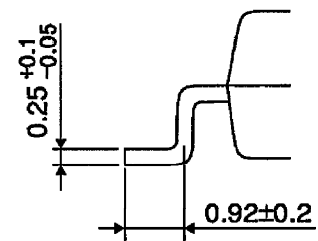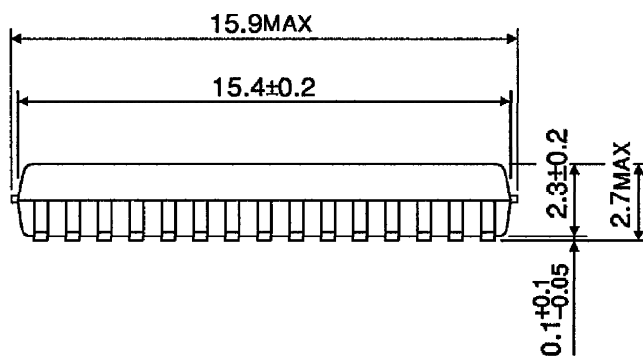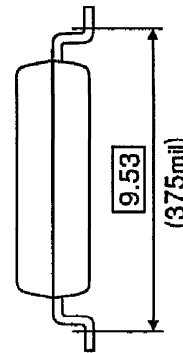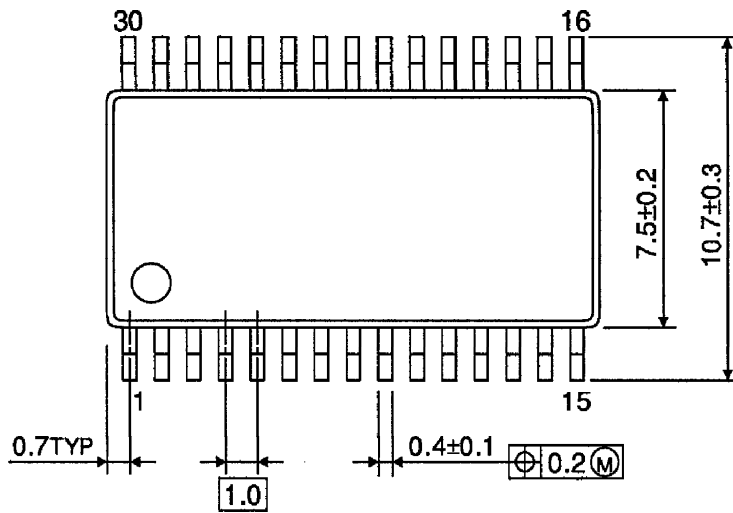When using a built-in PNP transistor :
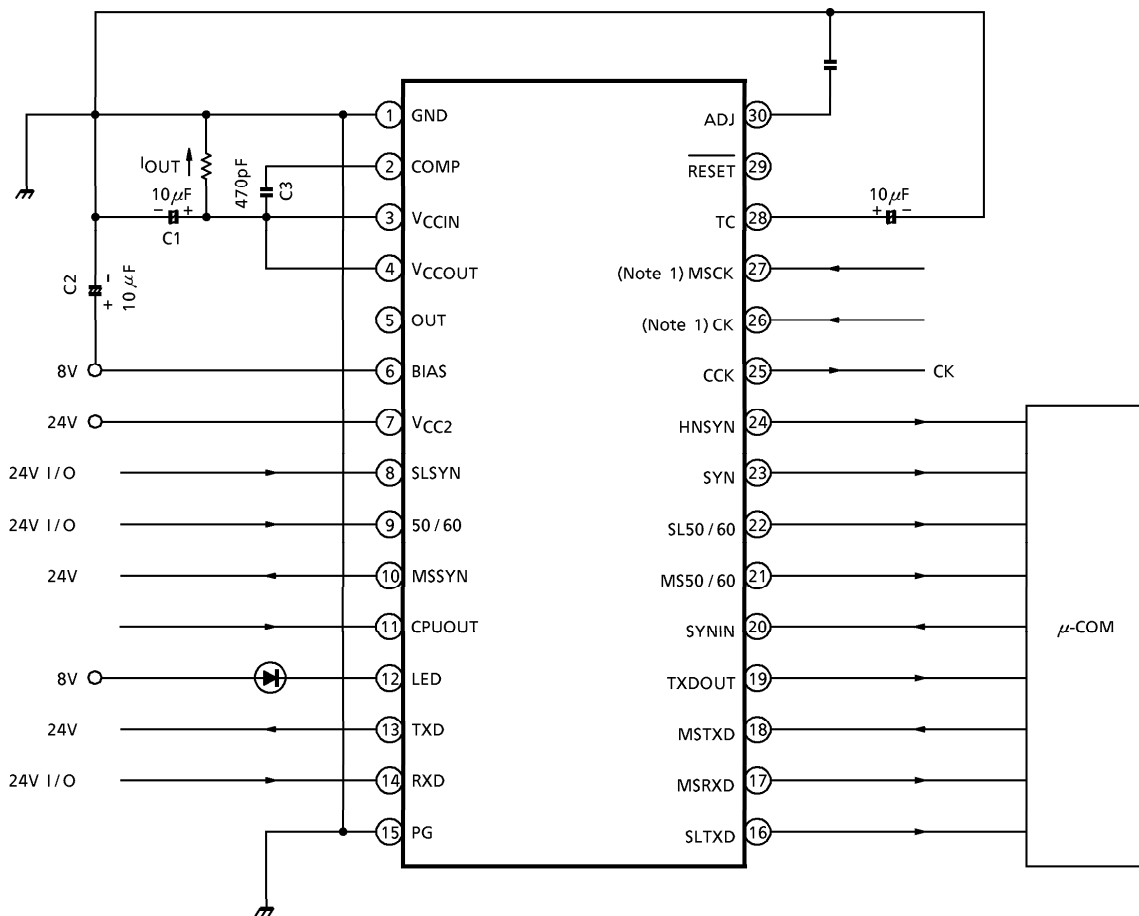


(Note 1)   When using the MSCK pin, short the CK pin with GND.
          When using the CK pin, short the MSCK pin with GND.
(Note 2)   C1 and C2 are necessary to absorb external noise, etc.
          Connect them as close to the IC as possible.
          C3 is used for phase correction, but this also must be connected as close to the IC as
          possible.

**OUTLINE DRAWING**

SSOP30-P-375-1.00

Unit : mm



Weight : 0.63g (Typ.)