# PIC18F6390/6490/8390/8490 Rev. B3 Silicon Errata

The PIC18F6390/6490/8390/8490 Rev. B3 parts you have received conform functionally to the Device Data Sheet (DS39629), except for the anomalies described below. Any Data Sheet Clarification issues related to the PIC18F6390/6490/8390/8490 will be reported in a separate Data Sheet errata. Please check the Microchip web site for any existing issues.

All of the issues listed here will be addressed in future revisions of the PIC18F6390/6490/8390/8490 silicon.

**The following silicon errata apply only to PIC18F6390/6490/8390/8490 devices with these Device/Revision IDs**:

| Part Number | Device ID | Revision ID |
|---|---|---|
| PIC18F6390 | 00 1011 101 | 00011 |
| PIC18F6490 | 00 0110 101 | 00011 |
| PIC18F8390 | 00 1101 100 | 00011 |
| PIC18F8490 | 00 0110 100 | 00011 |

The Device IDs (DEVID1 and DEVID2) are located at addresses 3FFFFEh:3FFFFFh in the device's configuration space. They are shown in hexadecimal in the format "DEVID2 DEVID1".

## 1. Module: MSSP

In its current implementation, the $I^2C$™ Master mode operates as follows:

a) The Baud Rate Generator for $I^2C$ in Master mode is slower than the rates specified in Table 15-3 of the Device Data Sheet.

For this revision of silicon, use the values shown in Table 1 in place of those shown in Table 15-3 of the Device Data Sheet. The differences are shown in **bold** text.

b) Use the following formula in place of the one shown in Register 15-4 (SSPCON1) of the Device Data Sheet for bit description SSPM3:SSPM0 = `1000`.

$SSPADD = INT((F_{CY}/F_{SCL}) - (F_{CY}/1.111\ MHz)) - 1$

**Date Codes that pertain to this issue:**

All engineering and production devices.

**TABLE 1: $I^2C$™ CLOCK RATE w/BRG**

| $F_{OSC}$ | $F_{CY}$ | $F_{CY} * 2$ | BRG Value | $F_{SCL}$ (2 Rollovers of BRG) |
|---|---|---|---|---|
| **40 MHz** | 10 MHz | 20 MHz | **0Eh** | 400 kHz(1) |
| **40 MHz** | 10 MHz | 20 MHz | **15h** | 312.5 kHz |
| **40 MHz** | 10 MHz | 20 MHz | **59h** | 100 kHz |
| **16 MHz** | 4 MHz | 8 MHz | **05h** | 400 kHz(1) |
| **16 MHz** | 4 MHz | 8 MHz | **08h** | 308 kHz |
| **16 MHz** | 4 MHz | 8 MHz | **23h** | 100 kHz |
| **4 MHz** | 1 MHz | 2 MHz | **01h** | 333 kHz(1) |
| **4 MHz** | 1 MHz | 2 MHz | **08h** | 100 kHz |
| **4 MHz** | 1 MHz | 2 MHz | 00h | 1 MHz(1) |

**Note 1:** The $I^2C$™ interface does not conform to the 400 kHz $I^2C$ specification (which applies to rates greater than 100 kHz) in all details, but may be used with care where higher rates are required by the application.

### 2. Module: MSSP

When the MSSP is configured for SPI™ Master mode, the SDO pin cannot be disabled by setting the TRISC<5> bit. The SDO pin always outputs the content of SSPBUF regardless of the state of the TRIS bit.

In Slave mode with Slave Select enabled, SSPM3:SSPM0 = 0010 (SSPCON1<3:0>), the SDO pin can be disabled by placing a logic high level on the $\overline{SS}$ pin (RF7).

**Work around**

None.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 3. Module: MSSP

After an $I^2C$ transfer is initiated, the SSPBUF register may be written for up to 10 $T_{CY}$ before additional writes are blocked. The data transfer may be corrupted if SSPBUF is written during this time.

The WCOL bit is set any time an SSPBUF write occurs during a transfer.

**Work around**

Avoid writing SSPBUF until the data transfer is complete, indicated by the setting of the SSPIF bit (PIR1<3>).

Verify the WCOL bit (SSPCON1<7>) is clear after writing SSPBUF to ensure any potential transfer in progress is not corrupted.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 4. Module: MSSP

In 10-bit Addressing mode, when a Repeated Start is issued followed by the high address byte and a write command (R/$\overline{W}$ = 0), an ACK is not issued.

**Work around**

There are two work arounds available:

1. Single-Master Environment:
   In a single-master environment, the user must issue a Stop, then a Start, followed by a write to the address high, then the address low followed by the data.
2. Multi-Master Environment:
   In a multi-master environment, the user must issue a Repeated Start, send a dummy write command to a different address, issue another Repeated Start and then send a write to the original address. This procedure will prevent loss of the bus.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 5. Module: MSSP

$I^2C$ Receive mode should be enabled (i.e., RCEN bit should be set) only when the system is idle (i.e., when ACKEN, RCEN, PEN, RSEN and SEN all equal zero). It should not be possible to set the RCEN bit when the system is not idle, however, the RCEN bit can be set under this circumstance.

**Work around**

Wait for the system to become idle before setting the RCEN bit. This requires a check for the following bits to be clear:

ACKEN, RCEN, PEN, RSEN and SEN.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 6. Module: CCP

When operating either Timer1 or Timer3 as a counter with a prescale value other than 1:1 and operating the CCP in Compare mode with the Special Event Trigger (CCP1CON bits CCP1M3:CCP1M0 = 1011), the Special Event Trigger Reset of the timer occurs as soon as there is a match between TMRxH:TMRxL and CCPR1H:CCPR1L.

This differs from the PIC18F452, where the Special Event Trigger Reset of the timer occurs on the next prescaler output pulse after the match between TMRxH:TMRxL and CCPR1H:CCPR1L.

**Work around**

To achieve the same timer Reset period on the PIC18F8490 family as the PIC18F452 family for a given clock source, add 1 to the value in CCPR1H:CCPR1L. In other words, if CCPR1H:CCPR1L = x for the PIC18F452, to achieve the same Reset period on the PIC18F8490 family, CCPR1H:CCPR1L = x + 1, where the prescale is 1, 2, 4 or 8 depending on the T1CKPS1:T1CKPS0 bit values.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 7. Module: CCP

The CCP1 and CCP2, configured for PWM mode with 1:1 Timer2 prescaler and duty cycle set to the period minus 1, may result in the PWM output(s) remaining at a logic low level.

Clearing the PR2 register to select the fastest period may also result in the output(s) remaining at a logic low output level.

**Work around**

To ensure a reliable waveform, verify that the selected duty cycle does not equal the 10-bit period minus 1 prior to writing these locations, or use 1:4 or 1:16 Timer2 prescale. Also, verify the PR2 register is not written to 00h.

All other duty cycle and period settings will function as described in the Device Data Sheet.

The CCP modules remain capable of 10-bit accuracy.

**Date Codes that pertain to this issue:**

All engineering and production devices.

## 8. Module: A/D

The A/D offset is greater than the specified limit in Table 26-23 of the Device Data Sheet. The addition of Parameter A06A and updated conditions and limits are shown in **bold** text in Table 2.

**Work around**

Three work arounds exist.

1. Configure the A/D to use the VREF+ and VREF- pins for the voltage references. This is done by setting the VCFG<1:0> bits (ADCON1<5:4>).
2. Perform a conversion on a known voltage reference voltage and adjust the A/D result in software.
3. Increase system clock speed to 40 MHz and adjust A/D settings accordingly. Higher system clock frequencies decrease offset error.

**TABLE 2: A/D CONVERTER CHARACTERISTICS: PIC18F6390/6490/8390/8490 (INDUSTRIAL) PIC18LF6390/6490/8390/8490 (INDUSTRIAL)**

| Param No. | Symbol | Characteristic | Min | Typ | Max | Units | Conditions |
|---|---|---|---|---|---|---|---|
| **A06A** | **EOFF** | **Offset Error** | **—** | **—** | **<±1.5** | **LSb** | **VREF = VREF+ and VREF-** |
| A06 | EOFF | Offset Error | — | — | **<±3.5** | LSb | **VREF = VSS and VDD** |

**Date Codes that pertain to this issue:**

All engineering and production devices.

## 9. Module: BOD

The BOD module may reset below the minimum operating voltage of the device when configured for BORV1:BORV0 = 11. The updated Reset voltage specifications are shown in **bold** in Table 3.

**TABLE 3: BROWN-OUT RESET VOLTAGE**

| Param No. | Sym | Characteristic | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| D005 | VBOR | **Brown-out Reset Voltage** | | | | |
| | | PIC18LF6390/6490/8390/8490 | | | | |
| | | BORV1:BORV0 = 11 | **N/A** | 2.05 | **N/A** | V |

**Work around**

Use the next higher BOD voltage setting to ensure a low VDD is detected above 2.0V.

**Date Codes that pertain to this issue:**

All engineering and production devices.

## 10. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTAx register is set), an ongoing transmission's timing can be corrupted if the TX9D bit (for the next transmission) is not written immediately following the setting of TXxIF. This is because any write to the TXSTAx register results in a reset of the Baud Rate Generator which will effect any ongoing transmission.

**Work around**

Load TX9D just after TXxIF is set, either by polling TXxIF or by writing TX9D at the beginning of the Interrupt Service Routine, or only write to TX9D when a transmission is not in progress (TRMT = 1).

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 11. Module: EUSART

When performing back-to-back transmission in 9-bit mode (TX9D bit in the TXSTAx register is set), the second byte may be corrupted if it is written into TXREGx immediately after the TMRT bit is set.

**Work around**

Execute a software delay, at least one-half the transmission's bit time, after TMRT is set and prior to writing subsequent bytes into TXREGx.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 12. Module: AUSART

The AUSART for PIC18F6390/6490/8390/8490 devices may not recognize a received Stop bit if the combined error rate is too high.

**Work around**

1. Increase the baud rate of the device by decrementing the SPBRGHx:SPBRGx register pair value by one. Verify that the new baud rate does not exceed the maximum combined error rate of the application.
2. Configure the transmitter to send two Stop bits.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 13. Module: Timer1/Timer3

When Timer1 or Timer3 is configured for external clock source and the CCPxCON register is configured with 0x0B (Compare mode, trigger special event), the timer is not reset on a Special Event Trigger.

**Work around**

Modify firmware to reset the Timer1/Timer3 registers upon detection of the compare match condition — TMRxL and TMRxH.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 14. Module: Timer1/Timer3

When Timer1 or Timer3 is in External Clock Synchronized mode and the external clock period is between 1 and 2 TCY, interrupts will occasionally be skipped.

**Work around**

Avoid using an external clock with a period (1/frequency) between 1 and 2 TCY.

**Date Codes that pertain to this issue:**

All engineering and production devices.

### 15. Module: Timer1/Timer3

When Timer1/Timer3 is operating in 16-bit mode and the prescale setting is not 1:1, a write to the TMR1H/TMR3H Buffer registers may lengthen the duration of the period between the increments of the timer for the period in which TMR1H/TMR3H was written.

**Work around**

Two work arounds are available: 1) Stop Timer1/Timer3 before writing the TMR1H/TMR3H registers; 2) Write TMR1L/TMR3L immediately after writing TMR1H/TMR3H.

**Date Codes that pertain to this issue:**

All engineering and production devices.

## 16. Module: Interrupts

If an interrupt occurs during a two-cycle instruction that modifies the STATUS, BSR or WREG register, the unmodified value of the register will be saved to the corresponding Fast Return (Shadow) register and upon a fast return from the interrupt, the unmodified value will be restored to the STATUS, BSR or WREG register.

For example, if a high priority interrupt occurs during the instruction, `MOVFF TEMP, WREG`, the `MOVFF` instruction will be completed and WREG will be loaded with the value of `TEMP` before branching to ISR. However, the previous value of WREG will be saved to the Fast Return register during ISR branching. Upon return from the interrupt with a fast return, the previous value of WREG in the Fast Return register will be written to WREG. This results in WREG containing the value it had before execution of `MOVFF TEMP, WREG`.

Affected instructions are:

`MOVFF Fs, Fd`
where `Fd` is WREG, BSR or STATUS;

`MOVSF Zs, Fd`
where `Fd` is WREG, BSR or STATUS; and

`MOVSS [Zs], [Zd]`
where the destination is WREG, BSR or STATUS.

**Work around**

1. Assembly Language Programming: If any two-cycle instruction is used to modify the WREG, BSR or STATUS register, do not use the `RETFIE FAST` instruction to return from the interrupt. Instead, save/restore WREG, BSR and STATUS via software per Example 8-1 in the Device Data Sheet. Alternatively, in the case of `MOVFF`, use the `MOVF` instruction to write to WREG instead. For example, use:

   ```
   MOVF TEMP, W
   MOVWF BSR
   ```

   instead of `MOVFF TEMP, BSR`.

2. C Language Programming: The exact work around depends on the compiler in use. Please refer to your C compiler documentation for details.

   If using the Microchip MPLAB® C18 C Compiler, define both high and low priority interrupt handler functions as “low priority” by using the `pragma interruptlow` directive. This directive instructs the compiler to not use the `RETFIE FAST` instruction. If the proper high priority interrupt bit is set in the IPRx register, then the interrupt is treated as high priority in spite of the `pragma interruptlow` directive.

   The following code snippet demonstrates the work around using the C18 compiler:

**Date Codes that pertain to this issue:**

All engineering and production devices.

```
#pragma interruptlow MyLowISR
void MyLowISR(void)
{
    // Handle low priority interrupts.
}

// Although MyHighISR is a high priority interrupt, use interruptlow pragma so that
// the compiler will not use retfie FAST.

#pragma interruptlow MyHighISR
void MyHighISR(void)
{
    // Handle high priority interrupts.
}

#pragma code highVector=0x08
void HighVector (void)
{
    _asm goto MyHighISR _endasm
}
#pragma code /* return to default code section */

#pragma code lowVector=0x18
void LowVector (void)
{
    _asm goto MyLowISR _endasm
}
#pragma code /* return to default code section */
```

## REVISION HISTORY

Rev A Document (8/2004)

First revision of this document which includes silicon issues 1-4 (MSSP), 5 (PWM), 6 (CCP), 7 (A/D), 8 (AUSART), 9 (Timer1/Timer3), 10 (Timer1) and 11 (LCD).

Rev B Document (2/2005)

Removed previous issue 11 (LCD). Added Date Code information for all issues and updated text in issues 1, 3, 4 and 5 (MSSP), 12 (AUSART), 14 (Timer1/Timer3) and added issues 6 (CCP), 9 (BOD), 10-11 (EUSART), 15 (Timer1/Timer3) and 16 (Interrupts).

**NOTES:**

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