HEWLETT PACKARD

Small Outline, 5 Lead, Low Input Current, High Gain Optocouplers

Technical Data

HCPL-M700
HCPL-M701

Features

- **Surface Mountable**
- **Very Small, Low Profile JEDEC Registered Package Outline**
- **Compatible with Infrared Vapor Phase Reflow and Wave Soldering Processes**
- **High Current Transfer Ratio - 2000%**
- **Low Input Current Capability - 0.5 mA**
- **TTL Compatible Output - V_{OL} = 0.1 V**
- **Guaranteed ac and dc Performance Over Temperature: 0°C to 70°C**
- **High Output Current - 60 mA**
- **Recognized under the Component Program of U.L. (File No. E55361) for Dielectric Withstand Proof Test Voltage of 2500 Vac, 1 Minute**

Description

These small outline, low input current, high gain optocouplers are single channel devices in a five lead miniature footprint. They are electrically equivalent to the following HP optocouplers:

SO-5 Package	Standard DIP	SO-8 Package
HCPL-M700	6N138	HCPL-0700
HCPL-M701	6N139	HCPL-0701

The SO-5 JEDEC registered (MO-155) package outline does not require “through holes” in a PCB. This package occupies approximately one-fourth the footprint area of the standard dual-in-line package. The lead profile is designed to be compatible with standard surface mount processes.

These high gain series optocouplers use a Light Emitting Diode and an integrated high gain photodetector to provide extremely high current transfer ratio between input and output. Separate pins for the photodiode and output stage results in TTL compatible saturation voltages and high speed operation. Where desired the V_{CC} and V_O terminals may be tied together to achieve conventional photodarlington operation.

CAUTION: The small device geometries inherent to the design of this bipolar component increase the component’s susceptibility to damage from electrostatic discharge (ESD). It is advised that normal static precautions be taken in handling and assembly of this component to prevent damage and/or degradation which may be induced by ESD.

The HCPL-M701 is for use in CMOS, LSTTL or other low power applications. A 400% minimum current transfer ratio is guaranteed over a 0-70°C operating range for only 0.5 mA of LED current.

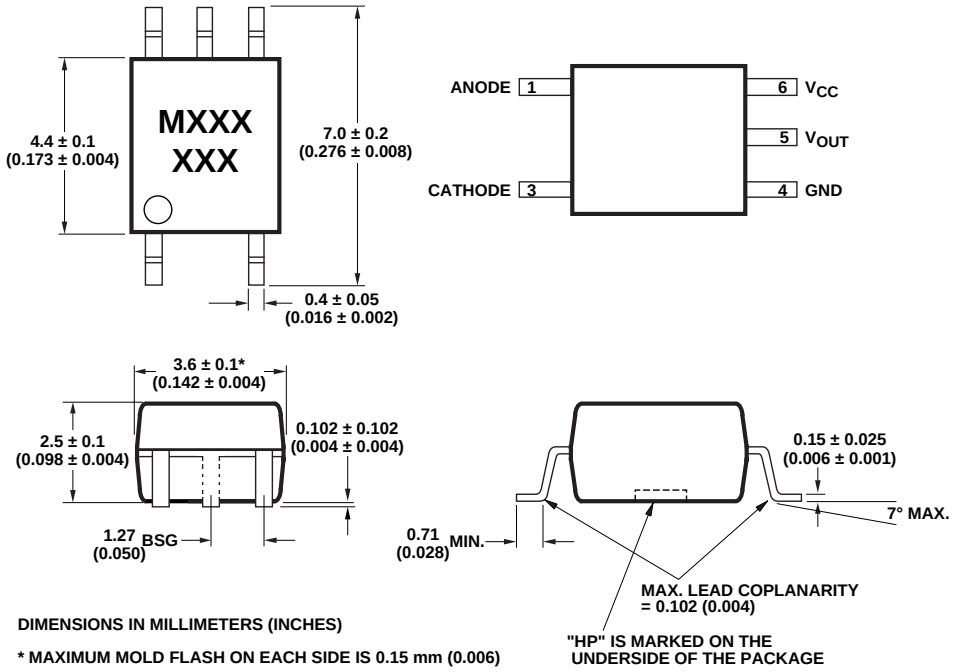
The HCPL-M700 is designed for use mainly in TTL applications. Current Transfer Ratio is 300% minimum over 0-70°C for an LED current of 1.6 mA [1 TTL Unit Load (U.L.)]. A 300% CTR enables operation with 1 U.L. out with a 2.2 kΩ pull-up resistor.

Selection for lower input currents down to 250 µA is available upon request.

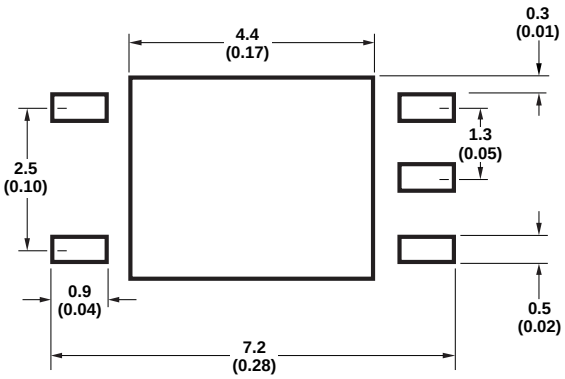
Applications

- **Ground Isolate Most Logic Families - TTL/TTL, CMOS/TTL, CMOS/CMOS, LSTTL/TTL, CMOS/LSTTL**
- **Low Input Current Line Receiver**
- **EIA RS232C Line Receiver**
- **Telephone Ring Detector**
- **ac Line Voltage Status Indicator - Low Input Power Dissipation**
- **Low Power Systems - Ground Isolation**

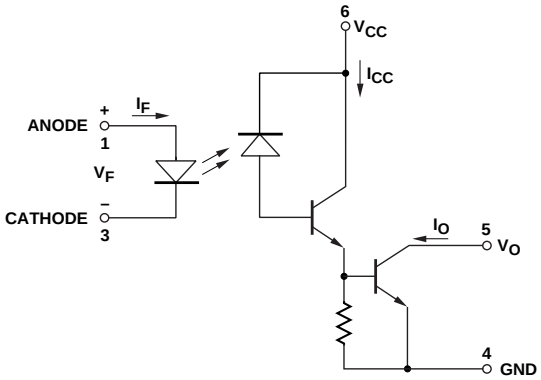
Outline Drawing (JEDEC MO-155)



Pin Location (for reference only)



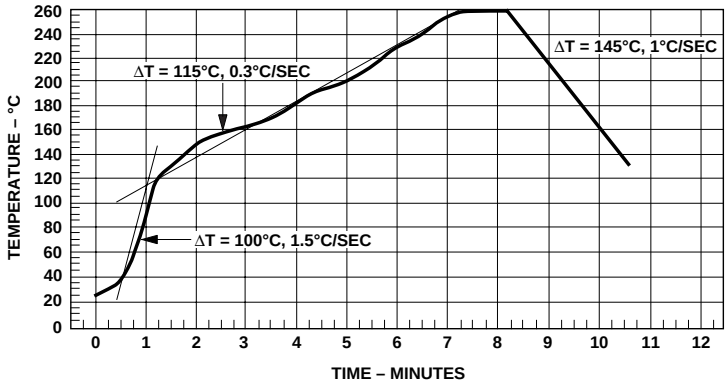
Schematic



Absolute Maximum Ratings

(No Derating Required up to 85°C)

Storage Temperature ..... -55°C to +125°C
Operating Temperature ..... -40°C to +85°C
Average Input Current - I_F ..... 20 mA
Peak Input Current - I_F ..... 40 mA
(50% duty cycle, 1 ms pulse width)
Peak Transient Input Current - I_F ..... 1.0 A
(≤1 µs pulse width, 300 pps)
Reverse Input Voltage - V_R ..... 5 V
Input Power Dissipation ..... 35 mW
Output Current - I_O (Pin 5) ..... 60 mA
Supply and Output Voltage - V_{CC} (Pin 6-4),V_O (Pin 5-4)
HCPL-M700 ..... -0.5 V to 7 V
HCPL-M701 ..... -0.5 V to 18 V
Output Power Dissipation ..... 100 mW
Infrared and Vapor Phase Reflow Temperature ..... see below



Maximum Solder Reflow Thermal Profile.
(Note: Use of Non-Chlorine Activated Fluxes is Recommended.)

Insulation Related Specifications

Parameter	Symbol	Value	Units	Conditions
Min. External Air Gap (Clearance)	L(IO1)	≥5	mm	Measured from input terminals to output terminals
Min. External Tracking Path (Creepage)	L(IO2)	≥5	mm	Measured from input terminals to output terminals
Min. Internal Plastic Gap (Clearance)		0.08	mm	Through insulation distance conductor to conductor
Tracking Resistance	CTI	175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group (per DIN VDE 0109)		IIIa		Material Group DIN VDE 0109

Electrical Specifications

Over recommended temperature (T_A = 0°C to 70°C) unless otherwise specified. (See note 6.)

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Units	Test Conditions	Fig.	Note
Current Transfer Ratio	CTR	M701	400	2000	3500	%	I_F = 0.5 mA, V_O = 0.4 V, V_{CC} = 4.5 V	2, 3	1
			500	1600	2600		I_F = 1.6 mA, V = 0.4 V, V_{CC} = 4.5 V		
		M700	300	1600	2600		I_F = 1.6 mA, V_O = 0.4 V, V_{CC} = 4.5 V		
Logic Low Output Voltage	V_{OL}	M701		0.1	0.4	V	I_F = 1.6 mA, I_O = 8 mA, V_{CC} = 4.5 V	1	
				0.1	0.4		I_F = 5 mA, I_O = 15 mA, V_{CC} = 4.5 V		
				0.2	0.4		I_F = 12 mA, I_O = 24 mA, V_{CC} = 4.5 V		
		M700		0.1	0.4		I_F = 1.6 mA, I_O = 24 mA, V_{CC} = 4.5 V		
Logic High Output	I_{OH}	M701		0.05	100	µA	I_F = 0 mA, V_O = V_{CC} = 18 V		
		M700		0.1	250		I_F = 0 mA, V_O = V_{CC} = 7 V		
Logic Low Supply Current	I_{CCL}			0.4	1.5	mA	I_F = 1.6 mA, V_O = Open, V_{CC} = 18 V		
Logic High Supply Current	I_{CCH}			0.01	10	µA	I_F = 0 mA, V_O = Open, V_{CC} = 18 V		
Input Forward Voltage	V_F			1.4	1.7	V	T_A = 25°C	4	
					1.75		I_F = 1.6 mA		
Input Reverse Breakdown Voltage	BV_R		5				I_R = 10 µA		
Temperature Coefficient of Forward Voltage	$\Delta V_F/\Delta T_A$			-1.8		mV/°C	I_F = 1.6 mA		
Input Capacitance	C_{IN}			60		pF	f = 1 MHz, V_F = 0		
Input-Output Insulation	V_{ISO}		2500			V_{RMS}	RH ≤ 50%, t = 1 min, T_A = 25°C		2, 3
Resistance (Input-Output)	R_{I-O}			10^{12}		Ω	V_{I-O} = 500 V_{DC}		2
Capacitance (Input-Output)	C_{I-O}			0.6		pF	f = 1 MHz		2

*All typicals at T_A = 25°C, V_{CC} = 5 V.

Switching Specifications

Over recommended temperature (T_A = 0°C to 70°C), V_{CC} = 5 V, unless otherwise specified.

Parameter	Symbol	Device HCPL-	Min.	Typ.*	Max.	Unit	Test Conditions	Fig.	Note
Propagation Delay Time to Logic Low at Output	t_{PHL}	M701		25	75	µs	T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	
					100				
				0.5	2		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					3				
		M700		5	20		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					25				
Propagation Delay Time to Logic High at Output	t_{PLH}	M701		10	60		T_A = 25°C, I_F = 0.5 mA, R_L = 4.7 kΩ	5, 6, 7	
					90				
				1	10		T_A = 25°C, I_F = 12 mA, R_L = 270 Ω		
					15				
		M700		10	35		T_A = 25°C, I_F = 1.6 mA, R_L = 2.2 kΩ		
					50				
Common Mode Transient Immunity at Logic High Output	$\|CM_H\|$		1,000	10,000		V/µs	I_F = 0 mA, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{p-p}	8	4, 5
Common Mode Transient Immunity at Logic Low Output	$\|CM_L\|$		1,000	10,000		V/µs	I_F = 1.6 mA, R_L = 2.2 kΩ, $\|V_{CM}\|$ = 10 V_{p-p}	8	4, 5

*All typicals at T_A = 25°C.

Notes:

1. dc CURRENT TRANSFER RATIO in percent is defined as the ratio of output collector current, I_O, to the forward LED input current, I_F, times 100.
2. Device considered a two terminal device: pins 1 and 3 shorted together, and pins 4, 5 and 6 shorted together.
3. In accordance with UL 1577, each optocoupler is proof tested by applying an insulation test voltage ≥ 3000 V_{RMS} for 1 second (leakage detection current limit, $I_{I-O} \leq 5$ µA).
4. Common transient immunity in a Logic High level is the maximum tolerable (positive) dV_{CM}/dt on the rising edge of the common mode pulse, V_{CM}, to assure that the output will remain in a Logic High state (i.e., V_O > 2.0 V). Common mode transient immunity in a Logic Low level is the maximum tolerable (negative) dV_{CM}/dt on the falling edge of the common mode pulse signal, V_{CM}, to assure that the output will remain in a Logic Low state (i.e., V_O < 0.8 V).
5. In applications where dV/dt may exceed 50,000 V/µs (such as static discharge) a series resistor, R_{CC}, should be included to protect the detector IC from destructively high surge currents. The recommended value is R_{CC} = 220 Ω.
6. Use of a 0.1 µF bypass capacitor connected between pins 4 and 6 is recommended.

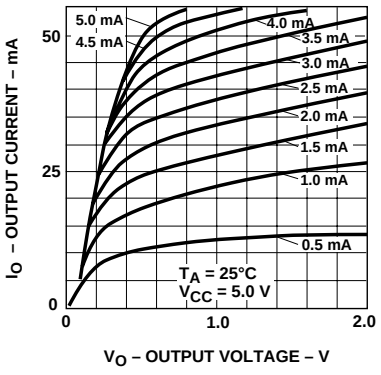


Figure 1. dc Transfer Characteristics.

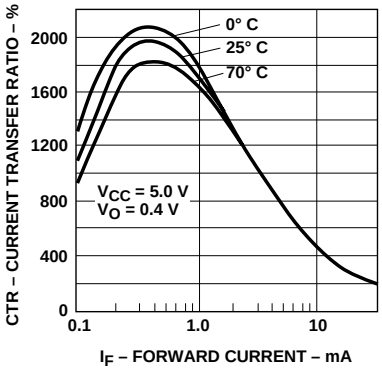


Figure 2. Current Transfer Ratio vs. Forward Current.

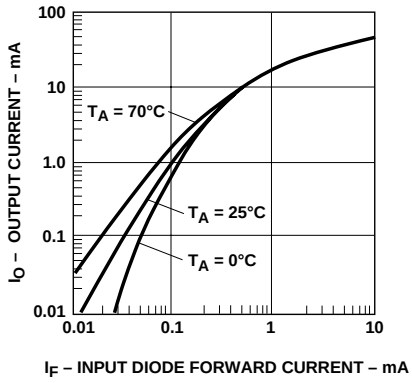


Figure 3. Output Current vs. Input Diode Forward Current.

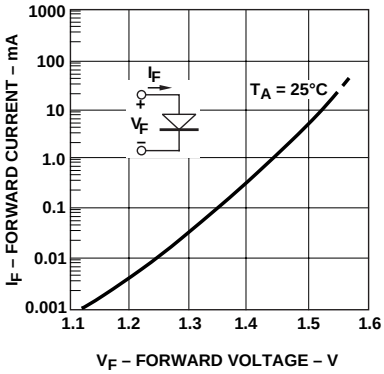


Figure 4. Input Diode Forward Current vs. Forward Voltage.

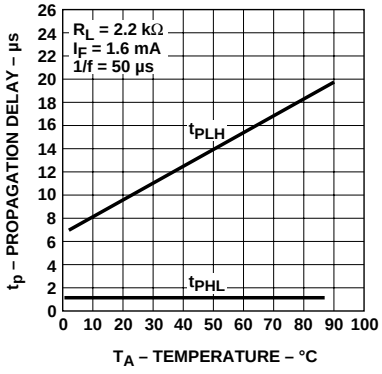


Figure 5. Propagation Delay vs. Temperature.

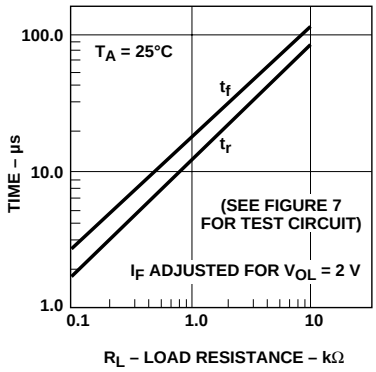


Figure 6. Non-Saturated Rise and Fall Times vs. Load Resistance.

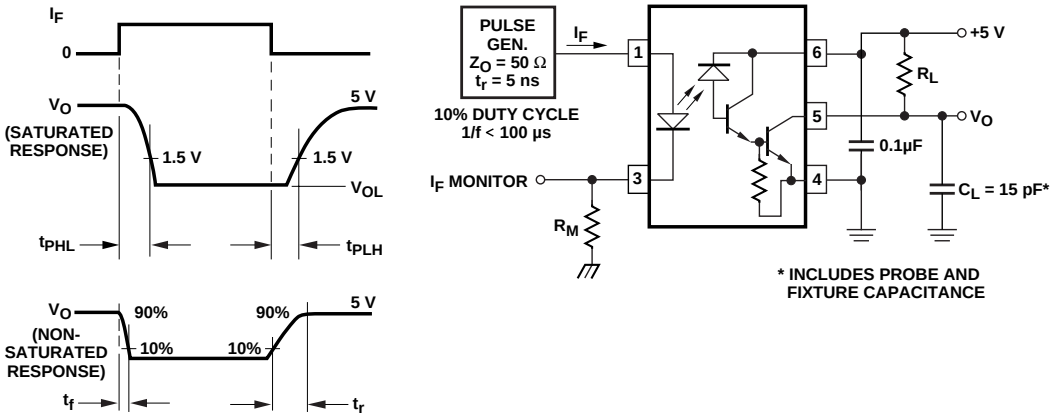


Figure 7. Switching Test Circuit.

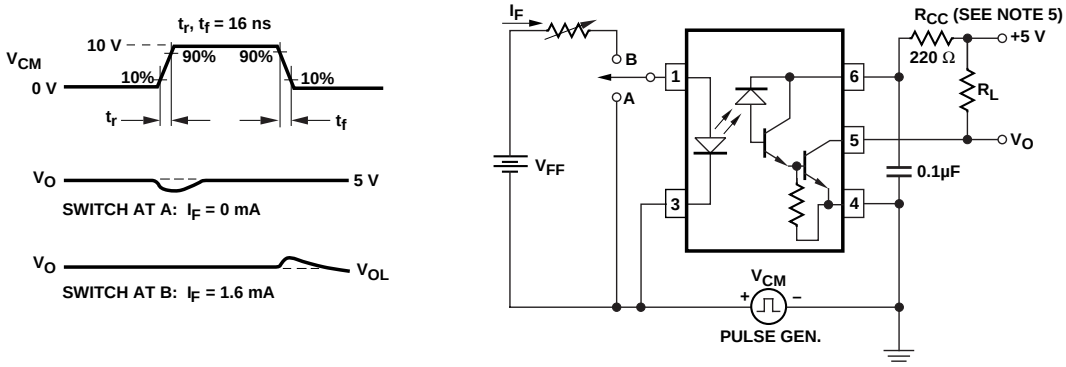


Figure 8. Test Circuit for Transient Immunity and Typical Waveforms.

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