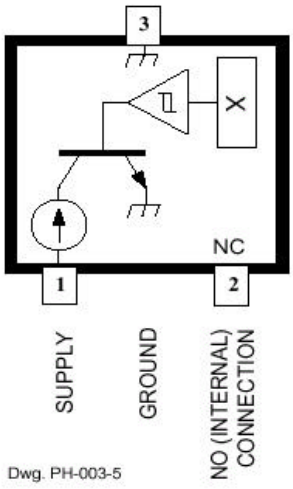
A1180 – A1184
Preliminary Data Sheet

PRELIMINARY DATA SHEET
SUBJECT TO CHANGE WITHOUT NOTICE

Suffix Code 'LH' Pinning
(SOT23W)



Pinning is shown viewed from branded side.

See typical application drawing for UA pinning.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage
V_{CC} ..... **26.5 V**
Reverse-Battery Voltage
V_{RB} ..... **-18 V**
Magnetic Flux Density
B ..... **Unlimited**
Package Power Dissipation θ_{ja},
UA..... **206 °C/W**
LH[1].....**248 °C/W**
Junction Temperature, T_J ..... **+170°C**
Operating Temperature Range, T_A
Suffix "E" ..... **- 40 °C to + 85 °C**
Suffix "L" ..... **- 40 °C to + 150 °C**
Storage Temperature Range
T_S ..... **-65 °C to +170 °C**

Two-Wire, Programmable, Chopper-Stabilized, Unipolar Hall-Effect Switch

The A118X is a two-wire, unipolar, Hall-effect switch family designed for use in high-temperature applications. This device uses a patented high frequency chopper-stabilization technique on Allegro's new DABIC5 BiCMOS wafer fabrication process to achieve magnetic stability and to eliminate offset inherent in single-element devices and from harsh-application environments.

The A118X FAMILY of devices incorporates a programmability function to allow for external trimming of the operate point. The programming is performed after final packaging of the sensor and placement of the Single In-Line Package (SIP) into the application. This advanced feature allows for optimization of sensor switching performance by effectively accounting for variations caused by magnet and SIP placement tolerances.

These devices provide on-chip transient protection. A zener clamp on the power supply protects against over-voltage conditions on the supply line.

The output of the A118X FAMILY, with the exception of the A1180/2, will switch HIGH in the presence of a sufficiently large south-pole magnetic field and will switch LOW with the removal of the field. The A1180/2 has the opposite polarity as the others, switching LOW in the presence of a sufficient magnetic field and HIGH with the removal of the field.

Two package styles provide a magnetically optimized package for most applications. Suffix "LH" is a miniature low profile package for surface-mount applications; suffix "UA" is a three-lead ultra-mini Single Inline Package (SIP) for through-hole mounting.

Factory programmed versions also available, see A1140/42/43/45. Programming software and/or hardware demonstration kits also available see ASEK-01 on the Allegro web site, www.allegromicro.com.

FEATURES / BENEFITS

- Chopper Stabilization
  - Extremely low switch-point drift
  - Low stress sensitivity
- One-time external programmability
  - Operate Point
- On-chip Protection
  - Supply transient protection
  - Robust ESD/EMC protection
  - Reverse-battery protection
- On-board Voltage Regulator
  - 3.8 V to 24 V operation

Order by complete part number (i.e. A1182LUA).

[1] The "LH" PPD is based on a 0.062" thick FR4, single-sided board using 2 oz. copper, with a 0.55 mm^2 area of copper attached to the ground lead.

CHARACTERISTICS

Valid over operating temperature range unless otherwise noted.

Part Number	Characteristics	Symbol	Test Conditions	Limits			
				Min.	Typ.	Max.	Units
ELECTRICAL CHARACTERISTICS							
A118X FAMILY	Supply Voltage	V_{CC}	Operating	3.8	-	24	V
A1182/3/4	Supply Current	$I_{GND(L)}$	Output I Low	5	-	6.9	mA
		$I_{GND(H)}$	Output I High	12	-	17	mA
A1180/1[2]	Supply Current	$I_{GND(L)}$	Output I Low	2	-	5	mA
		$I_{GND(H)}$	Output I High	12	-	17	mA
A118X	Output Rise Time[3]	t_r	R_L=100 Ohms, C_{BYP}=0.1uF	-	20	-	us
	Output Fall Time[3]	t_f	R_L=100 Ohms, C_{BYP}=0.1uF	-	20	-	us
	Chopping Frequency	f_C	-	-	340	-	kHz
	Power-Up Time	t_{on}	-	-	-	25	µs
	Power-Up State	POS	$t < t_{on}$, $t_r < 5us$, no bypass capacitor	-	HIGH	-	-
	Zener Voltage	V_Z	I = 10mA	28	36	40	V
MAGNETIC CHARACTERISTICS							
A1180/1/2/3[4]	Minimum Programmable Operate Point	B_{OPmin}	B>B_{op}, I_{GND}=Low (A1180/2) I_{GND}=High (A1181/3)	60			G
	Maximum Programmable Operate Point	B_{OPmax}				200	G
	Switch Point Step Size	B_{RES}	-		8		G
A1184[5]	Minimum Programmable Operate Point	B_{OPmin}	B>B_{op}, I_{GND}=High (A1184)	300			G
	Maximum Programmable Operate Point	B_{OPmax}				600	G
	Switch Point Step Size	B_{RES}	-		16		G
A118X	Number of Programming Bits	-	Switch Point	-	5	-	Bit(s)
			Programming Lock	-	1	-	Bit(s)
	Temperature Drift of B_{OP}	ΔB_{OP}	A1180-A1183			+/-20	G
	Hysterisis	B_{HYS}	B_{OP} - B_{RP}	5	15	30	G

[2] These are the A3161 current levels.
[3] Typical rise and fall time of the Hall sensor is 1us, the true rise and fall time is dependent on the load circuit as indicated by the 20us specification.
[4] Programming is typically performed at Ta = 25°C and does not take into account temperature drift of the switch point. See ΔB_{OP}.
[5] Programming is typically performed at Ta = 25°C and does not take into account temperature drift of the sw itch point. ΔB_{OP} has not yet been characterized for the A1184 and may require additional tolerance due to the high magnetic switch points.

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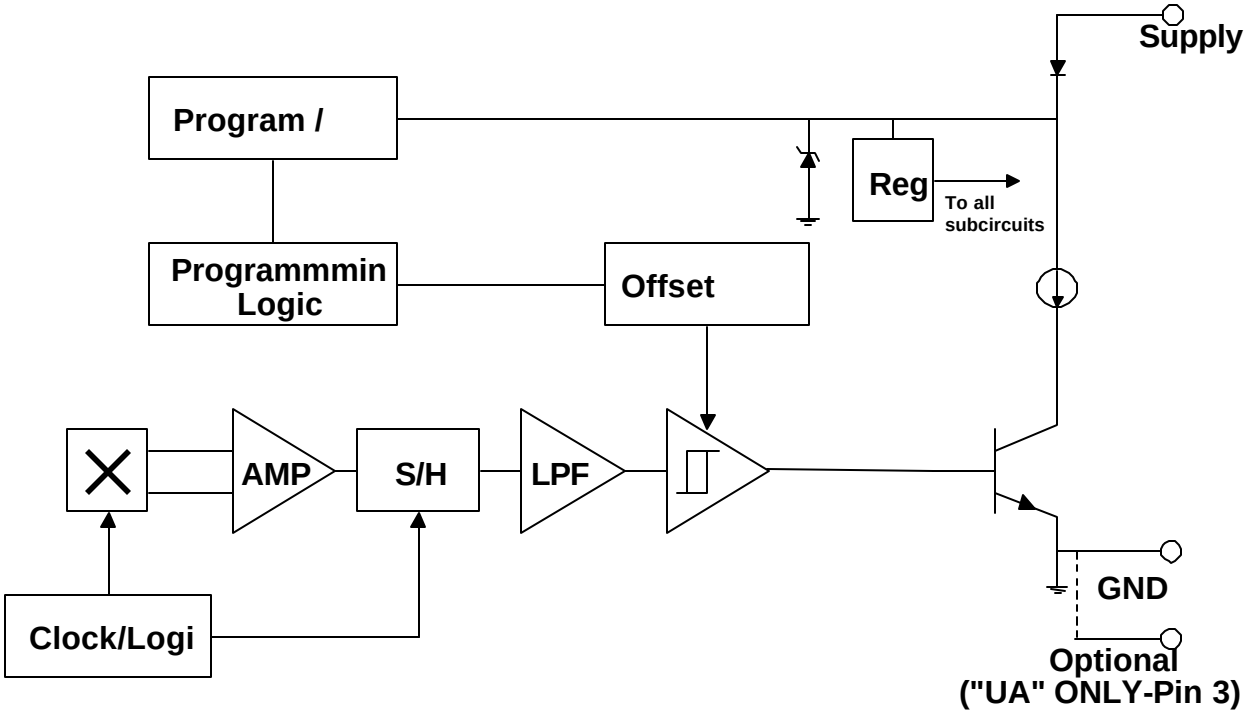
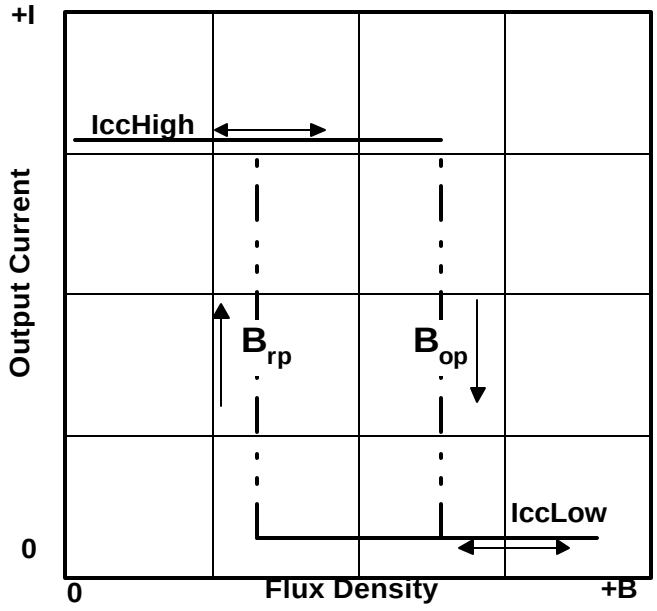
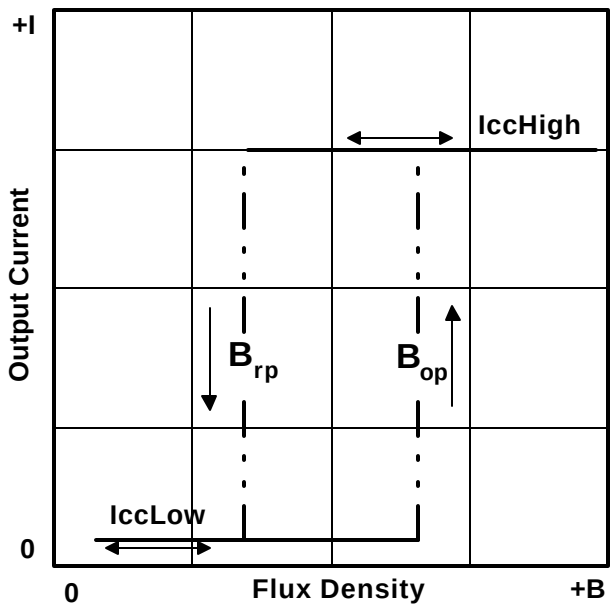
FUNCTIONAL BLOCK DIAGRAM



A1180/2 Hysteresis Curve



A1181/3/4 Hysteresis Curve



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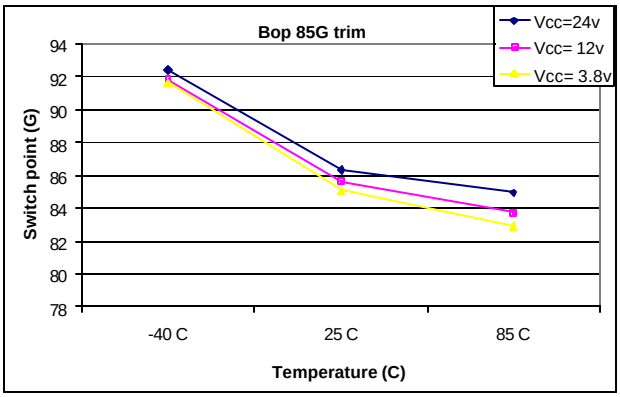
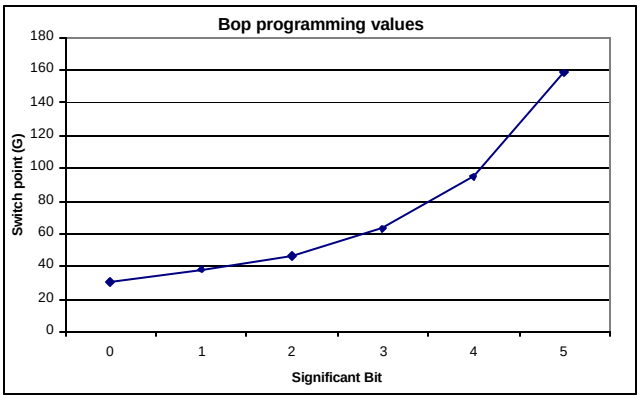
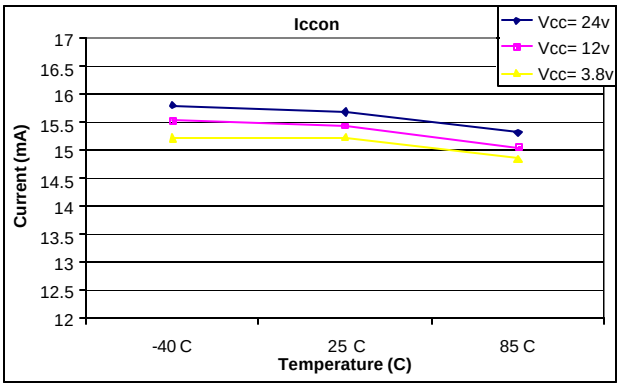
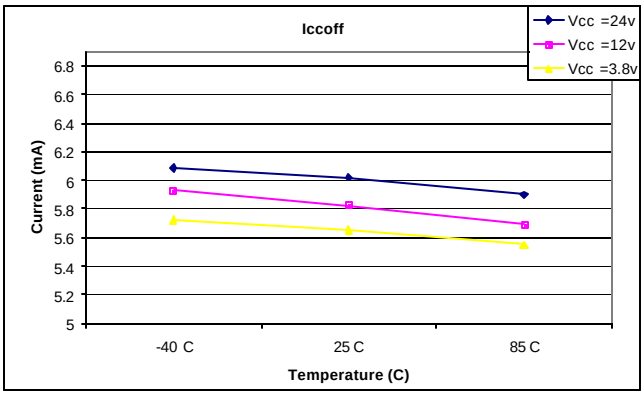
Typical Characterization Data

All data is the average of 1 Lot, >1000 Units









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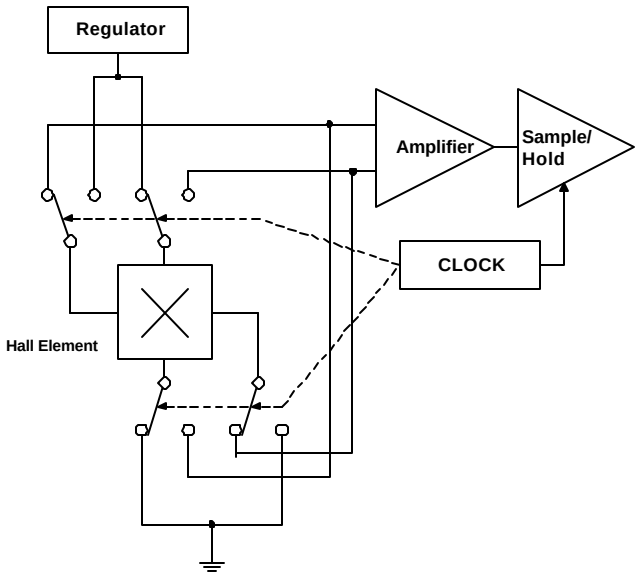
Functional Description

Chopper-Stabilization Technique. A limiting factor for switch point accuracy when using Hall effect technology is the small signal voltage developed across the Hall plate. This voltage is proportionally small relative to the offset that can be produced at the output of the Hall sensor. This makes it difficult to process the signal and maintain an accurate, reliable output over the specified temperature and voltage range.

Chopper Stabilization is a unique approach used to minimize Hall offset on the chip. The Allegro patented technique; dynamic quadrature offset cancellation, removes key sources of the output drift induced by temperature and package stress. This offset reduction technique is based on a signal modulation-demodulation process. The undesired offset signal is separated from the magnetically induced signal in the frequency domain through modulation. The subsequent demodulation acts as a modulation process for the offset causing the magnetically induced signal to recover its original spectrum at base band while the dc offset becomes a high frequency signal. Then, using a low-pass filter the signal passes while the modulated dc offset is suppressed.

The chopper stabilization technique uses a 170 kHz high frequency clock. The Hall plate chopping occurs on each clock edge resulting in a 340 kHz chop frequency. The high frequency operation allows for a greater sampling, which produces higher accuracy and faster signal processing capability. Using this chopper stabilization approach, the chip is de-sensitized to the effects of temperature and stress. This technique produces devices that have an extremely stable quiescent Hall output voltage, is immune to thermal stress, and has precise recoverability after temperature cycling. This technique is made possible through the use of a BiCMOS process which allows the use of low offset and low noise amplifiers in combination with high-density logic integration and sample and hold circuits.

The repeatability of switching with a magnetic field is slightly affected using a chopper technique. Allegro's high frequency chopping approach minimizes the affect of jitter and makes it imperceptible in most applications. Applications that may notice the degradation are those that require the precise sensing of alternating magnetic fields such as ring magnet speed sensing. For those applications, Allegro recommends the "low jitter" family of digital sensors.



Concept of Dynamic Quadrature Offset Cancellation

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PROGRAMMING PROTOCOL

The operate points are programmed by serially addressing the devices through the supply terminal V_{CC} (pin 1). After the correct operate point is determined, the device programming bits are permanently blown, and a locking bit is blown to prevent any further programming.

Switch Point Program Enable. To program the device, a keying sequence is used to activate / enable the addressing mode as shown in Figure 1. This sequence consisting of a VPP pulse, one VPH pulse, and a VPP pulse with no supply interruptions, is designed to prevent the device from being programmed accidentally (e.g., as a result of noise on the supply line).

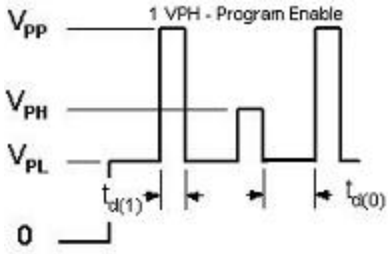

Figure 1. Program Enable Pulse Sequence.

Valid over operating temperature range unless otherwise noted.

Part Number	Characteristics	Symbol	Test Conditions	Limits			
				Min.	Typ.	Max.	Units
PROGRAMMING PROTOCOL (T_A = +25 °C)							
A118X Family	Programming Voltage[6]	V_{PL}	Minimum voltage range during programming	4.5	5	5.5	V
		V_{PH}		11.5	12.5	13.5	V
		V_{PP}		25	26	27	V
	Programming Current	I_{PP}	t_r = 11us, 5V→26V, C_{bypass} = 0.1uF	-	190	-	mA
	Pulse width	$t_{d(0)}$	OFF time between bits	20	-	-	µs
		$t_{d(1)}$	Pulse duration for enable and addressing sequences	20	-	-	µs
		t_{dP}	Pulse duration for fuse blowing	100	300	-	µs
	Pulse Rise Time	t_r	V_{PL} to V_{PH} or V_{PP}	5	-	100	µs
	Pulse Fall Time	t_f	V_{PH} or V_{PP} to V_{PL}	5	-	100	µs

[6] Programming Voltages are measured at Pin #1 (Vcc) of SIP. A minimum capacitance of 0.1uF must be connected from Vcc to GND of the SIP to provide the current necessary to blow the fuse.

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…PROGRAMMING PROTOCOL CONTINUED

Addressing. The magnetic operate point (Bop) is adjustable using 5 bits or 31 addresses. The 31 addresses are sequentially selected (Figure 2) until the required operate point is reached. Note that the difference between Bop and the magnetic release point (Brp), the Hysteresis (Hys), is fixed for all addresses.

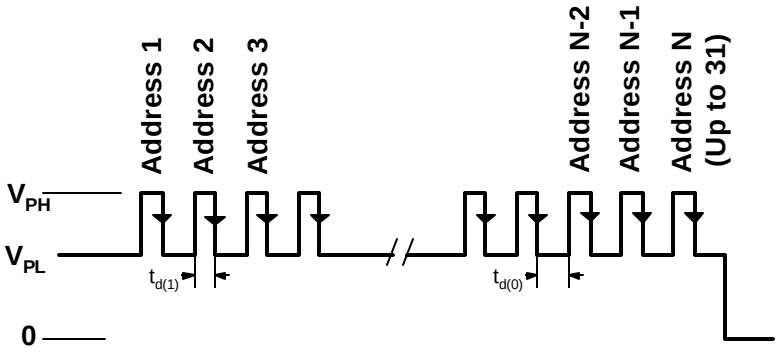

Figure 2. Sequential selected addresses.

Code Programming. After the desired switch point address is selected (0 through 31), each bit of the corresponding binary address should be programmed individually, not at the same time. For example, to program code 5 (binary 000101), bits 1 (code 1) and bit 3 (code 4) need to be programmed. Bit programming is accomplished by addressing the code and applying a V_{PP} pulse, the programming is not reversible. An appropriate sequence for blowing code 5 is shown in Figure 3.

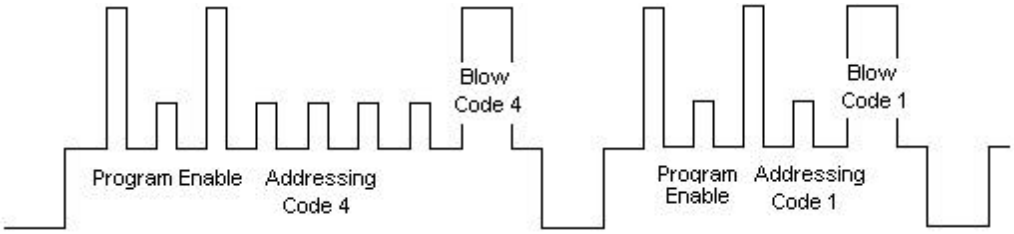

Figure 3. Bit programming.

Lock-Bit Programming. After the desired code is programmed, the lock bit, or code 32, can be programmed (figure 4) to prevent further programming of the device.

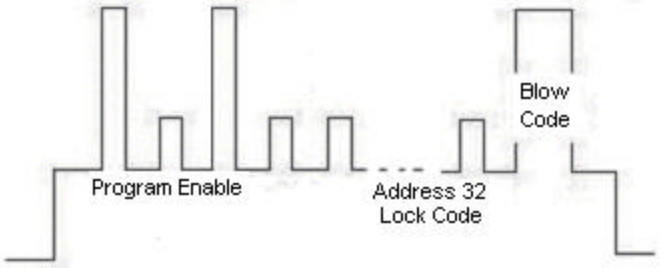

Figure 4. Lock-bit programming

See Allegro website at http://www.allegromicro.com for extensive information on device programming as well as programming products. Programming hardware is available for purchase and programming software is available for free.

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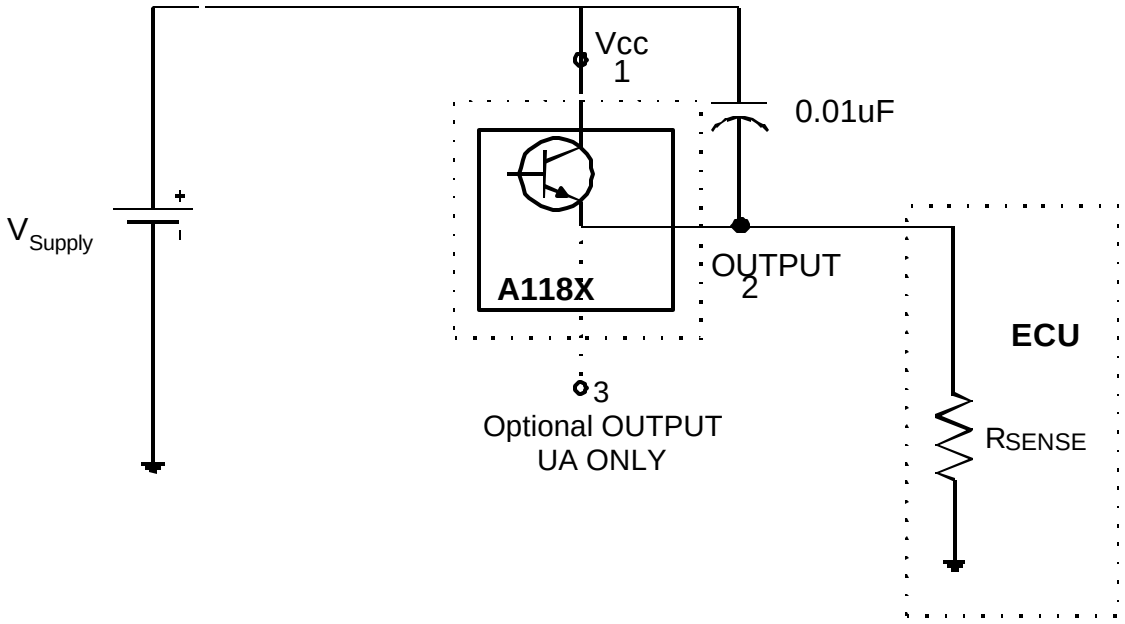
TYPICAL APPLICATION CIRCUIT

Applications. It is *necessary* that an external bypass capacitor be connected between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique and ensure sufficient energy to guarantee proper programming. (A 0.1uF cap is recommended for proper fuse blowing and may reside on the programming board) *The bypass capacitor in the application should be no further than 5 mm away from the Hall sensor.* The bypass capacitor is to protect the Hall IC only. All high frequency interferences conducted along the supply lines will be passed directly to the load through the bypass capacitor. Therefore, the ECU must have sufficient protection other than the bypass capacitor placed in parallel with the Hall IC.

A series resistor on the supply side, Rs (not shown), in combination with the bypass capacitor will create a filter for EMC pulses. The series resistor (Rs) and/or sense resistor (Rsense) will have voltage drops across them that must be considered for the minimum Vcc requirement of the device. The preferred sense resistor value is approximately 100 ohms. All programming, code and lock-bit programming, should be done directly across the part, between V_{CC} and Output with the use of a 0.1uF bypass capacitor. *Programming across the series resistor or sense resistor may not allow enough energy to properly blow the fuses. The result would be incorrect switch points.*

Typical Application (UA Pkg):



Extensive applications information on magnets and Hall-effect sensors including Chopper-Stabilization is available in the *Allegro Electronic Data Book* CD, or at the website: http://www.allegromicro.com .

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DEVICE QUALIFICATION PROGRAM

Test Name	Test Conditions	Test Length	# of Lots	Sample / lot	Comments
Pre/Post Test	Ta = room, hot, cold				
High Temperature Operating Life (HTOL)	Ta = 150°C, Tj ? 170°C	408 hrs	1	77	JESD22-A108
High Temperature Bake (HTB)	Ta = 170°C	1000 hrs	1	77	JESD22-A103
Pre Conditioning (PC)	85°C/85%RH	168 hrs	1	231	JESD22-A112 & A113
Temperature Humidity Bias (THB) or HAST	85°C/85%RH 130°C/85%RH	1000 hrs 50 hrs	1	77	JESD22-A101 JESD22-A110
Autoclave (AC)	121°C/15 psig	96 hrs	1	77	JESD22-A102
Temperature Cycle (TC)	-65°C to +150°C or -50°C to +150°C	500 cycles 1000 cycles	1	77	JESD22-A104
External Visual (EV)					
Physical Dimensions (PD)			1	30	
Lead Integrity Bond Pull Strength			1 1	45 30	
ESD	HBM & MM		1	3 per model per V step	JESD22-A114 & A115,CDF-AEC-Q100-002, 003 & 011
Solderability (SD)			1	15	JESD22-B102
Early Life Failure Rate (ELFR)	125°C or 150°C	48 hrs 24 hrs	1	800	JESD22-A108
Gate Leakage (GL)			1	6	CDF- AEC-Q100-006
Electrical Distributions (ED)	Ta = room, hot, cold		3	30	

EMC Requirements (Electromagnetic Compatibility)

Please contact your local representative for EMC results

Test Name	Reference Specification
ESD – Human Body Model	AEC-Q100-002
ESD – Machine Model	AEC-Q100-003
Conducted Transients	ISO 7637-1
Direct RF Injection	ISO 11452-7
Bulk Current Injection	ISO 11452-4
TEM Cell	ISO 11452-3

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POWER DE-RATING

Due to internal power consumption, the junction temperature of the IC, Tj, is higher than the ambient environment temperature, Ta. To ensure that the device does not operate above the maximum rated junction temperature use the following calculations:

$$\Delta T = P_D * R\theta ja$$

Where: $P_D = Vcc * Icc$

$$\therefore \Delta T = Vcc * Icc * R\theta ja$$

Where ΔT denotes the temperature rise resulting from the IC's power dissipation.

$$Tj = Ta + \Delta T$$

For the sensor :

Tj(max) = 170°C
Rθja (UA Pkg) = 206°C/W

Typical Tj calculation:

Ta = 25 °C
Vcc = 12 V
$Icc = Icc_{ONtyp}$ = 14.5 mA

$P_D = Vcc * Icc = 12\ V * 14.5\ mA = 174\ mW$

$\Delta T = P_D * R\theta ja = 174\ mW * 206°C/W = 35.8\ °C$

$Tj = Ta + \Delta T = 25\ °C + 35.8\ °C = 60.8\ °C$

Maximum Allowable Power Dissipation Calculation for A118X Family[7]:

Assume:

Ta = Ta_{max} = 150 °C
Tj(max) = 170°C
Icc = I_{ONmax} = 17 mA

If:

$$Tj = Ta + \Delta T$$

Then:

$$\Delta T_{max} = Tj_{max} - Ta_{max} = 170\ °C - 150\ °C = 20\ °C$$

If:

$$\Delta T = P_D * R\theta ja$$

Then:

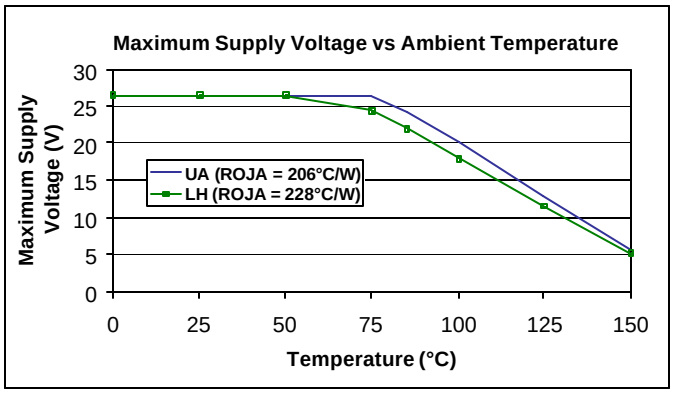
$P_{Dmax} = \Delta T_{max} / R\theta ja = 20\ °C / 206\ °C/W = 97.1\ mW$

If:

$$P_D = Vcc * Icc$$

Then the maximum Vcc at 150°C is therefore:

$Vccmax = P_{Dmax} / Icc = 97.1\ mW / 17\ mA = 5.7\ V$



[7] The "LH" PPD is based on a 0.062" thick FR4, single-sided board using 2 oz. copper, with a 0.55 mm^2 area of copper attached to the ground lead.

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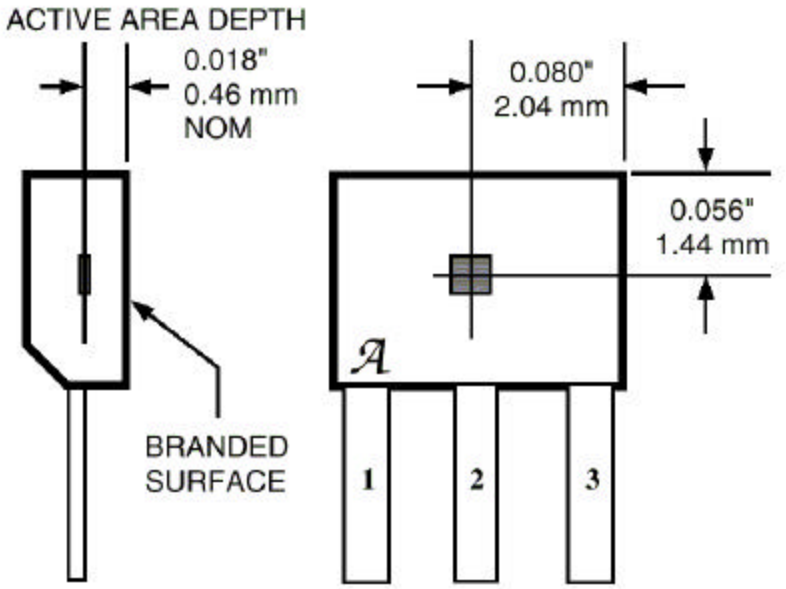
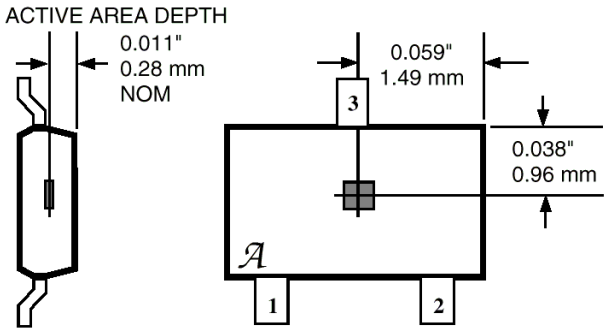
Package Designators 'UA' and 'UA-TL'



Dwg. MH-011-9A

Package Designator 'LH'



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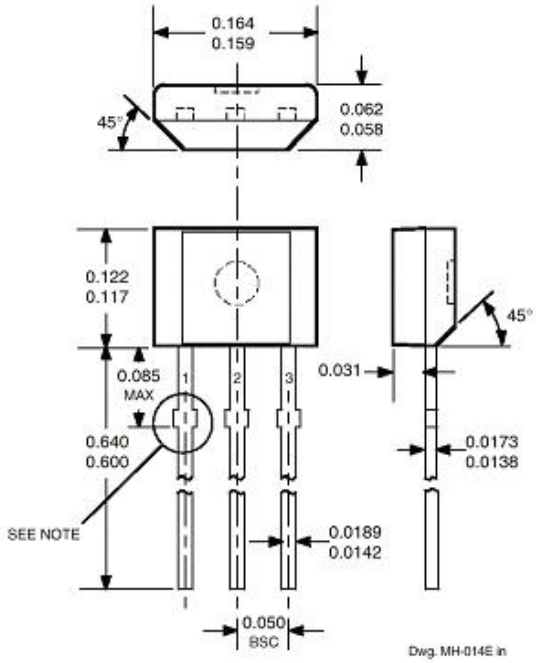
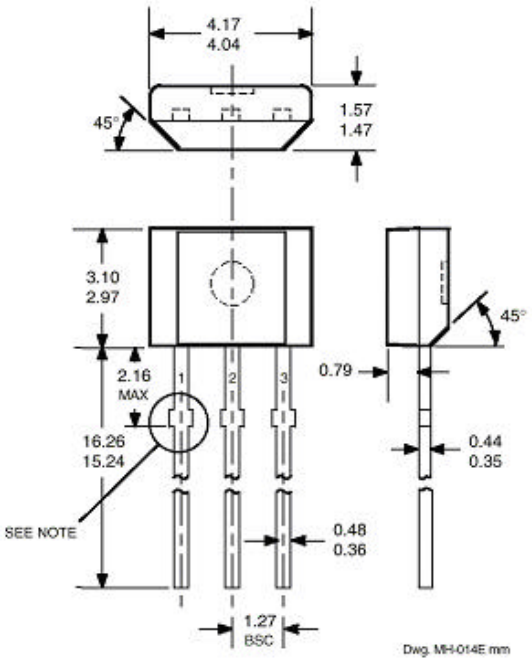
PACKAGE DESIGNATOR 'UA'

Dimensions in Inches
(controlling dimensions)



Dimensions in Millimeters
(for reference only)



NOTES:
1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Recommended minimum PWB hole diameter to clear transition area is 0.035" (0.89 mm).
5. Where no tolerance is specified, dimension is nominal.

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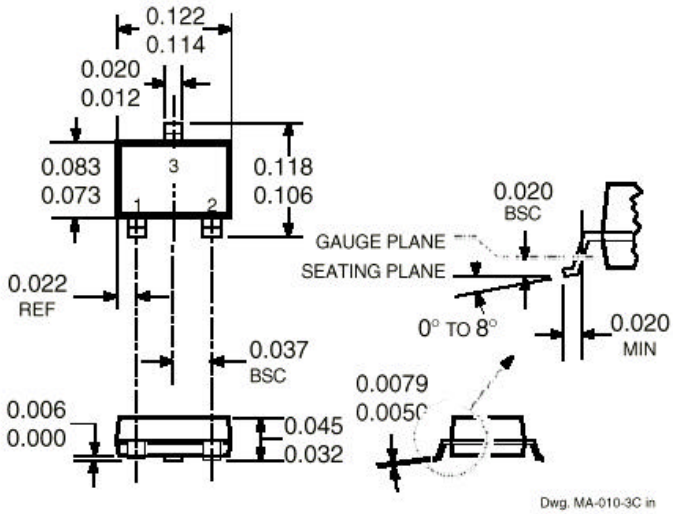
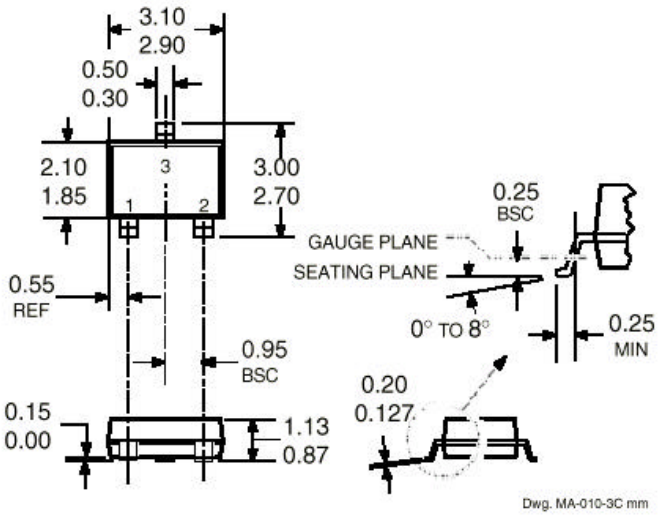
PACKAGE DESIGNATOR 'LH'

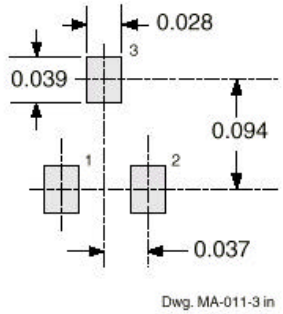
(fits SC-74A solder-pad layout)

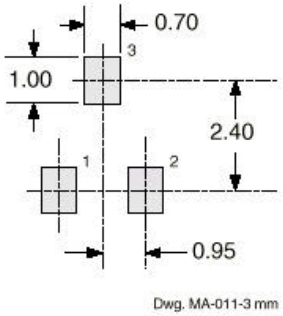
Dimensions in Inches
(for reference only)



Dimensions in Millimeters
(controlling dimensions)







NOTES:
1. Tolerances on package height and width represent allowable mold offsets. Dimensions given are measured at the widest point (parting line).
2. Exact body and lead configuration at vendor's option within limits shown.
3. Height does not include mold gate flash.
4. Where no tolerance is specified, dimension is nominal.
5. Add "LT" to part number for tape and reel.

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The products described herein are manufactured under one or more of the following U.S. patents: 5,045,920; 5,264,783; 5,442,283; 5,389,889; 5,581,179; 5,517,112; 5,619,137; 5,621,319; 5,650,719; 5,686,894; 5,694,038; 5,729,130; 5,917,320; and other patents pending.

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