Preliminary Product Information
November 1996 *(1 of 5)*

1.85 to 1.91 GHz 5V, 28.5 dBm, PCS Power Amplifier

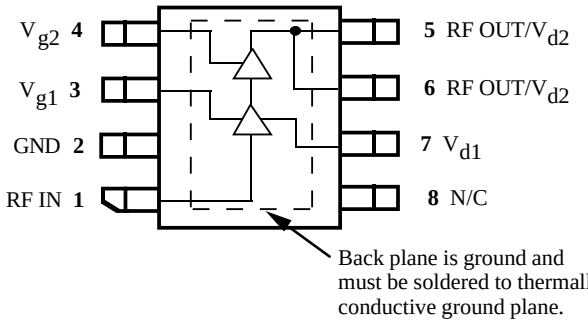
Features

- ❑ **30% Linear Power Added Efficiency**
- ❑ **28.5 dBm Output Power (ANSI J-STD-018 CDMA)**
- ❑ **24 dB Gain**
- ❑ **Tested Under Digital Modulation**
- ❑ **Low Cost SO-8 Surface Mount Package**

Applications

- ❑ **PCS Handsets**
- ❑ **PCS Base Stations**
- ❑ **Wireless Local Loop Subscriber Units**
- ❑ **1.6 GHz Satellite Subscriber Units**

Functional Block Diagram



Description

The CMM1321 is a 5 V linear power amplifier intended for use in PCS handsets, wireless local loop subscriber units and PCS base stations. The CMM1321 offers maximum performance and flexibility. The amplifier is designed to support the requirements of PCS CDMA (ANSI J-STD-018) systems.

The CMM1321 is packaged in a low-cost, space efficient SO-8 power package that gives excellent electrical stability and thermal handling performance with a R_Θ of less than 18° C/W. The part is designed to require minimal external circuitry for bias and matching, simplifying design and keeping board space and cost to a minimum. Through matching adjustment, equivalent performance can also be achieved for the 1.93 to 1.99 GHz PCS bands as well as the 1.6 GHz satellite bands.

Absolute Maximum Ratings

Parameter	Rating	Parameter	Rating	Parameter	Rating
Drain Voltage ($+V_d$)	+9.0 V*	Power Dissipation	5 W	Operating Temperature	-40°C to +100°C
Drain Current (I_d)	1.8 A	Thermal Resistance	18°C/W	Channel Temperature	175°C
RF Input Power	+15 dBm*	Storage Temperature	-65°C to +150°C	Soldering Temperature	260°C for 5 Sec.
DC Gate Voltage ($-V_g$)	-4.0 V*				

* Max ($+V_d$) and ($-V_g$) under linear operation. Max potential difference across the device in RF compression ($2V_d + |-V_g|$) not to exceed the minimum breakdown voltage (V_{br}) of +18V.

Recommended Operating Conditions

Parameter	Typ	Units	Parameter	Typ	Units
Drain Voltage ($+V_d$)	4.5 to 5.1	Volts	Operating Temperature (PC Board)	-30 to +80	°C

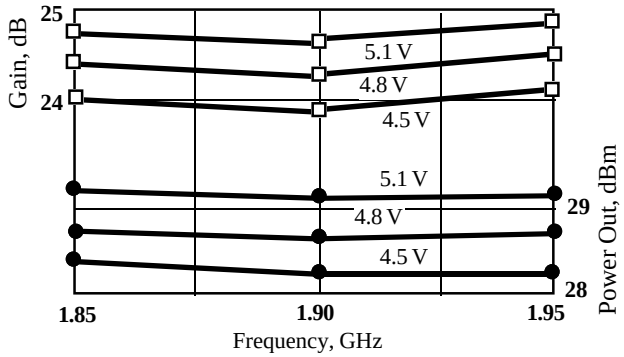
Electrical Characteristics

Unless otherwise specified, the following specifications are guaranteed at room temperature with drain voltage ($+V_d$) = 4.8 V in Celeritek test fixture.

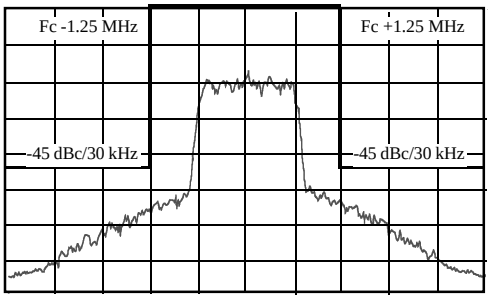
Parameter	Condition	Min	Typ	Max	Units
Frequency Range		1.85		1.91	GHz
Gain	@ Digital power output	22	24		dB
Power Output	Meets J-STD-018 CDMA mask	28.0	28.5		dBm
Harmonics	2nd @ Digital power output 3rd @ Digital power output		-35 -40	-30 -35	dBc dBc
Noise Figure			4.5	5.0	dB
Return Loss			10		dB
Efficiency	Pout CDMA	27	30		%
Positive Supply Current (I_d)	Pout CDMA		500		mA
Quiescent Current (I_q)	No RF		250		mA
Negative Supply Current ($-I_g$)			0.5	1.0	mA
Negative Supply Voltage ($-V_g$)		-1.3	-1.7	-2.2	V

Typical Performance

Gain & J-STD-018 CDMA Output Power vs Frequency Over Voltage @ +25°C

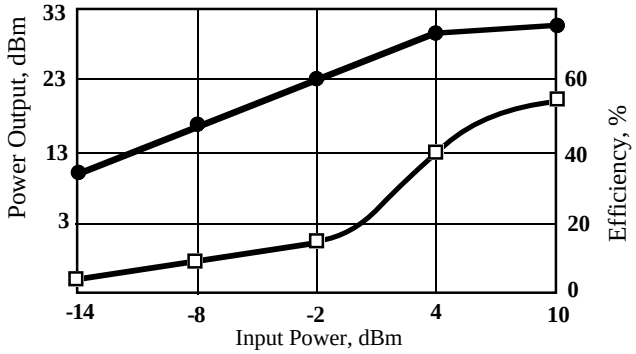


J-STD-018 CDMA Spectral Mask

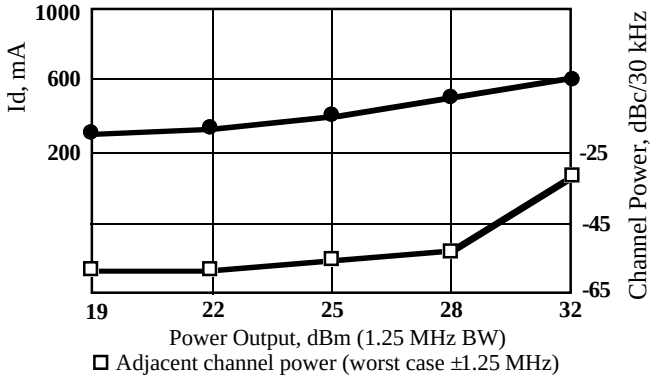


Span: 6.2 MHz, Frequency: 1880 MHz, RF Level: 28 dBm

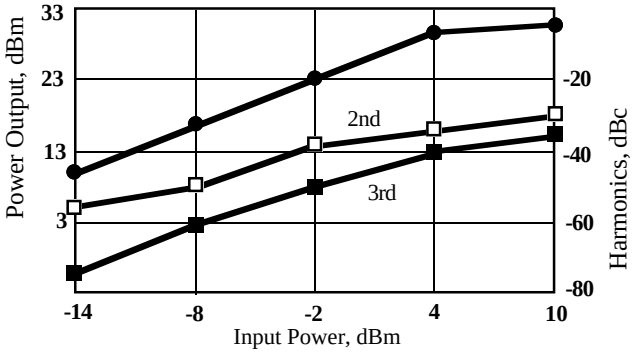
Power Output and Efficiency vs Input Power (4.8V, 1.88 GHz)



Id & J-STD-018 CDMA Channel Power vs Power Output (4.8V, 1.88 GHz)



Power Output, 2nd and 3rd Harmonics vs Input Power (4.8V, 1.88 GHz)



Typical Performance

Application Information

The CMM1321 is a two stage amplifier that requires a positive and negative supply voltage for proper operation. It is essential when turning on the device that the negative supply be applied before the positive supply. When turning the device off, the positive supply should be removed before the negative supply is removed.

The CMM1321 can be operated over a range of supply voltages and bias points. It is important that the maximum power dissipation of the package be observed at all times and that the maximum voltage across the device, as specified, is not exceeded.

Design Considerations

Biasing A negative voltage is needed to bias the 2 stage GaAs FET power amplifier. The output stage is controlled via Vg2 and the input stage via Vg1.

The positive supply voltage is applied to pins 5, 6 and 7. The negative voltage supply should be adjusted to achieve the typical quiescent current specified prior to characterization. The RF input (pin 1) is internally DC blocked.

Matching Circuits Input and output matching circuits are required. The CMM1321 evaluation board schematic and layout are on page 4. The test board is designed to be used at multiple frequencies. The matching elements for proper operation at 1.85–1.91 GHz are described on page 4.

A single shunt capacitor is used to match the output.

Note: Circuit board 8217 is a multiple-use test board.

The portions of the board that are used with the CMM1321 are shown as solid traces on the board layout drawing on page 4. The interface/connection points to the evaluation board are shown. These connection points may not be labeled identically on Celeritek's PB-CMM1321 evaluation board. Contact the factory for support in translating the external match to a specific application.

Supply Ramping To obtain the necessary power ramp, supply side switching should be used. Drain voltages should be tied together and ramped to produce the required power vs. time response.

Modulation When biased as specified, the CMM1321 will achieve the required adjacent channel response for the digital PCS system specified. Celeritek tests each product under digital modulation to ensure correlation to customer applications.

Thermal

1. The copper pad on the backside of the CMM1321 must be soldered to the ground plane.
2. All 8 leads of the package must be soldered to the appropriate electrical connection.
3. A large ground plane area with plated thru-holes as shown on the PCB layout should be used as a backside connection.

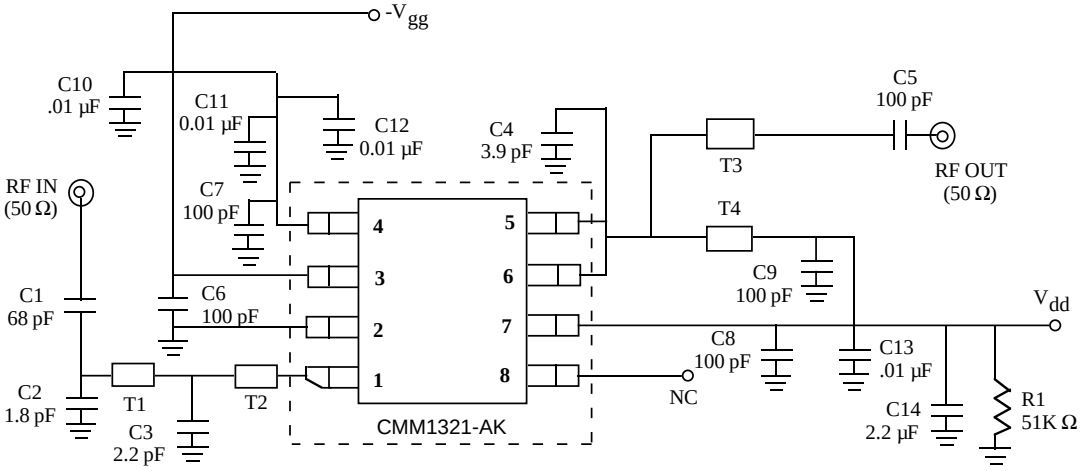
Contact the factory for a copy of a manufacturing application note containing more detailed information.

Test Circuits
Evaluation Board Schematic

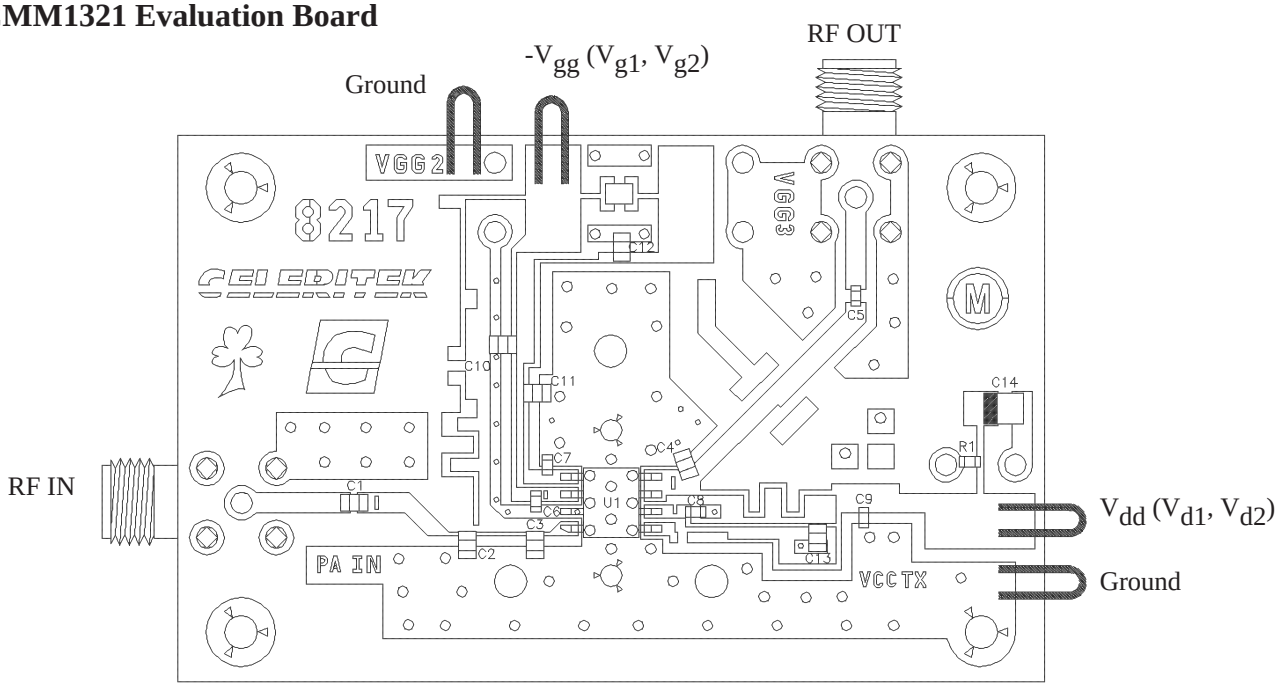
Board substrate:
ER = 4.60
Thickness = 0.031 in.

Transmission line electrical lengths at 1.88 GHz. (Dimensions in inches)

Line	Z (Ø)	E (°)
T1	75	9
T2	75	3
T3	65	16
T4	75	83



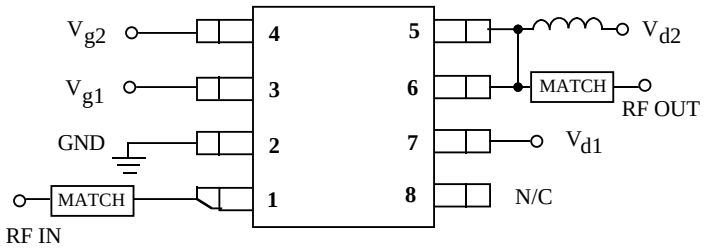
PB-CMM1321 Evaluation Board



Evaluation Board Parts List

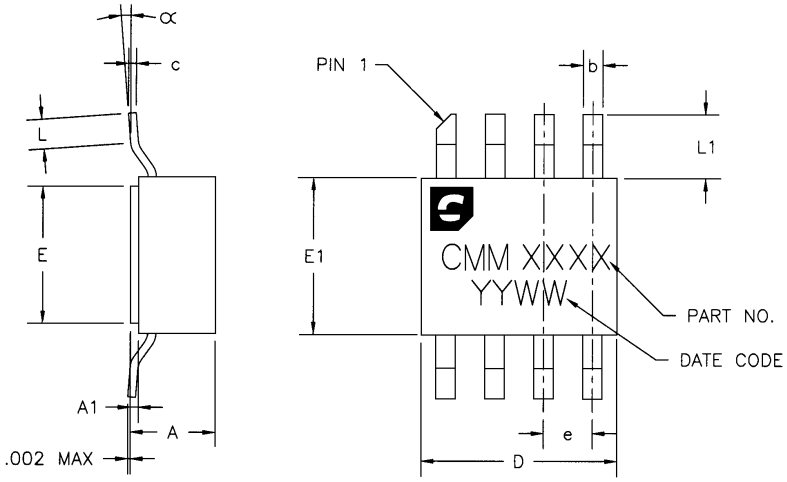
Part Type	Reference Designator	Description	Manufacturer	Part Number
Resistor	R1	51 KΩ 0603	Rohm	MCR 03J 513
Capacitor	C1	68 pF 0603 NPO	Rohm	MCH 185 A068JK
Capacitor	C2	1.8 pF 0603 NPO	Rohm	MCH 185 A1R8CK
Capacitor	C3	2.2 pF 0603 NPO	Rohm	MCH 185 A2R2CK
Capacitor	C4	3.9 pF 0603 NPO	Rohm	MCH 185 A3R9CK
Capacitor	C5, C6, C7, C8, C9	100 pF 0603 NPO	Rohm	MCH 185 A101JK
Capacitor	C11, C12, C13	0.01 µF 0805 X7R	Rohm	MCH 215 C103KK
Capacitor	C14	2.2 µF Tantalum	Matsuo	267 M2002225M

Connection Diagram and Pin Descriptions



Pin #	Name	Description
1	RF IN	RF input (DC Blocked)
2	GND	Ground
3	V_{g1}	Input stage gate bias
4	V_{g2}	Output stage gate bias
5	RF OUT/V_{d2}	RF output and V_{d2}. External matching circuit required
6	RF OUT/V_{d2}	RF output and V_{d2}. External matching circuit required
7	V_{d1}	Input stage drain bias
8	N/C	Ground this pin

Physical Dimensions



DIMENSION	MINIMUM	NOMINAL	MAXIMUM
A		.086[2.184]	.100[2.540]
A1	.005[.1270]	.008[.2032]	.011[.2794]
b	.017[.4318]	.020[.5080]	.023[.5842]
c	.007[.1778]	.008[2032]	.009[.2286]
D	.195[4.953]	.200[5.080]	.205[5.207]
E	.135[3.429]	.140[3.556]	.145[3.683]
E1	.155[3.937]	.160[4.064]	.165[4.191]
e		.050[1.270]	
L	.020[.5080]		.040[1.016]
L1	.055[1.397]	.065[1.651]	.075[1.905]
∝	0°		8°

DIMENSIONS IN INCHES [MILIMETERS]

Ordering Information

The CMM1321 is available in a surface mount SO-8 power package and devices are available in tape and reel.

Part Number for Ordering	Package
CMM1321-AK	**SO-8 surface mount power package**
CMM1321-AK-000T	**SO-8 surface mount power package in tape and reel**
PB-CMM1321	**Evaluation Board with SMA connectors**

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