LH5164A-10LF

64K Static RAM

(Model Number: LH516A2)

Spec. Issue Date: October 22, 2004
Spec No: EL16X051

SHARP

SPEC No. EL16X051
ISSUE: Oct. 22. 2004

To;

SPECIFICATIONS

Product Type 64k SRAM

Model No. LH5164A-10LF
(LH516A2)

*This specifications contains 18 pages including the cover and appendix.
If you have any objections, please contact us before issuing purchasing order.

CUSTOMER ACCEPTANCE

DATE:

BY:

PRESENTED
BY: M. Okada

M. OKADA
Dept. General Manager

REVIEWED BY: M. Kuwata

PREPARED BY: T. Morimura

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Integrated Circuits Group
SHARP CORPORATION

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- When using the products covered herein, please observe the conditions written herein and the precautions outlined in the following paragraphs. In no event shall the company be liable for any damages resulting from failure to strictly adhere to these conditions and precautions.

  (1) The products covered herein are designed and manufactured for the following application areas. When using the products covered herein for the equipment listed in Paragraph (2), even for the following application areas, be sure to observe the precautions given in Paragraph (2). Never use the products for the equipment listed in Paragraph (3).

  - Office electronics
  - Instrumentation and measuring equipment
  - Machine tools
  - Audiovisual equipment
  - Home appliances
  - Communication equipment other than for trunk lines

  (2) Those contemplating using the products covered herein for the following equipment which demands high reliability, should first contact a sales representative of the company and then accept responsibility for incorporating into the design fail-sale operation, redundancy, and other appropriate measures for ensuring reliability and safety of the equipment and the overall system.

  - Control and safety devices for airplanes, trains, automobiles, and other transportation equipment
  - Mainframe computers
  - Traffic control systems
  - Gas leak detectors and automatic cutoff devices
  - Rescue and security equipment
  - Other safety devices and safety equipment, etc.

  (3) Do not use the products covered herein for the following equipment which demands extremely high performance in terms of functionality, reliability, or accuracy.

  - Aerospace equipment
  - Communications equipment for trunk lines
  - Control equipment for the nuclear power industry
  - Medical equipment related to life support, etc.

  (4) Please direct all queries and comments regarding the interpretation of the above three Paragraphs to a sales representative of the company.

- Please direct all queries regarding the products covered herein to a sales representative of the company.

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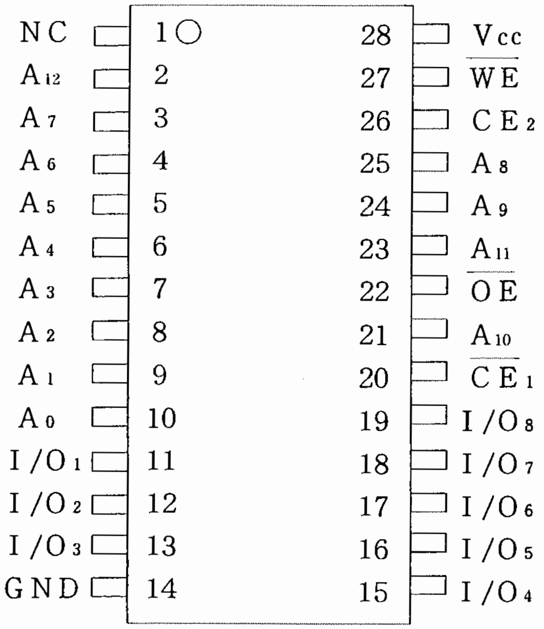
1. Decription

The LH5164A−10LF is a static RAM organized as 8, 192×8 bit with provides low-power standby mode.
It is fabricated using silicon-gate CMOS process technology.

Features

○Access Time · · · · 100 ns (Max.)
○Operating current · · · · 45 mA (Max.)
· · · · 10 mA (Max. t_{RC}, $t_{WC}=1\mu s$)
○Standby current · · · · 1.0 μA (Max.)
○Data retention current · · · · 0.2 μA (Max. $V_{CCDR}=3V$, $Ta=25℃$)
○Single power supply · · · · 5V±10%
○Operating temperature · · · · −10℃to+70℃
○Fully static operation
○Three-state output
○Not designed or rated as radiation hardened
○28pin DIP (DIP28−P−600) plastic package
○P-type bulk silicon

2. Pin Configuration


NC 1 ○ 28 Vcc
A12 2 27 $\overline{WE}$
A7 3 26 CE2
A6 4 25 A8
A5 5 24 A9
A4 6 23 A11
A3 7 22 $\overline{OE}$
A2 8 21 A10
A1 9 20 $\overline{CE_1}$
A0 10 19 I/O8
I/O1 11 18 I/O7
I/O2 12 17 I/O6
I/O3 13 16 I/O5
GND 14 15 I/O4

(Top View)

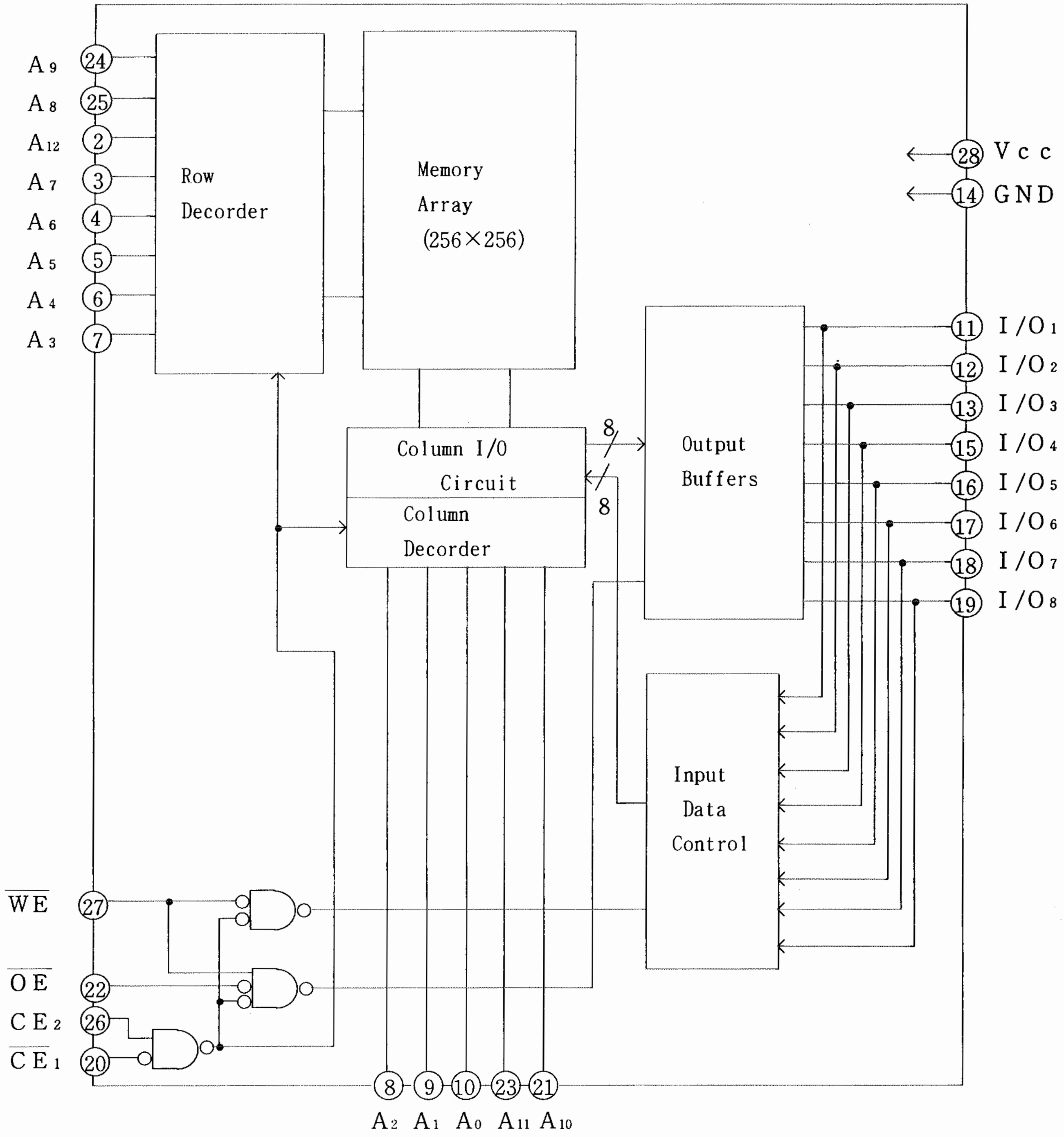
Pin Name	Function
A_0 to A_{12}	Address inputs
$\overline{CE_1}$/CE_2	Chip enable
$\overline{WE}$	Write enable
$\overline{OE}$	Output enable
I/O_1 to I/O_8	Data inputs/outputs
Vcc	Power supply
GND	Ground
NC	Non connection

3. Truth Table

$\overline{CE_1}$	CE_2	$\overline{WE}$	$\overline{OE}$	Mode	I/O_1 to I/O_8	Supply current
H	*	*	*	Standby	High impedance	Standby (I_{SB})
*	L	*	*	Standby	High impedance	Standby (I_{SB})
L	H	L	*	Write	Data input	Active (I_{CC})
L	H	H	L	Read	Data output	Active (I_{CC})
L	H	H	H	Output disable	High impedance	Active (I_{CC})

(*=Don't Care, L=Low, H=High)

4. Block Diagram


A9 24
A8 25
A12 2
A7 3
A6 4
A5 5
A4 6
A3 7
Row Decorder
Memory Array (256×256)
Vcc 28
GND 14
Column I/O Circuit
Column Decorder
8
8
Output Buffers
I/O1 11
I/O2 12
I/O3 13
I/O4 15
I/O5 16
I/O6 17
I/O7 18
I/O8 19
Input Data Control
WE 27
OE 22
CE2 26
CE1 20
8 9 10 23 21
A2 A1 A0 A11 A10

5. Absolute Maximum Ratings

Parameter	Symbol	Ratings	Unit
Supply voltage (*1)	V_{CC}	−0.3 to +7.0	V
Input voltage (*1)	V_{IN}	−0.3 (*2) to V_{CC}+0.3	V
Operating temperature	T_{opr}	−10 to +70	℃
Storage temperature	T_{stg}	−65 to +150	℃

Note) *1. The maximum applicable voltage on any pin with respect to GND.
*2. Undershoot of −3.0V is allowed width of pluse bellow 50ns.

6. Recommended DC Operating Conditions

(Ta= −10℃ to +70℃)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input voltage	V_{IH}	2.2		V_{CC}+0.3	V
	V_{IL}	−0.3 (*3)		0.8	V

Note) *3. Undershoot of −3.0V is allowed width of pluse below 50ns.

7. DC Electrical Characteristics

(Ta= −10℃ to +70℃, Vcc= 5V±10%)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Input leakage current	I_{LI}	V_{IN}=0V to V_{CC}		−1.0		1.0	μA
Output leakage current	I_{LO}	$\overline{CE_1}=V_{IH}$ or $CE_2=V_{IL}$ or $\overline{OE}=V_{IH}$ or $\overline{WE}=V_{IL}$ $V_{I/O}$=0V to V_{CC}		−1.0		1.0	μA
Operating supply current	I_{CC}	$\overline{CE_1}=V_{IL}$, $V_{IN}=V_{IL}$ or V_{IH} $CE_2=V_{IH}$, $I_{I/O}$=0mA	t_{CYCLE} =100ns			45	mA
	I_{CC1}	$\overline{CE_1}$=0.2V, V_{IN}=0.2V or V_{CC}−0.2V $CE_2=V_{CC}$−0.2V, $I_{I/O}$=0mA	t_{CYCLE} =1.0μs			10	mA
Standby current	I_{SB}	$\overline{CE_1}$, $CE_2 \geqq V_{cc}$−0.2V or $CE_2 \leqq$ 0.2V				1.0	μA
	I_{SB1}	$\overline{CE_1}$, $=V_{IH}$ or $CE_2=V_{IL}$				5	mA
Output voltage	V_{OL}	I_{OL}= 2.1mA				0.4	V
	V_{OH}	I_{OH}=−1.0mA		2.4			V

8. AC Electrical Characteristics

AC Test Conditions

Input pulse level	0.6 V to 2.4 V
Input rise and fall time	10 ns
Input and Output timing Ref. level	1.5 V
Output load	1TTL+C_L(100pF) (*4)

Note) *4. Including scope and jig capacitance.

Read cycle

(Ta= −10℃to+70 ℃, Vcc=5V±10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Read cycle time	t_{RC}	100			ns
Address access time	t_{AA}			100	ns
$\overline{CE_1}$ access time	t_{ACE1}			100	ns
CE_2 access time	t_{ACE2}			100	ns
Output enable to output valid	t_{OE}			40	ns
Output hold from address change	t_{OH}	10			ns
$\overline{CE_1}$ Low to output active	t_{LZ1}	10			ns
CE_2 High to output active	t_{LZ2}	10			ns
$\overline{OE}$ Low to output active	t_{OLZ}	5			ns
$\overline{CE_1}$ High to output in High impedance	t_{HZ1}	0		30	ns
CE_2 Low to output in High impedance	t_{HZ2}	0		30	ns
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0		20	ns

Write cycle

(Ta= −10℃to+70℃, Vcc= 5V±10%)

Parameter	Symbol	Min.	Typ.	Max.	Unit
Write cycle time	t_{WC}	100			ns
$\overline{CE_1}$ Low to end of write	t_{CW1}	80			ns
CE_2 High to end of write	t_{CW2}	80			ns
Address valid to end of write	t_{AW}	80			ns
Address setup time	t_{AS}	0			ns
Write plise width	t_{WP}	60			ns
Write recovery time	t_{WR}	0			ns
Input data setup time	t_{DW}	40			ns
Input data hold time	t_{DH}	0			ns
$\overline{WE}$ High to output active	t_{OW}	10			ns
$\overline{WE}$ Low to output in High impedance	t_{WZ}	0		30	ns
$\overline{OE}$ High to output in High impedance	t_{OHZ}	0		20	ns

9. Data Retention Characteristics

(Ta=−10°C to+70°C)

Paramenter	Symbol	Conditions		Min.	Typ.	Max.	Unit
Data Retention supply voltage	V_{CCDR}	$CE_2 \leq 0.2V$ or $\overline{CE_1} \geq V_{CCDR}-0.2V$ (*5)		2.0		5.5	V
Data Retention supply current	I_{CCDR}	$V_{CCDR}=3V$ $CE_2 \leq 0.2$ or $\overline{CE_1} \geq V_{CCDR}-0.2V$ (*5)	$Ta=25°C$			0.2	μA
			$Ta=40°C$			0.4	μA
						0.6	μA
Chip enable setup time	t_{CDR}			0			ns
Chip enable hold time	t_R			(*6) t_{RC}			ns

Note) *5. $CE_2 \geq V_{CCDR}-0.2V$ or $CE_2 \leq 0.2V$
*6. Read Cycle

10. Pin Capacitance

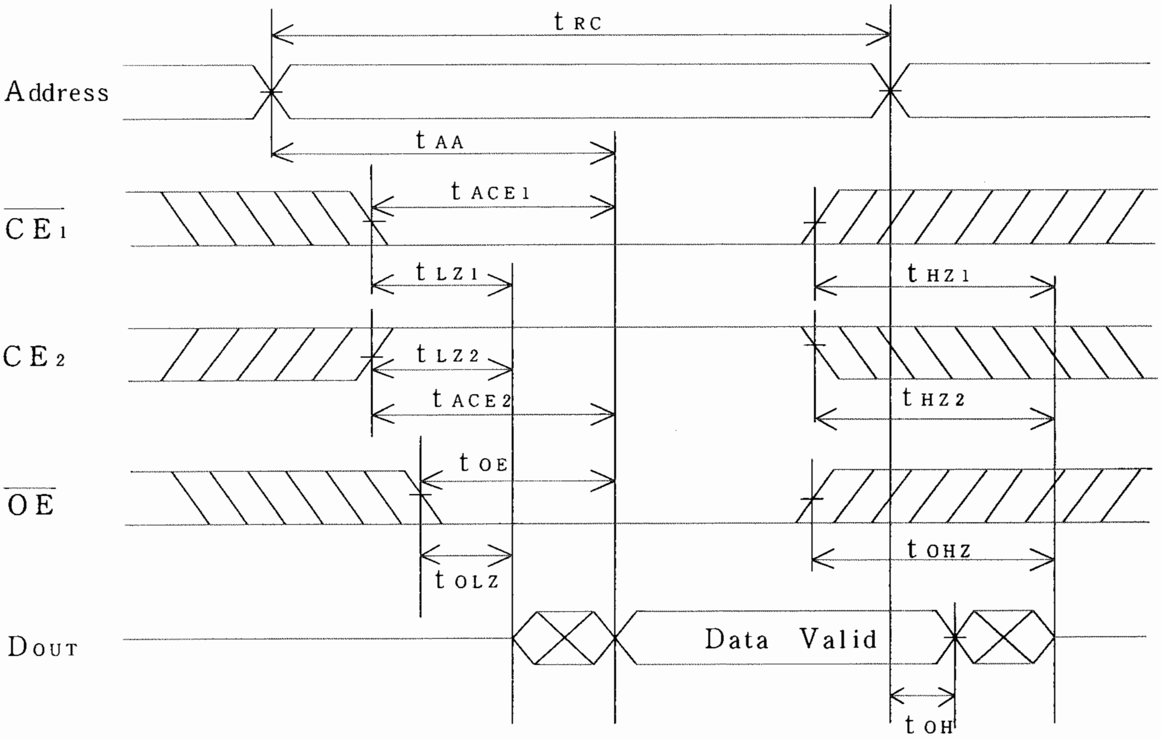
(Ta=25°C, f=1MHz)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit	
Input capacitance	C_{IN}	$V_{IN}=0V$			7	pF	*7
I/O capacitance	$C_{I/O}$	$V_{I/O}=0V$			10	pF	*7

Note) *7. This parameter is sampled and not production tested.

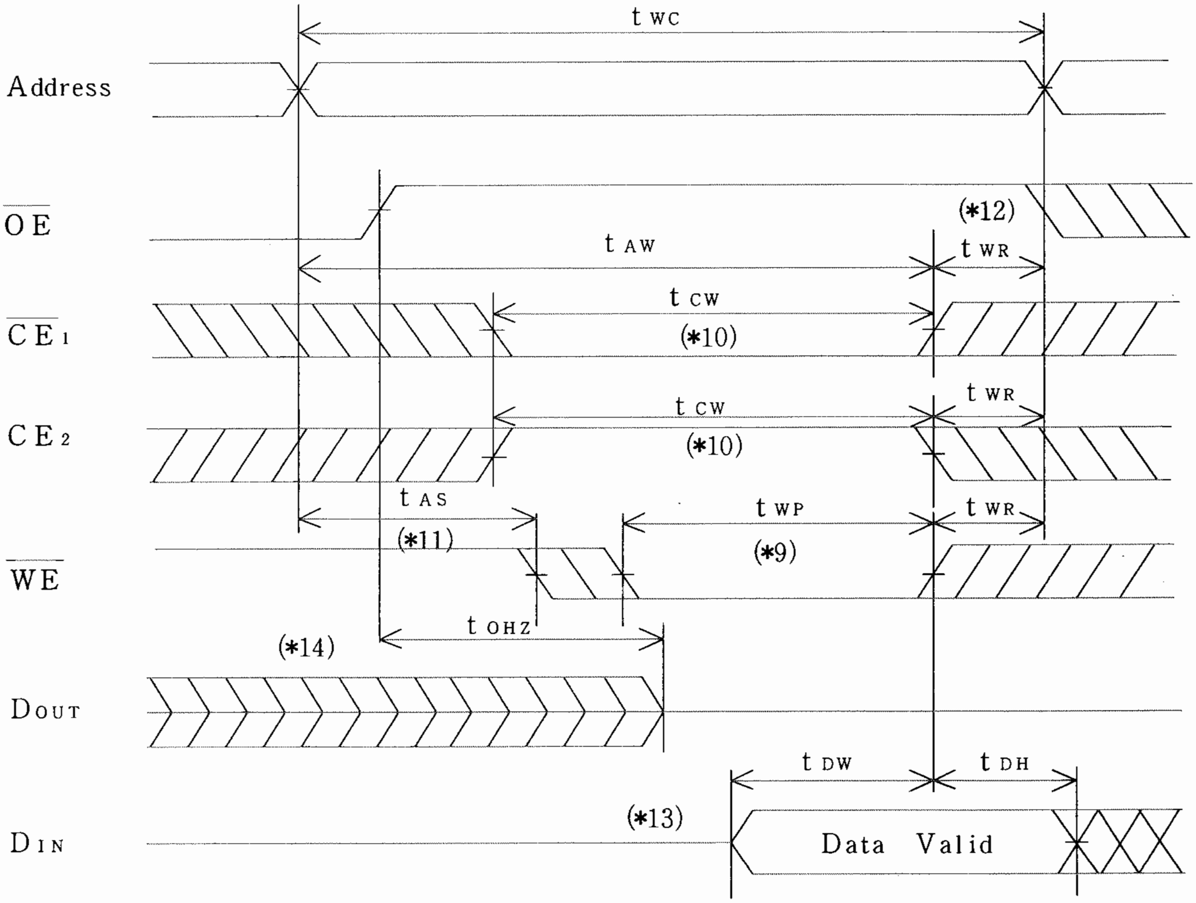
11. Timing Chart

Read cycle timing chart— (*8)

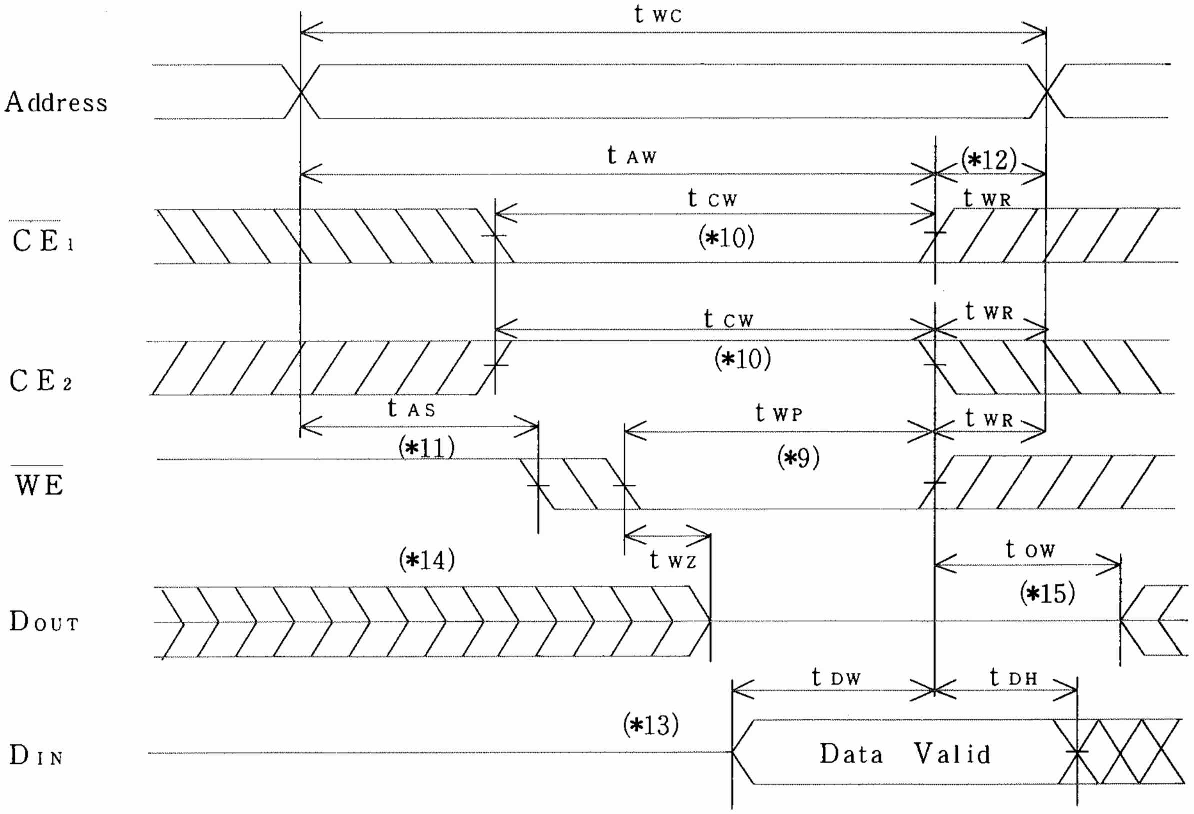

t RC
Address
t AA
CE1
t ACE1
t LZ1
t HZ1
CE2
t LZ2
t ACE2
t HZ2
t OE
OE
t OLZ
t OHZ
DOUT
Data Valid
t OH

Note) *8. WE is high for Read cycle.

Write cycle timing chart— (OE Controlled)


t WC
Address
OE
(*12)
t AW
t WR
t CW
CE1
(*10)
t WR
t CW
CE2
(*10)
t AS
t WP
t WR
(*11)
(*9)
WE
t OHZ
(*14)
DOUT
t DW
t DH
(*13)
DIN
Data Valid

Write cycle timing chart— ($\overline{OE}$ Low fixed)



Note) ∗ 9. A write occurs during the overlap of a low $\overline{CE_1}$, a high CE_2 and a low $\overline{WE}$,
A write begins at the latest transition among $\overline{CE_1}$ going low, CE_2 going high and $\overline{WE}$ going low.
A write ends at the earliest transition among $\overline{CE_1}$ going high, CE_2 going low and $\overline{WE}$ going high. t_{WP} is measured from the beginning of write to the end of write.

∗ 10. t_{CW} is measured from the later of $\overline{CE_1}$ going low or CE_2 going high to the end of write.

∗ 11. t_{AS} is measured from the address valid to the beginning of write.

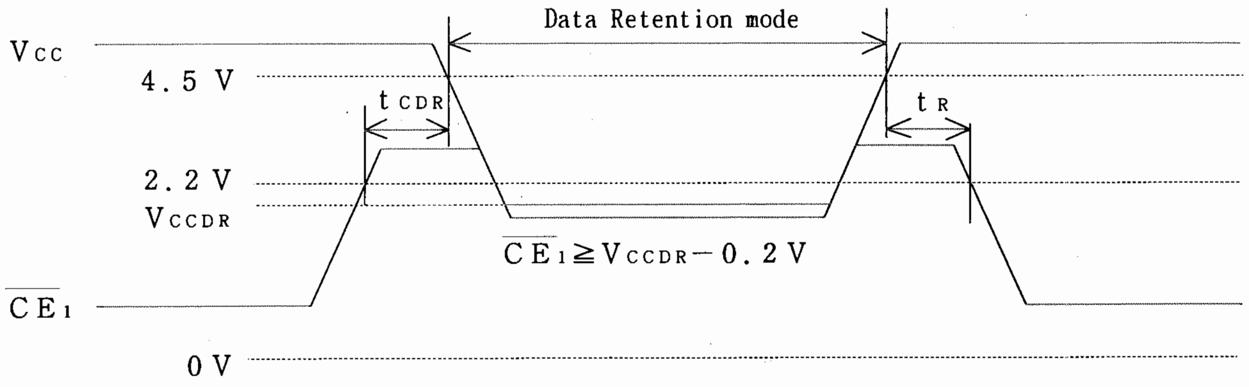
∗ 12. t_{WR} is measured from the end of write to the address change. t_{WR1} applies in case a write ends at $\overline{CE_1}$ or $\overline{WE}$ going high. t_{WR2} applies in case a write ends at CE_2 going low.

∗ 13. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.

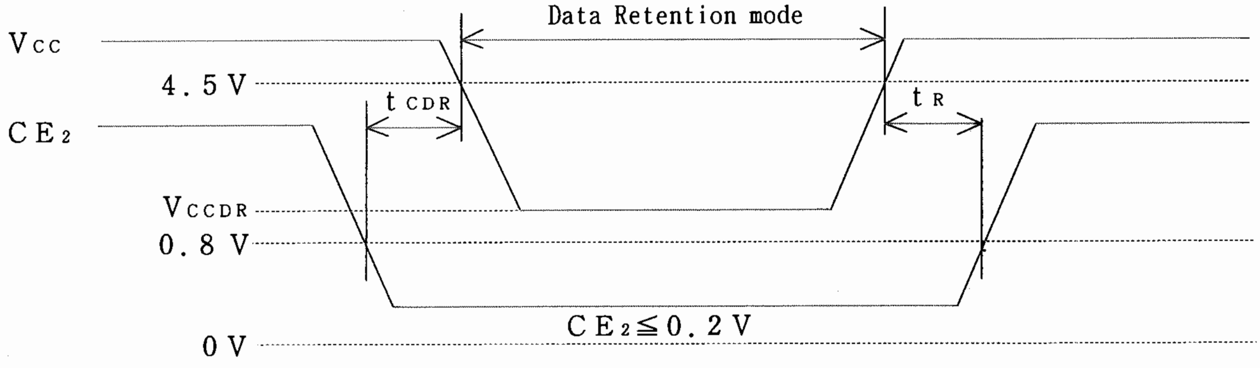
∗ 14. If $\overline{CE_1}$ goes low simultaneously with $\overline{WE}$ going low or after $\overline{WE}$ going low, the outputs remain in high impedance state.

∗ 15. If $\overline{CE_1}$ goes high simultaneously with $\overline{WE}$ going high or before $\overline{WE}$ going high, the outputs remain in high impedance state.

Data Retention timing chart— ($\overline{CE_1}$ Controlled) (*16)


Data Retention mode
Vcc
4.5 V
tCDR
tR
2.2 V
VCCDR
$\overline{CE_1} \geq V_{CCDR} - 0.2V$
$\overline{CE_1}$
0 V

Data Retention timing chart— (CE₂ Controlled)


Data Retention mode
Vcc
4.5 V
tCDR
tR
CE₂
VCCDR
0.8 V
$CE_2 \leq 0.2V$
0 V

Note) *15. To control the data retention mode at $\overline{CE_1}$, fix the input level of CE_2 between V_{CCDR} and $V_{CCDR}-0.2V$ or 0V and 0.2V during the data retention mode.

12 Package and packing specification

[Applicability]

This specification applies to IC package of the LEAD-FREE delivered as a standard specification.

1. Storage Conditions.

- Normal temperature : 5～40℃
- Normal humidity : 80%(Relative humidity) max.

*"Humidity" means "Relative humidity"

2. Baking Condition.

Baking is no necessity.

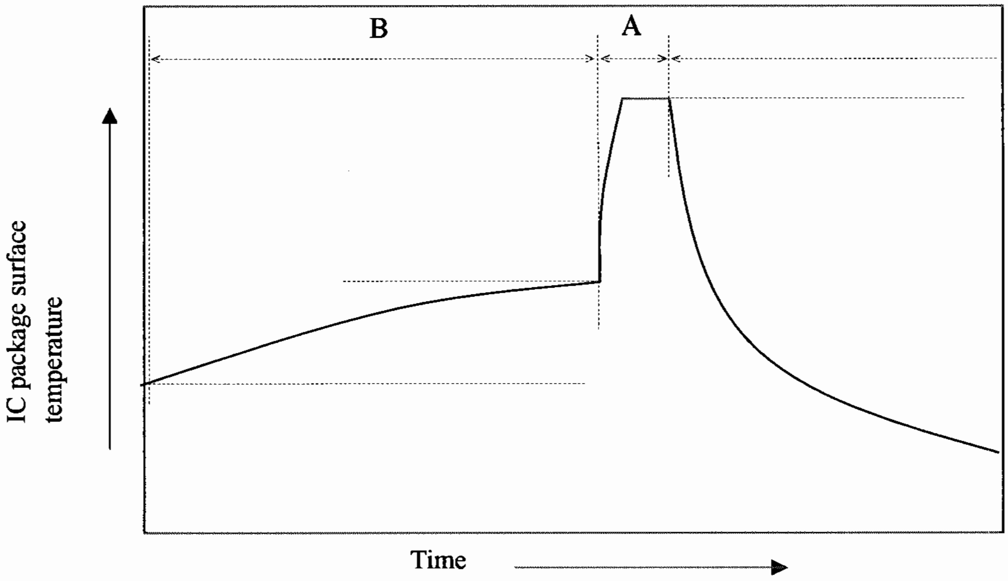
3. Mounting conditions.

Please mount the ICs as follows in order to prevent the IC quality deteriorating.

1-1.Soldering conditions. (The following conditions apply only to one-time soldering.)

(1) Solder dipping. (one-time dipping only)

- Temperature and period :
  - A) Peak temperature. 260℃ max. for 10 seconds Max.
  - B) Preheat temperature of 120 to 150℃ for 120±60 seconds
- Measuring point :
  - A) Solder bath.
  - B) IC package surface.
- Temperature profile :



(2) Manual soldering (soldering iron) (one-time soldering only)

Soldering iron should only touch the IC's outer leads.

- Temperature and period :

  350℃ max. for 3 seconds / pin max.

  (Soldering iron should only touch the IC's outer leads.)
- Measuring point : Soldering iron tip.

4. Condition for removal of residual flux.

(1) Ultrasonic washing power : 25 watts / liter max.

(2) Washing time : Total 1 minute max.

(3) Solvent temperature : 15～40℃

5. Package outline specification.
   Refer to the attached drawing.
   (Plastic body dimensions do not include burr of resin.)
   The contents of LEAD-FREE TYPE application of the specifications. (*2)

6. Markings.

6-1.Marking details. (The information on the package should be given as follows.)

(1) Product name : LH5164A-10LF

(2) Company name : SHARP

(3) Date code : (Example) YYWW XXX

YY → Denotes the production year. (Last two digits of the year.)

WW → Denotes the production week. (01・02・～・52・53)

XXX → Denotes the production ref. code (1～3 digits).

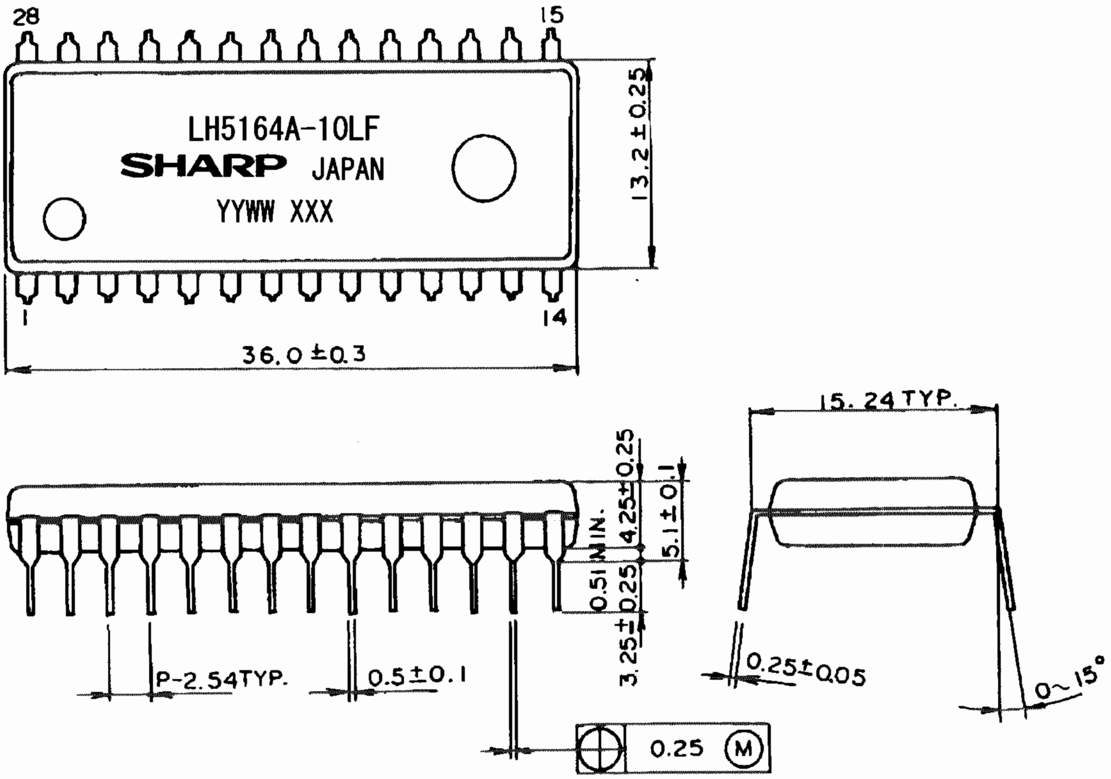
(4) "JAPAN" indicates the country of origin.

6-2.Marking layout.
The layout is shown in the attached drawing.
(However, this layout does not specify the size of the marking character and marking position.)

*2 The contents of LEAD-FREE TYPE application of the specifications.

LEAD FINISH or BALL TYPE	LEAD-FREE TYPE (Sn-Bi)
DATE CODE	They are those with an underline.
The word of " LEAD FREE" is printed on the packing label	Printed

(Note)It is those with an underline printing in a date code because of a LEAD-FREE type.


28
15
LH5164A-10LF
SHARP JAPAN
YYWW XXX
1
14
13.2±0.25
36.0±0.3
15.24TYP.
0.51MIN.
4.25±0.25
5.1±0.1
3.25±0.25
P-2.54TYP.
0.5±0.1
0.25±0.05
0~15°
0.25 M

DIP028-P-0600-AA852

LEAD TYPE	LEAD FINISH		LEAD MATERIAL
	Sn-Bi PLATING		42Alloy
NAME	DIP028-P-0600	NOTE : Plastic body dimensions do not include burr of resin.	
DRAWING NO.	AA852	UNIT	mm

7.Packing specifications.

7-1. Packing materials.

Material name	Material specifications	Purpose
Magazine	Anti-static treated plastic (15 devices/magazine)	Packing of devices.
Stopper	Plastic or rubber	Securing of devices.
Label	Paper (1piece/inner carton)	Indication of product name, quantity and packed date.
Inner carton	Cardboard (600 devices/carton max.)	Packing the magazines.
Outer carton	Cardboard (2400 devices/carton max.)	Outer packing.

(Devices must be inserted into the magazine in the same direction.)

7-2.Outline dimension of magazine.

Refer to the attached drawing.

7-3. Outline dimension of carton.

Refer to the attached drawing.

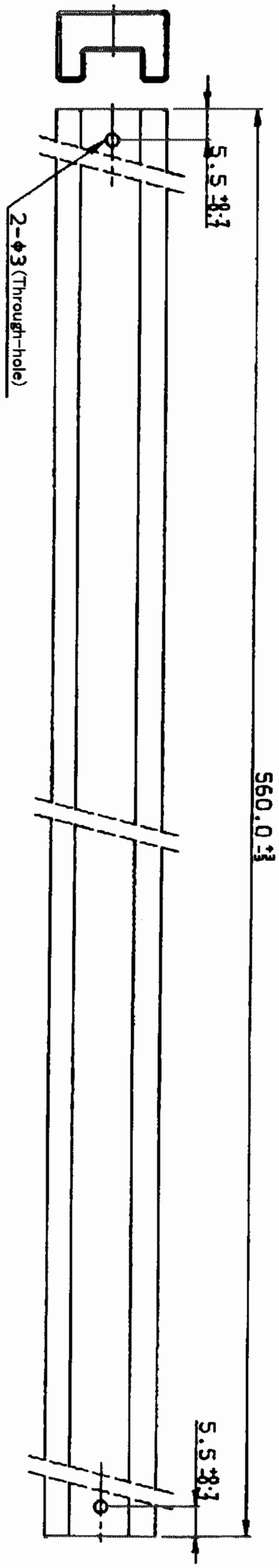
8.Precautions for use.

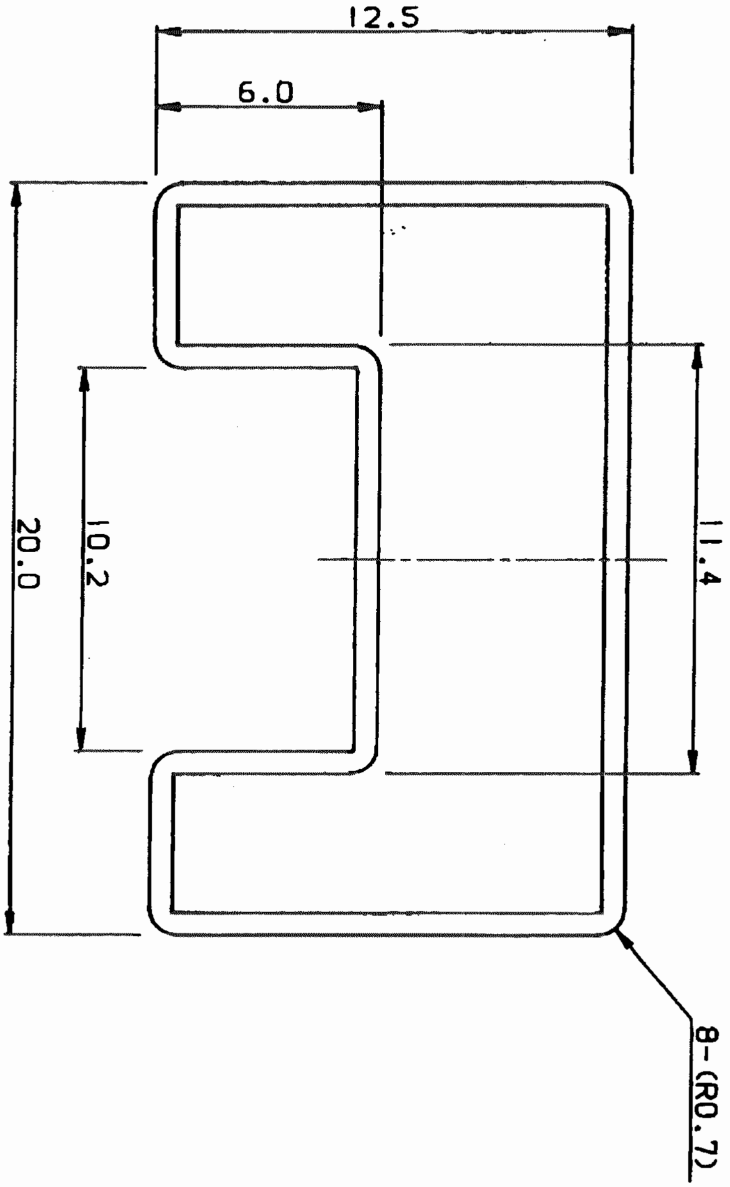
(1) Opening must be done on an anti-ESD treated workbench.
All workers must also have undergone anti-ESD treatment.

(2) The magazines have undergone anti-ESD treatment.

(3) Be sure to fit stoppers to both ends of the magazine when storing to prevent the devices from slipping out.

(4) The devices should be stored at a temperature of 5～35℃(normal temperature) and maximum relative humidity of 75%, and should be mounted within one year of the date of delivery.

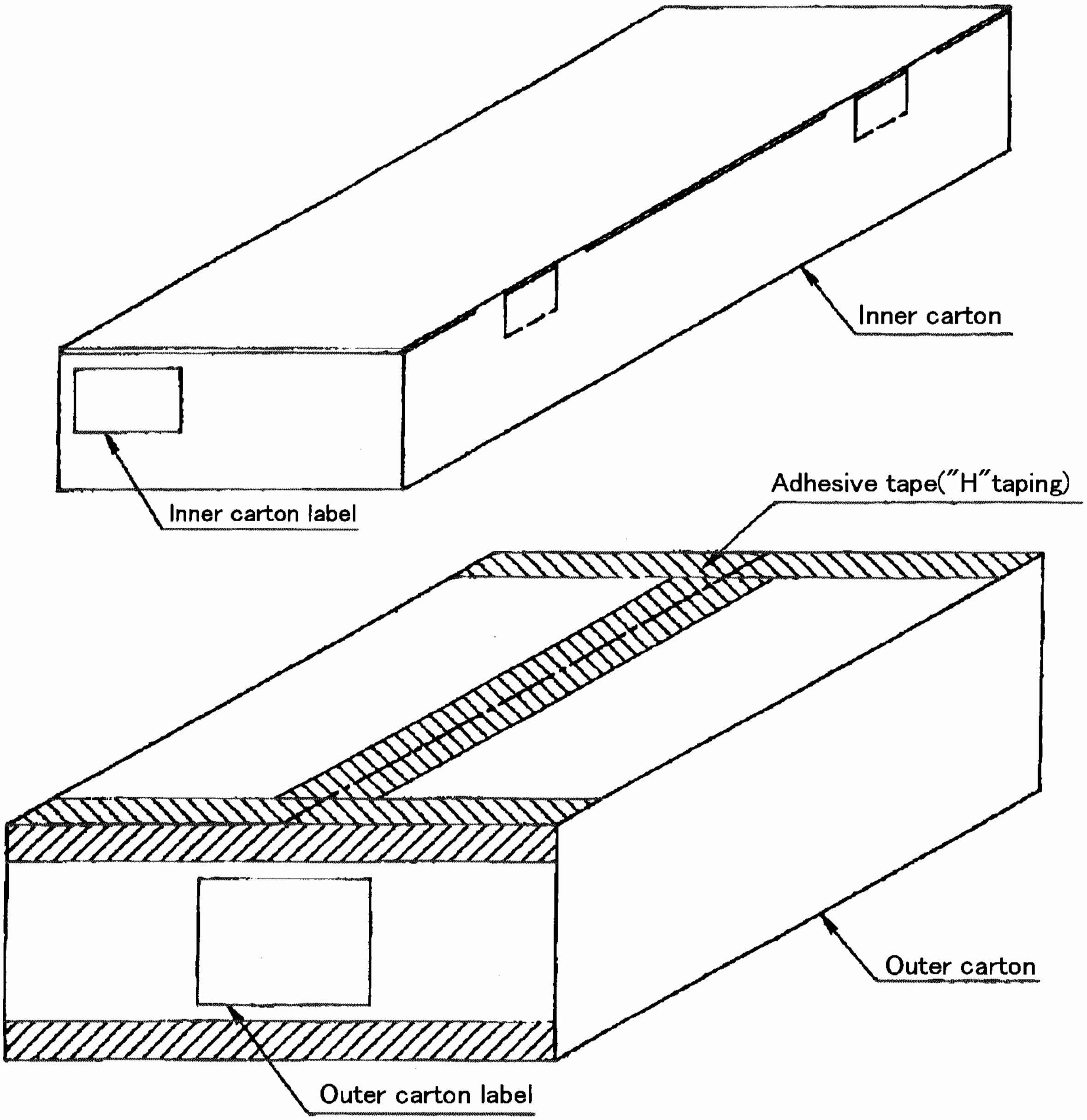

5.5 ±0.3
2-φ3 (Through-hole)
560.0 ±3
5.5 ±0.3


12.5
6.0
20.0
10.2
11.4
8-(R0.7)

注記 ：片側ピンストッパー、片側ゴムストッパーとする。
指示無き寸法公差は全て±0.4mmとする。

NOTES : One end of the magazine(sleeve) is plugged by a rubber stopper, and the other end is plugged by plastic pin-stopper.
All tolerances are ±0.4mm unless otherwise specified.

名称 Name	DP600SPK-A2			備考 Note
Drawing no.	CV651	単位 Unit	mm	

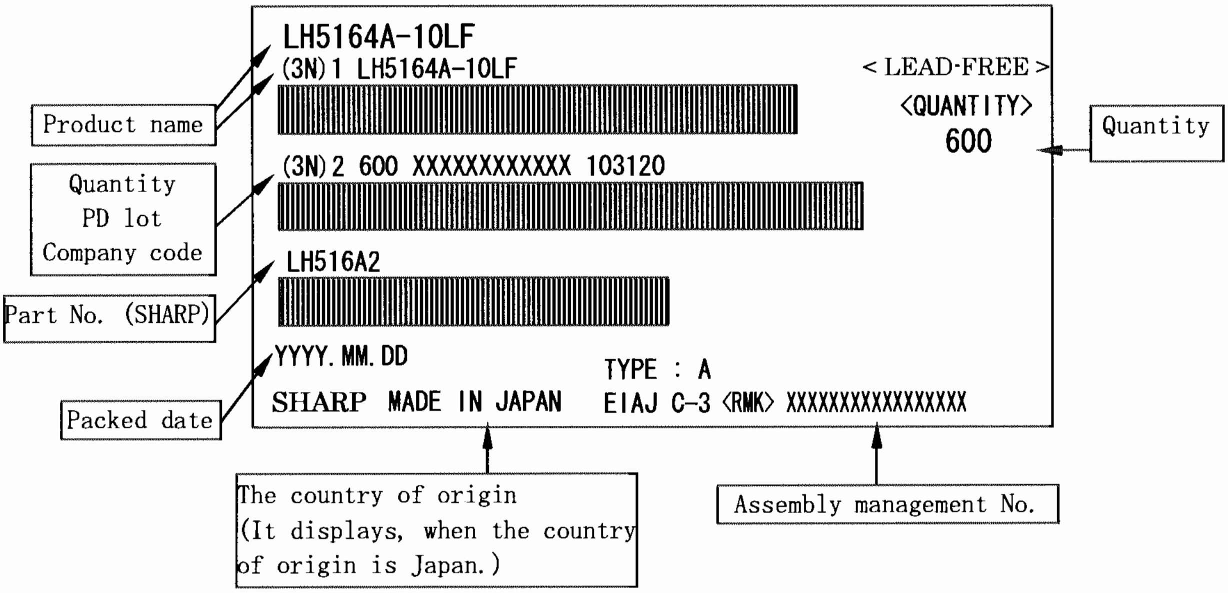

Inner carton
Inner carton label
Adhesive tape("H"taping)
Outer carton
Outer carton label

L × W× H
Inner carton - Outer dimensions : 580×170×70
Outer carton - Outer dimensions : 600×360×185

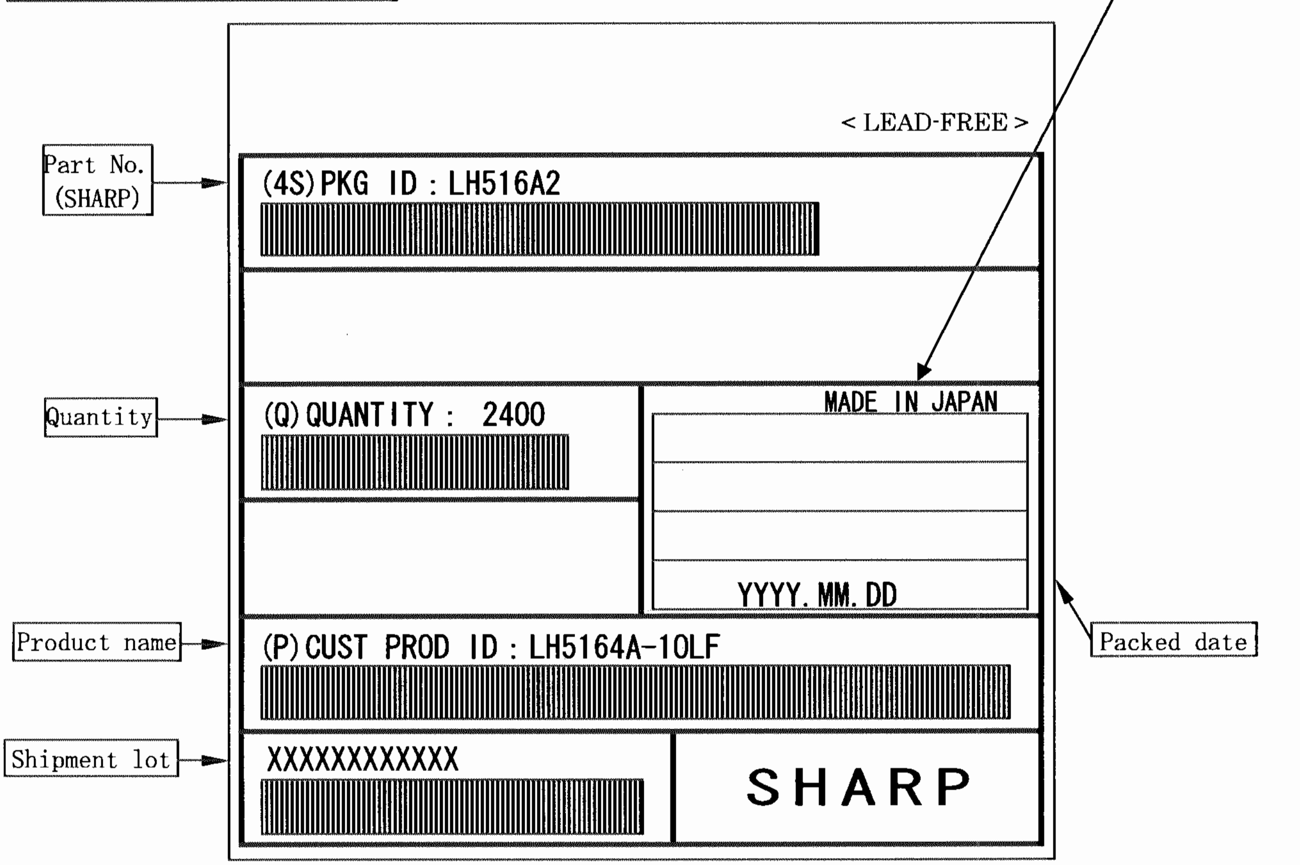
名称 NAME	DIP 600 Packing specifications			備考 出荷数量が端数の場合、本仕様と異なることがあります。 NOTE There is a possibility different from this specification when the number of shipments is fractions.
DRAWING NO.	BJ383	単位 UNIT	mm	

(Note) The <LEAD-FREE> display shows a lead-free article.

Inner carton label


LH5164A-10LF
(3N)1 LH5164A-10LF
< LEAD-FREE >
<QUANTITY>
600
(3N)2 600 XXXXXXXXXXXX 103120
LH516A2
YYYY. MM. DD
TYPE : A
SHARP MADE IN JAPAN
EIAJ C-3 <RMK> XXXXXXXXXXXXXXXXX
Product name
Quantity
PD lot
Company code
Part No. (SHARP)
Packed date
Quantity
The country of origin
(It displays, when the country of origin is Japan.)
Assembly management No.

Outer carton label


The country of origin
(It displays, when the country of origin is Japan.)
< LEAD-FREE >
Part No. (SHARP)
(4S)PKG ID : LH516A2
Quantity
(Q)QUANTITY : 2400
MADE IN JAPAN
YYYY. MM. DD
Packed date
Product name
(P)CUST PROD ID : LH5164A-10LF
Shipment lot
XXXXXXXXXXXX
SHARP

(Former) EIAJ B Standard conforming