



NEC Electronics Inc.

μPD791
4096-BIT CCD
IMAGE SENSOR

PRELIMINARY INFORMATION

Description

The μPD791 is a CCD (charge-coupled device) linear image sensor that changes optical images to electrical signals. It has 4096 photo-elements, two lines of 2061-bit CCD charge transfer registers, two output amplifiers, and two compensation signal amplifiers.

The photo-elements have excellent response characteristics because of their PN junction construction. They are 7 by 5 μm separated by 2-μm channel stoppers.

The CCD charge transfer registers have very high transfer efficiency, above 99.996 percent.

Features

- Excellent photo-electrical characteristics
- Single 12-volt power supply
- Compensation amplifier signal can reduce output signal noise
- High resolution of 16 dots per mm across 25.6-cm page
- Transfer efficiency above 99.996 percent
- 24-pin ceramic DIP

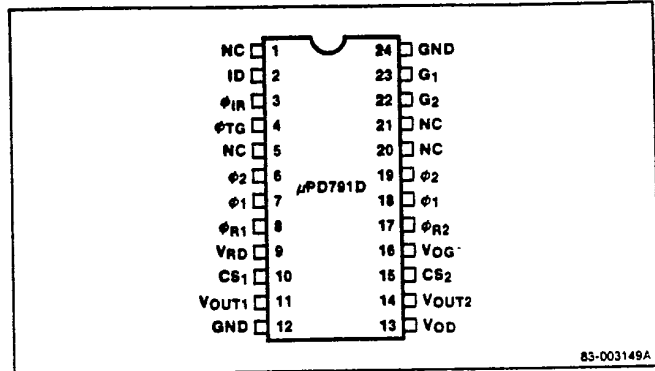
Applications

Facsimile
OCR (optical character reader)
Instrumentation

Ordering Information

Part Number	Package	Operating Ambient Temperature
μPD791D	24-pin ceramic DIP	-25 to +55 °C

Pin Configuration



Pin Identification

Pin	Name	*Function
1	NC	No connection
2	ID	Test input
3	φIR	Test input
4	φTG	Transfer gate clock input
5	NC	No connection
6, 7	φ2, φ1	Register clock input
8	φR1	Reset gate clock 1 input
9	VRD	Reset part power supply input
10	CS1	Compensation signal 1 output
11	VOUT1	Output 1 (bit 1, 3, 5,...)
12	GND	Ground
13	VOD	Output amplifier power supply input
14	VOUT2	Output 2 (bit 2, 4, 6...)
15	CS2	Compensation signal 2 output
16	VOG	Output gate bias input
17	φR2	Reset gate clock 2 input
18, 19	φ1, φ2	Register clock input
20, 21	NC	No connection
22	G2	Test input
23	G1	Test input
24	GND	Ground

*All NC pins should be connected to ground.

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Block Diagram

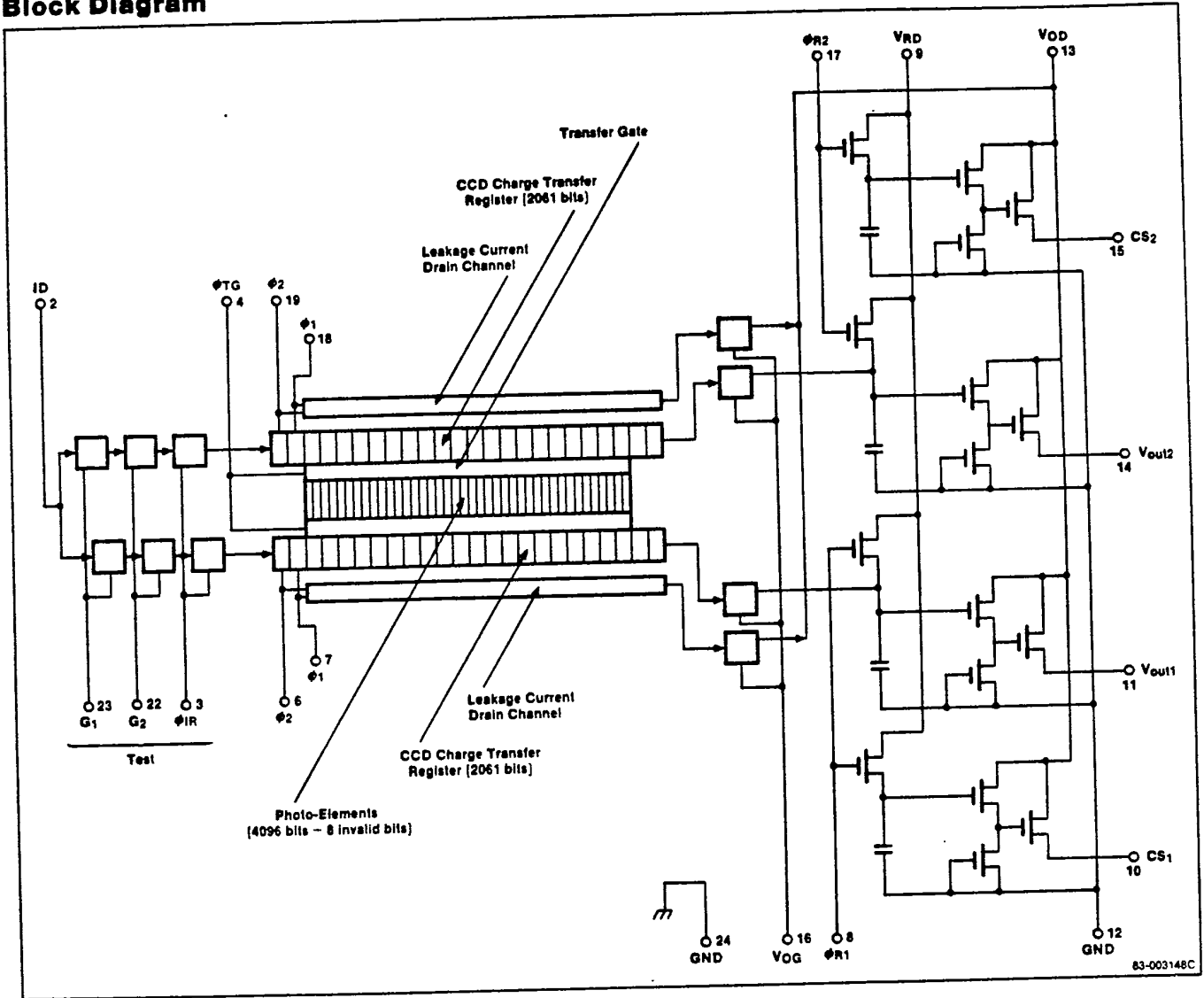
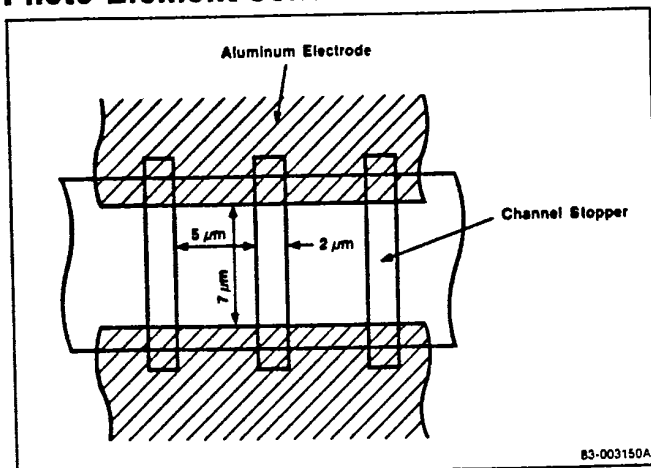


Photo-Element Construction





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Electrical Characteristics

$T_A = +25^\circ\text{C}$; source of light, 2856 K tungsten lamp; exposure period = 5.0 ms; $f_{\phi 1}$, $f_{\phi 2}$, and $f_{\phi R} = 1\text{ MHz}$; external load resistance = 2 kΩ; V_{OD} and $V_{RD} = 12.0\text{ V}$; $V_{OG} = 3.2\text{ V}$; V_{G1} and $V_{G2} = 0\text{ V}$.

Parameter	Symbol	Limits			Unit	Test Conditions
		Min	Typ	Max		
Saturation Output Voltage	V_{SAT}	300	400		mV	
Saturation Exposure	SE		0.22		ixes	
Photo-Response Nonuniformity	PRNU		±5	±10	%	$V_{OUT} = 200\text{ mV}$; Infrared cut filter, Corning 1-75
Average Dark Signal	ADS		2	10	mV	No exposure
Dark Signal Nonuniformity	DSNU		10	20	mV	No exposure
Working Power Consumption	P_D	70	150	230	mW	Current of pins 9 and 13 x supply voltage
Spectral Response Range Limits	SR	0.3		1.1	μm	
Sensitivity	S	1300	1900	3000	mV/ixes	
Offset Voltage	V_{IO}	4	6	8	V	0% level of V_{OUT} in timing waveforms
Output Delay Time	t_D		50	120	ns	See timing waveforms.
Difference between V_{OUT1} and V_{OUT2}	dV_{OUT}			±10	%	$V_{OUT1} = 200\text{ mV}$

Reference Characteristics

Parameter	Limits			Unit
	Min	Typ	Max	
Input Capacitance at ϕ_1 or ϕ_2 (pins 6, 7, 18, 19)	400	800	1200	pF
Input Capacitance at ϕ_R (pins 8, 17)	5	10	15	pF
Input Capacitance at ϕ_{TG} (pin 4)	50	100	150	pF
Output Impedance at V_{OUT} or CS (pins 10, 11, 14, 15) with 2-kΩ external load resistor		1.0	2.0	kΩ

Absolute Maximum Ratings

$T_A = +25^\circ\text{C}$

Output Amplifier Supply Voltage, V_{OD}	-0.3 to +18 V
Reset Part Supply Voltage, V_{RD}	-0.3 to +18 V
Output Gate Voltage, V_{OG}	-0.3 to +18 V
Register Clock Signal Voltage, $V_{\phi 1\phi 2}$	-0.3 to +18 V
Transfer Gate Clock Signal Voltage, $V_{\phi TG}$	-0.3 to +18 V
Reset Gate Clock Signal Voltage, $V_{\phi R}$	-0.3 to +18 V
Operating Temperature, T_{OPT}	-25 to +55°C
Storage Temperature, T_{STG}	-40 to +100°C

Comment: Stress above those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

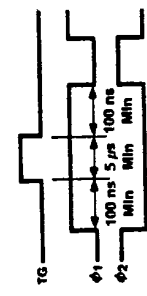
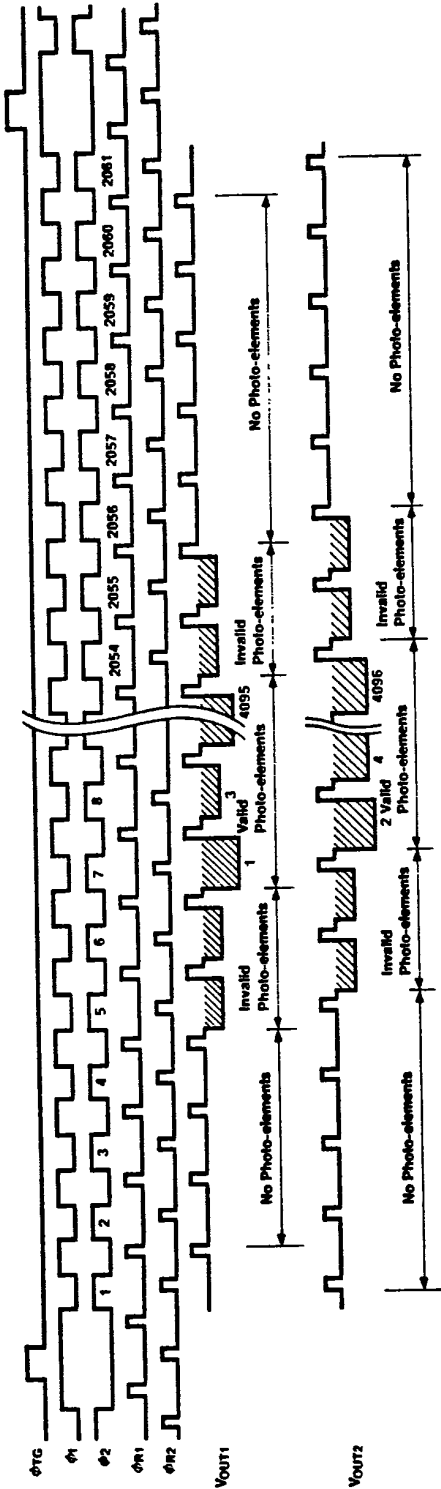
$T_A = -25$ to $+55^\circ\text{C}$

Parameter	Symbol	Limits			Unit
		Min	Typ	Max	
Output Amplifier Supply Voltage	V_{OD}	11.4	12.0	12.6	V
Reset Part Supply Voltage	V_{RD}	11.4	12.0	12.6	V
Output Gate Bias Voltage	V_{OG}	2.7	3.2	3.7	V
Test Terminal G_1 Voltage	V_{G1}		0		V
Test Terminal G_2 Voltage	V_{G2}		0		V
Test Terminal ID Voltage	V_{ID}	10	12.0	15	V
Test Terminal ϕ_R Voltage	$V_{\phi R}$		0		V
High Level of Register Clock Signal	$V_{\phi 1\phi 2H}$	9.0	12.0	12.5	V
Low Level of Register Clock Signal	$V_{\phi 1\phi 2L}$	-0.3	0	0.5	V
High Level of Transfer Gate Clock Signal	$V_{\phi TGH}$	9.0	12.0	12.5	V
Low Level of Transfer Gate Clock Signal	$V_{\phi TGL}$	-0.3	0	0.5	V
High Level of Reset Gate Clock Signal	$V_{\phi RH}$	9.0	12.0	12.5	V
Low Level of Reset Gate Clock Signal	$V_{\phi RL}$	-0.3	0	0.5	V
Register Clock Signal Frequency (see Note)	$f_{\phi 1\phi 2}$		1	3.5	MHz
Reset Gate Clock Signal Frequency (see Note)	$f_{\phi R}$		1	3.5	MHz

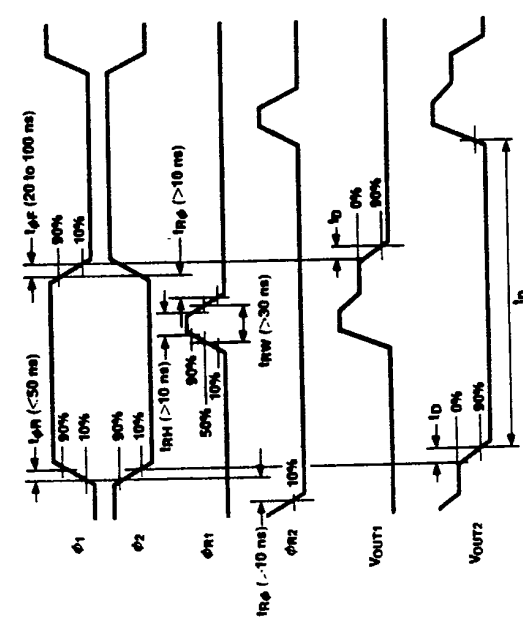
Note: At lower frequencies, t_p of output signal is $>100\text{ ns}$. (See Timing Waveforms.)

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Timing Waveforms



- ϕ_1 and ϕ_2 are symmetrical.
- The crossing voltage of ϕ_1 and ϕ_2 should be kept above VOG + 1 V.
- The register clock pulse should be not more than 2061 cycles.
- Width of the transfer gate pulse should be less than 20 μ s.



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Definitions of Electrical Parameters

Saturation Output Voltage [V_{SAT}]. An output signal level above which the PRNU (photo-response non-uniformity) is ≥10% or the response is nonlinear.

Saturation Exposure [SE]. Product of illuminance (lx) and exposure period (s) in which the output is saturated.

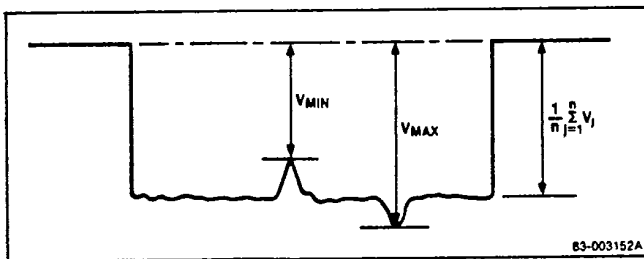
Photo-Response Nonuniformity [PRNU]. Percentage of peak output level and bottom output level against average output level of all valid photo-elements in static and uniform light.

$$PRNU (\%) = \left(\frac{V_{MAX} \text{ OR } V_{MIN}}{\frac{1}{n} \sum_{j=1}^n V_j} - 1 \right) \times 100$$

where

n = number of valid photo-elements

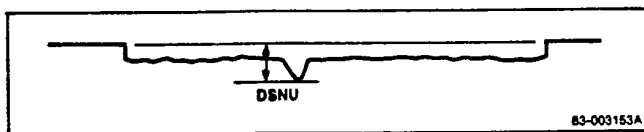
V_j = output voltage of each photo element



Average Dark Signal [ADS]. Average output level of valid photo-elements with no exposure.

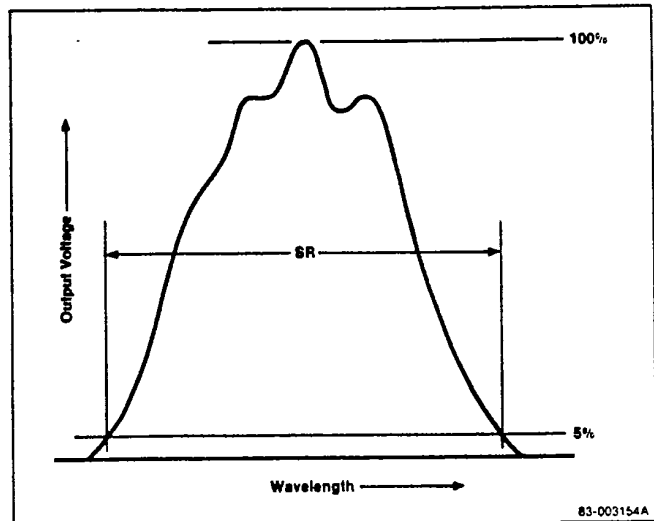
$$ADS (mV) = \frac{1}{n} \sum_{j=1}^n V_j$$

Dark Signal Nonuniformity [DSNU]. Peak output level with no exposure.



Working Power Consumption [P_W]. Product of supply voltage and current when supply voltage is 12.0 V.

Spectral Response Range Limits [SR]. Short side and long side limits of response spectral range having sensitivity above 5 percent of sensitivity of most sensitive wavelength.



Sensitivity [S]. Quotient of the output level divided by exposure (lx·s).

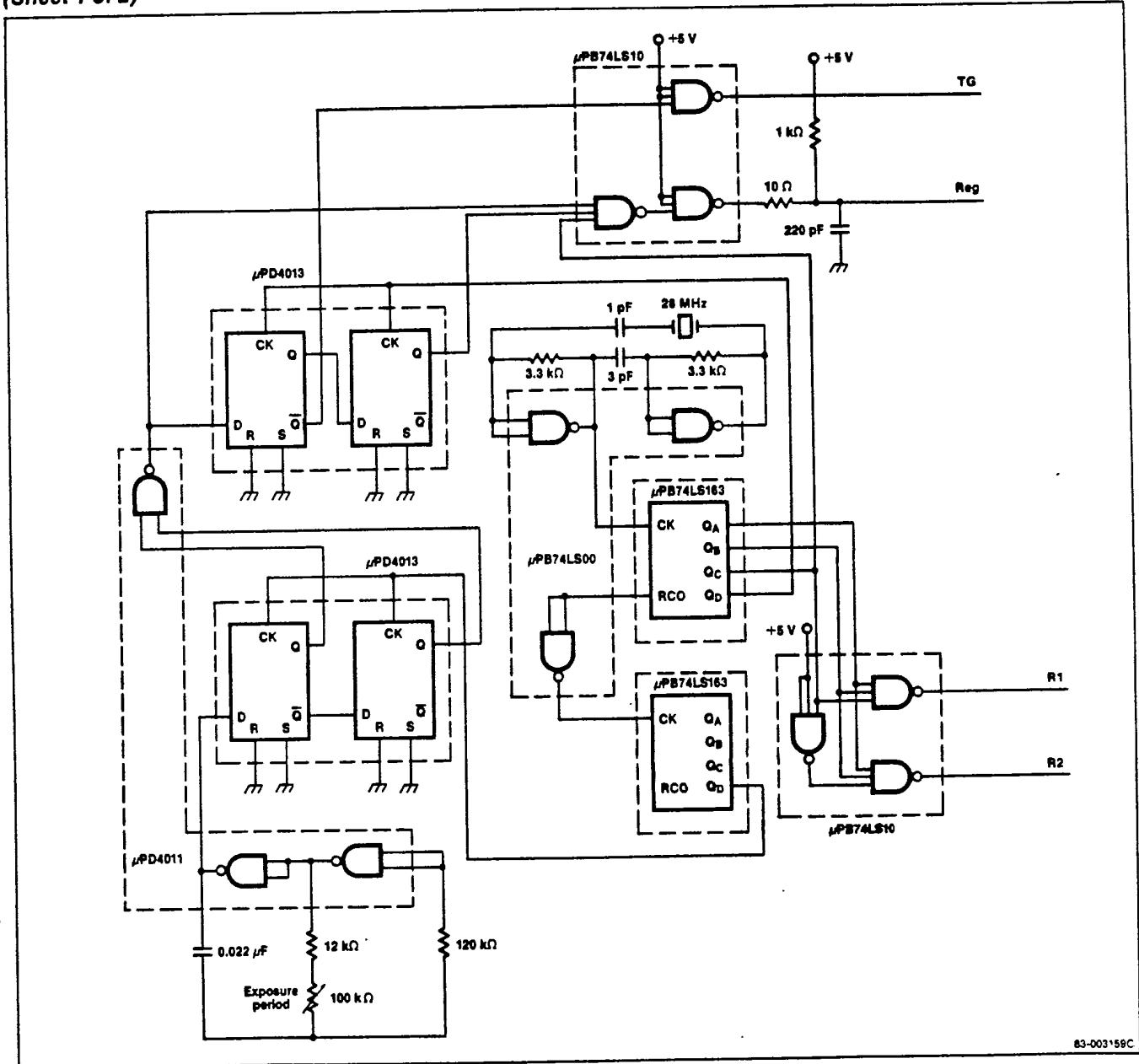
Offset Voltage [V_{OS}]. Output terminal potential with no exposure.



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Example of Driving Circuit

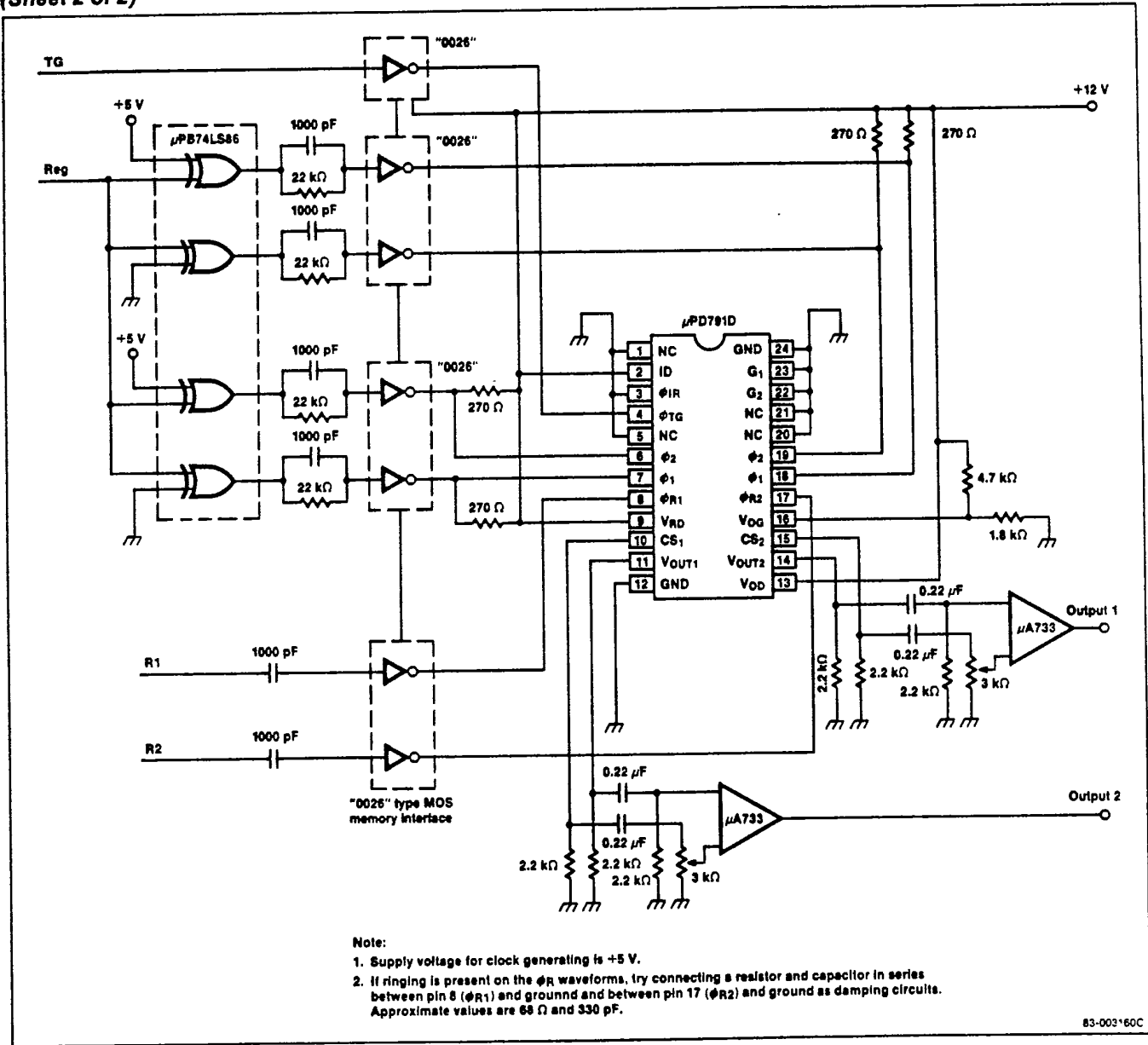
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Example of Driving Circuit (Cont.)

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Operating Characteristics
 $T_A = 25^\circ\text{C}$

