I^{2}C BUS Control 5-Input 2-Output AV Switch
Monolithic IC MM1313

Outline

This IC is a 5-input 2-output AV switch with I^{2}C control, developed for use in televisions. Two outputs enable it to support two screens or "picture-in-picture".

Features

1. Serial control by I^{2}C bus.
2. 5-inputs, 2-outputs.
3. Video and audio system switches can be controlled independently.
4. 6dB amplifier built in to video system.
5. Built-in Y/C MIX circuit.
6. Slave address can be changed : 90H or 92H.
7. Audio muting possible by external pin.
8. Maintains high impedance even when I^{2}C BUS line (SDA, SCL) power supply is off.
9. Built-in 3 value discrimination function.
10. On-chip power ON reset function.
11. Two types of audio input impedance : 60kΩ and 30kΩ.
      MM1313AD : 60kΩ   MM1313BD : 30kΩ
12. Supports 2-screen or P-IN-P TV.

Package

SDIP-42A (MM1313AD, MM1313BD)

Applications

1. Televisions
2. Other video equipment

Equivalent Block Diagram
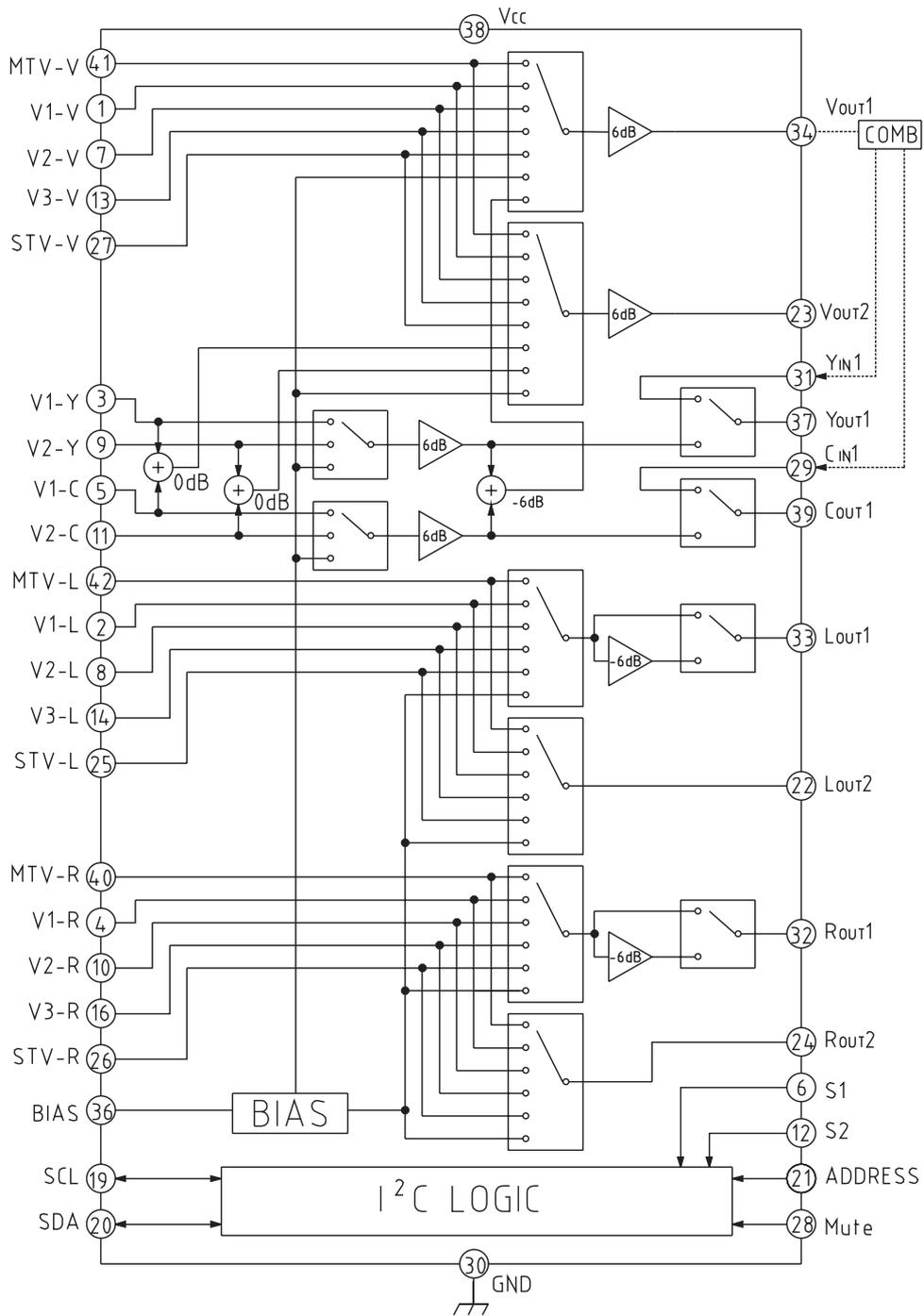
Pin Function

Pin No.	Name	Internal equivalent circuit diagram	Pin No.	Name	Internal equivalent circuit diagram
41	MTV–V		33	$L_{OUT}1$	
1	V1–V		22	$L_{OUT}2$	
7	V2–V		32	$R_{OUT}1$	
13	V3–V		24	$R_{OUT}2$	
27	STV–V				
3	V1–Y				
9	V2–Y				
31	$Y_{IN}1$				
5	V1–C		36	BIAS	
11	V2–C				
29	$C_{IN}1$				
42	MTV–L		19	SCL	
2	V1–L				
8	V2–L				
14	V3–L				
25	STV–L				
40	MTV–R				
4	V1–R				
10	V2–R				
16	V3–R				
26	STV–R				
34	$V_{OUT}1$		20	SDA	
23	$V_{OUT}2$				
37	$Y_{OUT}1$		6	S1	
39	$C_{OUT}1$		12	S2	
			21	ADR	
			28	Mute	

Absolute Maximum Ratings (Ta=25°C)

| Item	Symbol	Ratings	Units
Storage temperature	T_{STG}	−40~+125	°C
Operating temperature	T_{OPR}	−20~+75	°C
Power supply voltage	V_{CC}	12	V
Allowable power dissipation	Pd	850	mW

Electrical Characteristics (Ta=25°C, Vcc=9V)

Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Operating power supply voltage	V_{CC}			8	9	10	V
Current consumption	I_{CC}	38	Vcc=9V, no signal, no load		40	52	mA
V$_{OUT}$1 output							
Voltage gain	G_{V1}	TP1	Sine wave 1.0V$_{P-P}$, 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	F_{V1}	TP1	Sine wave 1.0V$_{P-P}$, 10MHz/100kHz	−1.0	0	1.0	dB
Differential gain	DG_{V1}	TP1	Vn-V : Staircase 1V$_{P-P}$ APL=10~90% / Vn-Y : Staircase (luminance signal) 1V$_{P-P}$ Vn-C : Chroma signal 0.3V$_{P-P}$ APL=10~90%	−3	0	3	%
Differential phase	DP_{V1}	TP1	Vn-V : Staircase 1V$_{P-P}$ APL=10~90% / Vn-Y : Staircase (luminance signal) 1V$_{P-P}$ Vn-C : Chroma signal 0.3V$_{P-P}$ APL=10~90%	−3	0	3	deg
Input dynamic range	D_{V1}	SG1~3	Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V$_{P-P}$
V$_{OUT}$2 output							
Voltage gain	G_{V2}	TP6	Sine wave 1.0V$_{P-P}$, 100kHz	5.5	6.0	6.5	dB
Frequency characteristics	F_{V2}	TP6	Sine wave 1.0V$_{P-P}$ 10MHz/100kHz	−1.0	0	1.0	dB
Differential gain	DG_{V2}	TP6	Vn-V : Staircase 1V$_{P-P}$ APL=10~90% / Vn-Y : Staircase (luminance signal) 1V$_{P-P}$ Vn-C : Chroma signal 0.3V$_{P-P}$ APL=10~90%	−3	0	3	%
Differential phase	DP_{V2}	TP6	Vn-V : Staircase 1V$_{P-P}$ APL=10~90% / Vn-Y : Staircase (luminance signal) 1V$_{P-P}$ Vn-C : Chroma signal 0.3V$_{P-P}$ APL=10~90%	−3	0	3	deg
Input dynamic range	D_{V2}	SG1~3	Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V$_{P-P}$
Y$_{OUT}$1 output							
Voltage gain	G_{Y1}	TP2	Vn-Y : Sine wave 1.0V$_{P-P}$, 100kHz	5.5	6.0	6.5	dB
	G_{Y2}	TP2	Y$_{IN}$1 : Sine wave 2.0V$_{P-P}$, 100kHz	−0.5	0	0.5	
Frequency characteristics	F_{Y1}	TP2	Vn−Y : Sine wave 1.0V$_{P-P}$ 10MHz/100kHz	−1.0	0	1.0	dB
	F_{Y2}	TP2	Y$_{IN}$1 : Staircase 2.0V$_{P-P}$ 10MHz/100kHz	−1.0	0	1.0	
Differential gain	DG_Y	TP2	Vn-Y : Staircase 1V$_{P-P}$ APL=10~90% / Y$_{IN}$1: Staircase 2V$_{P-P}$ APL=10~90%	−3	0	3	%
Differential phase	DP_Y	TP2	Vn-Y : Staircase 1V$_{P-P}$ APL=10~90% / Y$_{IN}$1 : Staircase 2V$_{P-P}$ APL=10~90%	−3	0	3	deg

Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
Input dynamic range	D_Y1	SG2	Vn-Y : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	1.6	1.9		V_{P-P}
	D_Y2	SG4	$V_{IN}1$: Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	3.2	3.8		
Output impedance	$Z_{OYC}1$				50		Ω
C_OUT1 output							
Voltage gain	G_C1	TP3	Vn-C : Sine wave 1.0V_{P-P}, 100kHz	5.5	6.0	6.5	dB
	G_C2	TP3	$C_{IN}1$: Sine wave 2.0V_{P-P}, 100kHz	–0.5	0	0.5	
Frequency characteristics	F_C1	TP3	Vn–C : Sine wave 1.0V_{P-P} 10MHz/100kHz	–1.0	0	1.0	dB
	F_C2	TP3	$C_{IN}1$: Sine wave 2.0V_{P-P} 10MHz/100kHz	–1.0	0	1.0	
Differential gain	DG_C	TP3	$C_{IN}1$: Staircase 2V_{P-P} APL=10~90%	–3	0	3	%
Differential phase	DP_C	TP3	$C_{IN}1$: Staircase 2V_{P-P} APL=10~90%	–3	0	3	deg
Input dynamic range	D_C1	SG3	Vn-C : Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	2.75	3.25		V_{P-P}
	D_C2	SG5	$C_{IN}1$: Sine wave 100kHz Maximum input for total higher harmonic distortion factor < 1.0%	5.5	6.5		
Input impedance	Z_{IC}		Vn–C, $C_{IN}1$	10	15	20	kΩ
Output impedance	$Z_{OC}1$				50		Ω
L_OUT1 output							
Voltage gain	G_L11	TP4	b7=0, Sine wave 2.5V_{P-P}, 1kHz	–6.5	–6.0	–5.5	dB
	G_L12	TP4	b7=1, Sine wave 2.5V_{P-P}, 1kHz	–0.5	0.0	0.5	
Frequency characteristics	F_L1	TP4	Sine wave 2.5V_{P-P}, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THD_L1	TP4	Sine wave 2.5V_{P-P}, 1kHz		0.03	0.1	%
Input dynamic range	D_L1	SG6	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	$V_{OFFL}1$	33	L_OUT1 pin DC difference during SW switching		0	±15	mV
Input impedance	$Z_{IL}1$			42	60	78	kΩ
Output impedance	$Z_{OL}1$				120		Ω
L_OUT2 output							
Voltage gain	G_L2	TP7	Sine wave 2.5V_{P-P}, 1kHz	–0.5	0.0	0.5	dB
Frequency characteristics	F_L2	TP7	Sine wave 2.5V_{P-P}, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THD_L2	TP7	Sine wave 2.5V_{P-P}, 1kHz		0.03	0.1	%
Input dynamic range	D_L2	SG6	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	$V_{OFFL}2$	22	L_OUT2 pin DC difference during SW switching		0	±15	mV
Output impedance	$Z_{OL}2$				120		Ω
R_OUT1 output							
Voltage gain	G_R11	TP5	b7=0, Sine wave 2.5V_{P-P}, 1kHz	–6.5	–6.0	–5.5	dB
	G_R12	TP5	b7=1, Sine wave 2.5V_{P-P}, 1kHz	–0.5	0.0	0.5	
Frequency characteristics	F_R1	TP5	Sine wave 2.5V_{P-P}, 1MHz/1kHz	–3.0	0	1.0	dB
Total higher harmonic distortion	THD_R1	TP5	Sine wave 2.5V_{P-P}, 1kHz		0.03	0.1	%
Input dynamic range	D_R1	SG7	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	$V_{OFFR}1$	32	R_OUT1 pin DC difference during SW switching		0	±15	mV
Input impedance	$Z_{IR}1$			42	60	78	kΩ
Output impedance	$Z_{OR}1$				120		Ω

Item	Symbol	Measurement pin	Conditions (unless otherwise indicated, Measurement Circuit Figure 1)	Min.	Typ.	Max.	Units
R$_{OUT}$2 output							
Voltage gain	G$_{R}$2	TP8	Sine wave 2.5V$_{P-P}$, 1kHz	−0.5	0.0	0.5	dB
Frequency characteristics	F$_{R}$2	TP8	Sine wave 2.5V$_{P-P}$, 1MHz/1kHz	−3.0	0	1.0	dB
Total higher harmonic distortion	THD$_{R}$2	TP8	Sine wave 2.5V$_{P-P}$, 1kHz		0.03	0.1	%
Input dynamic range	D$_{R}$2	SG7	Sine wave 1kHz Maximum input for total higher harmonic distortion factor < 0.5%	2.6	2.8		Vrms
Output offset voltage	V$_{OFFR}$2	24	R$_{OUT}$2 pin DC difference during switching		0	±15	mV
Output impedance	Z$_{OR}$2				120		Ω
Crosswalk							
V$_{OUT}$1	C$_{TV}$1	TP1	Measurement Circuit Figure 2 for SG1 input : 4.43MHz, 1V$_{P-P}$ for SG2 input : 4.43MHz, 0.5V$_{P-P}$		−60	−53	dB
V$_{OUT}$2	C$_{TV}$2	TP2			−60	−53	dB
Y$_{OUT}$1	C$_{TY}$1	TP3			−60	−53	dB
C$_{OUT}$1	C$_{TC}$1	TP6			−60	−53	dB
L$_{OUT}$1	C$_{TL}$1	TP4	Measurement Circuit Figure 2 1kHz, 2.5V$_{P-P}$		−90	−80	dB
L$_{OUT}$2	C$_{TL}$2	TP5			−90	−80	dB
R$_{OUT}$1	C$_{TR}$1	TP7			−90	−80	dB
R$_{OUT}$2	C$_{TR}$2	TP8			−90	−80	dB
Video I/O Pin Voltage							
Input pin voltage	V$_{VIP}$		No signal, no load	4.6	4.9	5.2	V
Output pin voltage	V$_{VOP}$		V$_{OUT}$1 pin, V$_{OUT}$2 pin No signal, no load	4.1	4.4	4.7	V
	V$_{SOP}$		Y$_{OUT}$1 pin, C$_{OUT}$1 pin No signal, no load	3.3	3.6	3.9	V
Audio I/O Pin Voltage							
Input pin voltage	V$_{AIP}$		No signal, no load	4.0	4.3	4.6	V
Output pin voltage	V$_{AOP}$		No signal, no load	3.9	4.2	4.5	V
Logic section (Refer to figure below)							
Input voltage L	V$_{IL}$		I²C logic low level discrimination value	0.0		1.5	V
Input voltage H	V$_{IH}$		I²C logic high level discrimination value	3.0		5.0	V
Low level output voltage (SDA)	V$_{OL}$		SDA for 3mA inflow	0.0		0.4	V
High level input current	I$_{IH}$		when SDA, SCL=4.5V impressed	−10		+10	μA
Low level input current	I$_{IL}$		when SDA, SCL=0.4V impressed	−10		+10	μA
Clock frequency	f$_{SCL}$					100	kHz
Data transmission waiting time	t$_{BUF}$			4.7			μS
SCL start hold time	t$_{HD;STA}$			4.0			μS
SCL low level hold time	t$_{LOW}$			4.7			μS
SCL high level hold time	t$_{HIGH}$			4.0			μS
SCL start set-up time	t$_{SU;STA}$			4.7			μS
SDA data hold time	t$_{HD;DAT}$			200			nS
SDA data set-up time	t$_{SD;DAT}$			250			nS
SCL rise time	t$_{R}$					1000	nS
SCL fall time	t$_{F}$					300	nS
SCL stop set-up time	t$_{SU;STO}$			4.0			μS

I²C BUS BUS Control Signal
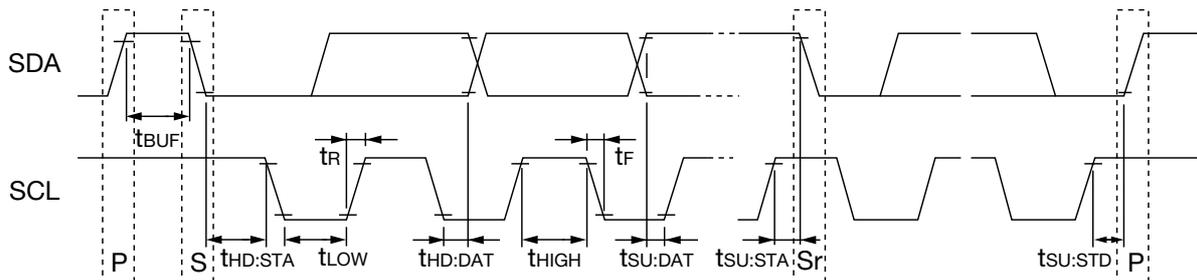
Measurement Circuit

■ Measurement Circuit 1
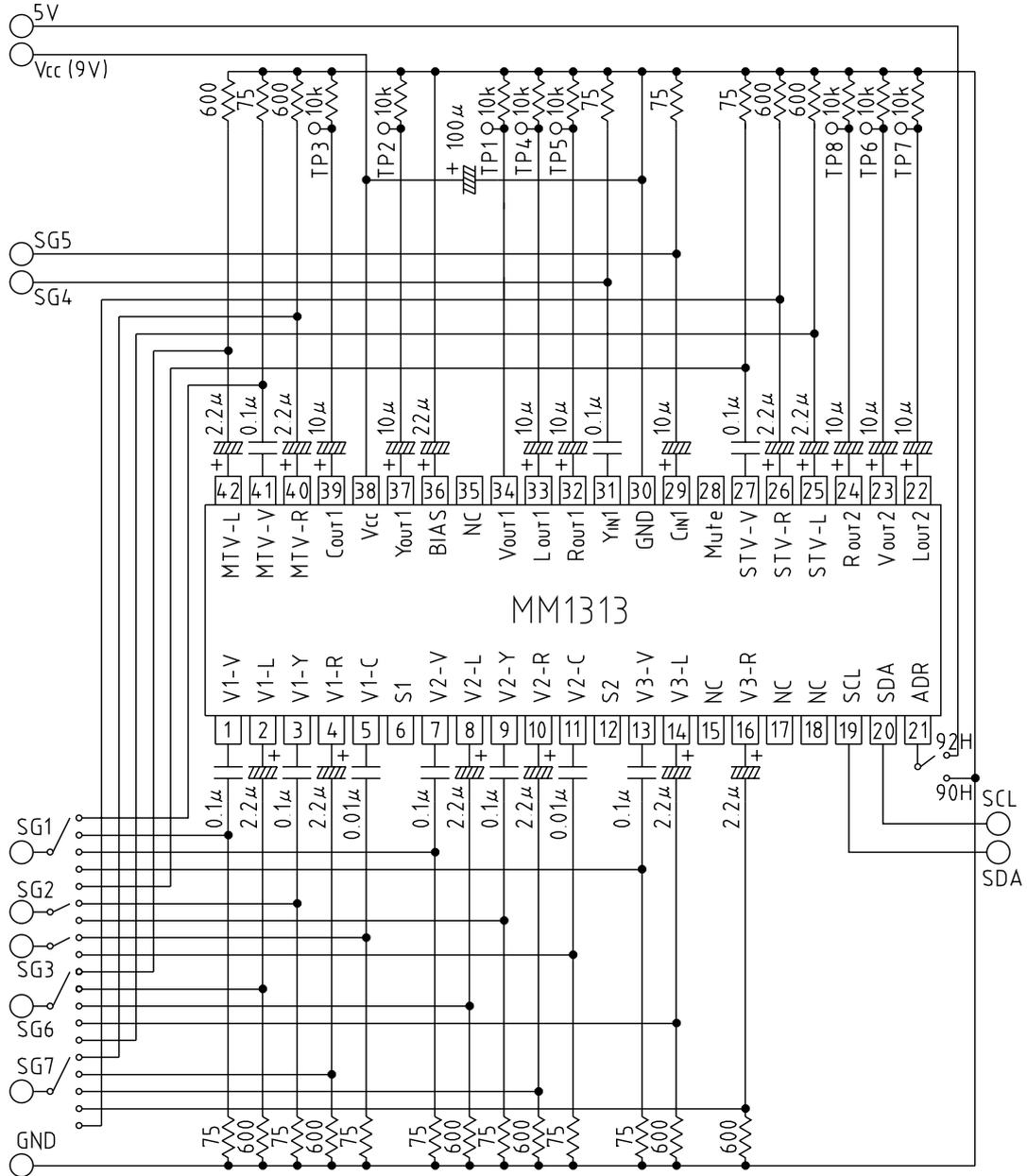
■ Measurement Circuit 2 (Crosstalk measurement)

I²C BUS

S:Start Condition
P:Stop Condition
A:Acknowledge
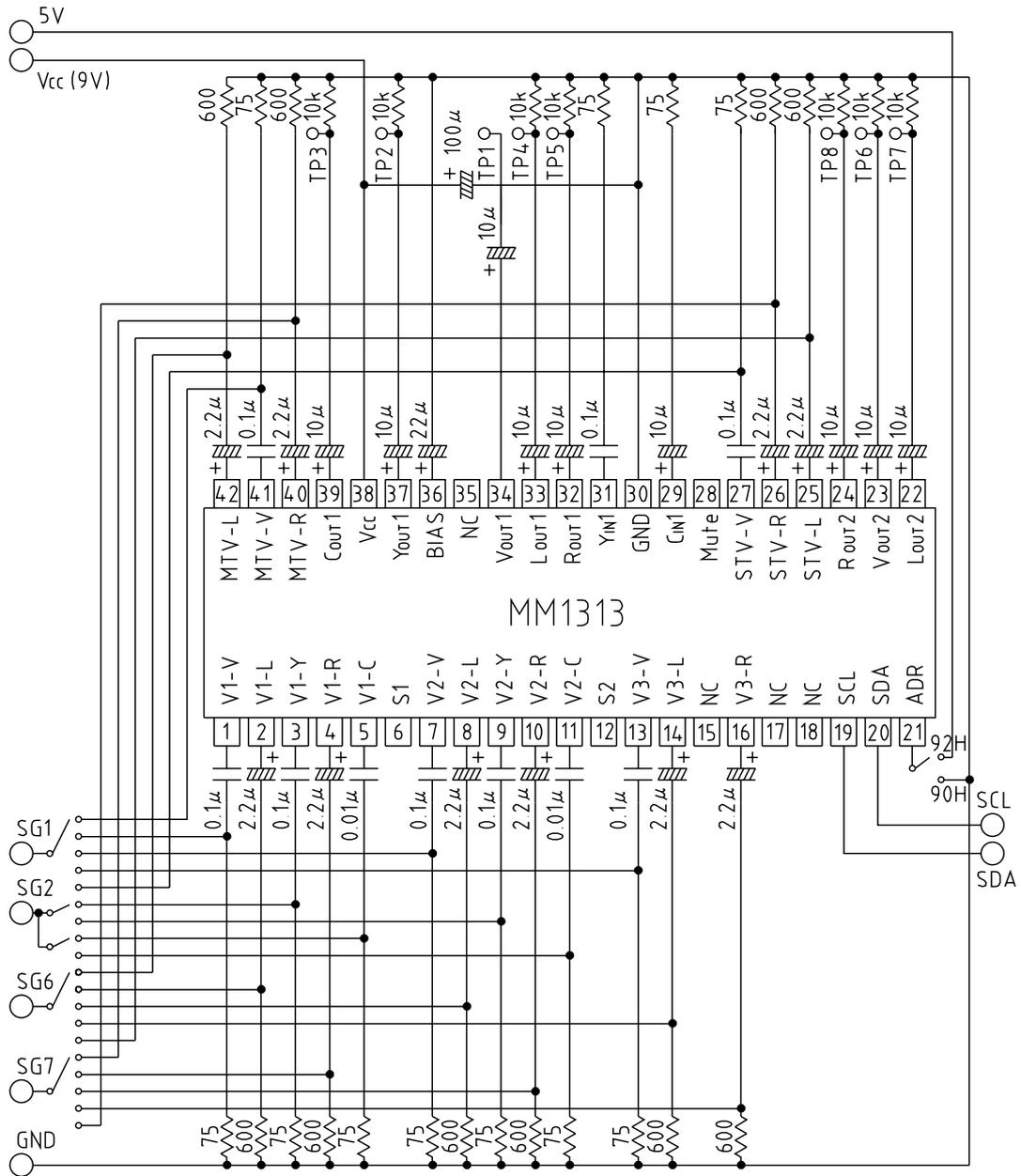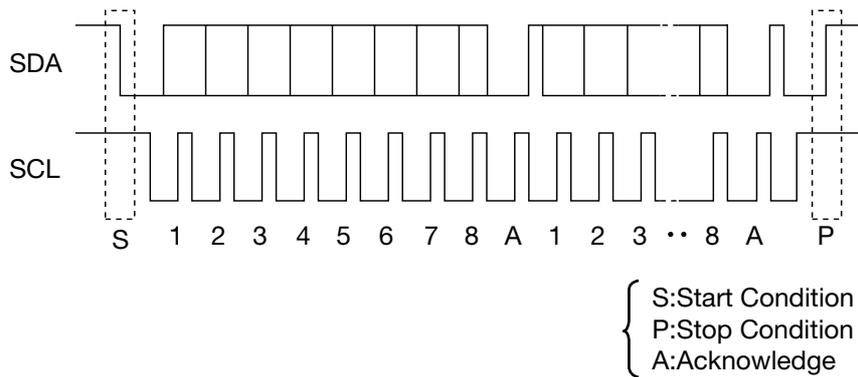
The I²C BUS is a BUS system developed by Philips for internal use in equipment. Data transmission is carried out by the two SDA and SCL lines, in byte units, with the MSB first from start condition.

[Control Register]
The control register contains data sent from the master in order to determine the status of each switch.
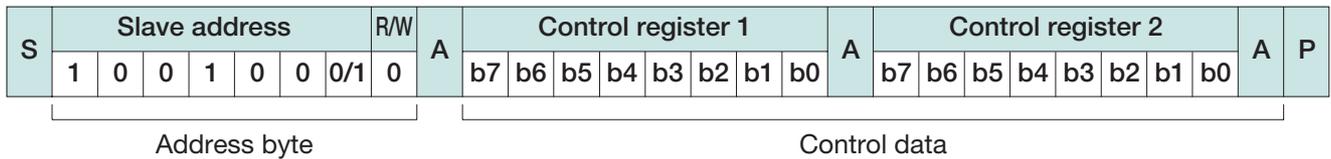
S	Slave address							R/W	A	Control register 1								A	Control register 2								A	P
	1	0	0	1	0	0	0/1	0		b7	b6	b5	b4	b3	b2	b1	b0		b7	b6	b5	b4	b3	b2	b1	b0		

Address byte   Control data

The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 0 when using as a control register.
The MM1313 slave address can be selected as 90H/92H depending on the status of the ADR pin. When ADR pin is low it is 90H.
The relationship between the control register bits and switch control is as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
Audio Gain	S/Comp Select	Video–Select			Audio–Select		

The control register bits are reset to 0 when power is applied.
MM1313 control is carried out by the 3-byte structure of the 1 address byte and 2 control data bytes. The first byte in the control data is control data for output 1, and the remaining 1 byte is control data for output 2.
All of the remaining data (fourth byte and after) are ignored.
Refer to the separate tables for details on switch control.

[Status Register]

The status register contains data for sending device status to the master.
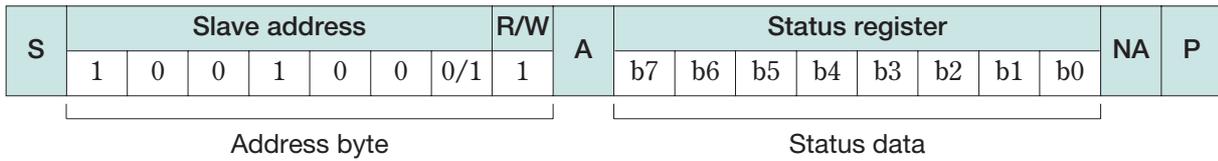
S	Slave address						R/W	A	Status register								NA	P
	1	0	0	1	0	0	0/1	1		b7	b6	b5	b4	b3	b2	b1	b0		

Address byte   Status data

The data format is set as shown in the figure above. The first 7 bits in the address byte are allocated to the slave address, and the remaining 1 bit is allocated to the read/write bit. The read/write bit is set at 1 when using as a status register.

The MM1313 slave address can be selected as 91H/93H depending on the status of the ADR pin. When the ADR pin is low it is 91H. However, the confirmation response after completion of the status register should be non-acknowledge.

The status register output data as shown below.

b7	b6	b5	b4	b3	b2	b1	b0
P-ON RESET	×	S1 OPEN	S1 SEL	S2 OPEN	S2 SEL	×	×

P-ON RESET : Returns 1 for power on reset. However once data read begins, 0 is returned next.
S1/S2 OPEN : Returns 0 when the S1/S2 pin is not open, and returns 1 when the S1/S2 pin is open
S1/S2 SEL : Returns 0 when the S1/S2 pin is not grounded, and returns 1 when the S1/S2 pin is grounded.

S1/S2 OPEN, SEL have 3-value discrimination, and the combinations are as shown below.

S1/S2 pin DC voltage	S1/S2 OPEN	S1/S2 SEL
0.8V or less	0	1
1.3V or more, 3.5V or less	0	0
4.5V or more	1	0

[Power On Reset]

Power on reset is built in to reset each control register to 0 when power is turned on.

Power on reset threshold has hysteresis as shown in the figure below. The IC power on reset status can be discriminated by reading the status register P-ON RESET.
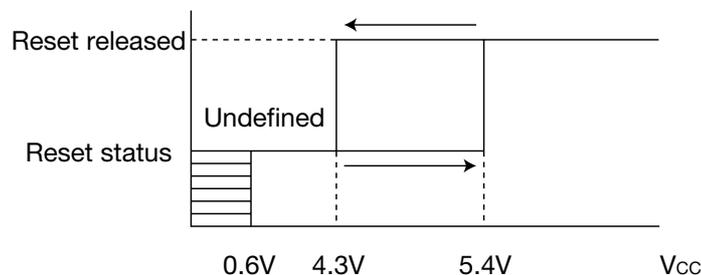
Switch Control Table

1. Video Output 1

b6	b5	b4	b3	V$_{OUT}$1	Y$_{OUT}$1	C$_{OUT}$1
0	0	0	0	Mute	Mute	Mute
0	0	0	1	MTV–V	Y$_{IN}$1	C$_{IN}$1
0	0	1	0	V1–V	Y$_{IN}$1	C$_{IN}$1
0	0	1	1	V2–V	Y$_{IN}$1	C$_{IN}$1
0	1	0	0	V3–V	Y$_{IN}$1	C$_{IN}$1
0	1	0	1	STV–V	Y$_{IN}$1	C$_{IN}$1
0	1	1	0	Mute	Mute	Mute
0	1	1	1	Mute	Mute	Mute
1	0	0	0	Mute	Mute	Mute
1	0	0	1	MTV–V	Y$_{IN}$1	C$_{IN}$1
1	0	1	0	V1–Y+C	V1–Y	V1–C
1	0	1	1	V2–Y+C	V2–Y	V2–C
1	1	0	0	V3–V	Y$_{IN}$1	C$_{IN}$1
1	1	0	1	STV–V	Y$_{IN}$1	C$_{IN}$1
1	1	1	0	Mute	Mute	Mute
1	1	1	1	Mute	Mute	Mute

2. Video Output 2

b6	b5	b4	b3	V$_{OUT}$2
0	0	0	0	Mute
0	0	0	1	MTV–V
0	0	1	0	V1–V
0	0	1	1	V2–V
0	1	0	0	V3–V
0	1	0	1	STV–V
0	1	1	0	Mute
0	1	1	1	Mute
1	0	0	0	Mute
1	0	0	1	MTV–V
1	0	1	0	V1–Y+C
1	0	1	1	V2–Y+C
1	1	0	0	V3–V
1	1	0	1	STV–V
1	1	1	0	Mute
1	1	1	1	Mute

3. Audio Output 1

Mute pin	b2	b1	b0	L$_{OUT}$1	R$_{OUT}$1
1.5V or less (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV–L	MTV–R
	0	1	0	V1–L	V1–R
	0	1	1	V2–L	V2–R
	1	0	0	V3–L	V3–R
	1	0	1	STV–L	STV–R
	1	1	0	Mute	Mute
	1	1	1	Mute	Mute
3.0V or more	–	–	–	Mute	Mute

4. Audio Output 1 Gain Switching

b7	Output gain
0	–6dB output
1	0dB output

5. Audio Output 2

Mute pin	b2	b1	b0	L$_{OUT}$2	R$_{OUT}$2
1.5V or less (OPEN)	0	0	0	Mute	Mute
	0	0	1	MTV–L	MTV–R
	0	1	0	V1–L	V1–R
	0	1	1	V2–L	V2–R
	1	0	0	V3–L	V3–R
	1	0	1	STV–L	STV–R
	1	1	0	Mute	Mute
	1	1	1	Mute	Mute
3.0V or more	–	–	–	Mute	Mute

Application Circuit
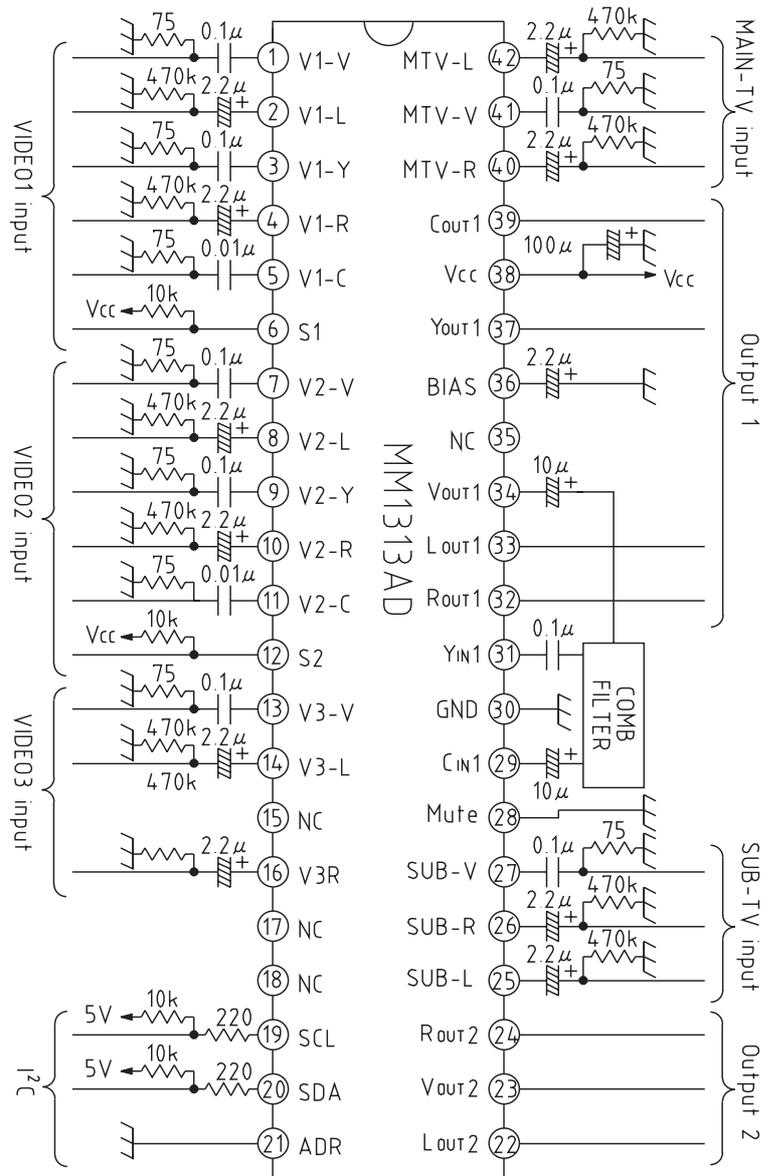
Notes

1. V$_{OUT}$ is set at 4.4V and C$_{IN}$ at 4.9V

   Please note that capacitance polarity may vary depending on comb filter bias.

2. Each audio output can be muted by making pin 19 high. Mute is off when it is open or low.