Freescale Semiconductor
Hardware Specification

MCF5275EC/D
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MCF5275 Integrated Microprocessor Family Hardware Specification

32-Bit Embedded Controller Division

The MCF5275 family is a highly integrated implementation of the ColdFire® family of reduced instruction set computing (RISC) microprocessors. This document describes pertinent features and functions characteristics of the MCF5275 family. The MCF5275 family includes the MCF5275, MCF5275L, MCF5274 and MCF5274L microprocessors. The differences between these parts are summarized in Table 1. This document is written from the perspective of the MCF5275 and unless otherwise noted, the information applies also to the MCF5275L, MCF5274 and MCF5274L.

The MCF5275 family delivers a new level of performance and integration on the popular version 2 ColdFire core with up to 159 (Dhrystone 2.1) MIPS @ 166MHz. These highly integrated microprocessors build upon the widely used peripheral mix on the popular MCF5272 ColdFire microprocessor (10/100 Mbps Ethernet MAC and USB device) by adding a second 10/100 Mbps Ethernet MAC (MCF5274 and MCF5275) and hardware encryption (MCF5275L and MCF5275). In addition, the MCF5275 family features an Enhanced Multiply Accumulate Unit (EMAC), large on-chip

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memory (64 Kbytes SRAM, 16 Kbytes configurable cache), and a 16-bit DDR SDRAM memory controller.

These devices are ideal for cost-sensitive applications requiring significant control processing for file management, connectivity, data buffering, and user interface, as well as signal processing in a variety of key markets such as security, imaging, networking, gaming, and medical. This leading package of integration and high performance allows fast time to market through easy code reuse and extensive third party tool support.

To locate any published errata or updates for this document, refer to the ColdFire products website at http://www.freescale.com.

1 MCF5275 Family Configurations

Table 1. MCF5275 Family Configurations

Module	5274L	5275L	5274	5275
ColdFire Version 2 Core with EMAC (Enhanced Multiply-Accumulate Unit)	x	x	x	x
System Clock	up to 166 MHz			
Performance (Dhrystone 2.1 MIPS)	up to 159			
Instruction/Data Cache	16 Kbytes (configurable)			
Static RAM (SRAM)	64 Kbytes			
Interrupt Controllers (INTC)	2	2	2	2
Edge Port Module (EPORT)	x	x	x	x
External Interface Module (EIM)	x	x	x	x
4-channel Direct-Memory Access (DMA)	x	x	x	x
DDR SDRAM Controller	x	x	x	x
Fast Ethernet Controller (FEC)	1	1	2	2
Watchdog Timer Module (WDT)	x	x	x	x
4-channel Programmable Interval Timer Module (PIT)	x	x	x	x
32-bit DMA Timers	4	4	4	4
USB	x	x	x	x
QSPI	x	x	x	x
UART(s)	3	3	3	3
I^2C	x	x	x	x
PWM	4	4	4	4
General Purpose I/O Module (GPIO)	x	x	x	x
CIM = Chip Configuration Module + Reset Controller Module	x	x	x	x

Table 1. MCF5275 Family Configurations

Module	5274L	5275L	5274	5275
Debug BDM	x	x	x	x
JTAG - IEEE 1149.1 Test Access Port	x	x	x	x
Hardware Encryption	—	x	—	x
Package	196 MAPBGA	196 MAPBGA	256 MAPBGA	256 MAPBGA

2 Block Diagram

The superset device in the MCF5275 family comes in a 256 Mold Array Plastic Ball Grid Array (MAPBGA) package.

Figure 1 shows a top-level block diagram of the MCF5275, the superset device.

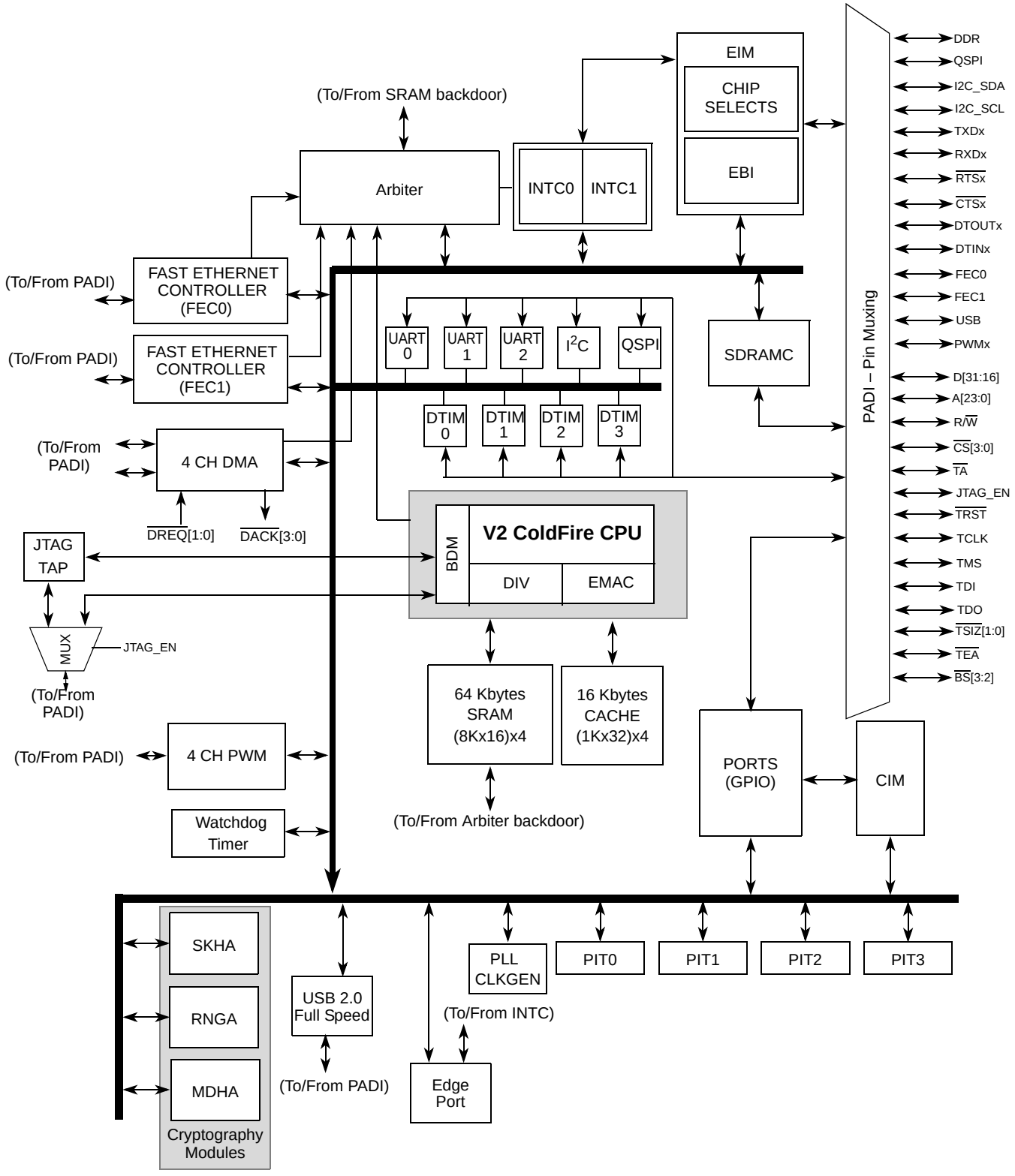


Figure 1. MCF5275 Block Diagram

3 Features

This document contains information on a new product. Specifications and information herein are subject to change without notice.

3.1 Feature Overview

- ColdFire version 2 variable-length RISC processor
  - Static operation
  - 32-bit address and data path on-chip
  - 166/133 MHz processor core and 83/66.5 MHz bus frequency
  - Sixteen general-purpose 32-bit data and address registers
  - Enhanced multiply accumulate unit (eMAC) for DSP and fast multiply operations
- System debug support
  - Real time trace for determining dynamic execution path while in emulator mode
  - Background debug mode (BDM) for debug features while halted
  - Real time debug support, with two user visible hardware breakpoint registers (PC and address with optional data) that can be configured into a 1- or 2-level trigger
- On chip memories
  - 16 Kbyte cache, configurable as I-cache or I-cache and D-cache
  - 64 Kbyte dual-ported SRAM on CPU internal bus with standby power supply support
- Power management
  - Fully static operation with processor sleep and whole chip stop modes
  - Very rapid response to interrupts from the low-power sleep mode (wake-up feature)
- Two Fast Ethernet Media Access Controllers (FEC MAC)
  - 10 base T capability, half or full duplex
  - 100 base T capability, half or full duplex throughput
  - On chip transmit and receive FIFOs
  - Built-in DMA controller
  - Memory-based flexible descriptor rings
  - Media independent interface (MII)
- USB Device Module
  - Supports full-speed 12-Mbps and low-speed 1.5-Mbps USB devices
  - Full compliance with the *Universal Serial Bus Specification, Revision 2.0*
  - Automatic hardware processing of USB standard device requests
  - Supports external USB transceiver
  - Protocol control and administration for up to four endpoints (programmable types)

  - One FIFO RAM per endpoint (2-Kbyte total)
  - Dedicated 1-Kbyte descriptor RAM, accessible from the Slave bus
  - Remote wake-up
- Hardware cryptography accelerator (optional)
  - Random number generator
  - DES/3DES/AES block cipher engine
  - MD5/SHA-1/HMAC accelerator
- Three Universal Asynchronous/synchronous Receiver Transmitters (UARTs)
  - Serial communication channel
  - 16-bit divider for clock generation
  - Internal channel control logic
  - Interrupt control logic
  - Maskable interrupts
  - DMA support
  - Programmable clock-rate generator
  - Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
  - Up to 2 stop bits in 1/16 increments
  - Error-detection capabilities
  - Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines
  - Transmit and receive FIFO buffers
- I^2C Module
  - Interchip bus interface for EEPROMs, LCD controllers, A/D converters, and keypads
  - Fully compatible with industry-standard I^2C bus
  - Master or slave modes support multiple masters
  - Automatic interrupt generation with programmable level
- Queued Serial Peripheral Interface (QSPI)
  - Full-duplex, three-wire synchronous transfer
  - Up to four chip selects available
  - Master operation
  - Programmable master bit rates
  - Up to 16 preprogrammed transfers
- Four 32-bit Timers with DMA request capability
- Pulse width modulation (PWM) unit
  - Four identical channels
- Software Watchdog Timer

  - 16-bit counter
  - Low power mode support
- Phase Locked Loop (PLL)
  - Reference crystal 8 to 25 MHz
  - Low power modes supported
  - Separate CLKOUT and $\overline{\text{DDR\_CLKOUT}}$ signals
- Four Programmable Interrupt Timers (PITs)
- Interrupt Controllers (x2)
  - Support for 58 independent interrupt sources, organized as follows:
    - 51 fully-programmable interrupt sources
    - 7 fixed-level external interrupt sources
  - Unique vector number for each interrupt source
  - Ability to mask any individual interrupt source or all interrupt sources (global mask-all)
  - Support for hardware and software interrupt acknowledge (IACK) cycles
  - Combinatorial path to provide wake-up from low power modes
- DMA Controller
  - Four fully programmable channels
  - Dual-address and single-address transfer support with 8-, 16-, and 32-bit data capability
  - Source/destination address pointers that can increment or remain constant
  - 24-bit transfer counter per channel
  - Auto-alignment transfers supported for efficient block movement
  - Bursting and cycle steal support
  - Two-bus-clock internal access
  - External request pins for each channel
- External Memory Interface
  - External glueless connections to 8-, 16-, and 32-bit external memory devices (e.g., SRAM, flash, ROM, etc.)
  - Glueless interface to SRAM devices with or without byte strobe inputs
  - Programmable wait state generator
  - 16-bit external bidirectional data bus
  - 24-bit address bus
  - Eight chip selects
  - Byte/write enables
  - Ability to boot from external memories that are 8 or 16 bits wide
- DDR SDRAM controller

  - Supports 16-bit wide memory devices
  - Supports Dual Data Rate (DDR) SDRAM.
  - Page mode support
  - Programmable refresh interval timer.
  - Sleep mode and self-refresh.
  - Supports 16-byte (4-beat, 4-byte) critical-word-first burst transfer.
  - Memory sizes from 8 Mbyte to 128 MByte (per chip select)
  - 166 MHz data transfer rate (DDR)
  - Two independent chip selects
- Reset
  - Separate Reset In and Reset Out signals
  - Six sources of reset (POR, External, Software, Watchdog, Loss of clock/lock)
  - Status flag indication of source of last reset
- Chip Configurations
  - System configuration during reset
  - Bus Monitor, Abort Monitor
  - Configurable output pad drive strength
  - Unique Part Identification and Part Revision Numbers
- General Purpose I/O interface
  - Up to 69 bits of general purpose I/O
  - Coherent 32-bit control
  - Bit manipulation supported via set/clear functions
  - Unused peripheral pins may be used as extra GPIO
- JTAG support for system level board testing
  - Unique JTAG Part Identification and Part Revision Numbers

3.2 V2 Core Overview

The ColdFire V2 core is comprised of two separate pipelines that are decoupled by an instruction buffer. The two-stage Instruction Fetch Pipeline (IFP) is responsible for instruction-address generation and instruction fetch. The instruction buffer is a first-in-first-out (FIFO) buffer that holds prefetched instructions awaiting execution in the Operand Execution Pipeline (OEP). The OEP includes two pipeline stages. The first stage decodes instructions and selects operands (DSOC); the second stage (AGEX) performs instruction execution and calculates operand effective addresses, if needed.

The V2 core implements the ColdFire Instruction Set Architecture Revision A with added support for a separate user stack pointer register and four new instructions to assist in bit processing. Additionally, the V2 core includes the enhanced multiply-accumulate unit (EMAC) for improved signal processing capabilities. The EMAC implements a 4-stage execution pipeline, optimized for 32 x 32 bit operations,

with support for four 48-bit accumulators. Supported operands include 16- and 32-bit signed and unsigned integers as well as signed fractional operands as well as a complete set of instructions to process these data types. The EMAC provides superb support for execution of DSP operations within the context of a single processor at a minimal hardware cost.

3.3 Debug Module

The ColdFire processor core debug interface is provided to support system debugging in conjunction with low-cost debug and emulator development tools. Through a standard debug interface, users can access real-time trace and debug information. This allows the processor and system to be debugged at full speed without the need for costly in-circuit emulators. The debug interface is a superset of the BDM interface provided on Motorola's 683xx family of parts.

The on-chip breakpoint resources include a total of 6 programmable registers—a set of address registers (with two 32-bit registers), a set of data registers (with a 32-bit data register plus a 32-bit data mask register), and one 32-bit PC register plus a 32-bit PC mask register. These registers can be accessed through the dedicated debug serial communication channel or from the processor's supervisor mode programming model. The breakpoint registers can be configured to generate triggers by combining the address, data, and PC conditions in a variety of single or dual-level definitions. The trigger event can be programmed to generate a processor halt or initiate a debug interrupt exception.

To support program trace, the Version 2 debug module provides processor status (PST[3:0]) and debug data (DDATA[3:0]) ports. These buses and the PSTCLK output provide execution status, captured operand data, and branch target addresses defining processor activity at the CPU's clock rate.

3.4 JTAG

The MCF5275 microprocessors support circuit board test strategies based on the Test Technology Committee of IEEE and the Joint Test Action Group (JTAG). The test logic includes a test access port (TAP) consisting of a 16-state controller, an instruction register, and three test registers (a 1-bit bypass register, a 326-bit boundary-scan register, and a 32-bit ID register). The boundary scan register links the device's pins into one shift register. Test logic, implemented using static logic design, is independent of the device system logic.

The MCF5275 implementation can do the following:

- Perform boundary-scan operations to test circuit board electrical continuity
- Sample MCF5275 system pins during operation and transparently shift out the result in the boundary scan register
- Bypass the MCF5275 for a given circuit board test by effectively reducing the boundary-scan register to a single bit
- Disable the output drive to pins during circuit-board testing
- Drive output pins to stable levels

3.5 On-chip Memories

The 64 Kbyte data RAM and the 16 Kbyte cache RAM for the processors are built using a RAM compiler. Both RAM blocks connect directly to the RAM controller via a standard single-port synchronous SRAM interface.

3.5.1 Cache

The 16-Kbyte cache can be configured into one of three possible organizations: a 16-Kbyte instruction cache, a 16-Kbyte data cache or a split 8-Kbyte instruction/8-Kbyte data cache. The configuration is software-programmable by control bits within the privileged Cache Configuration Register (CACR). In all configurations, the cache is a direct-mapped single-cycle memory.

3.5.2 SRAM

The SRAM module provides a general-purpose 64-Kbyte memory implemented as four 16-Kbyte blocks that the ColdFire core can access in a single cycle. The location of the memory block can be set to any 64-Kbyte boundary within the 4-Gbyte address space. The memory is ideal for storing critical code or data structures, for use as the system stack, or for storing FEC data buffers. Because the SRAM module is physically connected to the processor's high-speed local bus, it can quickly service core-initiated accesses or memory-referencing commands from the debug module.

The SRAM module is also accessible by non-core bus masters, for example the DMA and/or the FECs. The dual-ported nature of the SRAM makes it ideal for implementing applications with double-buffer schemes, where the processor and a DMA device operate in alternate regions of the SRAM to maximize system performance. As an example, system performance can be increased significantly if Ethernet packets are moved from the FEC into the SRAM (rather than external memory) prior to any processing.

3.6 Power Management

The MCF5275 family incorporates several low power modes of operation which are entered under program control and exited by several external trigger events. An integrated Power-On Reset (POR) circuit monitors the input supply and forces an MCU reset as the supply voltage rises.

3.7 Fast Ethernet Controller (FEC)

The MCF5275 family contains up to two 10/100 BaseT fast Ethernet Controllers (FECs). Refer to Table 1 for device configurations.

Each FEC includes these distinctive features:

- IEEE 802.3 MAC (compliant with IEEE 802.3 1998 edition)
- Built-in FIFO and DMA controller
- Support for different Ethernet physical interfaces:
  - 100Mbps IEEE 802.3 MII
  - 10Mbps IEEE 802.3 MII

- Support for full-duplex operation (200Mbps throughput) with a minimum system clock of 50MHz
- Support for half-duplex operation (100Mbps throughput) with a minimum system clock rate of 25MHz
- IEEE 802.3 full duplex flow control
- Programmable max frame length supports IEEE 802.1 VLAN tags and priority
- Retransmission from transmit FIFO following a collision (no system bus utilization)
- Automatic internal flushing of the receive FIFO for runts (collision fragments) and address recognition rejects (no system bus utilization)
- Address recognition
  - Frames with broadcast address may be always accepted or always rejected
  - Exact match for single 48-bit individual (unicast) address
  - Hash (64-bit hash) check of individual (unicast) addresses
  - Hash (64-bit hash) check of group (multicast) addresses
  - Promiscuous mode
- RMON and IEEE statistics
- Interrupts for network activity and error conditions

3.8 Universal Serial Bus (USB)

The USB controller supports device mode data communications with a USB host (typically a PC).

The programmable USB registers allow the user to enable or disable the module, control characteristics of individual endpoints, and monitor traffic flow through the module without ever seeing the low-level details of the USB protocol.

The USB module provides the following features to the user:

- Supports full-speed 12-Mbps USB devices and low-speed 1.5-Mbps devices
- Full compliance with the *Universal Serial Bus Specification, Revision 2.0*
- Automatic hardware processing of USB standard device requests
- USB device controller with protocol control and administration for up to eight endpoints, 16 interfaces, and 16 configurations. Endpoint types are programmable with support for up to eight control, interrupt, bulk, or isochronous endpoints
- Independent interrupts for each endpoint
- Supports remote wakeup via a register bit
- Detects start-of-frame and missed start-of-frame for isochronous endpoint synchronization
- Notification of start-of-frame, reset, suspend, and resume events

3.9 Cryptography

Some of the MCF5275 family devices incorporate small, fast, and dedicated hardware accelerators for random number generation, message digest and hashing, and the DES, 3DES, and AES block cipher functions. This allows for the implementation of common Internet security protocol cryptography operations with performance well in excess of software-only algorithms. Refer to Table 1 for device configurations.

3.10 UARTs

The MCF5275 family of microprocessors each contain three (3) UARTs that function independently. Any of the three UARTs can be clocked by the system bus clock, eliminating the need for an external crystal.

Each UART module contains the following major functional features:

- Serial communication channel
- 16-bit divider for clock generation
- Internal channel control logic
- Interrupt control logic
- Maskable interrupts
- DMA support
- Programmable clock-rate generator
- Data formats can be 5, 6, 7 or 8 bits with even, odd or no parity
- Up to 2 stop bits in 1/16 increments
- Error-detection capabilities
- Modem support includes request-to-send (RTS) and clear-to-send (CTS) lines
- Transmit and receive FIFO buffers
- UART Modes of Operation:
  - Full-duplex
  - Auto-echo loopback
  - Local loopback
  - Remote loopback

3.11 I^2C Bus

The I^2C is a two-wire, bidirectional serial bus that provides a simple, efficient method of data exchange, minimizing the interconnection between devices. This bus is suitable for applications requiring occasional communications over a short distance between many devices. The flexible I^2C allows additional devices to be connected to the bus for expansion and system development.

The I^2C includes these distinctive features:

- Compatibility with I^2C bus standard

- Multiple-master operation
- Software programmable for one of 64 different serial clock frequencies
- Software selectable acknowledge bit
- Interrupt driven, byte-by-byte data transfer
- Arbitration lost interrupt with automatic mode switching from master to slave
- Calling address identification interrupt
- Start and stop signal generation/detection
- Repeated START signal generation
- Acknowledge bit generation/detection
- Bus-busy detection
- DMA support

3.12 QSPI

The queued serial peripheral interface module provides a serial peripheral interface with queued transfer capability. It allows users to enqueue up to 16 transfers at once, eliminating CPU intervention between transfers. Transfer RAMs in the QSPI are indirectly accessible using address and data registers.

The QSPI contains the following features:

- Programmable queue to support up to 16 transfers without user intervention
- Supports transfer sizes of 8 to 16 bits in 1-bit increments
- Four peripheral chip-select lines
- Baud rates from 162.1 Kbps to 20.75 Mbps at 83 MHz
- Programmable delays before and after transfers
- Programmable clock phase and polarity
- Supports wraparound mode for continuous transfers

3.13 DMA Timers (DTIM0-DTIM3)

There are four independent, general purpose 32-bit platform timers (DTIM0, DTIM1, DTIM2, DTIM3) on the MCF5275 family of microprocessors. The output of an 8-bit prescaler clocks each timer.

Each of the platform timer modules has these distinctive features:

- Programmable sources for the clock input, including external clock
- Input capture capability with programmable trigger edge on input pin
- Output compare with programmable mode for the output pin
- Free run and restart modes
- Maskable interrupts on input capture or reference compare
- DMA support

Each of the four timer modules has four operating modes:

- Capture mode
- Output mode
- Reference compare mode

3.14 Pulse Width Modulation (PWM) Module

The Pulse Width Modulation (PWM) module generates a synchronous series of pulses having programmable duty cycle. With a suitable low-pass filter, the PWM can be used as a digital-to-analog converter.

The PWM module has six channels with independent control of left and center aligned outputs on each channel. The MCF5275 family uses four of these channels namely 0, 1, 2 and 3. The emergency shutdown functionality (channel 5 only) is not used for the MCF5275 family.

Each of the PWM channels has a programmable period and duty cycle as well as a dedicated counter. A flexible clock select scheme allows a total of four different clock sources to be used with the counters. Each of the modulators can create independent continuous waveforms with software-selectable duty rates from 0% to 100%. The PWM outputs can be programmed as left aligned outputs or center aligned outputs

Summary of the main features include:

- Independent PWM channels with programmable period and duty cycle
- Dedicated counter for each PWM channel
- Programmable PWM enable/disable for each channel
- Software selection of PWM duty pulse polarity for each channel
- Period and duty cycle are double buffered. Change takes effect when the end of the effective period is reached (PWM counter reaches zero) or when the channel is disabled.
- Programmable center or left aligned outputs on individual channels
- 16-bit PWM resolution available by concatenating 8-bit channels
- Four clock sources (A, B, SA and SB) provide for a wide range of frequencies.
- Programmable Clock Select Logic

3.15 Software Watchdog Timer (WDT)

The watchdog timer is a 16-bit timer for helping software recover from runaway code. The watchdog counter is a free-running down-counter that generates a reset on underflow. To prevent a reset, software must periodically restart the countdown.

3.16 Phase Locked Loop (PLL)

The clock module contains a crystal oscillator (OSC), frequency modulated phase-locked loop (PLL), reduced frequency divider (RFD), status/control registers, and control logic. To improve noise immunity,

the PLL and OSC have their own power supply inputs, VDDPLL and VSSPLL. All other circuits are powered by the normal supply pins, VDD and VSS.

3.17 Interrupt Controllers (INTC0/INTC1)

There are two interrupt controllers which support 58 interrupt sources on the MCF5275. Each interrupt controller is organized as 7 levels with 9 interrupt sources per level. Each interrupt source has a unique interrupt vector, and 51 of the 58 sources of a given controller provide a programmable level [1-7] and priority within the level.

3.18 Direct Memory Access Controller (DMAC)

The Direct Memory Access Controller (DMA) Module provides an efficient way to move blocks of data with minimal processor interaction. The DMA module provides four channels that allow byte, word, or longword operand transfers. These transfers can be single or dual address to off-chip devices or dual address to on-chip devices.

The DMA contains the following features:

- Four fully independent, programmable DMA controller channels/bus modules
- Auto-alignment feature for source or destination accesses
- Single- and dual-address transfers
- Up to four external request pins ($\overline{\text{DREQ}}$[3:0])
- Channel arbitration on transfer boundaries
- Data transfers in 8-, 16-, 32- or 128-bit blocks via a 16-byte buffer
- Supports continuous-mode and cycle-steal transfers
- Independent transfer widths for source and destination
- Independent source and destination address registers
- Provide two clock data transfers

3.19 External Interface Module (EIM)

The external interface module on MCF5275 devices handles the transfer of information between the internal core and memory, peripherals, or other processing elements in the external address space.

Programmable chip select outputs provide signals to enable external memory and peripheral circuits, providing all handshaking and timing signals for automatic wait-state insertion and data bus sizing.

Base memory address and block size are programmable, with some restrictions. For example, the starting address must be on a boundary that is a multiple of the block size. Each chip select is general purpose; however, any one of the chip selects can be programmed to provide read and write enable signals suitable for use with most popular static RAMs and peripherals. Data bus width (8-bit, 16-bit, or 32-bit) is programmable on all chip selects, and further decoding is available for protection from user mode access or read-only access.

The key features of the EIM are summarized below:

- Eight independent, user-programmable chip-select signals (CS[7:0]) that interface with various memory types and peripherals
- Address masking for 64 Kbyte to 4 gigabyte memory block sizes
- Programmable wait states and port sizes
- External master access to chip selects

3.20 Double Data Rate (DDR) Synchronous DRAM (SDRAM) Controller

The SDRAMC provides a 16-bit glueless external interface to double-data-rate (DDR) SDRAM memory devices. It is responsible for providing address, data and control signals for up to two independent chip-selects.

The SDRAMC includes the following features:

- Supports a glueless interface to DDR SDRAMs
- 16-bit fixed memory port width
- 32-bit data bus interface to Coldfire core
- 16 bytes (8 beat x 16-bit) critical word first burst transfer
- Up to 14 row address lines, up to 12 column address lines, maximum of two chip selects. The maximum row bits plus column bits is 24.
- Supported SDRAM devices include: 8, 16, 32, 64, and 128Mbyte per chip select
- Minimum memory configuration of 8 Mbyte—12 bit row address (RA), 8 bit column address (CA), 2 bit bank address (BA) and one chip select
- Supports page mode to maximize the data rate
- Supports sleep mode and self-refresh mode
- Error detect and parity check are not supported

3.21 Resets

The Reset Controller is provided to determine the cause of reset, assert the appropriate reset signals to the system, and then to keep a history of what caused the reset.

The MCF5275 family has six (6) sources of reset:

- External
- Power On Reset (POR)
- Watchdog timer
- PLL Loss of Lock
- PLL Loss of Clock
- Software

External reset on the RSTOUT pin is software-assertable independent of chip reset state. There are also software-readable status flags indicating the cause of the last reset.

3.22 General Purpose I/O

Most peripheral I/O pins on MCF5275 devices are muxed with GPIO, adding flexibility and usability to all signals on the chip.

4 Signal Descriptions

Table 2 lists the signals for the MCF5275 in functional group order.

NOTE

In this table and throughout this document a single signal within a group is designated without square brackets (i.e., A24), while designations for multiple signals within a group use brackets (i.e., A[23:21]) and is meant to include all signals within the two bracketed numbers when these numbers are separated by a colon.

NOTE

The primary functionality of a pin is not necessarily its default functionality. Pins that are muxed with GPIO will default to their GPIO functionality.

Table 2. Signal Information and Muxing

Name	GPIO Port	Alternate1	Alternate2	Dir.[1]	Bonded on MCF5274/75 256 MAPBGA	Bonded on MCF5274L/5L 196 MAPBGA
Reset						
$\overline{\text{RESET}}$	—	—	—	I	1	1
$\overline{\text{RSTOUT}}$	—	—	—	O	1	1
Clock						
EXTAL	—	—	—	I	1	1
XTAL	—	—	—	O	1	1
CLKOUT	—	—	—	O	1	1
Mode Selection						
CLKMOD[1:0]	—	—	—	I	2	2
$\overline{\text{RCON}}$	—	—	—	I	1	1
External Memory Interface and Ports						
A[23:21]	PADDR[7:5]	$\overline{\text{CS}}$[6:4]	—	O	3	3

Table 2. Signal Information and Muxing (continued)

Name	GPIO Port	Alternate1	Alternate2	Dir.[1]	Bonded on MCF5274/75 256 MAPBGA	Bonded on MCF5274L/5L 196 MAPBGA
A[20:0]	—	—	—	O	21	21
D[31:16]	—	—	—	O	16	16
$\overline{BS}$[3:2]	$\overline{PBS}$[3:2]	$\overline{CAS}$[3:2]	—	O	2	2
$\overline{OE}$	PBUSCTL[7]	—	—	O	1	1
$\overline{TA}$	PBUSCTL[6]	—	—	I	1	1
$\overline{TEA}$	PBUSCTL[5]	$\overline{DREQ1}$	—	I	1	0
R/$\overline{W}$	PBUSCTL[4]	—	—	O	1	1
TSIZ1	PBUSCTL[3]	$\overline{DACK1}$	—	O	1	1
TSIZ0	PBUSCTL[2]	$\overline{DACK0}$	—	O	1	1
$\overline{TS}$	PBUSCTL[1]	$\overline{DACK2}$	—	O	1	1
$\overline{TIP}$	PBUSCTL[0]	$\overline{DREQ0}$	—	O	1	0
Chip Selects						
$\overline{CS}$[7:1]	PCS[7:1]	—	—	O	7	7
CS0	—	—	—	O	1	1
DDR SDRAM Controller						
DDR_CLKOUT	—	—	—	O	1	1
$\overline{DDR\_CLKOUT}$	—	—	—	O	1	1
$\overline{SD\_CS}$[1:0]	PSDRAM[7:6]	$\overline{CS}$[3:2]	—	O	2	2
$\overline{SD\_SRAS}$	PSDRAM[5]	—	—	O	1	1
$\overline{SD\_SCAS}$	PSDRAM[4]	—	—	O	1	1
$\overline{SD\_WE}$	PSDRAM[3]	—	—	O	1	1
SD_A10	—	—	—	O	1	1
$\overline{SD\_DQS}$[1:0]	PSDRAM[1:0]	—	—	I/O	2	2
SD_CKE	PSDRAM[2]	—	—	O	1	1
SD_VREF	—	—	—	I	2	2
External Interrupts Port						
$\overline{IRQ}$[7:5]	PIRQ[7:5]	—	—	I	3	3
$\overline{IRQ}$[4]	PIRQ[4]	$\overline{DREQ2}$	—	I	1	1
$\overline{IRQ}$[3:2]	PIRQ[3:2]	$\overline{DREQ}$[3:2]	—	I	2	2
$\overline{IRQ1}$	PIRQ[1]	—	—	I	1	1

Table 2. Signal Information and Muxing (continued)

Name	GPIO Port	Alternate1	Alternate2	Dir.[1]	Bonded on MCF5274/75 256 MAPBGA	Bonded on MCF5274L/5L 196 MAPBGA
FEC0						
FEC0_MDIO	PFECI2C[5]	I2C_SDA	U2RXD	I/O	1	1
FEC0_MDC	PFECI2C[4]	I2C_SCL	U2TXD	O	1	1
FEC0_TXCLK	PFEC0H[7]	—	—	I	1	1
FEC0_TXEN	PFEC0H[6]	—	—	I	1	1
FEC0_TXD[0]	PFEC0H[5]	—	—	O	1	1
FEC0_COL	PFEC0H[4]	—	—	I	1	1
FEC0_RXCLK	PFEC0H[3]	—	—	I	1	1
FEC0_RXDV	PFEC0H[2]	—	—	I	1	1
FEC0_RXD[0]	PFEC0H[1]	—	—	I	1	1
FEC0_CRS	PFEC0H[0]	—	—	I	1	1
FEC0_TXD[3:1]	PFEC0L[7:5]	—	—	O	3	3
FEC0_TXER	PFEC0L[4]	—	—	O	1	1
FEC0_RXD[3:1]	PFEC0L[3:1]	—	—	I	3	3
FEC0_RXER	PFEC0L[0]	—	—	O	1	1
FEC1						
FEC1_MDIO	PFECI2C[3]	—	—	I/O	1	0
FEC1_MDC	PFECI2C[2]	—	—	O	1	0
FEC1_TXCLK	PFEC1H[7]	—	—	I	1	0
FEC1_TXEN	PFEC1H[6]	—	—	I	1	0
FEC1_TXD[0]	PFEC1H[5]	—	—	O	1	0
FEC1_COL	PFEC1H[4]	—	—	I	1	0
FEC1_RXCLK	PFEC1H[3]	—	—	I	1	0
FEC1_RXDV	PFEC1H[2]	—	—	I	1	0
FEC1_RXD[0]	PFEC1H[1]	—	—	I	1	0
FEC1_CRS	PFEC1H[0]	—	—	I	1	0
FEC1_TXD[3:1]	PFEC1L[7:5]	—	—	O	3	0
FEC1_TXER	PFEC1L[4]	—	—	O	1	0
FEC1_RXD[3:1]	PFEC1L[3:1]	—	—	I	3	0
FEC1_RXER	PFEC1L[0]	—	—	O	1	0

Table 2. Signal Information and Muxing (continued)

Name	GPIO Port	Alternate1	Alternate2	Dir.[1]	Bonded on MCF5274/75 256 MAPBGA	Bonded on MCF5274L/5L 196 MAPBGA
I^2C						
I2C_SDA	PFECI2C[1]	U2RXD	—	I/O	1	1
I2C_SCL	PFECI2C[0]	U2TXD	—	I/O	1	1
DMA						
$\overline{DACK}$[3:0] and $\overline{DREQ}$[3:0] do not have a dedicated bond pads. Please refer to the following pins for muxing: PCS3/PWM3 for $\overline{DACK3}$, PCS2/PWM2 for $\overline{DACK2}$, TSIZ1 for $\overline{DACK1}$, TSIZ0 for $\overline{DACK0}$, $\overline{IRQ3}$ for $\overline{DREQ3}$, $\overline{IRQ2}$ and $\overline{TA}$ for $\overline{DREQ2}$, $\overline{TEA}$ for $\overline{DREQ1}$, and $\overline{TIP}$ for $\overline{DREQ0}$.					—	—
QSPI						
QSPI_CS[3:2]	PQSPI[6:5]	PWM[3:2]	$\overline{DACK}$[3:2]	O	2	2
QSPI_CS1	PQSPI[4]	SD_CKE	—	O	1	1
QSPI_CS0	PQSPI[3]	—	—	O	1	1
QSPI_CLK	PQSPI[2]	I2C_SCL	—	O	1	1
QSPI_DIN	PQSPI[1]	I2C_SDA	—	I	1	1
QSPI_DOUT	PQSPI[0]	—	—	O	1	1
UARTs						
$\overline{U0CTS}$	PUARTL[0]	—	—	I	1	1
$\overline{U0RTS}$	PUARTL[1]	—	—	O	1	1
U0RXD	PUARTL[3]	—	—	I	1	1
U0TXD	PUARTL[2]	—	—	O	1	1
$\overline{U1CTS}$	PUARTL[4]	—	—	I	1	1
$\overline{U1RTS}$	PUARTL[5]	—	—	O	1	1
U1RXD	PUARTL[7]	—	—	I	1	1
U1TXD	PUARTL[6]	—	—	O	1	1
$\overline{U2CTS}$	PUARTH[1]	PWM1	—	I	1	0
$\overline{U2RTS}$	PUARTH[0]	PWM0	—	O	1	0
U2RXD	PUARTH[3]	—	—	I	1	0
U2TXD	PUARTH[2]	—	—	O	1	0
USB						
USB_SPEED	PUSBH[0]	—	—	I/O	1	1

Table 2. Signal Information and Muxing (continued)

Name	GPIO Port	Alternate1	Alternate2	Dir.[1]	Bonded on MCF5274/75 256 MAPBGA	Bonded on MCF5274L/5L 196 MAPBGA
USB_CLK	PUSBL[7]	—	—	I	1	1
USB_RN	PUSBL[6]	—	—	I	1	1
USB_RP	PUSBL[5]	—	—	I	1	1
USB_RXD	PUSBL[4]	—	—	I	1	1
USB_SUSP	PUSBL[3]	—	—	O	1	1
USB_TN	PUSBL[2]	—	—	O	1	1
USB_TP	PUSBL[1]	—	—	O	1	1
USB_TXEN	PUSBL[0]	—	—	O	1	1
Timers (and PWMs)						
DT3IN	PTIMER[7]	DT3OUT	$\overline{\text{U2RTS}}$	I	1	1
DT3OUT	PTIMER[6]	PWM3	$\overline{\text{U2CTS}}$	O	1	1
DT2IN	PTIMER[5]	DT2OUT	—	I	1	1
DT2OUT	PTIMER[4]	PWM2	—	O	1	1
DT1IN	PTIMER[3]	DT1OUT	—	I	1	1
DT1OUT	PTIMER[2]	PWM1	—	O	1	1
DT0IN	PTIMER[1]	DT0OUT	—	I	1	1
DT0OUT	PTIMER[0]	PWM0	—	O	1	1
BDM/JTAG[2]						
DSCLK	—	$\overline{\text{TRST}}$	—	I	1	1
PSTCLK	—	TCLK	—	O	1	1
BKPT	—	TMS	—	I	1	1
DSI	—	TDI	—	I	1	1
DSO	—	TDO	—	O	1	1
JTAG_EN	—	—	—	I	1	1
DDATA[3:0]	—	—	—	O	4	4
PST[3:0]	—	—	—	O	4	4
Test						
TEST	—	—	—	I	1	1
PLL_TEST	—	—	—	I	1	1
Power Supplies						

Table 2. Signal Information and Muxing (continued)

Name	GPIO Port	Alternate1	Alternate2	Dir.[1]	Bonded on MCF5274/75 256 MAPBGA	Bonded on MCF5274L/5L 196 MAPBGA
VDDPLL	—	—	—	I	1	1
VSSPLL	—	—	—	I	1	1
VDD	—	—	—	I		
VSS	—	—	—	I		
OVDD	—	—	—	I		
OVSS	—	—	—	I		
SD_VDD	—	—	—	I		

NOTES:
1 Refers to pin's primary function. All pins which are configurable for GPIO have a pullup enabled in GPIO mode with the exception of PBUSCTL[7], PBUSCTL[4:0], PADDR, PBS, PSDRAM.
2 If JTAG_EN is asserted, these pins default to Alternate 1 (JTAG) functionality. The GPIO module is not responsible for assigning these pins.

4.1 Reset Signals

Table 3 describes signals that are used to either reset the chip or as a reset indication.

Table 3. Reset Signals

Signal Name	Abbreviation	Function	I/O
Reset In	$\overline{\text{RESET}}$	Primary reset input to the device. Asserting $\overline{\text{RESET}}$ immediately resets the CPU and peripherals.	I
Reset Out	$\overline{\text{RSTOUT}}$	Driven low for 128 CPU clocks when the soft reset bit of the system configuration register (SCR[SOFTRST]) is set. It is driven low for 32K CPU clocks when the software watchdog timer times out or when a low input level is applied to $\overline{\text{RESET}}$.	O

4.2 PLL and Clock Signals

Table 4 describes signals that are used to support the on-chip clock generation circuitry.

Table 4. PLL and Clock Signals

Signal Name	Abbreviation	Function	I/O
External Clock In	EXTAL	Always driven by an external clock input except when used as a connection to the external crystal when the internal oscillator circuit is used. The clock source is configured during reset by CLKMOD[1:0].	I
Crystal	XTAL	Used as a connection to the external crystal when the internal oscillator circuit is used to drive the crystal.	O
Clock Out	CLKOUT	This output signal reflects the internal system clock.	O

4.3 Mode Selection

Table 5 describes signals used in mode selection.

Table 5. Mode Selection Signals

Signal Name	Abbreviation	Function	I/O
Clock Mode Selection	CLKMOD[1:0]	Configure the clock mode after reset.	I
Reset Configuration	$\overline{\text{RCON}}$	Indicates whether the external D[31:16] pin states affect chip configuration at reset.	I

4.4 External Memory Interface Signals

These signals are used for doing transactions on the external bus.

Table 6 describes signals that are used for doing transactions on the external bus.

Table 6. External Memory Interface Signals

Signal Name	Abbreviation	Function	I/O
Address Bus	A[23:0]	The 24 dedicated address signals define the address of external byte, word, and longword accesses. These three-state outputs are the 24 lsbs of the internal 32-bit address bus and multiplexed with the SDRAM controller row and column addresses.	O
Data Bus	D[31:16]	These three-state bidirectional signals provide the general purpose data path between the processor and all other devices.	I/O

Table 6. External Memory Interface Signals (continued)

Signal Name	Abbreviation	Function	I/O
Byte Strobes	$\overline{BS}$[3:2]	Define the flow of data on the data bus. During SRAM and peripheral accesses, these output signals indicate that data is to be latched or driven onto a byte of the data when driven low. The $\overline{BS}$[3:2] signals are asserted only to the memory bytes used during a read or write access. $\overline{BS3}$ controls access to the most significant byte lane of data, and $\overline{BS2}$ controls access to the least significant byte lane of data. The $\overline{BS}$[3:2] signals are asserted during accesses to on-chip peripherals but not to on-chip SRAM, or cache. During SDRAM accesses, these signals act as the $\overline{CAS}$[3:2] signals, which indicate a byte transfers between SDRAM and the chip when driven high. For SRAM or Flash devices, the $\overline{BS}$[3:2] outputs should be connected to individual byte strobe signals. For SDRAM devices, the $\overline{BS}$[3:2] should be connected to individual SDRAM DQM signals. Note that most SDRAMs associate DQM1 with the MSB, in which case $\overline{BS3}$ should be connected to the SDRAM's DQM1 input.	O
Output Enable	$\overline{OE}$	Indicates when an external device can drive data during external read cycles.	O
Transfer Acknowledge	$\overline{TA}$	Indicates that the external data transfer is complete. During a read cycle, when the processor recognizes $\overline{TA}$, it latches the data and then terminates the bus cycle. During a write cycle, when the processor recognizes $\overline{TA}$, the bus cycle is terminated.	I
Transfer Error Acknowledge	$\overline{TEA}$	Indicates an error condition exists for the bus transfer. The bus cycle is terminated and the CPU begins execution of the access error exception.	I
Read/Write	R/$\overline{W}$	Indicates the direction of the data transfer on the bus for SRAM (R/$\overline{W}$) and SDRAM ($\overline{SD\_WE}$) accesses. A logic 1 indicates a read from a slave device and a logic 0 indicates a write to a slave device	O
Transfer Size	$\overline{TSIZ}$[1:0]	When the device is in normal mode, dynamic bus sizing lets the programmer change data bus width between 8, 16, and 32 bits for each chip select. The initial width for the bootstrap program chip select, CS0, is determined by the state of $\overline{TSIZ}$[1:0]. The program should select bus widths for the other chip selects before accessing the associated memory space. These pins our output pins.	O
Transfer Start	$\overline{TS}$	Bus control output signal indicating the start of a transfer.	O
Transfer in Progress	$\overline{TIP}$	Bus control output signal indicating bus transfer in progress.	O
Chip Selects	$\overline{CS}$[7:0]	These output signals select external devices for external bus transactions. The $\overline{CS}$[3:2] can also be configured to function as SDRAM chip selects $\overline{SD\_CS}$[1:0].	O

4.5 DDR SDRAM Controller Signals

Table 7 describes signals that are used for DDR SDRAM accesses.

Table 7. SDRAM Controller Signals

Signal Name	Abbreviation	Function	I/O
SDRAM Clock Out	DDR_CLKOUT	This output signal reflects the internal system clock.	O
SDRAM Inverted Clock Out	$\overline{\text{DDR\_CLKOUT}}$	This output signal reflects the inverted internal system clock.	O
SDRAM Synchronous Row Address Strobe	$\overline{\text{SD\_SRAS}}$	SDRAM synchronous row address strobe.	O
SDRAM Synchronous Column Address Strobe	$\overline{\text{SD\_SCAS}}$	SDRAM synchronous column address strobe.	O
SDRAM Write Enable	$\overline{\text{SD\_WE}}$	SDRAM write enable.	O
SDRAM A10	SD_A10	SDRAM address bit 10 or command.	O
SDRAM Chip Selects	$\overline{\text{SD\_CS}}$[1:0]	SDRAM chip select signals.	O
SDRAM Clock Enable	$\overline{\text{SD\_CKE}}$	SDRAM clock enable.	O
SDRAM Data Strobes	$\overline{\text{SD\_DQS}}$[3:2]	SDRAM byte-lane read/write data strobe signals.	O

4.6 External Interrupt Signals

Table 8 describes the external interrupt signals.

Table 8. External Interrupt Signals

Signal Name	Abbreviation	Function	I/O
External Interrupts	$\overline{\text{IRQ}}$[7:1]	External interrupt sources. $\overline{\text{IRQ}}$[3:2] can also be configured as DMA request signals $\overline{\text{DREQ}}$[3:2]. $\overline{\text{IRQ4}}$ can also be configured as DMA request signals $\overline{\text{DREQ2}}$.	I

4.7 Fast Ethernet Controller Signals

The following signals are used by the Ethernet modules for data and clock signals.

Table 9. Ethernet Module (FEC) Signals

Signal Name	Abbreviation	Function	I/O
Management Data	FEC*n*_MDIO	Transfers control information between the external PHY and the media-access controller. Data is synchronous to FEC*n*_MDC. Applies to MII mode operation. This signal is an input after reset. When the FEC is operated in 10Mbps 7-wire interface mode, this signal should be connected to VSS.	I/O
Management Data Clock	FEC*n*_MDC	In Ethernet mode, FEC*n*_MDC is an output clock which provides a timing reference to the PHY for data transfers on the FEC*n*_MDIO signal. Applies to MII mode operation.	O
Transmit Clock	FEC*n*_TXCLK	Input clock which provides a timing reference for FEC*n*_TXEN, FEC*n*_TXD[3:0] and FEC*n*_TXER	I

Table 9. Ethernet Module (FEC) Signals (continued)

Signal Name	Abbreviation	Function	I/O
Transmit Enable	FEC*n*_TXEN	Indicates when valid nibbles are present on the MII. This signal is asserted with the first nibble of a preamble and is negated before the first FEC*n*_TXCLK following the final nibble of the frame.	O
Transmit Data 0	FEC*n*_TXD0	FEC*n*_TXD0 is the serial output Ethernet data and is only valid during the assertion of FEC*n*_TXEN. This signal is used for 10-Mbps Ethernet data. It is also used for MII mode data in conjunction with FEC*n*_TXD[3:1].	O
Collision	FEC*n*_COL	Asserted upon detection of a collision and remains asserted while the collision persists. This signal is not defined for full-duplex mode.	I
Receive Clock	FEC*n*_RXCLK	Provides a timing reference for FEC*n*_RXDV, FEC*n*_RXD[3:0], and FEC*n*_RXER.	I
Receive Data Valid	FEC*n*_RXDV	Asserting the receive data valid (FEC*n*_RXDV) input indicates that the PHY has valid nibbles present on the MII. FEC*n*_RXDV should remain asserted from the first recovered nibble of the frame through to the last nibble. Assertion of FEC*n*_RXDV must start no later than the SFD and exclude any EOF.	I
Receive Data 0	FEC*n*_RXD0	FEC*n*_RXD0 is the Ethernet input data transferred from the PHY to the media-access controller when FEC*n*_RxDV is asserted. This signal is used for 10-Mbps Ethernet data. This signal is also used for MII mode Ethernet data in conjunction with FEC*n*_RXD[3:1].	I
Carrier Receive Sense	FEC*n*_CRS	When asserted, indicates that transmit or receive medium is not idle. Applies to MII mode operation.	I
Transmit Data 1–3	FEC*n*_TXD[3:1]	In Ethernet mode, these pins contain the serial output Ethernet data and are valid only during assertion of FEC*n*_TXEN in MII mode.	O
Transmit Error	FEC*n*_TXER	In Ethernet mode, when FEC*n*_TXER is asserted for one or more clock cycles while FEC*n*_TXEN is also asserted, the PHY sends one or more illegal symbols. FEC*n*_TXER has no effect at 10 Mbps or when FEC*n*_TXEN is negated. Applies to MII mode operation.	O
Receive Data 1–3	FEC*n*_RXD[3:1]	In Ethernet mode, these pins contain the Ethernet input data transferred from the PHY to the Media Access Controller when FEC*n*_RXDV is asserted in MII mode operation.	I
Receive Error	FEC*n*_RXER	In Ethernet mode, FEC*n*_RXER—when asserted with FEC*n*_RXDV—indicates that the PHY has detected an error in the current frame. When FEC*n*_RXDV is not asserted FEC*n*_RXER has no effect. Applies to MII mode operation.	O

4.8 Queued Serial Peripheral Interface (QSPI)

Table 10 describes QSPI signals.

Table 10. Queued Serial Peripheral Interface (QSPI) Signals

Signal Name	Abbreviation	Function	I/O
QSPI Syncrhonous Serial Output	QSPI_DOUT	Provides the serial data from the QSPI and can be programmed to be driven on the rising or falling edge of QSPI_CLK. Each byte is sent msb first.	O
QSPI Synchronous Serial Data Input	QSPI_DIN	Provides the serial data to the QSPI and can be programmed to be sampled on the rising or falling edge of QSPI_CLK. Each byte is written to RAM lsb first.	I
QSPI Serial Clock	QSPI_CLK	Provides the serial clock from the QSPI. The polarity and phase of QSPI_CLK are programmable. The output frequency is programmed according to the following formula, in which *n* can be any value between 1 and 255: $SPI\_CLK = f_{sys}/2 \div n$	O
Synchronous Peripheral Chip Selects	QSPI_CS[1:0]	Provide QSPI peripheral chip selects that can be programmed to be active high or low. QSPI_CS1 can also be configured as SDRAM clock enable signal SD_CKE.	O

4.9 I^2C I/O SIGNALS

Table 11 describes the I^2C serial interface module signals.

Table 11. I^2C I/O Signals

Signal Name	Abbreviation	Function	I/O
Serial Clock	I2C_SCL	Open-drain clock signal for the for the I^2C interface. Either it is driven by the I^2C module when the bus is in the master mode or it becomes the clock input when the I^2C is in the slave mode.	I/O
Serial Data	I2C_SDA	Open-drain signal that serves as the data input/output for the I^2C interface.	I/O

4.10 UART Module Signals

The UART modules use the signals in this section for data. The baud rate clock inputs are not supported.

Table 12. UART Module Signals

Signal Name	Abbreviation	Function	I/O
Transmit Serial Data Output	U*n*TXD	Transmitter serial data outputs for the UART modules. The output is held high (mark condition) when the transmitter is disabled, idle, or in the local loopback mode. Data is shifted out, lsb first, on this pin at the falling edge of the serial clock source.	O
Receive Serial Data Input	U*n*RXD	Receiver serial data inputs for the UART modules. Data received on this pin is sampled on the rising edge of the serial clock source lsb first. When the UART clock is stopped for power-down mode, any transition on this pin restarts it.	I

Table 12. UART Module Signals (continued)

Signal Name	Abbreviation	Function	I/O
Clear-to-Send	U*n*$\overline{\text{CTS}}$	Indicate to the UART modules that they can begin data transmission.	I
Request-to-Send	U*n*$\overline{\text{RTS}}$	Automatic request-to-send outputs from the UART modules. U*n*$\overline{\text{RTS}}$ can also be configured to be asserted and negated as a function of the RxFIFO level.	O

4.11 USB Signals

Table 13 describes the USB serial interface module signals.

Table 13. USB Module Signals

Signal Name	Abbreviation	Function	I/O
USB Clock	USB_CLK	This 48MHz (or 6MHz) clock is used by the USB module for both clock recovery and generation of a 12Mhz (or 1.5MHz) internal bit clock.	I
USB Speed	USB_SPEED	Applications which make use of low speed USB signalling must be able to switch the USB transceiver between low speed and full speed operations. Software has control of this function by driving the state of the USB_SPD bit in the USB_CTRL register onto the USB_SPEED pin.	I/O
USB Received D-	USB_RN	This signal is one half of the differential USB signal, and is extracted from the USB cable via a single ended input buffer on the analog front end. This signal is used by the module for detecting the single ended 0 (SE0) USB bus state.	I
USB Received D+	USB_RP	This signal is one half of the differential USB signal, and is extracted from the USB cable via a single ended input buffer on the analog front end. This signal is used by the module for detecting the single ended 0 (SE0) USB bus state.	I
USB Receive Data	USB_RXD	Input data from the differential input receiver. USB_RXD is the single-ended data extracted from the USB_RP and USB_RN signals via a differential input buffer.	I
USB Suspended	USB_SUSP	After a long period of inactivity (3.0ms minimum), the USB will enter suspend mode, indicated on the interface by an active state on USB_SUSP. During this mode, the device is supposed to enter a low power state while waiting for a wake-up from the USB Host. When the device enters suspend mode, it asserts the suspend signal which forces the analog front end into a low power state. When the device leaves suspend mode, USB_SUSP is deasserted, enabling the analog front end for normal USB operations.	O
USB Transmitted D-	USB_TN	This signal is one half of the differential NRZI formatted output from the USB module. It is fed to the transmitted D- input of the analog front end.	O

Table 13. USB Module Signals (continued)

Signal Name	Abbreviation	Function	I/O
USB Transmitted D+	USB_TP	This signal is one half of the differential NRZI formatted output from the module. It is fed to the transmitted D+ input of the analog front end.	O
USB Transmit Enable	USB_TXEN	This signal is an active low output enable for the differential drivers on the analog front end. When this signal is active, the differential drivers will drive the USB. When this signal is inactive, the differential drivers will tristate their outputs.	O

4.12 DMA Timer Signals

Table 14 describes the signals of the four DMA timer modules.

Table 14. DMA Timer Signals

Signal Name	Abbreviation	Function	I/O
DMA Timer 0 Input	DT0IN	Can be programmed to cause events to occur in first platform timer. It can either clock the event counter or provide a trigger to the timer value capture logic.	I
DMA Timer 0 Output	DT0OUT	The output from first platform timer.	O
DMA Timer 1 Input	DT1IN	Can be programmed to cause events to occur in the second platform timer. This can either clock the event counter or provide a trigger to the timer value capture logic.	I
DMA Timer 1 Output	DT1OUT	The output from the second platform timer.	O
DMA Timer 2 Input	DT2IN	Can be programmed to cause events to occur in the third platform timer. It can either clock the event counter or provide a trigger to the timer value capture logic.	I
DMA Timer 2 Output	DT2OUT	The output from the third platform timer.	I
DMA Timer 3 Input	DT3IN	Can be programmed as an input that causes events to occur in the fourth platform timer. This can either clock the event counter or provide a trigger to the timer value capture logic.	I
DMA Timer 3 Output	DT3OUT	The output from the fourth platform timer.	O

4.13 Pulse Width Modulator Signals

Table 15 describes the PWM signals. Note that the primary functions of these pins are DMA Timer outputs (DT*n*OUT).

Table 15. PWM Signals

Signal Name	Abbreviation	Function	I/O
PWM Output Channel 0	PWM0	Pulse width modulated output for PWM channel 0.	O
PWM Output Channel 1	PWM1	Pulse width modulated output for PWM channel 1.	O
PWM Output Channel 2	PWM2	Pulse width modulated output for PWM channel 2.	O
PWM Output Channel 3	PWM3	Pulse width modulated output for PWM channel 3.	O

4.14 Debug Support Signals

These signals are used as the interface to the on-chip JTAG controller and also to interface to the BDM logic.

Table 16. Debug Support Signals

Signal Name	Abbreviation	Function	I/O
Test Reset	$\overline{\text{TRST}}$	This active-low signal is used to initialize the JTAG logic asynchronously.	I
Test Clock	TCLK	Used to synchronize the JTAG logic.	I
Test Mode Select	TMS	Used to sequence the JTAG state machine. TMS is sampled on the rising edge of TCLK.	I
Test Data Input	TDI	Serial input for test instructions and data. TDI is sampled on the rising edge of TCLK.	I
Test Data Output	TDO	Serial output for test instructions and data. TDO is three-stateable and is actively driven in the shift-IR and shift-DR controller states. TDO changes on the falling edge of TCLK.	O
Development Serial Clock	DSCLK	Clocks the serial communication port to the BDM module during packet transfers.	I
Breakpoint	$\overline{\text{BKPT}}$	Used to request a manual breakpoint.	I
Development Serial Input	DSI	This internally-synchronized signal provides data input for the serial communication port to the BDM module.	I
Development Serial Output	DSO	This internally-registered signal provides serial output communication for BDM module responses.	O
Debug Data	DDATA[3:0]	Display captured processor data and breakpoint status. The CLKOUT signal can be used by the development system to know when to sample DDATA[3:0].	O
Processor Status Outputs	PST[3:0]	Indicate core status, as shown in Table 17. Debug mode timing is synchronous with the processor clock; status is unrelated to the current bus transfer. The CLKOUT signal can be used by the development system to know when to sample PST[3:0].	O

Table 17. Processor Status

PST[3:0]	Processor Status
0000	Continue execution
0001	Begin execution of one instruction
0010	Reserved
0011	Entry into user mode
0100	Begin execution of PULSE and WDDATA instructions
0101	Begin execution of taken branch
0110	Reserved
0111	Begin execution of RTE instruction
1000	Begin one-byte transfer on DDATA
1001	Begin two-byte transfer on DDATA
1010	Begin three-byte transfer on DDATA
1011	Begin four-byte transfer on DDATA
1100	Exception processing
1101	Reserved
1110	Processor is stopped
1111	Processor is halted

4.15 Test Signals

Table 18 describes test signals.

Table 18. Test Signals

Signal Name	Abbreviation	Function	I/O
Test	TEST	Reserved for factory testing only and in normal modes of operation should be connected to VSS to prevent unintentional activation of test functions.	I
PLL Test	PLL_TEST	Reserved for factory testing only and should be treated as a no-connect (NC).	I

4.16 Power and Ground Pins

The pins described in Table 19 provide system power and ground to the chip. Multiple pins are provided for adequate current capability. All power supply pins must have adequate bypass capacitance for high-frequency noise suppression.

Table 19. Power and Ground Pins

Signal Name	Abbreviation	Function	I/O
PLL Analog Supply	VDDPLL, VSSPLL	Dedicated power supply signals to isolate the sensitive PLL analog circuitry from the normal levels of noise present on the digital power supply.	I
Positive Supply	VDDO	These pins supply positive power to the I/O pads.	I
Positive Supply	VDD	These pins supply positive power to the core logic.	I
Ground	VSS	This pin is the negative supply (ground) to the chip.	

5 Chip Configuration

5.1 Device Operating Options

- Chip operating mode:
  - Master mode
- Boot device/size:
  - External device boot
    - 32-bit
    - 16-bit (Default)
    - 8-bit
- Output pad strength:
  - Partial drive strength (Default)
  - Full drive strength
- Clock mode:
  - Normal PLL with external crystal
  - Normal PLL with external clock
  - 1:1 PLL Mode
  - External oscillator mode (no PLL)
- Chip Select Configuration:
  - PADDR[7:5] configured as chip select(s) and/or address line(s)
    - PADDR[7:5] configured as A23-A21 (default)
    - PADDR configured as $\overline{\text{CS6}}$, PADDR[6:5] as A22-A21
    - PADDR[7:6] configured as $\overline{\text{CS}}$[6:5], PADDR5 as A21
    - PADDR[7:5] configured as $\overline{\text{CS}}$[6:4]

5.2 Chip Configuration Pins

Table 20. Configuration Pin Descriptions

Pin	Chip Configuration Function	Pin State/Meaning	Comments
$\overline{\text{RCON}}$	Chip configuration enable	1 disabled 0 enabled	Active low: if asserted, then all configuration pins must be driven appropriately for desired operation
D26, D17, D16	Select chip operating mode	111 master 110 reserved 101 reserved 100 reserved 0xx reserved	
D19, D18	Select external boot device data port size	00,11 external (32-bit) 10 external (8-bit) 01 external (16-bit)	Value read defaults to 32-bit
D21	Select output pad drive strength	1 Full 0 Partial	
CLKMOD1, CLKMOD0	Select clock mode	00 External clock mode (no PLL) 01 1:1 PLL mode 10 Normal PLL with external clock reference 11 Normal PLL with crystal clock reference	VDDPLL must be supplied if a PLL mode is selected
D25, D24	Select chip select / address line	00 PADDR[7:5] configured as A23-A21 (default) 10 PADDR7 configured as $\overline{\text{CS6}}$, PADDR[6:5] as A22-A21 01 PADDR[7:6] configured as $\overline{\text{CS}}$[6:5], PADDR5 as A21 11 PADDR[7:5] configured as $\overline{\text{CS}}$[6:4]	
JTAG_EN	Selects BDM or JTAG mode	0 BDM mode 1 JTAG mode	

5.3 Chip Configuration Circuit

Figure 2 shows a block diagram of the recommended circuit used to drive the reset configuration values for the MCF5275.

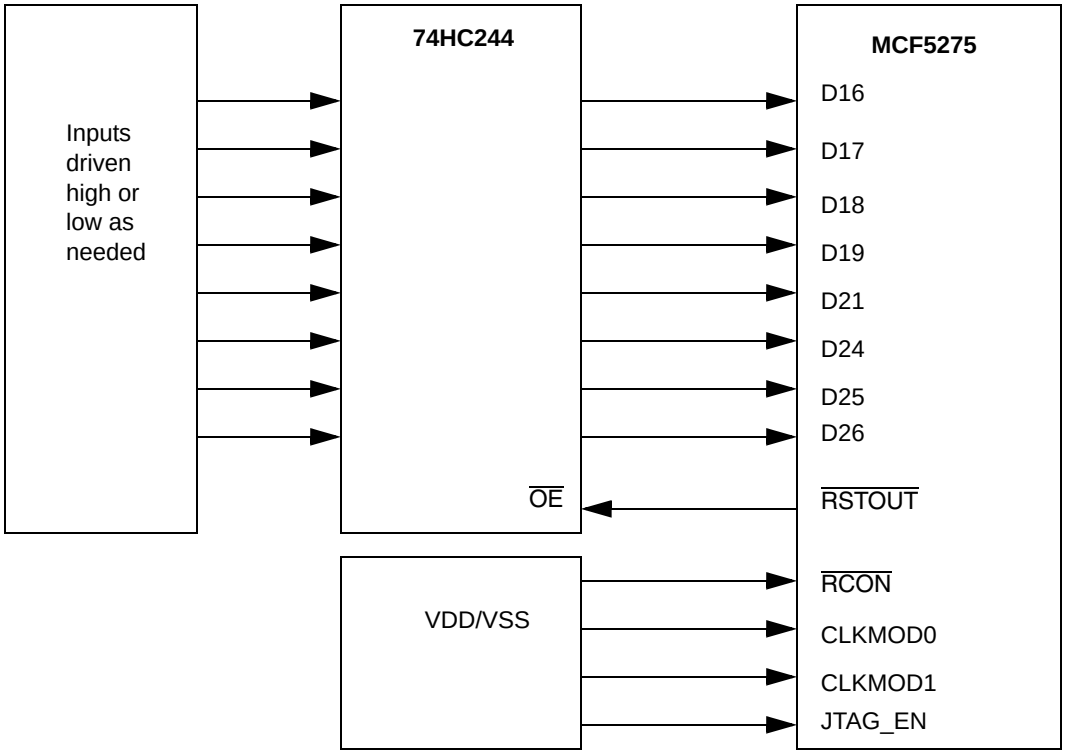


Figure 2. MCF5275 Recommended Reset Configuration Circuit

6 Design Recommendations

6.1 Layout

- Use a 4-layer printed circuit board with the VDD and GND pins connected directly to the power and ground planes for the MCF5275.
- See application note AN1259 System Design and Layout Techniques for Noise Reduction in MCU-Based Systems.
- Match the PC layout trace width and routing to match trace length to operating frequency and board impedance. Add termination (series or therein) to the traces to dampen reflections. Increase the PCB impedance (if possible) keeping the trace lengths balanced and short. Then do cross-talk analysis to separate traces with significant parallelism or are otherwise "noisy". Use 6 mils trace and separation. Clocks get extra separation and more precise balancing.

6.2 Power Supply

- 33uF, 0.1uF and 0.01uF across each power supply

6.3 Decoupling

- Place the decoupling capacitors as close to the pins as possible, but they can be outside the footprint of the package.
- 0.1uF and 0.01uF at each supply input

6.4 Buffering

- Use bus buffers on all data/address lines for all off-board accesses and for all on-board accesses when excessive loading is expected. See electricals.

6.5 Pull-up Recommendations

- Use external pull-up resistors on unused inputs. See pin table.

6.6 Clocking Recommendations

- Use a multi-layer board with a separate ground plane.
- Place the crystal and all other associated components as close to the EXTAL and XTAL (oscillator pins) as possible.
- Do not run a high frequency trace around crystal circuit.
- Ensure that the ground for the bypass capacitors is connected to a solid ground trace.
- Tie the ground trace to the ground pin nearest EXTAL and XTAL. This prevents large loop currents in the vicinity of the crystal.
- Tie the ground pin to the most solid ground in the system.
- Do not connect the trace that connects the oscillator and the ground plane to any other circuit element. This tends to make the oscillator unstable.
- Tie XTAL to ground when an external oscillator is clocking the device.

6.7 Interface Recommendations

6.7.1 DDR SDRAM Controller

6.7.1.1 SDRAM Controller Signals in Synchronous Mode

Table 21 shows the behavior of SDRAM signals in synchronous mode.

Table 21. Synchronous DRAM Signal Connections

Signal	Description
$\overline{\text{SD\_SRAS}}$	Synchronous row address strobe. Indicates a valid SDRAM row address is present and can be latched by the SDRAM. $\overline{\text{SD\_SRAS}}$ should be connected to the corresponding SDRAM $\overline{\text{SD\_SRAS}}$. Do not confuse $\overline{\text{SD\_SRAS}}$ with the DRAM controller's $\overline{\text{SDRAM\_CS}}$[1:0], which should not be interfaced to the SDRAM $\overline{\text{SD\_SRAS}}$ signals.
$\overline{\text{SD\_SCAS}}$	Synchronous column address strobe. Indicates a valid column address is present and can be latched by the SDRAM. $\overline{\text{SD\_SCAS}}$ should be connected to the corresponding signal labeled $\overline{\text{SD\_SCAS}}$ on the SDRAM.
$\overline{\text{SD\_WE}}$	DRAM read/write. Asserted for write operations and negated for read operations.
$\overline{\text{SD\_CS}}$[1:0]	Row address strobe. Select each memory block of SDRAMs connected to the MCF5275. One $\overline{\text{SDRAM\_CS}}$ signal selects one SDRAM block and connects to the corresponding $\overline{\text{CS}}$ signals.
SD_CKE	Synchronous DRAM clock enable. Connected directly to the CKE (clock enable) signal of SDRAMs. Enables and disables the clock internal to SDRAM. When CKE is low, memory can enter a power-down mode where operations are suspended or they can enter self-refresh mode. SD_CKE functionality is controlled by DCR[COC]. For designs using external multiplexing, setting COC allows SD_CKE to provide command-bit functionality.
$\overline{\text{BS}}$[3:2]	Column address strobe. For synchronous operation, $\overline{\text{BS}}$[3:2] function as byte enables to the SDRAMs. They connect to the DQM signals (or mask qualifiers) of the SDRAMs.
DDR_CLKOUT	Bus clock output. Connects to the CLK input of SDRAMs.

6.7.1.2 Address Multiplexing

Table 22 shows the generic address multiplexing scheme for SDRAM configurations. All possible address connection configurations can be derived from this table.

Table 22. Generic Address Multiplexing Scheme

Address Pin	Row Address	Column Address	Notes Related to Port Sizes
17	17	0	8-bit port only
16	16	1	8- and 16-bit ports only
15	15	2	
14	14	3	
13	13	4	
12	12	5	
11	11	6	
10	10	7	
9	9	8	
17	17	16	32-bit port only
18	18	17	16-bit port only or 32-bit port with only 8 column address lines
19	19	18	16-bit port only when at least 9 column address lines are used
20	20	19	
21	21	20	

Table 22. Generic Address Multiplexing Scheme (continued)

Address Pin	Row Address	Column Address	Notes Related to Port Sizes
22	22	21	
23	23	22	
24	24	23	
25	25	24	

The following tables provide a more comprehensive, step-by-step way to determine the correct address line connections for interfacing the MCF5275 to SDRAM. To use the tables, find the one that corresponds to the number of column address lines on the SDRAM and to the port size as seen by the MCF5275, which is not necessarily the SDRAM port size. For example, if two 8M x 8-bit SDRAMs together form a 8M x 16-bit memory, the port size is 16 bits. Most SDRAMs likely have fewer address lines than are shown in the tables, so follow only the connections shown until all SDRAM address lines are connected.

Table 23. MCF5275 to SDRAM Interface (8-Bit Port, 9-Column Address Lines)

MCF5275 Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	17	16	15	14	13	12	11	10	9	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Column	0	1	2	3	4	5	6	7	8														
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22

Table 24. MCF5275 to SDRAM Interface (8-Bit Port,10-Column Address Lines)

MCF5275 Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	17	16	15	14	13	12	11	10	9	19	20	21	22	23	24	25	26	27	28	29	30	31
Column	0	1	2	3	4	5	6	7	8	18												
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21

Table 25. MCF5275 to SDRAM Interface (8-Bit Port,11-Column Address Lines)

MCF5275 Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A19	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	17	16	15	14	13	12	11	10	9	19	21	22	23	24	25	26	27	28	29	30	31
Column	0	1	2	3	4	5	6	7	8	18	20										
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20

Table 26. MCF5275 to SDRAM Interface (8-Bit Port,12-Column Address Lines)

MCF5275 Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A19	A21	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	17	16	15	14	13	12	11	10	9	19	21	23	24	25	26	27	28	29	30	31
Column	0	1	2	3	4	5	6	7	8	18	20	22								
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19

Table 27. MCF5275 to SDRAM Interface (8-Bit Port,13-Column Address Lines)

MCF5275 Pins	A17	A16	A15	A14	A13	A12	A11	A10	A9	A19	A21	A23	A25	A26	A27	A28	A29	A30	A31
Row	17	16	15	14	13	12	11	10	9	19	21	23	25	26	27	28	29	30	31
Column	0	1	2	3	4	5	6	7	8	18	20	22	24						
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18

Table 28. MCF5275 to SDRAM Interface (16-Bit Port, 8-Column Address Lines)

MCF5275 Pins	A16	A15	A14	A13	A12	A11	A10	A9	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	16	15	14	13	12	11	10	9	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Column	1	2	3	4	5	6	7	8															
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21	A22

Table 29. MCF5275 to SDRAM Interface (16-Bit Port, 9-Column Address Lines)

MCF5275 Pins	A16	A15	A14	A13	A12	A11	A10	A9	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	16	15	14	13	12	11	10	9	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Column	1	2	3	4	5	6	7	8	17													
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21

Table 30. MCF5275 to SDRAM Interface (16-Bit Port, 10-Column Address Lines)

MCF5275 Pins	A16	A15	A14	A13	A12	A11	A10	A9	A18	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	16	15	14	13	12	11	10	9	18	20	21	22	23	24	25	26	27	28	29	30	31
Column	1	2	3	4	5	6	7	8	17	19											
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20

Table 31. MCF5275 to SDRAM Interface (16-Bit Port, 11-Column Address Lines)

MCF5275 Pins	A16	A15	A14	A13	A12	A11	A10	A9	A18	A20	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	16	15	14	13	12	11	10	9	18	20	22	23	24	25	26	27	28	29	30	31
Column	1	2	3	4	5	6	7	8	17	19	21									
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19

Table 32. MCF5275 to SDRAM Interface (16-Bit Port, 12-Column Address Lines)

MCF5275 Pins	A16	A15	A14	A13	A12	A11	A10	A9	A18	A20	A22	A24	A25	A26	A27	A28	A29	A30	A31
Row	16	15	14	13	12	11	10	9	18	20	22	24	25	26	27	28	29	30	31
Column	1	2	3	4	5	6	7	8	17	19	21	23							
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18

Table 33. MCF5275 to SDRAM Interface (16-Bit Port, 13-Column-Address Lines)

MCF5275 Pins	A16	A15	A14	A13	A12	A11	A10	A9	A18	A20	A22	A24	A26	A27	A28	A29	A30	A31
Row	16	15	14	13	12	11	10	9	18	20	22	24	26	27	28	29	30	31
Column	1	2	3	4	5	6	7	8	17	19	21	23	25					
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17

Table 34. MCF5275 to SDRAM Interface (32-Bit Port, 8-Column Address Lines)

MCF5275 Pins	A15	A14	A13	A12	A11	A10	A9	A17	A18	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	15	14	13	12	11	10	9	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
Column	2	3	4	5	6	7	8	16														
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20	A21

Table 35. MCF5275 to SDRAM Interface (32-Bit Port, 9-Column Address Lines)

MCF5275 Pins	A15	A14	A13	A12	A11	A10	A9	A17	A19	A20	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	15	14	13	12	11	10	9	17	19	20	21	22	23	24	25	26	27	28	29	30	31
Column	2	3	4	5	6	7	8	16	18												
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19	A20

Table 36. MCF5275 to SDRAM Interface (32-Bit Port, 10-Column Address Lines)

MCF5275 Pins	A15	A14	A13	A12	A11	A10	A9	A17	A19	A21	A22	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	15	14	13	12	11	10	9	17	19	21	22	23	24	25	26	27	28	29	30	31
Column	2	3	4	5	6	7	8	16	18	20										
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18	A19

Table 37. MCF5275 to SDRAM Interface (32-Bit Port, 11-Column Address Lines)

MCF5275 Pins	A15	A14	A13	A12	A11	A10	A9	A17	A19	A21	A23	A24	A25	A26	A27	A28	A29	A30	A31
Row	15	14	13	12	11	10	9	17	19	21	23	24	25	26	27	28	29	30	31
Column	2	3	4	5	6	7	8	16	18	20	22								
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17	A18

Table 38. MCF5275 to SDRAM Interface (32-Bit Port, 12-Column Address Lines)

MCF5275 Pins	A15	A14	A13	A12	A11	A10	A9	A17	A19	A21	A23	A25	A26	A27	A28	A29	A30	A31
Row	15	14	13	12	11	10	9	17	19	21	23	25	26	27	28	29	30	31
Column	2	3	4	5	6	7	8	16	18	20	22	24						
SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12	A13	A14	A15	A16	A17

6.7.1.2.1 SDRAM Interfacing Example

The tables in the previous section can be used to configure the interface in the following example. To interface one 2M x 32-bit x 4 bank SDRAM component (8 columns) to the MCF5275, the connections would be as shown in Table 39.

Table 39. SDRAM Hardware Connections

SDRAM Pins	A0	A1	A2	A3	A4	A5	A6	A7	A8	A9	A10 = CMD	BA0	BA1
MCF5275 Pins	A15	A14	A13	A12	A11	A10	A9	A17	A18	A19	A20	A21	A22

6.7.2 Ethernet PHY Transceiver Connection

The FEC supports both an MII interface for 10/100 Mbps Ethernet and a seven-wire serial interface for 10 Mbps Ethernet. The interface mode is selected by R_CNTRL[MII_MODE]. In MII mode, the 802.3 standard defines and the FEC module supports 18 signals. These are shown in Table 40.

Table 40. MII Mode

Signal Description	MCF5275 Pin
Transmit clock	FEC*n*_TXCLK
Transmit enable	FEC*n*_TXEN
Transmit data	FEC*n*_TXD[3:0]
Transmit error	FEC*n*_TXER
Collision	FEC*n*_COL
Carrier sense	FEC*n*_CRS
Receive clock	FEC*n*_RXCLK
Receive enable	FEC*n*_RXDV
Receive data	FEC*n*_RXD[3:0]
Receive error	FEC*n*_RXER
Management channel clock	FEC*n*_MDC
Management channel serial data	FEC*n*_MDIO

The serial mode interface operates in what is generally referred to as AMD mode. The MCF5275 configuration for seven-wire serial mode connections to the external transceiver are shown in Table 41.

Table 41. Seven-Wire Mode Configuration

Signal Description	MCF5275 Pin
Transmit clock	FEC*n*_TXCLK
Transmit enable	FEC*n*_TXEN
Transmit data	FEC*n*_TXD[0]
Collision	FEC*n*_COL
Receive clock	FEC*n*_RXCLK
Receive enable	FEC*n*_RXDV
Receive data	FEC*n*_RXD[0]
Unused, configure as PB14	FEC*n*_RXER
Unused input, tie to ground	FEC*n*_CRS
Unused, configure as PB[13:11]	FEC*n*_RXD[3:1]
Unused output, ignore	FEC*n*_TXER
Unused, configure as PB[10:8]	FEC*n*_TXD[3:1]
Unused, configure as PB15	FEC*n*_MDC
Input after reset, connect to ground	FEC*n*_MDIO

Refer to the M5275EVBevaluation board user's manual for an example of how to connect an external PHY. Schematics for this board are accessible at the MCF5275 site by navigating from: http://e-www.motorola.com/ following the 32-bit Embedded Processors, 68K/ColdFire, MCF5xxx, MCF5275 and M5275EVB links.

6.7.3 BDM

Use the BDM interface as shown in the M5275EVB evaluation board user's manual. The schematics for this board are accessible at the MCF5275 site by navigating from: http://e-www.motorola.com/ following the 32-bit Embedded Processors, 68K/ColdFire, MCF5xxx, MCF5275 and M5275EVB links.

7 Pinout

7.1 256 MAPBGA Pinout

Figure 3 is a consolidated MCF5274/75 pinout for the 256 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	
A	VSS	FEC1_ RXD1	FEC1_ RXDV	FEC1_ CRS	FEC1_ COL	FEC0_ COL	FEC0_ MDIO	U0RXD	U1RXD	VSS	A23	A20	A17	A14	SD_ VREF	VSS	A
B	FEC1_ RXD3	FEC1_ RXD2	FEC1_ RXD0	FEC1_ RXCLK	FEC0_ RXDV	FEC0_ RXCLK	FEC0_ MDC	U0TXD	U1TXD	I2C_ SDA	A22	A19	A16	A13	A11	A9	B
C	FEC1_ TXCLK	FEC1_ RXER	FEC0_ TXCLK	FEC0_ RXER	FEC0_ RXD2	FEC0_ RXD0	FEC0_ CRS	$\overline{\text{U0CTS}}$	$\overline{\text{U1CTS}}$	I2C_ SCL	A21	A18	A15	A12	A10	A8	C
D	FEC1_ TXER	FEC1_ TXEN	FEC0_ TXER	FEC0_ TXEN	FEC0_ RXD3	FEC0_ RXD1	$\overline{\text{U0RTS}}$	VDD	$\overline{\text{U1RTS}}$	$\overline{\text{CS7}}$	$\overline{\text{CS6}}$	$\overline{\text{CS5}}$	$\overline{\text{CS4}}$	A7	A6	TSIZ1	D
E	FEC1_ TXD3	FEC1_ TXD2	FEC0_ TXD3	NC	VSS	OVDD	OVDD	OVDD	SD_VDD	SD_VDD	SD_VDD	VSS	$\overline{\text{CS3}}$	A5	A4	A3	E
F	FEC1_ TXD0	FEC1_ TXD1	FEC0_ TXD2	FEC0_ TXD1	OVDD	VSS	OVDD	OVDD	SD_VDD	SD_VDD	VSS	SD_VDD	$\overline{\text{CS2}}$	A2	A1	A0	F
G	FEC1_ MDIO	FEC1_ MDC	DT0OUT	FEC0_ TXD0	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	$\overline{\text{IRQ7}}$	USB_ SPEED	USB_ CLK	TSIZ0	G
H	DT1IN	DT1OUT	DT0IN	NC	OVDD	OVDD	VSS	VSS	VSS	VSS	SD_VDD	SD_VDD	VDD	$\overline{\text{IRQ4}}$	$\overline{\text{IRQ5}}$	$\overline{\text{IRQ6}}$	H
J	VSS	DT2IN	DT2OUT	DT3IN	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{\text{IRQ2}}$	$\overline{\text{IRQ3}}$	USB_RP	USB_RN	J
K	$\overline{\text{OE}}$	$\overline{\text{SD_WE}}$	DT3OUT	VDD	SD_VDD	SD_VDD	VSS	VSS	VSS	VSS	OVDD	OVDD	$\overline{\text{IRQ1}}$	USB_TN	USB_TP	VSSPLL	K
L	$\overline{\text{SD_ SCAS}}$	$\overline{\text{SD_ SRAS}}$	SD_CKE	$\overline{\text{TS}}$	SD_VDD	VSS	SD_VDD	SD_VDD	OVDD	OVDD	VSS	OVDD	$\overline{\text{TA}}$	USB_ TXEN	USB_ RXD	EXTAL	L
M	D31	$\overline{\text{SD_CS1}}$	$\overline{\text{BS3}}$	SD_DQS3	VSS	SD_VDD	SD_VDD	SD_VDD	OVDD	OVDD	OVDD	NC	USB_ SUSP	PLL_ TEST	VDDPLL	XTAL	M
N	D30	D29	D28	D20	D16	SD_A10	$\overline{\text{CS1}}$	VDD	TEST	DDATA2	DDATA0	QSPI_ CS2	CLK MOD1	$\overline{\text{RSTOUT}}$	$\overline{\text{RESET}}$	VSS	N
P	D27	D26	D23	D19	SD_DQS2	$\overline{\text{TIP}}$	R/$\overline{\text{W}}$	$\overline{\text{RCON}}$	$\overline{\text{U2CTS}}$	DDATA3	DDATA1	QSPI_ CS0	CLK MOD0	$\overline{\text{TRST}}$/ DSCLK	TDO/ DSO	TCLK/ PSTCLK	P
R	D25	D24	D22	D18	$\overline{\text{BS2}}$	$\overline{\text{CS0}}$	VSS	$\overline{\text{U2RTS}}$	U2TXD	PST2	PST0	QSPI_ DOUT	QSPI_ CS3	JTAG_ EN	$\overline{\text{TMS}}$/ $\overline{\text{BKPT}}$	TDI/DSI	R
T	VSS	SD_ VREF	D21	D17	$\overline{\text{SD_CS0}}$	$\overline{\text{DDR_CLK OUT}}$	DDR_CLK OUT	$\overline{\text{TEA}}$	U2RXD	PST3	PST1	CLKOUT	QSPI_ DIN	QSPI_ CS1	QSPI_ CLK	VSS	T
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	

Figure 3. MCF5274 and MCF5275 Pinout (256 MAPBGA)

7.2 196 MAPBGA Pinout

Figure 4 is a consolidated MCF5274L/75L pinout for the 196 MAPBGA package. Table 2 lists the signals by group and shows which signals are muxed and bonded on each of the device packages.

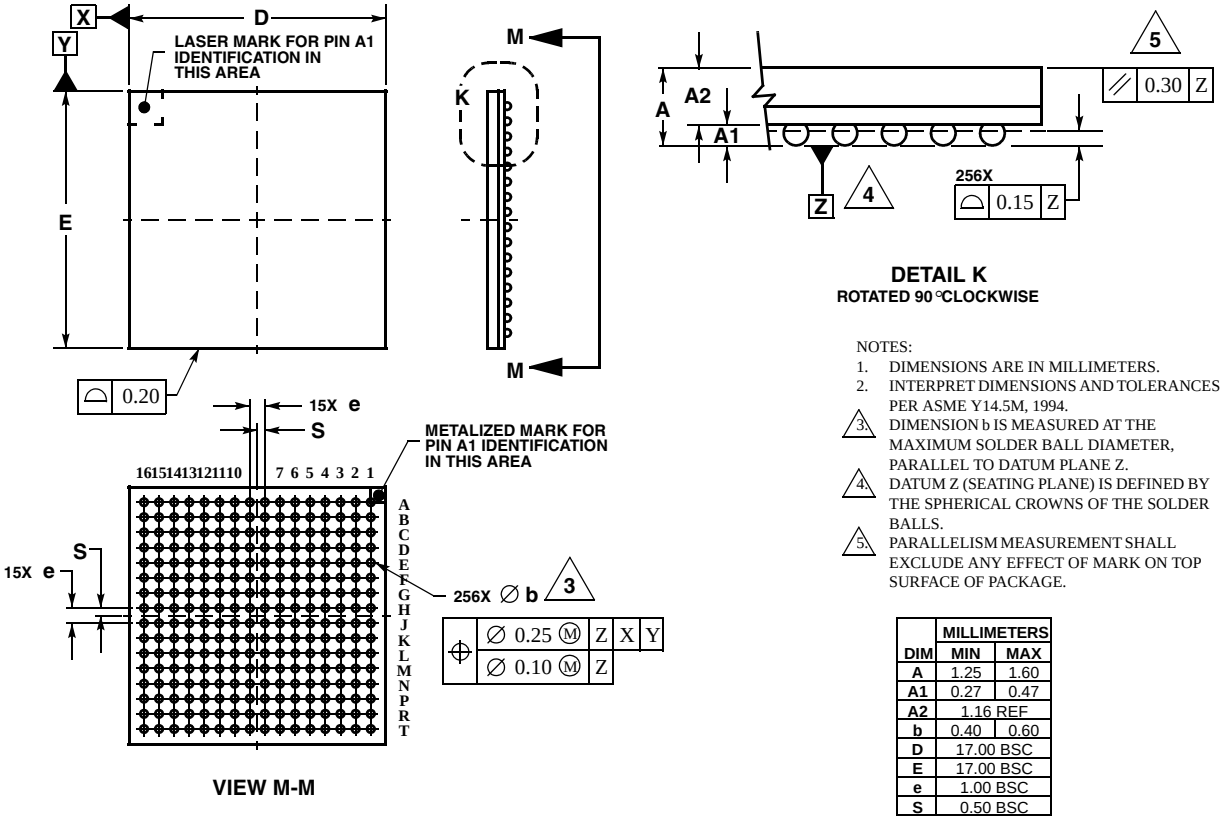
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	
A	NC	FEC0_ CRS	FEC0_ MDIO	U0RXD	U0TXD	U1RXD	I2C_SCL	A23	$\overline{CS6}$	$\overline{CS5}$	A15	A12	SD_ VREF	NC	A
B	FEC0_ RXD2	FEC0_ RXD1	FEC0_ RXCLK	FEC0_ COL	$\overline{U0RTS}$	$\overline{U1RTS}$	I2C_SDA	A22	A20	A16	A13	$\overline{CS3}$	A9	TSIZ1	B
C	FEC0_ TXCLK	FEC0_ TXER	FEC0_ TXEN	FEC0_ RXDV	FEC0_ MDC	$\overline{U0CTS}$	$\overline{U1CTS}$	A21	A18	A17	A14	A10	A8	$\overline{CS2}$	C
D	FEC0_ TXD3	FEC0_ TXD0	FEC0_ TXD1	FEC0_ RXD3	FEC0_ RXD0	VDD	U1TXD	$\overline{CS7}$	A19	$\overline{CS4}$	A11	A7	A5	A2	D
E	DT0IN	DT0OUT	FEC0_ TXD2	FEC0_ RXER	OVDD	OVDD	OVDD	SD_VDD2	SD_VDD2	SD_VDD2	A6	A4	A1	TSIZ0	E
F	DT1IN	DT1OUT	DT2IN	DT2OUT	OVDD	OVDD	VSS	VSS	SD_VDD2	SD_VDD2	A3	USB_CLK	A0	$\overline{IRQ7}$	F
G	DT3OUT	DT3IN	$\overline{SD\_CAS}$	$\overline{SD\_WE}$	VDD	VSS	VSS	VSS	VSS	SD_VDD2	USB_ SPEED	VDD	$\overline{IRQ6}$	$\overline{IRQ5}$	G
H	$\overline{SD\_SRAS}$	$\overline{TS}$	$\overline{SD\_CS1}$	$\overline{OE}$	SD_VDD1	VSS	VSS	VSS	VSS	OVDD	$\overline{IRQ4}$	$\overline{IRQ2}$	USB_RN	$\overline{IRQ3}$	H
J	SD_CKE	SD_DQS3	D31	D22	SD_VDD1	SD_VDD1	VSS	VSS	OVDD	OVDD	USB_RP	USB_TP	$\overline{IRQ1}$	USB_TN	J
K	$\overline{BS3}$	D29	D28	D23	SD_VDD1	SD_VDD1	SD_VDD1	OVDD	OVDD	OVDD	TDO/DSO	$\overline{RESET}$	USB_ TXEN	$\overline{TA}$	K
L	D30	D26	D25	D24	$\overline{BS2}$	R/$\overline{W}$	VDD	PST2	DDATA0	QSPI_ DOUT	QSPI_CLK	$\overline{RSTOUT}$	VSSPLL	USB_RXD	L
M	D27	D21	D18	D17	$\overline{SD\_CS0}$	$\overline{RCON}$	DDATA3	PST1	QSPI_ CS0	QSPI_DIN	CLKMOD1	TDI/DSI	VDDPLL	EXTAL	M
N	D20	D19	D16	SD_A10	$\overline{CS0}$	TEST	DDATA2	PST0	QSPI_ CS2	QSPI_ CS1	CLKMOD0	TMS/$\overline{BKPT}$	USB_ SUSP	XTAL	N
P	NC	SD_ VREF	SD_DQS2	$\overline{CS1}$	$\overline{DDR\_CLK\ OUT}$	DDR_CLK OUT	PST3	DDATA1	CLKOUT	QSPI_ CS3	JTAG_EN	TCLK/PST CLK	$\overline{TRST}$/DSC LK	NC	P
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	

Figure 4. MCF5274L and MCF5275L Pinout (196 MAPBGA)

8 Mechanicals

8.1 Package Dimensions - 256 MAPBGA

Figure 6 shows MCF5275 256 MAPBGA package dimensions.

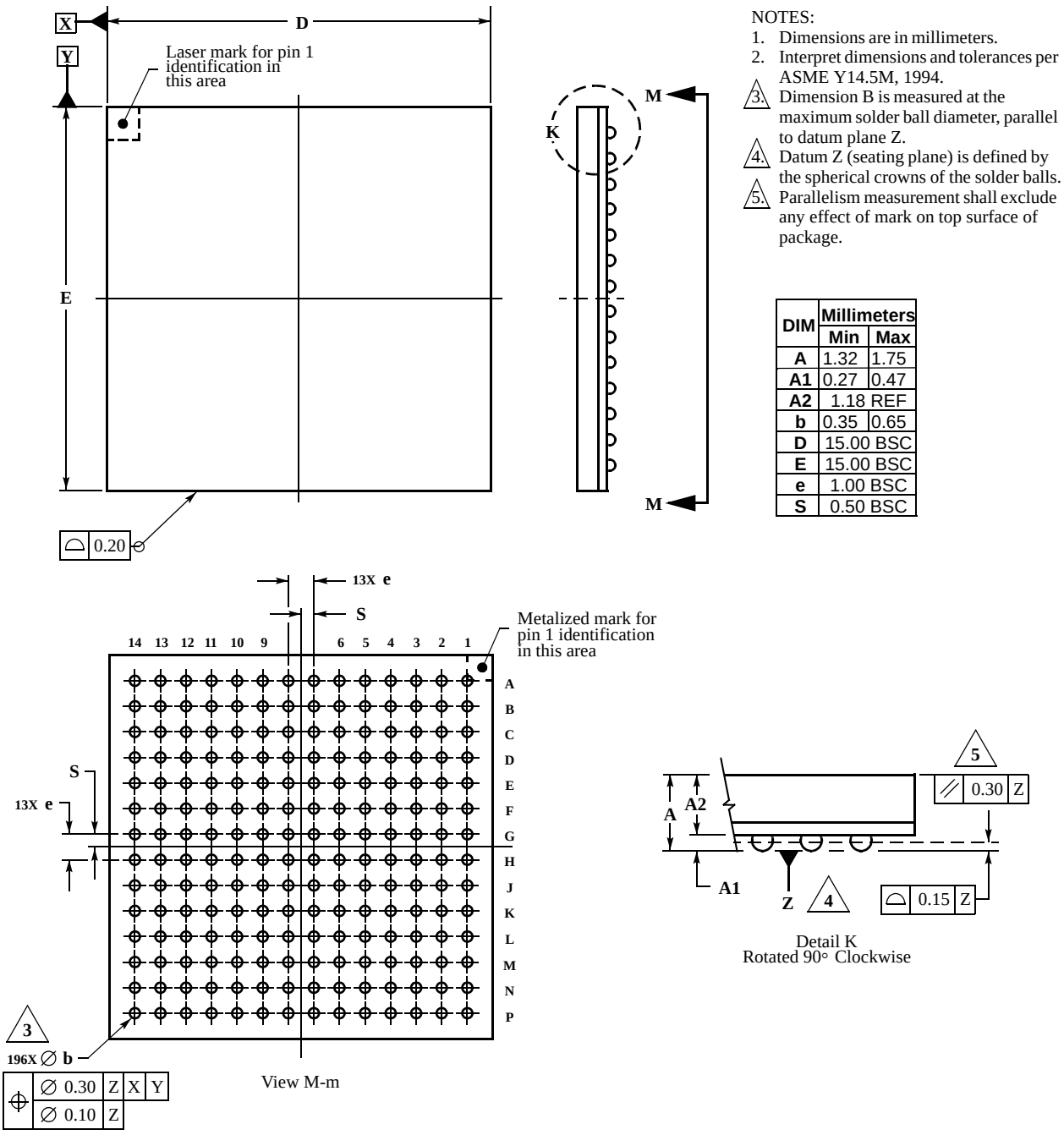


DIM	MILLIMETERS MIN	MAX
A	1.25	1.60
A1	0.27	0.47
A2	1.16 REF	
b	0.40	0.60
D	17.00 BSC	
E	17.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 5. 256 MAPBGA Package Dimensions

8.2 Package Dimensions - 196 MAPBGA

Figure 6 shows MCF5275 196 MAPBGA package dimensions.



NOTES:
1. Dimensions are in millimeters.
2. Interpret dimensions and tolerances per ASME Y14.5M, 1994.
3. Dimension B is measured at the maximum solder ball diameter, parallel to datum plane Z.
4. Datum Z (seating plane) is defined by the spherical crowns of the solder balls.
5. Parallelism measurement shall exclude any effect of mark on top surface of package.

DIM	Millimeters	
	Min	Max
A	1.32	1.75
A1	0.27	0.47
A2	1.18 REF	
b	0.35	0.65
D	15.00 BSC	
E	15.00 BSC	
e	1.00 BSC	
S	0.50 BSC	

Figure 6. 196 MAPBGA Package Dimensions

9 Ordering Information

Table 42. Orderable Part Numbers

Motorola Part Number	Description	Speed	Temperature
MCF5274LVM133	MCF5274L RISC Microprocessor, 196 MAPBGA	133MHz	0° to +70° C
MCF5274LVM166	MCF5274L RISC Microprocessor, 196 MAPBGA	166MHz	0° to +70° C
MCF5274VM133	MCF5274 RISC Microprocessor, 256 MAPBGA	133MHz	0° to +70° C
MCF5274VM166	MCF5274 RISC Microprocessor, 256 MAPBGA	166MHz	0° to +70° C
MCF5275LCVM133	MCF5275L RISC Microprocessor, 196 MAPBGA	133MHz	-40° to +85° C
MCF5275LCVM166	MCF5275L RISC Microprocessor, 196 MAPBGA	166MHz	-40° to +85° C
MCF5275CVM133	MCF5275 RISC Microprocessor, 256 MAPBGA	133MHz	-40° to +85° C
MCF5275CVM166	MCF5275 RISC Microprocessor, 256 MAPBGA	166MHz	-40° to +85° C

10 Preliminary Electrical Characteristics

This appendix contains electrical specification tables and reference timing diagrams for the MCF5275 microcontroller unit. This section contains detailed information on power considerations, DC/AC electrical characteristics, and AC timing specifications of MCF5275.

The electrical specifications are preliminary and are from previous designs or design simulations. These specifications may not be fully tested or guaranteed at this early stage of the product life cycle, however for production silicon these specifications will be met. Finalized specifications will be published after complete characterization and device qualifications have been completed.

NOTE

The parameters specified in this appendix supersede any values found in the module specifications.

10.1 Maximum Ratings

Table 43. Absolute Maximum Ratings[1, 2]

Rating	Symbol	Value	Unit
Core Supply Voltage	V_{DD}	– 0.5 to +2.0	V
I/O Pad Supply Voltage (3.3V)	O V_{DD}	– 0.3 to +4.0	V
Memory Interface SSTL 2.5V Pad Supply Voltage	SD V_{DD}	– 0.3 to + 2.8	V
Memory Interface SSTL 3.3V Pad Supply Voltage	SD V_{DD}	– 0.3 to +4.0	V
Clock Synthesizer Supply Voltage	V_{DDPLL}	– 0.3 to +4.0	V
Digital Input Voltage [3]	V_{IN}	– 0.3 to + 4.0	V
EXTAL pin voltage	V_{EXTAL}	0 to 3.3	V
XTAL pin voltage	V_{XTAL}	0 to 3.3	V

Table 43. Absolute Maximum Ratings[1, 2]

Instantaneous Maximum Current Single pin limit (applies to all pins) [4, 5]	I_D	25	mA
Operating Temperature Range (Packaged)	T_A (T_L - T_H)	– 40 to 85	°C
Storage Temperature Range	T_{stg}	– 65 to 150	°C

NOTES:
1. Functional operating conditions are given in DC Electrical Specifications. Absolute Maximum Ratings are stress ratings only, and functional operation at the maxima is not guaranteed. Stress beyond those listed may affect device reliability or cause permanent damage to the device.
2. This device contains circuitry protecting against damage due to high static voltage or electrical fields; however, it is advised that normal precautions be taken to avoid application of any voltages higher than maximum-rated voltages to this high-impedance circuit. Reliability of operation is enhanced if unused inputs are tied to an appropriate logic voltage level (e.g., either V_{SS} or O V_{DD}).
3. Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
4. All functional non-supply pins are internally clamped to V_{SS} and O V_{DD}.
5. Power supply must maintain regulation within operating O V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current (V_{in} > O V_{DD}) is greater than I_{DD}, the injection current may flow out of O V_{DD} and could result in external power supply going out of regulation. Insure external O V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power (ex; no clock).Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions.

10.2 Thermal Characteristics

Table 44 lists thermal resistance values

Table 44. Thermal characteristics

Characteristic		Symbol	Value	Unit
Junction to ambient, natural convection	256 MBGA Four layer board (2s2p)	θ_{JMA}	26[1,2]	°C/W
Junction to ambient (@200 ft/min)	256 MBGA Four layer board (2s2p)	θ_{JMA}	23	°C/W
Junction to board	256 MBGA	θ_{JB}	15[3]	°C/W
Junction to case	256 MBGA	θ_{JC}	10[4]	°C/W
Junction to top of package	Natural convection	Ψ_{jt}	2[5]	°C/W
Maximum operating junction temperature	256 MBGA	T_j	105	°C

NOTES:
1. θ_{JMA} and Ψ_{jt} parameters are simulated in conformance with EIA/JESD Standard 51-2 for natural convection. Motorola recommends the use of θ_{JmA} and power dissipation specifications in the system design to prevent device junction temperatures from exceeding the rated specification. System designers should be aware that device junction temperatures can be significantly influenced by board layout and surrounding devices. Conformance to the device junction temperature specification can be verified by physical measurement in the customer's system using the Ψ_{jt} parameter, the device power dissipation, and the method described in EIA/JESD Standard 51-2.
2. Per JEDEC JESD51-6 with the board horizontal.
3. Thermal resistance between the die and the printed circuit board in conformance with JEDEC JESD51-8. Board temperature is measured on the top surface of the board near the package.

4 Thermal resistance between the die and the case top surface as measured by the cold plate method (MIL SPEC-883 Method 1012.1).

5 Thermal characterization parameter indicating the temperature difference between package top and the junction temperature per JEDEC JESD51-2. When Greek letters are not available, the thermal characterization parameter is written in conformance with Psi-JT.

The average chip-junction temperature (T_J) in °C can be obtained from:

$$T_J = T_A + (P_D \times \Theta_{JMA}) \quad (1)$$

Where:

T_A = Ambient Temperature, °C

Θ_{JMA} = Package Thermal Resistance, Junction-to-Ambient, °C/W

P_D = $P_{INT} + P_{I/O}$

P_{INT} = $I_{DD} \times V_{DD}$, Watts - Chip Internal Power

$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications $P_{I/O} < P_{INT}$ and can be ignored. An approximate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273°C) \quad (2)$$

Solving equations 1 and 2 for K gives:

$$K = P_D \times (T_A + 273\ °C) + \Theta_{JMA} \times P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

10.3 ESD Protection

Table 45. ESD Protection Characteristics[1, 2]

Characteristics	Symbol	Value	Units
ESD Target for Human Body Model	HBM	2000	V
ESD Target for Machine Model	MM	200	V
HBM Circuit Description	R_{series}	1500	ohms
	C	100	pF
MM Circuit Description	R_{series}	0	ohms
	C	200	pF
Number of pulses per pin (HBM) positive pulses negative pulses	 — —	 1 1	—
Number of pulses per pin (MM) positive pulses negative pulses	 — —	 3 3	—
Interval of Pulses	—	1	sec

NOTES:

1 All ESD testing is in conformity with CDF-AEC-Q100 Stress Test Qualification for Automotive Grade Integrated Circuits.

[2] A device is defined as a failure if after exposure to ESD pulses the device no longer meets the device specification requirements. Complete DC parametric and functional testing is performed per applicable device specification at room temperature followed by hot temperature, unless specified otherwise in the device specification.

10.4 DC Electrical Specifications

Table 46. DC Electrical Specifications[1]

Characteristic	Symbol	Min	Max	Unit
Core Supply Voltage	V_{DD}	1.35	1.65	V
I/O Pad Supply Voltage	O V_{DD}	3.0	3.6	V
SSTL I/O Pad Supply Voltage	SD V_{DD}	2.3	2.7	V
Input High Voltage	V_{IH}	0.7 x O V_{DD}	3.6	V
Input Low Voltage	V_{IL}	V_{SS} – 0.3	0.35 x O V_{DD}	V
Input High Voltage SSTL 2.5V I/O Pads	V_{IH}	2.0	2.8	V
Input Low Voltage SSTL 2.5V I/O Pads	V_{IL}	– 0.5	0.8	V
Input High Voltage SSTL 3.3V I/O Pads	V_{IH}	2.0	3.6	V
Input Low Voltage SSTL 3.3V I/O Pads	V_{IL}	– 0.5	0.8	V
Input Hysteresis	V_{HYS}	0.06 x V_{DD}	—	mV
Input Leakage Current V_{in} = V_{DD} or V_{SS}, Input-only pins	I_{in}	–1.0	1.0	µA
High Impedance (Off-State) Leakage Current V_{in} = V_{DD} or V_{SS}, All input/output and output pins	I_{OZ}	–1.0	1.0	µA
Output High Voltage (All input/output and all output pins) I_{OH} = –2.0 mA	V_{OH}	O V_{DD} - 0.5	—	V
Output Low Voltage (All input/output and all output pins) I_{OL} = 2.0mA	V_{OL}	—	0.5	V
Weak Internal Pull Up Device Current, tested at V_{IL} Max.[2]	I_{APU}	-10	- 130	µA
Input Capacitance [3] All input-only pins All input/output (three-state) pins	C_{in}	 — —	 7 7	pF
Load Capacitance[4] Low Drive Strength High Drive Strength	C_L		 25 50	pF
Core Operating Supply Current [5] Master Mode WAIT DOZE STOP	I_{DD}	 — — — —	 175 15 10 100	 mA mA mA µA
I/O Pad Operating Supply Current Master Mode Low Power Modes	O I_{DD}	 — —	 250 250	 mA µA
DC Injection Current [3, 6, 7, 8] $V_{NEGCLAMP}$ =V_{SS}– 0.3 V, $V_{POSCLAMP}$ = V_{DD} + 0.3 Single Pin Limit Total MCU Limit, Includes sum of all stressed pins	I_{IC}	 -1.0 -10	 1.0 10	mA

NOTES:
1 Refer to Table 47 for additional PLL specifications.
2 Refer to the MCF5274 signals chapter for pins having weak internal pull-up devices.

3 This parameter is characterized before qualification rather than 100% tested.
4 pF load ratings are based on DC loading and are provided as an indication of driver strength. High speed interfaces require transmission line analysis to determine proper drive strength and termination.
5 Current measured at maximum system clock frequency, all modules active, and default drive strength with matching load.
6 All functional non-supply pins are internally clamped to V_{SS} and their respective V_{DD}.
7 Input must be current limited to the value specified. To determine the value of the required current-limiting resistor, calculate resistance values for positive and negative clamp voltages, then use the larger of the two values.
8 Power supply must maintain regulation within operating V_{DD} range during instantaneous and operating maximum current conditions. If positive injection current ($V_{in} > V_{DD}$) is greater than I_{DD}, the injection current may flow out of V_{DD} and could result in external power supply going out of regulation. Insure external V_{DD} load will shunt current greater than maximum injection current. This will be the greatest risk when the MCU is not consuming power. Examples are: if no system clock is present, or if clock rate is very low which would reduce overall power consumption. Also, at power-up, system clock is not present during the power-up sequence until the PLL has attained lock.

10.5 Oscillator and Phase Lock Loop (PLLMRFM) Electrical Specifications

Table 47. PLL Electrical Specifications[1]

Characteristic	Symbol	Min	Max	Unit
PLL Reference Frequency Range Crystal reference External reference 1:1 Mode (NOTE: $f_{sys/2} = 2 \times f_{ref\_1:1}$)	 $f_{ref\_crystal}$ f_{ref_ext} $f_{ref\_1:1}$	 8 8 24	 25 25 83	MHz
Core frequency CLKOUT Frequency [2] External reference On-Chip PLL Frequency	f_{core} $f_{sys/2}$	 0 f_{ref} / 32	166 83 83	MHz MHZ MHz
Loss of Reference Frequency [3, 5]	f_{LOR}	100	1000	kHz
Self Clocked Mode Frequency [4, 5]	f_{SCM}	TBD	TBD	MHz
Crystal Start-up Time [5, 6]	t_{cst}	—	10	ms
EXTAL Input High Voltage Crystal Mode All other modes (Dual Controller (1:1), Bypass, External)	V_{IHEXT} V_{IHEXT}	 TBD TBD	 TBD TBD	V
EXTAL Input Low Voltage Crystal Mode All other modes (Dual Controller (1:1), Bypass, External)	V_{ILEXT} V_{ILEXT}	 TBD TBD	 TBD TBD	V
XTAL Output High Voltage I_{OH} = 1.0 mA	V_{OH}	 TBD	 —	V
XTAL Output Low Voltage I_{OL} = 1.0 mA	V_{OL}	—	 TBD	V
XTAL Load Capacitance[7]		5	30	pF
PLL Lock Time [8]	t_{lpll}	—	750	µs
Power-up To Lock Time [6, 9] With Crystal Reference Without Crystal Reference[10]	t_{lplk}	 — —	 11 750	 ms µs
1:1 Mode Clock Skew (between CLKOUT and EXTAL) [11]	t_{skew}	-1	1	ns
Duty Cycle of reference [5]	t_{dc}	40	60	% $f_{sys/2}$

Table 47. PLL Electrical Specifications[1]

Characteristic	Symbol	Min	Max	Unit
Frequency un-LOCK Range	f_{UL}	- 3.8	4.1	% $f_{sys/2}$
Frequency LOCK Range	f_{LCK}	- 1.7	2.0	% $f_{sys/2}$
CLKOUT Period Jitter, [5, 6, 9,12, 13] Measured at $f_{sys/2}$ Max Peak-to-peak Jitter (Clock edge to clock edge) Long Term Jitter (Averaged over 2 ms interval)	C_{jitter}	 — —	 5 .01	% $f_{sys/2}$
Frequency Modulation Range Limit[14, 15] ($f_{sys/2}$Max must not be exceeded)	C_{mod}	0.8	2.2	% $f_{sys/2}$
ICO Frequency. $f_{ico} = f_{ref} * 2 * (MFD+2)$[16]	f_{ico}	48	83	MHz

NOTES:
1 All values given are initial design targets and subject to change.
2 All internal registers retain data at 0 Hz.
3 "Loss of Reference Frequency" is the reference frequency detected internally, which transitions the PLL into self clocked mode.
4 Self clocked mode frequency is the frequency that the PLL operates at when the reference frequency falls below f_{LOR} with default MFD/RFD settings.
5 This parameter is guaranteed by characterization before qualification rather than 100% tested.
6 Proper PC board layout procedures must be followed to achieve specifications.
7 Load Capacitance determined from crystal manufacturer specifications and will include circuit board parasitics.
8 This specification applies to the period required for the PLL to relock after changing the MFD frequency control bits in the synthesizer control register (SYNCR).
9 Assuming a reference is available at power up, lock time is measured from the time V_{DD} and V_{DDPLL} are valid to $\overline{RSTOUT}$ negating. If the crystal oscillator is being used as the reference for the PLL, then the crystal start up time must be added to the PLL lock time to determine the total start-up time.
10 $t_{lpll} = (64 * 4 * 5 + 5 \times \tau) \times T_{ref}$, where $T_{ref} = 1/F_{ref\_crystal} = 1/F_{ref\_ext} = 1/F_{ref\_1:1}$, and $\tau = 1.57x10^{-6} \times 2(MFD + 2)$
11 PLL is operating in 1:1 PLL mode.
12 Jitter is the average deviation from the programmed frequency measured over the specified interval at maximum $f_{sys/2}$. Measurements are made with the device powered by filtered supplies and clocked by a stable external clock signal. Noise injected into the PLL circuitry via V_{DDPLL} and V_{SSPLL} and variation in crystal oscillator frequency increase the jitter percentage for a given interval.
13 Based on slow system clock of 33MHz maximum frequency.
14 Modulation percentage applies over an interval of 10μs, or equivalently the modulation rate is 100KHz.
15 Modulation rate selected must not result in $f_{sys/2}$ value greater than the $f_{sys/2}$ maximum specified value. Modulation range determined by hardware design.
16 $f_{sys/2} = f_{ico} / (2 * 2^{RFD})$

10.6 External Interface Timing Characteristics

Table 48 lists processor bus input timings.

NOTE

All processor bus timings are synchronous; that is, input setup/hold and output delay with respect to the rising edge of a reference clock. The reference clock is the CLKOUT output.

All other timing relationships can be derived from these values.

Table 48. Processor Bus Input Timing Specifications

Name	Characteristic[1]	Symbol	Min	Max	Unit
B0	CLKOUT	tCYC	12	—	ns
Control Inputs					
B1a	Control input valid to CLKOUT high[2]	tCVCH	9	—	ns
B1b	$\overline{\text{BKPT}}$ valid to CLKOUT high[3]	tBKVCH	9	—	ns
B2a	CLKOUT high to control inputs invalid[2]	tCHCII	0	—	ns
B2b	CLKOUT high to asynchronous control input $\overline{\text{BKPT}}$ invalid[3]	tBKNCH	0	—	ns
Data Inputs					
B4	Data input (D[31:16]) valid to CLKOUT high	tDIVCH	4	—	ns
B5	CLKOUT high to data input (D[31:16]) invalid	tCHDII	0	—	ns

NOTES:
1 Timing specifications have been indicated taking into account the full drive strength for the pads.
2 $\overline{\text{TEA}}$ and $\overline{\text{TA}}$ pins are being referred to as control inputs.
3 Refer to figure A-19.

Timings listed in Table 48 are shown in Figure 7.

* The timings are also valid for inputs sampled on the negative clock edge.

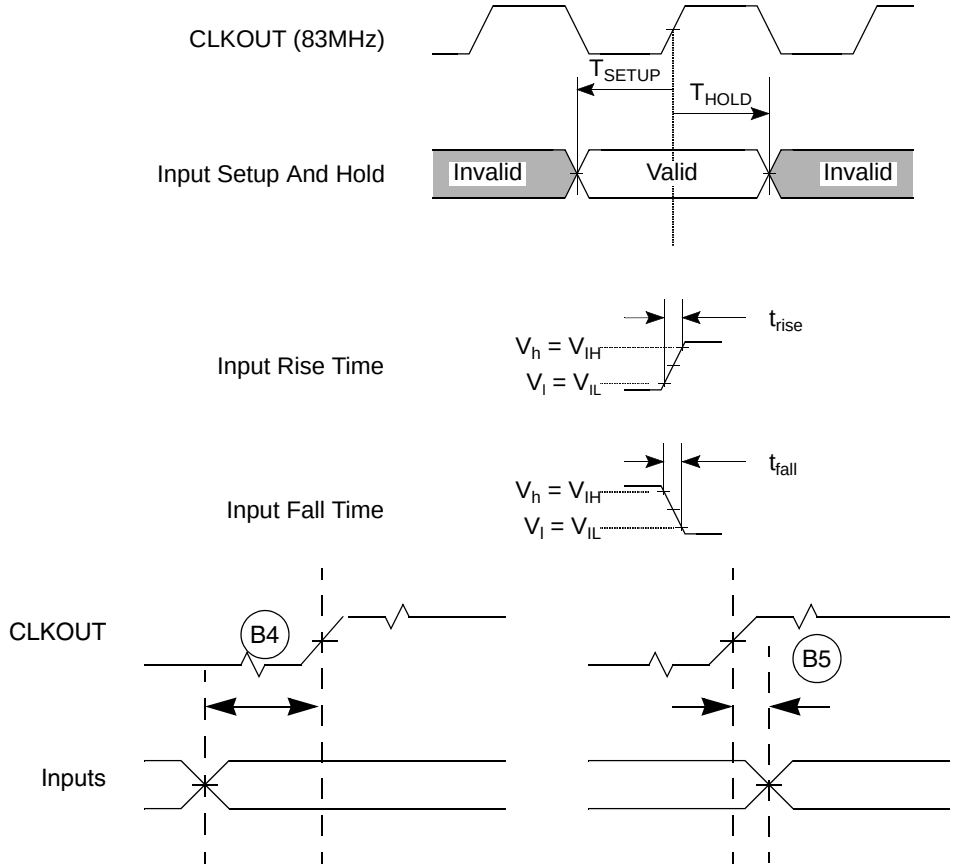


Figure 7. General Input Timing Requirements

10.7 Processor Bus Output Timing Specifications

Table 49 lists processor bus output timings.

Table 49. External Bus Output Timing Specifications

Name	Characteristic	Symbol	Min	Max	Unit
Control Outputs					
B6a	CLKOUT high to chip selects ($\overline{CS}$[7:0]) valid [1]	tCHCV	—	$0.5t_{CYC}$ + 5	ns
B6b	CLKOUT high to byte enables ($\overline{BS}$[3:2]) valid[2]	tCHBV	—	$0.5t_{CYC}$ + 5	ns
B6c	CLKOUT high to output enable ($\overline{OE}$) valid[3]	tCHOV	—	$0.5t_{CYC}$ + 5	ns
B7	CLKOUT high to control output ($\overline{BS}$[3:2], $\overline{OE}$) invalid	tCHCOI	$0.5t_{CYC}$ + 1.5	—	ns
B7a	CLKOUT high to chip selects invalid	tCHCI	$0.5t_{CYC}$ + 1.5	—	ns
Address and Attribute Outputs					
B8	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, TSIZ[1:0], $\overline{TIP}$, R/$\overline{W}$) valid	tCHAV	—	9	ns

Table 49. External Bus Output Timing Specifications (continued)

Name	Characteristic	Symbol	Min	Max	Unit
B9	CLKOUT high to address (A[23:0]) and control ($\overline{TS}$, TSIZ[1:0], $\overline{TIP}$, R/$\overline{W}$) invalid	tCHAI	1.5	—	ns
Data Outputs					
B11	CLKOUT high to data output (D[31:16]) valid	tCHDOV	—	9	ns
B12	CLKOUT high to data output (D[31:16]) invalid	tCHDOI	1.5	—	ns
B13	CLKOUT high to data output (D[31:16]) high impedance	tCHDOZ	—	9	ns

NOTES:
1. $\overline{CS}$ transitions after the falling edge of CLKOUT.
2. $\overline{BS}$ transitions after the falling edge of CLKOUT.
3. $\overline{OE}$ transitions after the falling edge of CLKOUT.

Read/write bus timings listed in Table 49 are shown in Figure 8, Figure 9, and Figure 10.

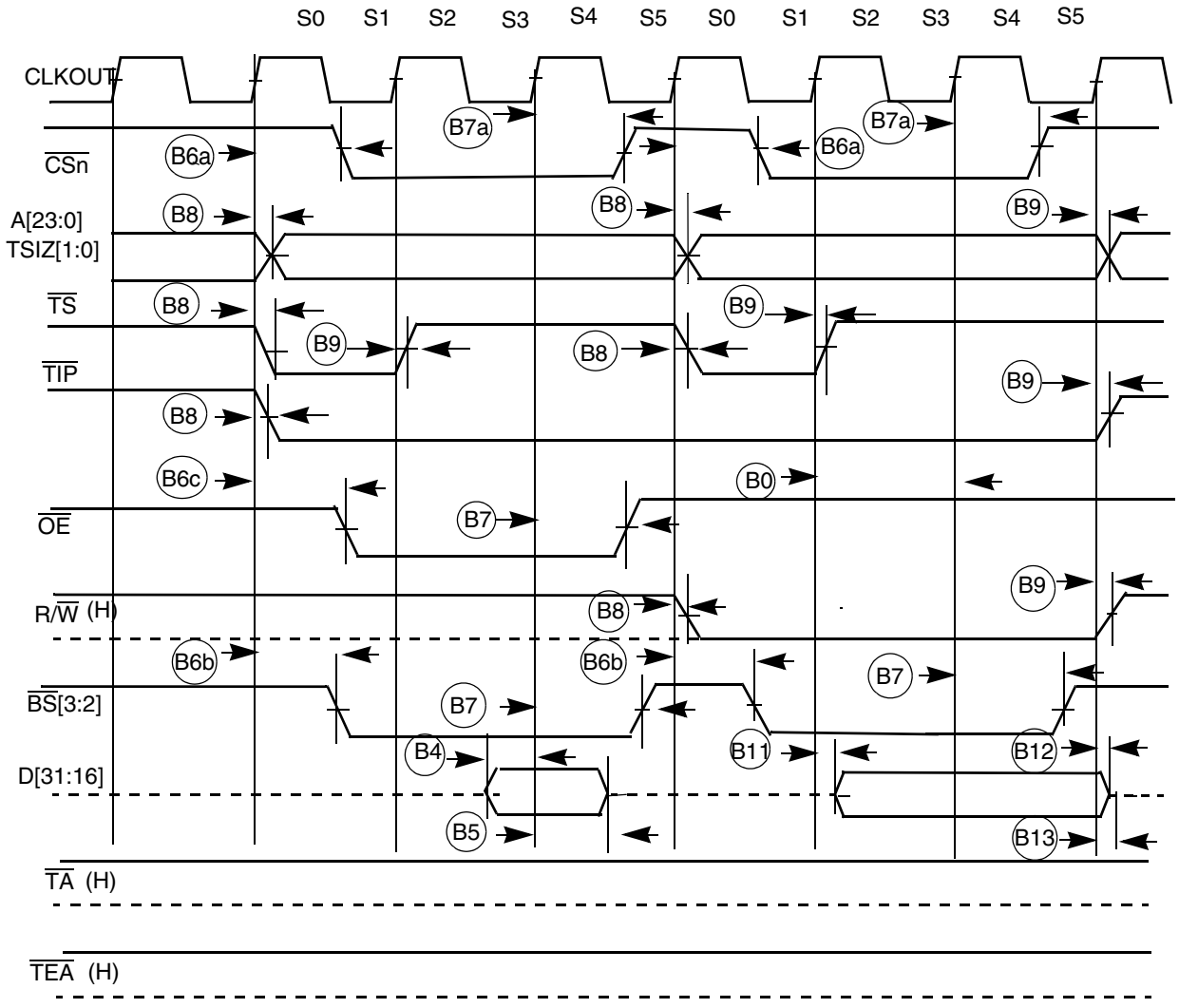


Figure 8. Read/Write (Internally Terminated) SRAM Bus Timing

Figure 9 shows a bus cycle terminated by $\overline{TA}$ showing timings listed in Table 49.

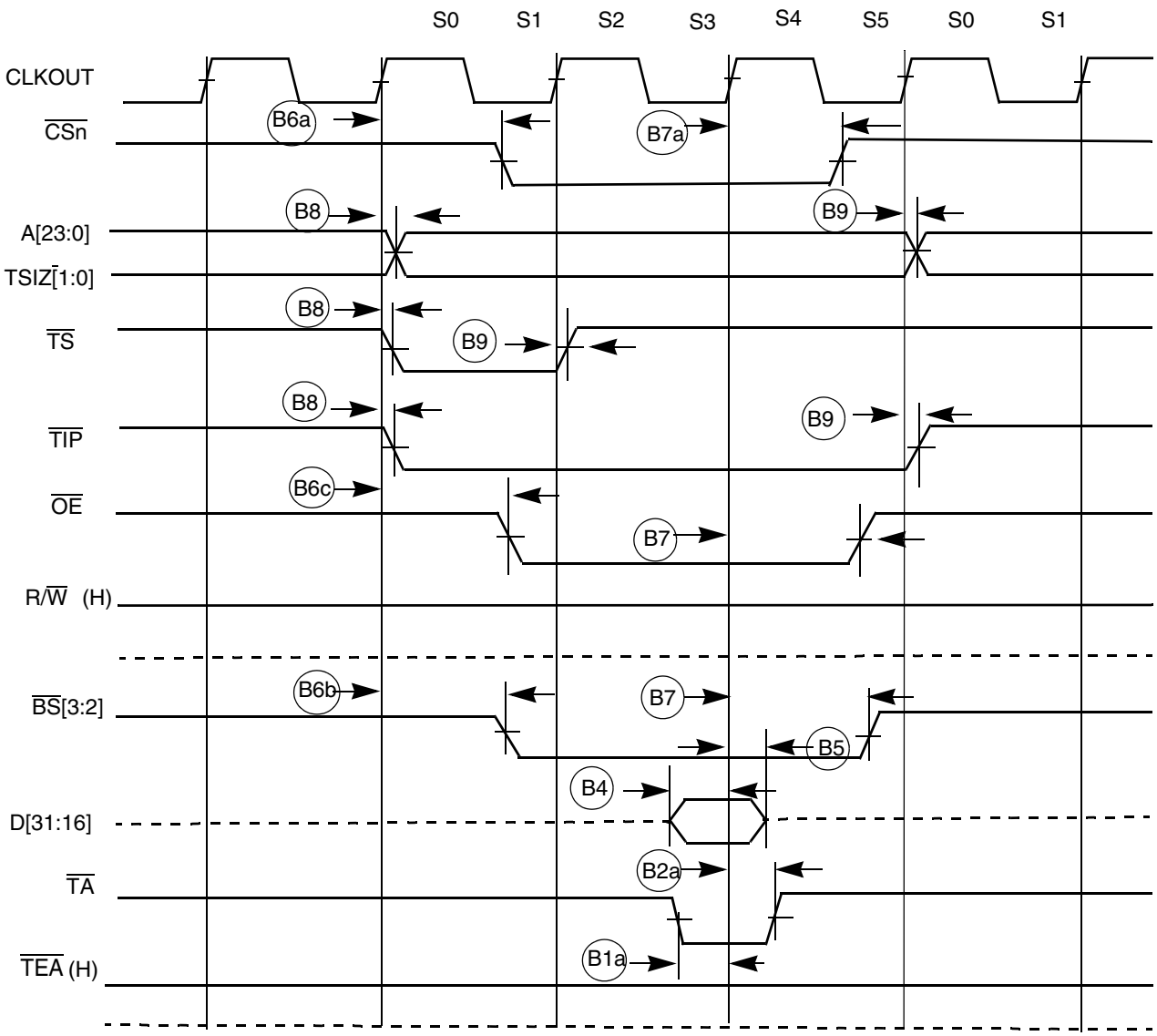


Figure 9. SRAM Read Bus Cycle Terminated by $\overline{TA}$

Figure 10 shows an SRAM bus cycle terminated by $\overline{TEA}$ showing timings listed in Table 49.

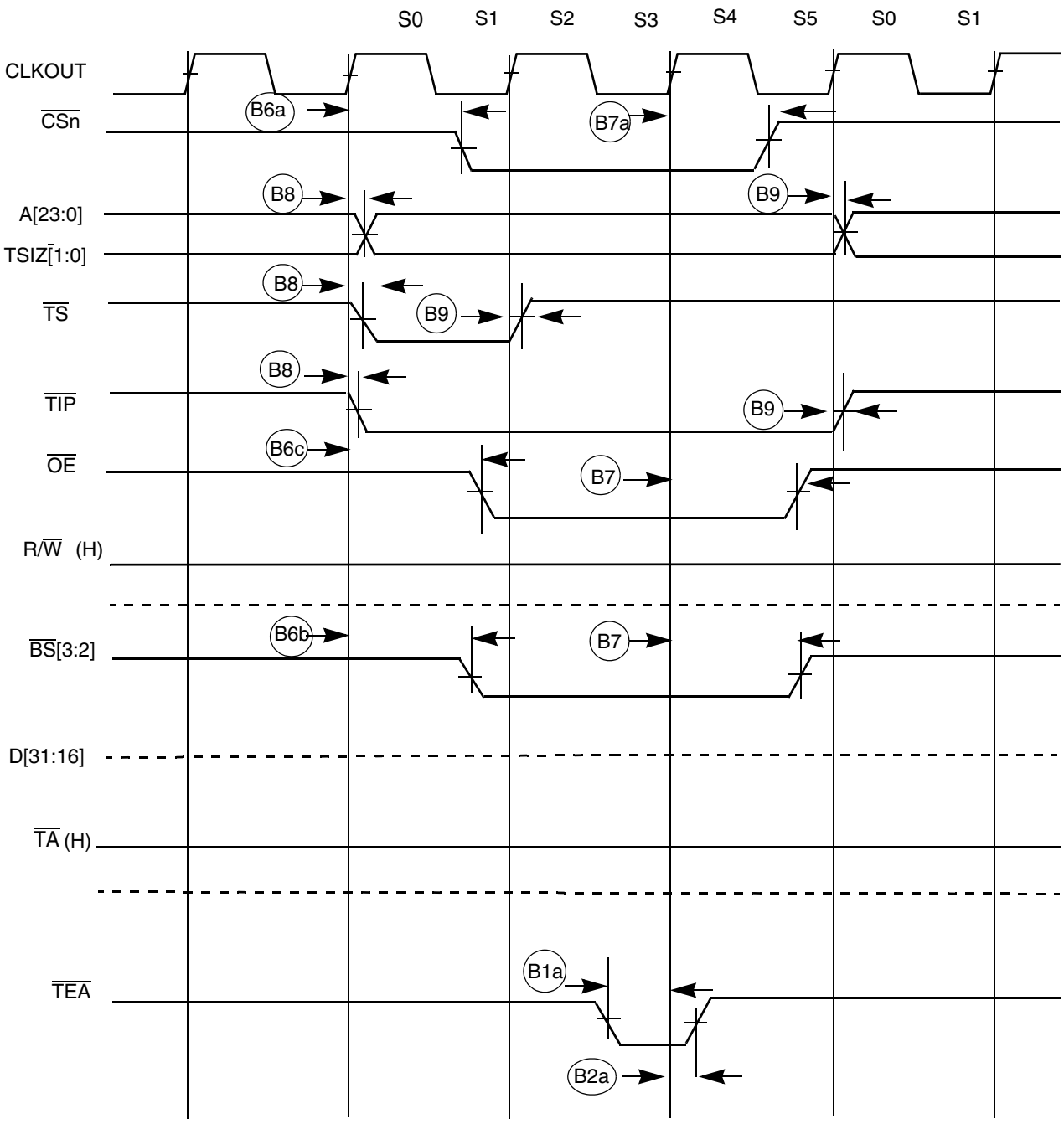


Figure 10. SRAM Read Bus Cycle Terminated by TEA

10.8 DDR SDRAM AC Timing Characteristics

The DDR SDRAM controller uses SSTL2 and I/O drivers. Either Class I or Class II drive strength is available and is user programmable. DDR Clock timing specifications are given in Table 50 and Figure 11.

Table 50. DDR Clock Timing Specifications[1]

Symbol	Characteristic	Min	Max	Unit
V_{MP}	Clock output mid-point voltage	1.05	1.45	V
V_{OUT}	Clock output voltage level	-0.3	SD V_{DD} + 0.3	V
V_{ID}	Clock output differential voltage (peak to peak swing)	0.7	SD V_{DD} + 0.6	V
V_{IX}	Clock crossing point voltage	1.05	1.45	V

NOTES:
1 SD V_{DD} is nominally 2.5V.

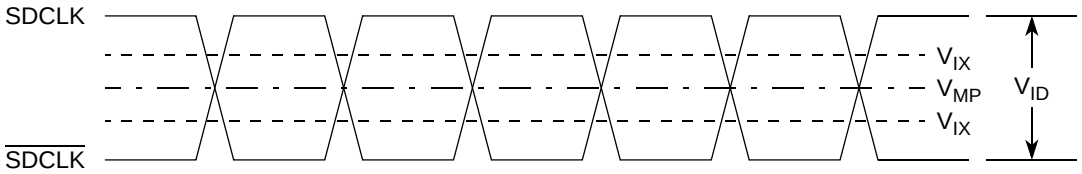


Figure 11. DDR Clock Timing Diagram

When using the DDR SDRAM controller the timing numbers in Table 51 must be followed to properly latch or drive data onto the memory bus. All timing numbers are relative to the two DQS byte lanes.

Table 51. DDR Timing

NUM	Characteristic[1]	Symbol	Min	Max	Unit
	Frequency of operation[2]		TBD	83	MHz
DD1	Clock Period (DDR_CLKOUT)	t_{CK}	12	TBD	ns
DD2	Pulse Width High[3]	t_{CKH}	0.45	0.55	t_{CK}
DD3	Pulse Width Low[3]	t_{CKI}	0.45	0.55	t_{CK}
DD4	DDR_CLKOUT high to DDR address, SD_CKE, SD_CS[1:0], SD_SCAS, SD_SRAS, SD_WE valid	t_{CMV}	-	0.5 x t_{CK} + 1	ns
DD5	DDR_CLKOUT high to DDR address, SD_CKE, $\overline{\text{SD\_CS}}$, $\overline{\text{SD\_SCAS}}$, $\overline{\text{SD\_SRAS}}$, $\overline{\text{SD\_WE}}$ invalid	t_{CMH}	2	-	ns
DD6	Write command to first $\overline{\text{SD\_DQS}}$ Latching Transition	t_{DQSS}	-	1.25	t_{CK}
DD7	$\overline{\text{SD\_DQS}}$ high to Data and DM valid (write) - setup[4,5]	t_{QS}	1.5	-	ns
DD8	$\overline{\text{SD\_DQS}}$ high to Data and DM invalid (write) - hold[4]	t_{QH}	1	-	ns
DD9	$\overline{\text{SD\_DQS}}$ high to Data valid (read) - setup[6]	t_{IS}	-	1	ns
DD10	$\overline{\text{SD\_DQS}}$ high to Data invalid (read) - hold[7]	t_{IH}	0.25 x t_{CK}+ 1	-	ns
DD11	$\overline{\text{SD\_DQS}}$ falling edge to CLKOUT high - setup	t_{DSS}	0.5	-	ns
DD12	$\overline{\text{SD\_DQS}}$ falling edge to CLKOUT high - hold	t_{DSH}	0.5	-	ns
DD13	DQS input read preamble width (t_{RPRE})	t_{RPRE}	0.9	1.1	t_{CK}
DD14	DQS input read postamble width (t_{RPST})	t_{RPST}	0.4	0.6	t_{CK}
DD15	DQS output write preamble width (t_{WPRE})	t_{WPRE}	0.25	—	t_{CK}
DD16	DQS output write postamble width (t_{WPST})	t_{WPST}	0.4	0.6	t_{CK}

NOTES:
1 All timing specifications are based on taking into account, a 25pF load on the SDRAM output pins.
2 DDR_CLKOUT operates at half the frequency of the PLLMRFM output and the ColdFire core.
3 t_{CKH} + t_{CKL} must be less than or equal to t_{CK}.
4 D[31:24] is relative to $\overline{\text{SD\_DQS3}}$ and D[23:16] is relative to $\overline{\text{SD\_DQS2}}$.

5 The first data beat will be valid before the first rising edge of $\overline{\text{SD\_DQS}}$ and after the $\overline{\text{SD\_DQS}}$ write preamble. The remaining data beats will be valid for each subsequent $\overline{\text{SD\_DQS}}$ edge

6 Data input skew is derived from each $\overline{\text{SD\_DQS}}$ clock edge. It begins with a $\overline{\text{SD\_DQS}}$ transition and ends when the last data line becomes valid. This input skew must include DDR memory output skew and system level board skew (due to routing or other factors).

7 Data input hold is derived from each $\overline{\text{SD\_DQS}}$ clock edge. It begins with a $\overline{\text{SD\_DQS}}$ transition and ends when the first data line becomes invalid.

Figure 13 shows a DDR SDRAM write cycle.

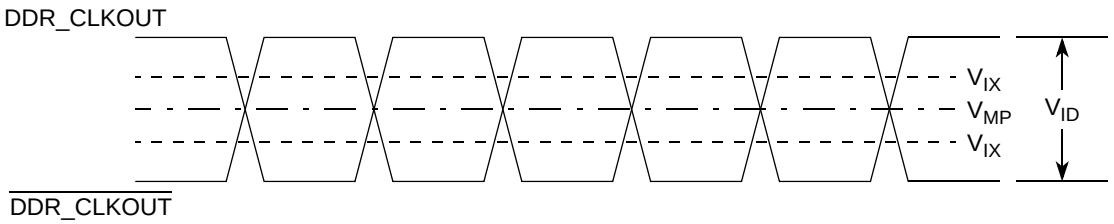


Figure 12. DDR_CLKOUT and $\overline{\text{DDR\_CLKOUT}}$ crossover timing

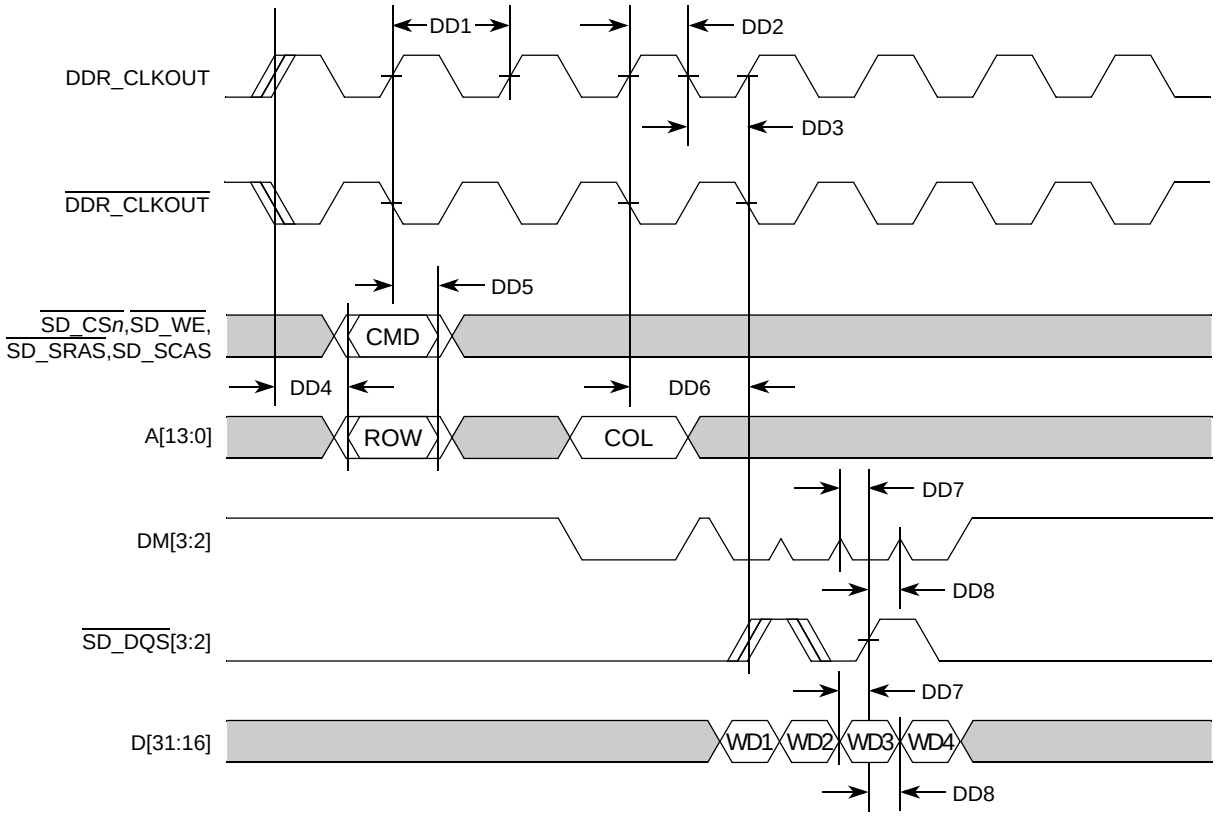


Figure 13. DDR Write Timing

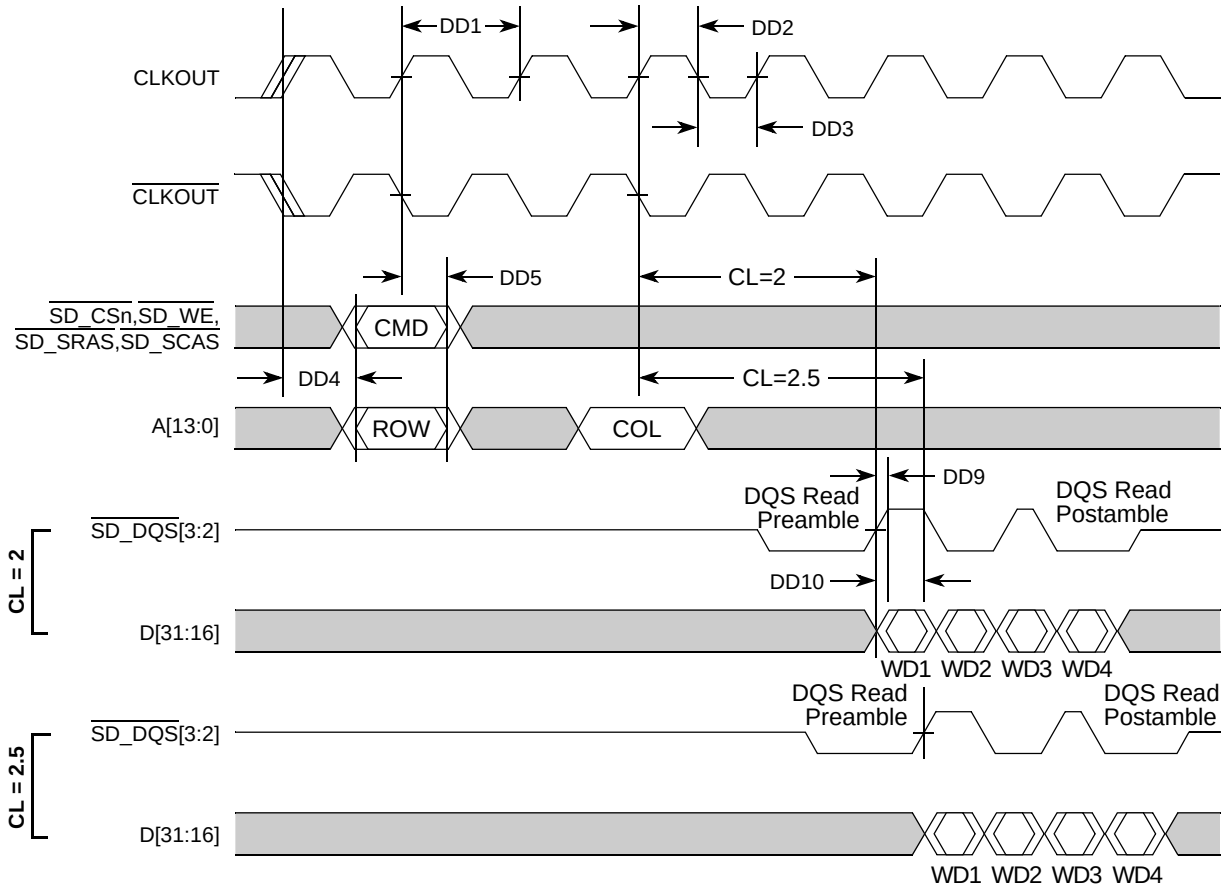


Figure 14. DDR Read Timing

10.9 General Purpose I/O Timing

GPIO can be configured for certain pins of the QSPI, DDR Control, TIMERS, UARTS, FEC0, FEC1, Interrupts and USB interfaces. When in GPIO mode the timing specification for these pins is given in Table 52 and Figure 15.

Table 52. GPIO Timing

NUM	Characteristic	Symbol	Min	Max	Unit
G1	CLKOUT High to GPIO Output Valid	t_{CHPOV}	-	10	ns
G2	CLKOUT High to GPIO Output Invalid	t_{CHPOI}	1.5	-	ns
G3	GPIO Input Valid to CLKOUT High	t_{PVCH}	9	-	ns
G4	CLKOUT High to GPIO Input Invalid	t_{CHPI}	1.5	-	ns

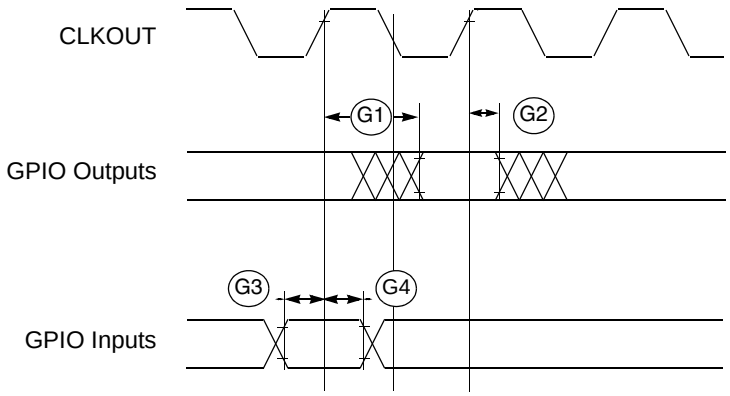


Figure 15. GPIO Timing

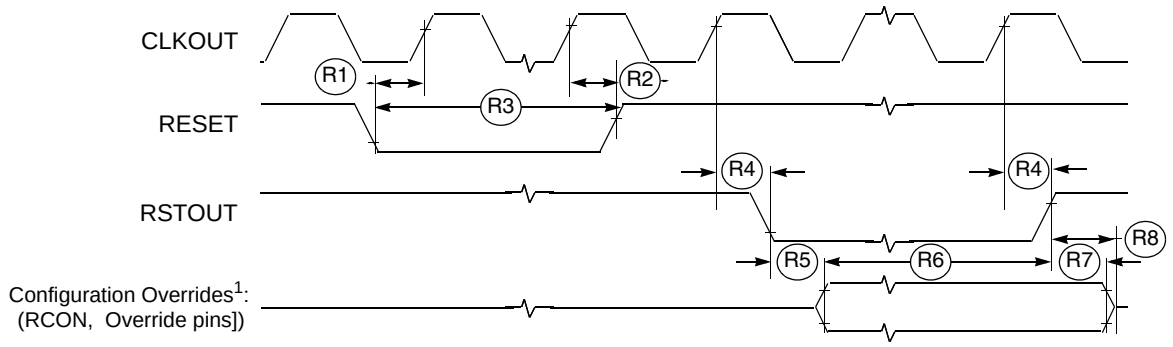
10.10 Reset and Configuration Override Timing

Table 53. Reset and Configuration Override Timing

(V_{DD} = 2.7 to 3.6 V, V_{SS} = 0 V, T_A = T_L to T_H)[1]

NUM	Characteristic	Symbol	Min	Max	Unit
R1	$\overline{\text{RESET}}$ Input valid to CLKOUT High	t_{RVCH}	9	-	ns
R2	CLKOUT High to $\overline{\text{RESET}}$ Input invalid	t_{CHRI}	1.5	-	ns
R3	$\overline{\text{RESET}}$ Input valid Time [2]	t_{RIVT}	5	-	t_{CYC}
R4	CLKOUT High to $\overline{\text{RSTOUT}}$ Valid	t_{CHROV}	-	10	ns
R5	$\overline{\text{RSTOUT}}$ valid to Config. Overrides valid	t_{ROVCV}	0	-	ns
R6	Configuration Override Setup Time to $\overline{\text{RSTOUT}}$ invalid	t_{COS}	20	-	t_{CYC}
R7	Configuration Override Hold Time after $\overline{\text{RSTOUT}}$ invalid	t_{COH}	0	-	ns
R8	$\overline{\text{RSTOUT}}$ invalid to Configuration Override High Impedance	t_{ROICZ}	-	1 x t_{CYC}	ns

NOTES:
1 All AC timing is shown with respect to 50% O V_{DD} levels unless otherwise noted.
2 During low power STOP, the synchronizers for the $\overline{\text{RESET}}$ input are bypassed and $\overline{\text{RESET}}$ is asserted asynchronously to the system. Thus, $\overline{\text{RESET}}$ must be held a minimum of 100 ns.



1. Refer to the Coldfire Integration Module (CIM) section for more information.

Figure 16. $\overline{\text{RESET}}$ and Configuration Override Timing

10.11 Fast Ethernet AC Timing Specifications

MII signals use TTL signal levels compatible with devices operating at either 5.0 V or 3.3 V.

10.11.1 MII Receive Signal Timing (FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER, and FEC*n*_RXCLK)

The receiver functions correctly up to a FEC*n*_RXCLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC*n*_RXCLK frequency.

Table 54 lists MII receive channel timings.

Table 54. MII Receive Signal Timing

Num	Characteristic	Min	Max	Unit
M1	FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER to FEC*n*_RXCLK setup	5	—	ns
M2	FEC*n*_RXCLK to FEC*n*_RXD[3:0], FEC*n*_RXDV, FEC*n*_RXER hold	5	—	ns
M3	FEC*n*_RXCLK pulse width high	35%	65%	FEC*n*_RXCLK period
M4	FEC*n*_RXCLK pulse width low	35%	65%	FEC*n*_RXCLK period

Figure 17 shows MII receive signal timings listed in Table 54.

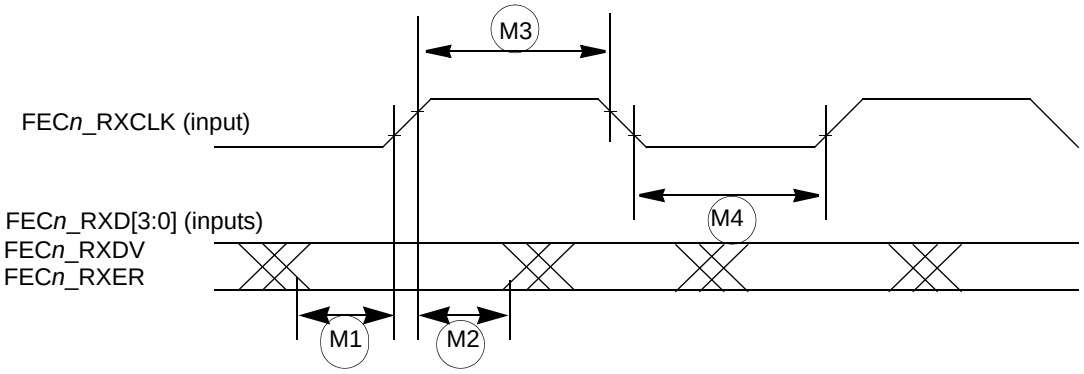


Figure 17. MII Receive Signal Timing Diagram

10.11.2 MII Transmit Signal Timing (FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER, FEC*n*_TXCLK)

Table 55 lists MII transmit channel timings.

The transmitter functions correctly up to a FEC*n*_TXCLK maximum frequency of 25 MHz +1%. There is no minimum frequency requirement. In addition, the processor clock frequency must exceed twice the FEC*n*_TXCLK frequency.

The transmit outputs (FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER) can be programmed to transition from either the rising or falling edge of FEC*n*_TXCLK, and the timing is the same in either case. This options allows the use of non-compliant MII PHYs.

Refer to the Ethernet chapter for details of this option and how to enable it.

Table 55. MII transmit channel timings.

Num	Characteristic	Min	Max	Unit
M5	FEC*n*_TXCLK to FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER invalid	5	—	ns
M6	FEC*n*_TXCLK to FEC*n*_TXD[3:0], FEC*n*_TXEN, FEC*n*_TXER valid	—	25	ns
M7	FEC*n*_TXCLK pulse width high	35%	65%	FEC*n*_TXCLK period
M8	FEC*n*_TXCLK pulse width low	35%	65%	FEC*n*_TXCLK period

Figure 18 shows MII transmit signal timings listed in Table 55.

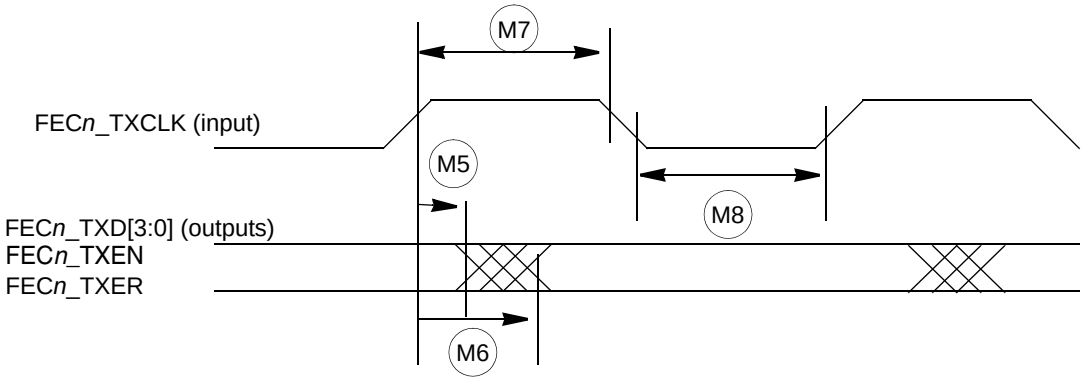


Figure 18. MII Transmit Signal Timing Diagram

10.11.3 MII Async Inputs Signal Timing (FEC*n*_CRS and FEC*n*_COL)

Table 56 lists MII asynchronous inputs signal timing.

Table 56. MII asynchronous input signal timing

Num	Characteristic	Min	Max	Unit
M9	FEC*n*_CRS, FEC*n*_COL minimum pulse width	1.5	—	FEC*n*_TXCLK period

Figure 19 shows MII asynchronous input timings listed in Table 56.

Figure 19. MII Async Inputs Timing Diagram

10.11.4 MII Serial Management Channel Timing (FEC*n*_MDIO and FEC*n*_MDC)

Table 57 lists MII serial management channel timings. The FEC functions correctly with a maximum MDC frequency of 2.5 MHz.

Table 57. MII serial management channel timings.

Num	Characteristic	Min	Max	Unit
M10	FEC*n*_MDC falling edge to FEC*n*_MDIO output invalid (minimum propagation delay)	0	—	ns
M11	FEC*n*_MDC falling edge to FEC*n*_MDIO output valid (max prop delay)	—	25	ns
M12	FEC*n*_MDIO (input) to FEC*n*_MDC rising edge setup	10	—	ns
M13	FEC*n*_MDIO (input) to FEC*n*_MDC rising edge hold	0	—	ns

Table 57. MII serial management channel timings.

Num	Characteristic	Min	Max	Unit
M14	FEC*n*_MDC pulse width high	40%	60%	MDC period
M15	FEC*n*_MDC pulse width low	40%	60%	MDC period

Figure 20 shows MII serial management channel timings listed in Table 57.

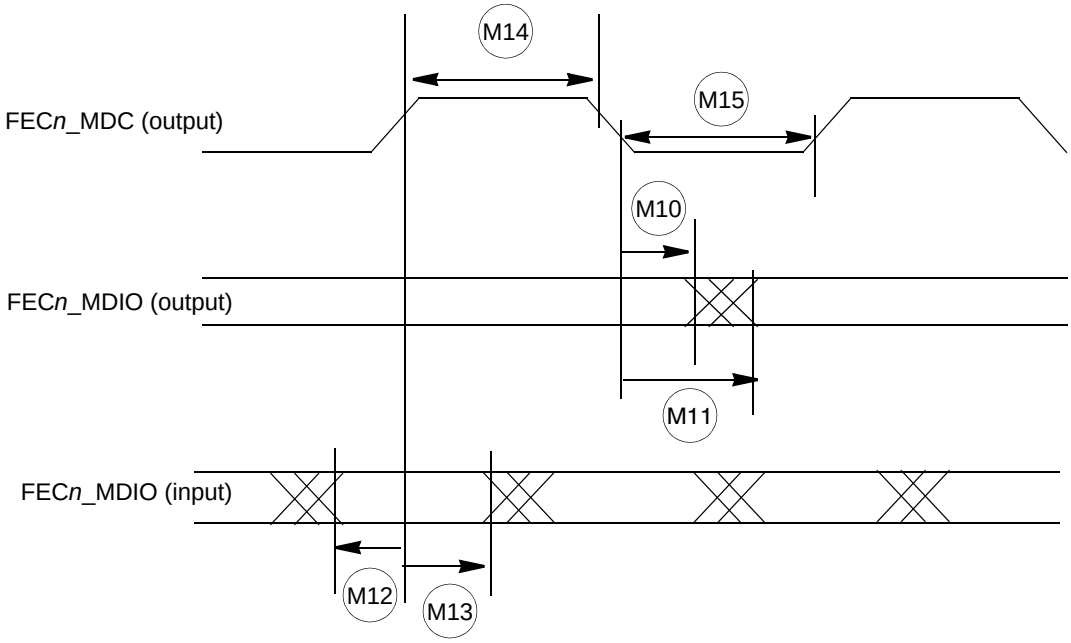


Figure 20. MII Serial Management Channel Timing Diagram

10.11.5USB Interface AC Timing Specifications

Table 58 lists USB Interface timings.

Table 58. USB Interface timings.

Num	Characteristic	Min	Max	Units
US1	USB_CLK frequency of operation	48	48	MHz
US2	USB_CLK fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	2	ns
US3	USB_CLK rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	2	ns
US4	USB_CLK duty cycle (at 0.5 x O V_{DD})	45	55	%
Data Inputs				
US5	USB_RP, USB_RN, USB_RXD valid to USB_CLK high	6	—	ns
US6	USB_CLK high to USB_RP, USB_RN, USB_RXD invalid	6	—	ns
Data Outputs				

Table 58. USB Interface timings.

Num	Characteristic	Min	Max	Units
US7	USB_CLK high to USB_TP, USB_TN, USB_SUSP valid	—	12	ns
US8	USB_CLK high to USB_TP, USB_TN, USB_SUSP invalid	3	—	ns

Figure 21 shows USB interface timings listed in Table 58.

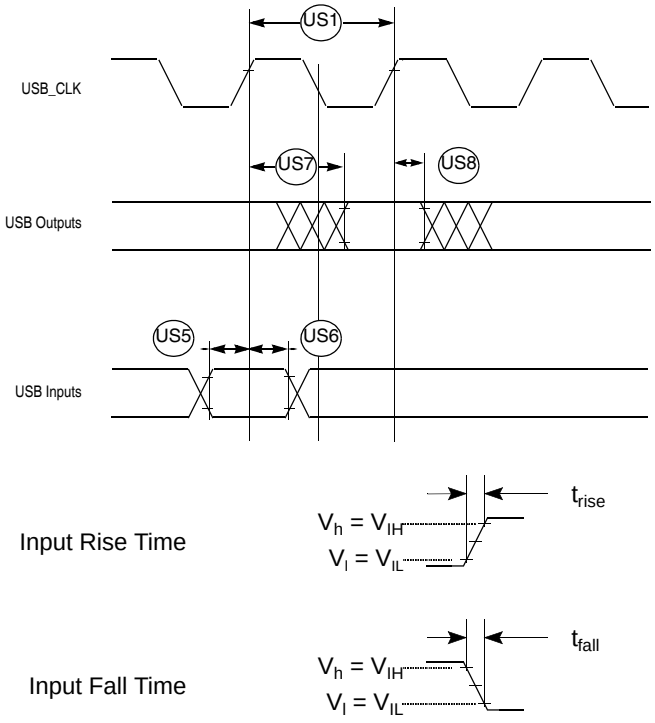


Figure 21. USB Signals timing diagram

10.12 I^2C Input/Output Timing Specifications

Table 59 lists specifications for the I^2C input timing parameters shown in Figure 22.

Table 59. I^2C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1	Start condition hold time	2 x t_{CYC}	—	ns
I2	Clock low period	8 x t_{CYC}	—	ns
I3	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	1	mS
I4	Data hold time	0	—	ns
I5	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	1	mS

Table 59. I²C Input Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I6	Clock high time	4 x t_{CYC}	—	ns
I7	Data setup time	0	—	ns
I8	Start condition setup time (for repeated start condition only)	2 x t_{CYC}	—	ns
I9	Stop condition setup time	2 x t_{CYC}	—	ns

Table 60 lists specifications for the I²C output timing parameters shown in Figure 22.

Table 60. I²C Output Timing Specifications between I2C_SCL and I2C_SDA

Num	Characteristic	Min	Max	Units
I1[1]	Start condition hold time	6 x t_{CYC}	—	ns
I2 [1]	Clock low period	10 x t_{CYC}	—	ns
I3 [2]	I2C_SCL/I2C_SDA rise time (V_{IL} = 0.5 V to V_{IH} = 2.4 V)	—	—	µS
I4 [1]	Data hold time	7 x t_{CYC}	—	ns
I5 [3]	I2C_SCL/I2C_SDA fall time (V_{IH} = 2.4 V to V_{IL} = 0.5 V)	—	3	ns
I6 [1]	Clock high time	10 x t_{CYC}	—	ns
I7 [1]	Data setup time	2 x t_{CYC}	—	ns
I8 [1]	Start condition setup time (for repeated start condition only)	20 x t_{CYC}	—	ns
I9 [1]	Stop condition setup time	10 x t_{CYC}	—	ns

NOTES:
1. Note: Output numbers depend on the value programmed into the IFDR; an IFDR programmed with the maximum frequency (IFDR = 0x20) results in minimum output timings as shown in Table 60. The I²C interface is designed to scale the actual data transition time to move it to the middle of the I2C_SCL low period. The actual position is affected by the prescale and division values programmed into the IFDR; however, the numbers given in Table 60 are minimum values.
2. Because I2C_SCL and I2C_SDA are open-collector-type outputs, which the processor can only actively drive low, the time I2C_SCL or I2C_SDA take to reach a high level depends on external signal capacitance and pull-up resistor values.
3. Specified at a nominal 50-pF load.

Figure 22 shows timing for the values in Table 59 and Table 60.

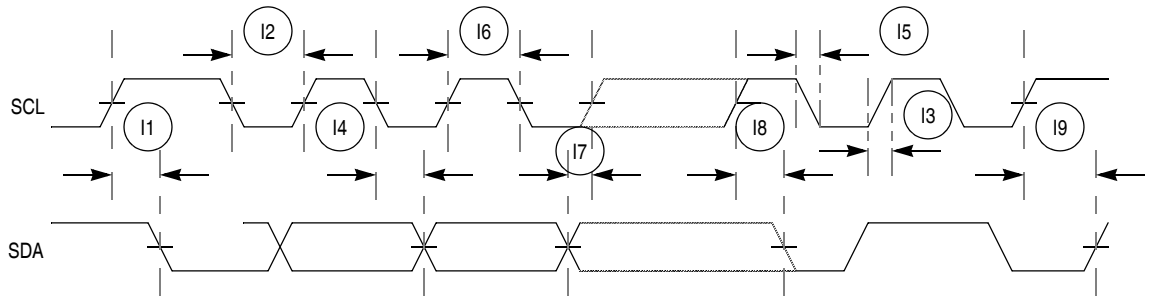


Figure 22. I²C Input/Output Timings

10.13 DMA Timers Timing Specifications

Table 61 lists timer module AC timings.

Table 61. Timer Module AC Timing Specifications

Name	Characteristic [1]	Min	Max	Unit
T1	T0IN / T1IN / T2IN / T3IN cycle time	3 x t_{CYC}	—	ns
T2	T0IN / T1IN / T2IN / T3IN pulse width	1 x t_{CYC}	—	ns

NOTES:
1 All timing references to CLKOUT are given to its rising edge.

10.14 QSPI Electrical Specifications

Table 62 lists QSPI timings.

Table 62. QSPI Modules AC Timing Specifications

Name	Characteristic	Min	Max	Unit
QS1	QSPI_CS[3:0] to QSPI_CLK	1	510	t_{CYC}
QS2	QSPI_CLK high to QSPI_DOUT valid.	—	10	ns
QS3	QSPI_CLK high to QSPI_DOUT invalid (Output hold)	2	—	ns
QS4	QSPI_DIN to QSPI_CLK (Input setup)	9	—	ns
QS5	QSPI_DIN to QSPI_CLK (Input hold)	9	—	ns

The values in Table 62 correspond to Figure 23.

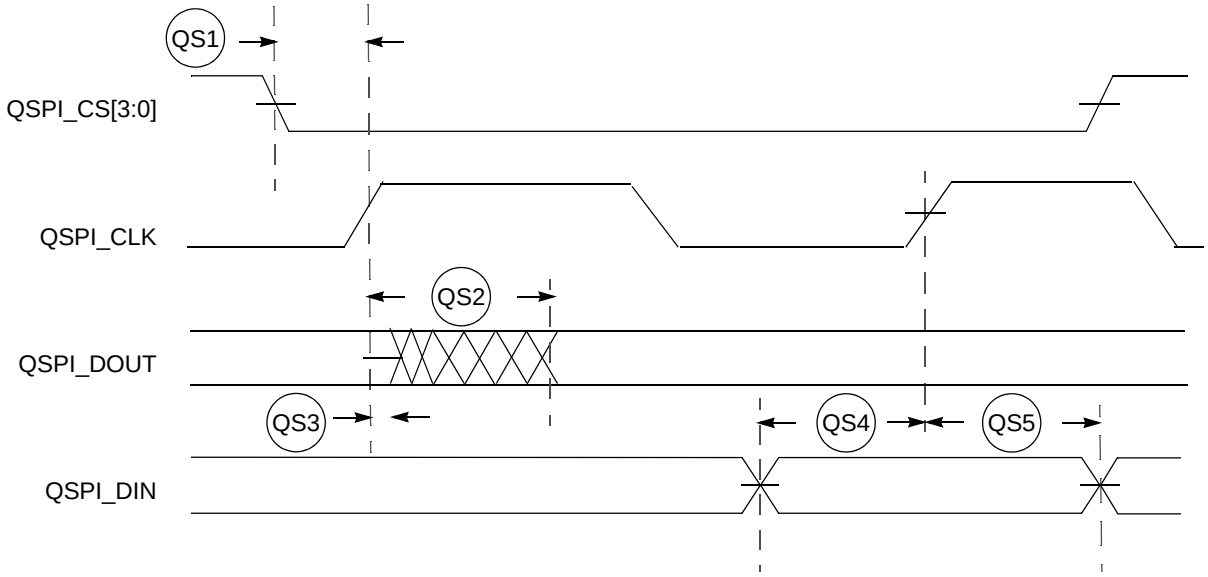


Figure 23. QSPI Timing

10.15 JTAG and Boundary Scan Timing

Table 63. JTAG and Boundary Scan Timing

Num	Characteristics[1]	Symbol	Min	Max	Unit
J1	TCLK Frequency of Operation	f_{JCYC}	DC	1/4	$f_{sys/2}$
J2	TCLK Cycle Period	t_{JCYC}	4 x t_{CYC}	-	ns
J3	TCLK Clock Pulse Width	t_{JCW}	26	-	ns
J4	TCLK Rise and Fall Times	t_{JCRF}	0	3	ns
J5	Boundary Scan Input Data Setup Time to TCLK Rise	t_{BSDST}	4	-	ns
J6	Boundary Scan Input Data Hold Time after TCLK Rise	t_{BSDHT}	26	-	ns
J7	TCLK Low to Boundary Scan Output Data Valid	t_{BSDV}	0	33	ns
J8	TCLK Low to Boundary Scan Output High Z	t_{BSDZ}	0	33	ns
J9	TMS, TDI Input Data Setup Time to TCLK Rise	t_{TAPBST}	4	-	ns
J10	TMS, TDI Input Data Hold Time after TCLK Rise	t_{TAPBHT}	10	-	ns
J11	TCLK Low to TDO Data Valid	t_{TDODV}	0	26	ns
J12	TCLK Low to TDO High Z	t_{TDODZ}	0	8	ns
J13	$\overline{TRST}$ Assert Time	t_{TRSTAT}	100	-	ns
J14	$\overline{TRST}$ Setup Time (Negation) to TCLK High	t_{TRSTST}	10	-	ns

NOTES:
1 JTAG_EN is expected to be a static signal. Hence, it is not associated with any timing.

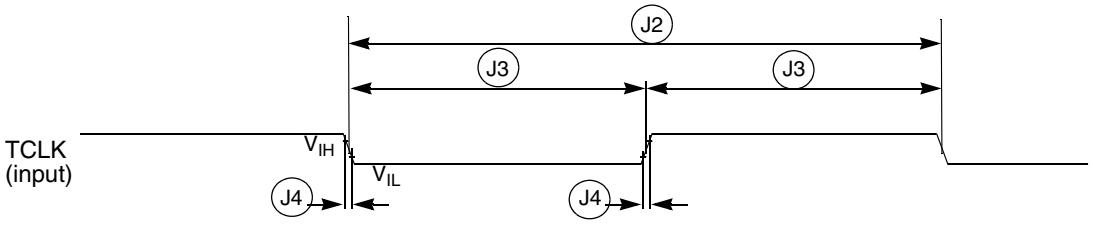


Figure 24. Test Clock Input Timing

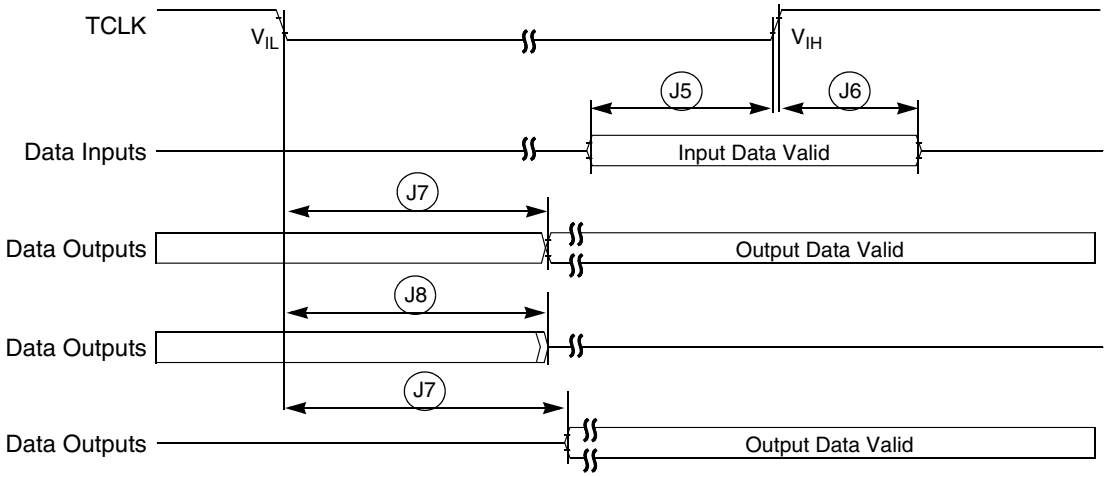


Figure 25. Boundary Scan (JTAG) Timing

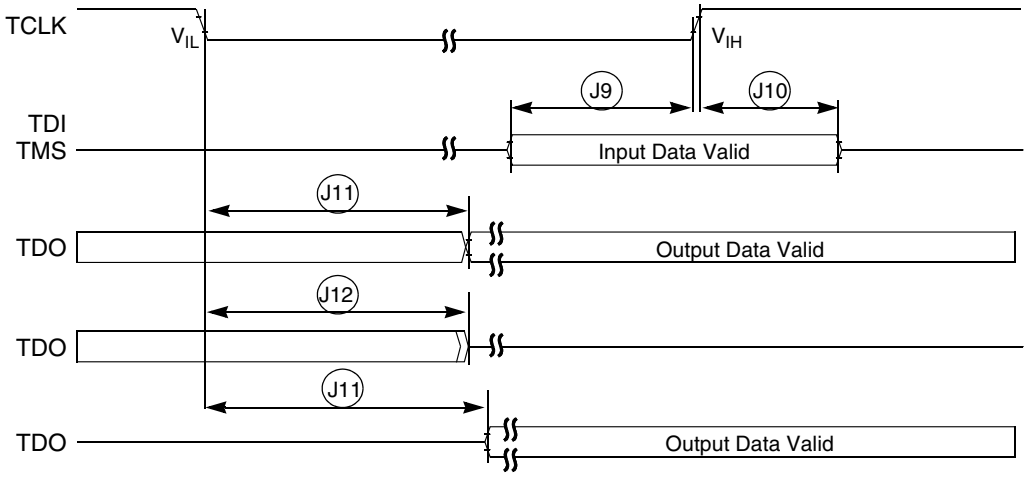


Figure 26. Test Access Port Timing

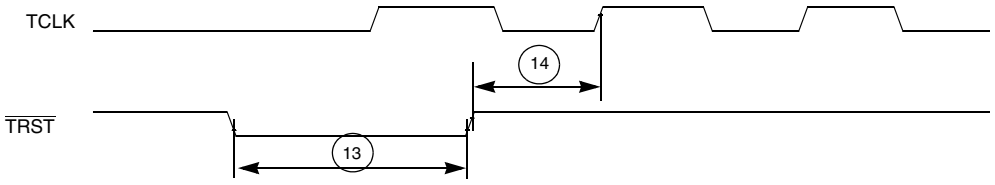


Figure 27. TRST Timing

10.16 Debug AC Timing Specifications

Table 64 lists specifications for the debug AC timing parameters shown in Figure 29.

Table 64. Debug AC Timing Specification

Num	Characteristic	166 MHz		Units
		Min	Max	
D0	PSTCLK cycle time		0.5	t_{CYC}
D1	PST, DDATA to CLKOUT setup	4		ns
D2	CLKOUT to PST, DDATA hold	1.5		ns
D3	DSI-to-DSCLK setup	1 x t_{CYC}		ns
D4 [1]	DSCLK-to-DSO hold	4 x t_{CYC}		ns

Table 64. Debug AC Timing Specification

Num	Characteristic	166 MHz		Units
		Min	Max	
D5	DSCLK cycle time	5 x t_{CYC}		ns
D6	$\overline{BKPT}$ input data setup time to CLKOUT Rise	4		ns
D7	$\overline{BKPT}$ input data hold time to CLKOUT Rise	1.5		ns
D8	CLKOUT high to $\overline{BKPT}$ high Z	0.0	10.0	ns

NOTES:
1 DSCLK and DSI are synchronized internally. D4 is measured from the synchronized DSCLK input relative to the rising edge of CLKOUT.

Figure 28 shows real-time trace timing for the values in Table 64.

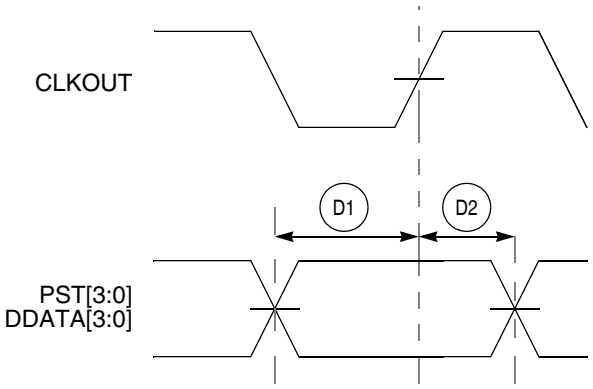


Figure 28. Real-Time Trace AC Timing

Figure 29 shows BDM serial port AC timing for the values in Table 64.

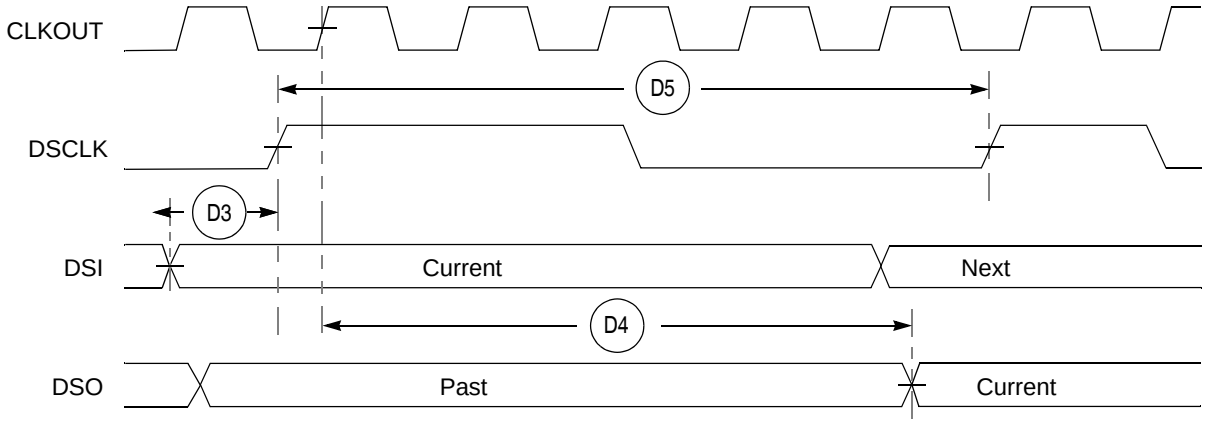


Figure 29. BDM Serial Port AC Timing

11 Device/Family Documentation List

Table 65. MCF5275 Documentation

Motorola Document Number	Title	Revision	Status
MCF5275EC/D	MCF5275 RISC Microprocessor Hardware Specifications	0	This Document
MCF5275RM/D	MCF5275 Reference Manual	0	In Process
MCF5275PB/D	MCF5275 Product Brief	0	Available
MCF5275FS	MCF5275 Fact Sheet	0	In Process
CFPRODFACT/D	The ColdFire Family of 32-Bit Microprocessors Family Overview and Technology Roadmap	0	Available
MCF5XXXWP	MCF5XXXWP WHITE PAPER: Motorola ColdFire VL RISC Processors	0	Available
MAPBGAPP	MAPBGA 4-Layer example	0	Available
CFPRM/D	ColdFire Family Programmer's Reference Manual	2	Available

12 Document Revision History

Table 66 provides a revision history for this hardware specification.

Table 66. Document Revision History

Rev. No.	Substantive Change(s)
1.1	Removed duplicate information in the module description sections. The information is all in the Signals Description Table.
1	Added Figure 6
0	Initial release.

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