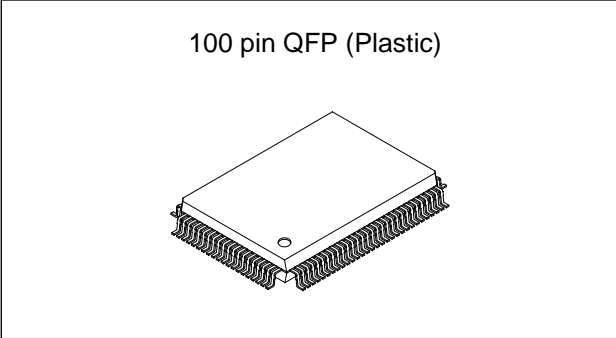# SONY

CXP88852/88860

CMOS 8-bit Single Chip Microcomputer

Description

The CXP88852/88860 is a CMOS 8-bit microcomputer which consists of A/D converter, serial interface, timer/counter, time base timer, high precision timing pattern generation circuits, PWM output, VISS/ VASS circuit, 32kHz timer/counter, remote control receiving circuit, VSYNC separator and the measurement circuit which measure signals of capstan FG amplifier and drum FG/PG amplifier and other servo systems, as well as basic configurations like 8-bit CPU, ROM, RAM and I/O port. They are integrated into a single chip.

Also, CXP88852/88860 provides sleep/stop function which enables to lower power consumption.
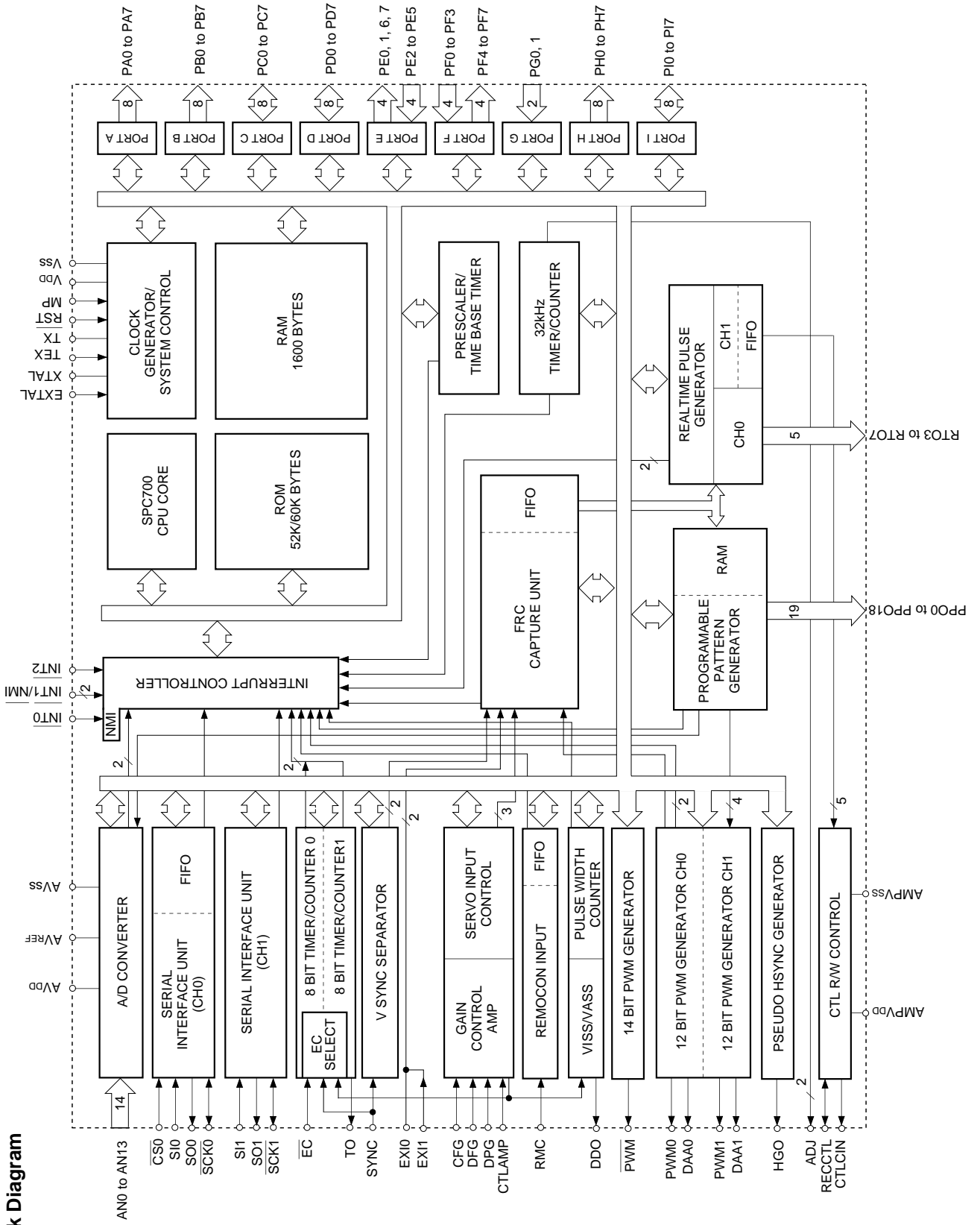
100 pin QFP (Plastic)
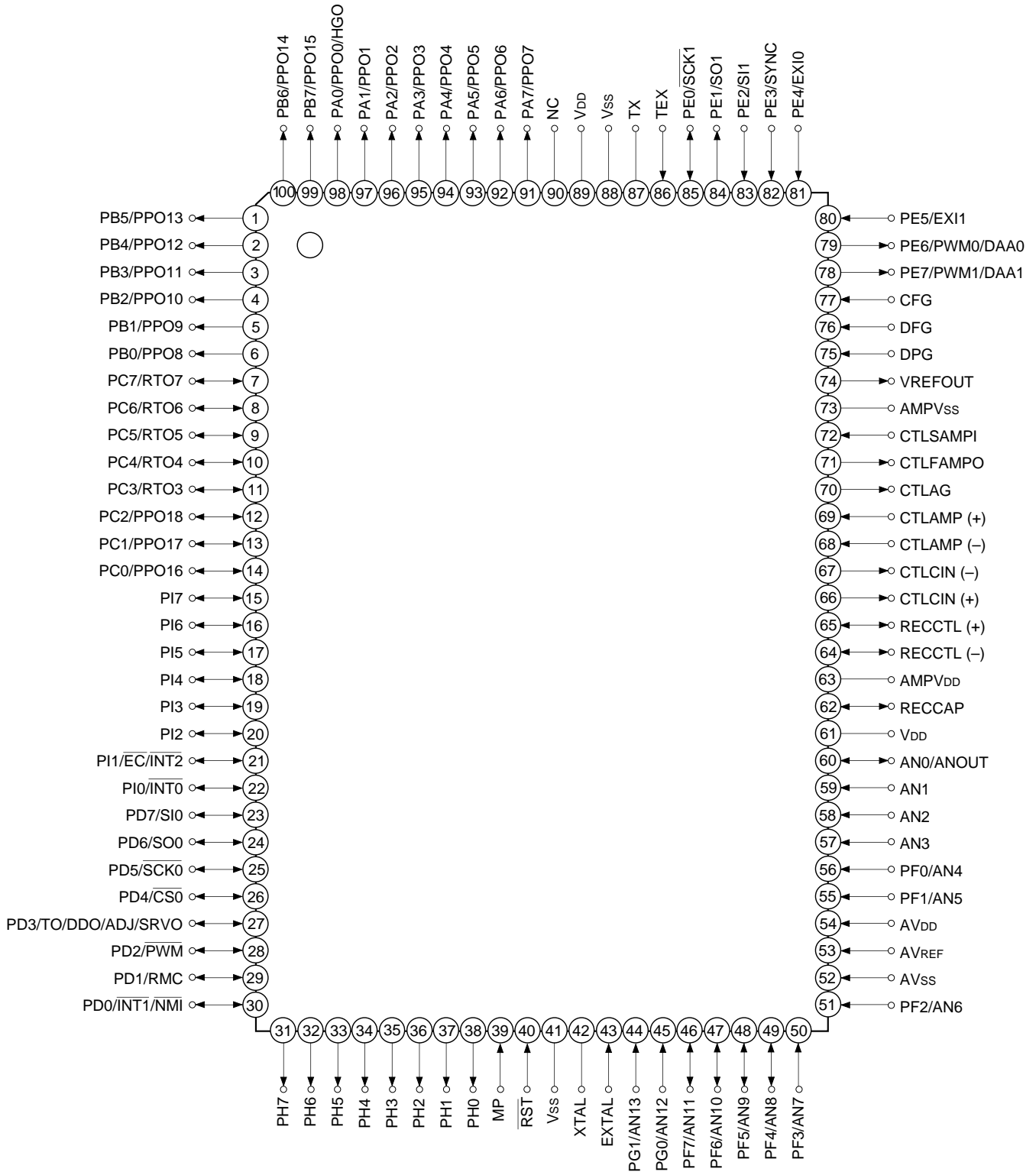
Structure
Silicon gate CMOS IC

Features
• A wide instruction set (213 instructions) which cover various types of data
  — 16-bit arithmetic/multiplication and division/boolean bit operation instructions
• Minimum instruction cycle   250ns at 16MHz operation
                                   122µs at 32kHz operation
• Incorporated ROM capacity   52K bytes (CXP88852)
                                   60K bytes (CXP88860)
• Incorporated RAM capacity   1600 bytes (including PPG RAM)
• Peripheral function
  — A/D converter   8 bits, 14 channels, successive approximation system
                                              (Conversion time of 20µs/16MHz)
  — Serial interface   Incorporated 8-bit, 8-stage FIFO for data
                                              (Auto transfer for 1 to 8 bytes), 1 channel
                                              8-bit clock sync type, 1 channel
  — Timer   8-bit timer/counter, 2 channels
                                              19-bit time base timer
                                              32kHz timer/counter
  — High precision timing pattern generation PPG 19 pins 32-stage programmable circuit
                                              RTG 5 pins, 1 channel
                                                       5-bit, 8-satge FIFO (RECCTL control), 1channel
  — PWM/DA gate output   12 bits, 2 channels (Repetitive frequency 62.5kHz/16MHz)
                                              DA gate pulse output, 13 bits, 2 channels
  — Analog signal input circuit   Capstan FG amplifier circuit
                                              Drum FG amplifier circuit
                                              Drum PG amplifier circuit
                                              PBCTL amplifier circuit
  — CTL write/rewrite circuit   Recording current control circuit
  — Servo input control   Capstan FG, Drum FG/PG, CTL input
  — VSYNC separator
  — FRC capture unit   Incorporated 26-bit and 8-stage FIFO
  — PWM output   14-bit, 1 channel
  — VISS/VASS circuit   Pulse duty auto detection circuit
  — 32kHz timer/event counter   32kHz oscillation circuit, ultra-low speed instruction mode
  — Remote control reception circuit   8-bit pulse measurement counter, 6-stage FIFO
  — Tri-state output   PPG 1 pin, output 8 pins
  — Pseudo HSYNC output function
  — High speed head switching circuit
• Interruption   20 factors, 15 vectors, multi-interruption possible
• Standby mode   SLEEP/STOP
• Package   100-pin plastic QFP
• Piggyback/evaluation chip   CXP88800 100-pin ceramic QFP

E96515-ST

Block Diagram

Pin Assignment (Top View)

Top pins (left to right, 100–81): PB6/PPO14, PB7/PPO15, PA0/PPO0/HGO, PA1/PPO1, PA2/PPO2, PA3/PPO3, PA4/PPO4, PA5/PPO5, PA6/PPO6, PA7/PPO7, NC, V$_{DD}$, V$_{SS}$, TX, TEX, PE0/$\overline{SCK1}$, PE1/SO1, PE2/SI1, PE3/SYNC, PE4/EXI0

Left pins (1–30):

Pin	Signal
1	PB5/PPO13
2	PB4/PPO12
3	PB3/PPO11
4	PB2/PPO10
5	PB1/PPO9
6	PB0/PPO8
7	PC7/RTO7
8	PC6/RTO6
9	PC5/RTO5
10	PC4/RTO4
11	PC3/RTO3
12	PC2/PPO18
13	PC1/PPO17
14	PC0/PPO16
15	PI7
16	PI6
17	PI5
18	PI4
19	PI3
20	PI2
21	PI1/$\overline{EC}$/$\overline{INT2}$
22	PI0/$\overline{INT0}$
23	PD7/SI0
24	PD6/SO0
25	PD5/$\overline{SCK0}$
26	PD4/$\overline{CS0}$
27	PD3/TO/DDO/ADJ/SRVO
28	PD2/$\overline{PWM}$
29	PD1/RMC
30	PD0/$\overline{INT1}$/$\overline{NMI}$

Right pins (80–51):

Pin	Signal
80	PE5/EXI1
79	PE6/PWM0/DAA0
78	PE7/PWM1/DAA1
77	CFG
76	DFG
75	DPG
74	VREFOUT
73	AMPV$_{SS}$
72	CTLSAMPI
71	CTLFAMPO
70	CTLAG
69	CTLAMP (+)
68	CTLAMP (−)
67	CTLCIN (−)
66	CTLCIN (+)
65	RECCTL (+)
64	RECCTL (−)
63	AMPV$_{DD}$
62	RECCAP
61	V$_{DD}$
60	AN0/ANOUT
59	AN1
58	AN2
57	AN3
56	PF0/AN4
55	PF1/AN5
54	AV$_{DD}$
53	AV$_{REF}$
52	AV$_{SS}$
51	PF2/AN6

Bottom pins (left to right, 31–50): PH7, PH6, PH5, PH4, PH3, PH2, PH1, PH0, MP, $\overline{RST}$, V$_{SS}$, XTAL, EXTAL, PG1/AN13, PG0/AN12, PF7/AN11, PF6/AN10, PF5/AN9, PF4/AN8, PF3/AN7

Note) 1. NC (Pin 90) is always connected to V$_{DD}$.

2. V$_{DD}$ (Pins 61 and 89) are both connected to V$_{DD}$

3. Vss (Pins 41 and 88) are both connected to GND.
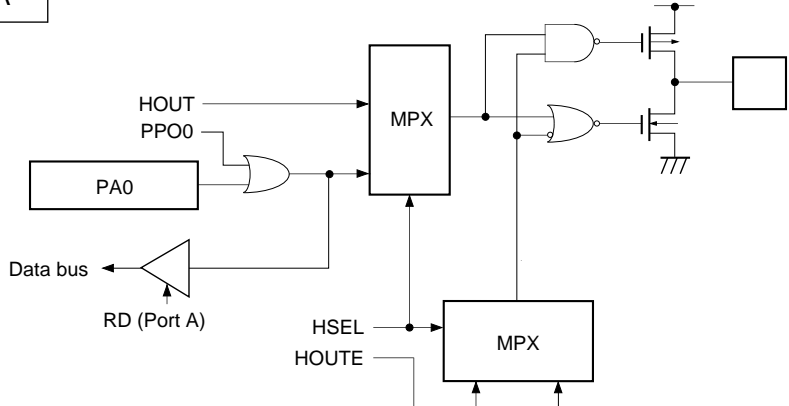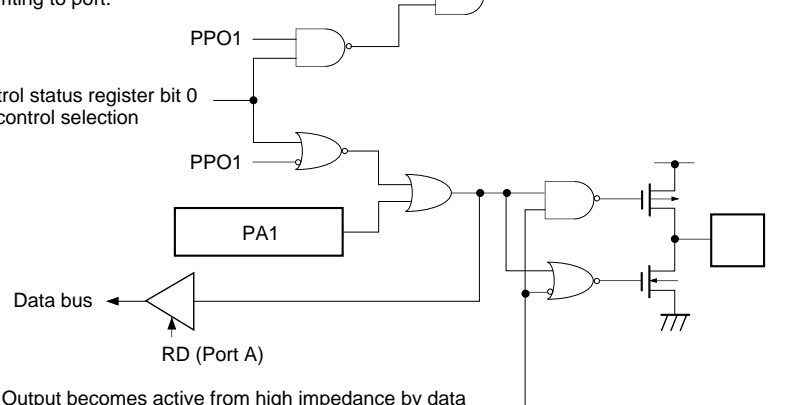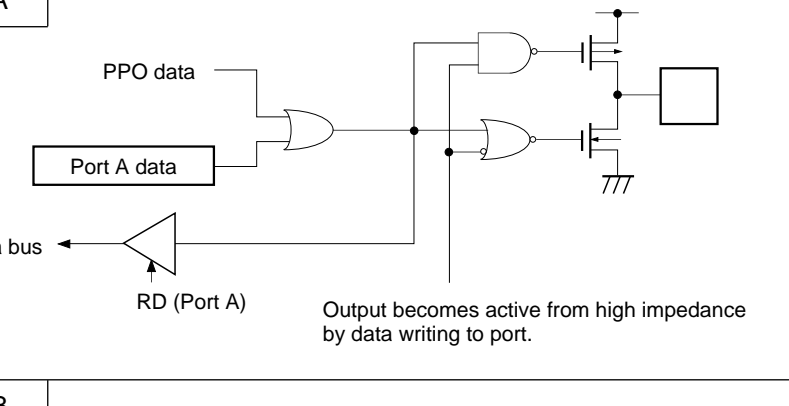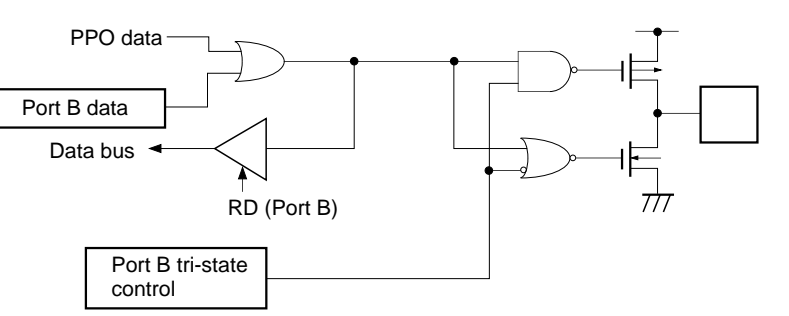
4. MP (Pin 39) must be connected to GND.

Pin Description

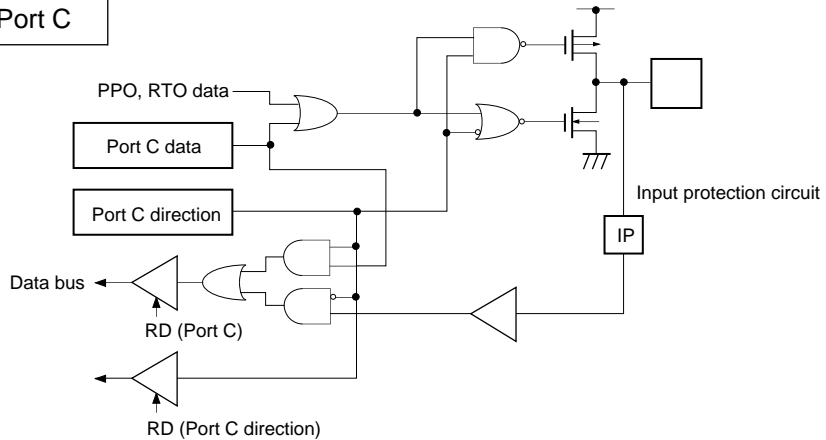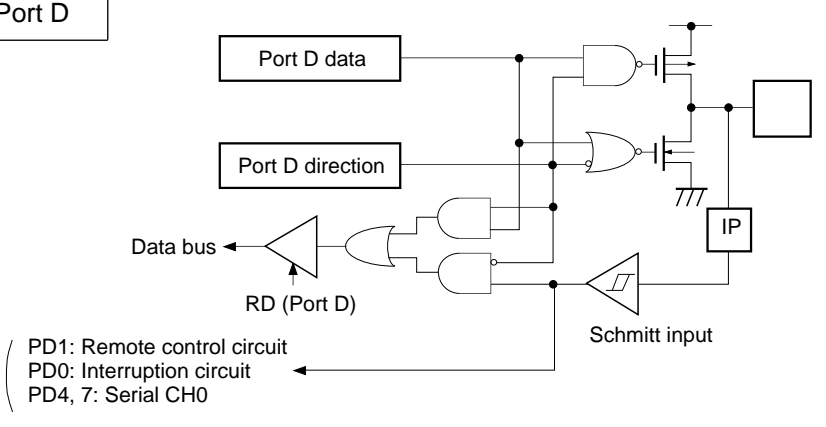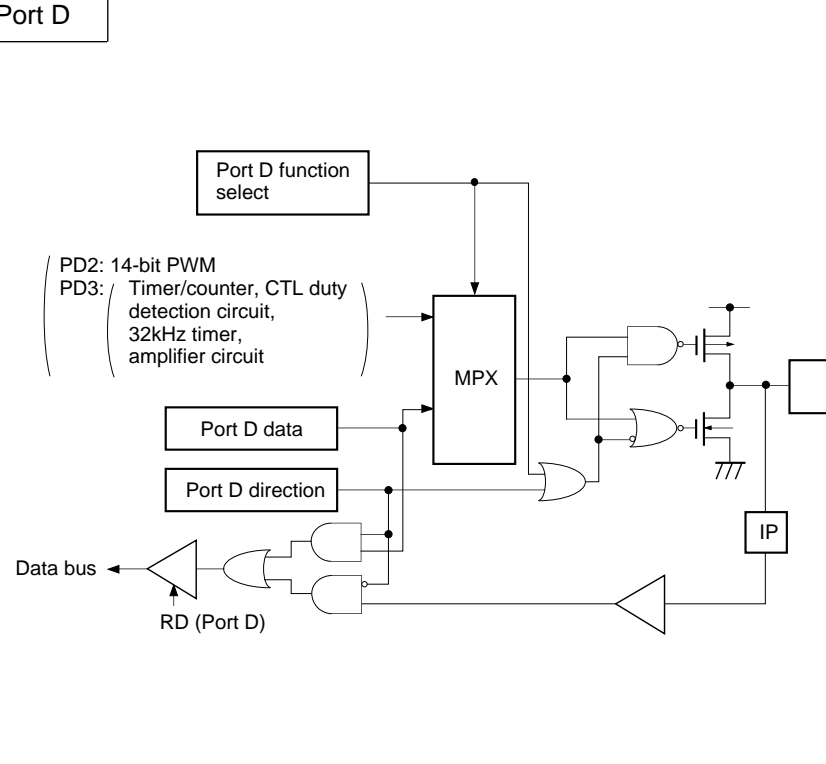| Symbol	I/O	Description	
PA0/PPO0 /HGO	Output/Real-time output/Output	(Port A) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. (8 pins)	Pseudo HSYNC output pin.
PA1/PPO1 to PA7/PPO7	Output/ Real-time output		Programmable pattern generator (PPG) output. Functions as high precision real-time pulse output port. (19 pins) PA0 can be tri-state controlled with PPG.
PB0/PPO8 to PB7/PPO15	Output/ Real-time output	(Port B) 8-bit output port. Data is gated with PPO contents by OR-gate and they are output. Tri-state control is possible. (8 pins)	
PC0/PPO16 to PC2/PPO18	I/O/ Real-time output	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Data is gated with PPO or RT contents by OR-gate and they are output. (8 pins)	
PC3/RTO3 to PC7/RTO7	I/O/ Real-time output		Real-time pulse generator (RTG) output. Functions as high precision real-time pulse output port. (5 pins)
PD0/$\overline{\text{INT1}}$/ $\overline{\text{NMI}}$	I/O/Input/Input	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. (8 pins)	Input pin to request external interruption and non-maskable interruption.
PD1/RMC	I/O/Input		Remote control receiving circuit input pin.
PD2/$\overline{\text{PWM}}$	I/O/Output		14-bit PWM output pin.
PD3/TO DDO/ADJ SRVO	I/O/Output/Output/ Output/Output		Timer/counter, CTL duty detector, 32kHz oscillation adjustment and servo amplifier output pin.
PD4/$\overline{\text{CS0}}$	I/O/Input		Serial chip select (CH0) input pin.
PD5/$\overline{\text{SCK0}}$	I/O/I/O		Serial clock (CH0) I/O pin.
PD6/SO0	I/O/Output		Serial data (CH0) output pin.
PD7/SI0	I/O/Input		Serial data (CH0) input pin.
PE0/$\overline{\text{SCK1}}$	Output/I/O	(Port E) 8-bit port. Bits 2, 3, 4 and 5 are for inputs; bits 0, 1, 6 and 7 are for outputs. (8 pins)	Serial clock (CH1) I/O pin
PE1/SO1	Output/Output		Serial data (CH1) output pin
PE2/SI1	Input/Input		Serial data (CH1) input pin
PE3/SYNC	Input/Input		Composite sync signal input pin.
PE4/EXI0	Input/Input		External input pin for FRC capture unit. (2 pins)
PE5/EXI1	Input/Input		
PE6/PWM0/ DAA0	Output/Output		PWM output pin. (2 pins) / DA gate pulse output pin. (2 pins)
PE7/PWM1/ DAA1	Output/Output		

– 4 –

Description	I/O	Description	
AN0/ANOUT	Input/Output		Analog circuit internal waveform output pin.
AN1 to AN3	Input		Analog input pin for A/D converter. (14 pins)
PF0/AN4 to PF3/AN7	Input/Input	(Port F) Lower 4 bits are for inputs; upper 4 bits are for outputs. Lower 4 bits are standby release input pins. (8 pins)	
PF4/AN8 to PF7/AN11	Output/Input		
PG0/AN12 PG1/AN13	Input/Input	(Port G) 2-bit input port. (2 pins)	
PH0 to PH7	Output	(Port H) 8-bit output port; N-ch open drain output of medium drive voltage (12V) and large current (12mA). (8 pins)	
PI0/$\overline{\text{INT0}}$	I/O/Input	(Port I) 8-bit I/O port. I/O can be set in a unit of single bits. Function as standby release input can be set in a unit of single bits. (8 pins)	Input pin to request external interruption. Active when falling edge.
PI1/$\overline{\text{EC}}$/ $\overline{\text{INT2}}$	I/O/Input/Input		External event input pin for timer/counter. Input pin to request external interruption. Active when falling edge.
PI2 to PI7	I/O		
CFG	Input	Capstan FG input pin.	
DFG	Input	Drum FG input pin.	
DPG	Input	Drum PG input pin.	
RECCTL (+) RECCTL (−)	I/O	RECCTL signal output pin. (2 pins)	PBCTL signal input pin. (2 pins)
CTLCIN (+) CTLCIN (−)	Output	Connected to RECCTL (+) and RECCTL (−) with the internal switch for playback. (2 pins)	
CTLAMP (+) CTLAMP (−)	Input	Input PBCTL signal with capacitor coupled. (2 pins)	
CTLFAMPO	Output	PBCTL signal 1st amplifier output.	
CTLSAMPI	Input	PBCTL signal 2nd amplifier input.	
RECCAP	I/O	Capacitor connecting pin for the slope setting of the CTL writing trapezoidal wave.	
VREFOUT	Output	Capacitor connecting pin for the VREF level smoothing of DPG, DFG and CFG.	
CTLAG	Output	Capacitor connecting pin for the CTL and AGND smoothing.	
AMPV$_{SS}$		Analog signal input circuit GND pin.	
AMPV$_{DD}$		Analog signal input circuit power supply pin.	

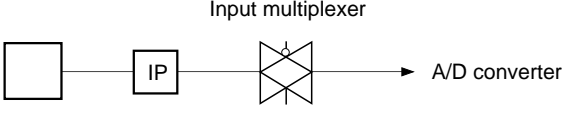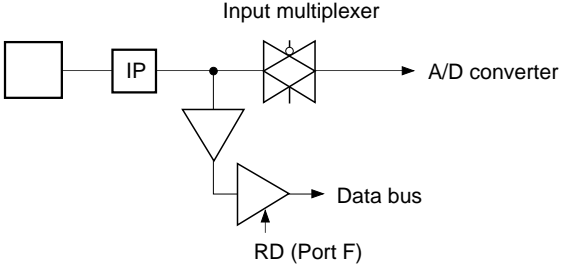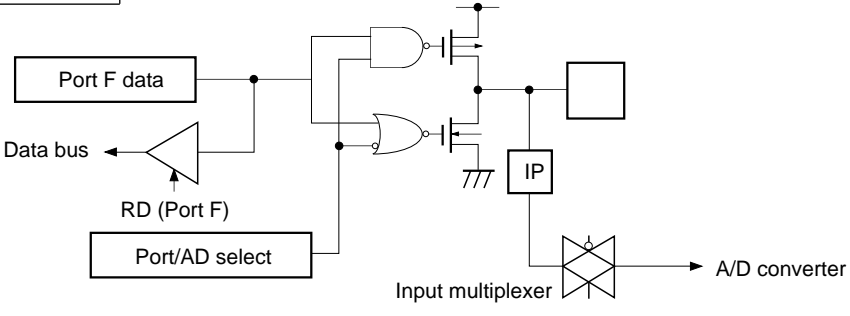| Symbol	I/O	Description
EXTAL	Input	Connecting pin of crystal oscillator for system clock. When supplying the external clock, input it to EXTAL pin and input the opposite phase clock to XTAL pin.
XTAL	Output	
TEX	Input	Connecting pin of crystal oscillator for 32kHz timer clock. When used as event counter, input to TEX pin and leave TX pin open.
TX	Output	(In this time, feedback resistor is not removed.)
$\overline{\text{RST}}$	Input	System reset pin; Low level active.
NC		NC pin. Connect this pin to V_{DD} for normal operation.
MP	Input	Test mode input pin. Always connect to GND.
AV_{DD}		Positive power supply pin for A/D converter.
AV_{REF}	Input	Reference voltage input pin for A/D converter.
AV_{SS}		GND pin for A/D converter.
V_{DD}		Positive power supply pin.
V_{SS}		GND pin. Connect both Vss pins to GND.

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/PPO0/ HGO 1 pin	Port A	Hi-Z
PA1/PPO1 1 pin		Hi-Z
PA2/PPO2 to PA7/PPO7 6 pins	Port A	Hi-Z
PB0/PPO8 to PB7/PPO15 8 pins	Port B	Hi-Z

Port A (PA0/PPO0/HGO, PA1/PPO1):

HOUT → MPX
PPO0
PA0
Data bus ← RD (Port A)
HSEL → MPX
HOUTE
Output becomes active from high impedance by data writing to port.
PPO1
PPG control status register bit 0
Tri-state control selection
PPO1
PA1
Data bus ← RD (Port A)
Output becomes active from high impedance by data writing to port.

Port A (PA2/PPO2 to PA7/PPO7):

PPO data
Port A data
Data bus ← RD (Port A)
Output becomes active from high impedance by data writing to port.

Port B (PB0/PPO8 to PB7/PPO15):

PPO data
Port B data
Data bus ← RD (Port B)
Port B tri-state control

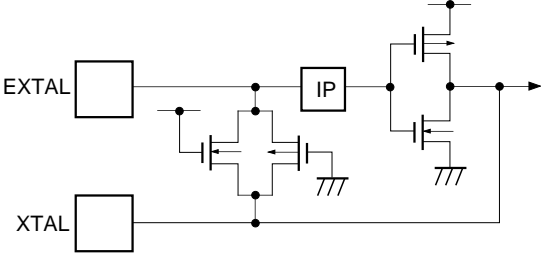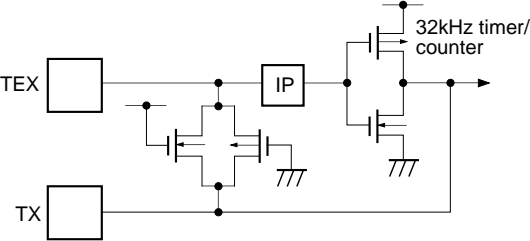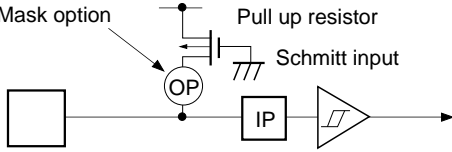| Pin	Circuit format	When reset
PC0/PPO16 to PC2/PPO18 PC3/RTO3 to PC7/RTO7 8 pins	**Port C** PPO, RTO data Port C data Port C direction Input protection circuit IP Data bus RD (Port C) RD (Port C direction)	Hi-Z
PD0/INT1/NMI PD1/RMC PD4/CS0 PD7/SI0 4 pins	**Port D** Port D data Port D direction IP Data bus RD (Port D) Schmitt input PD1: Remote control circuit PD0: Interruption circuit PD4, 7: Serial CH0	Hi-Z
PD2/PWM PD3/TO/ DDO/ADJ/ SRVO 2 pins	**Port D** Port D function select PD2: 14-bit PWM PD3: Timer/counter, CTL duty detection circuit, 32kHz timer, amplifier circuit MPX Port D data Port D direction IP Data bus RD (Port D)	Hi-Z

Pin	Circuit format	When reset
PD5/$\overline{SCK0}$ PD6/SO0 2 pins	**Port D** Port D function select / SIO CH0 / Port D data / Port D direction / MPX / MPX / IP Note) PD5 is schmitt input / PD6 is inverter input Data bus / RD (Port D) / SIO CH0	Hi-Z
PE0/$\overline{SCK1}$ 1 pin	**Port E** Port/SCK output select / SIO CH1 / Port E data / MPX / Hi-Z control / IP Data bus / RD (Port E) / SIO CH1	Hi-Z
PE1/SO1 1 pin	**Port E** Port E function select / SIO CH1 / Port E data / MPX / Hi-Z control Data bus / RD (Port E)	Hi-Z
PE2/SI1 PE3/SYNC PE4/EXI0 PE5/EXI1 4 pins	**Port E** Schmitt input / IP / PE2: SIO CH1 / PE3 PE4 PE5 Servo input / Data bus / RD (Port E) Note) For PE3/SYNC, CMOS schmitt input or TTL schmitt input can be selected with the mask oprion.	Hi-Z

Pin	Circuit format	When reset
PE6/PWM0/ DAA0 PE7/PWM1/ DAA1 2 pins	**Port E** — Port/DA/PWM select; DA gate output or PWM output; MPX; Port E data; Data bus; RD (Port E); Hi-Z control	High level
AN0/ANOUT 1 pin	**Port E** — Input multiplexer; IP; A/D converter; From amplifier circuit; Analog output control	Hi-Z
AN1 to AN3 3 pin	Input multiplexer; IP; A/D converter	Hi-Z
PFO/AN4 to PF3/AN7 4 pins	**Port F** — Input multiplexer; IP; A/D converter; Data bus; RD (Port F)	Hi-Z
PF4/AN8 to PF7/AN11 4 pins	**Port F** — Port F data; Data bus; RD (Port F); Port/AD select; IP; Input multiplexer; A/D converter	Hi-Z

Pin	Circuit format	When reset
PG0/AN12 to PG1/AN13 2 pins	**Port G**	Hi-Z
PH0 to PH7 8 pins	**Port H**	Hi-Z
PI0/INT0 to PI1/EC/INT2 2 pins	**Port I**	Hi-Z
PI2 to PI7 6 pins	**Port I**	Hi-Z

Pin	Circuit format	When reset
CTLAMP (+) CTLAMP (−) CTLFAMPO 3 pins		1/2AMPV$_{DD}$
CTLSAMPI 1 pin		1/2AMPV$_{DD}$
CFG DFG DPG 3 pins		1/2AMPV$_{DD}$
CTLAG VREFOUT 2 pins		1/2AMPV$_{DD}$

Pin	Circuit format	When reset
RECCTL (+) 1 pin		Hi-Z
RECCTL (−) 1 pin		Hi-Z
CTLCIN (+) 1 pin		Hi-Z
CTLCIN (−) 1 pin		Hi-Z
RECCAP 1 pin		Low level

Pin	Circuit format	When reset
EXTAL XTAL 2 pins	EXTAL — IP XTAL ∗ Shows the circuit composition during oscillation. ∗ Feedback resistor is removed and XTAL outputs High level during stop.	Oscillation
TEX TX 2 pins	TEX — IP — 32kHz timer/counter TX ∗ Shows the circuit composition during oscillation. ∗ Feedback resistor is removed during 32kHz oscillation circuit stop by software. At this time, TEX pin outputs Low level and TX pin outputs High level.	Oscillation
$\overline{\text{RST}}$ 1 pin	Mask option — Pull up resistor OP — Schmitt input IP	Low level

Absolute Maximum Ratings   (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	−0.3 to +7.0	V	
	AV_{DD}	AVss to +7.0[*1]	V	
	AV_{SS}	−0.3 to +0.3	V	
	$AMPV_{DD}$	AMPVss to +7.0[*2]	V	
	$AMPV_{SS}$	−0.3 to +0.3	V	
Input voltage	V_{IN}	−0.3 to +7.0[*3]	V	
Output voltage	V_{OUT}	−0.3 to +7.0[*3]	V	
Medium drive output voltage	V_{OUTP}	−0.3 to +15.0	V	Port H
High level output current	I_{OH}	−5	mA	
High level total output current	ΣI_{OH}	−50	mA	Total of output pins
Low level output current	I_{OL}	15	mA	Other than large current output ports (value per pin)
	I_{OLC}	20	mA	Large current output port[*4] (value per pin)
Low level total output current	ΣI_{OL}	130	mA	Total of output pins
Operating temperature	Topr	−20 to +75	°C	
Storage temperature	Tstg	−55 to +150	°C	
Allowable power dissipation	P_D	600	mW	QFP package type

[*1] AV_{DD} and V_{DD} must not exceed +0.3V.

[*2] $AMPV_{DD}$ and V_{DD} must not exceed +0.3V.

[*3] V_{IN} and V_{OUT} must not exceed V_{DD} +0.3V.

[*4] The large current output port is port H (PH).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should better take place under the recommended operating conditions. Exceeding those conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range for 1/2 and 1/4 frequency dividing clock
		3.5	5.5		Guaranteed operation range for 1/16 frequency dividing clock or during SLEEP mode
		2.7	5.5		Guaranteed operation range by TEX clock
		2.5	5.5		Guaranteed data hold operation range during STOP
Analog power supply	AV_{DD}	4.5	5.5	V	[1]
	$AMPV_{DD}$	4.5	5.5	V	[2]
High level input voltage	V_{IH}	$0.7V_{DD}$	V_{DD}	V	[3]
	V_{IHS}	$0.8V_{DD}$	V_{DD}	V	CMOS schmitt input[4]
	V_{IHTS}	2.2	V_{DD}	V	TTL schmitt input[5]
	V_{IHEX}	$V_{DD} - 0.4$	$V_{DD} + 0.3$	V	EXTAL pin[6] TEX pin[7]
Low level input voltage	V_{IL}	0	$0.3V_{DD}$	V	[3]
	V_{ILS}	0	$0.2V_{DD}$	V	CMOS schmitt input[4]
	V_{ILTS}	0	0.8	V	TTL schmitt input[5]
	V_{ILEX}	−0.3	0.4	V	EXTAL pin[6] TEX pin[7]
Operating temperature	Topr	−20	+75	°C	

[1] AV_{DD} and V_{DD} should be set to the same voltage.

[2] $AMPV_{DD}$ and V_{DD} should be set to the same voltage.

[3] Normal input port (each pin of PC, PD2, PD3, PD6, PF0 to PF3, PG and PI2 to PI7), MP pin

[4] Each pin of $\overline{RST}$, PD0/$\overline{INT1}$/$\overline{NMI}$, PD1/RMC, PD4/$\overline{CS0}$, PD5/SCK0, PD7/SI0, PE0/$\overline{SCK1}$, PE2/SI1, PE3/SYNC, PE4/EXI0, PE5/EXI1, PI0/$\overline{INT0}$, PI1/$\overline{EC}$/$\overline{INT2}$ (For PE3/SYNC, when CMOS schmitt input is selected with mask option.)

[5] PE3/SYNC (when TTL schmitt input is selected with mask option.)

[6] Specifies only during external clock input.

[7] Specifies only during external event input.

Electrical Characteristics

DC Characteristics (V_{DD} = 4.5 to 5.5V)   (Ta = −20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V_{OH}	PA to PD, PE0 to PE1, PE6 to PE7, PF4 to PF7, PH (V_{OL} only) PI	V_{DD} = 4.5V, I_{OH} = −0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = −1.2mA	3.5			V
Low level output voltage	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PH	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.5		−40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IH} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	−0.1		−10	µA
	I_{ILR}	$\overline{RST}$[1]		−1.5		−400	µA
I/O leakage current	I_{IZ}	PA to PG, PI, MP, AN0 to AN3, $\overline{RST}$[1]	V_{DD} = 5.5V, V_I = 0, 5.5V			±10	µA
Open drain output leakage current (N-CH Tr off state)	I_{LOH}	PH	V_{DD} = 5.5V V_{OH} = 12V			50	µA
Supply current[2]	I_{DD1}	V_{DD}, Vss	16MHz crystal oscillation (C_1 = C_2 = 15pF) V_{DD} = 5.5V[3]		35	45	mA
	I_{DDS1}		SLEEP mode V_{DD} = 5.5V		2.0	8	mA
	I_{DD2}		32kHz crystal oscillation (C_1 = C_2 = 47pF) V_{DD} = 3.3V		50	100	µA
	I_{DDS2}		SLEEP mode V_{DD} = 3V ± 0.3V		9	35	µA
	I_{DDS3}		STOP mode (EXTAL and TEX pins oscillation stop) V_{DD} = 5V±0.5V			10	µA
Input capacity	C_{IN}	PC, PD, PE0, PE2 to PE5 PF, PG, PI, RECCTL (+), RECCTL (−), CTLAMP (+), CTLAMP (−), CTLSAMPI, CFG, DFG, DPG, EXTAL, TEX	Clock 1MHz 0V other than the measured pins		10	20	pF

[1] $\overline{RST}$ pin specifies the input current when the pull-up resistor is selected, and specifies leakage current when no resistor is selected.

[2] When entire output pins are open.

[3] When setting upper 2 bits (CPU clock selection) of clock control register (CLC: 00FE$_H$) to "00" and operating in high speed mode (1/2 frequency dividing clock).

AC Characteristics

(1) Clock timing   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		16	MHz
System clock input pulse width	t_{XL}, t_{XH}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive	28			ns
System clock input rise and fall times	t_{CR}, t_{CF}	XTAL EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count clock input pulse width	t_{EH}, t_{EL}	$\overline{EC}$	Fig. 3	t_{sys} + 200[1]			ns
Event count clock input rise and fall times	t_{ER}, t_{EF}	$\overline{EC}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count clock input pulse width	t_{TL}, t_{TH}	TEX	Fig. 3	10			μs
Event count clock input rise and fall times	t_{TR}, t_{TF}	TEX	Fig. 3			20	ms

[1] t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FEH) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")
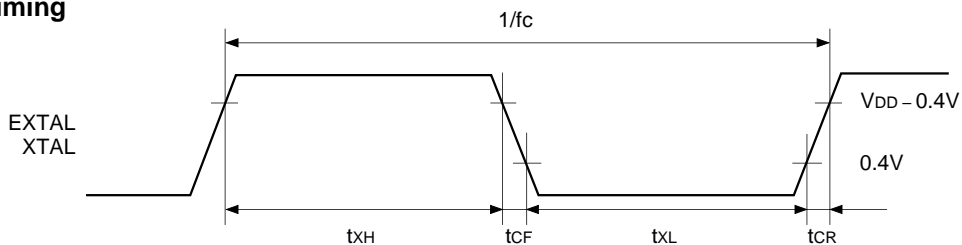
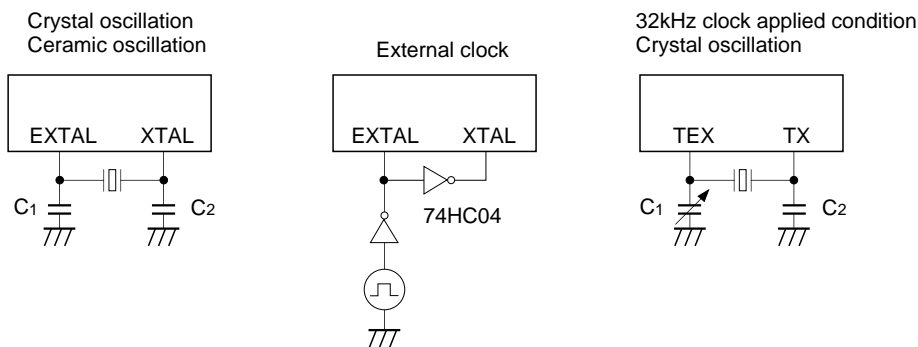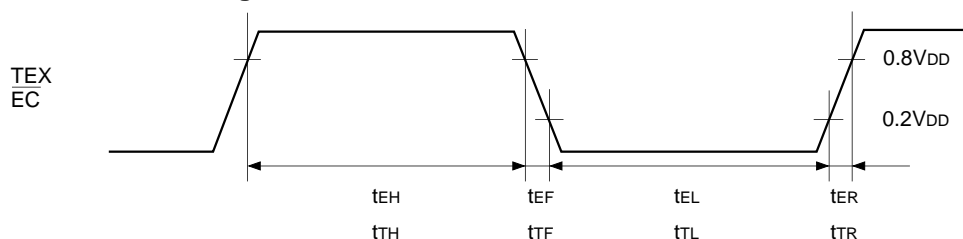### Fig. 1. Clock timing

Fig. 2. Clock applied condition

Fig. 3. Event count clock timing

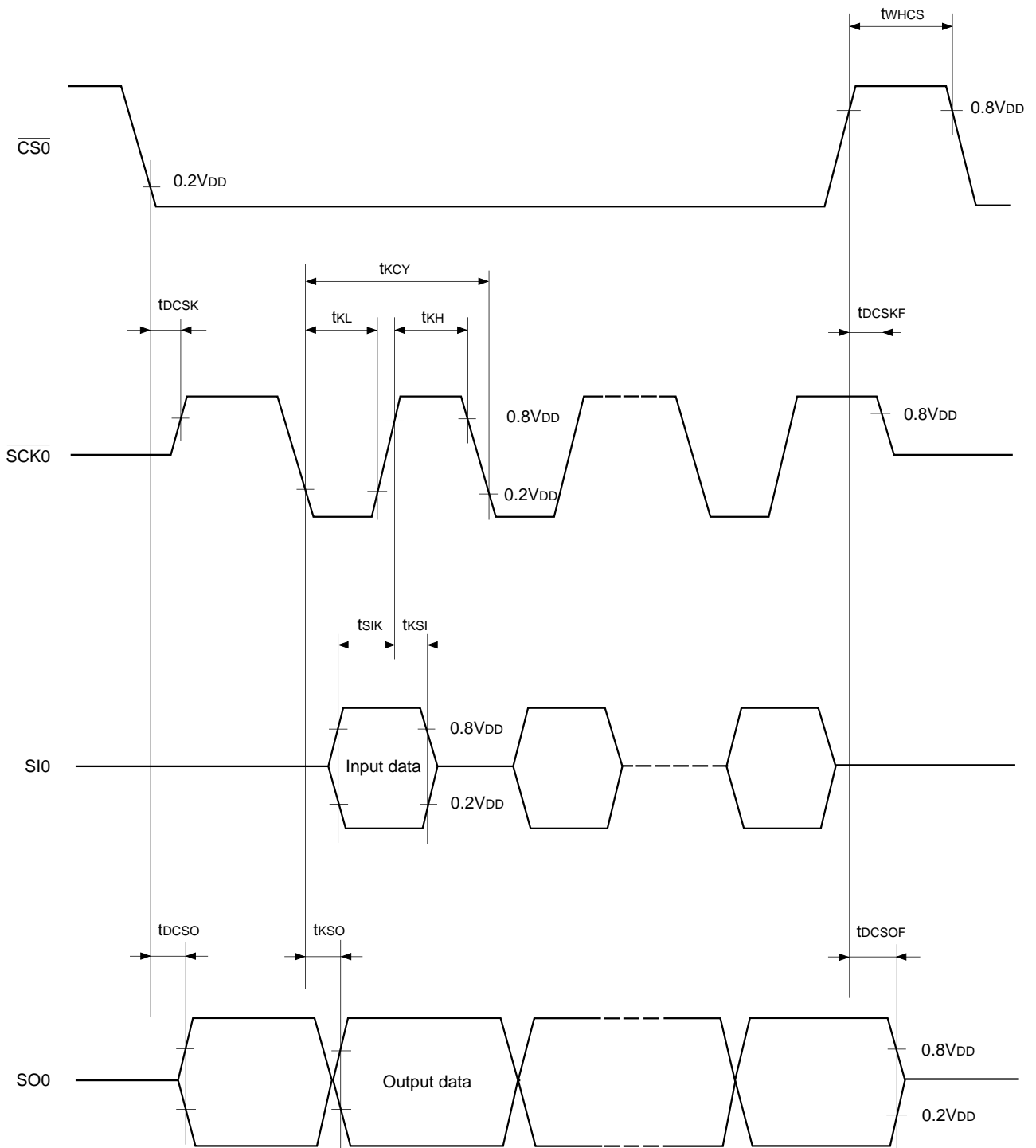**(2) Serial transfer (CH0)**   (Ta = −20 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t_{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ floating delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		t_{sys} + 200	ns
$\overline{CS0} \downarrow \rightarrow SO0$ delay time	t_{DCSO}	SO0	Chip select transfer mode		t_{sys} + 200	ns
$\overline{CS0} \uparrow \rightarrow SO0$ floating delay time	t_{DCSOF}	SO0	Chip select transfer mode		t_{sys} + 200	ns
$\overline{CS0}$ high level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	t_{sys} + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2t_{sys} + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ high and low level widths	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	t_{sys} + 100		ns
			Output mode	8000/fc − 50		ns
SI0 input set-up time (against $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (against $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	t_{sys} + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow SO0$ delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		t_{sys} + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) t_{sys} indicates three values according to the contents of the clock control register (CLC; 00FE$_H$) upper 2 bits (CPU clock selection).

t_{sys} [ns] = 2000/fc (Upper 2 bits = "00"), 4000/fc (Upper 2 bits = "01"), 16000/fc (Upper 2 bits = "11")

Note 2) The load of $\overline{SCK0}$ output mode and SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer timing (CH0)

Serial transfer (CH1) (Ta = −20 to +75°C, V$_{DD}$ = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.
$\overline{SCK1}$ cycle time	t$_{KCY}$	$\overline{SCK1}$	Input mode	1000	
			Output mode	16000/fc	
$\overline{SCK1}$ high and low level widths	t$_{KH}$ t$_{KL}$	$\overline{SCK1}$	Input mode	400	
			Output mode	8000/fc − 50	
SI1 input set-up time (against $\overline{SCK1}$ ↑)	t$_{SIK}$	SI1	$\overline{SCK1}$ input mode	100	
			$\overline{SCK1}$ output mode	200	
SI1 input hold time (against $\overline{SCK1}$ ↑)	t$_{KSI}$	SI1	$\overline{SCK1}$ input mode	200	
			$\overline{SCK1}$ output mode	100	
$\overline{SCK1}$ ↓ → SO1 delay time	t$_{KSO}$	SO1	$\overline{SCK1}$ input mode		200
			$\overline{SCK1}$ output mode		100

Note) The load of $\overline{SCK1}$ output mode and SO1 output delay time is 50pF + 1TTL.
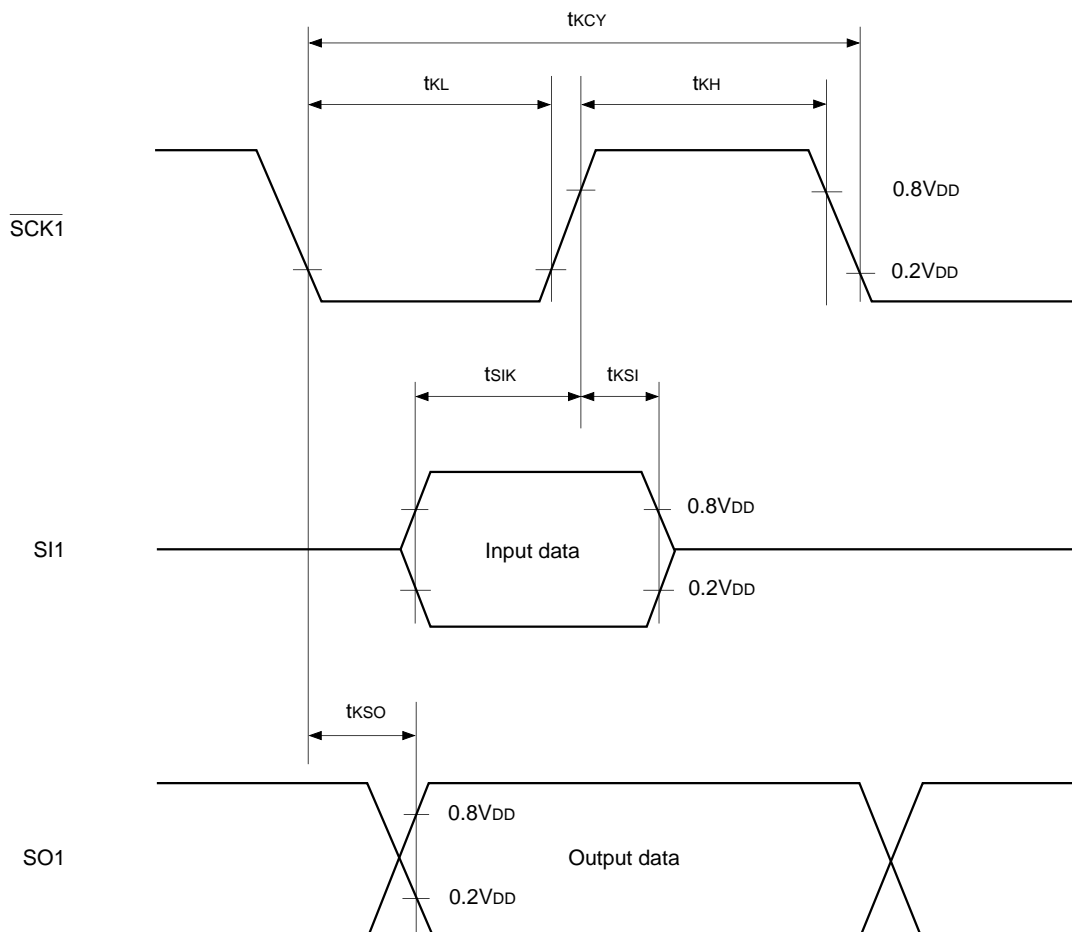
Fig. 5. Serial transfer timing (CH1)

(3) A/D converter characteristics

(Ta = −20 to +75°C, VDD = AVDD = 4.5 to 5.5V, AVREF = 4.0 to AVDD, Vss = AVss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C VDD = AVDD = AVREF = 5.0V VDD = AVss = 0V			±1	LSB
Absolute error						±2	LSB
Conversion time	t_{CONV}			160/f_{ADC} [*1]			μs
Sampling time	t_{SAMP}			12/f_{ADC} [*1]			μs
Reference input voltage	V_{REF}	AVREF		AVDD − 0.5		AVDD	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AVREF	V
AVREF current	I_{REF}	AVREF	Operation mode		0.6	1.0	mA
			SLEEP mode STOP mode 32kHz operation mode			10	μA

Fig. 6. Definitions of A/D converter terms

[*1] f_{ADC} indicates the below values due to the contents of bit 0 (ADCCK) of the ADC operation clock selection register (MSC: 01FFH), bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: 00FEH).

ADCCK \ PCK1, PCK0	0 (φ/2 selection)	1 (φ selection)
00 (φ = fEX/2)	f_{ADC} = fc/2	f_{ADC} = fc
01 (φ = fEX/4)	f_{ADC} = fc/4	f_{ADC} = fc/2
11 (φ = fEX/16)	f_{ADC} = fc/16	f_{ADC} = fc/8

(4) Interruption, reset input (Ta = –20 to +75°C, V$_{DD}$ = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption high and low level widths	t$_{IH}$ t$_{IL}$	$\overline{INT0}$ $\overline{INT1}$ $\overline{INT2}$ $\overline{NMI}$		1		µs
Reset input low level width	t$_{RSL}$	$\overline{RST}$		32/fc		µs

Fig. 7. Interruption input timing

$\overline{INT0}$
$\overline{INT1}$
$\overline{INT2}$
$\overline{NMI}$
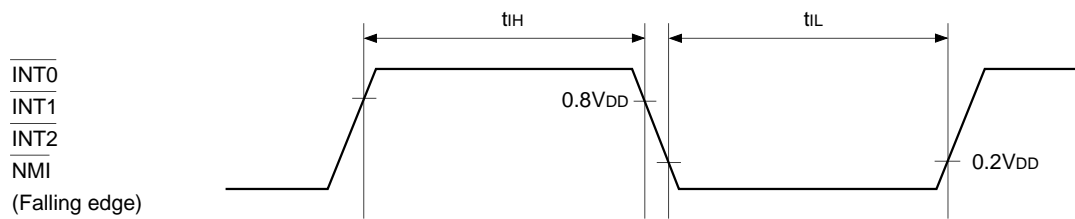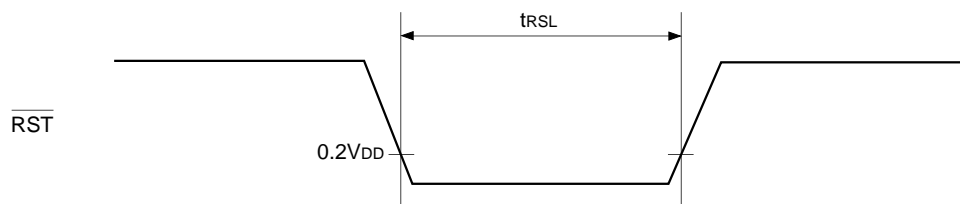(Falling edge)

Fig. 8. Reset input timing

$\overline{RST}$

Analog Circuit Characteristics

(1) Amplifier circuit reference voltage characteristics

(Ta = −20 to +75°C, V_{DD} = AMPV$_{DD}$ = 5.0V, Vss = AMPVss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Reference level output voltage	V_{OR}	VREFOUT		2.2	2.4	2.6	V
		CTLAG		2.15	2.35	2.55	V
Reference level output current	I_{OR}	VREFOUT	VREFOUT = VREFOUT + 0.5V	3.50	6.5		mA
			VREFOUT = VREFOUT − 0.5V	−0.30	−0.85		mA
		CTLAG	CTLAG = CTLAG + 0.5V	2.80	5.5		mA
			CTLAG = CTLAG − 0.5V	−0.30	−0.85		mA

(2) CTL 1st amplifier characteristics

(Ta = −20 to +75°C, V_{DD} = AMPV$_{DD}$ = 5.0V, Vss = AMPVss = 0V, CTLAG reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Voltage gain [1]	A_{VCTL1}	RECCTL (+) CTLFAMPO[2]	Gain = 16dB RECCTL (−) = 0V	12.5	14.5	16.5	dB
			Gain = 27dB RECCTL (−) = 0V	23.5	25.5	27.5	dB
			Gain = 42dB RECCTL (−) = 0V	39.0	41.5	44.0	dB
			Gain = 58dB RECCTL (−) = 0V	54.5	57.0	59.5	dB
Offset voltage	V_{OSCTL1}		CTLAMP (+) and CTLAMP (−) = open	−40	0	+40	mV
Input resistance	R_{INCTL1}	CTLAMP (+)	Charge switch OFF CTLAMP (+) = +0.2V	26.0	44.5		kΩ
		CTLAMP (−)	Charge switch OFF CTLAMP (−) = +0.2V	1.20	2.0		kΩ
Charge switch ON resistance	R_{CCTL1}	CTLAMP (+)	Charge switch ON CTLAMP (+) = +0.5V		560	1010	Ω
		CTLAMP (−)	Charge switch ON CTLAMP (−) = +0.5V		560	1010	Ω
RECCTL and CTLCIN connection switch ON resistance	R_{READ}	RECCTL (+) CTLCIN (+)	During CTL read operation, CTLCIN (+) − RECCTL (+) = 0.2V	315	400	770	Ω
		RECCTL (−) CTLCIN (−)	During CTL read operation, CTLCIN (−) − RECCTL (−) = 0.2V	315	400	770	Ω
CTLCIN 0V fix switch ON resistance	R_{WRITE}	CTLCIN (+)	During CTL write operation, CTLCIN (+) = AMPVss + 0.2V		250	310	Ω
		CTLCIN (−)	During CTL write operation, CTLCIN (−) = AMPVss + 0.2V		250	310	Ω

[1] When CTLCIN (+), CTLAMP (+) pins and CTLCIN (−), CTLAMP (−) pins are AC coupled, and then the signal is input from RECCTL (+) pin.

[2] The result after measuring output waveform of CTLFAMPO pin or voltage value.

Note) The gain increases by approximately 1.5dB when the AC coupling capacitor (47μF) is connected to CTLAMP (+) and CTLAMP (−) pins, and the signal is input from CTLAMP (+) and CTLAMP (−) pins.

(3) CTL 2nd amplifier characteristics

(Ta = −20 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, Vss = $AMPV_{SS}$ = 0V, CTLAG reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Voltage gain[*1, *2]	A_{VCTL2}		Gain = 5dB	4.8	5.8	6.8	dB
			Gain = 11dB	10.4	11.5	12.6	dB
			Gain = 16dB	15.3	16.5	17.7	dB
			Gain = 20dB	19.3	20.5	21.7	dB
LPF cut-off frequency[*1, *2]	f_{CCTL}		f_{DC} − 3dB	15.0	25.0	40.0	kHz
Offset voltage[*2]	V_{OSCTL2}	CTLSAMPI	CTLSAMPI = open	−50	0	+50	mV
Comparator level[*2]	V_{CCTL}		Comparator level = +100mV0-p	70.0	100	130	mV0-p
			Comparator level = +250mV0-p	215	245	275	mV0-p
			Comparator level = +400mV0-p	370	400	430	mV0-p
			Comparator level = −100mV0-p	−70.0	−100	−130	mV0-p
			Comparator level = −250mV0-p	−220	−250	−280	mV0-p
			Comparator level = −400mV0-p	−370	−400	−430	mV0-p
Input resistance	R_{INCTL2}		Charge switch OFF CTLSAMPI = +0.2V	10.0	18.0		kΩ
Charge switch ON resistance	R_{CCTL2}		Charge switch ON CTLSAMPI = +0.5V		770	1140	Ω

[*1] When the signal is input with the AC coupling capacitor (47μF) connected to CTLSAMPI pin.

[*2] The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

(4) CTLAMP characteristics (1st amplifier + 2nd amplifier)

(Ta = −20 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, Vss = $AMPV_{SS}$ = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
Voltage gain[*1]	A_{VCTL}		CTL 1st amplifier gain = 16dB CTL 2nd amplifier gain = 20dB RECCTL (−) = 0V	31.8	35.0	38.2	dB
Input amplitude (peak value)	V_{PKCTL}	RECCTL (+)	RECCTL (−) = 0V			±300	mV0-p
Input sensitivity	V_{SCTL}		CTL 1st amplifier gain = 58dB CTL 2nd amplifier gain = 20dB Comparator level = +400mV0-p −400mV0-p		0.08	0.10	mV0-p
Input dead band	V_{NSCTL}		RECCTL (−) = 0V	0.015	0.04		mV0-p

[*1] As for other combinations of the amplifier gains, CTL 1st amplifier and CTL 2nd amplifier are added respectively.

Note) The result when the signal is input from RECCTL (+) pin with CTL 1st amplifier + CTL 2nd amplifier after performing AC coupling of CTLCIN (+), CTLAMP (+) pins and CTLCIN (−), CTLAMP (−) pins, and CTLFAMPO, CTLSAMPI pins.

(5) CFGAMP characteristics

(Ta = −20 to +75°C, V$_{DD}$ = AMPV$_{DD}$ = 5.0V, Vss = AMPV$_{DD}$ = 0V, VREFOUT reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain[1], [2]	A$_{VCFG}$		Gain = 0dB	−0.3	0.6	2.2	dB
			Gain = 20dB	19.2	20.8	22.4	dB
			Gain = 34dB	33.2	34.8	36.4	dB
			Gain = 38dB	37.0	38.7	40.4	dB
LPF cut-off frequency[1], [2]	f$_{CCFG}$		f$_{DC}$ − 3dB	30.0	55.0	80.0	kHz
Offset voltage[2]	V$_{OSCFG}$		CFG = open	−50	0	+50	mV
Comparator judgment level width[2]	V$_{CCFG}$		Comparator schimitt width = 320mVp-p	260	320	360	mVp-p
			Comparator schimitt width = 160mVp-p	110	155	200	mVp-p
Input sensitivity[1]	V$_{SCFG}$	CFG	Gain = 38dB Comparator level = 320mVp-p		4.20	5.00	mVp-p
			Gain = 38dB Comparator level = 160mVp-p		2.10	2.40	mVp-p
Input dead band[1]	V$_{NSCFG}$		Gain = 38dB Comparator level = 320mVp-p	3.40	4.10		mVp-p
			Gain = 38dB Comparator level = 160mVp-p	1.50	2.00		mVp-p
Input resistance	R$_{INCFG}$		Charge switch OFF CFG = +0.2V	5.5	8.3		kΩ
Charge switch ON resistance	R$_{CCFG}$		Charge switch ON CFG = +0.5V		455	710	Ω
Digital output waveform duty[1], [3]	D$_{TYCFG}$		CFG = sine wave with 50% duty	48.0	50.0	52.0	%
Input amplitude (peak value)[1]	V$_{PKCFG}$					±2.4	V$_{0}$-p

[1] When the signal is input with the AC coupling capacitor (47μF) connected to CFG pin.

[2] The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

[3] The result after measuring the digital signal waveform output from the amplifier circuit.

(6) DFGAMP characteristics

(Ta = −20 to +75°C, V_{DD} = AMPV$_{DD}$ = 5.0V, Vss = AMPVss = 0V, VREFOUT reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain[*1], [*2]	A$_{VDFG}$		Gain = 0dB	−0.3	0.6	2.2	dB
			Gain = 20dB	19.2	20.8	22.4	dB
			Gain = 34dB	33.2	34.8	36.4	dB
			Gain = 38dB	37.0	38.7	40.4	dB
LPF cut-off frequency[*1], [*2]	f$_{CDFG}$		f$_{DC}$ − 3dB	30.0	55.0	80.0	kHz
Offset voltage[*2]	V$_{OSDFG}$		DFG = open	−50	0	+50	mV
Comparator judgment level width[*2]	V$_{CDFG}$		Comparator schmitt width = 320mVp-p	260	320	360	mVp-p
		DFG	Comparator schmitt width = 160mVp-p	110	155	200	mVp-p
Input sensitivity[*1]	V$_{SDFG}$		Gain = 38dB Comparator level = 320mVp-p		4.20	5.00	mVp-p
			Gain = 38dB Comparator level = 160mVp-p		2.10	2.40	mVp-p
Input dead band[*1]	V$_{NSDFG}$		Gain = 38dB Comparator level = 320mVp-p	3.40	4.10		mVp-p
			Gain = 38dB Comparator level = 160mVp-p	1.50	2.00		mVp-p
Input resistance	R$_{INDFG}$		Charge switch OFF DFG = +0.2V	5.5	8.3		kΩ
Charge switch ON resistance	R$_{CDFG}$		Charge switch ON DFG = +0.5V		455	710	Ω
Digital output waveform duty[*1], [*3]	D$_{TYDFG}$		CFG = sine wave of 50% duty	48.0	50.0	52.0	%
Input amplitude (peak value)[*1]	V$_{PKDFG}$					±2.4	V$_0$-p

[*1] When the signal is input with the AC coupling capacitor (47µF) connected to DFG pin.

[*2] The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

[*3] The result after measuring the digital signal waveform output from the amplifier circuit.

(7) DPGAMP characteristics

(Ta = −20 to +75°C, V_{DD} = AMPV$_{DD}$ = 5.0V, Vss = AMPVss = 0V, VREFOUT reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Voltage gain[1], [2]	A$_{VDPG}$			11.1	12.0	13.2	dB
LPF cut-off frequency[1], [2]	f$_{CDPG}$		f$_{DC}$ − 3dB	30.0	55.0	85.0	kHz
Offset voltage[2]	V$_{OSDPG}$		DFG = open	−35	0	+35	mV
Comparator level[2]	V$_{CDPG}$		Comparator level = 600mV$_{0}$-p	570	605	640	mV$_{0}$-p
			Comparator level = 400mV$_{0}$-p	370	400	432	mV$_{0}$-p
			Comparator level = 200mV$_{0}$-p	175	200	220	mV$_{0}$-p
			Comparator level = 100mV$_{0}$-p	72	100	125	mV$_{0}$-p
			Comparator level = −600mV$_{0}$-p	−572	−605	−643	mV$_{0}$-p
			Comparator level = −400mV$_{0}$-p	−368	−400	−438	mV$_{0}$-p
			Comparator level = −200mV$_{0}$-p	−174	−200	−223	mV$_{0}$-p
			Comparator level = −100mV$_{0}$-p	−71	−100	−124	mV$_{0}$-p
Input sensitivity[1]	V$_{SDPG}$	DPG	Comparator level = 600mV$_{0}$-p, 200mV$_{0}$-p		150	180	mV$_{0}$-p
			Comparator level = 400mV$_{0}$-p, 100mV$_{0}$-p		100	120	mV$_{0}$-p
			Comparator level = −600mV$_{0}$-p, −200mV$_{0}$-p		−155	−185	mV$_{0}$-p
			Comparator level = −400mV$_{0}$-p, −100mV$_{0}$-p		−109	−130	mV$_{0}$-p
Input dead band[1]	V$_{NSDPG}$		Comparator level = 600mV$_{0}$-p, 200mV$_{0}$-p	113	142		mV$_{0}$-p
			Comparator level = 400mV$_{0}$-p, 100mV$_{0}$-p	70	90		mV$_{0}$-p
			Comparator level = −600mV$_{0}$-p, −200mV$_{0}$-p	−120	−150		mV$_{0}$-p
			Comparator level = −400mV$_{0}$-p, −100mV$_{0}$-p	−80	−103		mV$_{0}$-p
Input resistance	R$_{INDPG}$		Charge switch OFF DPG = +0.2V	24.0	44.5		kΩ
Charge switch ON resistance	R$_{CDPG}$		Charge switch ON DPG = +0.5V		450	860	Ω
Input amplitude (peak value)[1]	V$_{PKDPG}$					±2.4	V

[1] When the signal is input with the AC coupling capacitor (47µF) connected to DPG pin.

[2] The result after measuring the output waveform of amplifier internal low-pass filter or voltage value.

(8) CTL write circuit characteristics

(Ta = –20 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, V_{SS} = $AMPV_{SS}$ = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Output resistance	R_{OH}	RECCAP	RECCAP = $AMPV_{DD}$ – 0.5V	450	625	1005	Ω
	R_{OL}		RECCAP = $AMPV_{DD}$ + 0.5V	410	555	840	Ω
Output current[1]	I_{OREC}	RECCTL (+) RECCTL (–)	Write current = 2.0mA	1.3	2.0	2.9	mA
			Write current = 2.5mA	1.7	2.5	3.7	mA
			Write current = 3.0mA	2.1	3.1	4.5	mA
			Write current = 3.5mA	2.6	3.6	5.2	mA
			Write current = 4.0mA	2.9	4.0	5.9	mA
			Write current = 4.5mA	3.3	4.6	6.6	mA
			Write current = 5.0mA	3.7	5.1	7.2	mA
			Write current = 5.5mA	4.0	5.6	8.0	mA
			Write current = 6.0mA	4.4	6.1	8.9	mA

[1] The current value which flows when RECCTL (+) pin and RECCTL (–) pin are shorted.

(9) Amplifier operating current characteristics

(Ta = –20 to +75°C, V_{DD} = $AMPV_{DD}$ = 5.0V, V_{SS} = $AMPV_{SS}$ = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Amplifier operating current	I_{AMP}	$AMPV_{DD}$	When the amplifier is operating[1]		7.6	12.0	mA
			When the amplifier is not operating			10	µA

[1] The CTL recording current is added during CTL write.

Note) The amplifier operation and NOT-operation is controlled according to the contents of amplifier power supply control register (ASWC: 05E2H) bits 5, 4, 1 and 0.

Supplement

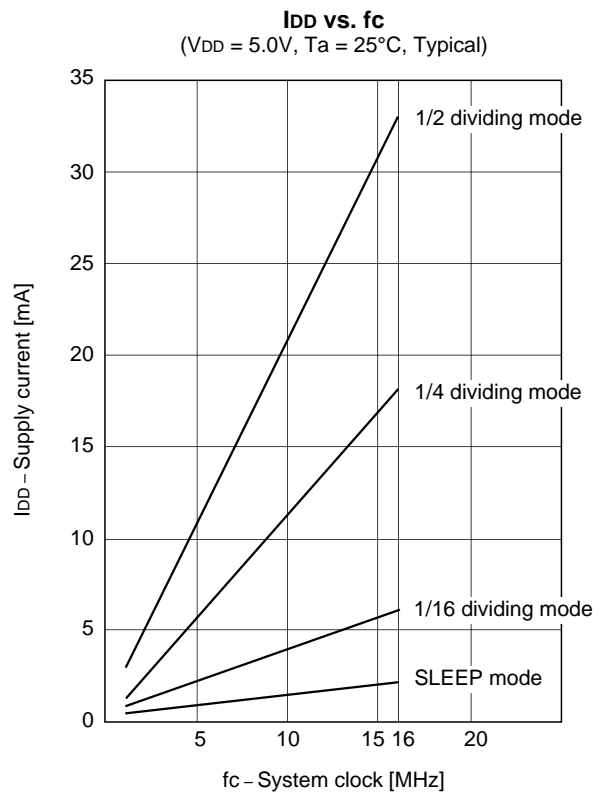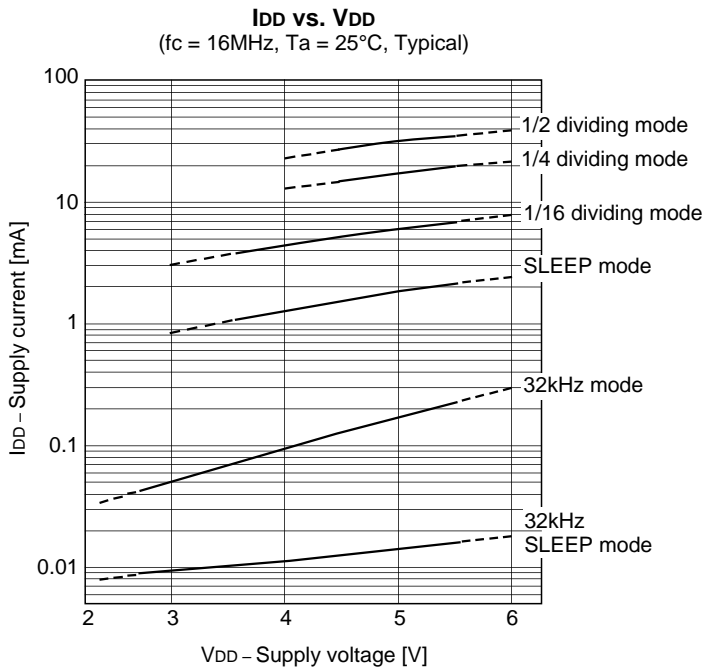**Fig. 9. Recommended oscillation circuit**

(i)   (ii)

Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
RIVER ELETEC CO., LTD.	HC-49/U03	8.00	10	10	0	(i)
		10.00				
		12.00	5	5		
		16.00				
KINSEKI LTD.	HC-49/U (-S)	8.00	16 (12)	16 (12)	0	(i)
		10.00	16 (12)	16 (12)		
		12.00	12	12		
		16.00	12	12		
	P3	32.768kHz	30	18	470k	(ii)

Mask option table

Item	Content	
Reset pin pull-up resistor	Non-existent	Existent
Input circuit format[*1]	CMOS schmitt	TTL schmitt

[*1] The input circuit format can be selected for PE3/SYNC pin.

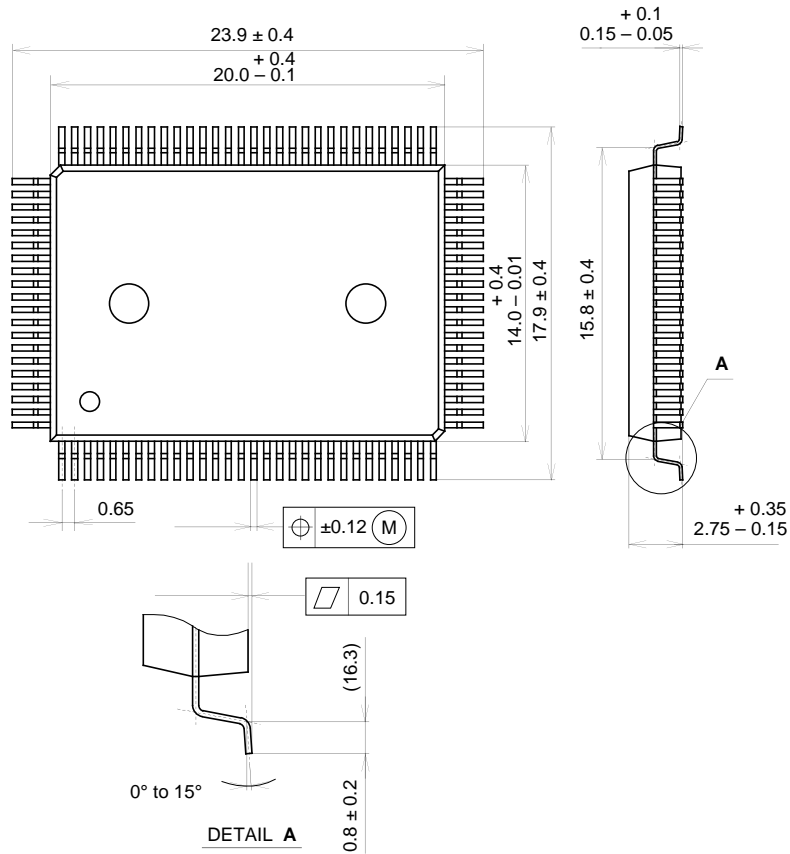## Characteristics Curve

I_DD vs. V_DD
(fc = 16MHz, Ta = 25°C, Typical)

I_DD vs. fc
(V_DD = 5.0V, Ta = 25°C, Typical)

Package Outline   Unit: mm

100PIN QFP (PLASTIC)

DETAIL **A**

0° to 15°

23.9 ± 0.4

20.0 $^{+0.4}_{-0.1}$

15.8 ± 0.4

0.15 $^{+0.1}_{-0.05}$

14.0 $^{+0.4}_{-0.01}$

17.9 ± 0.4

0.65

⊕ ±0.12 Ⓜ

2.75 $^{+0.35}_{-0.15}$

▱ 0.15

(16.3)

0.8 ± 0.2

SONY CODE	QFP-100P-L01
EIAJ CODE	∗QFP100-P-1420-A
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER / 42 ALLOY
PACKAGE WEIGHT	1.4g