M5M51008BFP,VP,RV,KV,KR -70VL,-10VL,-12VL,-15VL, -70VLL,-10VLL,-12VLL,-15VLL

1048576-BIT(131072-WORD BY 8-BIT)CMOS STATIC RAM

DESCRIPTION

The M5M51008BFP,VP,RV,KV,KR are a 1048576-bit CMOS static RAM organized as 131072 word by 8-bit which are fabricated using high-performance triple polysilicon CMOS technology. The use of resistive load NMOS cells and CMOS periphery result in a high density and low power static RAM.

They are low standby current and low operation current and ideal for the battery back-up application.

The M5M51008BVP,RV,KV,KR are packaged in a 32-pin thin small outline package which is a high reliability and high density surface mount device(SMD).Two types of devices are available. VP,KV(normal lead bend type package),RV,KR(reverse lead bend type package). Using both types of devices, it becomes very easy to design a printed circuit board.

FEATURES

Type name	Access time (max)	Vcc	Power supply current	
			Active (1MHz) (max)	stand-by (max)
M5M51008BFP,VP,RV,KV,KR-70VL	70ns	3.3±0.3V	10mA	60µA
M5M51008BFP,VP,RV,KV,KR-10VL	100ns			
M5M51008BFP,VP,RV,KV,KR-12VL	120ns	3.0±0.3V	10mA	55µA
M5M51008BFP,VP,RV,KV,KR-15VL	150ns			
M5M51008BFP,VP,RV,KV,KR-70VLL	70ns	3.3±0.3V	10mA	12µA
M5M51008BFP,VP,RV,KV,KR-10VLL	100ns			
M5M51008BFP,VP,RV,KV,KR-12VLL	120ns	3.0±0.3V	10mA	11µA
M5M51008BFP,VP,RV,KV,KR-15VLL	150ns			

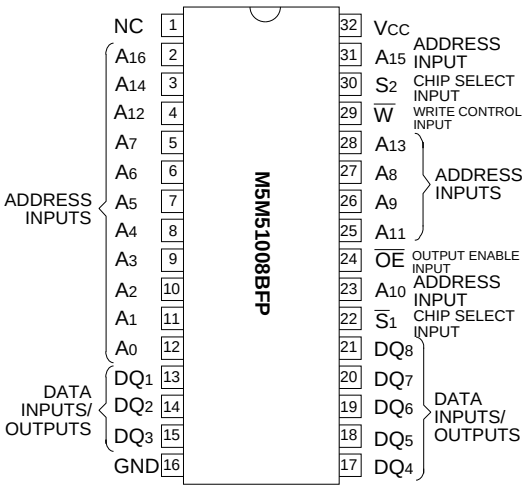
- Low stand-by current 0.3µA (typ.)
- Directly TTL compatible : All inputs and outputs
- Easy memory expansion and power down by $\overline{S}_1$,S_2
- Data hold on +2V power supply
- Three-state outputs : OR - tie capability
- OE prevents data contention in the I/O bus
- Common data I/O
- Package

  M5M51008BFP ·····32pin 525mil SOP
  M5M51008BVP,RV ·····32pin 8 X 20 mm² TSOP
  M5M51008BKV,KR ·····32pin 8 X 13.4 mm² TSOP

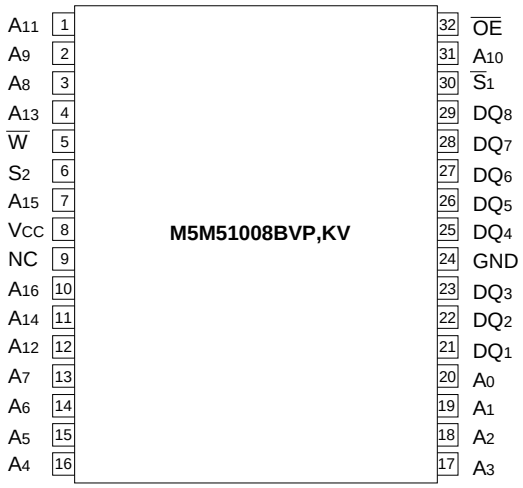
APPLICATION

Small capacity memory units

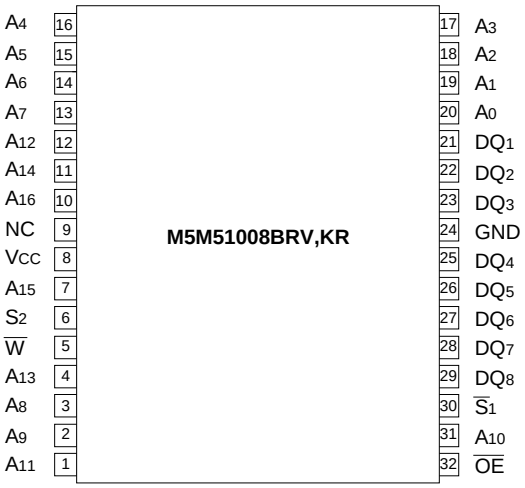
PIN CONFIGURATION (TOP VIEW)



Outline 32P2M-A



Outline 32P3H-E(VP), 32P3K-B(KV)



Outline 32P3H-F(RV), 32P3K-C(KR)

NC : NO CONNECTION

MITSUBISHI ELECTRIC

M5M51008BFP,VP,RV,KV,KR -70VL,-10VL,-12VL,-15VL, -70VLL,-10VLL,-12VLL,-15VLL

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FUNCTION

The operation mode of the M5M51008B series are determined by a combination of the device control inputs $\overline{S}_1$,S_2,$\overline{W}$ and $\overline{OE}$.

Each mode is summarized in the function table.

A write cycle is executed whenever the low level $\overline{W}$ overlaps with the low level $\overline{S}_1$ and the high level S_2. The address must be set up before the write cycle and must be stable during the entire cycle. The data is latched into a cell on the trailing edge of $\overline{W}$,$\overline{S}_1$ or S_2,whichever occurs first,requiring the set-up and hold time relative to these edge to be maintained. The output enable input $\overline{OE}$ directly controls the output stage. Setting the $\overline{OE}$ at a high level, the output stage is in a high-impedance state, and the data bus contention problem in the write cycle is eliminated.

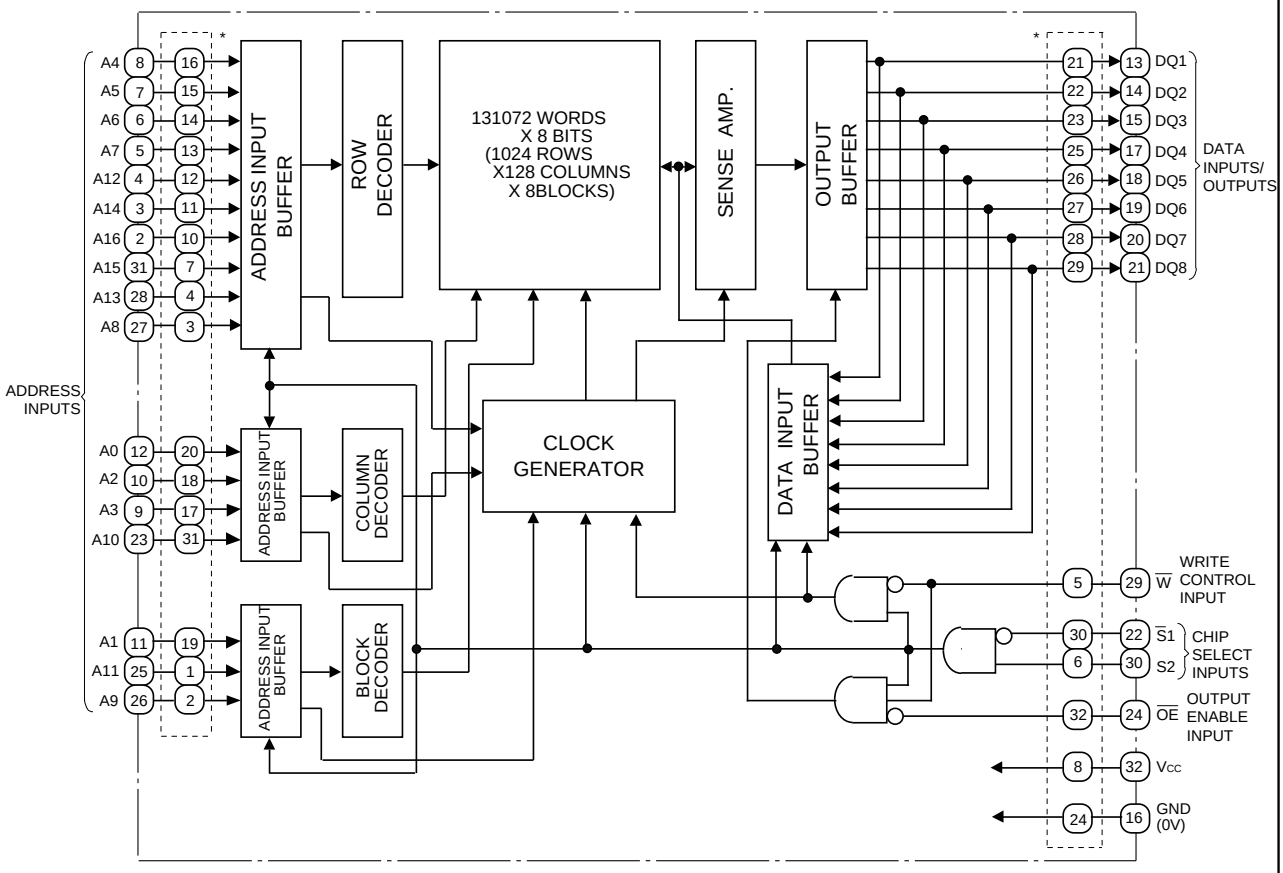
A read cycle is executed by setting $\overline{W}$ at a high level and $\overline{OE}$ at a low level while $\overline{S}_1$ and S_2 are in an active state($\overline{S}_1$=L,S_2=H).

When setting $\overline{S}_1$ at a high level or S_2 at a low level, the chip are in a non-selectable mode in which both reading and writing are disabled. In this mode, the output stage is in a high- impedance state, allowing OR-tie with other chips and memory expansion by $\overline{S}_1$ and S_2. The power supply current is reduced as low as the stand-by current which is specified as I_{CC3} or I_{CC4}, and the memory data can be held at +2V power supply, enabling battery back-up operation during power failure or power-down operation in the non-selected mode.

FUNCTION TABLE

$\overline{S}_1$	S_2	$\overline{W}$	$\overline{OE}$	Mode	DQ	I_{CC}
X	L	X	X	Non selection	High-impedance	Stand-by
H	X	X	X	Non selection	High-impedance	Stand-by
L	H	L	X	Write	Din	Active
L	H	H	L	Read	Dout	Active
L	H	H	H		High-impedance	Active

BLOCK DIAGRAM



* Pin numbers inside dotted line show those of TSOP

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Conditions	Ratings	Unit
V_{CC}	Supply voltage	With respect to GND	– 0.3*~4.6	V
V_I	Input voltage		– 0.3*~Vcc + 0.3 (Max 4.6)	V
V_O	Output voltage		0~Vcc	V
P_d	Power dissipation	Ta=25°C	700	mW
T_{opr}	Operating temperature		0~70	°C
T_{stg}	Storage temperature		– 65~150	°C

* –3.0V in case of AC (Pulse width ≤ 30ns)

DC ELECTRICAL CHARACTERISTICS (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions		Limits						Unit
				-70VL, -70VLL -10VL, -10VLL			-12VL, -12VLL -15VL, -15VLL			
				V_{CC}=3.3±0.3V			V_{CC}=3.0±0.3V			
				Min	Typ	Max	Min	Typ	Max	
V_{IH}	High-level input voltage			2.0		Vcc +0.3V	2.0		Vcc +0.3V	V
V_{IL}	Low-level input voltage			–0.3		0.6	–0.3		0.6	V
V_{OH1}	High-level output voltage 1	I_{OH}= –0.5mA		2.4			2.4			V
V_{OH2}	High-level output voltage 2	I_{OH}= –0.05mA		Vcc -0.5V			Vcc -0.5V			V
V_{OL}	Low-level output voltage	I_{OL}=2mA				0.4			0.4	V
I_I	Input current	V_I=0~Vcc				±1			±1	µA
I_O	Output current in off-state	$\overline{S}_1$=V_{IH} or S_2=V_{IL} or OE=V_{IH} $V_{I/O}$=0~V_{CC}				±1			±1	µA
I_{CC1}	Active supply current (Min cycle)	$\overline{S}_1$=V_{IL},S_2=V_{IH}, other inputs=V_{IH} or V_{IL} Output-open(duty 100%)			20	35		15	30	mA
I_{CC2}	Active supply current (1MHz)				3	10		3	10	
I_{CC3}	Stand-by current	1) S_2 ≤ 0.2V 2) $\overline{S}_1$ ≥ V_{CC}–0.2V, S_2 ≥ V_{CC}–0.2V other inputs=0~V_{CC}	-L			60			55	µA
			-LL			12			11	
I_{CC4}	Stand-by current	$\overline{S}_1$=V_{IH} or S_2=V_{IL}, other inputs=0~V_{CC}				0.33			0.33	mA

* –3.0V in case of AC (Pulse width ≤ 30ns)

CAPACITANCE (Ta=0~70°C, unless otherwise noted)

Symbol	Parameter	Test conditions	Limits			Unit
			Min	Typ	Max	
C_I	Input capacitance	V_I=GND, V_I=25mVrms, f=1MHz			6	pF
C_O	Output capacitance	V_O=GND,V_O=25mVrms, f=1MHz			8	pF

Note 1: Direction for current flowing into an IC is positive (no mark).
2: Typical value is Vcc = 3V, Ta = 25°C

AC ELECTRICAL CHARACTERISTICS (Ta = 0~70°C, unless otherwise noted)

(1) MEASUREMENT CONDITIONS

V_{CC} ····· 3.3±0.3V(-70VL,-70VLL,-10VL,-10VLL)
3.0±0.3V(-12VL,-12VLL,-15VL,-15VLL)
Input pulse level ····· V_{IH}=2.2V,V_{IL}=0.4V
Input rise and fall time ····· 5ns
Reference level ····· V_{OH}=V_{OL}=1.5V
Output loads ····· Fig.1,C_L=100pF (-15VL,-15VLL,)
C_L=30pF (-70VL,-10VL,12VL,-70VLL,-10VLL,12VLL)
C_L=5pF (for t_{en},t_{dis})
Transition is measured ± 500mV from steady state voltage. (for t_{en},t_{dis})

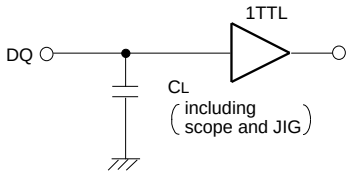


Fig.1 Output load

(2) READ CYCLE

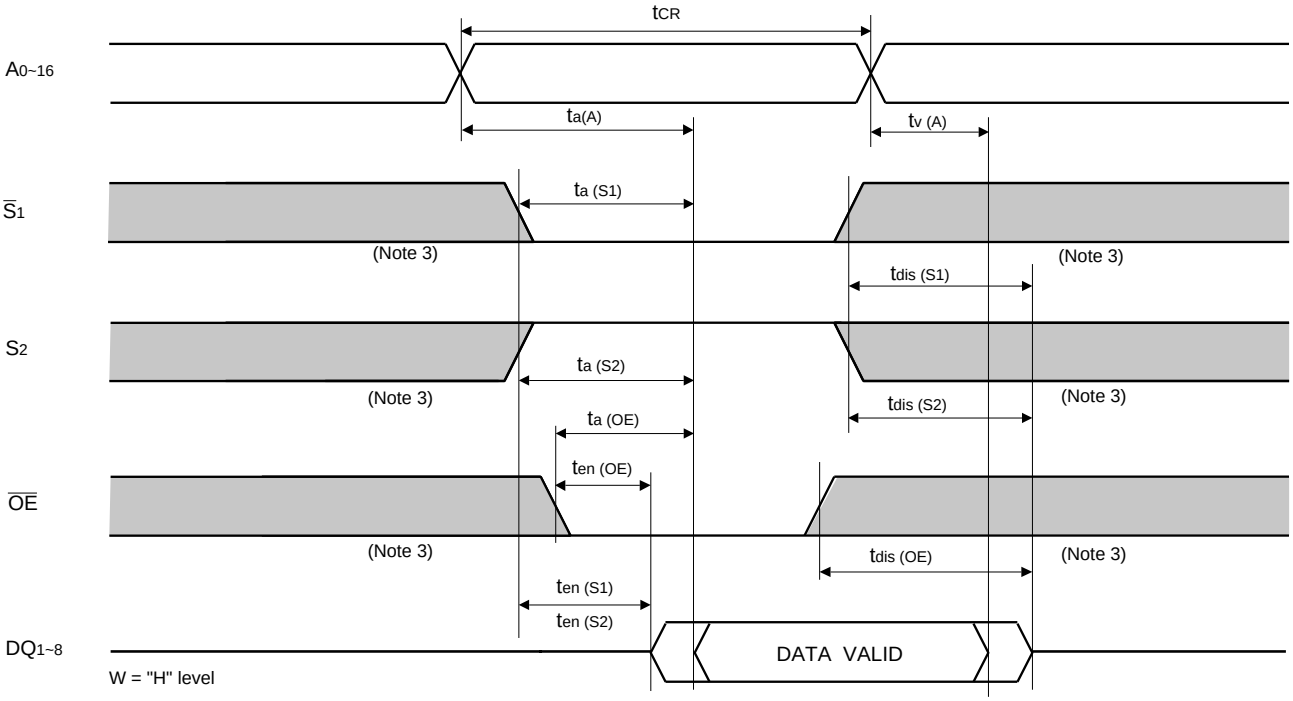
Symbol	Parameter	Limits								Unit
		-70VL,VLL		-10VL,VLL		-12VL,VLL		-15VL,VLL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CR}	Read cycle time	70		100		120		150		ns
$t_{a(A)}$	Address access time		70		100		120		150	ns
$t_{a(S1)}$	Chip select 1 access time		70		100		120		150	ns
$t_{a(S2)}$	Chip select 2 access time		70		100		120		150	ns
$t_{a(OE)}$	Output enable access time		35		50		60		75	ns
$t_{dis(S1)}$	Output disable time after $\overline{S}_1$ high		25		35		40		50	ns
$t_{dis(S2)}$	Output disable time after S_2 low		25		35		40		50	ns
$t_{dis(OE)}$	Output disable time after $\overline{OE}$ high		25		35		40		50	ns
$t_{en(S1)}$	Output enable time after $\overline{S}_1$ low	10		10		10		10		ns
$t_{en(S2)}$	Output enable time after S_2 high	10		10		10		10		ns
$t_{en(OE)}$	Output enable time after $\overline{OE}$ low	5		5		5		5		ns
$t_{V(A)}$	Data valid time after address	10		10		10		10		ns

(3) WRITE CYCLE

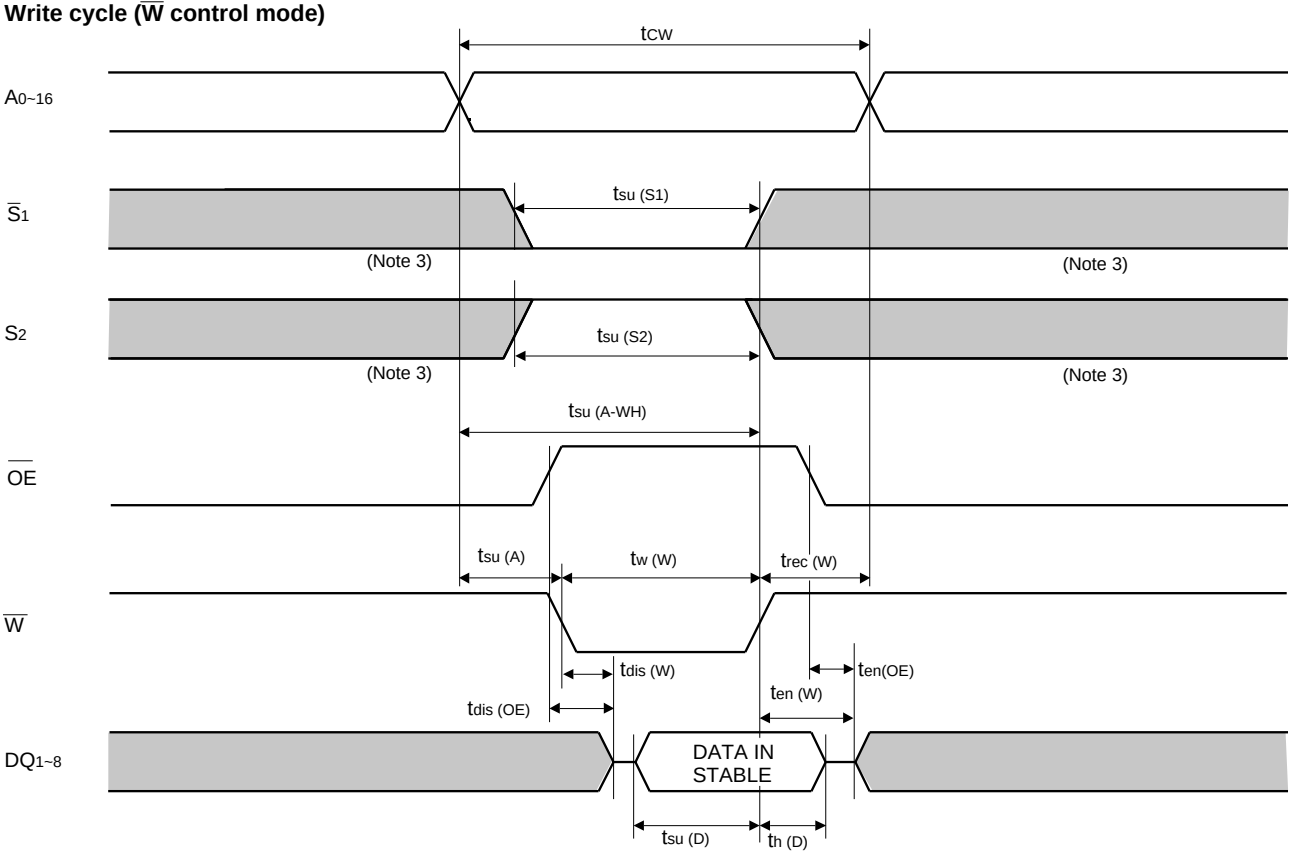
Symbol	Parameter	Limits								Unit
		-70VL,VLL		-10VL,VLL		-12VL,VLL		-15VL,VLL		
		Min	Max	Min	Max	Min	Max	Min	Max	
t_{CW}	Write cycle time	70		100		120		150		ns
$t_{w(W)}$	Write pulse width	55		75		85		100		ns
$t_{su(A)}$	Address setup time	0		0		0		0		ns
$t_{su(A-WH)}$	Address setup time with respect to $\overline{W}$	65		85		100		120		ns
$t_{su(S1)}$	Chip select 1 setup time	65		85		100		120		ns
$t_{su(S2)}$	Chip select 2 setup time	65		85		100		120		ns
$t_{su(D)}$	Data setup time	30		40		45		50		ns
$t_{h(D)}$	Data hold time	0		0		0		0		ns
$t_{rec(W)}$	Write recovery time	0		0		0		0		ns
$t_{dis(W)}$	Output disable time from $\overline{W}$ low		25		35		40		50	ns
$t_{dis(OE)}$	Output disable time from $\overline{OE}$ high		25		35		40		50	ns
$t_{en(W)}$	Output enable time from $\overline{W}$ high	5		5		5		5		ns
$t_{en(OE)}$	Output enable time from $\overline{OE}$ low	5		5		5		5		ns

(4) TIMING DIAGRAMS

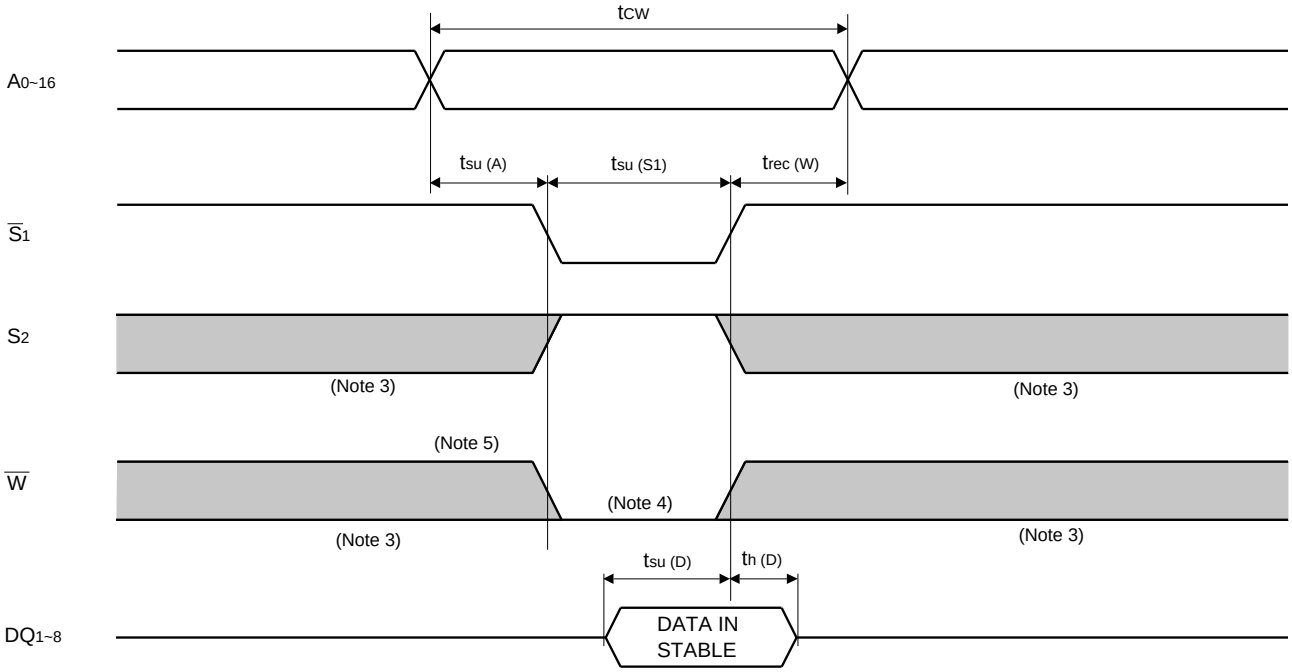
Read cycle



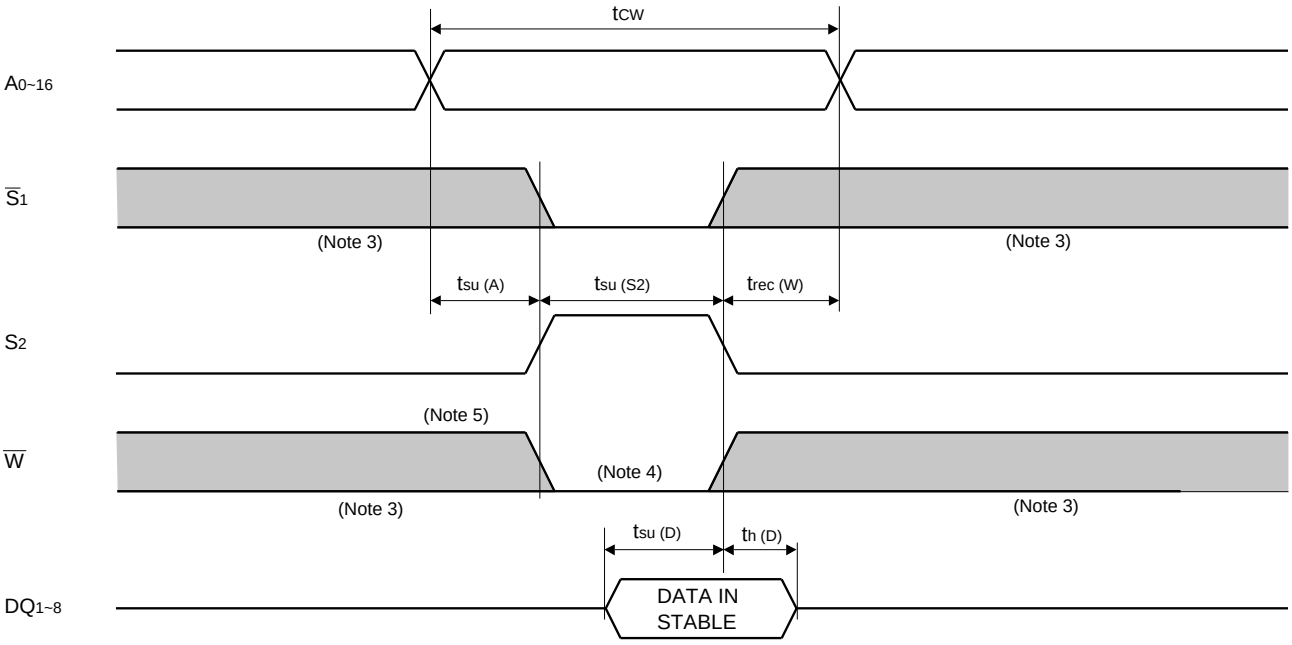
Write cycle ($\overline{W}$ control mode)



Write cycle ($\overline{S}_1$ control mode)



Write cycle (S_2 control mode)



Note 3: Hatching indicates the state is "don't care".
4: Writing is executed while S_2 high overlaps $\overline{S}_1$ and $\overline{W}$ low.
5: When the falling edge of W is simultaneously or prior to the falling edge of $\overline{S}_1$ or rising edge of S_2, the outputs are maintained in the high impedance state.
6: Don't apply inverted phase signal externally when DQ pin is output mode.