FAIRCHILD SEMICONDUCTOR TM

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LVDS Description and Family Characteristics

Low Voltage Differential Signaling (LVDS) defines a reduced swing, differential I/O technology for high-speed interface (Figure 1 and Figure 2). Many LVDS devices are defined by the ANSI/TIA/EIA-644 standard also known as RS-644. RS-644 compliant devices provide specific I/O characteristics designed to provide a low noise, low power, low EMI, high-speed interface. All Fairchild LVDS devices meet or exceed the ANSI/TIA/EIA-644 standard.

LVDS devices are typically used for point-to-point and limited multi-drop cable driving configurations. Many Fairchild LVDS devices offer features to increase performance such as common mode (Figure 3) for increased application flexibility and failsafe to eliminate false or unexpected states.

Many LVDS devices are pin replacements for existing interface technologies such as RS-422, PECL, and LVPECL. This compatibility makes upgrades to higher performance possible with minimum redesign.

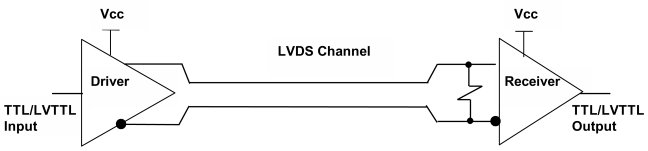

FIGURE 1.

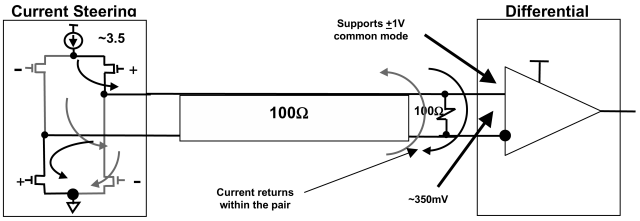

FIGURE 2.

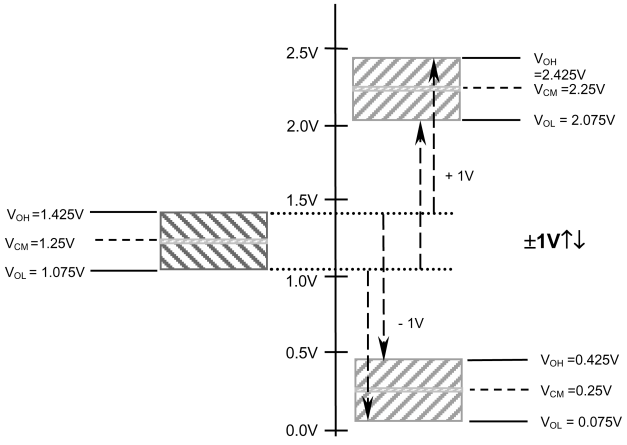

FIGURE 3.

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