Data Sheet | February 2004 | FN9131

High Voltage ORing MOSFET Controller

The ISL6144 ORing MOSFET Controller and a suitably sized N-channel power MOSFET(s) increases power distribution efficiency and availability when replacing a power ORing diode in high current applications.

In a multiple supply, fault tolerant, redundant power distribution system, paralleled power supplies contribute equally to the load current through various power sharing schemes. Regardless of the scheme, a common design practice is to include discrete ORing power diodes to protect against reverse current flow should one of the power supplies develop a catastrophic output short to ground. In addition, reverse current can occur if the current sharing scheme fails and an individual power supply voltage falls significantly below the others.

Although the discrete ORing diode solution has been used for some time and is inexpensive to implement, it has some drawbacks. The primary downside is the increased power dissipation loss in the ORing diodes as power requirements for systems increase. Another disadvantage when using an ORing diode would be failure to detect a shorted or open ORing diode, jeopardizing power system reliability. An open diode reduces the system to single point of failure while a diode short might pose a hazard to technical personnel servicing the system while unaware of this failure.

The ISL6144 can be used in 10V to 75V systems and has an internal charge pump to provide a floating gate drive for the N-channel ORing MOSFET. The High Speed (HS) Comparator protects the common bus from individual power supply shorts by turning off the shorted feed's ORing MOSFET in less than 300ns and ensuring low reverse current.

An external resistor-programmable detection level for the HS Comparator allows users to set the N-channel MOSFET "VOUT - VIN" trip point to adjust control sensitivity to power supply noise.

The Hysteretic Regulating (HR) Amplifier provides a slow turn off of the ORing MOSFET. This turn off is achieved in less than 100µs when one of the sourcing power supplies is shutdown slowly for system diagnostics, ensuring zero reverse current. This slow turn off mechanism also reacts to output voltage droop, degradation, or power down.

An open drain $\overline{\text{FAULT}}$ pin will indicate that a fault has occurred. The fault detection circuitry covers different types of failures; including dead short in the sourcing supply, a short of any two ORing MOSFET terminals, or a blown fuse in the power distribution path.

Features

- Wide Supply Voltage Range +10V to +75V
- Transient Rating to +100V
- Reverse Current Fault Isolation
- Internal Charge Pump allows the use of N-channel MOSFET
- HS Comparator Provides Very Fast <0.3µs Response Time to Dead Shorts on Sourcing Supply. HS Comparator also has resistor-adjustable trip level
- HR Amplifier allows Quiet, <100µs MOSFET Turn Off for Power Supply Slow Shut Down
- Open Drain, Active Low Fault Output with 120µs Delay
- Provided in Packages Compliant to UL60950 (UL1950) Creepage Requirements
- QFN Package:
  - Compliant to JEDEC PUB95 MO-220 QFN - Quad Flat No Leads - Package Outline
  - Near Chip Scale Package footprint, which improves PCB efficiency and has a thinner profile
- Lead-Free Available as an Option

Applications

- ORing MOSFET Control in Power Distribution Systems
- N+1 Redundant Distributed Power Systems
- File and Network Servers (12V and 48V)
- Telecom/Datacom Systems

Ordering Information

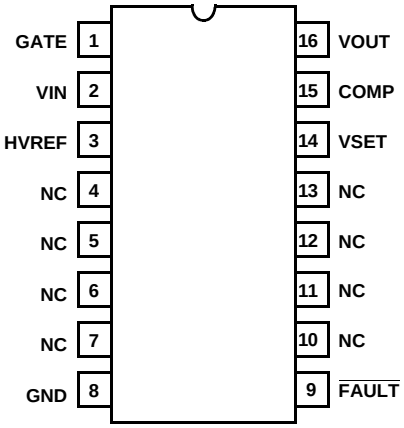
PART #	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6144IV	-40 to +105	16 Ld TSSOP	M16.173
ISL6144IVZA (See Note)	40 to +105	16 Ld TSSOP (Lead-Free)	M16.173
ISL6144IR	-40 to +105	20 Ld 5x5 QFN	L20.5x5
ISL6144IRZA (See Note)	-40 to +105	20 Ld 5x5 QFN (Lead-Free)	L20.5x5

NOTE: Intersil Lead-Free products employ special lead-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which is compatible with both SnPb and lead-free soldering operations. Intersil Lead-Free products are MSL classified at lead-free peak reflow temperatures that meet or exceed the lead-free requirements of IPC/JEDEC J Std-020B.

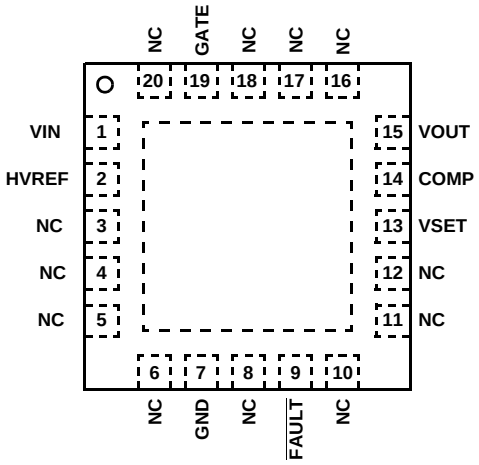
Tape and Reel available. Add "T" suffix for Tape and Reel Packing Option.

Pinouts

ISL6144 (16 LEAD TSSOP)
TOP VIEW



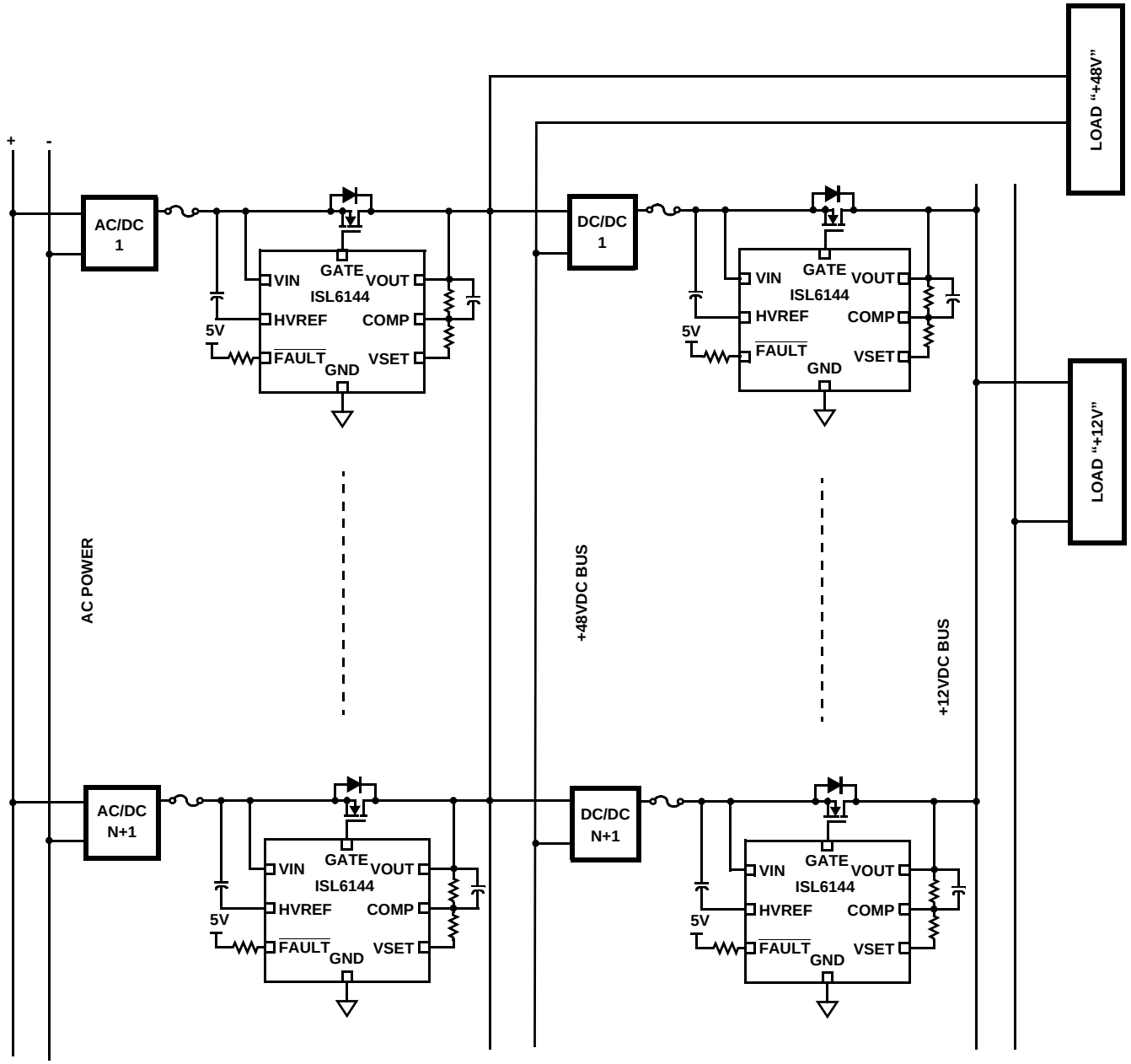
ISL6144 (20 LEAD 5x5 QFN)
TOP VIEW



Pin Descriptions

TSSOP PIN #	QFN PIN #	SYMBOL	FUNCTION	DESCRIPTION
1	19	GATE	External FET Gate Drive	Allows active control of external N-channel FET gate to perform ORing function.
2	1	VIN	Power supply connection	Chip bias input. Also provides a sensing node for external FET control.
3	2	HVREF	Chip high voltage reference	Low side of floating high voltage reference for all of the HV chip circuitry.
8	7	GND	Chip ground reference	Chip ground reference point.
9	9	$\overline{\text{FAULT}}$	Fault Output	Provides an open drain active low output as an indication that a fault has occurred: GATE is OFF (GATE < VIN+0.37V) or other types of faults resulting in VIN-VOUT > 0.41V.
14	13	VSET	Low side connection for trip level	Resistor connected to COMP provides adjustable “Vd-Vs” trip level along with pin COMP.
15	14	COMP	High side connection for HS Comparator trip level	Resistor connected to VOUT provides sense point for the adjustable Vd-Vs trip level along with pin VSET.
16	15	VOUT	Chip bias and Load connection	Provides the second sensing node for external FET control and chip output bias.
4-7, 10-13	3-6, 8, 10-12, 16-18, 20	NC	No Connection	

General Application Circuit



NOTES:

1. AC/DC 1 through (N+1) are multistage AC/DC converters which include AC/DC rectification stage and a DC/DC Converter with a + 48VDC output (also might include a Power Factor Correction stage).
2. DC/DC Converter 1 through (N+1) are DC/DC converters to provide additional Intermediate Bus
3. Load "+12V" and Load "+48V" might include other DC/DC converter stages to provide lower voltages such as ±15V, ±5V, +3.3V, +2.5V, +1.8V etc.
4. Fuse location might vary depending on power system architecture.

FIGURE 1. ISL6144 GENERAL APPLICATION CIRCUIT IN A DISTRIBUTED POWER SYSTEM

Simplified Block Diagram

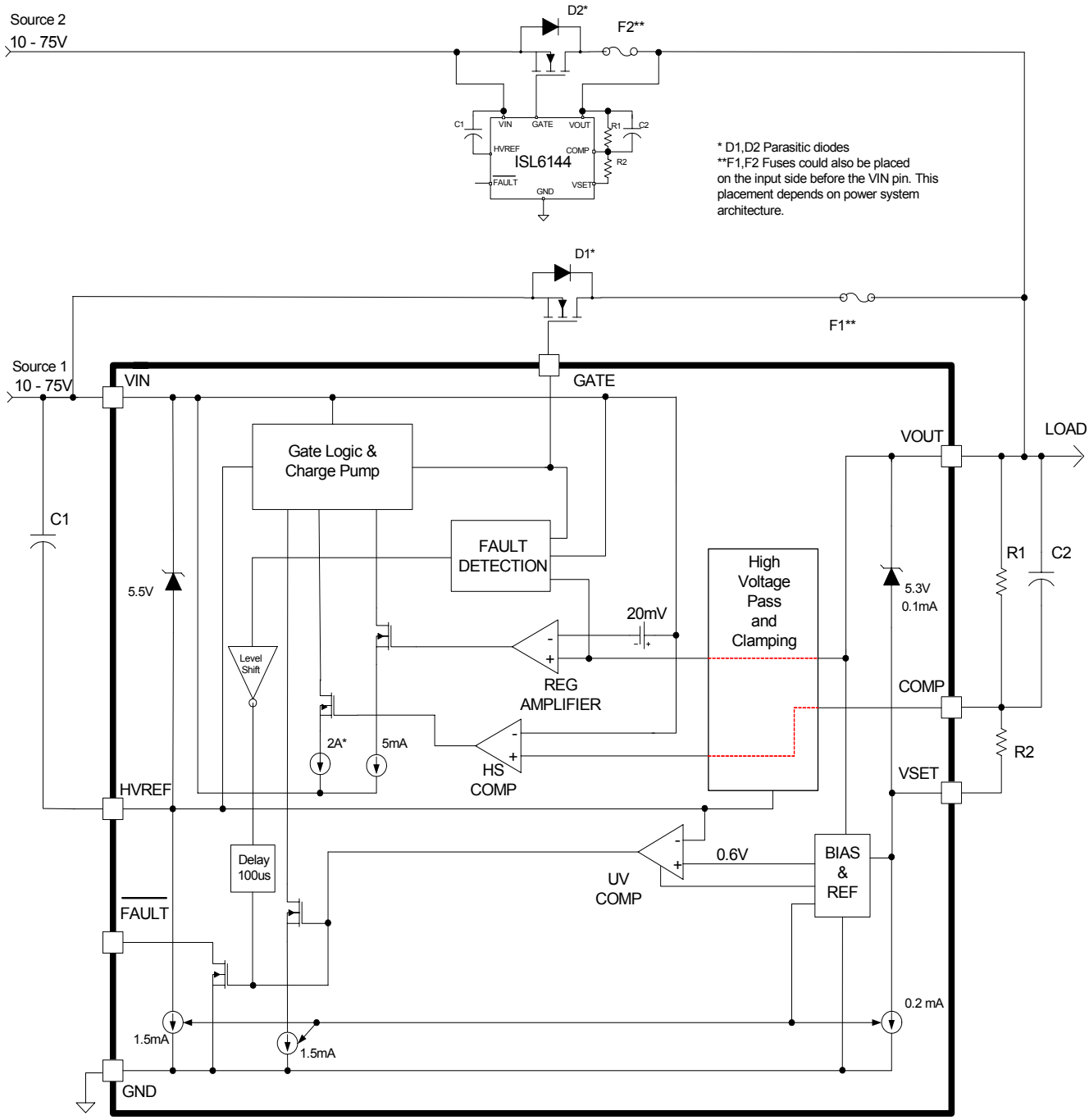


FIGURE 2. SIMPLIFIED BLOCK DIAGRAM

Absolute Maximum Ratings $T_A = 25^oC$

VIN, VOUT . . . . . -0.3V to +100V
GATE . . . . . -0.3V to VIN+12V
HVREF . . . . . -0.3V to VIN- 5V
COMP . . . . . -0.3V to VOUT
VSET . . . . . -0.3V to VOUT-5V
$\overline{FAULT}$ . . . . . -0.3V to 16V
ESD Classification . . . . . CLASS 2

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
TSSOP Package (Note 1)	90	N/A
QFN Package (Notes 3, 4)	35	5

Maximum Junction Temperature (Plastic Package) . . . . . 150°C
Maximum Storage Temperature Range . . . . . -65°C to 150°C
Maximum Lead Temperature (Soldering 10s) . . . . . 300°C

Operating Conditions

Supply Voltage Range . . . . . +10 to +75V
Temperature Range (T_A) . . . . . -40°C to +105°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. (See Tech Brief, #TB379.1 for details.)
2. All voltages are relative to GND, unless otherwise specified.
3. For θ_{JC}, the "case temp" location is the center of the exposed metal pad on the package underside.
4. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with "die attach" features. (See Tech Brief, #TB379 for details.)

Electrical Specifications VIN = 48V, $T_A = -40^oC$ to 105^oC, Unless Otherwise Specified

PARAMETER	SYMBOL		TEST CONDITIONS	MIN	TYP	MAX	UNITS
BIAS "V_{IN}"							
POR Rising	POR_{L2H}		V_{IN} Rising to $V_{GATE} > V_{IN}+7.5V$	10	-	-	V
12V Bias Current	I_{12V}		V_{IN} = 12V, $V_{GATE} = V_{IN} + V_{GQP}$	-	3.5	-	mA
48V Bias Current	I_{48V}		V_{IN} = 48V, $V_{GATE} = V_{IN} + V_{GQP}$	-	4.5	-	mA
75V Bias Current	I_{75V}		V_{IN} = 75V, $V_{GATE} = V_{IN} + V_{GQP}$	-	5	-	mA
GATE							
Charge Pump Voltage	V_{GQP}		V_{IN} = 12V to 75V	VIN+9	VIN+10.5	VIN+12	V
Gate Low Voltage Level	V_{GL}		$V_{IN} - V_{OUT} < 0V$	-0.3	VIN	VIN+0.5	V
Low Pull Down Current	I_{PDL}	*	Cgs = 39nF, $I_{PDL} = Cgs*dVgs/T_{tofs}$	-	5	-	mA
High Pull Down Current	I_{PDH}	*	Cgs = 39nF, $I_{PDH} = Cgs*dVgs/T_{toff}$	-	2	-	A
Slow Turn-off Time	T_{toffs}		Cgs = 39nF	-	-	100	µs
Fast Turn-off Time	T_{toff}		Turn-off from $V_{GATE} = V_{IN}+V_{GQP}$ to V_{IN}+1V with Cgs = 39nF (includes HS Comparator delay time)	-	250	300	ns
Start up "Turn-On" Time	T_{ON}		Turn-on from $V_{GATE} = V_{IN}$ to V_{IN}+ 7.5V into 39nF	-	1	-	ms
GATE Turn-On Current	I_{ON}	*	V_{IN} = 10V to 75V	-	1	-	mA
CONTROL AND REGULATION I/O							
HR Amplifier Forward Voltage Regulation	V_{FWD_HR}		ISL6144 controls voltage across FET Vds to V_{FWD_HR} during static forward operation at loads resulting in $I*r_{DS(ON)} < V_{FWD\_HR}$	10	20	30	mV
HS COMP Externally Programmable Threshold	$V_{TH(HS)}$	*	Externally programmable threshold for noise sensitivity (System Dependant), typical 0.05 to 0.3V	0	0.05	5.3	V
HS Comparator Offset Voltage	$V_{OS(HS)}$			-40	0	25	mV
COMP Input Current (bias current)	I_{COMP}			-	1.1	-	µA

Electrical Specifications VIN = 48V, T_A = -40°C to 105°C, Unless Otherwise Specified **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
HVREF Voltage (VIN-HVREF)	$HV_{REF(VZ)}$	V_{IN} = 10V to 75V	-	5.5	-	V
VSET Voltage (VOUT-VSET)	$V_{REF(VSET)}$	V_{IN} = 10V to 75V	-	5.3	-	V
$\overline{\text{Fault}}$ Low Output Voltage	V_{FLT_L}	V_{IN} - V_{OUT} < 0V, V_{GATE} = V_{GL}	-	-	0.5	V
$\overline{\text{Fault}}$ Sink Current	I_{FLT_SINK}	$\overline{\text{FAULT}}$ = V_{FLT_L}, V_{IN} < V_{OUT}, V_{GATE} = V_{GL}	4	-	-	mA
$\overline{\text{Fault}}$ Leakage Current	I_{FLT_LEAK}	$\overline{\text{FAULT}}$ = "V_{FLT_H}", V_{IN} >V_{OUT}, V_{GATE} = V_{IN} + V_{GQP}	-	-	10	µA
$\overline{\text{Fault}}$ Delay -Low to High	T_{FLT}	GATE = V_{GL} to $\overline{\text{FAULT}}$ = V_{FLT_L}	-	120	-	µs

NOTES:

5. The * denotes parameters which are guaranteed by design and not production tested.
6. Specifications to +105°C and -40°C are guaranteed by design and not production tested.

Functional Pin Description

GATE

This is the Gate Drive output of the external N-Channel MOSFET generated by the IC internal charge pump. Gate turn on time is typically 1ms.

VIN

Input bias pin connected to the sourcing supply side (ORing MOSFET Source). Also serves as the sense pin to determine the sourcing supply voltage. The ORing MOSFET will be turned off when VIN becomes lower than VOUT by a value more than the externally set threshold.

VOUT

Connected to the Load side (ORing MOSFET Drain). This is the VOUT sense pin connected to the load. This is the common connection point for multiple paralleled supplies. VOUT is compared to VIN to determine when the ORing FET has to be turned off.

HVREF

Low side of the internal IC High Voltage Reference used by internal circuitry, also available as an external pin for additional external capacitor connection.

COMP

This is the high side connection for the HS Comparator trip level setting ($V_{TH(HS)}$). A resistor R1 connected between COMP and VOUT along with resistor R2 provides adjustable VOUT-VIN trip level (0 to 5V). This provides flexibility to externally set the desired level depending on particular system requirement.

VSET

Low side connection for the HS Comparator trip level setting A second resistor R2 connected between VSET and COMP provides adjustable "V_{IN} - V_{OUT}" level along with R1.

$\overline{\text{FAULT}}$

Open-Drain pull-down $\overline{\text{FAULT}}$ Output with internal on chip filtering (T_{FLT}). The ISL6144 fault detection circuitry will pull down this pin to GND as soon as it detects a fault. Different types of faults and their detection mechanisms are discussed in more detail in the Block Diagram Description section.

GND

IC ground reference

Detailed Description

The ISL6144 and a suitably sized N-Channel power MOSFET(s) increases power distribution efficiency and availability when replacing a power ORing diode in high current applications. Refer to the Application Consideration section for power saving when using ISL6144 with an N-channel ORing MOSFET compared to a typical ORing diode.

Functional Block Description

REG. AMPLIFIER - Slow (Quiet) Turn Off

A Hysteretic Regulating (HR) Amplifier is used for a Quiet/ Slow turn off mechanism. This slow turn off is initiated when the sourcing power supply is turned off slowly for system diagnostics. Under normal operating conditions as VOUT pulls up to 20mV below V_{IN} (V_{IN}-20mV > V_{OUT}), the HR Amplifier regulates the gate voltage to keep the 20mV (V_{FWD_HR}) forward voltage drop across the ORing MOSFET (Vs-Vd). This will continue until the load current exceeds the MOSFET ability to deliver the current with Vsd of 20mV. In this case Gate will be charged to the full charge pump voltage (V_{GQP}) to fully enhance the MOSFET. At this point the MOSFET will be fully enhanced and behave as a constant resistor valued at the $r_{DS(ON)}$. Once V_{IN} starts to drop below V_{OUT}, regulation cannot be maintained and the output of the HR Amp is pulled high and the gate is pulled down to V_{IN} slowly in less than a 100µs. As a result, the ORing FET is turned off, avoiding reverse current as well as voltage and current stresses on supply components.

The slow turn off is achieved in two stages. The first stage starts with a slow turn off action and lasts for up to 20µs. The gate pull down current for the first stage is 2mA. The second slow turn off stage completes the gate turn off with a 10mA pull down current. The 20µs delay filters out any false trip off due to noise or glitches that might be present on the supply line.

The gate turn on and gate turn off drivers have a 50kHz filter to reduce the variation in FET forward voltage drop (and FET gate voltage) due to normal SMPS system switching noises (typically higher than 50kHz). These filters do not affect the total turn on or slow turn off times.

Special system design precautions must be taken to insure that no AC mains related low frequency noise will be present at the input or output of ISL6144. Filters and multiple power conversion stages, which are part of any distributed dc power system, normally filter out all such noise.

HS Comparator - Fast Turn Off

There is a High Speed (HS) Comparator used for fast turn-off of the ORing MOSFET to protect the common bus against hard short faults at a sourcing power supply output (refer to Figure 3).

During normal operation the gate of the ORing MOSFET is charge pumped to a voltage that depends on whether it is in the 20mV regulation mode or fully enhanced. In this case:

$$V_{OUT} = V_{IN} - I_{OUT} \bullet r_{DS(ON)} \quad \text{(EQ. 1)}$$

If a dead short fault occurs in the sourcing supply, it causes V_{IN} to drop very quickly while V_{OUT} is not affected as more than one supply are paralleled. In the absence of the ISL6144 functionality, a very high reverse current will flow from Output to the Input supply pulling down the common DC Bus, resulting in an overall “catastrophic” system failure.

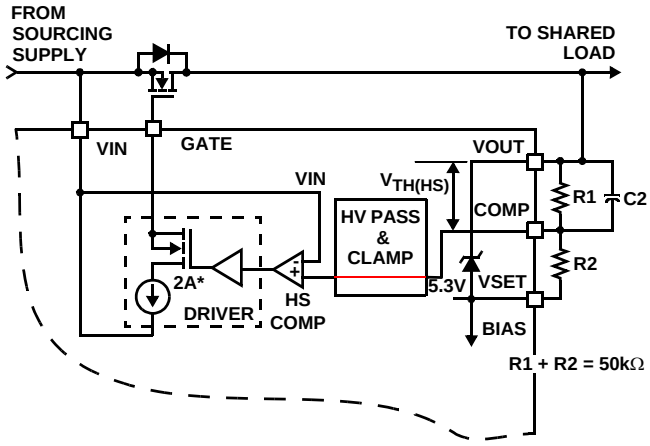


FIGURE 3. HS COMPARATOR

The fault can be detected and isolated by using the ISL6144 and an N-channel ORing MOSFET. V_{IN} is compared to V_{COMP}, and whenever:

$V_{IN} < V_{COMP}$; where

$$V_{COMP} = V_{OUT} - V_{TH(HS)}, \quad \text{(EQ. 2)}$$

$V_{TH(HS)}$ is defined below

The fast turn off mechanism will be activated and the MOSFET(s) will be turned off very quickly. The speed of this turn off depends on the amount of equivalent gate loading capacitance. For an equivalent Cgs = 39nF. The gate turn off time is <300ns and gate pull down current is 2A.

The level of $V_{TH(HS)}$ (HS Comparator trip level) is adjustable by means of external resistors R1 and R2 to a value theoretically ranging from 0-5.3V. Typical values are 0.05V to 0.3V. This is done in order to avoid false turn off due to noise or minor glitches present in the DC switching power supply. The threshold voltage is calculated as:

$$V_{TH(HS)} = \frac{R1}{(R1 + R2)} V_{REF(VSET)} \quad \text{(EQ. 3)}$$

Where $V_{REF(VSET)}$ is an internal zener reference (5.3V typical) between VOUT and VSET pins. R1 and R2 must be chosen such that their sum is about 50kΩ. An external capacitor C2 is needed between VOUT and COMP pins to provide high frequency decoupling. The HS comparator has an internal delay time on the order of 50ns which is part of the <300ns overall turn off time specification (with Cgs=39nF).

Gate Logic and Charge Pump

The IC has two charge pumps:

The first charge pump generates the floating gate drive for the N-channel MOSFET. The second charge pump output current opposes the pull down current of the slow turn off transistor to provide regulation of the GATE voltage.

The presence of the charge pump allows the use of an N-channel MOSFET with a floating gate drive. The N-channel MOSFETs normally have lower $r_{DS(ON)}$ (not to mention cost saving) compared to P-Channel MOSFETs, allowing further reduction of conduction losses.

BIAS & REF

Bias currents for the two internal zener supplies (HVREF and VSET) is provided by this block. This block also provides a 0.6V band-gap reference used in the UV detection circuit.

Undervoltage Comparator

The undervoltage comparator compares HVREF to 0.6V internal reference. Once it falls below this level the UV circuitry pulls and holds down the gate pin as long as the HVREF UV condition is present. Voltage at both VIN and HVREF pins track each other.

High Voltage Pass and Clamp

A high voltage pass and clamping circuit prevents the high output voltage from damaging the comparators in case of quick drop in V_{IN}. The comparators are running from the 5V supply between HVREF and VIN. These devices are rated for 5V and will be damaged if V_{OUT} is allowed to be present (as the output is powered from other parallel supplies), and does not fall when V_{IN} is falling. For example, if V_{IN} falls to 30V, V_{OUT} remains at 48V and the differential Voltage between the "-" and "+" terminals of the comparator would be 18V, exceeding the rating of the devices and causing permanent damage to the IC.

Fault Detection Block

The fault detection block has two monitoring circuits (refer to Figure 4):

1. Gate monitoring detects when the GATE < V_{IN}+0.37V
2. VOUT monitoring detects when V_{IN}-0.41V > V_{OUT}

These two outputs are ORed, inverted, level shifted, and delayed using an internal filter (T_{FLT})

The following failures can be detected by the fault detection circuitry:

1. ORing FET off due to dead short in the sourcing supply, leading to V_{IN} < V_{OUT}
2. Shorted Terminals of the ORing FET
3. Blown fuse in the power path of the sourcing supply
4. Open Gate terminal
5. HVREF UV

The $\overline{\text{FAULT}}$ pin is not latched off and the pull down will shut off as soon as the fault is removed and the pin becomes high impedance. Typically, an external pull-up resistor is connected to an external voltage source (for example 5V, 3.3V) to pull the pin high, an LED can be used to indicate the presence of a fault.

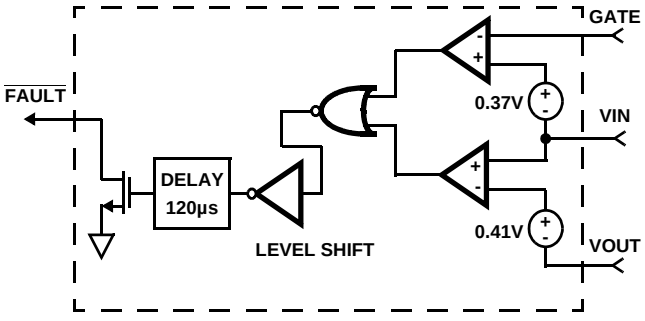


FIGURE 4. FAULT DETECTION BLOCK

Application Considerations

ORing MOSFET Selection

Using an ORing MOSFET instead of an ORing diode results in increased overall power system efficiency as losses across the ORing elements are reduced. The use of ORing MOSFETs becomes more important at higher current levels, as power loss across the traditionally used ORing diode is very high. The high power dissipation across these diodes requires special thermal design precautions such as heat sinks and forced airflow.

For example, in a 48V, 40A (1+1) redundant system with current sharing, using a Schottky diode as the ORing (auctioneering) device (refer to Figure 5), the forward voltage drop is in the 0.4-0.7V range, let us assume it is 0.5V. Power loss across each diode:

$$P_{loss(D1)} = P_{loss(D2)} = \frac{I_{OUT}}{2} \cdot V_F = 20A \cdot 0.5V = 10W$$

Total power loss across the two ORing diodes is 20W.

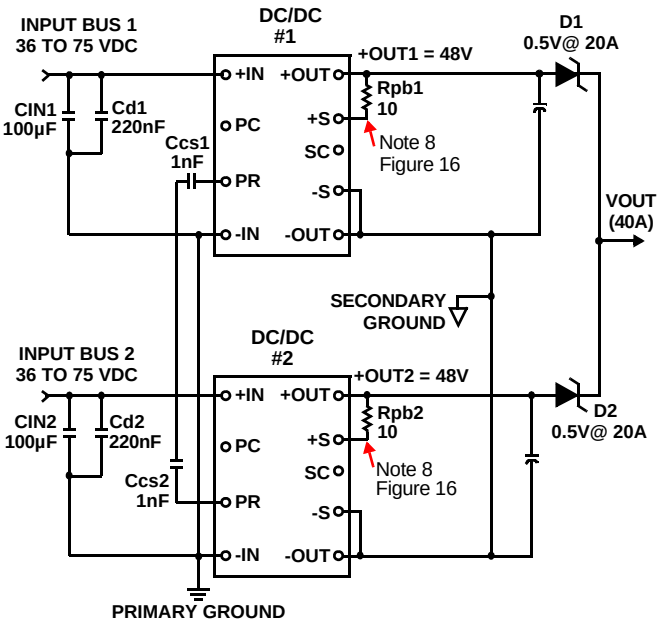


FIGURE 5. 1+1 REDUNDANT SYSTEM WITH DIODE ORing

If a 5mΩ single MOSFET per feed is used, the Power loss across each MOSFET is:

$$P_{loss(M1)} = P_{loss(M2)} = \left(\frac{I_{OUT}}{2}\right)^2 \cdot r_{DS(ON)} \qquad \text{(EQ. 4)}$$

$$P_{loss(M1)} = (20A)^2 \cdot 5m\Omega = 2W$$

Total power loss across the two ORing MOSFETs is 4W.

In case of failure of current sharing scheme, or failure of DC/DC #1, the full load will be supplied by DC/DC #2. ORing

MOSFET M2 or ORing Diode D2 will be conducting the full load current. Power loss across the ORing devices is:

$$P_{loss(D2)} = I_{OUT} \cdot V_F = 40A \cdot 0.5V = 20W \quad \text{(EQ. 5)}$$

$$P_{loss(M2)} = (I_{OUT})^2 \cdot R_{dson} = (40A)^2 \cdot 5m\Omega = 8W$$

This shows that worst-case failure scenario has to be accounted for when choosing the ORing MOSFET. In this case we need to use two MOSFETs in parallel per feed to reduce overall power dissipation and prevent excessive temperature rise of any single MOSFET. Another alternative would be to choose a MOSFET with lower $r_{DS(ON)}$.

The final choice of the N-Channel ORing MOSFET depends on the following aspects:

1. Voltage Rating: The drain-source breakdown voltage V_{DSS} has to be higher than the maximum input voltage including transients and spikes. Also the gate to source voltage rating has to be considered, The ISL6144 maximum Gate charge voltage is 12V, make sure the used MOSFET has a maximum V_{GS} rating >12V.
2. Power Losses: In this application the ORing MOSFET is used as a series pass element, which is normally fully enhanced at high load currents, switching losses are negligible. The major losses are conduction losses, which depend on the value of the on-state resistance of the MOSFET $r_{DS(ON)}$, and the per feed load current. For an N+1 redundant system with perfect current sharing, the per feed MOSFET losses are:

$$P_{loss(FET)} = \left(\frac{I_{LOAD}}{N+1}\right)^2 \cdot r_{DS(ON)} \quad \text{(EQ. 6)}$$

   The $r_{DS(ON)}$ value also depends on junction temperature; a curve showing this relationship is usually part of any MOSFET's data sheet. The increase in the value of the $r_{DS(ON)}$ over temperature has to be taken into account.
3. Current handling capability, steady state and peak, are also two important parameters that must be considered. The limitation on the maximum allowable drain current comes from limitation on the maximum allowable device junction temperature. The thermal board design has to be able to dissipate the resulting heat without exceeding the MOSFET's allowable junction temperature.

Another important consideration when choosing the ORing MOSFET is the forward voltage drop across it, if this drop approaches the 0.41V limit, which is used in the VOUT fault monitoring mechanism then this will result in a permanent fault indication. Normally the voltage drop would be chosen not to exceed a value around 100mV.

"ISL6144+ORing FET" vs "ORing Diode" Solution

"ISL6144+ORing FET" solution is more efficient, which will result in simplified PCB and thermal design. It will also eliminate the need for a heat sink for the ORing diode. This will result in cost savings. In addition is the fact that the ISL6144 solution provides a more flexible, reliable and controllable ORing functionality and protecting against system fault scenarios (refer to fault detection block description).

On the other hand the most common failures caused by diode ORing include open circuit and short circuit failures. If one of these diodes (Feed A) has failed open, then the other Feed B will provide all of the power demand. The system will continue to operate without any notification of this failure reducing the system to a single point of failure. A much more dangerous failure is where the diode has failed short. The system will continue to operate without notification that the short has occurred. With this failure transients and failures on Feed B propagate to Feed A. Also this silent short failure could pose a significant safety hazard for technical personnel servicing these feeds.

"ISL6144 + ORing FET" vs "Discrete ORing FET" Solution

If we compare the ISL6144 integrated solution to discrete ORing MOSFET solutions, the ISL6144 wins in all aspects, the main ones being PCB real estate saving, cost savings, and reduction in the MTBF of this section of the circuit as the overall number of components is reduced.

In brief the solution offered by this IC enhances power system performance and protection while not adding any considerable cost, on the contrary saving PCB board real estate and providing simple to implement integrated solution.

Setting the External HS Comparator Threshold Voltage

In general, paralleled modules in a redundant power system have some form of active current sharing, to realize the full benefit of this scheme including lower operating temperatures, lower system failure rate, as well as better transient response when load step is shared. Current sharing is realized using different techniques; all of these techniques will lead to similar modules operating under similar conditions in terms of switching frequency, duty cycle, output voltage and current. When paralleled modules are current sharing, their individual output ripple will be similar in amplitude and frequency and the common bus will have the same ripple as these individual modules and will not cause any of the turn off mechanisms to be activated as the same ripple will be present on both sensing nodes (VIN and VOUT). This would allow setting the high speed comparator threshold ($V_{TH(HS)}$) to a very low value. As a starting point a $V_{TH(HS)}$ of 50mV could be used, the final value of this TH will be system dependant and has to be finalized in the system prototype stage. If the gate experiences false turn-off due to system noise, the $V_{TH(HS)}$ has to be increased.

The reverse current peak can be estimated as:

$$I_{reverseP} = \frac{V_{TH(HS)} + V_{SD} + V_{OS(HS)}}{r_{DS(ON)}}; \text{ where} \qquad \text{(EQ. 7)}$$

V_{SD} is the MOSFET forward voltage drop

$V_{OS(HS)}$ is the voltage offset of HS Comparator

The duration of the reverse current pulse is few hundred nanoseconds and is normally kept well below current rating of the ORing MOSFET.

Reducing the value of $V_{TH(HS)}$ results in lower reverse current amplitude and reduces transients on the common bus output voltage.

HVREF and COMP Capacitor Values

HVREF Capacitor (C1): this capacitor is necessary to stabilize the $HV_{REF(VZ)}$ supply and a value of 150nF is sufficient. Increasing this value will result in gate turn on time increase.

COMP Capacitor (C2):Placed between VOUT and COMP pins to provide filtering and decoupling. A 10nF capacitor is adequate for most cases.

Typical Performance Curves and Waveforms

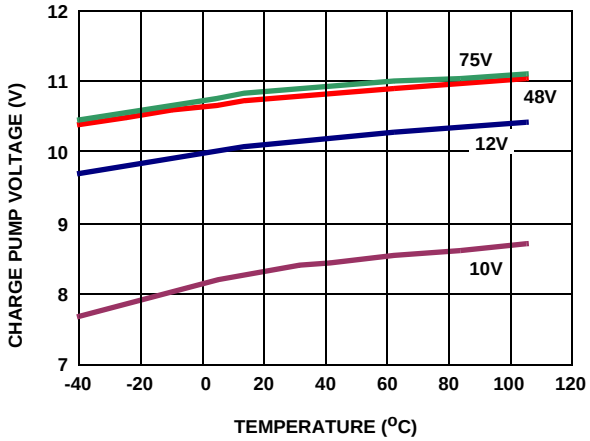


FIGURE 6. CHARGE PUMP VOLTAGE (V_{GQP}) vs TEMPERATURE

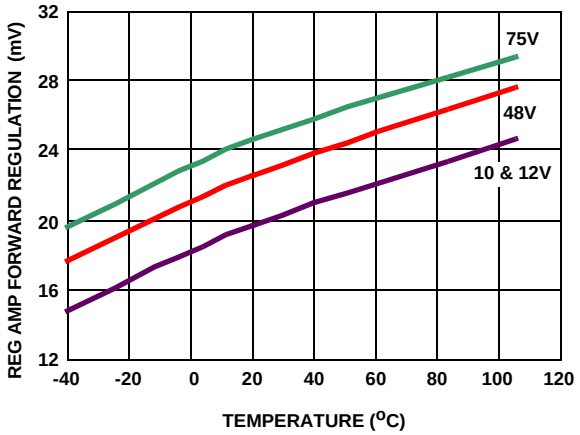


FIGURE 7. REG. AMP FORWARD REGULATION

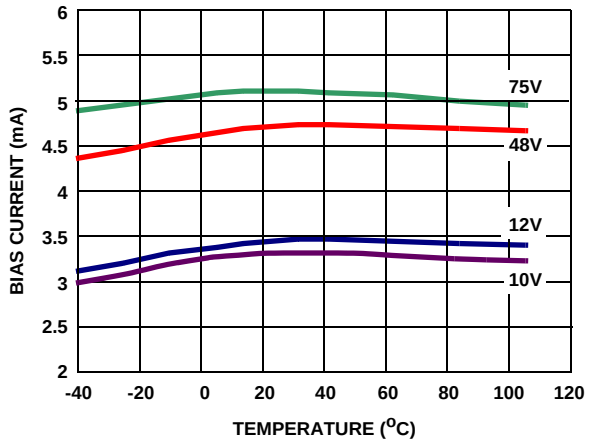


FIGURE 8. I BIAS CURRENT vs TEMPERATURE

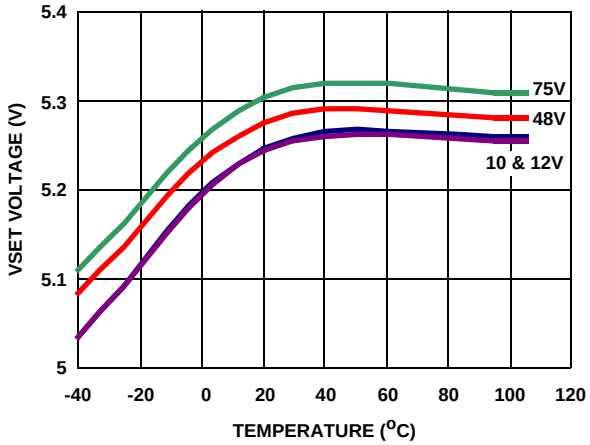


FIGURE 9. VSET VOLTAGE

Typical Performance Curves and Waveforms (Continued)

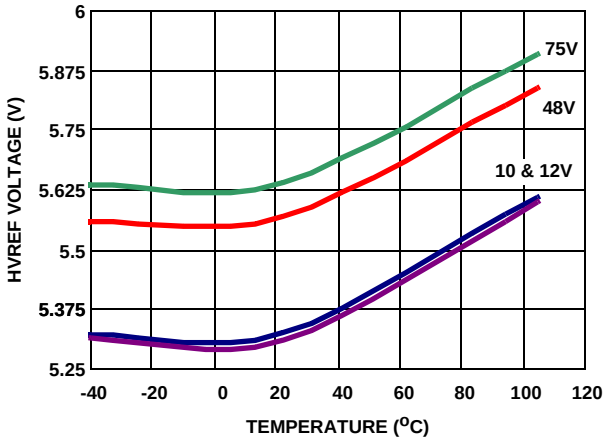


FIGURE 10. HVREF VOLTAGE

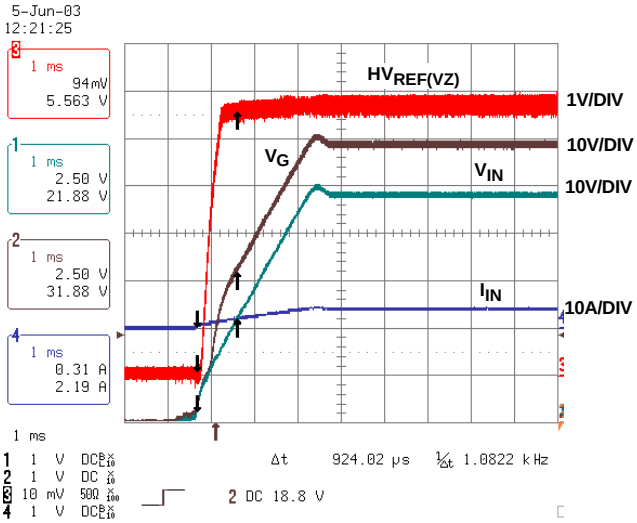


FIGURE 11. FIRST SUPPLY START UP

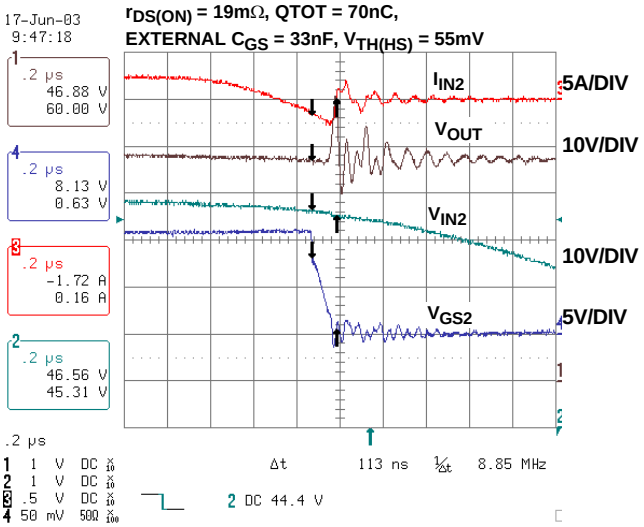


FIGURE 12. HIGH SPEED TURN OFF, VIN = 48V, COMMON LOAD IS SMPS (C_{LOAD} = 100µF) WITH EQUIVALENT 4A LOAD

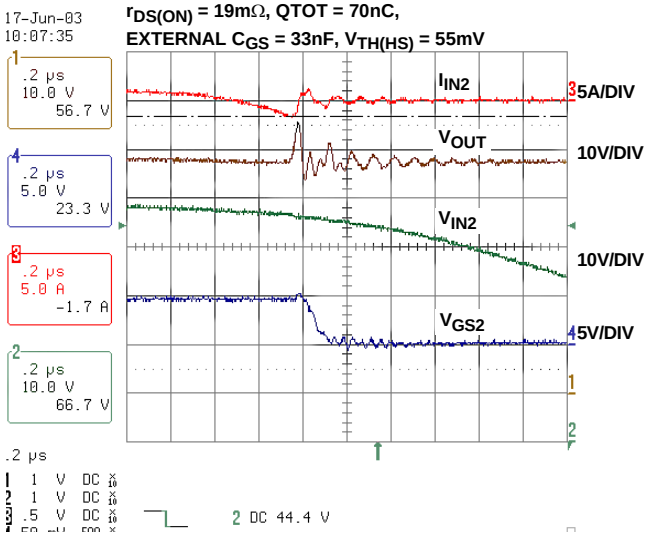


FIGURE 13. HIGH SPEED TURN OFF, VIN = 48V, COMMON LOAD IS SMPS (C_{LOAD} = 100µF) WITH EQUIVALENT 1.3A LOAD

Typical Performance Curves and Waveforms (Continued)

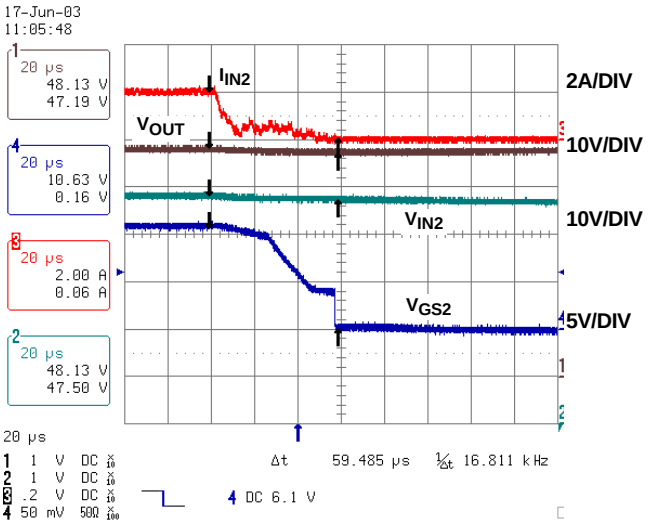


FIGURE 14. SLOW SPEED TURN OFF, VIN = 48V, COMMON LOAD IS SMPS (C_{LOAD} = 100µF) WITH EQUIVALENT 4A LOAD

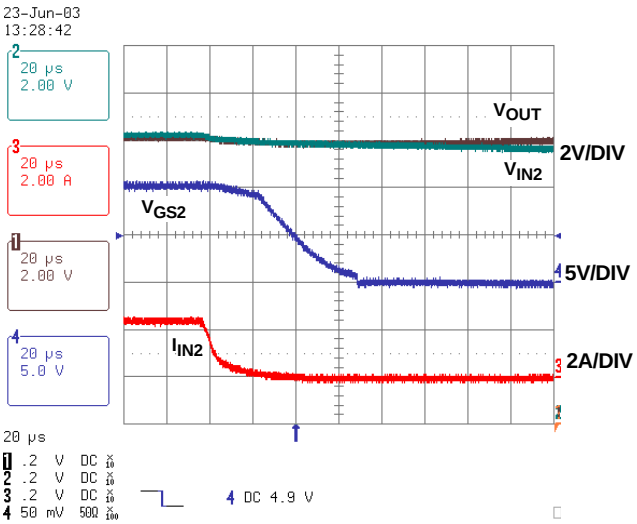
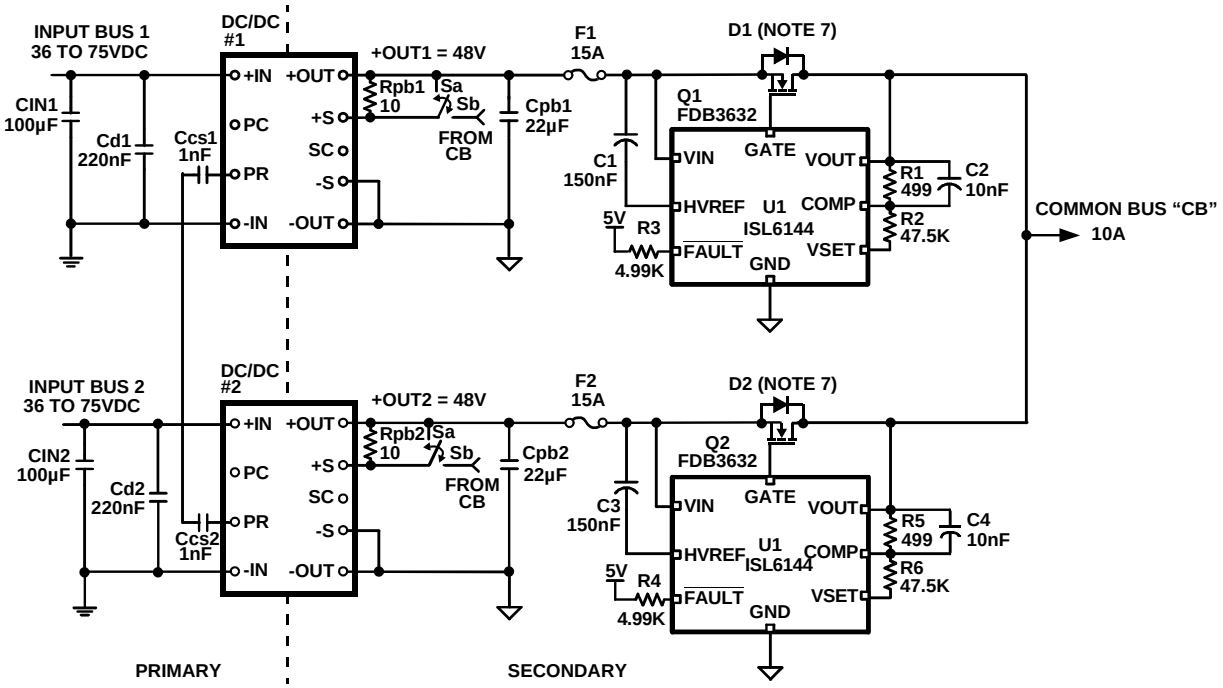


FIGURE 15. SLOW SPEED TURN OFF, VIN = 12V, COMMON LOAD IS SMPS (C_{LOAD} = 100µF) WITH EQUIVALENT 4A LOAD

Application Circuit

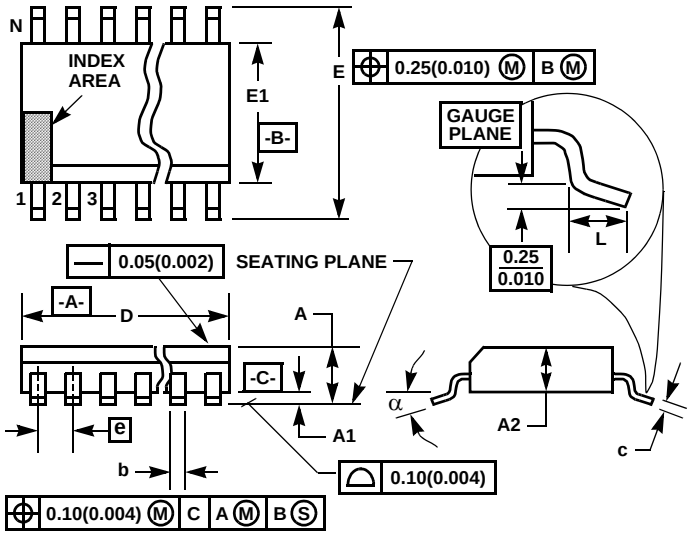


NOTES:

7. D1, D2 are parasitic MOSFET diodes.
8. Remote Sense pin (+S) on both DC/DC converters has to be connected either directly at the module output (Sa closed) or to the CB point (Sb closed). Connecting to CB is not recommended as it might cause Fault propagation in case of short circuit on a PS output.
9. F1, F2 are optional and can be eliminated depending on power system configuration and requirements.
10. DC/DC #1, 2 configuration is based on Vicor V48B48C250AN3.

FIGURE 16. APPLICATION CIRCUIT FOR A 1+1 REDUNDANT 48V SYSTEM

Thin Shrink Small Outline Plastic Packages (TSSOP)



NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-153-AB, Issue E.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.15mm (0.006 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. Dimension “b” does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total in excess of “b” dimension at maximum material condition. Minimum space between protrusion and adjacent lead is 0.07mm (0.0027 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact. (Angles in degrees)

M16.173

16 LEAD THIN SHRINK SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.043	-	1.10	-
A1	0.002	0.006	0.05	0.15	-
A2	0.033	0.037	0.85	0.95	-
b	0.0075	0.012	0.19	0.30	9
c	0.0035	0.008	0.09	0.20	-
D	0.193	0.201	4.90	5.10	3
E1	0.169	0.177	4.30	4.50	4
e	0.026 BSC		0.65 BSC		-
E	0.246	0.256	6.25	6.50	-
L	0.020	0.028	0.50	0.70	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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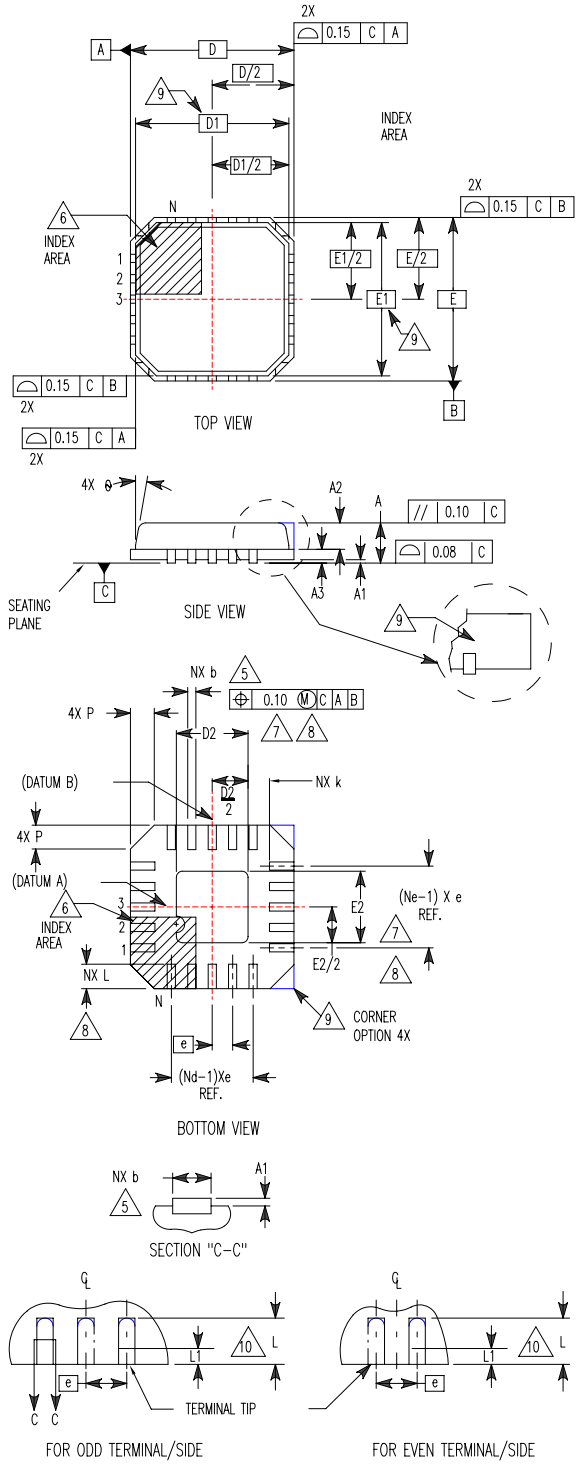
Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L20.5x5

20 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHC ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.38	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		20		2
Nd		5		3
Ne		5		3
P	-	-	0.60	9
θ	-	-	12	9

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NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.