

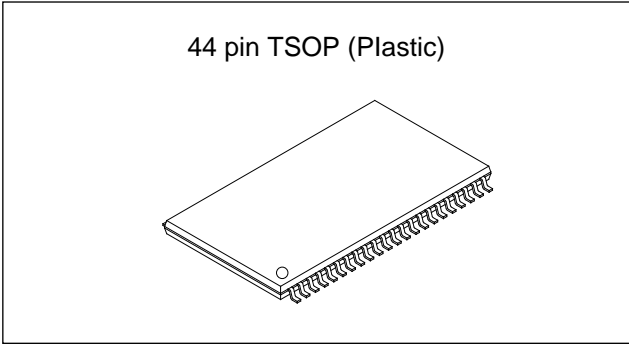
65536-word × 16-bit High Speed CMOS Static RAM Preliminary

Description

The CXK5T16100TM is a general purpose high speed CMOS static RAM organized as 65536-words by 16-bits.

Special feature are low power consumption and high speed.

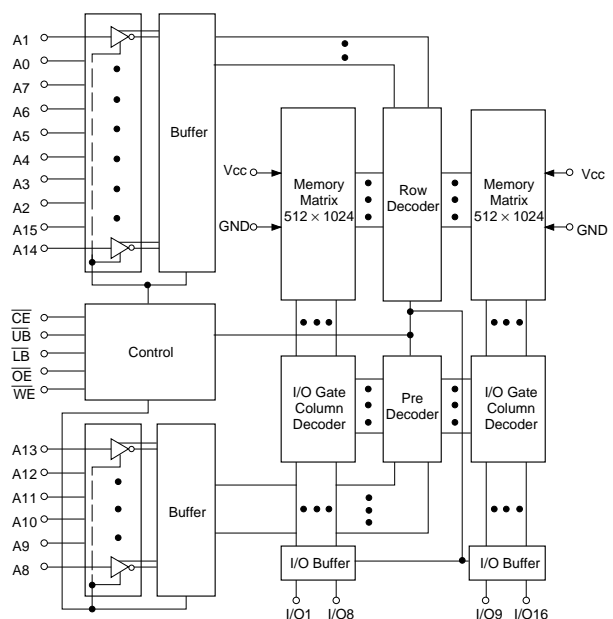
The CXK5T16100TM is a suitable RAM for portable equipment with battery back up.



Features

- Extended operating temperature range: -25 to +85°C
- Wide supply voltage range operation: 2.7 to 3.6V
- Fast access time: (Access time)
 - 3.0V operation 120ns (max.)
 - 3.3V operation 100ns (max.)
- Low power consumption operation:
 - Standby / DC operation
 - 1.6μW (typ.) / 3.3mW (typ.)
 - 100μW (max.) / 11mW (max.)
- Fully static memory ... No clock or timing strobe required
- Equal access and cycle time
- Common data input and output: three state output
- Directly LVTTTL compatible: All inputs and outputs
- Low voltage data retention: 2.0V (min.)
- 400mil 44pin TSOP (type II) package

Block Diagram



Function

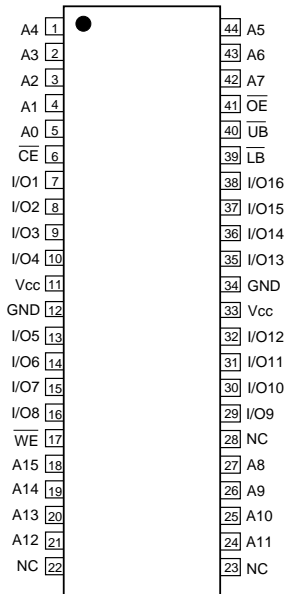
65536-word x 16-bit static RAM

Structure

Silicon gate CMOS IC

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Pin Configuration (Top View)



Pin Description

Symbol	Description
A0 to A15	Address input
I/O1 to I/O16	Data input/output
\overline{CE}	Chip enable input
\overline{LB}	Byte enable input (I/O1 to I/O8)
\overline{UB}	Byte enable input (I/O9 to I/O16)
\overline{WE}	Write enable input
\overline{OE}	Output enable input
Vcc	Power supply
GND	Ground
NC	No connection

Absolute Maximum Ratings

(Ta = 25°C, GND = 0V)

Item	Symbol	Rating	Unit
Supply voltage	Vcc	-0.5 to +4.6	V
Input voltage	V _{IN}	-0.5*1 to Vcc + 0.5	V
Input and output voltage	V _{I/O}	-0.5*1 to Vcc + 0.5	V
Allowable power dissipation	P _D	0.7	W
Operating temperature	Topr	-25 to +85	°C
Storage temperature	Tstg	-55 to +150	°C
Soldering temperature · time	Tsolder	235 · 10	°C · s

*1 V_{IN}, V_{I/O} = -3.0V Min. for pulse width less than 50ns.

Truth Table

\overline{CE}	\overline{OE}	\overline{WE}	\overline{LB}	\overline{UB}	I/O1 to I/O8	I/O9 to I/O16	Vcc Current
H	×	×	×	×	Not selected	Not selected	I _{SB1} , I _{SB2}
L	L	H	L	L	Read	Read	I _{CC1} , I _{CC2} , I _{CC3}
			L	H	Read	High-Z	I _{CC1} , I _{CC2} , I _{CC3}
			H	L	High-Z	Read	I _{CC1} , I _{CC2} , I _{CC3}
L	×	L	L	L	Write	Write	I _{CC1} , I _{CC2} , I _{CC3}
			L	H	Write	Not Write/Hi-Z	I _{CC1} , I _{CC2} , I _{CC3}
			H	L	Not Write/Hi-Z	Write	I _{CC1} , I _{CC2} , I _{CC3}
L	H	H	×	×	High-Z	High-Z	I _{CC1} , I _{CC2} , I _{CC3}
L	×	×	H	H	High-Z	High-Z	I _{CC1} , I _{CC2} , I _{CC3}

×: "H" or "L"

DC Recommended Operating Conditions

(Ta = -25 to +85°C, GND = 0V)

Item	Symbol	Vcc = 2.7 to 3.6V			Vcc = 3.3V ± 0.3V			Unit
		Min.	Typ.	Max.	Min.	Typ.	Max.	
Supply voltage	Vcc	2.7	3.3	3.6	3.0	3.3	3.6	V
Input high voltage	V _{IH}	2.4	—	Vcc + 0.3	2.0	—	Vcc + 0.3	
Input low voltage	V _{IL}	-0.3*1	—	0.4	-0.3*1	—	0.8	

*1 V_{IL} = -3.0V Min. for pulse width less than 50ns.

Electrical Characteristics

DC and operating characteristics

(Vcc = 2.7 to 3.6V, GND = 0V, Ta = -25 to +85°C)

Item	Symbol	Test condition	Min.	Typ.*2	Max.	Unit	
Input leakage current	I _{LI}	V _{IN} = GND to Vcc	-1	—	1	μA	
Output leakage current	I _{LO}	$\overline{CE} = V_{IH}$ or $\overline{UB} = V_{IH}$ or $\overline{LB} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$ V _{I/O} = GND to Vcc	-1	—	1	μA	
Operating power supply current	I _{CC1}	$\overline{CE} = V_{IL}$ V _{IN} = V _{IH} or V _{IL} I _{OUT} = 0mA	—	1	3	mA	
Average operating current	I _{CC2}	Min. cycle Duty = 100% I _{OUT} = 0mA	—	35	50	mA	
	I _{CC3}	Cycle time 1μs Duty = 100% I _{OUT} = 0mA $\overline{CE} \leq 0.2V$ V _{IL} ≤ 0.2V V _{IH} ≥ Vcc - 0.2V	—	10	20	mA	
Standby current	I _{SB1}	$\overline{CE} \geq V_{CC} - 0.2V$	-25 to +85°C	—	—	28	μA
			-25 to +70°C	—	—	14	
			+25°C	—	0.48	—	
	I _{SB2}	$\overline{CE} = V_{IH}$	—	0.03	0.6	mA	
Output high voltage	V _{OH}	I _{OH} = -2.0mA	2.4	—	—	V	
Output low voltage	V _{OL}	I _{OL} = 2.0mA	—	—	0.4	V	

*2 Vcc = 3.3V, Ta = 25°C

I/O capacitance

(Ta = 25°C, f = 1MHz)

Item	Symbol	Test conditions	Min.	Typ.	Max.	Unit
Input capacitance	C _{IN}	V _{IN} = 0V	—	—	8	pF
I/O capacitance	C _{I/O}	V _{I/O} = 0V	—	—	10	pF

Note) This parameter is sampled and is not 100% tested.

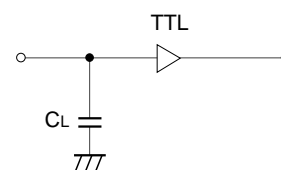
AC Characteristics

• AC test conditions

(Ta = -25 to +85°C)

Item	Conditions	
	V _{CC} = 2.7 to 3.6V	V _{CC} = 3.3V ± 0.3V
Input pulse high level	V _{IH} = 2.4V	V _{IH} = 2.2V
Input pulse low level	V _{IL} = 0.4V	V _{IL} = 0.6V
Input rise time	t _r = 5ns	t _r = 5ns
Input fall time	t _f = 5ns	t _f = 5ns
Input and output reference level	1.4V	1.4V
Output load conditions	C _L *1 = 100pF, 1TTL	C _L *1 = 100pF, 1TTL

*1 C_L includes scope and jig capacitances.



• Read cycle ($\overline{WE} = "H"$)

Item	Symbol	$V_{CC} = 2.7 \text{ to } 3.6\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		Unit
		Min.	Max.	Min.	Max.	
Read cycle time	t_{RC}	120	—	100	—	ns
Address access time	t_{AA}	—	120	—	100	ns
Chip enable access time (\overline{CE})	t_{CO}	—	120	—	100	ns
Byte enable access time ($\overline{UB}, \overline{LB}$)	t_{BO}	—	60	—	50	ns
Output enable to output valid	t_{OE}	—	60	—	50	ns
Output hold from address change	t_{OH}	10	—	10	—	ns
Chip enable to output in low Z (\overline{CE})	t_{LZ}	10	—	10	—	ns
Output enable to output in low Z (\overline{OE})	t_{OLZ}	5	—	5	—	ns
Byte enable to output in low Z ($\overline{UB}, \overline{LB}$)	t_{BLZ}	5	—	5	—	ns
Chip disable to output in high Z (\overline{CE})	t_{HZ}^{*1}	—	40	—	40	ns
Chip disable to output in high Z (\overline{OE})	t_{OHZ}^{*1}	—	35	—	35	ns
Byte disable to output in high Z ($\overline{UB}, \overline{LB}$)	t_{BHZ}^{*1}	—	35	—	35	ns

*1 t_{HZ} , t_{OHZ} and t_{BHZ} are defined as the time required for outputs to turn to high impedance state and are not referred to as output voltage levels.

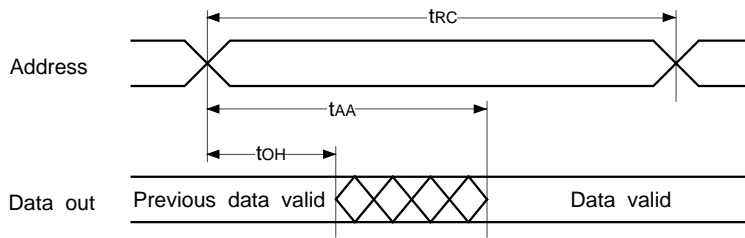
• Write cycle

Item	Symbol	$V_{CC} = 2.7 \text{ to } 3.6\text{V}$		$V_{CC} = 3.3\text{V} \pm 0.3\text{V}$		Unit
		Min.	Max.	Min.	Max.	
Write cycle time	t_{WC}	120	—	100	—	ns
Address valid to end of write	t_{AW}	100	—	80	—	ns
Chip enable to end of write	t_{CW}	100	—	80	—	ns
Byte enable to end of write	t_{BW}	100	—	80	—	ns
Data to write time overlap	t_{DW}	50	—	40	—	ns
Data hold from write time	t_{DH}	0	—	0	—	ns
Write pulse width	t_{WP}	70	—	70	—	ns
Address setup time	t_{AS}	0	—	0	—	ns
Write recovery time (\overline{WE})	t_{WR}	5	—	5	—	ns
Write recovery time ($\overline{CE}, \overline{UB}, \overline{LB}$)	t_{WR1}	5	—	5	—	ns
Output active from end of write	t_{OW}	5	—	5	—	ns
Write to output in high Z	t_{WHZ}^{*2}	—	40	—	40	ns

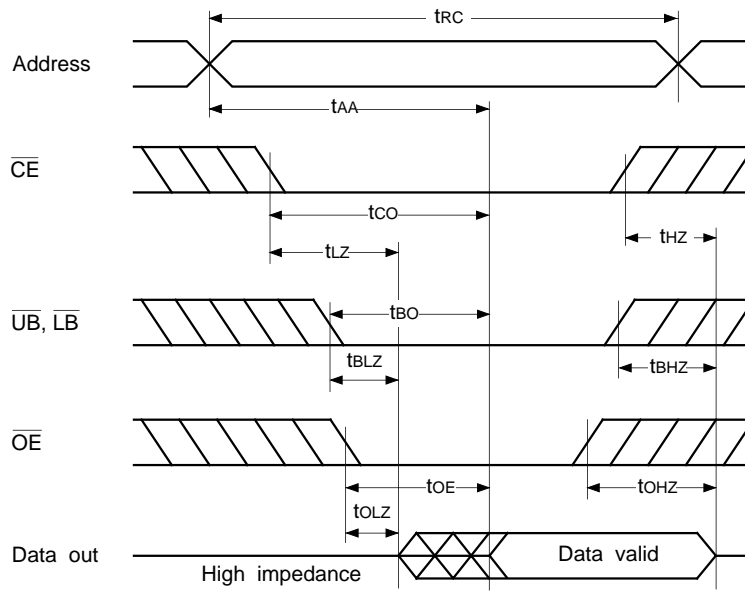
*2 t_{WHZ} is defined as the time required for outputs to turn to high impedance state and is not referred to as output voltage levels.

Timing Waveform

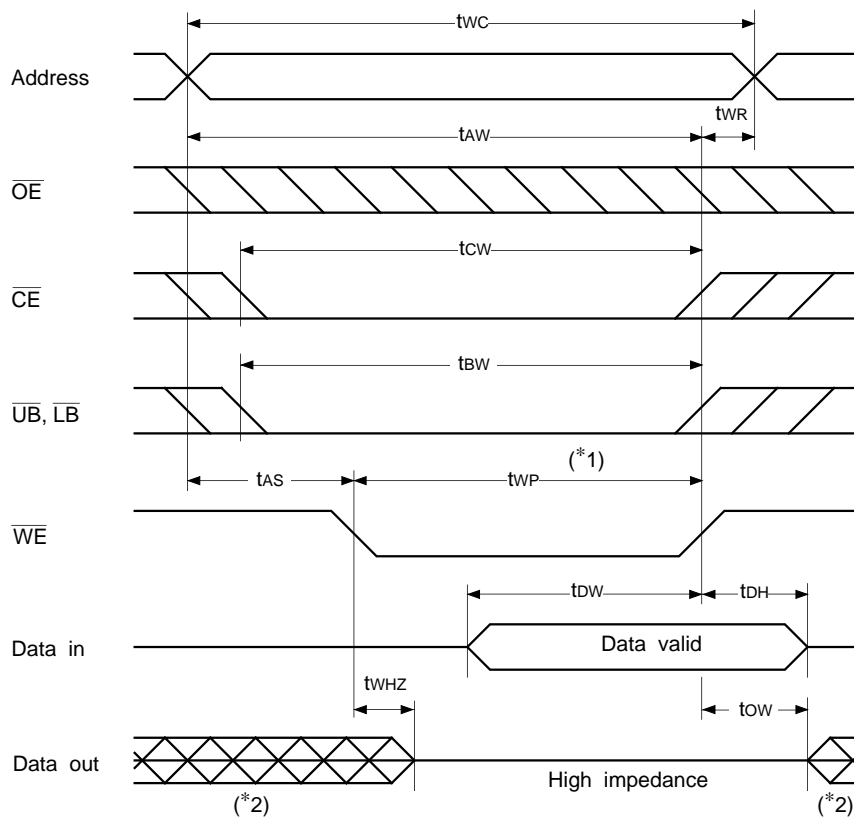
- Read cycle (1) : $\overline{CE} = \overline{OE} = V_{IL}$, $\overline{WE} = V_{IH}$, \overline{UB} and, or $\overline{LB} = V_{IL}$



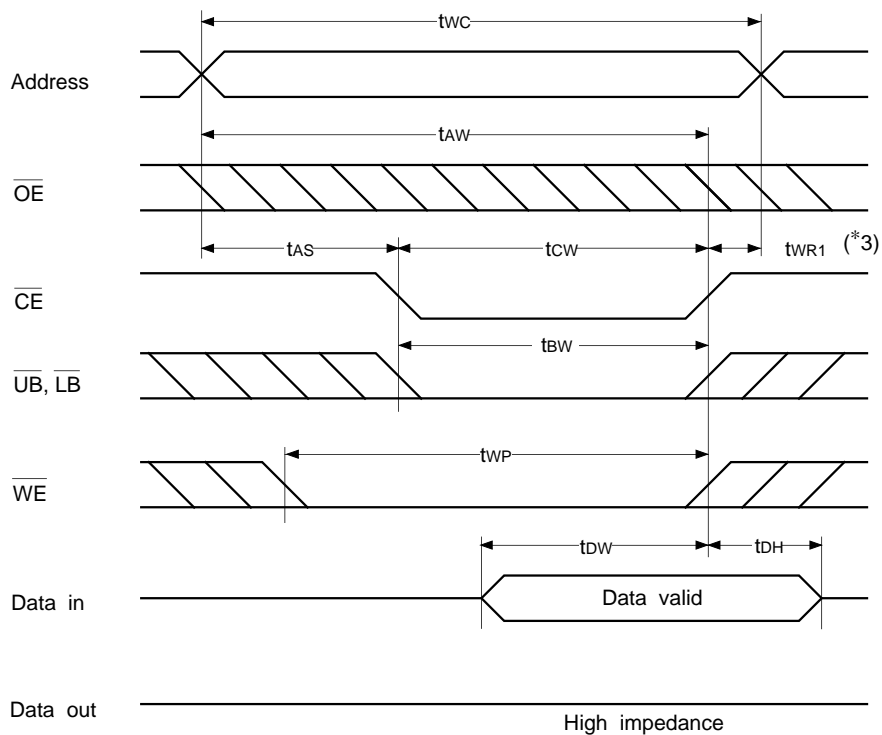
- Read cycle (2) : $\overline{WE} = V_{IH}$



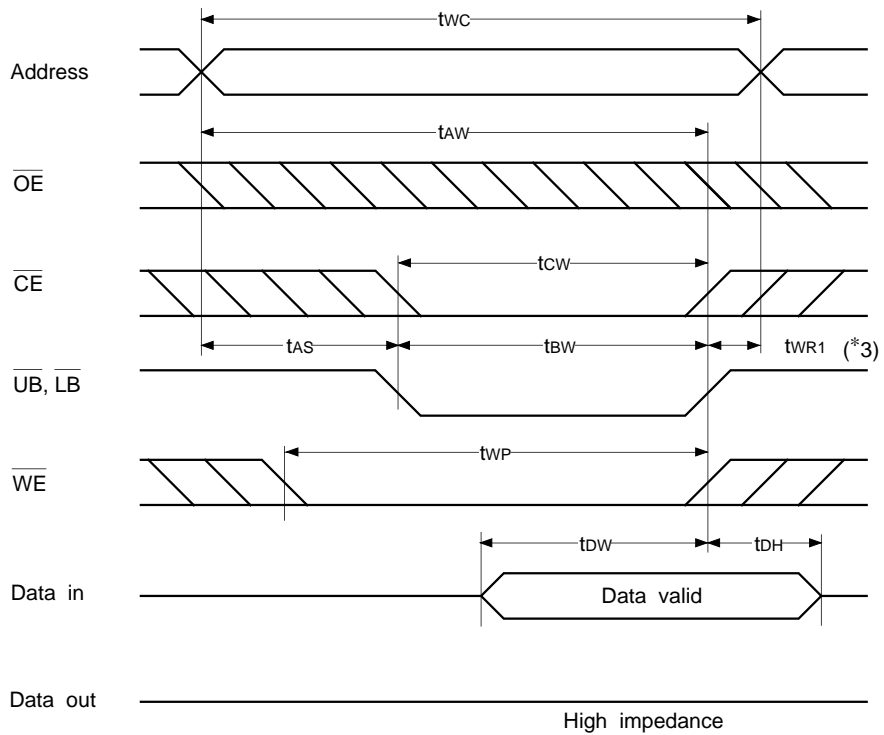
• Write cycle (1) : \overline{WE} control



• Write cycle (2) : \overline{CE} control



• Write cycle (3) : \overline{UB} , \overline{LB} control



*1 Write is executed when all of the \overline{CE} , \overline{WE} and (\overline{UB} and, or \overline{LB}) are at low simultaneously.

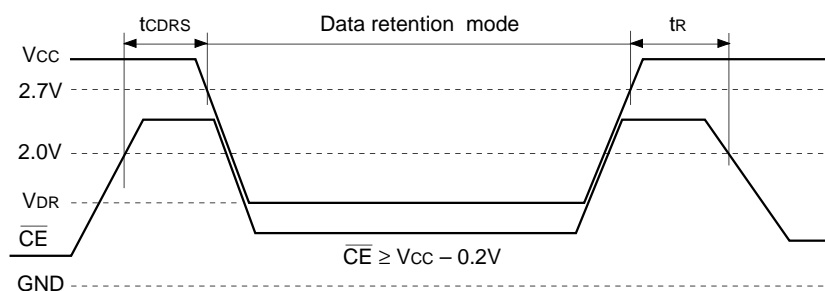
*2 Do not apply the data input voltage of the opposite phase to the output while I/O pin is in output condition.

*3 t_{WR1} (for I/O1 to 8) is tested from either the rising edge of \overline{CE} or \overline{LB} , whichever comes earlier, until the end of the write cycle.

t_{WR1} (for I/O9 to 16) is tested from either the rising edge of \overline{CE} or \overline{UB} , whichever comes earlier, until the end of the write cycle.

Data Retention Waveform

- Low supply voltage data retention waveform



Data Retention Characteristics

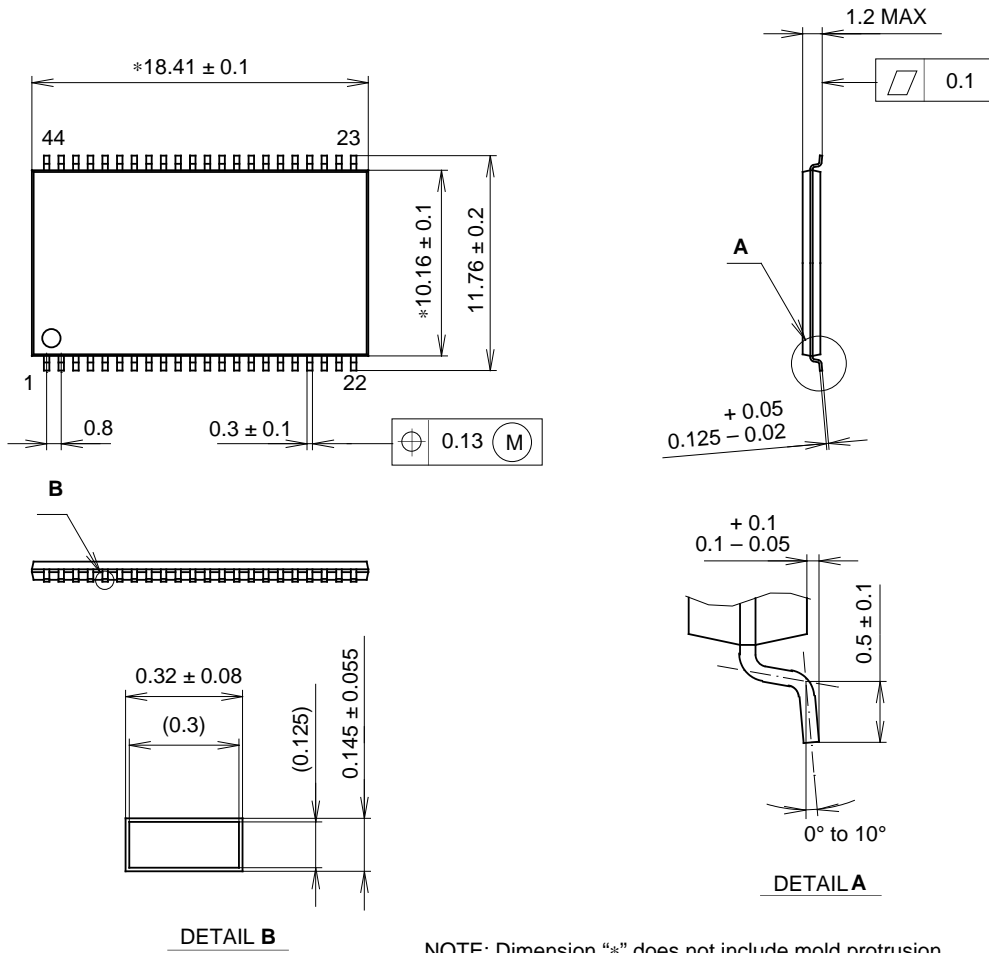
($T_a = -25$ to $+85^\circ\text{C}$)

Item	Symbol	Test condition	Min.	Typ.	Max.	Unit	
Data retention voltage	V_{DR}	$\overline{CE} \geq V_{CC} - 0.2V$	2.0	—	3.6	V	
Data retention current	I_{CCDR1}	$V_{CC} = 3.0V$	-25 to $+85^\circ\text{C}$	—	—	24	μA
			-25 to $+70^\circ\text{C}$	—	—	12	
			$+25^\circ\text{C}$	—	0.4	—	
	I_{CCDR2}	$V_{CC} = 2.0$ to $3.6V$	—	0.48*1	28	μA	
Data retention setup time	t_{CDRS}	Chip disable to data retention mode	0	—	—	ns	
Recovery time	t_R		5	—	—	ms	

*1 $V_{CC} = 3.3V$, $T_a = 25^\circ\text{C}$

Package Outline Unit : mm

44PIN TSOP (II) (PLASTIC) 400mil



NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	TSOP (II) -44P-L01	MOLDING COMPOUND	EPOXY / PHENOL RESIN
EIAJ CODE	TSOP (II) 044-P-0400-A	LEAD TREATMENT	SOLDER PLATING
JEDEC CODE	_____	LEAD MATERIAL	42 ALLOY
		PACKAGE WEIGHT	0.5g