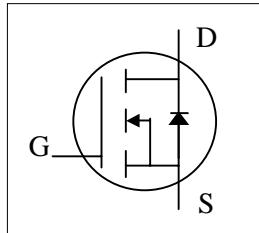




**Advanced Power
Electronics Corp.**

**N-CHANNEL ENHANCEMENT MODE
POWER MOSFET**

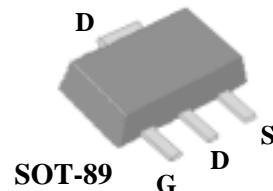
- ▼ Lower gate charge
- ▼ Capable of 2.5V gate drive
- ▼ Single Drive Requirement



BV_{DSS}	20V
$R_{DS(ON)}$	50m Ω
I_D	4A

Description

The Advanced Power MOSFETs from APEC provide the designer with the best combination of fast switching, ruggedized device design, ultra low on-resistance and cost-effectiveness.



Absolute Maximum Ratings

Symbol	Parameter	Rating	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-Source Voltage	± 16	V
$I_D @ T_C=25^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V^3$	4	A
$I_D @ T_C=100^\circ C$	Continuous Drain Current, $V_{GS} @ 4.5V^3$	2.5	A
I_{DM}	Pulsed Drain Current ¹	12	A
$P_D @ T_C=25^\circ C$	Total Power Dissipation	1.25	W
	Linear Derating Factor	0.01	W/ $^\circ C$
T_{STG}	Storage Temperature Range	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	-55 to 150	$^\circ C$

Thermal Data

Symbol	Parameter	Value	Unit
R_{thj-a}	Thermal Resistance Junction-ambient ³	Max. 100	$^\circ C/W$



Electrical Characteristics @ $T_j=25^\circ\text{C}$ (unless otherwise specified)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{\text{GS}}=0\text{V}, I_{\text{D}}=250\mu\text{A}$	20	-	-	V
$\Delta \text{BV}_{\text{DSS}}/\Delta T_j$	Breakdown Voltage Temperature Coefficient	Reference to 25°C , $I_{\text{D}}=1\text{mA}$	-	0.03	-	$\text{V}/^\circ\text{C}$
$R_{\text{DS}(\text{ON})}$	Static Drain-Source On-Resistance ²	$V_{\text{GS}}=10\text{V}, I_{\text{D}}=4\text{A}$	-	-	38	$\text{m}\Omega$
		$V_{\text{GS}}=4.5\text{V}, I_{\text{D}}=4\text{A}$	-	-	50	$\text{m}\Omega$
		$V_{\text{GS}}=2.5\text{V}, I_{\text{D}}=3\text{A}$	-	-	80	$\text{m}\Omega$
$V_{\text{GS}(\text{th})}$	Gate Threshold Voltage	$V_{\text{DS}}=V_{\text{GS}}, I_{\text{D}}=250\mu\text{A}$	0.7	-	1.5	V
g_{fs}	Forward Transconductance ²	$V_{\text{DS}}=5\text{V}, I_{\text{D}}=3\text{A}$	-	10	-	S
I_{DSS}	Drain-Source Leakage Current ($T_j=25^\circ\text{C}$)	$V_{\text{DS}}=20\text{V}, V_{\text{GS}}=0\text{V}$	-	-	1	μA
	Drain-Source Leakage Current ($T_j=70^\circ\text{C}$)	$V_{\text{DS}}=16\text{V}, V_{\text{GS}}=0\text{V}$	-	-	25	μA
I_{GSS}	Gate-Source Leakage	$V_{\text{GS}}= \pm 16\text{V}$	-	-	± 100	nA
Q_g	Total Gate Charge ²	$I_{\text{D}}=4\text{A}$	-	6	10	nC
Q_{gs}	Gate-Source Charge	$V_{\text{DS}}=16\text{V}$	-	1	-	nC
Q_{gd}	Gate-Drain ("Miller") Charge	$V_{\text{GS}}=4.5\text{V}$	-	2	-	nC
$t_{\text{d}(\text{on})}$	Turn-on Delay Time ²	$V_{\text{DS}}=10\text{V}$	-	8	-	ns
t_r	Rise Time	$I_{\text{D}}=1\text{A}$	-	9	-	ns
$t_{\text{d}(\text{off})}$	Turn-off Delay Time	$R_G=3.3\Omega, V_{\text{GS}}=5\text{V}$	-	13	-	ns
t_f	Fall Time	$R_D=10\Omega$	-	3	-	ns
C_{iss}	Input Capacitance	$V_{\text{GS}}=0\text{V}$	-	360	570	pF
C_{oss}	Output Capacitance	$V_{\text{DS}}=20\text{V}$	-	80	-	pF
C_{rss}	Reverse Transfer Capacitance	f=1.0MHz	-	65	-	pF

Source-Drain Diode

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
V_{SD}	Forward On Voltage ²	$I_S=1\text{A}, V_{\text{GS}}=0\text{V}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$I_S=4\text{A}, V_{\text{GS}}=0\text{V},$ $dI/dt=100\text{A}/\mu\text{s}$	-	18	-	ns
Q_{rr}	Reverse Recovery Charge		-	10	-	nC

Notes:

1. Pulse width limited by safe operating area.
2. Pulse width $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$.
3. Surface mount on FR4 board, $t \leq 10\text{s}$.

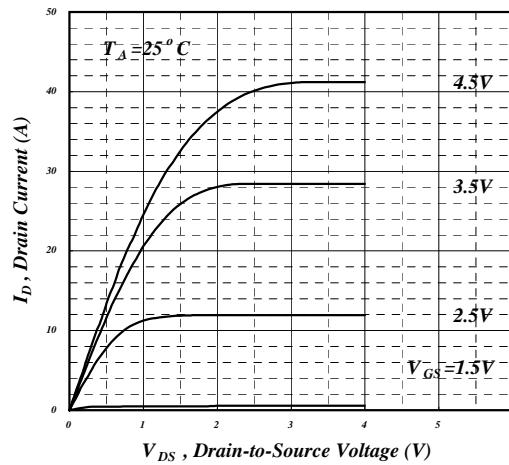


Fig 1. Typical Output Characteristics

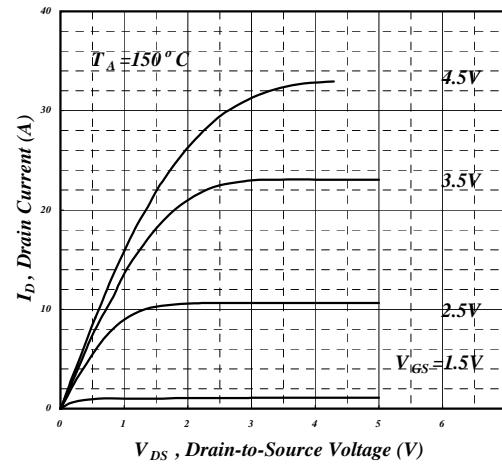


Fig 2. Typical Output Characteristics

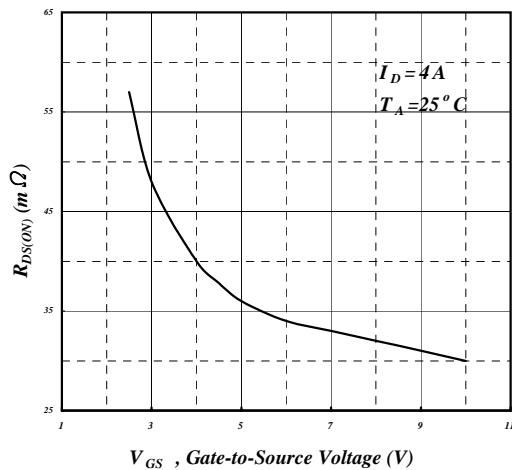


Fig 3. On-Resistance v.s. Gate Voltage

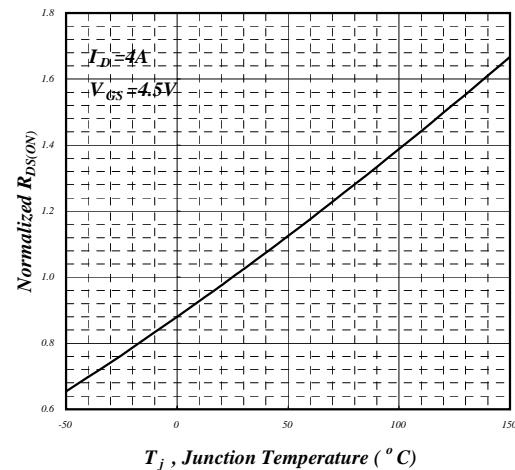


Fig 4. Normalized On-Resistance v.s. Junction Temperature

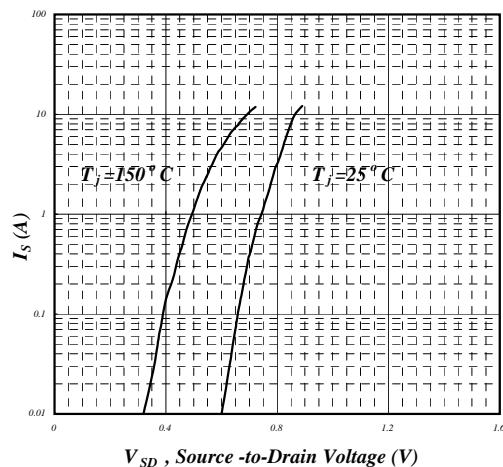


Fig 5. Forward Characteristic of Reverse Diode

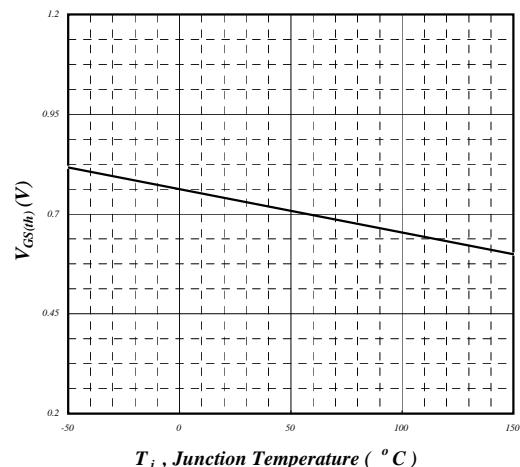


Fig 6. Gate Threshold Voltage v.s. Junction Temperature