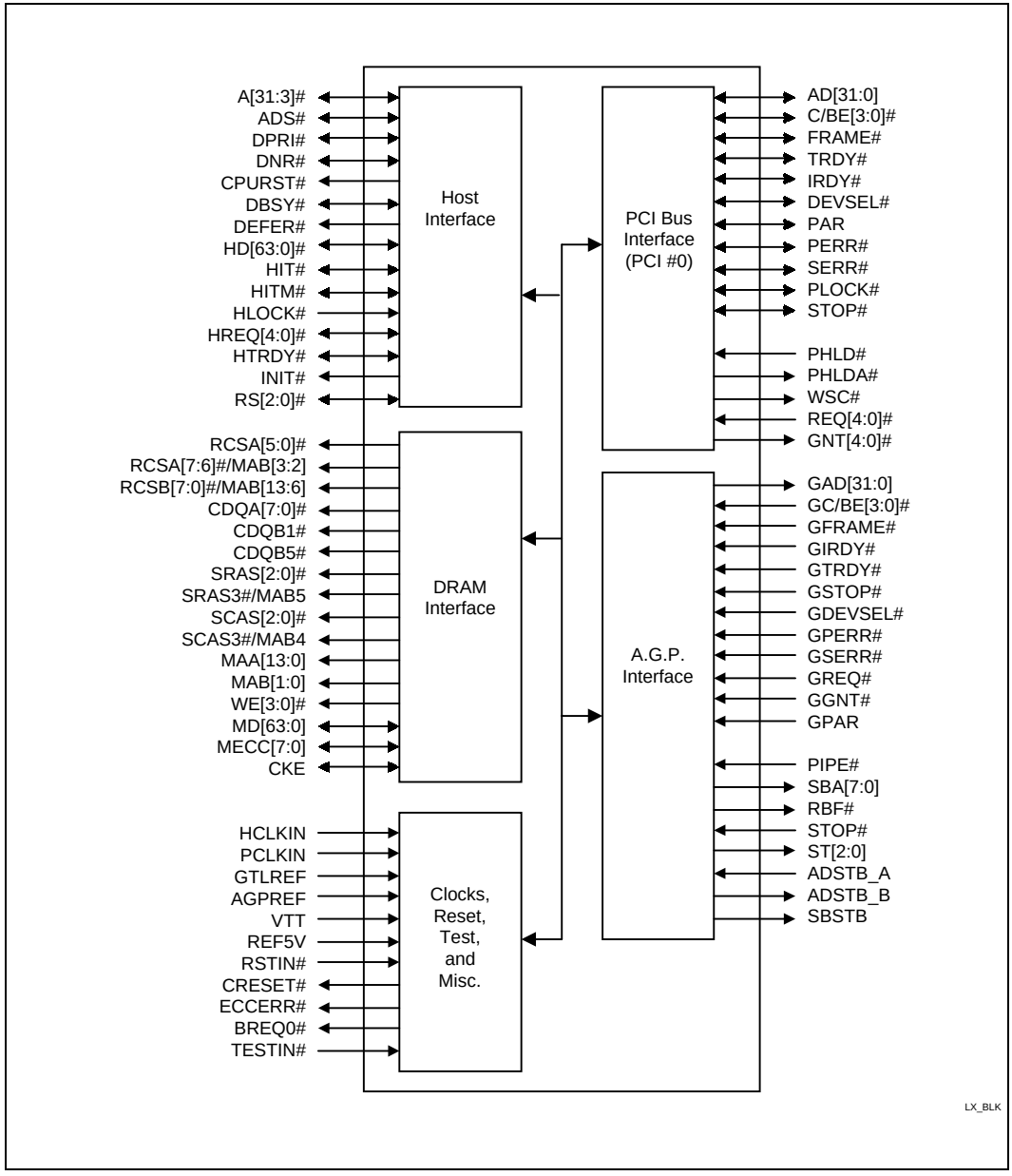
INTEL 440LX AGPSET: 82443LX PCI A.G.P. CONTROLLER (PAC)

- **Supports the Pentium® II Processor at a Bus Frequency of 66 MHz**
  - **— Supports 32-Bit Addressing**
  - **— Optimized In-Order and Request Queue**
  - **— Full Symmetric Multi-Processor (SMP) Protocol for Up to Two Processors**
  - **— Dynamic Deferred Transaction Support**
  - **— GTL+ Compliant Host Bus Supports WC Cycles**
- **Integrated DRAM Controller**
  - **— EDO (Extended Data Out), and Synchronous DRAM Support**
  - **— Supports a Maximum Memory Size of 512 MB With SDRAM, or 1 GB With EDO**
  - **— 64/72-bit Path to Memory**
  - **— Configurable DRAM Interface**
  - **— Support for Auto Detection of Memory Type: (DIMM Serial Presence Detect)**
  - **— 8 RAS Lines Available**
  - **— Support for 4-, 16- and 64-Mbit DRAM devices**
  - **— Support for Symmetrical and Asymmetrical DRAM Addressing**
  - **— Configurable Support for ECC/EC**
  - **— ECC With Single Bit Error Correction and Multiple Bit Error Detection**
  - **— Read-Around-Write Support for Host and PCI DRAM Read Accesses**
  - **— Supports 3.3V DRAMs**
- **Accelerated Graphics Port (A.G.P.) Interface**
  - **— A.G.P. Specification Compliant**
  - **— A.G.P. 66/133 MHz 3.3V Devices Supported**
  - **— Synchronous Coupling to the Host Bus Frequency**
- **PCI Bus Interface**
  - **— PCI Revision 2.1 Interface Compliant**
  - **— Greater Than 100-MBps Data Streaming for PCI-to-DRAM Accesses**
  - **— Integrated Arbiter With Multi-Transaction PCI Arbitration Acceleration Hooks**
  - **— Five PCI Bus Masters are Supported in Addition to the Host and PCI-to-ISA I/O Bridge**
  - **— Delayed Transaction Support**
  - **— PCI Parity Checking and Generation Support**
- **Data Buffering For Increased Performance**
  - **— Extensive CPU-to-DRAM, PCI-to-DRAM, and A.G.P.-to-DRAM Write Data Buffering**
  - **— CPU-to-A.G.P., PCI-to-A.G.P., and A.G.P.-to-PCI Data Buffering**
  - **— Write Combining Support for CPU-to-PCI Burst Writes**
  - **— Supports Concurrent Host, PCI, and A.G.P. Transactions to Main Memory**
- **System Management Mode (SMM) Compliant**
- **492 Pin BGA Package**

The 82443LX (PAC) is the first generation of desktop AGPset designed for the Pentium® II processor. The 82443LX PCI A.G.P. Controller (PAC) integrates a Host-to-PCI bridge, optimized DRAM controller and data path, and an Accelerated Graphics Port (A.G.P.) interface. A.G.P. is a high performance, component level interconnect, targeted at 3D graphics applications and based on a set of performance enhancements to PCI. The I/O subsystem portion of the PAC platform is based on the PIIX4, a highly integrated version of the Intel's PCI-to-ISA bridge family. PAC is developed as the ultimate Pentium II processor platform and is targeted for emerging 3D graphics and multimedia applications. The 440LX AGPset may contain design defects or errors known as errata which may cause the product to deviate from published specifications. Current characterized errata are available on request.

January 1998 Order Number: 290564-002



82443LX Block Diagram

CONTENTS

REVISION HISTORY

Date of Revision	Version	Description
July, 1997	-001	This is the first release of the 82443LX data sheet.
January, 1998	-002	1. The following sections have been added to the data sheet: - Section 4.3.5, Serial Presence Detect (SPD) for SDRAM - Section 4.3.6, Single Clock Command Mode for SDRAM - Section 4.3.7, Support for 2 and 4 Banks SDRAM 2. The pinout diagrams (Figures 32 and 33) are top views. 3. The package dimension diagram (Figure 35) has been updated to show the correct ball placement. In the previous revision of the data sheet, some ball placements were missing. 4. Electrical Characteristics Chapter has been added. This chapter contains absolute maximum ratings, thermal characteristics, DC characteristics, AC characteristics, and timing waveforms. 5. Minor text changes have been made throughout this document for clarification.

1.0. OVERVIEW

PAC integrates a Host-to-PCI bridge, optimized DRAM controller and data path, and an Accelerated Graphics Port (A.G.P.) interface. The A.G.P. is a high performance, component level interconnect, targeted at 3D graphics applications and based on a set of performance enhancements to PCI. The I/O subsystem portion of the PAC platform is based on the PIIX4, a highly integrated version of the Intel's PCI-to-ISA bridge family. The PAC is developed as the ultimate Pentium II processor platform and is targeted for emerging 3D graphics and multimedia applications. The PAC component includes the following functions and capabilities:

- Support for single and dual Pentium II processor configurations
- 64-bit GTL+ based Host Interface
- 32-bit Host address Support
- 64/72-bit Main Memory Interface with optimized support for SDRAM
- 32-bit PCI Bus Interface with integrated PCI arbiter
- A.G.P. Interface with up to 133-MHz data transfer capability
- Extensive Data Buffering between all interfaces for high throughput and concurrent operations

Figure 1 shows a block diagram of a typical platform based on the 440LX AGPset. The PAC host bus interface supports up to two Pentium II processors at 66 MHz. The physical interface design is based on the GTL+ specification. The PAC provides an optimized 72-bit DRAM interface (64-bit Data plus ECC). This interface supports 3.3V DRAM technologies. The PAC provides the interface to a PCI bus operating at 33 MHz. This interface implementation is compliant with PCI Rev 2.1 Specification. The PAC is the first Intel product that introduces the Accelerated Graphics Port interface. The PAC A.G.P. interface implementation is based on the A.G.P. Specification Rev 1.0. It can support up to 133-MHz data transfer rates.

PAC is designed to support the PIIX4 I/O bridge. PIIX4 is a highly integrated multi-functional component that supports the following functions and capabilities:

- PCI Rev 2.1 compliant PCI-to-ISA Bridge with support for 33-MHz PCI operations
- Deep Green Desktop Power Management Support
- Enhanced DMA controller
- 8259 Compatible Programmable Interrupt Controller
- System Timer functions
- Integrated IDE controller with Ultra DMA/33 support
- USB host interface with support for two USB ports
- System Management Bus (SMB) with support for DIMM Serial Presence Detect
- Support for an external I/O APIC component

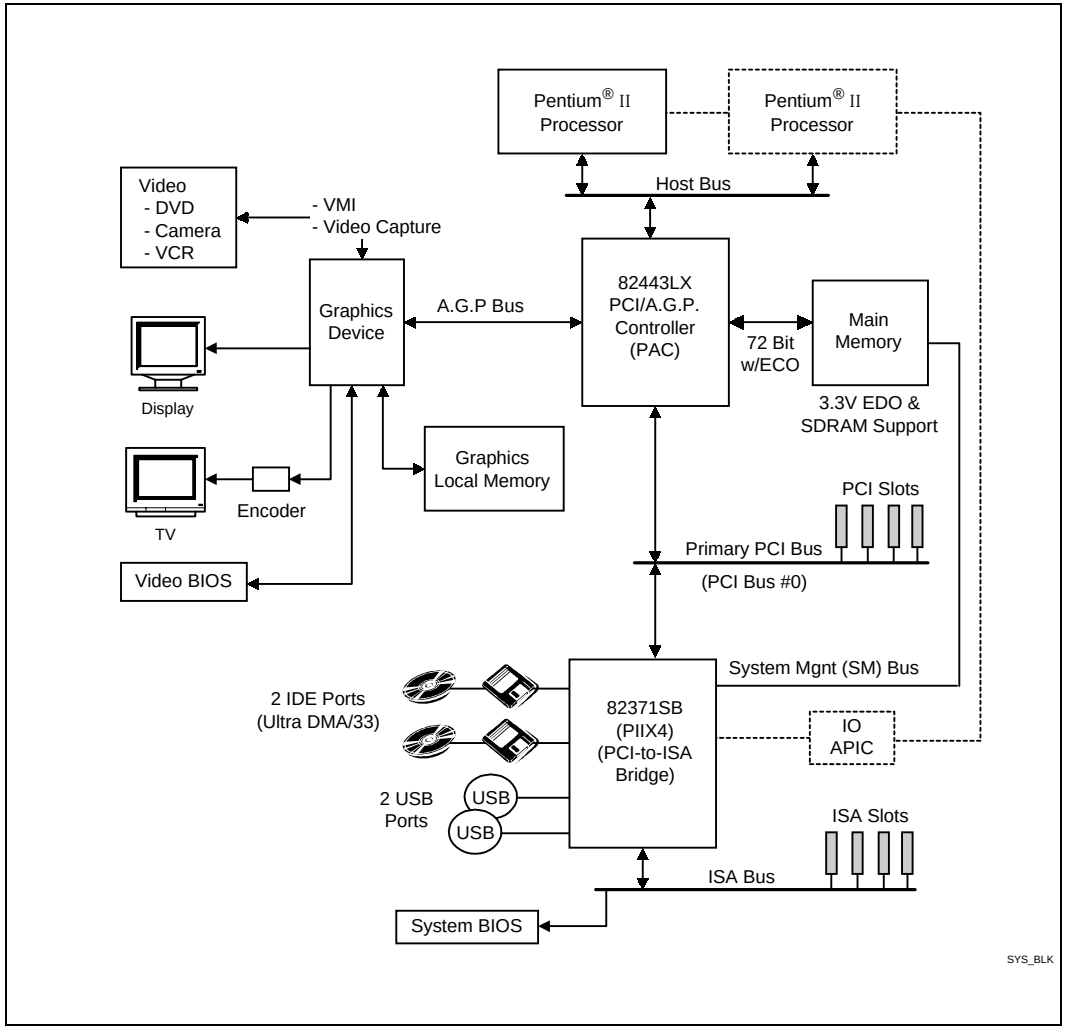


Figure 1. 440LX System Block Diagram

Host Interface

The Pentium II processor supports a second level cache size of 256K or 512K. All cache control logic is provided in the Pentium II processor. PAC supports a maximum of 32-bit address or 4-GB memory address space from the processor perspective. PAC provides bus control signals and address paths for transfers between the processor's host bus, PCI bus, Accelerated Graphics Port and main memory. The PAC supports a 4-deep in-order queue (i.e., it provides support for pipelining of up to four outstanding transaction requests on the host bus). Due to the system concurrency requirements, along with support for pipelining of address requests from the host bus, the PAC supports general request queuing for all three interfaces (Host, A.G.P. and PCI).

In Host-to-PCI transfers, depending on the PCI address space being accessed, the address will be either translated or directly forwarded on the PCI bus. If the access is to a PCI configuration space, the processor I/O cycle is mapped to a configuration cycle. If the access is to a PCI I/O or memory space, the processor address is passed without modification to the PCI bus, unless it hits a certain PCI memory address range (later referred in a document as the A.G.P. Aperture or Graphics Aperture) dedicated for graphics memory address space. If this space, or a portion of it, is mapped to main memory, then the address will be translated via the A.G.P. address remapping mechanism. The request will also be forwarded to the DRAM subsystem. Host cycles forwarded to A.G.P. are defined by the A.G.P. address map.

PAC also receives requests from PCI bus and A.G.P. bus initiators for access to main memory. If a target address is within the graphics aperture, then the request is translated into the appropriate memory address. A.G.P. accesses destined to the graphics aperture are not snooped on the host bus because coherency of aperture data is maintained by software. All accesses to the aperture, from the Host, PCI or A.G.P., are translated using the A.G.P. address remapping mechanism.

DRAM Interface

The PAC integrates a main memory controller that supports a 64/72-bit DRAM interface. The DRAM controller supports the following features:

- **DRAM type.** Extended Data Out (EDO) and Synchronous (SDRAM) DRAM controller optimized for dual-bank SDRAM organization
- **Memory Size.**
  - SDRAM: 8 MB to 512 MB with eight memory rows
  - EDO: 8 MB to 1 GB with eight memory rows
- **Addressing Type.** Symmetrical and Asymmetrical addressing
- **Memory Modules:** Single and double density DIMMs
- **Configurable DRAM Interface.**
  - Configuration #1: Large Memory Array
    - Support for single-sided DIMMs based on x4 DRAMs
    - Support for single and double-sided x8 and x16 DIMMs
    - External buffering is required on MAA[13:2] signals (Do not buffer MAA[1:0] or MAB[1:0])
    - 8 Row, 4 DS DIMM socket configuration
  - Configuration #2: Small Memory Array
    - Support for single and double-sided x8 and x16 DIMMs only
    - Two copies of MA[13:2] signals supplied by the PAC (no external buffers required on MA signals)
    - 6 Row, 3 DS DIMM socket configuration
- **DRAM device technology.** 4 Mbit, 16 Mbit and 64 Mbit
- **DRAM Speeds.** 50 ns and 60 ns for asynchronous EDO DRAM and equivalent SDRAM 66-MHz parameters for synchronous memory.

The 440LX AGPset also provides a DIMM plug-and-play support via Serial Presence Detect (SPD) mechanism. This is supported via the PIIX4 SMB interface. The PAC provides optional data integrity features including EC or ECC in the memory array. Error Checking (EC) mode provides single and multiple bit error detection. In ECC mode, the PAC provides error checking and correction of the data during reads from the DRAM. The PAC supports multiple-bit error detection and single-bit error correction when ECC mode is enabled and single/multi-bit error detection when correction is disabled. During writes to the DRAM, PAC generates ECC for the data.

Accelerated Graphics Port (A.G.P.) Interface

The 440LX is the first AGPset product designed to support the A.G.P. interface. The PAC A.G.P. implementation is compatible with the Accelerated Graphics Port Specification 1.0. PAC supports only a synchronous A.G.P. interface, coupling to the host bus frequency. The A.G.P. interface can reach a theoretical ~532 Mbytes/sec transfer rate. The actual bandwidth will be limited by the capability of the PAC memory subsystem.

PCI Interface

The PAC PCI interface is 33-MHz Revision 2.1 compliant and supports up to five external PCI bus masters in addition to the I/O bridge (PIIX4). PAC supports only synchronous PCI coupling to the host bus frequency.

Read/Write Buffers

PAC defines a sophisticated data buffering scheme to support the required level of concurrent operations and provide adequate sustained bandwidth between DRAM subsystem and all other system interfaces (CPU, A.G.P. and PCI).

System Clocking

PAC operates the host interface at 66 MHz, PCI at 33 MHz and A.G.P. at 66/133 MHz. Coupling between all interfaces and internal logic is done in a synchronous manner. PAC is not designed to support host bus frequencies lower than 66 MHz. The PAC clocking scheme uses an external clock synthesizer (which produces reference clocks for the host, A.G.P. and PCI interfaces).

I/O APIC

The I/O APIC is used to support dual processors. In configurations that use PIIX4 with a stand-alone I/O APIC component, PAC supports an external status output signal that can be used to control synchronization of interrupts.

2.0. SIGNAL DESCRIPTION

This section provides a detailed description of each signal for the PAC. The signals are arranged in functional groups according to their associated interface.

The "#" symbol at the end of a signal name indicates that the active, or asserted state occurs when the signal is at a low voltage level. When "#" is not present after the signal name, the signal is asserted when at the high voltage level.

The terms "assertion" and "negation" are used extensively. This is done to avoid confusion when working with a mixture of "active-low" and "active-high" signals. The term **assert** or **assertion,** indicates that the signal is active, independent of whether that level is represented by a high or low voltage. The term **negate,** or **negation** indicates that a signal is inactive.

The following notations are used to describe the signal type:

I	Input pin
O	Output pin
OD	Open Drain Output pin. This pin requires a pull-up to an appropriate voltage
I/O	Bi-directional input/output pin

The signal description also includes the type of buffer used for the particular signal:

GTL+	Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details
PCI	PCI bus interface signals. These signals are compliant with the PCI 5.0V Signaling Environment DC and AC Specifications
A.G.P.	A.G.P. interface signals. These signals are compatible with A.G.P. Signaling Environment DC and AC Specifications
LVTTL	Low Voltage TTL compatible signals. These are also 3.3V inputs and outputs.

Note that the Pentium II processor address and data bus signals are logically inverted signals. In other words, the actual values are inverted of what appears on the Pentium II processor bus. All control signals follow normal convention. A 0 (low voltage) indicates an active level if the signal is followed by # symbol, and a 1 (high voltage) indicates an active level if the signal has no # suffix.

2.1. PAC Signals

2.1.1. HOST INTERFACE SIGNALS

Table 1. Host Interface Signals

Name	Type	Description
A[31:3]#	I/O GTL+	**Address Bus:** A[31:3]# connect to the processor address bus. During host cycles, the A[31:3]# are inputs. PAC drives A[31:3]# during snoop cycles on behalf of PCI and A.G.P. initiators. Note that the address signals are inverted on the CPU bus.
ADS#	I/O GTL+	**Address Strobe:** The CPU bus owner asserts ADS# to indicate the first of two cycles of a request phase.
BPRI#	O GTL+	**Priority Agent Bus Request:** PAC is the only Priority Agent on the CPU bus. This signal is used to obtain the ownership of the address bus. Unless the HLOCK# signal was asserted, BPRI# has priority over symmetric bus requests and causes the current symmetric owner to stop issuing new transactions.
BNR#	I/O GTL+	**Block Next Request:** Used to block the current request bus owner from issuing a new request. This signal is used to dynamically control the CPU bus pipeline depth.
CPURST#	O GTL+	**CPU Reset.** The CPURST# pin is an output from PAC. PAC generates this signal based on the RSTIN# input signal (from PIIX4). The CPURST# allow the CPU(s) to begin execution in a known state.
DBSY#	I/O GTL+	**Data Bus Busy:** Used by the data bus owner to hold the data bus for transfers requiring more than one cycle.
DEFER#	O GTL+	**Defer: PAC** will generate a deferred response. PAC will also use the DEFER# signal to indicate a retry response on the CPU bus.
DRDY#	I/O GTL+	**Data Ready:** Asserted for each cycle that data is transferred.
HD[63:0]#	I/O GTL+	**Host Data:** These signals are connected to the CPU data bus. Note that the data signals are inverted on the CPU bus.
HIT#	I/O GTL+	**Hit:** Indicates that a caching agent holds an unmodified version of the requested line. Also, the target may extend the snoop window by driving HIT# in conjunction with HITM#.
HITM#	I/O GTL+	**Hit Modified:** Indicates that a caching agent holds a modified version of the requested line and that this agent assumes responsibility for providing the line. It is also driven in conjunction with HIT# to extend the snoop window.
HLOCK#	I GTL+	**Host Lock:** HLOCK# provides a mechanism to insure that cycles on the Host bus are atomic. All cycles initiated while HLOCK# is asserted are guaranteed atomic. (i.e., no PCI or A.G.P.-snoopable access to DRAM is allowed when HLOCK# signal is asserted by the CPU.)
HREQ[4:0]#	I/O GTL+	**Request Command:** Asserted during both clocks of request phase. In the first clock, the signals define the transaction type to a level of detail that is sufficient to begin a snoop request. In the second clock, the signals carry additional information to define the complete transaction type.

Table 1. Host Interface Signals

Name	Type	Description
HTRDY#	I/O GTL+	**Host Target Ready:** Indicates that the target of the CPU bus transaction is able to enter the data transfer phase.
INIT#	O LVTTL	**Initialization.** This is the output signal generated by the PAC after a CPU shutdown bus cycle, or after a soft reset is initiated by writing to the reset control register.
RS[2:0]#	I/O GTL+	**Response Signals:** Indicates type of response according to the following table: **RS[2:0] Response type** / **RS[2:0] Response type** 000 Idle state / 100 Hard Failure 001 Retry response / 101 No data response 010 Deferred response / 110 Implicit Writeback 011 Reserved / 111 Normal data response
HCLKIN	I LVTTL (2.5V)	**Host Clock In:** See *Clocks, Reset, and Miscellaneous Signals* Section.

NOTES:
All of the signals in the host interface are described in the Pentium II Processor data book. The preceding table highlights PAC specific uses of these signals.

2.1.2. DRAM INTERFACE SIGNALS

The PAC DRAM Controller supports two different memory configurations, which are selected during Reset via a strapping on the CKE pin. Configuration #1 is the large memory array. Configuration #2 is the small memory array.

Table 2. DRAM Interface Signals

Signal	Type	Description
RCSA[5:0]#	O LVTTL	**Row Address Strobe 5-0 (EDO):** These signals are used to latch the row address into the memory array. Each signal is used to select one DRAM row. These signals drive the DRAM array directly without any external buffers. **Chip Select 5-0 (SDRAM):** For the memory row configured with SDRAM, these pins perform the function of selecting the particular SDRAM components during the active state. Same function for Configuration #1 and Configuration #2. These signals have programmable buffer strengths for optimization under different signal loading conditions.

Table 2. DRAM Interface Signals

Signal	Type	Description
RCSA[7:6]# / MAB[3:2]	O LVTTL	**Configuration #1:** **Row Address Strobe 7-6 (EDO):** These signals are used to latch the row address into the memory array. Each signal is used to select one DRAM row. These signals drive the DRAM array directly without any external buffers. **Chip Select 7-6 (SDRAM):** For the memory row configured with SDRAM, these pins perform the function of selecting the particular SDRAM components during the active state. **Configuration #2:** **Extra Copy of Memory Address 3-2 (EDO/SDRAM):** MAB[3:2] are extra copies of Memory Address [3:2] and should be routed to the closest DIMM socket to the PAC(socket #0). MAB[3:2] will change value if the current or next access is directed to a memory address range mapped to DIMM socket #0. During accesses directed to DIMM socket #1 or #2, these signals will preserve the previously driven state. These signals behave logically and electrically the same way as MAA[3:2]. These signals have programmable buffer strengths for optimization under different signal loading conditions.
RCSB[7:0]# / MAB[13:6]	O LVTTL	**Configuration #1:** **Extra copy of Row Address Strobe 7-0 (EDO):** These signals are used to latch the row address into the memory array. Each signal is used to select one DRAM row. These signals drive the DRAM array directly without any external buffers. **Extra Copy of Chip Select 7-0 (SDRAM):** For the memory row configured with SDRAM, these pins perform the function of selecting the particular SDRAM components during the active state. **Configuration #2:** **Extra Copy of Memory Address 13-6 (EDO/SDRAM):** MAB[13:6] are extra copies of Memory Address [13:6] and should be routed to the closest DIMM socket to the PAC(socket #0). MAB[13:6] will change value if the current or next access is directed to a memory address range mapped to DIMM socket #0. During accesses directed to DIMM socket #1 or #2, these signals will preserve the previously driven state. These signals behave logically and electrically the same way as MAA[13:6]. These signals have programmable buffer strengths for optimization under different signal loading conditions.

Table 2. DRAM Interface Signals

Signal	Type	Description
CDQA[7:0]#	O LVTTL	**Column Address Strobe (EDO):** For EDOs, these signals are used to latch the column address into the memory array (CAS signals). They drive the DRAM array directly without external buffering. **Input/Output Data Mask (SDRAM):** These pins act as synchronized output enables during read cycles and as byte enables during write cycles. In the case of write cycles, byte masking functions are performed during the same clock that write data is driven (i.e., 0 clock latency). Same function for Configuration #1 and Configuration #2. These signals have programmable buffer strengths for optimization under different signal loading conditions.
CDQB1#	O LVTTL	**Extra Copy of Column Address Strobe 1 (EDO) / Input/Output Data Mask 1 (SDRAM):** This is a copy of CAS1#/DQM1 signal. It is used to balance the loading for CAS1#/DQM1 in the ECC memory configurations where this signal is double-loaded. Same function for Configuration #1 and Configuration #2. These signals have programmable buffer strengths for optimization under different signal loading conditions.
CDQB5#	O LVTTL	**Extra Copy of Column Address Strobe 5 (EDO) / Input/Output Data Mask 5 (SDRAM):** This is a copy of CAS5#/DQM5 signal. It is used to balance the loading for CAS5#/DQM5 in the ECC memory configurations where this signal is double-loaded. Same function for Configuration #1 and Configuration #2. These signals have programmable buffer strengths for optimization under different signal loading conditions.
SRAS[2:0]#	O LVTTL	**SDRAM Row Address Strobe (SDRAM):** The SRAS[2:0]# signals are multiple copies (for loading purposes) of the same logical SRASx signal used to generate SDRAM command. These commands are encoded on SRASx/SCASx/WE signals. When SRASx is sampled active at the rising edge of the SDRAM clock, the row address is latched into the SDRAMs. Same function for Configuration #1 and Configuration #2. These signals have programmable buffer strengths for optimization under different signal loading conditions.

Table 2. DRAM Interface Signals

Signal	Type	Description
SRAS3# / MAB5	O LVTTL	**Configuration #1:** **SDRAM Row Address Strobe 3 (SDRAM):** The SRAS3# signal is a copy (for loading purposes) of the same logical SRASx signal. It generates SDRAM commands encoded on SRASx/SCASx/WE signals. When SRASx is sampled active at the rising edge of the SDRAM clock, the row address is latched into the SDRAMs. **Configuration #2:** **Extra Copy of Memory Address 5 (EDO/SDRAM):** MAB[5] is an extra copy of Memory Address 5 and should be routed to the closest DIMM socket to the PAC(socket #0). MAB5 will change value if the current or next access is directed to a memory address range mapped to DIMM socket #0. During accesses directed to DIMM socket #1 or #2, these signals will preserve the previously driven state. This signal behaves logically and electrically the same way as MAA5. These signals have programmable buffer strengths for optimization under different signal loading conditions.
SCAS[2:0]#	O LVTTL	**SDRAM Column Address Strobe (SDRAM):** The SCAS[2:0]# signals are multiple copies (for loading purposes) of the same logical SCASx signal used to generate SDRAM commands. These commands are encoded on SRASx/SCASx/WE signals. When SCASx is sampled active at the rising edge of the SDRAM clock, the column address is latched into the SDRAMs. Same function for Configuration #1 and Configuration #2. These signals have programmable buffer strengths for optimization under different signal loading conditions.
SCAS3# / MAB4	O LVTTL	**Configuration #1:** **SDRAM Column Address Strobe 3 (SDRAM):** The SCAS3# signal is a physical copy (for loading purposes) of the same logical SCASx signal used to generate SDRAM command encoded on SRASx/SCASx/WE signals. When SCASx is sampled active at the rising edge of the SDRAM clock, the column address is latched into the SDRAMs. These signals drive the SDRAM array directly without any external buffers. **Configuration #2:** **Extra Copy of Memory Address 4 (EDO/SDRAM):** MAB[4] is an extra copy of Memory Address 4 and should be routed to the closest DIMM socket to the PAC(socket #0). MAB4 will change value if the current or next access is directed to a memory address range mapped to DIMM socket #0. During accesses directed to DIMM socket #1 or #2, these signals will preserve the previously driven state. This signal behaves logically and electrically the same way as MAA4. These signals have programmable buffer strengths for optimization under different signal loading conditions.

Table 2. DRAM Interface Signals

Signal	Type	Description
MAA[13:0]	O LVTTL	**Memory Address A (EDO/SDRAM):** MAA[13:0] is used to provide the multiplexed row and column address to DRAM. In configuration #1, the MA[13:2] lines are externally buffered to drive the address of the DRAM. External buffering is not required for these signals in Configuration #2. These signals have programmable buffer strengths for optimization under different signal loading conditions.
MAB[1:0]	O LVTTL	**Lower Memory Address Copy (EDO/SDRAM):** MAB[1:0] are the lower two bits of the memory address used to complete the row and column address to DRAM. These two bits are toggled during the burst phase for EDO cycles. MAB[1:0] will change value if the current or next access is directed to a memory address range mapped to DIMM socket #0 (the closest DIMM to the PAC). During accesses directed to DIMM socket #1 or #2, these signals will preserve the previously driven state. Same function for Configuration #1 and Configuration #2. These signals have programmable buffer strengths for optimization under different signal loading conditions.
WE[3:0]#	O LVTTL	**Write Enable Signal (EDO/SDRAM):** The WE[3:0]# signals are multiple copies (for loading purposes) of the same logical WEx# signal used to generate write strobe for EDO or SDRAM command. These commands are encoded on SRASx/SCASx/WEx# signals. These signals drive the DRAM array directly without any external buffers. Same function for Configuration #1 and Configuration #2. These signals have programmable buffer strengths for optimization under different signal loading conditions.
MD[63:0]	I/O LVTTL	**Memory Data (EDO/SDRAM):** These signals are used to interface to the DRAM data bus. These signals are internally connected to 20 kΩ pull-down resistors. These signals have programmable buffer strengths for optimization under different signal loading conditions.
MECC[7:0]	I/O LVTTL	**Memory ECC Data (EDO/SDRAM):** These signals carry Memory ECC data during DRAM access. These signals are internally connected to 20 kΩ pull-down resistors. These signals are outputs when PAC is writing to the DRAM; otherwise, they will be inputs. These signals have programmable buffer strengths for optimization under different signal loading conditions.

Table 2. DRAM Interface Signals

Signal	Type	Description
CKE	I/O LVTTL	**Clock Enable (SDRAM):** This signal is used to enable/disable the SDRAM clock (internally within the SDRAM component). When “high,” it enables normal SDRAM operation. When “low,” it deactivates the SDRAM clock and the SDRAM components enter Power Down Mode. Note that all SDRAM banks must be pre-charged before CKE is negated. The SDRAM Power Down Mode is used only for the PAC DRAM array power management. The CKE signal must be externally buffered, using a CMOS buffer, if SDRAM power management capability is utilized. Note that starting with the assertion of RSTIN#, and until 4 clocks of the CPURST# signal negation, this signal will be controlled as an input to allow sampling of the strap attached to this pin. CKE is connected to a 20 kΩ internal pull-down resistor.

2.1.3. PCI INTERFACE SIGNALS

Table 3. PCI Interface Signals

Name	Type	Description
Standard PCI Signals		
AD[31:0]	I/O PCI	**PCI Address/Data:** These signals are connected to the PCI address/data bus. Address is driven with FRAME# assertion and data is driven or received on following clocks.
DEVSEL#	I/O PCI	**Device Select:** Assertion indicates that a PCI target device has decoded its address as the target of the current access. PAC asserts DEVSEL# if the current access is: • within Main Memory • within the A.G.P. aperture • resides on the A.G.P. interface • a configuration cycle targeting the PAC As an input, this signal indicates whether a device on the bus has been selected.
FRAME#	I/O PCI	**Frame:** Assertion indicates the address phase of a PCI transfer. Negation indicates that one more data transfer is desired by the cycle initiator.
IRDY#	I/O PCI	**Initiator Ready:** Asserted when the initiator is ready for a data transfer.

Table 3. PCI Interface Signals

Name	Type	Description
C/BE[3:0]#	I/O PCI	**Command/Byte Enable:** The command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks. PCI Bus command encoding and types are listed below. **C/BE[3:0]# Command Type** / **C/BE[3:0]# Command Type** 0000 Interrupt Acknowledge / 1000 Reserved 0001 Special Cycle / 1001 Reserved 0010 I/O Read / 1010 Configuration Read 0011 I/O Write / 1011 Configuration Write 0100 Reserved / 1100 Memory Read Multiple 0101 Reserved / 1101 Reserved (Dual Addr Cyc) 0110 Memory Read / 1110 Memory Read Line 0111 Memory Write / 1111 Memory Write and Invalidate
PAR	I/O PCI	**Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0]. Even parity is generated across AD[31:0] and C/BE[3:0]#.
PERR#	I/O PCI	**PCI Parity Error:** Pulsed by an agent receiving data with bad parity one clock after PAR is asserted. PAC generates PERR# active if it detects a parity error on the PCI bus and the PERR# Enable bit in the PCICMD register is set.
PLOCK#	I/O PCI	**Lock:** Used to establish, maintain, and release resource locks on PCI.
TRDY#	I/O PCI	**Target Ready:** Asserted when the target is ready for a data transfer.
SERR#	I/O PCI	**System Error:** PAC asserts this signal to indicate an error condition. The SERR# assertion by the PAC is enabled globally via the SERRE bit of the PCICMD register. SERR# is asserted under the following conditions: 1. PAC asserts SERR# when it is configured for ECC operation, ECC error signaling via the SERR# mechanism is enabled via the ERRCMD_control register, and a single bit (correctable) ECC error or multiple bit (non-correctable) ECC error occurred. 2. PAC asserts SERR# for one clock when it detects a target abort during PAC initiated PCI cycle. 3. PAC can also assert SERR# when a PCI parity error occurs during the address phase if Parity Error Enable (register 04h, bit 6), SERR Enable (register 04h, bit 8), and SERR# on PCI Parity Error (register 90h, device 3) are set. 4. PAC can assert SERR# when it samples PERR# asserted on the PCI bus. This capability is controlled by bit 3 of the ERRCMD register. 5. PAC can assert SERR# when it detects assertion of G-SERR# input signal. This capability is controlled by bit 5 of the ERRCMD register.
STOP#	I/O PCI	**Stop:** Asserted by the target to request the master to stop the current transaction.
PCLKIN	I LVTTL	**PCI Clock In:** See *Clocks, Reset, and Miscellaneous Signals* Section.

Table 3. PCI Interface Signals

Name	Type	Description
PCI Arbitration Signals		
PHLD#	I PCI	**PCI Hold:** This signal comes from the PIIX4. It is the PIIX4 request for PCI bus ownership. PAC will flush and disable the CPU to PCI write buffers before granting the PIIX4 the PCI bus via PHLDA#. This ensures prevention of a bus deadlock condition between PCI and ISA.
PHLDA#	O PCI	**PCI Hold Acknowledge:** This signal is driven by the PAC to grant PCI bus ownership to the PIIX4 after CPU to PCI post buffers have been flushed and disabled.
WSC#	O PCI	**Write Snoop Complete:** This signal is asserted active to indicate that all of the snoop activity on the host bus on the behalf of the last PCI to DRAM write transaction (from PIIX4) is complete and that an APIC interrupt message can be sent. **NOTE** 1. This signal is used only in configurations where an I/O APIC is installed. 2. In non-APIC configurations, the WSC# mechanism can be completely disabled by bit 15 of the PACCFG register.
REQ[4:0]#	I PCI	**PCI Bus Request:** REQ[4:0]# are the PCI bus request signals used as inputs by the internal PCI arbiter. If any of the REQ[x]# signals are **NOT** used, these inputs must be pulled up to $V_{CC}3$.
GNT[4:0]#	O PCI	**PCI Grant:** GNT[4:0]# are the PCI bus grant output signals generated by the internal PCI arbiter.

NOTES:
All PCI interface signals conform to the PCI specification, Revision 2.1.

2.1.4. A.G.P. INTERFACE SIGNALS

The A.G.P. interface consists of a set of signals similar to PCI called A.G.P. FRAME# Protocol signals. In addition, there are 16 new signals added that constitute the A.G.P. sideband interface. The sections below are organized in five groups: 1.) A.G.P. Sideband Addressing Signals, 2.) A.G.P. Sideband Flow Control Signals, 3.) A.G.P. Sideband Status Signals, 4.) A.G.P. Sideband Clocking Signals (Strobes), and 5.) A.G.P. FRAME# Protocol Signals.

Table 4. A.G.P. Signals

Name	Type	Description
A.G.P. Sideband Addressing Signals[1]		
PIPE#	I A.G.P.	**Pipelined Operation:** PIPE# is asserted by the current master to indicate a full width address is to be queued by the target. The master queues one request each rising clock edge while PIPE# is asserted. When PIPE# is negated, no new requests are enqueued across the AD bus. PIPE# is a sustained tri-state signal from a *master (graphics controller)* and is an input to the PAC.
SBA[7:0]	I A.G.P.	**Sideband Address bus:** SBA[7:0] provide an additional bus to pass addresses and commands to the PAC from the A.G.P. master.

Table 4. A.G.P. Signals

Name	Type	Description
A.G.P. Sideband Flow Control Signals		
RBF#	I A.G.P.	**Read Buffer Full:** RBF# indicates if the master is ready to accept previously requested low priority read data. When RBF# is asserted, PAC is not allowed to return (low priority) read data to the A.G.P. master.
A.G.P. Sideband Status Signals		
ST[2:0]	O A.G.P.	**Status Bus:** ST[2:0] provide information from the arbiter to an A.G.P. master on what it may do. ST[2:0] only has meaning to the master when its GNT# is asserted. When GNT# is negated these signals have no meaning and must be ignored. **ST[2:0] Description** 000 Indicates that previously requested low priority read data is being returned to the master. 001 Indicates that previously requested high priority read data is being returned to the master. 010 Indicates that the master is to provide low priority write data for a previous enqueued write command. 011 Indicates that the master is to provide high priority write data for a previous enqueued write command. 100 Reserved 101 Reserved 110 Reserved 111 Indicates that the master has been given permission to start a bus transaction. The master may enqueue A.G.P. requests by asserting PIPE# or start a PCI transaction by asserting GFRAME#. ST[2:0] are always outputs from PAC and inputs to the master.
A.G.P. Sideband Clocking Signals (Strobes)		
ADSTB_A	I/O (t/s) A.G.P.	**AD Bus Strobe A:** Provides timing for double clocked data on GAD[15:0]**.** The agent that is providing data drives this signal. This signal has been labeled ADSTB_A in some documents.
ADSTB_B	I/O (t/s) A.G.P.	**AD Bus Strobe B:** Provides timing for double clocked data on the GAD[31:16]**.** The agent that is providing data drives this signal. This signal has been labeled ADSTB_B in some documents.
SBSTB	I A.G.P.	**Sideband Strobe:** Provides timing for SBA[7:0]. It is always driven by the A.G.P. compliant master.
A.G.P. FRAME# Protocol Signals (similar to PCI)[2]		
GFRAME#	I/O A.G.P.	**A.G.P. Frame:** Assertion indicates the address phase of a A.G.P. FRAME# protocol transfer. Negation indicates that one more data transfers are desired by the cycle initiator. GFRAME# remains negated by an internal pull up resistor.

Table 4. A.G.P. Signals

Name	Type	Description
GIRDY#	I/O A.G.P.	**A.G.P. Initiator Ready:** For A.G.P. Frame# protocol transactions, this signal is asserted when the initiator is ready for a data transfer. It indicates that the A.G.P. compliant master is ready to provide *all* write data for the first block of a sideband transaction.
GTRDY#	I/O A.G.P.	**A.G.P. Target Ready:** For A.G.P. Frame# protocol transactions, this signal is asserted when the target is ready for a data transfer. It indicates the A.G.P. compliant target is ready to provide read data for the first block of a sideband transaction .
GSTOP#	I/O A.G.P.	**A.G.P. Stop:** Asserted by the target to request the master to stop the current transaction.
GDEVSEL#	I/O A.G.P.	**A.G.P. Device Select:** Assertion indicates that a A.G.P. target device has decoded its address as the target of the current access. PAC asserts DEVSEL# if the current access is: • within Main Memory • resides on the PCI interface As an input, this signal indicates whether a device on the bus has been selected.
GPERR#	I/O A.G.P.	**A.G.P. Parity Error:** Pulsed by an agent receiving data with bad parity one clock after GPAR is asserted.
GSERR#	I A.G.P.	**A.G.P. System Error:** May be used by A.G.P. master to report a catastrophic error. Routed internally within PAC to the primary PCI bus SERR# signal (direct connection between GSERR# 66-MHz signal and SERR# 33-MHz signal is not possible).
GREQ#	I A.G.P.	**A.G.P. Bus Request:** Used to request access to the bus to initiate an A.G.P. request.
GGNT#	O A.G.P.	**A.G.P. Grant (additional information is provided on ST[2:0]):** The additional information indicates that the selected master is the recipient of previously requested read data (high or normal priority). It is to provide write data (high or normal priority) for a previously enqueued write command or has been given permission to start an A.G.P. bus transaction .
GAD[31:0]	I/O A.G.P.	**A.G.P. Address / Data:** The standard address and data lines. Address is driven with FRAME# assertion; data is driven or received in following clocks.
GC/BE[3:0]#	I/O A.G.P.	**A.G.P. Command / Byte Enables:** For FRAME# protocol transactions, the command is driven with FRAME# assertion. Byte enables corresponding to supplied or requested data are driven on following clocks. The encoding is the same as for PCI transactions. Provides command information (different commands than PCI) when requests are being enqueued using PIPE#. These signals provide valid byte information during A.G.P. write transactions and is driven by the master. The target drives “0000” during the return of A.G.P. read data and is ignored by the A.G.P. compliant master.

Table 4. A.G.P. Signals

Name	Type	Description
GPAR	I/O A.G.P.	**A.G.P. Parity:** A single parity bit is provided over AD[31:0] and C/BE[3:0]#. Even parity is generated across AD[31:0] and C/BE[3:0]#. Not used on A.G.P. sideband transactions.

NOTES:

1. **A.G.P. Addressing Signals.** This section of the table contains two mechanisms to enqueue requests by the A.G.P. master. Note that the master can only use one mechanism. When PIPE# is used to enqueue addresses the master is not allowed to enqueue addresses using the SB bus. For example, during configuration time, if the master indicates that it can use either mechanism, the configuration software will indicate which mechanism the master will use. Once this choice has been made, the master continues to use the mechanism selected until the master is reset (and reprogrammed) to use the other mode. This change of modes is not a dynamic mechanism, but rather a static decision when the device is first being configured after reset.
2. **A.G.P. FRAME# Protocol Signals (similar to PCI):** These signals, for the most part, are redefined when used in A.G.P. transactions using A.G.P. sideband protocol extensions. For transactions on the A.G.P. interface using FRAME# protocol, these signals preserve PCI semantics. The exact role of these signals during A.G.P. sideband transactions is defined in this section of the table.
   a. RSTIN# is used to reset A.G.P. interface logic within the PAC. The A.G.P. agent will use a system PCIRST# signal provided by the I/O bridge (i.e., PIIX4) as an input to reset its internal logic.
   b. LOCK# signal is not supported on the A.G.P. interface (even for FRAME# protocol operations).
   c. **Pins During A.G.P. FRAME# protocol Transactions.** Signals described in a previous table behave according to PCI 2.1 specifications when used to perform A.G.P. FRAME# protocol transactions on the A.G.P. Interface.

2.1.5. CLOCKS, RESET, AND MISCELLANEOUS SIGNALS

Table 5. Clocks, Reset, Reference Voltage, and Miscellaneous Signals

Name	Type	Description
HCLKIN	I LVTTL (2.5V)	**Host Clock In:** This pin receives a buffered host clock. This clock is used by all of the PAC logic that is in the Host clock domain.
PCLKIN	I LVTTL	**PCI Clock In:** This is a buffered PCI clock reference that is synchronously derived by an external clock synthesizer component from the host clock (divide-by-2). This clock is used by all of the PAC logic that is in the PCI clock domain.
GTLREF	I	**GTL+ Reference Voltage:** This is the reference voltage derived from the termination voltage to the pull-up resistors and determines the noise margin for the signals. This signal goes to the reference input of the GTL+ sense amp on each GTL+ input or I/O pin.
AGPREF	I	**A.G.P. Reference Voltage.**
V_{TT}	I	**GTL+ Termination Reference Voltage.**
REF5V	I	**5V Reference Voltage:** This reference pin provides a reference voltage for the 5V safe PCI Bus interface.

Table 5. Clocks, Reset, Reference Voltage, and Miscellaneous Signals

Name	Type	Description
RSTIN#	I TTL	**Reset Input:** This input is controlled by the I/O bridge (i.e., PIIX4). It is activated for both power-on reset sequences and software-invoked reset sequences. This signal is used as a trigger for the PAC generated CPURST# signal. The RSTIN# is synchronous to 33-MHz PCI clock. Upon detection of RSTIN# assertion, PAC asserts the CPURST# signal. PAC holds CPURST# asserted for 1 msec after detecting the negation of RSTIN#. RSTIN# (PCIRST#) must be inverted and routed to OE# on the DIMM sockets as well as the OE# on the tri-state buffer that is buffering CKE.
CRESET#	O LVTTL	**CHIP RESET:** This signal is a delayed version of CPURST#. CRESET# is asserted with CPURST# and its negation is delayed for 2 Host Clocks.
ECCERR#	O TTL	**ECC Error:** This signal is asserted when an ECC error is detected, either recoverable (single bit) ECC error or non-recoverable (multi-bit) ECC error. It is negated after software clears the ECC error status flags in the ERRSTS register. In the non-ECC configuration (i.e., when PACCFG bits[8:7]=00), this signal is disabled (i.e., masked). This signal can be connected to an IRQ input of the 8259 compatible PIC, or I/O APIC, SMI-input on PIIX4, or to the NMI system logic. This signal is internally connected to a 20 kΩ pull-down resistor.
BREQ0#	O GTL+	**Symmetric Agent Bus Request:** Asserted by PAC when CPURST# is asserted to configure the symmetric bus agents. BREQ0# is negated 2 host clocks after CPURST# is negated.
TESTIN#	I TTL	**TEST Input:** Test Input pin to enable the Tri-State Test Mode and NAND Tree Test Mode.

2.2. Power-Up/Reset Strapping Options

Below is the list of power-up options that are loaded into PAC during system reset. PAC floats all the signals connected to straps during system reset (RSTIN# active) and keeps them floated for a minimum of 4 host clocks after the end of the reset sequence. The first column lists the signal that is sampled to obtain the strapping option. The second column shows the register the strapping option is loaded into. The third column is a description of what functionality the strapping selects.

NOTE

All signals used to select power-up strap options are connected to internal pull-down resistors of approximately 20 kohms. This selects the default mode by forcing a logical 0 on the signal during reset. To enable different modes, external pull-up resistors of approximately 5 kohms can be connected to particular signals. These pull-up resistors should be connected to the 3.3V power supply. The GTL+ signals are connected to V_{TT} through the GTL+ termination resistors. The CPU bus straps controlled by the PAC (e.g., A7#) are driven active at least six clocks prior to the active-to-inactive edge of CPURST# and driven inactive four clocks after the active-to-inactive edge of the CPURST#.

Table 6. Power-Up/Reset Strapping Options

Signal	Register Name/bit	Description
CKE	none	**DRAM Interface Configuration.** This strapping is used to select between DRAM interface configurations #1 and #2. CKE is not driven by PAC during reset (from assertion of RSTIN# until 4 clocks after negation of CPURST#). It is sampled upon the negation of the RSTIN# signal. If CKE is 0(default), the mode will be configuration #2. If CKE is 1, the mode will be configuration #1.

NOTES:

1. All signals listed above are connected to internal pull-down resistors.

2.3. State of PAC Output and Bi-directional Signals During Hard Reset

Table 7 shows the PAC signal state during a hard reset. Hard reset is defined as CPURST# being driven low by the PAC.

Table 7. Signals During Reset

Signal Name	State
Host Signals	
A[31:3]	not driven[1]
ADS#	not driven
BNR#	not driven
BPRI#	not driven
CPURST#	driven active
DBSY#	not driven
DEFER#	not driven
DRDY#	not driven
HIT#	not driven
HITM#	not driven
HLOCK#	not driven
HREQ[4:0]#	not driven
HTRDY#	not driven
INIT#	not driven[2]
RS[2:0]	not driven
BREQ0#	Low[3]
HD[63:0]#	not driven
PCI Signals and PCI Sideband Signals	
AD[31:0]#	Low
C/BE[3:0]#	Low
PAR	Low
DEVSEL#	Tri-state
FRAME#	Tri-state

Signal Name	State
GDEVSEL#	Tri-state
GFRAME#	Tri-state
GGNT#	Tri-state
GIRDY#	Tri-state
GPERR#	Tri-state
GREQ#	—
GSERR#	Tri-state
GSTOP#	Tri-state
GTRDY#	Tri-state
PIPE#	Tri-state
SBA[7:0]	Tri-state
RBF#	—
ST[2:0]	Low
AD_STBA	Tri-state
AD_STBB	Tri-state
SBSTB	Tri-state
DRAM Signals	
CDQA[7:0]#	High
CDQB1#	High
CDQB5#	High
RCSA[5:0]#	High
MAA[13:0]	Low
MAB[1:0]	Low
RCSB[7:0]#/MAB[13:6]	High / —

Table 7. Signals During Reset

Signal Name	State
GNT[4:0]#	Tri-state
IRDY#	Tri-state
PERR#	Tri-State
PHLD#	—
PHLDA#	Tri-state
PLOCK#	Tri-state
REQ[4:0]#	—
SERR#	Tri-state
STOP#	Tri-state
TRDY#	Tri-state
WSC#	High
A.G.P. Signals and A.G.P. Sideband Signals	
GAD[31:0]#	Low
GC/BE[3:0]#	Low
GPAR	Low

Signal Name	State
RCSA[7:6]#/MAB[3:2]	High / —
SRAS3#/MAB5	High / —
SCAS3#/MAB4	High / —
WE[3:0]#	High
SRAS[2:0]#	High
SCAS[2:0]#	High
MD[63:0]	Low
MECC[7:0]	Low
CKE	Strapped Value
Miscellaneous Signals	
ECCERR#	Low
CRESET	Low

NOTES:

1. If MECC was sampled low during the rising edge of PWROK, PAC is responsible for driving A7# active at least 6 host clocks prior to the CPURST# active-to-inactive transition. PAC drives A7# inactive 4 host clocks after the rising edge of CPURST#. If MECC was sampled high during the rising edge of PWROK, then A7# will not be driven.
2. INIT is driven active (low) for a software generation of BIST.
3. BREQ0# must stay asserted (low) for a minimum of 2 host clocks after the rising edge of CPURST#. PAC then releases (tri-states) the BREQ0# signal.
4. "—" is "don't care."

3.0. REGISTER DESCRIPTION

PAC contains two sets of software accessible registers, accessed via the Host CPU I/O address space:

1. Two control registers that are I/O mapped in the CPU I/O space. These registers provide access to PCI and Accelerated Graphics Port (A.G.P.) configuration space.
2. Two sets of configuration registers residing within PAC are partitioned into two “logical” PCI device register sets (“logical” since they reside within a single physical package). The first being dedicated to the Host-to-PCI Bridge function (controls the PCI, DRAM and A.G.P. functions, and other AGPset operating parameters). The second set being dedicated to the standard PCI-to-PCI Bridge function that controls the A.G.P. interface address mapping and PCI-standard configuration parameters of A.G.P. (i.e., A.G.P. is seen as another PCI bus from a configuration point of view).

NOTE

This configuration scheme is necessary to accommodate the existing and future software configuration model. (The term “**virtual**” is used to designate that no real physical embodiment of the PCI-to-PCI Bridge functionality exists within PAC, but that PAC’s internal configuration register sets are organized in the particular manner to create that impression to the standard configuration software.) PAC supports PCI configuration space access using the mechanism denoted as configuration mechanism 1 in the PCI specification.

PAC registers (both Control and Configuration registers) are accessible by the Host CPU. The registers can be accessed as Byte, Word (16-bit), or DWord (32-bit) quantities, with the exception of CONFADD which can only be accessed as a DWord. All multi-byte numeric fields use “little-endian” ordering (i.e., lower addresses contain the least significant parts of the field). The following nomenclature is used for access attributes:

RO **Read Only**. If a register is read only, writes to this register have no effect.
R/W **Read/Write**. A register with this attribute can be read and written.
R/WC **Read/Write Clear**. A register bit with this attribute can be read and written. However, a write of 1 clears (sets to 0) the corresponding bit and a write of 0 has no effect.

Some of the PAC registers described in this section contain reserved bits. Software must deal correctly with fields that are reserved. On reads, software must use appropriate masks to extract the defined bits and not rely on reserved bits being any particular value. On writes, software must ensure that the values of reserved bit positions are preserved. That is, the values of reserved bit positions must first be read, merged with the new values for other bit positions, and then written back. Note the software does not need to perform read, merge, write operations for the configuration address register.

In addition to reserved bits within a register, PAC contains address locations in the configuration space of the Host-PCI Bridge function that are marked “Reserved.” PAC responds to accesses to these address locations by completing the host cycle. Software should not write to reserved configuration locations in the device-specific region (above address offset 3Fh).

During a hard reset, PAC sets its internal configuration registers to predetermined default states. The default state represents the minimum functionality feature set required to successfully bring up the system. Hence, it does not represent the optimal system configuration. It is the responsibility of the system initialization software (usually BIOS) to properly determine the DRAM configurations, operating parameters and optional system features that are applicable, and to program PAC registers accordingly.

NOTE

The 440LX AGPset depends on the atomically of configuration cycles in a 2-way SMP system. Thus, software (BIOS or OS) must guarantee that in a system with two processors only one processor can access the configuration space at any time. During system initialization, only the “Boot Processor” should be allowed access to configuration space. Additionally, PnP BIOS and EISA configuration utilities must guarantee that addresses 0CF8h to 0CFFh are allocated as motherboard addresses and not available as I/O locations.

3.1. Register Access

PAC contains two registers that reside in the CPU I/O address space—the Configuration Address (CONFADD) Register and the Configuration Data (CONFDATA) Register. The Configuration Address Register enables/disables the configuration space and determines what portion of configuration space is visible through the Configuration Data window.

3.1.1. CONFADD—CONFIGURATION ADDRESS REGISTER

I/O Address: 0CF8h Accessed as a DWord
Default Value: 00000000h
Access: Read/Write

CONFADD is a 32-bit register accessed only when referenced as a DWord. A Byte or Word reference will "pass through" the Configuration Address Register onto the PCI bus as an I/O cycle. The CONFADD register contains the Bus Number, Device Number, Function Number, and Register Number for which a subsequent configuration access is intended.

Bit	Descriptions
31	**Configuration Enable (CFGE).** 1=Enable. 0=Disable.
30:24	**Reserved.**
23:16	**Bus Number (BUSNUM).** When BUSNUM is programmed to 00h, the target of the Configuration Cycle is either the PAC or the PCI Bus that is directly connected to the PAC, depending on the Device Number field. If the BUSNUM=00 and PAC is not the target, a type 0 Configuration Cycle is generated on PCI. If BUSNUM≠00 and < SBUSN, a type 1 configuration cycle is generated on PCI with the BUSNUM mapped to AD[23:16] during the address phase. If BUSNUM > SBUSN, a type 1 Configuration Cycle is generated on the A.G.P. Interface with BUSNUM mapped to AD[23:16] during the address phase. If SUBUSN > BUSNUM=SBUSN, a type 0 Configuration Cycle is generated on the A.G.P. Interface. SBUSN and SUBUSN are registers described in *Section 3.4, AGP Configuration Registers*.
15:11	**Device Number (DEVNUM).** This field selects one agent on the PCI bus selected by the Bus Number. During a Type 1 Configuration cycle this field is mapped to AD[15:11]. During a Type 0 PCI Configuration Cycle, this field is decoded and one of AD[31:11] is driven to a 1. During a Type 0 A.G.P. Configuration Cycle, this field is decoded and one of GAD[31:16] is driven to a 1. PAC is always Device Number 0 for the Host Bridge entity and Device Number 1 for the "virtual" PCI-PCI Bridge device, and therefore, its AD11 and AD12 pins are used internally as a corresponding logical IDSELs during PCI configuration cycles. Note that AD11 and AD12 **MUST NOT** be connected to any other PCI bus device as IDSEL signals.
10:8	**Function Number (FUNCNUM).** This field is mapped to AD[10:8] during PCI configuration cycles. This allows the configuration registers of a particular function in a multi-function device to be accessed. PAC responds only to configuration cycles with a function number of 000b; all other function number values attempting access to the PAC (Device Number=0 and 1, Bus Number=0) will generate a master abort.
7:2	**Register Number (REGNUM).** This field selects one register within a particular Bus, Device, and Function as specified by the other fields in the Configuration Address Register. This field is mapped to AD[7:2] during PCI configuration cycles.
1:0	**Reserved.**

3.1.2. CONFDATA—CONFIGURATION DATA REGISTER

I/O Address: 0CFCh
Default Value: 00000000h
Access: Read/Write

CONFDATA is a 32-bit/16-bit/8-bit read/write window into configuration space. The portion of configuration space that is referenced by CONFDATA is determined by the contents of CONFADD.

Bit	Descriptions
31:0	**Configuration Data Window (CDW).** If bit 31 of CONFADD is 1 any I/O reference that falls in the CONFDATA I/O space will be mapped to configuration space using the contents of CONFADD.

3.1.3. CONFIGURATION SPACE MECHANISM

PAC supports two bus interfaces—PCI and A.G.P. The A.G.P. interface is treated as a second PCI interface. Note that A.G.P. address space and A.G.P.'s interface standard PCI-style configuration parameters are controlled via internal "virtual" PCI-to-PCI Bridge entity that is seen by the PCI configuration software as a Device 1 residing on the PCI Bus #0. The following sections describe the configuration space mapping mechanism associated with both interfaces.

3.1.3.1. Routing the Configuration Accesses to PCI or A.G.P.

Routing of configuration accesses to A.G.P. is controlled via the PCI-to-PCI bridge standard mechanism using information contained within : PRIMARY BUS NUMBER, SECONDARY BUS NUMBER and SUBORDINATE BUS NUMBER registers of the A.G.P.'s internal "virtual" PCI-to-PCI Bridge device. Detailed description of the mechanism for translating CPU's I/O bus cycles to configuration cycles on one of the two buses is described below. For the purpose of distinguishing between PCI configuration cycles targeted to PCI and A.G.P. configuration space, a PCI bus 0 is frequently referred to within this document as a Primary PCI.

3.1.3.2. PCI Bus Configuration Mechanism

The PCI Bus defines a slot based "configuration space" that allows each device to contain up to 8 functions with each function containing up to 256 8-bit configuration registers. The PCI specification defines two bus cycles to access the PCI configuration space—**Configuration Read** and **Configuration Write**. While memory and I/O spaces are supported directly by the CPU, configuration space is supported via mapping mechanism implemented within PAC. The PCI specification defines two mechanisms to access configuration space, Mechanism 1 and Mechanism 2. PAC supports only Mechanism 1.

The configuration access mechanism makes use of the CONFADD Register and CONFDATA Register. To reference a configuration register, a DWord I/O write cycle is used to place a value into CONFADD that specifies the PCI bus, the device on that bus, the function within the device, and a specific configuration register of the device function being accessed. CONFADD[31] must be 1 to enable a configuration cycle. CONFDATA then becomes a window into the four bytes of configuration space specified by the contents of CONFADD. Any read or write to CONFDATA will result in the Host Bridge translating CONFADD into a PCI configuration cycle.

Type 0 Access: If CONFADD[BUSNUM]=0, a Type 0 configuration cycle is performed on Primary PCI bus (i.e., bus #0). CONFADD[10:2] are mapped directly to AD[10:2]. The DEVNUM field is decoded onto AD[31:16]. The Host Bridge entity within PAC is accessed as a Device 0 on the Primary PCI bus segment and "virtual" PCI-to-PCI bridge entity is accessed as a Device 1 on the Primary PCI bus. If accessing internal configuration registers within the Host-Bridge entity, PAC asserts AD11 during a configuration cycle and claims the cycle itself. If accessing internal configuration registers within the PCI-to-PCI Bridge entity, PAC

asserts AD12 and then claims the cycle itself. To access PCI Device #2 PAC asserts AD13, for PCI Device #3 PAC asserts AD14, and so forth up to PCI Device #20 for which PAC asserts AD31 for PCI Type 0 Configuration Cycles. Only one AD line is asserted at a time. All device numbers higher than 20 cause a type 0 configuration access with no IDSEL asserted, which results in a master abort. To access A.G.P. Device #0 PAC will assert GAD16, to access A.G.P. Device #1 PAC will assert GAD17, for A.G.P. Device #2 PAC will assert GAD18, and so forth up to Device #15 for which will assert GAD31. Only one GAD line is asserted at a time. All device numbers higher than 15 cause a Type 0 A.G.P. configuration access with no IDSEL asserted, which result in a Master Abort.

Type 1 Access: If the CONFADD[BUSNUM]≠0 but NOT within the range defined as:

SUBORDINATE-BUS-NUMBER ≥ range ≥ SECONDARY-BUS-NUMBER,

then a Type 1 Configuration cycle is performed on the Primary PCI bus (i.e., BUS #0). Note that SECONDARY-BUS-NUMBER and SUBORDINATE-BUS-NUMBER are values contained within the corresponding configuration registers of PAC's "virtual" PCI-to-PCI Bridge entity. CONFADD[23:2] are mapped directly to AD[23:2]. AD[1:0] are driven to 01 to indicate a Type 1 Configuration cycle. All other lines are driven to 0.

3.1.3.3. Mapping of Configuration Cycles on A.G.P.

From the AGPset configuration perspective, A.G.P. is another PCI bus interface residing on a Secondary Bus side of the "virtual" PCI-to-PCI Bridge embedded within PAC. On the Primary Bus side the "virtual" PCI-to-PCI bridge is attached to the BUS #0. Therefore the Secondary side would be denoted as a BUS#1 in the system where configuration software would scan devices on the PCI bus #0 going from the lowest (0) to the highest (20) device number. The "virtual" PCI-to-PCI bridge entity is used to map Type #1 PCI Bus Configuration cycles directed to BUS #0 onto the Type #0 or Type #1 configuration cycles on the A.G.P. interface based on the following rule:

If the CONFADD[BUSNUM]≠0 but within the range defined as:

SUBORDINATE-BUS-NUMBER ≥ range ≥ SECONDARY-BUS-NUMBER

then Type 0 or Type 1 Configuration cycles are performed on A.G.P. If the Bus Number matches a SECONDARY-BUS-NUMBER of the "virtual" PCI-TO-PCI device, then Type 0 configuration cycles are executed on the A.G.P. Otherwise, Type 1 cycles are performed on A.G.P.

To prepare for mapping of the configuration cycles on A.G.P., the initialization software will go through the following sequence:

1. Scan all devices residing at the Primary PCI bus (i.e., bus #0) using Type 0 configuration accesses.
2. For every device residing at bus #0 which implements PCI-to-PCI bridge functionality, it will configure the secondary bus of the bridge with the appropriate number and scan further down the hierarchy. (This process will include the configuration of the "virtual" PCI-TO-PCI Bridge within PAC used to map the A.G.P. address space in a software standard manner.)

3.2. PCI Configuration Space (Device 0 and Device 1)

PAC is implemented as a dual PCI device residing within a single physical component:

- Device 0=Host Bridge (includes PCI bus #0 interface, Main Memory Controller, Graphics Aperture control, PAC's specific A.G.P. control registers).
- Device 1="Virtual" PCI-to-PCI Bridge (includes mapping of A.G.P. space and standard PCI interface control functions of the PCI-to-PCI Bridge).

Table 8 shows the configuration space for Device 0. Shows PAC configuration space for Device #1. Corresponding configuration registers for both devices are mapped as devices residing at the Primary PCI bus (bus #0). The configuration registers layout and functionality for the Device 0 is implemented with a high level of compatibility with a previous generation of PCIsets (i.e., 440FX). Configuration registers of PAC Device 1 are based on the standard configuration space template of a PCI-to-PCI Bridge.

Table 8. PCI Configuration Space—Device 0 (Host-to-PCI Bridge)

Address Offset	Register Symbol	Register Name	Power Down Default Value	Access	Page #
00–01h	VID	Vendor Identification	8086h	RO	35
02–03h	DID	Device Identification	7180h	RO	35
04–05h	PCICMD	PCI Command Register	0006h	R/W	36
06–07h	PCISTS	PCI Status Register	0290h	RO, R/WC	37
08	RID	Revision Identification	00h	RO	38
0Ah	SUBC	Sub-Class Code	00h	RO	38
0Bh	BCC	Base Class Code	06h	RO	38
0Dh	MLT	Master Latency Timer	00h	R/W	39
0Eh	HDR	Header Type	00h	RO	39
10–13h	APBASE	Aperture Base Address	00000008h	R/W	39
34h	CAPPTR	Capabilities Pointer	A0h	RO	40
50–51h	PACCFG	PAC Configuration	0s00_s000_0000_0s00b	R/W	41
53h	DBC	Data Buffering Control	83h	R/W	42
55–56h	DRT	DRAM Row Type	0000h	R/W	43
57h	DRAMC	DRAM Control	01h	R/W	44
58h	DRAMT	DRAM Timing	00h	R/W	44
59–5Fh	PAM[6:0]	Programmable Attribute Map (7 registers)	00h	R/W	46
60–67h	DRB[7:0]	DRAM Row Boundary (8 registers)	01h	R/W	48
68h	FDHC	Fixed DRAM Hole Control	00h	R/W	50
6A-6Bh	DRAMXC	DRAM Extended Mode Select	0000h	R/W	51
6C-6Fh	MBSC	Memory Buffer Strength Control Register	55555555h	R/W	52
70h	MTT	Multi-Transaction Timer	00h	R/W	54
72h	SMRAM	System Management RAM Control	02h	R/W	55
90h	ERRCMD	Error Command Register	00h	R/W	56
91h	ERRSTS0	Error Status Register 0	00h	R/WC	58
92h	ERRSTS1	Error Status Register 1	00h	R/WC	59
93h	RSTCTRL	Reset Control Register	00h	R/W	60
A0–A3h	ACAPID	A.G.P. Capability Identifier	00100002h	RO	61
A4–A7h	AGPSTAT	A.G.P. Status Register	1F000203h	R/W	62

Table 8. PCI Configuration Space—Device 0 (Host-to-PCI Bridge)

Address Offset	Register Symbol	Register Name	Power Down Default Value	Access	Page #
A8–ABh	—	A.G.P. Command Register	00000000h	R/W	62
B0–B3h	AGPCTRL	A.G.P. Control Register	00000000h	R/W	63
B4h	APSIZE	Aperture Size Control Register	0000h	R/W	64
B8–BBh	ATTBASE	Aperture Translation Table Base Register	00000000h	R/W	65
BCh	AMTT	A.G.P. MTT Control Register	00h	R/W	65
BDh	LPTT	A.G.P. Low Priority Transaction Timer Reg.	00h	R/W	65

Table 9. PCI Configuration Space—Device 1 (“Virtual” PCI-to-PCI Bridge)

Address Offset	Register Symbol	Register Name	Power Down Default Value	Access	Page #
00–01h	VID1	Vendor Identification	8086h	RO	66
02–03h	DID1	Device Identification	7181h	RO	66
04–05h	PCICMD1	PCI Command Register	0000h	R/W	66
06–07h	PCISTS1	PCI Status Register	02A0h	RO, R/WC	67
08	RID1	Revision Identification	00h	RO	67
0Ah	SUBC1	Sub-Class Code	04h	RO	67
0Bh	BCC1	Base Class Code	06h	RO	68
0Eh	HDR1	Header Type	01h	RO	68
18h	PBUSN	Primary Bus Number Register	00h	RO	68
19h	SBUSN	Secondary Bus Number	00h	R/W	69
1Ah	SUBUSN	Subordinate Bus Number	00h	R/W	69
1Bh	SMLT	Secondary Bus Master Latency Timer	00h	R/W	69
1Ch	IOBASE	I/O Base Address Register	F0h	R/W	70
1Dh	IOLIMIT	I/O Limit Address Register	00h	R/W	70
1E–1Fh	SSTS	Secondary Status Register	02A0h	R/W	71
20–21h	MBASE	Memory Base Address Register	FFF0h	R/W	72
22–23h	MLIMIT	Memory Limit Address Register	0000h	R/W	72
24–25h	PMBASE	Prefetchable Memory Base Address Reg.	FFF0h	R/W	73
26–27h	PMLIMIT	Prefetchable Memory Limit Address Reg.	0000h	R/W	73
3E–3Fh	BCTRL	Bridge Control Register	0000h	R/W	74

3.3. Register Set—Device 0 (Host-to-PCI Bridge)

3.3.1. VID—VENDOR IDENTIFICATION REGISTER (DEVICE 0)

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only

The VID Register contains the vendor identification number. This 16-bit register combined with the Device Identification Register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number**. This is a 16-bit value assigned to Intel. Intel VID=8086h.

3.3.2. DID—DEVICE IDENTIFICATION REGISTER (DEVICE 0)

Address Offset: 02–03h
Default Value: 7180h
Attribute: Read Only

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number**. This is a 16-bit value assigned to the PAC Host Bridge (i.e., Device 0). DID=7180h.

3.3.3. PCICMD—PCI COMMAND REGISTER (DEVICE 0)

Address Offset: 04–05h
Default: 0006h
Access: Read/Write

This 16-bit register provides basic control over PAC's PCI interface ability to respond to PCI cycles. The PCICMD Register enables and disables the SERR# signal, parity checking (PERR# signal), PAC response to PCI special cycles, and enables and disables PCI bus masters' accesses to main memory.

Bit	Description
15:9	**Reserved**.
8	**SERR# Enable (SERRE)**. 1=PAC's SERR# signal driver is enabled and SERR# is asserted for all relevant bits set in the ERRSTS and PCISTS as controlled by the corresponding bits of the ERRCMD register. 0=SERR# is never driven by PAC. SERR# is asserted under the following conditions: 1. PAC can assert SERR# when it is configured for ECC operation and a single bit (correctable) ECC error, multiple bit (non-correctable) ECC error, or a DRAM parity error occurred. ECC error signaling is enabled via the ERRCMD register (90h, Function 0). 2. PAC asserts SERR# when it detects a target abort during a PAC-initiated PCI cycle. 3. PAC can also assert SERR# when a PCI parity error occurs during the address phase as controlled by bits 8 and 6 of PAC's PCICMD register. 4. PAC can assert SERR# when it samples PERR# asserted on the PCI bus. This capability is controlled by bit 3 of the ERRCMD register. **NOTE** This bit only controls SERR# for the PCI bus (Device 0). Device 1 has its own SERRE bit (PCICMD1 register) to control error reporting for bus conditions occurring on the A.G.P. bus.
7	**Reserved.**
6	**Parity Error Enable (PERRE).** PERRE controls PAC's PCI interface response to the PCI parity errors during the data phase when PAC receives the data (i.e., during reads on the PCI bus and PAC is the initiator and during writes when PAC is a target on the PCI bus). 1=Parity errors are reported on the PERR# signal. Note that when PERRE=1, address parity is reported via SERR# mechanism (if enabled via SERRE bit) and not via PERR# pin. 0=No parity errors are reported by PAC's PCI interface via PERR# or SERR# signals. (Note that other types of error conditions can be still signaled via SERR# mechanism.)
5:0	**Reserved**.

3.3.4. PCISTS—PCI STATUS REGISTER (DEVICE 0)

Address Offset: 06–07h
Default Value: 0290h
Access: Read Only, Read/Write Clear
Size: 16 bits

PCISTS is a 16-bit status register that reports the occurrence of a PCI master abort and PCI target abort on the PCI bus. PCISTS also indicates the DEVSEL# timing that has been set by PAC hardware for target responses on the PCI bus. Bits [15:12] and bit 8 are read/write clear and bits [10:9] are read only.

Bit	Description
15	**Detected Parity Error (DPE)—R/WC**. Software sets DPE to 0 by writing a 1 to this bit. 1 = Indicates PAC's detection of a parity error in either the data or address phase of the Primary PCI bus transactions. Note that the function of this bit is not affected by the PERRE bit.
14	**Signaled System Error (SSE)—R/WC**. Software sets SSE to 0 by writing a 1 to this bit. 1 =When PAC PCI interface logic asserts the SERR# signal, this bit is set to a 1.
13	**Received Master Abort Status (RMAS)—R/WC**. Software resets this bit to 0 by writing a 1 to it. 1 = When PAC terminates a PCI bus transaction (PAC is a PCI master) with an unexpected master abort, this bit is set to a 1. Note that master abort is the normal and expected termination of PCI special cycles.
12	**Received Target Abort Status (RTAS)—R/WC**. Software resets RTAS to 0 by writing a 1 to it. 1 = When a PAC-initiated PCI transaction is terminated with a target abort, RTAS is set to 1. PAC also asserts SERR# if enabled in the ERRCMD register.
11	**Reserved.**
10:9	**DEVSEL# Timing (DEVT)—RO**. This 2-bit field indicates the timing of the DEVSEL# signal when PAC responds as a target on the PCI Bus. 01b=Medium (Hardwired). Indicates the time when a valid DEVSEL# can be sampled by the initiator of the PCI cycle.
8	**Data Parity Detected (DPD)—R/WC.** Software sets DPD to 0 by writing a 1 to this bit. 1 = This bit is set to a 1, when all of the following conditions are met: 1. PAC asserted PERR# or sampled PERR# on the PCI Bus. 2. PAC was the initiator for the operation in which the error occurred on the PCI bus. 3. The PERRE bit in the Primary PCI Command register is set to 1.
7:0	**Reserved**.

3.3.5. RID—REVISION IDENTIFICATION REGISTER (DEVICE 0)

Address Offset: 08h
Default Value: See Stepping Information.
Access: Read Only

This register contains the revision number of PAC Device 0. These bits are read only and writes to this register have no effect.

Bit	Description
7:0	**Revision Identification Number**. This is an 8-bit value that indicates the revision identification number for PAC Device 0. 03h=Hardwired

3.3.6. SUBC—SUB-CLASS CODE REGISTER (DEVICE 0)

Address Offset: 0Ah
Default Value: 00h
Access: Read Only

This register contains the Sub-Class Code definition for PAC.

Bit	Description
7:0	**Sub-Class Code (SUBC).** 00h=Host Bridge.

3.3.7. BCC—BASE CLASS CODE REGISTER (DEVICE 0)

Address Offset: 0Bh
Default Value: 06h
Access: Read Only

This register contains the Base Class Code definition for PAC.

Bit	Description
7:0	**Base Class Code (BASEC).** 06h=Bridge device.

3.3.8. MLT—MASTER LATENCY TIMER REGISTER (DEVICE 0)

Address Offset: 0Dh
Default Value: 00h
Access: Read/Write

MLT is an 8-bit register that controls the amount of time PAC, as a PCI bus master, can burst data on the PCI Bus. The count value is an 8-bit quantity. However, MLT[2:0] are 0 when determining the count value. PAC's MLT is used to guarantee to the PCI agents (other than PAC) a minimum amount of the system resources.

Bit	Description
7:3	**Master Latency Timer Count Value for PCI Bus Access.** The number of clocks programmed in the MLT represents the guaranteed time slice (measured in PCI clocks; 33 MHz for standard PAC configurations) allotted to PAC, after which it must complete the current data transfer phase and surrender the bus as soon as its bus grant is removed. For example, if the MLT is programmed to 18h, the value is 24 PCI clocks. The default value of MLT is 00h and disables this function.
2:0	**Reserved.**

3.3.9. HDR—HEADER TYPE REGISTER (DEVICE 0)

Offset: 0Eh
Default: 00h
Access: Read Only

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Description
7:0	**Header Type.** This read only field always returns 0 when read and writes have no effect.

3.3.10. APBASE—APERTURE BASE CONFIGURATION REGISTER (DEVICE 0)

Offset: 10–13h
Default: 00000008h
Access: Read/Write, Read Only

The APBASE is a standard PCI Base Address register that is used to request the size of the Graphics Aperture. The standard PCI Configuration mechanism defines the base address configuration register in the way that only a fixed amount of space can be requested (dependent on which bits are hardwired to 0 or behave as hardwired to 0). To allow for flexibility, an additional register called APSIZE is used as a "back-end" register to control which bits of the APBASE will behave as hardwired to 0.

Bit	Description
31:28	**Upper Programmable Base Address bits (R/W).** These bits (default=0) locate the range size which is selected by the lower bits (that are either hardwired to 0 or behave as hardwired to 0 depending on the contents of the APSIZE register).
27:22	**Lower "Hardwired"/Programmable Base Address bits.** These bits behave as a hardwired or as a programmable depending on the contents of the APSIZE register as defined below: **27 26 25 24 23 22 Aperture Size** R/W R/W R/W R/W R/W R/W 4 MB R/W R/W R/W R/W R/W 0 8 MB R/W R/W R/W R/W 0 0 16 MB R/W R/W R/W 0 0 0 32 MB R/W R/W 0 0 0 0 64 MB R/W 0 0 0 0 0 128 MB 0 0 0 0 0 0 256 MB Bits [27:22] are controlled by bits [5:0] of the APSIZE register. For example, if bit APSIZE[5]=0, APBASE[27]=0. If APSIZE[5]=1, APBASE[27]=R/W. The same applies, correspondingly, to other bits. The default for APSIZE[5:0] (000000b) forces the APBASE[27:22] default to be 000000b (i.e., all bits respond as hardwired to 0). **NOTE** When programming the APSIZE register such that APBASE register bits change from "read only" to "read/write," the value of those bits is undefined and must be written first to have a known value.
21:0	**Reserved.**

3.3.11. CAPPTR—CAPABILITIES POINTER (DEVICE 0)

Offset: 34h
Default: A0h
Access: Read Only

The CAPPTR provides the offset that is the pointer to the location where A.G.P. standard registers are located.

Bit	Description
7:0	**Pointer to the start of A.G.P. standard register block.** Default Value=A0h

3.3.12. PACCFG—PAC CONFIGURATION REGISTER (DEVICE 0)

Offset: 50–51h
Default: 0s00_s000_0000_0s00b
Access: Read/Write, Read Only

PACCFG is a 16-bit register that is used for indicating the system level configuration

Bit	Description
15	**WSC# Handshake Disable—R/W.** This bit disables the internal WSC# handshake mechanism for the configurations in which an I/O APIC is NOT used as a system interrupt controller. 1=Disable. 0=Enable (default).
14	**Host Frequency—RO.** This bit reflects the value of strap attached to the MECC0 pin. Information stored in this bit is used by the DRAM refresh circuitry to select an optimum refresh count and also by the BIOS to display the system bus frequency. 1=60 MHz. 0=66 MHz.
13:12	**Reserved.**
10	**PCI Agent to Aperture Access Disable—R/W.** This bit is used to prevent access to the aperture from the primary PCI side **(**i.e., PAC's PCI interface does not respond as a target with DEVSEL# if the access is within the aperture). This bit is don't care if bit 9 is 0. 1 = Disable. 0 = Enable. If this bit is 0 (default) and bit 9 of this register is 1, then accesses to the aperture are enabled for the primary PCI side.
9	**Aperture Access Global Enable—R/W.** This bit is used to prevent access to the aperture from any port (CPU, PCI or A.G.P.) before aperture range is established by the configuration software and appropriate translation table in the main DRAM has been initialized. 1=Enable. It must be set after the system is fully configured for aperture accesses. 0=Disable (Default). **NOTE** This bit globally controls accesses to the aperture and that bit 10 provides the next level of control for accesses originated from the primary PCI side.
8:7	**DRAM Data Integrity Mode (DDIM)—R/W**. These bits provide software configurability of selecting between ECC mode, EC-only (error checking only) mode, or non-ECC mode of operation of the DRAM interface in the following manner: **DDIM** — **DRAM Data Integrity Mode** 00 — Non-ECC (Byte-Wise Writes supported) (Default) 01 — EC-only—Checking with No correction 10 — reserved 11 — ECC Generation and Checking/Correction
6	**ECC_TEST Diagnostic Mode Enable (ETPDME)—R/W.** 1=Enable. PAC enters an ECC Diagnostic test mode. 0=Disable (default). Normal mode.

Bit	Description
5	**MDA Present—R/W.** This bit works with the VGA Enable bit in the BCTRL register of device 1 to control the routing of CPU initiated transactions targeting MDA compatible I/O and memory address ranges. When the VGA Enable bit is set to 1, and this bit is reset to 0, references to MDA resources are sent to A.G.P. In all other cases references to MDA resources are sent to PCI. MDA resources are defined as the following: Memory: 0B0000h–0B7FFFh I/O: 3B4h, 3B5h, 3B8h, 3B9h, 3BAh, 3BFh, (including ISA address aliases, A[15:10] are not used in decode) Any I/O reference that includes the I/O locations listed above, or their aliases, will be forwarded to PCI even if the reference includes I/O locations not listed above. The following table shows the behavior for all combinations of the MDA present and VGA forward bits: **VGA** / **MDA** / **Behavior** 0 / 0 / All references to MDA and VGA go to PCI 0 / 1 / Reserved 1 / 0 / All references to VGA go to A.G.P.—MDA-only (I/O 3BFh and aliases) references go to PCI 1 / 1 / VGA references go to A.G.P.; MDA references go to PCI
4:0	**Reserved.**

3.3.13. DBC—DATA BUFFER CONTROL REGISTER (DEVICE 0)

Address Offset: 53h
Default Value: 83h
Access: Read/Write

This 8-bit register allows for PAC buffer control.

Bit	Description
7	**Reserved.**
6	**CPU-to-PCI IDE Posting Enable (CPIE).** 1=Enable. 0=Disable (default). When disabled, the cycles are treated as normal I/O write transactions.
5	**WC Write Post During I/O Bridge Access Enable (WPIO).** 1 = Enable. When enabled, posting of WC transactions to PCI occur, even if the I/O bridge has been granted access to the PCI bus via corresponding arbitration and buffer management protocol (PHLD#/PHLDA#/WSC#). 0 = Disable (default). **NOTE** USWC Write posting should only be enabled if a USWC region is located on the PCI bus.
4:0	**Reserved.**

3.3.14. DRT—DRAM ROW TYPE REGISTER (DEVICE 0)

Address Offset: 55–56h
Default Value: 0000h
Access: Read/Write

This 16-bit register identifies the type of DRAM (SDRAM, EDO) used in each row or if the row is empty, and should be programmed by BIOS for optimum performance. It also identifies if a particular row is left unpopulated and the total number of rows populated in the system. The hardware uses these bits to determine the correct cycle timing to use before a DRAM cycle is run.

Bit	Description
15:0	**DRAM Row Type (DRT).** Each pair of bits in this register corresponds to the DRAM row identified by the corresponding DRB register.

DRT bits	Corresponding DRB register	DRT bits	Corresponding DRB register
DRT[1:0]	DRB0, row 0	DRT[9:8]	DRB4, row 4
DRT[3:2]	DRB1, row 1	DRT[11:10]	DRB5, row 5
DRT[5:4]	DRB2, row 2	DRT[13:12]	DRB6, row 6
DRT[7:6]	DRB3, row 3	DRT[15:14]	DRB7, row 7

The value programmed in each DRT pair of bits uniquely identifies the DRAM timings used for the corresponding row.

DRT pair	DRAM Type
00	EDO
01	Reserved
10	SDRAM
11	Empty Row

3.3.15. DRAMC—DRAM CONTROL REGISTER (DEVICE 0)

Address Offset: 57h
Default Value: 01h
Access: Read/Write

This 8-bit register controls main memory operating modes and features. The timing parameters assume 66-MHz host bus.

Bit	Description
7:6	**Reserved.**
5	**DRAM EDO Auto-Detect Mode Enable (DEDM).** 1=Enable a special timing mode for BIOS to detect EDO DRAM type on a row-by-row basis. 0=Disable (default).
4	**SDRAM Power Management Support Enable (SPME).** SDRAM power management capability is supported as described in the *DRAM Interface* Section (*DRAM Subsystem Power Management* Sub-Section.) 1=Enable. 0=Disable (default).
3	**Reserved.**
2:0	**DRAM Refresh Rate (DRR)**. The DRAM refresh rate is adjusted according to the frequency selected by this field. When the refresh rate is selected as 'normal,' then the refresh rate is based on configuration information stored in PACCFG register bit 14. 000=Refresh Disabled 001=Normal 010–1 1 1=Reserved. **NOTE** 1. Refresh is also disabled via this field, and that disabling refresh results in the eventual loss of DRAM data. 2. Changing the DRR value will reset the refresh request timer.

3.3.16. DRAMT—DRAM TIMING REGISTER (DEVICE 0)

Address Offset: 58h
Default Value: 00h
Access: Read/Write

This 8-bit register controls main memory DRAM timings.

Bit	Description
7	SDRAM **RAS to CAS Delay (SRCD).** This bit defines the delay in assertion of CAS# (SCAS#) from the assertion of RAS# (SRAS#) in 66-MHz clocks. 1=2 clock delay 0=3 clock delay (default)

Bit	Description
6	**SDRAM CAS Latency (SCLT)**. This bit defines the CLT timing parameter of SDRAM expressed in 66-MHz clocks. 1=2 clocks 0=3 clocks (default)
5	**SDRAM RAS Precharge Time (SRPT).** This bit defines the RAS precharge requirements for the SDRAM memory type in 66-MHz clocks. 1=2 clocks 0=3 clocks (default)
4	**EDO DRAM Read Burst Timing (DRBT)**. The DRAM read burst timings are controlled by the DRBT field. Slower rates may be required in certain system designs to support loose layouts or slower memories. Most system designs will be able to use one of the faster burst mode timings. The timing used depends on the type of DRAM on a per-row basis, as indicated by the DRT register. 1=Read Rate is x222 0=Read Rate is x333 (default)
3	**EDO DRAM Write Burst Timing (DWBT)**. The DRAM write burst timings are controlled by the DWBT field. Slower rates may be required in certain system designs to support loose layouts or slower memories. Most system designs will be able to use one of the faster burst mode timings. The timing used depends on the type of DRAM on a per-row basis, as indicated by the DRT register. 1=Write Rate is x222 0=Write Rate is x333 (default)
2	**EDO RAS Precharge Time (RPT).** This bit defines the RAS precharge requirements for the EDO memory type in 66-MHz clocks. 1=3 clocks. 0=4 clocks (default)
1	**EDO RAS to CAS Delay (RCD).** This bit defines the delay in assertion of CAS# (SCAS#) from assertion of RAS# (SRAS#) in 66-MHz clocks. 1=2 clock delay. 0=3 clock delay (default)
0	**MA Wait State (MAWS).** This bit selects FAST or SLOW MA bus timing. Note that SLOW timing is equal to FAST +1, in terms of clock numbers for EDO. For SDRAM, FAST timing means zero MA wait state. This setting will enable PAC to support a Single Clock Command Mode. SLOW means one MA wait state, which forces PAC to support the normal operation (one command per two clocks). 1=FAST 0=SLOW (default)

3.3.17. PAM—PROGRAMMABLE ATTRIBUTE MAP REGISTERS (PAM[6:0]) (DEVICE 0)

Address Offset: 59 (PAM0)–5Fh (PAM6)
Default Value: 00h
Attribute: Read/Write

PAC allows programmable memory attributes on 13 *Legacy* memory segments of various sizes in the 640-KB to 1-MB address range. Seven Programmable Attribute Map (PAM) Registers are used to support these features. Cacheability of these areas is controlled via the MTRR registers in the Pentium II processor. Two bits are used to specify memory attributes for each memory segment. These bits apply to both host accesses and PCI/A.G.P. initiator accesses to the PAM areas. These attributes are:

RE **Read Enable**. When RE=1, the host/A.G.P. read accesses to the corresponding memory segment are claimed by PAC and directed to main memory. Conversely, when RE=0, the read access is directed to PCI.

WE **Write Enable**. When WE=1, the host/A.G.P. write accesses to the corresponding memory segment are claimed by PAC and directed to main memory. Conversely, when WE=0, the write access is directed to PCI.

The RE and WE attributes permit a memory segment to be read only, write only, read/write, or disabled (i.e., if a memory segment has RE=1 and WE=0, the segment is read only). Each PAM Register controls two regions, typically 16 KB. Each of these regions has a 4-bit field. The 4 bits that control each region have the same encoding and are defined in Table 10.

Table 10. Attribute Bit Assignment

Bits [7, 3] Reserved	Bits [6, 2] Reserved	Bits [5, 1] WE	Bits [4, 0] RE	Description
X	X	0	0	**Disabled.** DRAM is disabled and all accesses are directed to PCI. PAC does not respond as a PCI target for any read or write access to this area.
X	X	0	1	**Read Only**. Reads are forwarded to DRAM and writes are forwarded to PCI for termination. This write protects the corresponding memory segment. PAC will respond as a PCI target for read accesses but not for any write accesses.
X	X	1	0	**Write Only**. Writes are forwarded to DRAM and reads are forwarded to the PCI for termination. PAC will respond as a PCI target for write accesses but not for any read accesses.
X	X	1	1	**Read/Write**. This is the normal operating mode of main memory. Both read and write cycles from the host are claimed by PAC and forwarded to DRAM. PAC will respond as a PCI target for both read and write accesses.

As an example, consider a BIOS that is implemented on the expansion bus. During the initialization process, BIOS can be shadowed in main memory to increase the system performance. When a BIOS is copied in main memory, it should be copied to the same address location. To shadow BIOS, the attributes for that address range should be set to write only. BIOS is shadowed by first doing a read of that address. This read is forwarded to the expansion bus. The host then does a write of the same address, which is directed to main memory. After BIOS is shadowed, the attributes for that memory area are set to read only so that all writes are forwarded to the expansion bus.

Table 11 shows the PAM registers and the associated attribute bits:

Table 11. PAM Registers and Associated Memory Segments

PAM Reg.	Attribute Bits				Memory Segment	Comments	Offset
PAM0[3:0]	Reserved						59h
PAM0[7:4]	R	R	WE	RE	0F0000h–0FFFFFh	BIOS Area	59h
PAM1[3:0]	R	R	WE	RE	0C0000h–0C3FFFh	ISA Add-on BIOS[1]	5Ah
PAM1[7:4]	R	R	WE	RE	0C4000h–0C7FFFh	ISA Add-on BIOS[1]	5Ah
PAM2[3:0]	R	R	WE	RE	0C8000h–0CBFFFh	ISA Add-on BIOS[1]	5Bh
PAM2[7:4]	R	R	WE	RE	0CC000h–0CFFFFh	ISA Add-on BIOS[1]	5Bh
PAM3[3:0]	R	R	WE	RE	0D0000h–0D3FFFh	ISA Add-on BIOS	5Ch
PAM3[7:4]	R	R	WE	RE	0D4000h–0D7FFFh	ISA Add-on BIOS	5Ch
PAM4[3:0]	R	R	WE	RE	0D8000h–0DBFFFh	ISA Add-on BIOS	5Dh
PAM4[7:4]	R	R	WE	RE	0DC000h–0DFFFFh	ISA Add-on BIOS	5Dh
PAM5[3:0]	R	R	WE	RE	0E0000h–0E3FFFh	BIOS Extension	5Eh
PAM5[7:4]	R	R	WE	RE	0E4000h–0E7FFFh	BIOS Extension	5Eh
PAM6[3:0]	R	R	WE	RE	0E8000h–0EBFFFh	BIOS Extension	5Fh
PAM6[7:4]	R	R	WE	RE	0EC000h–0EFFFFh	BIOS Extension	5Fh

NOTES:

1. The C0000h to CFFFFh segment can be used for SMM space if enabled by the SMRAM register.

DOS Application Area (00000h–9FFFFh)

The DOS area is 640 KB in size and is further divided into two parts. The 512-KB area at 0 to 7FFFFh is always mapped to the main memory controlled by PAC, while the 128-KB address range from 080000 to 09FFFFh can be mapped to PCI or to main DRAM. By default this range is mapped to main memory and can be declared as a main memory hole (accesses forwarded to PCI) via PAC's FDHC configuration register.

Video Buffer Area (A0000h–BFFFFh)

This 128-KB area is not controlled by attribute bits. The host-initiated cycles in this region are always forwarded to either PCI or A.G.P. bus for termination. Routing of accesses is controlled by AGPCTRL register (Device 1). This area can be programmed as SMM area via the SMRAM register. When used as a SMM space this range can not be accessed from PCI or A.G.P.

Expansion Area (C0000h–DFFFFh)

This 128-KB area is divided into eight 16-KB segments which can be assigned with different attributes via PAM control register. The C0000–DFFFFh segment can be used for SMM space by programming the SMRAM register. If C0000–DFFFFh segment is used for SMRAM, the PAM register values are not used and are treated as don't care. When used as a SMM space, this range can not be accessed from PCI or A.G.P.

Extended System BIOS Area (E0000h–EFFFFh)

This 64-KB area is divided into four 16-KB segments that can be assigned different attributes via the PAM registers.

System BIOS Area (F0000h–FFFFFh)

This area is a single 64-KB segment which can be assigned with different attributes via the PAM registers.

3.3.18. DRB—DRAM ROW BOUNDARY REGISTERS (DEVICE 0)

Address Offset: 60–67h
Default Value: 01h
Access: Read/Write

PAC supports eight physical rows of DRAM. The width of a row is 64 bits. The DRAM Row Boundary Registers define upper and lower addresses for each DRAM row. Contents of these 8-bit registers represent the boundary addresses in 8-MB granularity. For example, a value of 01h indicates 8 MB.

60h DRB0=Total memory in row0 (in 8 MB)
61h DRB1=Total memory in row0 + row1 (in 8 MB)
62h DRB2=Total memory in row0 + row1 + row2 (in 8 MB)
63h DRB3=Total memory in row0 + row1 + row2 + row3 (in 8 MB)
64h DRB4=Total memory in row0 + row1 + row2 + row3 + row4 (in 8 MB)
65h DRB5=Total memory in row0 + row1 + row2 + row3 + row4 + row5 (in 8 MB)
66h DRB6=Total memory in row0 + row1 + row2 + row3 + row4 + row5 + row6 (in 8 MB)
67h DRB7=Total memory in row0 + row1 + row2 + row3 + row4 + row5 + row6 + row7 (in 8 MB)

The DRAM array can be configured with 1M x 64(72), 2M x 64(72), 4M x 64(72), 8M x 64(72) and 16M x64(72) single or double-sided DIMMs. Each register defines an address range that cause a particular RAS# line (or CS# in the SDRAM case) to be asserted (e.g., if the first DRAM row is –8 MB, accesses within the 0- to 8-MB range cause RAS0#/CS0# to be asserted). The DRAM Row Boundary (DRB) registers are programmed with an 8-bit upper address limit value. This limit is compared to bits [30:23] of the requested address, for each row, to determine if DRAM is being targeted.

Bit	Description
7:0	**Row Boundary Address**. This 8-bit value is compared against address lines A[30:23] to determine the upper address limit of a particular row (i.e., DRB minus previous DRB=row size).

Row Boundary Address

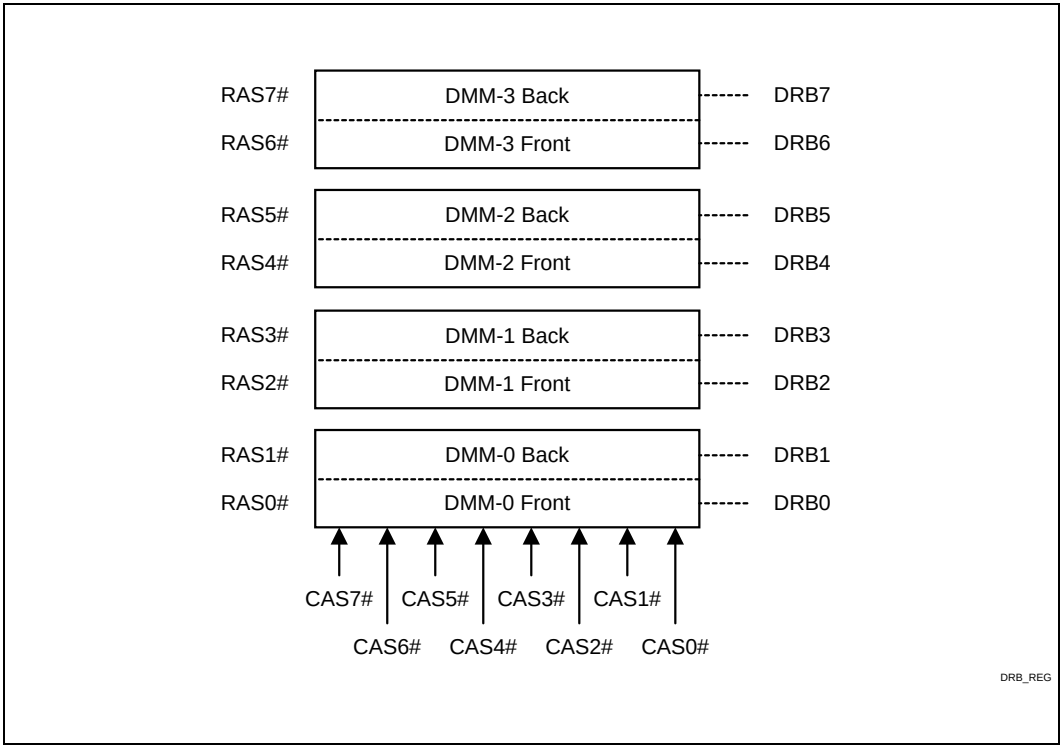


Figure 2. DIMMs and Corresponding DRB Registers

The following 2 examples describe how the DRB Registers are programmed for cases of single-sided and double-sided DIMMs on a motherboard with 4 DIMM sockets.

Example #1 Single-sided DIMMs. Assume a total of 16 MB of DRAM are required using single-sided 1 MB x 64 DIMMs. Since the memory array is 64-bits wide, two DIMMs are required.

DRB0=01h	populated (1 DIMM, 8 MB this row)
DRB1=01h	empty row (empty side of single-sided DIMM)
DRB2=02h	populated (1 DIMM, 8 MB this row)
DRB3=02h	empty row (empty side of single-sided DIMM)
DRB4=02h	empty row (empty socket)
DRB5=02h	empty row (empty socket)
DRB6=02h	empty row (empty socket)
DRB7=02h	empty row (empty socket)

Example #2 Mixed Single-/Double-sided DIMMs. As another example, consider the requirements that a system is initially shipped with 8 MB of memory using one 1M x 64 DRAM DIMM and the rest of the memory array should be upgradable to a maximum supported memory of 200 MB. This can be handled by further populating the array with one 8M x 64 single-sided DIMM (one row) and one 16M x 64 double-sided DIMM (two rows), yielding a total of 200 MB of DRAM. The DRB Registers are programmed as follows:

DRB0=01h	populated with 8 MB (1 MB x 64 single-sided DRAM DIMM)
DRB1=01h	empty row (empty side of single-sided DIMM)
DRB2=09h	populated with 64 MB (8M x 64 single-sided DIMM)
DRB3=09h	empty row (empty side of single-sided DIMM)
DRB4=11h	populated with 64 MB (1/2 16M x 64 double-sided DIMM)
DRB5=19h	populated with 64 MB (1/2 16M x 64 double-sided DIMM)
DRB6=19h	empty row (empty socket)
DRB7=19h	empty row (empty socket)

3.3.19. FDHC—FIXED DRAM HOLE CONTROL REGISTER (DEVICE 0)

Address Offset: 68h
Default Value: 00h
Access: Read/Write

This 8-bit register controls 2 fixed DRAM holes: 512 KB–640 KB and 15 MB–16 MB.

Bit	Description
7:6	**Hole Enable (HEN).** This field enables a memory hole in DRAM space. Host cycles matching an enabled hole are passed on to PCI. PCI cycles matching an enabled hole will be ignored by PAC (no DEVSEL#). Note that a selected hole is not remapped. 00=None 01=512 KB–640 KB (128 KB) 10=15 MB–16 MB (1 MB) 11=Reserved
5:0	**Reserved.**

3.3.20. DRAMXC—DRAM EXTENDED CONTROL REGISTER (DEVICE 0)

Address Offset: 6A–6Bh
Default Value: 0000h
Access: Read/Write

Bit	Description
15:8	**Reserved.**
7:5	**SDRAM MODE SELECT** **Bits[7:5] Operating Mode** 000 Normal Operating Mode (default) 001 NOP Command Enabled (NOPCE). This overrides the output values of SRAS#, SCAS#, and WE# to be 1 1 1 (i.e., a NOP command). When in this mode, the only SDRAM operation that PAC will perform is a NOP command. 010 All Banks Pre-charge Command Enable (ABPCE). This overrides the output values of SRAS#, SCAS#, and WE# to be 0 1 0 (i.e., Pre-charge command). When in this mode the only SDRAM operation that PAC will perform is a Pre-charge command. 011 Mode Register Set Command Enable (MRSCE). This overrides the output values of SRAS#, SCAS#, and WE# to be 0 0 0 (i.e., MRS command). When in this mode the only SDRAM operation that PAC will perform is a MRS command. 100 CBR Cycle Enable (CBRC). This overrides the output values of SRAS#, SCAS#, and WE# to be 0 0 1 (i.e., Refresh command). When in this mode the only SDRAM operation that PAC will perform is a Refresh command. 101–11X Reserved.
4	**Reserved.**
3:2	**Page Timeout Select (PTOS).** Clock Counts are elapsed time waiting for a new Request in the REQW State. 00=16 Clocks (default) 01=Reserved 10=Reserved 11=Reserved
1:0	**Close Both Banks Control (CBBC)** 00=Close Both Banks on Arb Switch PageMiss (default) 01=Reserved 10=Reserved 11=Reserved

3.3.21. MBSC—MEMORY BUFFER STRENGTH CONTROL REGISTER (DEVICE 0)

Address Offset: 6C–6Fh
Default Value: 55555555h
Access: Read/Write

This register programs the various DRAM interface signal buffer strengths, based on memory configuration (Configuration #1 or Configuration #2), DRAM type (EDO or SDRAM), DRAM density (x4, x8, x16, or x32), DRAM technology (16 Mb or 64 Mb), and rows populated.

Bit	Description
31:30	**MAA[1:0] Buffer Strength.** This field sets the buffer strength for MAA[1:0]. 00=48 mA 01=42 mA 10=22 mA 11=Reserved
29:28	**MECC[7:0] Buffer Strength.** This field sets the buffer strength of the MECC pin. 00=42 mA 01=38 mA 10=33 mA 11=Reserved
27:26	**MD[63:0] Buffer Strength.** This field sets the buffer strength of the MD[63:0] pin. 00=42 mA 01=38 mA 10=33 mA 11=Reserved
25:24	**RCSA[0]# & RCSB[0]#/MAB[6] Buffer Strength.** This field sets the buffer strength for RCSA[0]# & RCSB[0]#/MAB[6] pins. 00=48 mA 01=42 mA 10=22 mA 11=Reserved
23:22	**MAB[1:0] Buffer Strength.** This field sets the buffer strength of the MAB[1:0] pin. 00=48 mA 01=42 mA 10=22 mA 11=Reserved
21:20	**MAA[13:2] Buffer Strength.** This field sets the buffer strength of the MAA[13:2] pin. 00=48 mA 01=42 mA 10=22 mA 11=Reserved

Bit	Description
19:18	**RCSA[1]# & RCSB[1]#/MAB[7] Buffer Strength.** This field sets the buffer strength for RCSA[1]# & RCSB[1]#/MAB[7] pins. 00=48 mA 01=42 mA 10=22 mA 11=Reserved
17:16	**RCSA[2]# & RCSB[2]#/MAB[8] Buffer Strength.** This field sets the buffer strength for RCSA[2]# & RCSB[2]#/MAB[8] pins. 00=48 mA 01=42 mA 10=22 mA 11=Reserved
15:14	**RCSA[3]# & RCSB[3]#/MAB[9] Buffer Strength.** This field sets the buffer strength for RCSA[3]# & RCSB[3]#/MAB[9] pins. 00=48 mA 01=42 mA 10=22 mA 11=Reserved
13:12	**RCSA[4]# & RCSB[4]#/MAB[10] Buffer Strength.** This field sets the buffer strength for RCSA[4]# & RCSB[4]#/MAB[10] pins. 00=48 mA 01=42 mA 10=22 mA 11=Reserved
11:10	**CDQB[5,1]# Buffer Strength.** This field sets the buffer strength of the CDQB[5,1]# pins. 00=42 mA 01=38 mA 10=33 mA 11=Reserved
9:8	**CDQA[5,1]# Buffer Strength.** This field sets the buffer strength of the CDQA[5,1]# pins. 00=42 mA 01=38 mA 10=33 mA 11=Reserved
7:6	**CDQA[7:6,4:2,0]# Buffer Strength.** This field sets the buffer strength of the CDQA[7:6,4:2,0]# pins. 00=42 mA 01=38 mA 10=33 mA 11=Reserved

Bit	Description
5:4	**RCSA[5]# & RCSB[5]#/MAB[11] Buffer Strength.** This field sets the buffer strength for RCSA[5]# & RCSB[5]#/MAB[11] pins. 00=48 mA 01=42 mA 10=22 mA 11=Reserved
3:2	**RCSA[6]#/MAB[2] & RCSB[6]#/MAB[12] Buffer Strength.** This field sets the buffer strength for RCSA[6]#/MAB[2] & RCSB[6]#/MAB[12] pins. 00=48 mA 01=42 mA 10=22 mA 11=Reserved
1:0	**RCSA[7]#/MAB[3] & RCSB[7]#/MAB[13] Buffer Strength.** This field sets the buffer strength for RCSA[7]#/MAB[3] & RCSB[7]#/MAB[13] pins. 00=48 mA 01=42 mA 10=22 mA 11=Reserved

NOTES:

WE#[3:0], SRAS#[3]/MAB[5], SCAS#[3]/MAB[4], SRAS#[2:0] and SCAS#[2:0] are no longer programmable. Their strength will be hard-wired to 42 mA (medium strength).

3.3.22. MTT—MULTI-TRANSACTION TIMER REGISTER (DEVICE 0)

Address Offset: 70h
Default Value: 00h
Access: Read/Write

MTT is an 8-bit register that controls the amount of time that PAC's arbiter allows a PCI initiator to perform multiple back-to-back transactions on the PCI bus. PAC's MTT mechanism is used to guarantee the fair share of the PCI bandwidth to an initiator that performs multiple back-to-back transactions to fragmented memory ranges (and as a consequence it can not use long burst transfers).

Bit	Description
7:3	**Multi-Transaction Timer Count Value.** The number of clocks programmed in this field represents the guaranteed time slice (measured in PCI clocks) allotted to the current agent, after which PAC will grant the bus as soon as other PCI initiators request the bus. The default value of MTT is 00h and disables this function. The MTT value can be programmed with 8 clock granularity in the same manner as the MLT register. For example, if the MTT is programmed to 18h, then the selected value corresponds to the time period of 24 PCI clocks.
2:0	**Reserved.**

3.3.23. SMRAM—SYSTEM MANAGEMENT RAM CONTROL REGISTER (DEVICE 0)

Address Offset: 72h
Default Value: 02h
Access: Read/Write

The System Management RAM Control Register controls how accesses to this space are treated. The Open, Close, and Lock SMRAM Space bits function only when the SMRAM enable bit is set to a 1. Also, the OPEN bit should be reset before the LOCK bit is set. Table 12 summarizes the operation of SMRAM space cycles targeting SMI space addresses.

Bit	Description
7	**Reserved.**
6	**SMM Space Open (DOPEN).** 1=When DOPEN=1 and DLCK=0, SMM space DRAM is made visible even when host cycle does not indicate SMM mode access via EXF4#/AB7# signal. This is intended to help BIOS initialize SMM space. Software should ensure that DOPEN=1 is mutually exclusive with DCLS=1. When DLCK is set to 1, DOPEN is set to 0 and becomes read only.
5	**SMM Space Closed (DCLS).** 1=When DCLS=1, SMM space DRAM is not accessible to data references, even if host cycle indicates SMM mode access via EXF4#/AB7# signal. Code references may still access SMM space DRAM. This will allow SMM software to reference “through” SMM space to update the display even when SMM space is mapped over the VGA range. Software should ensure that DOPEN=1 is mutually exclusive with DCLS=1.
4	**SMM Space Locked (DLCK).** 1=When DLCK is set to 1, DOPEN is set to 0 and both DLCK and DOPEN become read only. DLCK can be set to 1 via a normal configuration space write but can only be cleared by a power-on reset. The combination of DLCK and DOPEN provide convenience with security. The BIOS can use the DOPEN function to initialize SMM space and then use DLCK to “lock down” SMM space in the future so that no application software (or BIOS itself) can violate the integrity of SMM space, even if the program has knowledge of the DOPEN function.
3	**SMRAM Enable (SMRAME)**. 1=Enable. When enabled, PAC provides 128 KB of DRAM accessible at the A0000h address or 64 KB of DRAM accessible at the C0000h address during Pentium II processor SMM space accesses (as indicated in the second clock of request phase on EXF4#/Ab7# signal). 0=Disable.
2:0	**SMM Space Base Segment (DBASESEG).** This field programs the location of SMM space. “SMM DRAM” is not remapped. It is simply “made visible” if the conditions are right to access SMM space, otherwise the access is forwarded to PCI. 010=A0000h–BFFFFh. 100=C0000h–CFFFFh. All other values are reserved. PCI initiators are not allowed access to SMM space and PAM bits for C0000h–CFFFFh range are don’t care.

Table 12. SMRAM Space Cycles

SMRAME	DLCK	DCLS	DOPEN	Pentium II Processor SMM Mode Request (0=active)	Code Fetch	Data Reference
0	X	X	X	X	PCI	PCI
1	0	0	0	0	DRAM	DRAM
1	0	X	0	1	PCI	PCI
1	0	0	1	X	DRAM	DRAM
1	0	1	0	0	DRAM	PCI
1	0	1	1	X	INVALID	INVALID
1	1	0	0	0	DRAM	DRAM
1	1	X	0	1	PCI	PCI
1	1	1	0	0	DRAM	PCI

3.3.24. ERRCMD—ERROR COMMAND REGISTER (DEVICE 0)

Address Offset: 90h
Default Value: 00h
Access: Read/Write

This 8-bit register controls PAC responses to various system errors. The actual assertion of SERR# or PERR# is enabled via the PCI Command register.

Bit	Description
7	**SERR# on A.G.P. Non-snoopable access outside of Graphics Aperture.** 1=Enable. When this bit is set to a 1, and bit 2 of the ERRSTS1 register transitions from a 0 to a 1 (during an A.G.P. access to the address outside of the graphics aperture), then an SERR# assertion event will be generated. 0=Disable (default) reporting of this condition.
6	**SERR# on A.G.P. Non-snoopable Access to the Location Outside of Main DRAM Ranges and Aperture Range.** 1=Enable. When bit 6=1 and an A.G.P. agent generates an access using enhanced A.G.P. protocol (i.e., PAC must accept the request without qualification with decode logic since there is no protocol mechanism to reject it) and access is not directed to either main memory range or the aperture range, then bit 1 of the ERRSTS1 register is set and SERR# asserted. 0=Disable (default). When disabled, this condition is not reported via SERR#. PAC ignores A[35:32] of SBA cycles, and therefore will not signal SERR# on accesses over 4G (unless the alias below 4G does not fall within main DRAM or the aperture).

Bit	Description
5	**SERR# on Access to Invalid Graphics Aperture Translation Table Entry.** 1=Enable. When bit 5=1 and access to an invalid entry of the Graphics Aperture Translation Table stored in the main DRAM occurs, then bit 0 of the ERRSTS1 register will be set and SERR# will be asserted. 0=Disable (default). Recommended programming value. **NOTE** The processor may do a speculative read to the aperture area that could hit an invalid entry in the Graphics Aperture Remapping Table Entry. Since the code actually did not want this data, the entry at this location may or may not be valid. If the entry happens to be invalid and the bit that generates SERR# on access to invalid Graphics Aperture Translation Table Entry (ERRCMD Register, Address Offset 90h, Bit 5) is enabled, then PAC will generate SERR#. This spurious generation of SERR# could result in unwanted error messages and/or system hangs. Disabled is the recommended value of this bit.
4	**SERR# on receiving target abort.** 1=Enable. PAC asserts SERR# upon receiving a target abort on either the Primary PCI or A.G.P. 0=Disable. PAC does not assert SERR# upon receipt of a target abort (default).
3	**SERR# on PCI Parity Error.** 1=Enable. PAC asserts SERR# upon sampling PERR# or GPERR# asserted. 0=Disable. PAC does not assert SERR# upon receipt of a parity error via the PERR# or GPERR# pins (default).
2	**Reserved.**
1	**SERR# on Receiving Multiple-Bit ECC/Parity Error.** 1=Enable. PAC asserts SERR# when it detects a multiple-bit error or parity error reported by the DRAM controller. For systems not supporting ECC, this function must be disabled (bit 1=0). 0=Disable.
0	**SERR# on Receiving Single-bit ECC Error.** When this bit is 1=Enable. PAC asserts SERR# when it detects a single-bit ECC error. 0=Disable.

3.3.25. ERRSTS0—ERROR STATUS REGISTER 0 (DEVICE 0)

Address Offset: 91h
Default Value: 00h
Access: Read Only, Read/Write Clear

This 8-bit register is used to report DRAM ECC error conditions. SERR# is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD register). Note that DRAM ECC error conditions can be signaled to the system via ECCERR# pin.

Bit	Description
7:5	**Multi-bit First Error (MBFRE) (RO).** This field contains the encoded value of the DRAM row in which the first multi-bit error occurred. When an error is detected, this field is updated and the MEF bit is set. This field will then be locked (no further updates) until the MEF flag has been reset. If MEF is 0, the value in this field is undefined.
4	**Multiple-bit ECC (uncorrectable) Error Flag (MEF) (R/WC).** 1=Memory data transfer had an uncorrectable error (i.e., multiple-bit error). When enabled by bit 1 in the ERRCMD register, a multiple bit error is reported by the DRAM controller and propagated to the SERR# pin. BIOS has to write a 1 to clear this bit and unlock the MBFRE field. **NOTE** If software writes a 1 to the MEF bit when the MEF bit is 0, and bit 1 of the ERRCMD register is 1 and bit 8 (SERRE) of the PCICMD register is 1, then an error will be reported via the SERR# pin. The MEF bit will remain cleared. Care should be taken by software not to unintentionally do this, since this will typically cause an NMI and result in a system reboot.
3:1	**Single-bit First Row Error (SBFRE) (RO).** This field contains the encoded value of the DRAM row in which the first single-bit error occurred. When an error is detected, this field is updated and SEF is set. This field is then locked (no further updates) until the SEF flag has been reset. If SEF is 0, the value in this field is undefined.
0	**Single-bit (correctable) ECC Error Flag (SEF) (R/WC).** 1=If this bit is set to 1, the memory data transfer had a single-bit correctable error and the corrected data was sent for the access. When ECC is enabled by bit 0 in the ERRCMD register, a single bit error is reported and propagated to the SERR# pin. BIOS has to write a 1 to clear this bit and unlock the SBFRE field.

3.3.26. ERRSTS1—ERROR STATUS REGISTER 1 (DEVICE 0)

Address Offset: 92h
Default Value: 00h
Access: Read Only, Read/Write Clear
Size: 8 bits

This 8-bit register is used to report A.G.P. error conditions. SERR# is generated on a zero to one transition of any of these flags (if enabled by the ERRCMD register).

Bit	Description
7:3	**Reserved**
2	**A.G.P. non-snoopable access outside of Graphics Aperture.** 1=Indicates that an A.G.P. access occurred to the address that is outside of the graphics aperture range. Software has to write 1 to clear this bit.
1	**A.G.P. non-snoopable access to the location outside of main DRAM ranges and aperture range.** Software has to write a 1 to clear this bit. 1=Indicates that an A.G.P. read access is not destined for main DRAM ranges (visible from A.G.P.) or to the aperture. PAC guarantees that the first access outside of DRAM will always receive a SERR# (provided the feature is enabled). SERR# may or may not be asserted for subsequent accesses outside DRAM depending on the delay between the abnormal cycles.
0	**Access to Invalid Graphics Aperture Translation Table Entry(AIGATT)(R/WC).** Software has to write a 1 to clear this bit. 1=Indicates that DRAM access to aperture resulted in an invalid translation table entry.

3.3.27. RSTCTRL—RESET CONTROL REGISTER (DEVICE 0)

Address Offset: 93h
Default Value: 00h
Access: Read/Write

The RSTCTRL Register is used to initiate host soft reset or host Built-in Self Test (BIST) mode hard reset.

NOTE

This register is only used to initiate soft reset or BIST mode hard reset. An I/O access to 0CF9h within PIIX4 I/O bridge should be used to initiate a hard reset.

Bit	Description
7:4	**Reserved.**
3	**BIST Enable (BISTE).** 1=Enable. Enables the host Built-in Self Test to be activated during a subsequent BIST mode hard reset sequence. During BIST mode hard reset, the PAC will assert CPURST# for 1 msec. INIT# will be asserted with CPURST# and negated 4 clocks after CPURST# is negated. 0=Disable **NOTE** BISTE and CSRE should not be 1 simultaneously.
2	**Soft Reset CPU (RCPU).** This bit is used to initiate a reset to the CPU. During soft reset, PAC asserts INIT# for 4 clocks (Figure 3). **BISTE / CSRE / Result** 0 / 0 / Nothing 0 / 1 / Soft Reset 1 / 0 / BIST Mode Hard Reset 1 / 1 / Reserved **NOTE** 1. BISTE and CSRE should not be 1 simultaneously. 2. If the CPU is to be placed into BIST mode hard reset, BISTE must be set to 1 *BEFORE* RCPU is written to. 3. If the CPU is to be placed into soft reset, CSRE must be set to 1 *BEFORE* RCPU is written to. 4. If PAC activates the CPU's BIST function, a hard reset must then be initiated (after BIST completion). The BIST mode sets the IOQ depth of the processor and PAC to 1. This is not a valid operating condition for PAC.
1	**CPU Soft Reset Enable (CSRE).** This bit is used to determine if the CPU will be soft reset when a 1 is written to RCPU. During soft reset, PAC asserts INIT# for 4 clocks. **NOTE** BISTE and CSRE should not be 1 simultaneously.
0	**Reserved.**

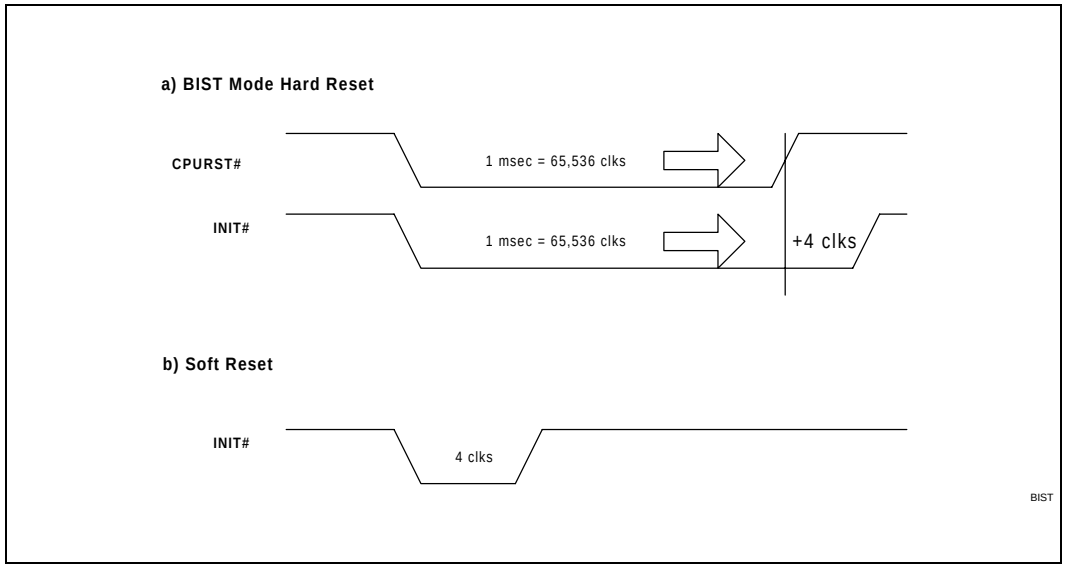


Figure 3. Soft Reset and BIST Hard Reset Timing

3.3.28. ACAPID—A.G.P. CAPABILITY IDENTIFIER REGISTER (DEVICE 0)

Address Offset: A0–A3h
Default Value: 00100002h
Access: Read Only

This register provides a standard identifier for A.G.P. capability.

Bit	Description
31:24	**Reserved.**
23:20	**Major A.G.P. Revision Number.** This field provides a major revision number of the A.G.P. specification to which this version of PAC conforms. This number is hardwired to value of “0001” (i.e., implying Rev 1.x)
19:16	**Minor A.G.P. Revision Number.** This field provides a minor revision number of the A.G.P. specification to which this version of PAC conforms. This number is hardwired to value of “0000” (i.e., implying Rev x.0). Together with major revision number this field identifies PAC as an A.G.P. REV 1.0 compliant device.
15:8	**Next Capability Pointer.** A.G.P. capability is the first and the last capability described with this mechanism, and therefore, these bits are hardwired to 0 to indicate the end of the capability linked list.
7:0	**A.G.P. Capability ID.** This field identifies the linked list item as containing A.G.P. registers. This field has a value of 0010b assigned by the PCI SIG.

3.3.29. AGPSTAT—A.G.P. STATUS REGISTER (DEVICE 0)

Address Offset: A4–A7h
Default Value: 1F000203h
Access: Read/Write, Read Only

This register provides control of the A.G.P. operational parameters and reports A.G.P. device capability/status.

Bit	Description
31:24	**A.G.P. Request Queue Depth—RO.** This field contains the maximum number of A.G.P. command requests PAC is configured to manage. The lower 6 bits of this field reflect the value programmed in A.G.P.CTRL[12:10]. Only discrete values of 32, 16, 8, 4, 2 and 1 can be selected via A.G.P.CTRL. Upper bits are hardwired to 0. Default=1Fh
23:10	**Reserved.**
9	**A.G.P. Side Band Addressing Supported.** Hardwired to 1. 1=Indicates that PAC supports side band addressing.
8:2	**Reserved.**
1:0	**A.G.P. Data Transfer Rates Supported.** Hardwired to 11b. This field indicates the data transfer rates supported by PAC. Note that this field applies to both AD bus and SBA bus. 11=Bit 0=1X, Bit 1=2X. Both 1x and 2x clocking are supported by PAC.

3.3.30. AGPCMD—A.G.P. COMMAND REGISTER (DEVICE 0)

Address Offset: A8–ABh
Default Value: 00000000h
Access: Read/Write

This register reports A.G.P. device capability/status.

Bit	Description
31:10	**Reserved.**
9	**A.G.P. Side Band Enable.** 1=Enable 0=Disable (Default)
8	**A.G.P. Enable.** 1=Enable. When this bit is set to a 0, PAC ignores all A.G.P. operations, including the sync cycle. Any A.G.P. operations received (queued) while this bit is 1, will be serviced even if this bit is subsequently reset to 0. If this bit transitions from a 1 to a 0 on a clock edge in the middle of an SBA command being delivered in 1X mode, the command will be serviced. When this bit is set to a 1, PAC responds to A.G.P. operations delivered via PIPE#. In addition, when this bit is set to a 1, PAC responds to A.G.P. operations delivered via SBA, if the A.G.P. Side Band Enable bit is also set to 1. 0=Disable (Default)
7:2	**Reserved.**

Bit	Description
1:0	**A.G.P. Data Transfer Rate.** One (*and only one*) bit in this field must be set to indicate the desired data transfer rate. <Bit 0: 1X, Bit 1: 2X>. The same bit must be set on both master and target. Default=00b Configuration software will update this field by setting only one bit that corresponds to the capability of the A.G.P. master (after that capability has been verified by accessing the same functional register within the A.G.P. master's configuration space). **NOTE** This field applies to AD and SBA buses.

3.3.31. AGPCTRL—A.G.P. CONTROL REGISTER (DEVICE 0)

Address Offset: B0–B3h
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides additional control of the A.G.P. interface capability.

Bit	Description
31:14	**Reserved.**
13	**Graphics Aperture Write-A.G.P. Read Synchronization Enable (CGAS).** 1=PAC ensures that all writes to the Graphics Aperture, posted in the Global Write Buffer, are retired to DRAM before PAC will initiate any CPU-to-A.G.P. cycle. This can be used to ensure synchronization between the CPU and A.G.P. master. 0=No synchronization is guaranteed (default).
12:10	**Reserved.**
9:8	**Expedite Transaction Throttle Timer.** These bits define the operations of the counter used to internally throttle the expedited transaction stream by masking the internal signal that indicates expedited request operations are pending. 00=no throttling (Default) 01=Reserved 10=192 clocks on—64 clocks off 11=Reserved
7	**GTLB Enable.** 1=Enable. Enables normal operations of the Graphics Translation Lookaside Buffer. 0=Disable (default). GTLB is flushed (i.e., all entry valid bits cleared). This disables fetching and storing of new entries into the GTLB. Also, accesses that require translation bypass the GTLB.
6:0	**Reserved.**

3.3.32. APSIZE—APERTURE SIZE (DEVICE 0)

Address Offset: B4h
Default Value: 0000h
Access: Read/Write

This register determines the effective size of the Graphics Aperture used in the particular PAC configuration. This register can be updated by PAC-specific BIOS configuration sequence before the PCI standard bus enumeration sequence takes place. If the register is not updated the aperture is set to the default size of 256 MB. The size of the table that will correspond to a 256-MB aperture is not practical for most applications. Therefore, these bits must be programmed to a smaller, more practical value. This forces an adequate address range to be requested from the PCI configuration software via ABASE register.

Bit	Description
7:6	**Reserved.**
5:0	**Graphics Aperture Size.** When a particular bit of this field is 0, it forces the corresponding bit of the bit field ABASE[27:22] to behave as “hardwired” to 0. When a bit is 1, it allows the corresponding bit of the ABASE[27:22] to be read/write accessible. Only the following combinations are allowed: **Bits[5:0] — Aperture Size** 11 1111b — 4 MB 11 1110b — 8 MB 11 1100b — 16 MB 11 1000b — 32 MB 11 0000b — 64 MB 10 0000b — 128 MB 00 0000b — 256 MB The default for APSIZE[5:0]=000000b forces default APBASE[27:22]=000000b (maximum aperture size of 256 MB). **NOTE** When programming the APSIZE register such that APBASE register bits change from “read only” to “read/write,” the value of those bits is undefined and must be written first to have a known value.

3.3.33. ATTBASE—APERTURE TRANSLATION TABLE BASE REGISTER (DEVICE 0)

Address Offset: B8–BBh
Default Value: 00000000h
Access: Read/Write
Size: 32 bits

This register provides the start address of the Graphics Aperture Translation Table, which is located in main system memory. This value is used by PAC's Graphics Aperture Address Translation logic (including the GTLB logic) to obtain the appropriate address translation entry. This is required during the translation of the aperture address into a corresponding physical DRAM address. Note that address provided via ATTBASE is 4-KB aligned.

Bit	Description
31:12	**Translation Table Base Address.** This field contains a pointer to the base of the translation table. This table is used to map memory space addresses in the aperture range to addresses in main memory.
11:0	**Reserved.**

3.3.34. AMTT—A.G.P. INTERFACE MULTI-TRANSACTION TIMER REGISTER (DEVICE 0)

Address Offset: BCh
Default Value: 00h
Access: Read/Write

AMTT is an 8-bit register that controls the amount of time that PAC's arbiter allows an A.G.P. master, using PCI protocol, to perform multiple back-to-back transactions on the A.G.P. interface. The AMTT mechanism applies to CPU-to-A.G.P. transactions as well, and it guarantees the CPU a fair share of the A.G.P. interface bandwidth.

Bit	Description
7:3	**Multi-Transaction Timer Count Value.**
2:0	**Reserved.**

3.3.35. LPTT—LOW PRIORITY TRANSACTION TIMER REGISTER (DEVICE 0)

Address Offset: BDh
Default Value: 00h
Access: Read/Write

LPTT is an 8-bit register similar in a function to AMTT. This register is used to control the minimum tenure on the A.G.P. for low priority data transaction (both reads and writes) issued using PIPE# or SB mechanisms.

Bit	Description
7:3	**Low Priority Transaction Timer Count Value.**
2:0	**Reserved.**

3.4. A.G.P. Configuration Registers—(Device 1)

3.4.1. VID1—VENDOR IDENTIFICATION REGISTER (DEVICE 1)

Address Offset: 00–01h
Default Value: 8086h
Attribute: Read Only

The VID1 register contains the vendor identification number for function 1. This 16-bit register combined with the Device Identification Register uniquely identify any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Vendor Identification Number**. This is a 16-bit value assigned to Intel. Intel VID=8086h.

3.4.2. DID1—DEVICE IDENTIFICATION REGISTER (DEVICE 1)

Address Offset: 02–03h
Default Value: 7181h
Attribute: Read Only

This 16-bit register combined with the Vendor Identification register uniquely identifies any PCI device. Writes to this register have no effect.

Bit	Description
15:0	**Device Identification Number**. This is a 16-bit value assigned to PAC Device 1. PAC Device 1 DID=7181h.

3.4.3. PCICMD1—PCI-PCI COMMAND REGISTER (DEVICE 1)

Address Offset: 04–05h
Default: 0000h
Access: Read/Write

This 16-bit register provides basic control over the “virtual” PCI-to-PCI bridge entity embedded within PAC. In this way, PAC’s A.G.P. interface is handled by the standard control mechanism of the PCI-to-PCI bridge, where A.G.P. corresponds to the Secondary Bus of the bridge.

Bit	Description
15:9	**Reserved**.
8	**SERR# Enable (SERRE1)**. 1=Enable. PAC’s common SERR# signal driver (common for Primary PCI and A.G.P.) is enabled for the error conditions that occurred on the A.G.P. (including GSERR# assertion and parity errors), and SERR# is asserted for all relevant bits set in the PCISTS1. If both SERRE and SERRE1 are reset to 0, then SERR# is never driven by PAC. Also, if this bit is set and the Parity Error Response Enable Bit (Register 3Eh, Device #1, Bit 0) is set, then PAC will report ADDRESS parity errors on A.G.P. (when it is potential target). 0=Disable.
7:0	**Reserved.**

3.4.4. PCISTS1—PCI-PCI STATUS REGISTER (DEVICE 1)

Address Offset: 06–07h
Default Value: 02A0h
Access: Read Only, Read/Write Clear

PCISTS1 is a 16-bit status register that reports the occurrence of error conditions associated with the primary side of the “virtual” PCI-to-PCI bridge in PAC.

Bit	Description
15	**Reserved.**
14	**Signaled System Error (SSE1)—R/WC**. 1=When PAC asserts the SERR# signal due to error condition on the A.G.P. side (i.e., GSERR# activated), this bit is also set to 1. Software sets SSE1 to 0 by writing a 1 to this bit.
13:0	**Reserved.**

3.4.5. RID1—REVISION IDENTIFICATION REGISTER (DEVICE 1)

Address Offset: 08h
Default Value: 03h
Access: Read Only

This register contains the revision number of PAC Device 1. These bits are read only and writes to this register have no effect. This value is hardwired to 03h.

Bit	Description
7:0	**Revision Identification Number**. This is an 8-bit value that indicates the revision identification number for PAC Device 1.

3.4.6. SUBC1—SUB-CLASS CODE REGISTER (DEVICE 1)

Address Offset: 0Ah
Default Value: 04h
Access: Read Only

This register contains the device programming interface information related to the Sub-Class Code definition for PAC device 1.

Bit	Description
7:0	**Sub-Class Code (SUBC1).** This is an 8-bit value that indicates the category of bridge for PAC device #1. 04h=Indicate a PCI-to-PCI Bridge.

3.4.7. BCC1—BASE CLASS CODE REGISTER (DEVICE 1)

Address Offset: 0Bh
Default Value: 06h
Access: Read Only

This register contains the device programming interface information related to the Base Class Code definition for PAC device 1.

Bit	Description
7:0	**Base Class Code (BASEC).** This is an 8-bit value that indicates the Base Class Code for PAC device #1. 06h=Indicates a bridge device.

3.4.8. HDR1—HEADER TYPE REGISTER (DEVICE 1)

Offset: 0Eh
Default: 01h
Access: Read Only

This register identifies the header layout of the configuration space. No physical register exists at this location.

Bit	Description
7:0	**Header Type (HEADT).** This read only field always returns 01h when read. Writes have no effect.

3.4.9. PBUSN—PRIMARY BUS NUMBER REGISTER—DEVICE #1

Offset: 18h
Default: 00h
Access: Read Only
Size: 8 bits

This register identifies that the “virtual” PCI-PCI bridge is connected to bus #0.

Bit	Description
7:0	**Bus Number.** The value of this 8-bit register is always 00h.

3.4.10. SBUSN—SECONDARY BUS NUMBER REGISTER (DEVICE 1)

Offset: 19h
Default: 00h
Access: Read/Write

This register identifies the bus number assigned to the second bus side of the virtual PCI-PCI bridge (i.e., to the A.G.P).

Bit	Description
7:0	**Bus Number.** This field is programmed by the PCI configuration software to allow mapping of configuration cycles to A.G.P. Default=00h.

3.4.11. SUBUSN—SUBORDINATE BUS NUMBER REGISTER (DEVICE 1)

Offset: 1Ah
Default: 00h
Access: Read/Write

This register identifies the subordinate bus, if any, that resides at the level below A.G.P.

Bit	Description
7:0	**Bus Number.** This field is programmed by the PCI configuration software to allow mapping of configuration cycles to A.G.P. Default=00h.

3.4.12. SMLT—SECONDARY MASTER LATENCY TIMER REGISTER (DEVICE 1)

Address Offset: 1Bh
Default Value: 00h
Access: Read/Write

This register controls the bus tenure of PAC on the A.G.P. interface in the same way that the MLT controls access to the primary PCI bus.

Bit	Description
7:3	**Secondary MLT Counter Value.** Default=00000b (i.e., SMLT disabled)
2:0	**Reserved.**

3.4.13. IOBASE—I/O BASE ADDRESS REGISTER (DEVICE 1)

Address Offset: 1Ch
Default Value: F0h
Access: Read/Write

This register controls the CPU to A.G.P. I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are treated as 0. Thus the bottom of the defined I/O address range will be aligned to a 4-KB boundary.

Bit	Description
7:4	**I/O Address Base.** Corresponds to A[15:12] of the I/O address. Default=1111b
3:0	**Reserved.**

3.4.14. IOLIMIT—I/O LIMIT ADDRESS REGISTER (DEVICE 1)

Address Offset: 1Dh
Default Value: 00h
Access: Read/Write

This register controls the CPU to A.G.P. I/O access routing based on the following formula:

IO_BASE ≤ address ≤ IO_LIMIT

Only the upper 4 bits are programmable. For the purpose of address decode, address bits A[11:0] are assumed to be FFFh. Thus, the top of the defined I/O address range will be at the top of a 4-KB aligned address block.

Bit	Description
7:4	**I/O Address Limit.** Corresponds to A[15:12] of the I/O address. Default=0000b
3:0	**Reserved.**

3.4.15. SSTS—SECONDARY PCI-PCI STATUS REGISTER (DEVICE 1)

Address Offset: 1E–1Fh
Default Value: 02A0h
Access: Read Only, Read/Write Clear

SSTS is a 16-bit status register that reports the occurrence of error conditions associated with the secondary side (i.e., A.G.P. side) of the "virtual" PCI-to-PCI bridge in PAC.

Bit	Description
15	**Detected Parity Error (DPE1)—R/WC**. 1=Indicates PAC's detection of a parity error in either the data or address phase. Software resets this bit to 0 by writing a 1 to it. Note that the function of this bit is not affected by the PERRE1 bit.
14	**Received System Error (SSE1)—R/WC**. 1=PAC detects GSERR# assertion on A.G.P. Software resets this bit to 0 by writing a 1 to it.
13	**Received Master Abort Status (RMAS1)—R/WC**. 1=PAC terminated a Host-to-A.G.P. with an unexpected master abort. Software resets this bit to 0 by writing a 1 to it.
12	**Received Target Abort Status (RTAS1)—R/WC**. 1=PAC-initiated transaction on A.G.P. is terminated with a target abort. Software resets RTAS1 to 0 by writing a 1 to it.
11:9	**Reserved.**
8	**Data Parity Detected (DPD1)—R/WC.** This bit is set to a 1, when all of the following conditions are met. Software resets this bit to 0 by writing a 1 to it. 1. PAC asserted GPERR# or sampled GPERR# asserted. 2. PAC was the initiator for the operation in which the error occurred. 3. The SPERRE bit in the BCTRL register is set to 1.
7:0	**Reserved**.

3.4.16. MBASE—MEMORY BASE ADDRESS REGISTER (DEVICE 1)

Address Offset: 20–21h
Default Value: FFF0h
Access: Read/Write

This register controls the CPU to A.G.P. non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

This register must be initialized by the configuration software. For address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Description
15:4	**Memory Address Base.** Corresponds to A[31:20] of the 32-bit memory address. Default=FFFh
3:0	**Reserved.** Read as 0s.

3.4.17. MLIMIT—MEMORY LIMIT ADDRESS REGISTER (DEVICE 1)

Address Offset: 22–23h
Default Value: 0000h
Access: Read/Write

This register controls the CPU to A.G.P. non-prefetchable memory access routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

This register must be initialized by the configuration software. For address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Bit	Description
15:4	**Memory Address Limit.** Corresponds to A[31:20] of the 32-bit memory address. Default=000h
3:0	**Reserved.** Read as 0s.

3.4.18. PMBASE—PREFETCHABLE MEMORY BASE ADDRESS REGISTER (DEVICE 1)

Address Offset: 24–25h
Default Value: FFF0h
Access: Read/Write

This register controls the CPU to A.G.P. prefetchable memory accesses routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

This register must be initialized by the configuration software. For address decode, address bits A[19:0] are assumed to be 0. Thus, the bottom of the defined memory address range will be aligned to a 1-MB boundary.

Bit	Description
15:4	**Memory Address Base.** Bits [15:4] corresponds to A[31:20] of the 32-bit memory address. Default=FFFh
3:0	**Reserved.** Read as 0s.

3.4.19. PMLIMIT—PREFETCHABLE MEMORY LIMIT ADDRESS REGISTER (DEVICE 1)

Address Offset: 26–27h
Default Value: 0000h
Access: Read/Write

This register controls the CPU to A.G.P. prefetchable memory accesses routing based on the following formula:

MEMORY_BASE ≤ address ≤ MEMORY_LIMIT

This register must be initialized by the configuration software. For address decode, address bits A[19:0] are assumed to be FFFFFh. Thus, the top of the defined memory address range will be at the top of a 1-MB aligned memory block.

Bit	Description
15:4	**Memory Address Limit.** Corresponds to A[31:20] of the 32-bit memory address. Default=000h
3:0	**Reserved.** Read as 0s.

3.4.20. BCTRL—PCI-PCI BRIDGE CONTROL REGISTER (DEVICE 1)

Address Offset: 3E–3Fh
Default: 0000h
Access: Read/Write

This register provides extensions to the PCICMD1 register that are specific to PCI-to-PCI bridges. The BCTRL provides additional control for the secondary interface (i.e., A.G.P.). It also provides bits that affect the overall behavior of the "virtual" PCI-to-PCI bridge embedded within PAC (e.g., VGA compatible address ranges mapping).

Bit	Description
15:11	**Reserved**.
10	**Discard Timer Status.** 1=Indicates that a delayed transaction has been discarded. When set, this bit can be cleared by writing a 1 to it.
9	**Secondary Discard Timer Enable.** 1=Enable. Enables the Discard Timer for delayed transactions on the A.G.P. (initiated by the A.G.P. agent using FRAME# protocol). The counter starts once the delayed transaction request is ready to complete **(**i.e., read data is pending on the top of the A.G.P. outbound queue). If the A.G.P. agent does not repeat the transaction before the counter expires after 1024 clocks (66 MHz), PAC will delete the delayed transaction from its queue and set the Discard Timer Status bit. 0=Disable.
8:4	**Reserved.**
3	**VGA Enable.** Controls the routing of CPU-initiated transactions targeting VGA compatible I/O and memory address ranges. 1=Enable. When enabled, PAC forwards the following CPU accesses to the A.G.P.: • Memory accesses in the range 0A0000h to 0BFFFFh • I/O addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases—A[15:10] are not decoded) When enabled, forwarding of these CPU issued accesses is independent of the I/O address and memory address ranges defined by the base and limit registers. Forwarding of these accesses is also independent of the settings of bit 2 (ISA Enable) of this register if this bit is a 1. 0=Disable (default). VGA compatible memory and I/O range accesses are not forwarded to A.G.P. unless they are mapped to A.G.P. via I/O and memory range registers defined above (IOBASE, IOLIMIT, MBASE, MLIMIT, PMBASE, PMLIMIT), they are mapped to primary PCI.
2	**ISA Enable.** Modifies the response by PAC to an I/O access issued by the CPU that targets ISA I/O addresses. This applies only to I/O addresses that are enabled by the IOBASE and IOLIMIT registers. 1=Enable. PAC blocks the forwarding of I/O transactions addressing the last 768 bytes in each 1-KB block to A.G.P. This occurs even if the addresses are within the range defined by the IOBASE and IOLIMIT. Instead of going to A.G.P., these cycles are forwarded to primary PCI where they are claimed by the ISA bridge. 0=Disable (default). All addresses defined by the IOBASE and IOLIMIT for the CPU I/O transactions will be mapped on A.G.P.

Bit	Description
1	**System Error Enable.** This bit controls forwarding of the GSERR# from the A.G.P. side to SERR# on the primary PCI. 1=Enable. SERRE1 bit of PCICMD1 is set, and the bridge detects the assertion of GSERR# on the A.G.P. interface. PAC then asserts SERR# on the primary PCI. 0=Disable (default). Forwarding of GSERR# to the primary SERR# is disabled.
0	**Parity Error Response Enable.** This bit controls PAC's response to parity errors on the A.G.P. interface. PAC generates parity on A.G.P. even if error reporting is disabled. 1=Enable. Enables parity error reporting on the A.G.P. interface via GPERR# and detection. 0=Disable (default). PAC ignores address and data parity errors on the A.G.P. interface. In addition, this bit enables the reporting of address parity errors via SERR#, provided that the SERRE1 bit of the PCICMD1 register (Register 04–05h, Device #1, bit 8) is set.

4.0. FUNCTIONAL DESCRIPTION

4.1. System Address Map

A Pentium II processor based system with the 440LX AGPset supports 4 GB of addressable memory space and 64 KB of addressable I/O space. The lower 1 MB of the addressable memory is divided into regions that can be individually controlled with programmable attributes such as disable, read/write, write only, or read only (see Register Description section for details). This section describes memory space partitioning and function. The I/O address space mapping is explained at the end of this section.

In this section, it is assumed that all of the compatibility memory ranges reside on the PCI bus, except VGA ranges that can be potentially mapped on A.G.P. Thus, the phrase “forwarded to PCI” refers to the PCI bus, unless the A.G.P. bus is specifically named.

NOTE

The Pentium II processor supports addressing of memory ranges larger than 4 GB. PAC claims any access over 4 GB and terminates the transaction (without forwarding it to the PCI bus). Host writes are terminated by completing the host cycle and discarding the data. Host reads are terminated by returning all zeros on the host bus. Note that PCI Dual Address Cycle Mechanism (DAC) that allows addressing of >4-GB range is not supported by PAC (either on PCI or on the A.G.P. interface).

4.1.1. MEMORY ADDRESS RANGES

The memory address map (Figure 4) represents the maximum 64 GB of CPU address space. PAC supports 4 GB of main memory. Accesses to memory space below 4 GB and above top of DRAM, to the compatibility video buffer range, to the programmable holes and to the memory window (if enabled) are forwarded to the PCI. Note that if the memory holes are enabled below the top of main memory area, then the corresponding DRAM ranges are not remapped.

4.1.1.1. Compatibility Area

This area is divided into the following address regions:

- 0–512-KB DOS Area
- 512-KB–640-KB DOS Area—Optional ISA/PCI Memory
- 640-KB–768-KB Video Buffer Area
- 768-KB–896-KB in 16-KB sections (total of 8 sections)—Expansion Area
- 896-KB–960-KB in 16-KB sections (total of 4 sections)—Extended System BIOS Area
- 960-KB–1-MB Memory (BIOS Area)—System BIOS Area

There are thirteen ranges which can be enabled or disabled independently for both read and write cycles and one (512 KB–640 KB) which can be mapped to either main DRAM or PCI.

DOS Area (00000h–9FFFh)

The DOS area is 640 KB and is divided into two parts. The 512-KB area (0h–7FFFFh) is always mapped to the main memory controlled by PAC. The 128-KB area (080000h–09FFFFh) can be mapped to PCI or to main memory. By default, this range is mapped to main memory and can be declared as a main memory hole (accesses forwarded to PCI) via the FDHC register.

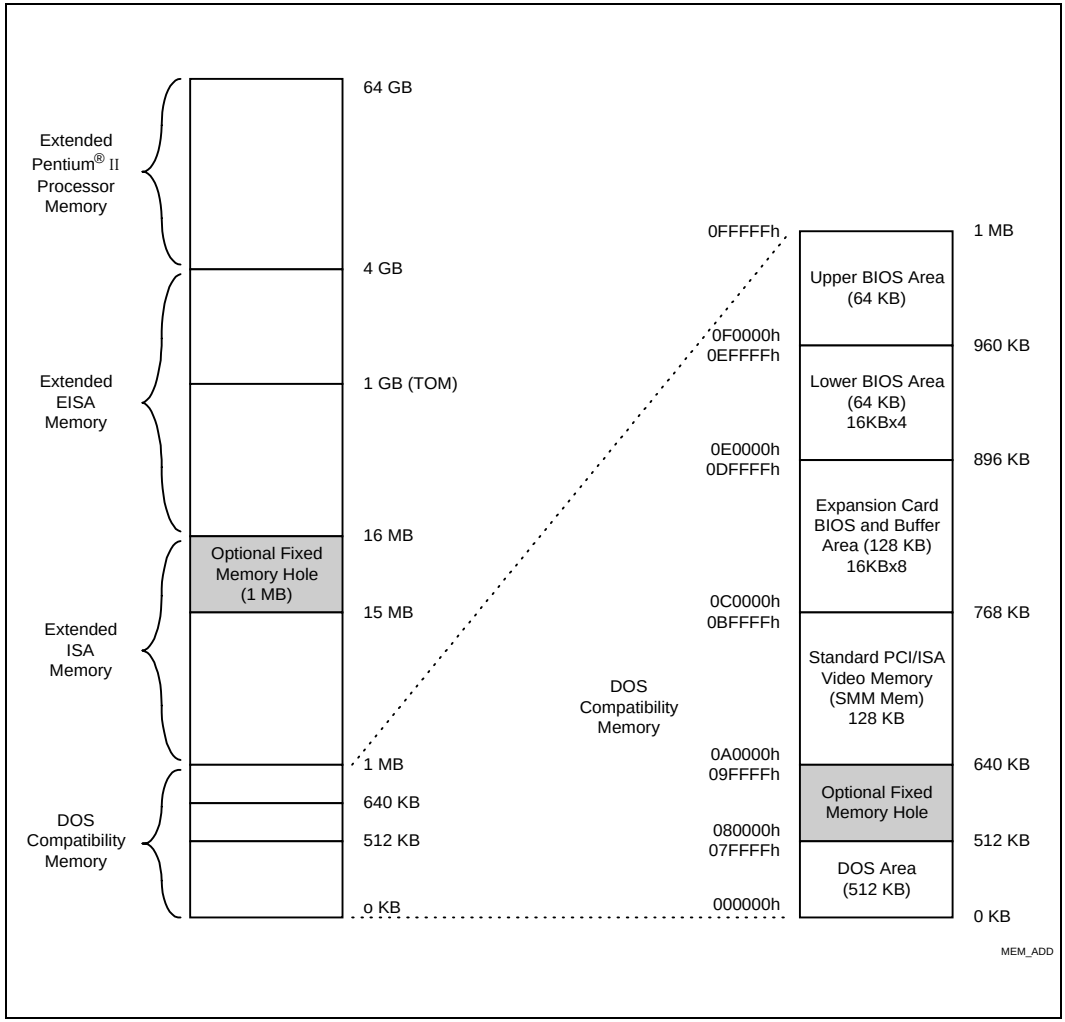


Figure 4. Detailed Memory System Address Map

Video Buffer Area (A0000h–BFFFFh)

The 128-KB graphics adapter memory region is normally mapped to a legacy video device on the PCI bus (typically VGA controller). This area is not controlled by attribute bits and CPU-initiated cycles in this region are forwarded to the PCI bus or A.G.P. for termination. This region is also the default region for SMM space.

The BCTRL (PCI-PCI Bridge Control Register) configuration registers of “virtual” PCI-to-PCI Bridge controls whether these accesses will be forwarded to PCI or to A.G.P. This applies to accesses initiated from any of the system interfaces (i.e., CPU bus, PCI or A.G.P.). Note that for A.G.P.<->PCI accesses, only write operations from PCI to A.G.P. are supported (i.e., A.G.P. -> PCI writes are not supported; PCI<->AGP reads are not supported). For more details see the PCI-to-PCI Bridge Control register description.

Expansion Area (C0000h–DFFFFh)

This 128-KB ISA Expansion region is divided into eight 16-KB segments. Each segment can be assigned one of four Read/Write states: read-only, write-only, read/write, or disabled. Typically, these blocks are mapped through the Primary PCI bridge to ISA space. Memory that is disabled is not remapped. C0000h–CFFFFh is also an optional SMM space.

Extended System BIOS Area (E0000h–EFFFFh)

This 64-KB area is divided into four 16-KB segments. Each segment can be assigned independent read and write attributes so it can be mapped either to main memory or to PCI. Typically, this area is used for RAM or ROM. Memory segments that are disabled are not remapped elsewhere.

System BIOS Area (F0000h–FFFFFh)

This area is a single 64-KB segment and can be assigned read and write attributes. The default is read/write disabled and cycles are forwarded to PCI. By manipulating the read/write attributes, PAC can “shadow” BIOS into the main memory. When disabled, this segment is not remapped.

Extended Memory Area

This memory area is from 1 MB to 4 GB - 1 (100000h to FFFFFFFFh) and is divided into the following regions:

- Main memory from 1 MB to the Top of Memory (maximum of 256 MB using 16-Mbit DRAM technology or 1 GB using 64-Mbit technology)
- PCI Memory space from the Top of Memory to 4 GB with two specific ranges:
  - — APIC Configuration Space from FEC0_0000h (4 GB minus 20 MB) to FECF_FFFFh and FEE0_0000h to FEEF_FFFFh.
  - — High BIOS area from 4 GB to 4 GB minus 2 MB

Main DRAM Address Range (0010_0000h to Top of Main Memory)

The address range from 1 MB to the top of main memory is mapped to main memory address range controlled by PAC. All accesses to addresses within this range are forwarded to main memory, unless a hole in this range is created via the FDHC register. Accesses within this hole are forwarded to PCI. The range of physical memory disabled by opening the hole is not remapped to the Top of the Memory.

PCI Memory Address Range (Top of Main Memory to 4 GB)

The address range from the top of main memory to 4 GB (top of physical memory space supported by PAC) is normally mapped to PCI. However, the A.G.P. memory window is mapped to the A.G.P. and Graphics Aperture range which is mapped to main memory.

NOTE

The A.G.P. Memory Window and Graphics Aperture Window override the default decode to PCI of the memory space above the top of the main DRAM.

There are two sub-ranges within this address range defined as APIC Configuration Space and High BIOS Address Range. The A.G.P. Memory Window and Graphics Aperture Window **MUST NOT** overlap with these two ranges. These ranges are described in detail in the following paragraphs.

APIC Configuration Space (FEC0_0000h – FECF_FFFFh, FEE0_0000h – FEEF_FFFFh)

This range is reserved for APIC configuration space which includes the default I/O APIC configuration space. The default Local APIC configuration space is FEE0_0000h to FEEF_0FFFh.

CPU accesses to the Local APIC configuration space do not result in external bus activity since the Local APIC configuration space is internal to the CPU. However, the MTRR's must be programmed to make the Local and I/O APIC range uncacheable (UC). In PAC partitioning, I/O APIC functionality is supported via a stand-alone component residing on the X-bus provided by the PIIX4 I/O bridge.

I/O APIC units are be located beginning at the default address FEC0_0000h. The first I/O APIC will be located at FEC0_0000h. Each I/O APIC unit is located at FEC0_x000h where *x* is I/O APIC unit number 0 through F(hex). This address range is normally mapped to PCI.

The address range between the APIC configuration space and the High BIOS (FEC0_FFFFh to FFE0_0000h) is always mapped to the PCI.

High BIOS Area (FFE0_0000h to FFFF_FFFFh)

The top 2 MB of the Extended Memory Region is reserved for System BIOS (High BIOS), extended BIOS for PCI devices, and the A20 alias of the system BIOS. CPU begins execution from the High BIOS after reset. This region is mapped to the PCI so that the upper subset of this region is alias to the 16-MB minus 256-KB range.

4.1.1.2. A.G.P. Memory Address Ranges

PAC can be programmed to direct memory accesses to the A.G.P. bus interface when addresses are within the appropriate range. This range is divided into two subranges. The first is controlled via the A.G.P. Memory Base Register (AMBASE) and A.G.P. Memory Limit Register (AMLIMIT). The second range is controlled by the A.G.P. Prefetchable Memory Base Register (APMBASE) and A.G.P. Prefetchable Memory Limit Register (APMLIMIT). Decode for these ranges is based on the following concept:

The top 12 bits of the Memory Base and Memory Limit registers correspond to address bits A[31:20] of a memory address. For the purpose of address decoding, PAC assumes that address bits A[19:0] of the memory base are zero and that address bits A[19:0] of the memory limit address are FFFFFh. This forces the memory address range to be aligned to 1-MB boundaries and to have a size granularity of 1 MB. The address ranges covered by these registers are defined by the following equation:

$$Base\_Address \leq Address \leq Limit\_Address$$

The effective size of the range is programmed by the plug-and-play configuration software and depends on the size of memory claimed by the A.G.P. device. Normally these ranges reside above the Top-of-Main Memory and below High BIOS and APIC address ranges. It is essential to support separate Prefetchable ranges to apply WC attributes (from the processor point of view) to that range.

4.1.1.3. A.G.P. Graphics Aperture

Memory-mapped, graphics data structures can reside in a *Graphics Aperture.* This aperture is an address range defined by the APBASE configuration register of PAC. The APBASE register follows the standard base address register template as defined by the PCI Specification. The size of the range claimed by the APBASE is programmed via APSIZE Register (programmed by the BIOS before a plug-and-play session is performed). The APSIZE Register allows the selection of an aperture size of 4 MB, 8 MB, 16 MB, 32 MB, 64 MB, 128 MB and 256 MB. By programming the APSIZE to a specific size, the corresponding lower bits of the APBASE are forced to 0. The default value of the APSIZE register forces an aperture size of 4 MB. The aperture address range is naturally aligned.

NOTE

When programming the APSIZE register such that the APBASE register bits change from “read only” (forced to 0) to “read/write,” the value of those bits is undefined and must be written first to have a known value. Note that the Aperture Size register (Offset B4h, Device 0) programming only effects the accessibility of bits 27:22 in the Aperture Base Register (Offset 10–13h, Device 0).

Accesses within the aperture range are forwarded to main memory. PAC translates the originally issued addresses via a translation table that is maintained in main memory. The aperture range should be programmed as not cacheable in the processor caches.

NOTE

The plug-and-play software configuration model does not allow overlap of different address ranges. Therefore, the A.G.P. aperture and the A.G.P. Memory Range are independent address ranges that may be contiguous, but not overlapping.

4.1.1.4. Address Mapping of PCI Devices on A.G.P.

The A.G.P. Memory Range registers are used also to allocate a memory address range for the PCI device (i.e., 66-MHz/3.3V PCI agent attached to the A.G.P. port). The same applies in the case of a multi-functional A.G.P. device where one or multiple of the functions are implemented as PCI-only devices.

4.1.2. SYSTEM MANAGEMENT MODE (SMM) MEMORY RANGE

PAC supports the use of main memory as SMM memory when the system management mode is enabled. When this function is disabled, the memory address range A0000h–BFFFFh is normally defined as a video buffer range where accesses are directed to either A.G.P. or PCI and physical DRAM memory is not accessed. When SMM is enabled via SMRAM configuration register the A0000h–BFFFFh range is used as a SMM RAM and no accesses from PCI or A.G.P. bus are allowed. CPU bus cycles executed in SMM mode access the A0000h–BFFFFh range by being mapped to a corresponding physical DRAM address range instead of being forwarded. Before this space is accessed in SMM mode, the corresponding main memory range must be first initialized. This is done using SMRAM register. Opening of SMM space in the 0C0000h–0CFFFFh is also allowed using the SMRAM register.

NOTE

A PCI or A.G.P. initiator can not access SMM space.

4.1.3. MEMORY SHADOWING

Any block of memory that can be designated as read only or write only can be “shadowed” in main memory. Typically, this is done to allow ROM code to execute more rapidly out of main memory. ROM is used as a read only during the copy process while DRAM is designated write only at the same time. After copying, the DRAM is designated read only so that ROM is shadowed. CPU bus transactions are routed accordingly.

4.1.4. I/O ADDRESS SPACE

PAC does not support the existence of any other I/O devices besides itself on the host bus. PAC generates either PCI or A.G.P. bus cycles for all CPU I/O accesses. PAC contains two internal registers in the CPU I/O space—CONFADD register and CONFDATA register. These locations are used to implement PCI configuration space access mechanism and is described in the Register Description section.

The CPU allows 64 KB to be addressed within the I/O space. PAC propagates the CPU I/O address without any translation on to the destination bus and, therefore, provides addressability for 64-KB locations. Note that the upper three locations past the 64-K boundary can be accessed only during I/O address wrap-around

when the CPU bus A16# address signal is asserted. A16# is asserted on the CPU bus when an I/O access is made to 4 bytes from address 0FFFDh, 0FFFEh, or 0FFFFh. A16# is also asserted when an I/O access is made to 2 bytes from address 0FFFFh.

The I/O accesses (other than addresses for PCI configuration space access) are forwarded normally to the PCI bus, unless they are in the A.G.P. I/O address range as defined by the following mechanisms.

A.G.P. Address Mapping

PAC directs I/O accesses to the A.G.P. port if they fall within the A.G.P. I/O address range. This range is defined by the A.G.P. I/O Base Register (AIOBASE) and A.G.P. I/O Limit Register (AIOLIMIT). Decode for these ranges is based on the following concept:

The top 4 bits of the I/O Base and I/O Limit registers correspond to address bits A[15:12] of an I/O address. For the purpose of address decoding, PAC assumes that the lower 12 address bits A[11:0] of the I/O base are zero and that address bits A[11:0] of the I/O limit address are FFFh. This forces I/O address range to be aligned to 4-KB boundary and to have a size granularity of 4 KB. The address range covered by these registers is defined by the following equation:

$$Base\_Address \leq Address \leq Limit\_Address$$

The effective size of the range is programmed by the plug-and-play configuration software and depends on the size of I/O space claimed by the A.G.P. device. PAC also forwards accesses to the Legacy VGA I/O ranges as defined and enabled by the “virtual” PCI-to-PCI bridge BCTRL and PCICMD1 configuration registers.

Address Mapping of PCI Devices on A.G.P.

The same A.G.P. I/O range is also used to allocate an I/O address range for the PCI device (i.e., agent attached to the A.G.P. port). The same applies in the case of a multi-functional A.G.P. device where one or more of the functions are implemented as PCI-only devices.

4.1.5. PAC DECODE RULES AND CROSS-BRIDGE ADDRESS MAPPING

The address map described above applies globally to accesses arriving on any of the three interfaces (i.e., Host bus, PCI, or A.G.P.).

4.1.5.1. PCI Interface Decode Rules

PCI accesses in the PCI range are not accepted. Accesses that do not fall within the PCI range but are within main memory, the A.G.P. range, or the Graphics Aperture range, are forwarded as described above. Note that only PCI memory write accesses within A.G.P. Memory Window ranges (which do not overlap with Graphics Aperture range) are forwarded to A.G.P. PCI cycles that are not claimed by PAC are either subtractively decoded or master-aborted on the PCI.

4.1.5.2. A.G.P. Interface Decode Rules

Cycles Initiated Using PCI Protocol

Accesses between the A.G.P. port and the PCI port are limited to memory writes using the A.G.P. FRAME# protocol. All A.G.P. memory write cycles will be claimed by PAC. If the addresses are not within the main DRAM range or Graphics Aperture range, the cycle will be forwarded to the PCI bus.

When the A.G.P. master issues a memory read transaction using FRAME# semantics, the cycle will be claimed by PAC only if the address is within main DRAM range or Graphics Aperture Range. All other memory read requests will be master-aborted as a consequence of PAC not responding to a transaction.

If the agent on A.G.P. issues an I/O, Configuration or Special Cycle transaction, PAC will not respond and the cycle will result in a master-abort.

Cycles Initiated Using A.G.P. Protocol

All cycles initiated using A.G.P. PIPE# or SBA protocol must reference main memory (i.e., main DRAM address range or Graphics Aperture range). If a cycle is outside of the main memory range, then it will terminate as follows:

- Reads: return random value.
- Writes: terminated internally without affecting any buffers or main memory.

4.1.5.3. Legacy VGA and MDA Ranges

The legacy VGA memory range A0000h–BFFFFh is mapped either to PCI or A.G.P. depending on the programming of the BCTRL1 and PCICMD1 configuration registers. The same registers control mapping of VGA I/O address ranges. VGA I/O range is defined as addresses where A[9:0] are in the ranges 3B0h to 3BBh and 3C0h to 3DFh (inclusive of ISA address aliases—A[15:10] are not decoded).

The legacy MDA range is not always forwarded with the VGA range. It may be necessary to forward MDA to PCI (for eventual forwarding to ISA) while forwarding VGA to A.G.P. This would be necessary if an ISA MDA adapter and an A.G.P. VGA adapter were in the system.

Table 13 explains the interaction of the ISA Enable, VGA Enable, MDA Enable bits and IOBASE/IOLIMIT registers:

Table 13. Legacy Programming Considerations

VGA Enable	IOBASE/IOLIMIT	ISA Enable	MDA Enable	Cycles Forwarded to
0	Outside	0	0	PCI/ISA
0	Outside	0	1	Invalid
0	Outside	1	0	PCI/ISA
0	Outside	1	1	Invalid
0	Inside	0	0	A.G.P.
0	Inside	0	1	Invalid
0	Inside	1	0	PCI/ISA
0	Inside	1	1	Invalid
1	Outside	0	0	PCI/ISA
1	Outside	0	1	PCI/ISA
1	Outside	1	0	PCI/ISA
1	Outside	1	1	PCI/ISA
1	Inside	0	0	PCI/ISA
1	Inside	0	1	PCI/ISA
1	Inside	1	0	PCI/ISA
1	Inside	1	1	PCI/ISA

4.2. Host Interface

The host interface of the 82443LX supports the Pentium II processor with a bus clock frequency of 66 MHz. PAC implements the address, control, and data bus interfaces for the 440LX AGPset. Host bus addresses are decoded by PAC for accesses to main memory, PCI memory, PCI I/O, PCI configuration space, and A.G.P. space (memory, I/O and configuration). PAC takes advantage of the pipelined addressing capability of the Pentium II processor to improve overall system performance.

PAC is optimized for a uni-processor system and supports the symmetrical multiprocessor configurations of up to two CPUs on the host bus.

PAC interface to the host bus includes a four deep in-order queue to track pipelined bus transactions. When the in-order queue is near full, the CPU bus pipeline is halted by asserting BNR#. BNR# is asserted until the in-order queue begins to drain.

To allow for high speed write capability for graphics, the Pentium II processor has introduced the WC memory type. This provides a write combining buffering mechanism for write operations. A high percentage of graphics transactions are writes to the memory mapped graphics region, normally known as the linear frame buffer. Reads and writes to WC are noncached and can have write side effects.

In the case of graphics, current 32-bit drivers (without modifications) would use Partial Write host bus cycles to update the frame buffer. The highest performance write transaction on the host bus is the Line Write. By

combining the several back-to-back Partial write transactions (internal to the CPU) into a Line write transaction on the CPU bus, the performance of frame buffer accesses is greatly improved. To this end, the CPU supports the WC memory. Writes to WC memory can be buffered and combined in the processor's write combining buffers (WCB). The WCB is flushed after executing a serializing, locked, I/O instruction, or the WCB is full (32 bytes). To extend this capability to the current drivers, it is necessary to set up the linear frame buffer address range to be WC memory type. This can be done by programming the MTRR registers in the CPU. Note that for dual processors, the MTRR must be programmed identically.

If non-contiguous bytes are written to the WCB, upon eviction, a series of write partial transactions will be performed. If a series of contiguous writes are written to a WC memory region (such as a copy) a series of write line transactions will be performed. PAC further optimizes this by providing write combining for CPU-to-PCI or CPU-to-A.G.P. write transactions. If the target of CPU writes is the PCI memory, data is combined and sent to the PCI bus as a single write burst. The same concept applies to CPU writes to A.G.P. memory. The WC writes that target DRAM are handled as regular main memory writes.

Note that the application of the WC memory attribute is not limited to the frame buffer and that PAC implements combining for any CPU-to-PCI or CPU-to-A.G.P. posted write, independent of the WC memory attribute.

The PAC host bridge allows an additional level of concurrency for CPU Write accesses to WC space on PCI during the time when the I/O bridge (i.e., PIIX4) prevents posting of the writes (via PHLD#/PHLDA# protocol) destined to UC (uncacheable space) located on PCI or ISA.

The PAC defers Stop Grant Acknowledge cycles generated by the processor in response to STPCLK# being asserted. The PAC completes the Stop Grant Acknowledge on the PCI bus and then issues a Defer Reply Transaction on the host bus to complete the Stop Grant Acknowledge cycle back to the processor. Once the Stop Grant Acknowledge has been completed on the PCI bus, there may be a delay in issuing the Defer Reply Transaction caused by high priority A.G.P. traffic. This delay prevents the use of clock throttling as defined in the 82371AB PIIX4 with the PAC. 440LX system designers should not enable manual (BIOS control) or thermal (THRM# pin active) clock throttling as defined in 82371AB PIIX4 datasheet.

4.3. DRAM Interface

The 82443LX integrates a main memory DRAM controller that supports a 72-bit memory data interface (64-bit memory data plus 8 ECC bits). The DRAM types supported are Extended Data Out (EDO), and Synchronous DRAM (SDRAM). PAC generates the Row Address Strobe/Chip Selects (RCSA# and RCSB#), Column Address Strobe/Data Mask (CDQA# and CDQB#), SCAS#, SRAS#, CKE, WE#, and Memory Addresses (MA) for the DRAM array. For CPU/PCI/A.G.P.-to-DRAM cycles, the address and data flows through PAC. PAC generates data on the MD and MECC busses for writes, and accepts data on these busses during reads. PAC also asserts ECCERR# in the event of a single-bit correctable or multi-bit uncorrectable error, if enabled. The PAC DRAM interface operates synchronously to the CPU clock. The DRAM controller interface is fully configurable through a set of control registers.

PAC supports industry standard 64/72-bit wide DIMM modules with EDO or SDRAM devices. Fourteen memory address signals (MAx[13:0]) allow PAC to support a wide variety of commercially available DIMMs. Both symmetrical and asymmetrical addressing are supported. Eight RCS# lines permit up to eight 64-bit wide rows of DRAM. For write operations of less than a QWord, PAC will either perform a byte-wise write (non ECC protected configuration) or a read-modify-write cycle by merging the write data on a byte basis with the previously read data (ECC configurations). PAC supports 50 ns and 60 ns EDO DRAMs, 66-MHz SDRAMs with CL2 and CL3, and supports both single and double-sided DIMMs.

Refresh functionality (DRAM refresh rate is 1 refresh/15.6 μs) is provided and there is a seven deep refresh queue with three levels of request priority. The refresh queue can be disabled, resulting in a high priority refresh request for every time-out. If the queue is enabled, the refresh request priority will work as follows:

- The high priority refresh request asserts when the queue is full and takes priority over all other DRAM operations.
- The medium priority request asserts when 4 queue slots are filled and takes priority over all other DRAM operations except A.G.P. expedites.
- Finally, the low priority request asserts when 1 queue slot is filled and only executes if there are no other DRAM operations in progress or pending.

The DRAM interface of PAC is configured by the Aperture Base Configuration Register, Graphics Aperture Remapping Table Base Register, A.G.P. Control Register, PAC Configuration Register, Memory Buffer Strength Control Register, DRAM Control Register, DRAM Timing Register, DRAM Row Type Register, and DRAM Row Boundary (DRB) Registers.

The DRAM configuration registers control the DRAM interface to select EDO DRAM or SDRAM DRAMs, RAS timings, and CAS rates. The eight DRB registers define the size of each row in the memory array, enabling PAC to assert the proper RCSA#/RCSB# line (Row Address A & B#/Chip Select#), for accesses to the array. PAC closes the page when there are no more DRAM requests and the DRAM arbiter (conceptual) enters the IDLE state. PAC does, however, hold the last accessed memory page open for PCI or A.G.P.-to-DRAM read accesses until there is a page miss or refresh.

Seven Programmable Attribute Map (PAM) registers are used to specify the PCI enable, and read/write status of the memory space between 640 KB and 1 MB. Each PAM Register defines a specific address area enabling the system to selectively mark specific memory ranges as read only, write only, read/write, or disabled. PAC supports one fixed memory hole selectable as either from 512 KB to 640 KB or from 15 MB to 16 MB in main memory. The SMRAM memory space is controlled by the SMRAM control register. This register selects if the SMRAM space is enabled, opened, closed, or locked.

NOTE

These MECC signals must be low when RSTIN# is negated. If CKE is low (clock disabled), SDRAM DIMMs could continue to drive the MECC lines through reset (the lines will stay in their existing state when CKE is low). RSTIN# should be inverted and tied to the output enable of the tri-state buffer that drives the CKE signal to the DIMMs. Thus, the tri-state buffer will tri-state and the pull-up resistors will pull CKE high (and the DIMMs can finish the cycle). This causes the SDRAM DIMMs to tri-state.

The MECC signals must be low when RSTIN# is negated. RSTIN# should be inverted and tied to the OE# pin on all DIMM sockets. If the DIMMs continue to drive the ECC lines at reset, this ensures that the signals are not being driven when RSTIN# is negated. It is possible that will keep CAS# asserted during reset and therefore EDO DIMMs will continue to drive their ECC lines.

4.3.1. DRAM ORGANIZATION AND CONFIGURATION

In the following discussion the term *row* refers to a set of memory devices that are simultaneously selected by a RCS[A,B]#/CS# signal. PAC supports a maximum of 8 rows of memory in memory configuration #1, or 6 rows in memory configuration #2. A row may be composed of one or more discrete DRAM devices (e.g., planar motherboard memory), or single-sided or double-sided DIMM modules arranged in sockets on the motherboard.

NOTE

The main DRAM design target is EDO/SDRAM configuration using 168-pin unbuffered DIMMs.

To create a memory array certain rules must be followed. The following set of rules allows for optimum configurations.

Rules for populating a PAC Memory Array

- DIMM sockets can be populated in any order. However, to take advantage of potentially faster MA timing it is recommended to populate sockets in order.
- SDRAM and EDO DIMMs can be mixed within the memory array.
- The DRAM Timing register, which provides the DRAM speed grade control for the entire memory array, must be programmed to use the timings of the slowest DRAMs installed.

PAC Memory Array Configurations

PAC offers multiplexed memory interface signals to support both large memory arrays (to reach a maximum memory size of 1 GB (EDO) or 512 MB (SDRAM), or smaller memory arrays (with minimal external signal buffering). PAC offers two memory configuration types, each offering a different memory signal interface. These memory configurations are selectable upon Boot/RESET by a strapping option on the CKE signal (*please refer to the CKE signal description table for more details*).

Configuration #1: Enables large memory arrays (up to 8 rows) with two copies of Row Address Strobe/Chip Selects (RCSAxx# & RCSBxx#), and extra copies of Column Address Strobe/Data Mask 5 & 1, (CDQB[5 & 1]# are the most loaded CAS#/DQM signals when using ECC DIMMs). Four SRAS#, SCAS# and WE# signals are also provided. This configuration supports Single-Sided and Double-Sided x8 and x16 DIMMs, and Single-Sided x4 DIMMs. The Configuration #1 interface signals are shown in Figure 5.

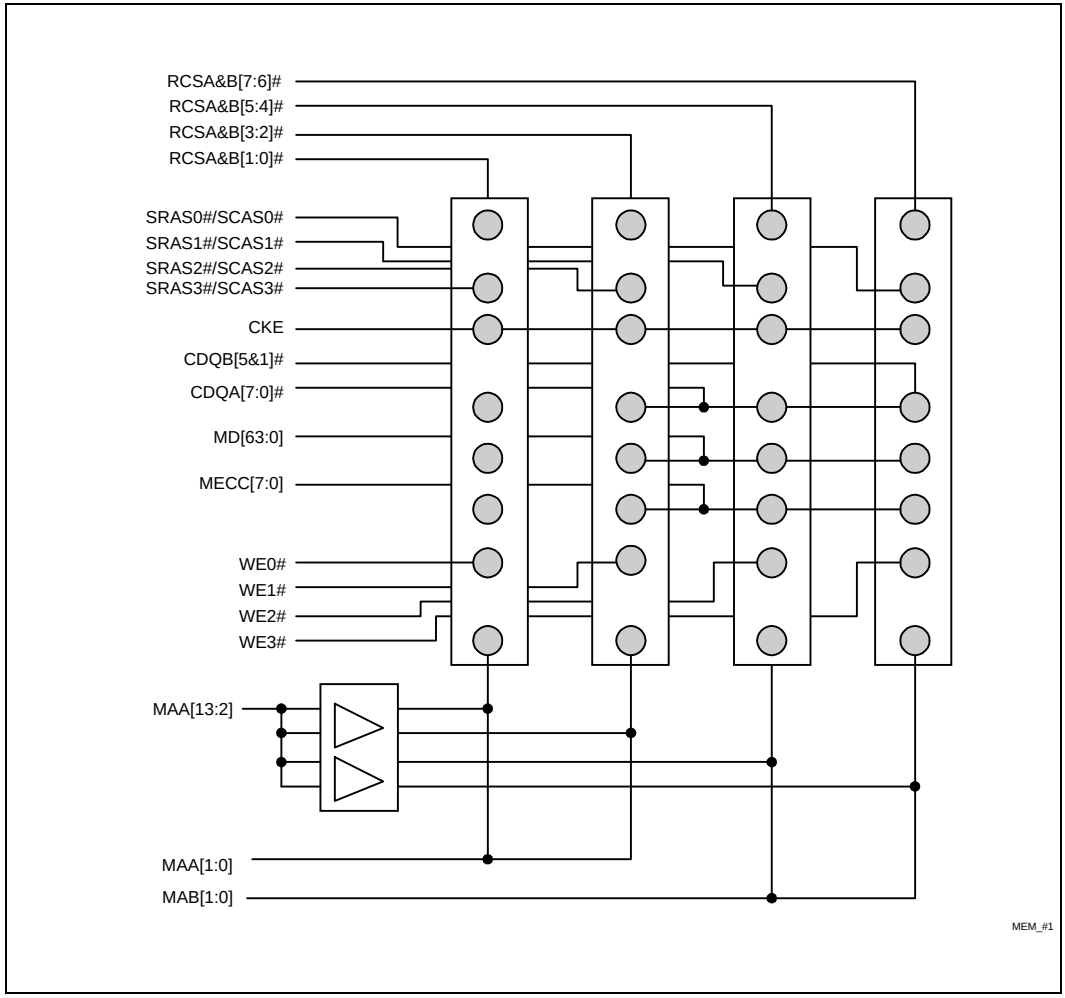


Figure 5. Configuration #1 (Large Memory Array)

In memory configuration #1, a buffered copy of MA[13:2] will go to all 4 DIMM sockets. MAA[1:0] will go to DIMM socket 1 and DIMM socket 2, and MAB[1:0] will go to DIMM socket 3 and DIMM socket 4. CDQA[7:0]# will go to DIMM socket 1 and DIMM socket 2. CDQA[7,6,4-2,0]# will go to DIMM socket 3 and DIMM socket 4. CDQB[5&1]# will go to DIMM 3 and DIMM 4.

One CKE signal provided by PAC is buffered and connected to each DIMM socket. Use a CMOS buffer to provide copies of the CKE signal. four copies of the WE# signal are provided by PAC, and one is connected to each DIMM socket.

The signal connections shown will support both EDO DRAM and SDRAM in the same memory array.

Configuration #2: Enables small memory arrays (up to 6 rows) with two copies of Memory Address signals. Three SRAS#, SCAS# and WE# signals are provided to support 3 DS DIMM sockets. This configuration supports Single-Sided and Double-Sided x8 and x16 DIMMs. The Configuration #2 interface signals are shown in Figure 6.

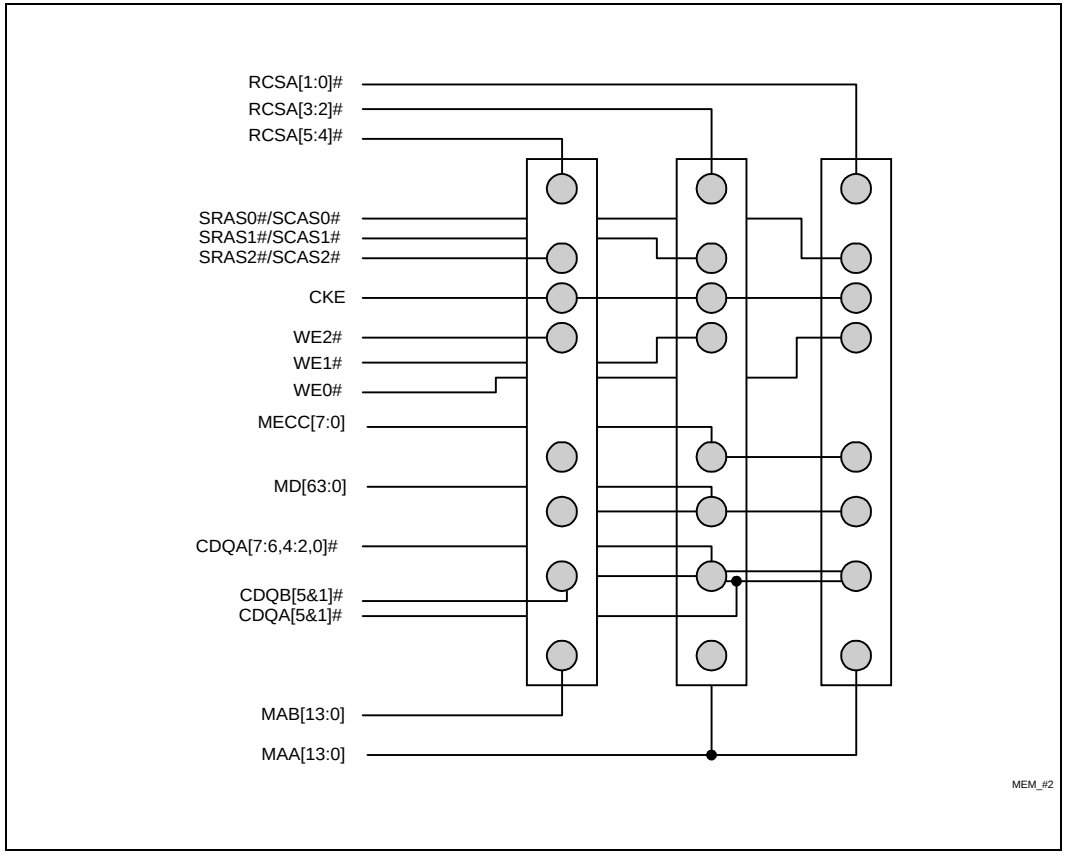


Figure 6. Configuration #2 (Small Memory Array)

In memory configuration #2, MAB[13:0] are connected to the closest DIMM socket to PAC. MAA[13:0] is connected to DIMM sockets 2 and 3. No external buffering is needed on the memory control and address signals.

One CKE signal provided by PAC is buffered and connected to each DIMM socket. Use a CMOS buffer to provide copies of the CKE signal. three copies of the WE# signal are provided by PAC, and one is connected to each DIMM socket.

The signal connections shown will support both EDO DRAM and SDRAM in the same memory array.

Table 14 provides a summary of the characteristics of memory configurations supported by PAC. Minimum values listed are obtained with single-density DIMMs and maximum values are obtained with double-density DIMMs. The minimum values used are also the smallest upgradable memory size.

Table 14 assumes Unbuffered EDO DRAM DIMMs and Unbuffered SDRAM DIMMs. The minimum memory size is for one row populated. The maximum memory size is 8 rows for memory configuration #1, and 6 rows for memory configuration #2.

Table 14. Minimum (Upgradable) and Maximum Memory Size for each configuration

DRAM Tech.	DRAM Depth	DRAM Width	DRAM DIMM		DRAM Addressing	Address Size		DRAM Array Size			
			SD	DD		Row	Col	Config #1		Config #2	
4M EDO	1M	4	1Mx72	2Mx72	Symmetric	10	10	8 MB	128 M[4]B	—	—
16M EDO	1M	16	1Mx72	2Mx72	Symmetric	10	10	8 MB	128 MB	8 MB	96 MB
16M EDO	1M	16	1Mx72	2Mx72	Asymmetric	12	8	8 MB	128 MB	8 MB	96 MB
16M EDO	2M	8	2Mx72	4Mx72	Asymmetric	11	10	16 MB	256 MB	16 MB	192 MB
16M EDO	2M	8	2Mx72	4Mx72	Asymmetric	12	9	16 MB	256 MB	16 MB	192 MB
16M EDO	4M	4	4Mx72	8Mx72	Symmetric	11	11	32 MB	512 M[4]B	—	—
16M EDO	4M	4	4Mx72	8Mx72	Asymmetric	12	10	32 MB	512 M[4]B	—	—
64M EDO	2M	32	2Mx72	4Mx72	Asymmetric	11	10	16 MB	256 MB	16 MB	192 MB
64M EDO	2M	32	2Mx72	4Mx72	Asymmetric	12	9	16 MB	256 MB	16 MB	192 MB
64M EDO	2M	32	2Mx72	4Mx72	Asymmetric	13	8	16 MB	256 MB	16 MB	192 MB
64M EDO	4M	16	4Mx72	8Mx72	Symmetric	11	11	32 MB	512 MB	32 MB	384 MB
64M EDO	4M	16	4Mx72	8Mx72	Asymmetric	12	10	32 MB	512 MB	32 MB	384 MB
64M EDO	8M	8	8Mx72	16Mx72	Asymmetric	12	11	64 MB	1 GB[3]	64M	384 MB
64M EDO	16M	4	16Mx72	32Mx72	Symmetric	12	12	128 MB	1 GB[3]	—	—
16M[1] SDRAM[1]	1M	16	1Mx72	2Mx72	Asymmetric	11	8	8 MB	128 MB	8 MB	96 MB
16M[1] SDRAM[1]	2M	8	2Mx72	4Mx72	Asymmetric	11	9	16 MB	256 MB	16 MB	192 MB
64M[1] SDRAM[1]	4M	16	4Mx72	8Mx72	Asymmetric	11	10	32 MB	512 MB	32 MB	384 MB
64M[1] SDRAM[1]	4M	16	4Mx72	8Mx72	Asymmetric	13	8	32 MB	512 MB	32 MB	384 MB
64M[1] SDRAM[1]	8M	8	8Mx72	16Mx72	Asymmetric	13	9	64 MB	512 MB	64 MB	384 MB
64M[2] SDRAM[1]	4M	16	4Mx72	8Mx72	Asymmetric	12	8	32 MB	512 MB	32 MB	384 MB
64M[2] SDRAM[1]	8M	8	8Mx72	16Mx72	Asymmetric	12	9	64 MB	512 MB	64 MB	384 MB

NOTES:

1. 2-bank SDRAM DIMMs.
2. 4-bank SDRAM DIMMs.
3. 1-GB memory array is achieved by using Double-Sided Buffered EDO DIMMs.
4. Single-Sided DIMMs only.

Supported DRAM Types

PAC supports both EDO (Extended Data Out) DRAM and SDRAM (Synchronous DRAM). PAC supports a 2-KB page size and page mode is always active. PAC supports ECC and non-ECC types of both EDO and SDRAM.

Extended Data Out (or Hyper Page Mode) DRAM is designed to improve the DRAM read performance. The EDO DRAM holds the memory data valid until the next CAS# falling edge. With EDO, the CAS# precharge overlaps the memory data valid time. This allows CAS# to negate earlier while still satisfying the memory data valid window time.

Synchronous DRAM (SDRAM), as the name suggests, is based on the synchronous interface between the DRAM controller and DRAM components. RAS#, CAS#, WE#, and CS# are pulsed signals driven by the DRAM controller and sampled by the DRAM components at the positive clock edge of an externally supplied clock (synchronous to 66-MHz system clock).

4.3.1.1. Configuration Mechanism for DIMMs

PAC DRAM Controller uses the Serial Presence Detect (SPD) mechanism for memory array configuration, as defined in the JEDEC 168-pin DIMM Standard Specification.

NOTE

It is very difficult to program the 82443LX DRAM Timing Register (Register 58h, Device #0) and the DRAM Buffer Strength register (Register 6C–6Fh, Device #0) without information garnered using Serial Presence Detect (SPD). Thus, support for SPD in a PAC memory array is required.

The system BIOS must program the DRAM size, type, timing, and buffer strength registers in the 82443LX. It gathers this information by the Serial Presence Detect (SPD) mechanism.

DRAM Configuration is performed by the BIOS, which follows these six steps:

1. The system BIOS must loop through the rows of memory (8 rows for Memory Configuration #1, 6 rows for Memory Configuration #2) reading Serial Presence Detect (SPD) data. This will allow it to determine whether each DIMM in the array is single or double sided. The system BIOS must also determine the type of memory contained in each row, and set the DRAM Type registers accordingly (DRT—Device #0, Register 55–56h). Also, note that, at this time, system BIOS should determine the SLOWEST CAS Latency of all of the available SDRAM DIMMs in the array.
2. BIOS must next loop through the rows of memory, initialize and configure each row of SDRAM. Note that the SDRAM DIMMs will ALL be programmed to either CAS Latency=2 or CAS Latency=3; whichever is the SLOWEST DIMM found in step 1.
3. BIOS must next loop through the rows of memory, reading SPD data to determine the DRAM size. The DRB's (DRB[7:0]—device #0, register 60–67h) can now be set. Additionally, several different bytes of SPD data can be read to determine the timing values to be used when programming the memory timing register (DRAMT—device #0, register 58h) and to determine if ECC can be enabled (if all available DIMM's support ECC).
4. BIOS must next program the Memory Buffer Strength Control Register (MBSC—device #0, register 6C–6Fh). To program this register properly, additional bytes of SPD data must be read for each row of memory.
5. BIOS can use the data found in step 3 to program the DRAM timing register (DRAMT—device #0, register 58h).
6. Lastly, if ALL of the DIMM's in the array support ECC, then ECC should be enabled in PAC.

4.3.2. DRAM ADDRESS TRANSLATION AND DECODING

The 82443LX translates the address received on the host bus to an effective memory or PCI address. This translation takes into account memory holes and the normal host to memory or A.G.P./PCI address. PAC supports a maximum of 64-Mbit DRAM device. PAC supports the DRAM page size of the smallest density DRAM that can be installed in the system. For 72-bit DIMMs, the overall DRAM DIMM page size is 8 KB. The page offset address is driven over MA[8:0] when driving the column address. MAx[13:0] are translated from the address lines A[26:3] for all memory accesses. The multiplexed row/column address to the DRAM memory array is provided by the MAx[13:0] signals. The MAx[13:0] bits are derived from the host address bus, as defined by Table 15, for symmetrical and asymmetrical DRAM devices.

Table 15. DRAM Address Translation

		Memory Address													
		13	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Row Size	**Row**	**A24**	**A23**	**A12**	**A22**	**A21**	**A20**	**A19**	**A18**	**A17**	**A16**	**A15**	**A14**	**A13**	**A11**
8 MB	Col_s			A12	P			A10	A9	A8	A7	A6	A5	A4	A3
	Col_e	A24	A23	A26	A12	A22	A12	A10	A9	A8	A7	A6	A5	A4	A3
16 MB	Col_s			A12	P		A23	A10	A9	A8	A7	A6	A5	A4	A3
	Col_e	A24	A23	A26	A12	A12	A23	A10	A9	A8	A7	A6	A5	A4	A3
32 MB	Col_s	A24	A23	A12	P	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3
	Col_e	A24	A23	A26	A12	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3
64 MB	Col_s	A24	A23	A12	P	A26	A25	A10	A9	A8	A7	A6	A5	A4	A3
	Col_e	A24	A23	A26	A25	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3
128 MB	Col_s	A24	A23	A12	P	A26	A25	A10	A9	A8	A7	A6	A5	A4	A3
	Col_e	A24	A23	A26	A25	A24	A23	A10	A9	A8	A7	A6	A5	A4	A3

NOTES:

Col_s=SDRAM Column Address Mapping. Col_e=EDO Column Address Mapping. P=denotes the pre-charge bit for SDRAM.

Table 16. 82443LX EDO DRAM Addressing

Memory Organization	Addressing	Address Size
4 MB		
1M x 4	Symmetric	10 x 10[1]
16 MB		
1M x 16	Symmetric	10 x 10
	Asymmetric	12 x 8
2M x 8	Asymmetric	11 x 10
	Asymmetric	12 x 9
4M x 4	Symmetric	11 x 11[1]
	Asymmetric	12 x 10[1]
64 MB		
2M x 32	Asymmetric	11 x 10
	Asymmetric	12 x 9
	Asymmetric	13 x 8
4M x 16	Symmetric	11 x 11
	Asymmetric	12 x 10
8M x 8	Asymmetric	12 x 11
16M x 4	Symmetric	12 x 12[1]

NOTES:

1. Single-Sided Unbuffered DIMMs.

Table 17. PAC SDRAM Addressing

Memory Organization	Addressing	Address Size	Bank Select
16 Mb (2-Bank)			
1M x 16	Asymmetric	11 x 8	1
2M x 8	Asymmetric	11 x 9	1
4M x 4	Asymmetric	11 x 10[1]	1
64 Mb (2-Bank)			
4M x 16	Asymmetric	11 x 10	1
		13 x 8	1
8M x 8	Asymmetric	13 x 9	1
64 Mb (4-Bank)			
4M x 16	Asymmetric	12 x 8	2
8M x 8	Asymmetric	12 x 9	2

NOTES:

1. Single-Sided DIMMs.

4.3.3. REFRESH CYCLES (CAS# BEFORE RAS#)

PAC supports CAS#-before-RAS# DRAM refresh cycles and generates refresh requests. When a refresh request is generated, it is placed in a 4 entry queue (this queue can be disabled in the DRAM Control Register, offset 57h, bit 6). PAC services a refresh request when the refresh queue is not empty and the controller has no other requests pending. When the refresh queue has accumulated four requests, refresh becomes the highest priority request and is serviced next by PAC.

PAC implements a “smart refresh” algorithm. Refresh is only performed on rows that are populated. In addition, PAC supports refresh staggering to minimize the power surge associated with refreshing a large DRAM array. PAC also supports concurrent refresh cycles in parallel with Host to A.G.P. or PCI cycles.

4.3.4. DRAM SUBSYSTEM POWER MANAGEMENT

PAC supports desktop-level power management capability. The DRAM controller within PAC supports power management of the DRAM array. Specific power management capability is engaged only when the memory array is populated with SDRAM (this includes mixed EDO/SDRAM memory array configurations), and the SPME bit of the DRAMC Register is set (bit 4 of configuration address 57h). The DRAM power management operates as follows:

PAC enters the SUSPEND state when:

- The SPME bit of the DRAMC Register is set (bit 4 of configuration address 57h).
- PAC completes all pending requests from all request queues, including the refresh queue.
- PAC closes active SDRAM pages according to PAC DRAM Paging Policy.
  a. After 4 Host clocks upon entering this state, the SDRAM CKE signal is negated and all memory rows populated with SDRAM enter a Power Down Mode.
  b. PAC remains in the SUSPEND state until any request, other than a low priority Refresh request, is pending.
  c. When in the SUSPEND regime, refresh requests are not serviced until they become a high-priority, i.e., 4 requests are queued.
  d. When a high-priority refresh request is generated (4th request queued), the DRAM controller asserts CKE. Four clocks after CKE is reasserted, the DRAM controller starts servicing refresh requests. Refreshes are serviced back-to-back (all four of them) until the refresh request queue is empty.
  e. Four clocks after reaching Idle state the DRAM controller negates CKE again (SDRAM components enter Power Down Mode again). The system stays in this state until 4 refresh requests are accumulated (typically after 4*15.6 µsec) and then PAC repeats steps 3 & 4.

The SUSPEND state is exited normally after any of the snoopable or non-snoopable request queues present an active request.

4.3.5. SERIAL PRESENCE DETECT (SPD) FOR SDRAM

A Slot 1/440LX AGPset Platform requires the support of Serial Presence Detect (SPD) for SDRAM DIMMs in the memory array. SPD is needed to gather specific DIMM information to program the Memory Buffer Strength Control Register. This information is ONLY obtainable through Serial Presence Detect.

A 82443LX (PAC) memory subsystem is dependent on the type and size of DRAM in the array. To properly program the DRAM Controller Registers, specific information is needed during Boot time. Information such as DRAM size (x4, x8, or x16), will affect the values programmed in the Memory Buffer Strength Register (Register 6C-6Fh, Device #0).

- **Why is SPD needed?** Previously, a BIOS algorithm could determine DRAM size and type dynamically. Buffer strength programming was limited to memory address signals only, based on the number of rows populated. In the PAC, every memory interface signal's buffer strength is programmable. This allows the PAC to support a wide range of DRAM types and sizes. To program these buffer strengths correctly, the BIOS needs information on DRAM size. For example, signal loading is greater when the array is populated with x4 DRAMs than x16 DRAMs. Thus, memory interface signal strengths will need to be greater.
- **Can SPD be Bypassed by disabling a row?** This is not an option. If the BIOS detects a row of SDRAM memory which does not support SPD, even if this row is disabled, signal loading from the non-SPD SDRAM DIMM exists, and the MBSR can not be programmed reliably.
- **Can an Error Message report a non-SPD DIMM?** Video is initialized during BIOS post testing well after DRAM is initialized. If the MBSR is not programmed properly, the BIOS post test will not make it far enough to report the error to the screen.

The memory subsystem must be designed to support Serial Presents Detect to properly program the Memory Buffer Strength Register. Also, ensure the SDRAM DIMMs used comply with the latest SPD JEDEC Specification, revision: December, 1996

4.3.6. SINGLE CLOCK COMMAND MODE FOR SDRAM

The graphics subsystem will potentially require data transfers of less than or equal to one QWord (8 bytes) per command consecutively during the memory access. One QWord is referred to a piece of data in a 64-bit memory interface. With CAS latency (CLT) equal to 2, there will be a 2 clock (3 clock with CLT=3) delay between the read command and data cycles. Without supporting single clock command mode, the system will not be able to achieve 1111 effective burst rate for this type of data access pattern. As illustrated from the following diagram, effective burst rate becomes 2222 with respect to the requested data if single clock command mode is not enabled.

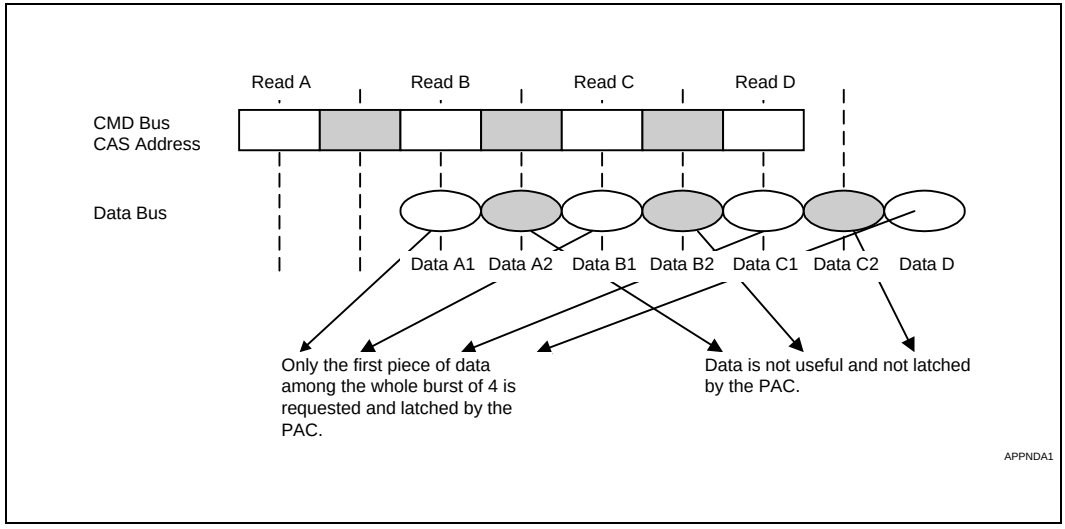


Figure 7. Single Clock Mode Disabled

To achieve the burst rate of 1111 during the above scenario, the memory controller needs to support single clock command mode. The output of each command interrupts the ongoing burst or begins at the end of 1st data cycle. With the support of single clock command mode, the timing is shown in Figure 8.

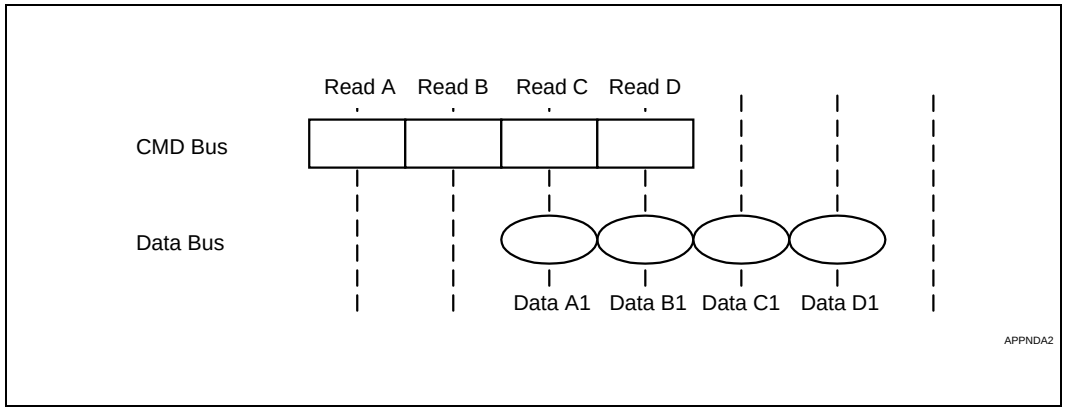


Figure 8. Single Clock Mode Enabled

Note that the support of SDRAM single clock command mode is an advanced feature for 440LX systems on a 3 DIMM design. During a burst pattern of 4 pieces of 64-bit data, if at least the first 2 pieces of data are needed, a 440LX system can still achieve a burst rate of x111 for SDRAM operation without supporting or enabling single clock command mode.

4.3.6.1. Enabling Single Clock Command Mode

MA Wait State(MAWS). This bit selects FAST or SLOW MA bus timing. Note that SLOW timing is equal to FAST + 1 in terms of clock numbers for EDO. For SDRAM, FAST timing means zero MA wait state. This setting will enable the PAC(440LX) to support single clock command mode; SLOW means one MA wait state, which forces the PAC to support the normal operation only (one command per two clocks).

4.3.6.2. Restrictions For Supporting Single Clock Command Mode

There is no support of single clock command mode for the configuration #1(4 DIMM design) because of the external buffer delay (not able to meet the AC timing). To support single clock command mode in configuration #2, the memory controller of 440LX needs to toggle memory address (CAS assertions) on every clock edge. This tightens memory AC timing requirements on the address signals. Because the loading of SDRAM modules has the direct effect on the AC timing, the maximum loading of memory module is limited while supporting single clock command mode. The following table shows the population rules and types (x8, x16, x32) of DIMM module that can be supported for running single clock command mode.

Table 18. Restrictions For Single Clock Command Mode Support

Memory config #2 (3DIMMs)				Types of SDRAM module	
DIMM Row#	MAB #3 5/4	MAA #2 3/2	MAA #1 1/0	SS/DS x8 DS x16 ECC & nonECC	SS x16 ECC & nonECC
			x	no	yes
		x		no	yes
	x			no	yes
	x	x		no	yes
	x		x	no	yes
		x	x	no	no
	x	x	x	no	no

NOTES:
x means populated, SS means single-sided, DS means double-sided.

4.3.6.3. Conclusion For Single Clock Command Mode Support

There is no support of single clock command mode for configuration #1(4 DIMMs solution). For a 3 DIMM design, as shown in the above table, set the MAWS bit to 1 to support SDRAM single clock command mode when DIMM sockets on the MAA copy is populated with:

- maximum 1 row of (0,1,2,3), and/or maximum 1 row of (4,5) for x16, regardless of ECC or non-ECC SDRAM

4.3.7. SUPPORT FOR 2 AND 4 BANKS SDRAM

The PAC supports both 2 and 4-bank SDRAM components. However, regardless of populating either 2 or 4-bank SDRAM DIMMs in a 440LX system, the SDRAM interface of the PAC can only open 2 pages at any time. The PAC is not able to open 4 pages simultaneously, even a 4-bank SDRAM module is used.

4.4. Data Integrity Support

Several data integrity features are included in PAC. These include EC or ECC on the 64-bit DRAM interface, Parity generation and checking on the PCI Bus and A.G.P. (for PCI transactions).

- **PCI Bus.** PAC implements parity generation/checking as defined by the PCI Specification. PAC can generate parity errors via the PERR# pin, if enabled via the PCICMD register. The PCISTS register logs error information related to the PERR# assertion. PERR# error conditions can be reported via the SERR# signal, if enabled in the ERRCMD register.
- **A.G.P. Bus.** For operations on the A.G.P. interface using PCI protocol, PAC supports Parity generation/checking as defined by the PCI Specification. PAC can generate parity errors via the GPERR# pin if this capability is enabled by the PCICMD1 (PCI Command) register. Bits of the PCISTS1 (PCI Status) register provide status information related to the GPERR# assertion. The ERRCMD (Error Command) register provides the capability to configure PAC to propagate GPERR# signaled error conditions onto the system SERR# signal.
- **Main Memory DRAM Protection Modes.** PAC supports three modes of data protection of the DRAM array: (These modes of operation are selected via bits [8:7] of PACCFG Configuration Register, offset 50–51h).
  - **Non-ECC (with Byte-Wise Write Support).** After system reset, PAC ECC control logic is set in the default mode (non-ECC with byte-wise write capability). In this mode, there is no provision for protecting the integrity of data within the DRAM array. After the BIOS configuration software detects that all memory modules within the DRAM array support 72-bit ECC mode of operation, the default operational mode can be changed to either ECC or EC-Only.
  - **EC-Only Mode of Operation (Error Checking Only w/out data correction).** In this mode, the ECC logic calculated 8-bit pattern is written, along with the 64-bit data, into main DRAM. Note that during write operations, an entire QWord must be written. This may require a read-merge-write operation if a quantity of less than a QWord is written to main memory.

    During read operations, 8-bit ECC code is read along with 64-bit data, and Error checking is performed. If an error is detected, a corresponding bit is set in the ERRSTS register and the condition is signaled to the rest of the system via the ECCERR# signal, or (if enabled) via SERR# logic. No correction of data takes place in this mode of operation.
  - **Main Memory (DRAM) ECC (Error Checking with data Correction).** When ECC is enabled and ERRCMD is used to set SERR# functionality, ECC errors are reported to the system via the SERR# pin. PAC can be programmed to signal SERR# on uncorrectable errors, correctable errors, or both. The type of error condition is latched until cleared by software (regardless of SERR# signaling). When a single or multi-bit error is detected, the offending DRAM row ID is latched in the ERRSTS register in PAC. The latched value is held until software explicitly clears the error status flag.

4.4.1. ECC GENERATION

When enabled, the DRAM ECC mechanism allows automatic generation of an 8-bit protection code for the 64-bit (QWord) of data during DRAM write operations. If the originally requested write operation transfers single or multiple QWords of data, then the ECC-protected DRAM writes are completed with no overhead (ECC code is calculated and written along with the data). If the originally requested write operation transfers less than 64 bits of data (less than a QWord), then PAC performs a READ-MERGE-WRITE operation. During this operation, the current memory contents are read from the QWord location to which new data needs to be written. Note that this read cycle is also checked for correct ECC (and single bit errors corrected if they occur). The write data will be superimposed (i.e., merged with the read data in an internal PAC buffer). After merging, the resulting QWord is written to the DRAM along with a new ECC code which will be automatically generated based on the bit pattern of the resulting QWord.

4.4.1.1. Error Detection and Correction

ECC is an optional data integrity feature provided by PAC. The feature provides single-error correction, double-error detection, and detection of all errors confined to a single nibble (SEC-DED-S4ED) for the DRAM memory subsystem. Additional features are provided that enable software-based system management capabilities.

- **ECC Checking and Correction.** When enabled, the ECC mechanism allows a detection of single-bit and multiple-bit errors and recovery of single-bit errors. During DRAM read operations, a full QWord of data is always transferred from DRAM to PAC, regardless of the size of the originally requested data and type of selected memory protection. Both 64-bit data and 8-bit ECC code are transferred simultaneously from DRAM to PAC. The ECC checking logic in PAC generates a new ECC code for the received 64-bit data and compares it with received ECC code. If a single-bit error is detected the ECC logic generates a new "recovered" 64-bit data with a pattern which corresponds to the originally received 8-bit ECC protection code. Note that recovered data is transferred from PAC to the original requester (Host, A.G.P. or PCI interface), but PAC does not initiate the DRAM write cycle to fix the error.
- **Error Reporting.** For single-bit error indication, the SEF flag is set by PAC in the ERRSTS0 (Error Status 0) Register, along with the row number associated with the first single-bit error. Similarly, for multiple bit error indication, the MEF flag is set in the ERRSTS0 Register along with the row number associated with the first multiple bit error. After logging the first error in both single-bit and multiple-bit error cases, the register is locked until the software writes to the respective flags and clears the SEF and MEF bits. This error condition is normally reported via ECCERR# signal and it can also be reported to the system via the SERR# mechanism. This functionality is controlled by the ERRCMD (Error Command) register.
- **DRAM Scrubbing.** The DRAM (if the root-cause of the error is a DRAM array) will still contain faulty data which will cause the repetition of error detection and recovery for the subsequent accesses to the same location. However, to prevent the accumulation of the single-bit errors which may result in an unrecoverable multi-bit error, the system software *can* provide a "scrubbing" functionality. After a single-bit correctable ECC error is reported, either via a hardware mechanism (ECCERR# signal that ties to an SMI or a regular interrupt, or the SERR# signal which typically causes an NMI) or by a software mechanism (periodic polling of the ERRSTS0 Register), a DRAM "scrubbing" software routine should initiate reads followed with writes of the same data to the locations at which the single-bit error occurred. Read of the data will result in a corrected 64-bit value which will be written back to establish the correct value within the DRAM array. Since it is not critical to fix the single-bit error right away, the "scrubbing" routine can be run as a part of the lowest priority task in the multitasking operating system environment, and hence, will not impose a significant overhead in the system. Note that information in the ERRSTS0 Register can be used later on to point to a faulty DRAM DIMM if the single-bit errors constantly occur during access to that DIMM.

Multi-bit uncorrectable errors are fatal system errors and will cause PAC to assert the SERR# signal if bit 1 of the ERRCMD register is a 1. SERR# will then activate NMI. When an uncorrectable error is detected, PAC will latch the row # where the error occurred in the ERRSTS1 Register.

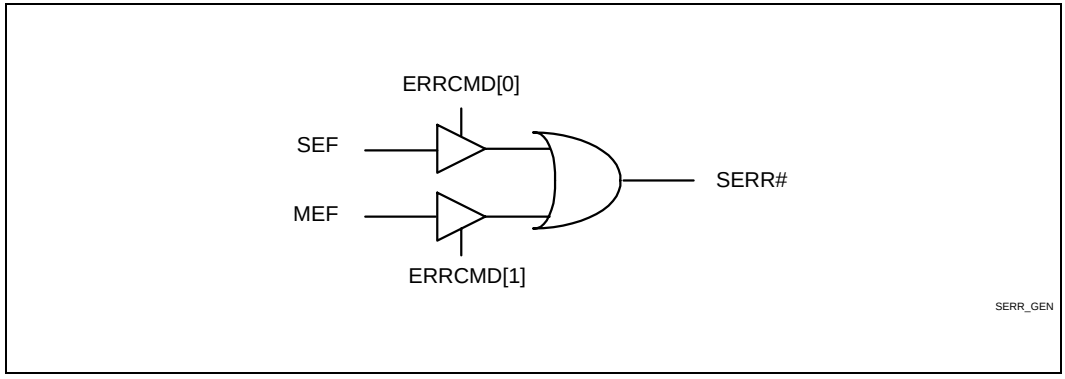


Figure 9. SERR# Generation for Single- or Double-bit Error

Software Requirements

- **Initialization.** When ECC is enabled, the whole DRAM array MUST first be initialized by doing writes before the DRAM read operations can be performed. This will establish the correlation between 64-bit data and associated 8-bit ECC code which does not exist after power-on.

4.4.1.2. ECC Test Diagnostic Mode of Operation

PAC provides the means for testing ECC at the system level via software. After reset, PAC DRAM data integrity control logic is set in the default mode of operation (i.e., non-ECC). To enter the ECC Diagnostic Mode of operation, ECC Mode must be enabled first and then the ETPDME bit (bit 6 of the PACCFG register, address offset 50–51h) must be set to 1. In the diagnostic mode, the signals MECC[7:0] are forced to 0 during DRAM writes. During DRAM reads, the MECC[7:0] signals are compared with internally generated ECC bits (depending on if ECC or non-ECC configuration is selected). Recognized errors are indicated via ECCERR# signal as in the normal mode of operation.

Single-Bit Pattern Test

Before a DRAM read operation can be executed, a write to the same location must be performed. To check for correct ECC circuitry operation, a value of Zero must be written. Reading this value back MUST NOT result in an ECC error indication. The pattern of all 72 bits (data + ECC)=0 is a correct pattern for the ECC checking logic. If the ECC configuration is selected, then a sequence of write and read operations can be executed with a single “walking” bit value of 1 in the bit pattern. Note that a write of a bit pattern with a single 1 is used to simulate the induction of a single-bit error in the DRAM array. All read operations MUST result in the corrected data (i.e., all 64 bits equal 0). Therefore, the ECC logic of fixing single bit errors can be verified for all 64-bit positions for an expected 64-bit data pattern of value zero. Single-bit detected/corrected errors are signaled via the ECCERR# mechanism and indicated via the SEF bit (bit 0) of PAC’s ERRSTS register (address offset 91–92h).

Note that from the CPU’s perspective, both 64-bit reads and writes can be split into two back-to-back 32-bit reads and two 32-bit writes. This can be used to simplify diagnostic software if more advanced software techniques (i.e., using cacheability / WC) are too difficult to be implemented.

Multi-Bit Pattern Test

If the ECC Mode is selected, checking of multiple-bit errors can be simply done by executing the sequence of writes and reads with write data containing permutations of multiple "1's." All reads will flow through the data correction circuitry and therefore the pattern of the returned read data will not match the original written pattern. It will be modified based on the algorithm defined in the *Pentium II Processor User Manual*. The error conditions are signaled via an ECCERR# mechanism and indicated via the MEF bit (bit 4) of the ERRSTS register (address offset 91–92h).

4.5. PCI Interface

The PAC Host Bridge provides a PCI Bus interface that is compliant with the *PCI Local Bus Specification*. The implementation is optimized for high-performance data streaming when PAC is acting as either the target or the initiator on the PCI bus.

NOTE

1. PAC can generate retry or disconnect cycles when accessed as a PCI target.
2. PAC can be locked as a PCI target device as defined by the PCI protocol. When locked from the PCI side, PAC disables CPU bus accesses by asserting BPRI#. The PCI-to-DRAM lock can not be established until all pending CPU-to-PCI cycles are complete. The CPU bus BPRI# mechanism is normally used to support deterministic PAC response during PCI reads. Since the first access of a locked PCI sequence must be a read, the same mechanism is used to support deterministic establishment of the lock for DRAM.
3. PAC supports the Delayed Transaction mechanism defined in the *PCI Local Bus Specification*. The process of latching all information (PCI address and command) required to complete a transaction, terminating with a retry, and then completing the request without holding the bus master in wait states is referred to as a *delayed transaction*.
4. When the host accesses the PCI, PAC can retry CPU-to-PCI cycles, if necessary.
5. PAC does not support the Distributed DMA protocol supported by the PIIX4.

4.6. A.G.P. Interface

For the definition of A.G.P. Interface functionality (protocols, rules and signaling mechanisms, as well as the platform level aspects of A.G.P. functionality), refer to *A.G.P. Interface Specification, Revision 1.0*. This document focuses only on PAC specifics of the A.G.P. interface functionality.

System Coherency/Snooping

The coherency in a system is normally maintained for all accesses directed to main memory (i.e., typically treated as a cacheable memory). The A.G.P. modifies these rules to minimize the overall impact of the coherency management overhead on system performance. It allows accesses to main memory that do not require coherency management (i.e., snoop requests on the host bus).

FRAME# Protocol Operations on A.G.P.

The A.G.P. Interface supports FRAME# protocol operations similar to those defined in the PCI Specification. Electrically, only 66-MHz FRAME# protocol operations are supported.

- **Host Bridge Target Operations.** As a target of FRAME#-initiated cycles via A.G.P., PAC responds only to memory accesses. These accesses are always directed to DRAM.
  - **Memory Read, Memory Read Line, Memory Read Multiple Operations.** PAC only responds to memory read cycles that target DRAM space. Reads to the PCI bus from an A.G.P. device are not supported.
  - **Memory Write, Memory Write and Invalidate Operations.** PAC responds to FRAME#-initiated memory writes that target either the DRAM space or the PCI Bus space.
  - **Configuration Read and Write Operations.** A.G.P. generated configuration cycles are ignored by PAC.
  - **PAC Disconnect Conditions.** PAC generates disconnect according to the A.G.P. Specification rules when being accessed as a target from the A.G.P. interface (using FRAME# protocol). The A.G.P. transaction issued using FRAME# semantics is retried by PAC based on the 32-clock rule only if there is a pending A.G.P.-to-DRAM request issued using A.G.P. protocol semantics (using PIPE# or side-band request).
  - **PAC Retry Conditions.** In the absence of A.G.P. requests, a FRAME#-initiated request is kept in wait states until it gets serviced or potentially retried due to buffer management requirements (i.e., CPU-to-A.G.P. writes occurs before A.G.P.-to-DRAM snoopable read gets serviced). PAC, as an A.G.P. target, retries the initial data phase of the FRAME#-initiated access when:
    - PAC's DRAM is locked from the CPU side or by an agent on the PCI Bus.
    - There is a CPU-to-A.G.P. posted write data that must be flushed before PAC can service A.G.P. PCI-to-DRAM reads. This also includes CPU-to-A.G.P. deferred writes.

    If, after completing the initial data phase, it takes longer than 8 A.G.P. clock periods to complete the particular data phase, the consecutive data phase(s) are disconnected.
  - **Fast Back-to-Back Transactions.** PAC, as a target, accepts fast back-to-back cycles from the A.G.P. master accessing different agents during a back-to-back sequence. As an initiator, PAC does not generate a fast back-to-back cycle.
  - **Delayed Transaction.** When an A.G.P.-to-DRAM read cycle is retried by PAC, it will be processed internally as a Delayed Transaction. PAC supports the Delayed Transaction mechanism on the A.G.P. interface as defined in the A.G.P. Specification.
- **Host Bridge Initiator Operations.** PAC translates valid CPU bus commands and PCI Bus write cycles destined to the A.G.P. bus into A.G.P. bus requests. For all CPU-to-A.G.P. transactions, PAC is a non-caching agent since PAC does not support cacheability on the A.G.P. Bus. However, PAC must respond appropriately to the CPU bus commands that are cache oriented. PAC will forward writes from the PCI bus to the A.G.P. Bus.
- **PCI Compatibility and Restrictions.** The A.G.P. Bus interface implementation is compatible with A.G.P. Specification, Revision 1.0. Transactions that are crossing from the A.G.P. Bus to the PCI Bus are limited **only** to memory writes.

4.7. Arbitration and Concurrency

PAC enhances system performance by providing a high level of concurrency (capability of running multiple operations simultaneously). System buses, as key resources, are arbitrated independently. Independent buses allow multiple transactions to be issued simultaneously. As long as transactions on the independently arbitrated buses do not compete for the common resources, they can proceed in parallel.

PAC's distributed arbitration model permits concurrency between the host bus, PCI bus, A.G.P. bus, and the DRAM interface. The arbitration algorithms and policies are designed to fulfill particular requirements of the agents sharing the resources. They may favor different aspects of system performance: low bus/resource acquisition latency, optimized instantaneous peak bandwidth, optimized sustained bandwidth, etc.

For the PCI bus, PAC supports five PCI masters in addition to the PIIX4 I/O bridge (Figure 10). REQ[4:0]#/GNT[4:0]# are used for the five PCI masters and PHLD#/PHLDA# are used for PIIX4.

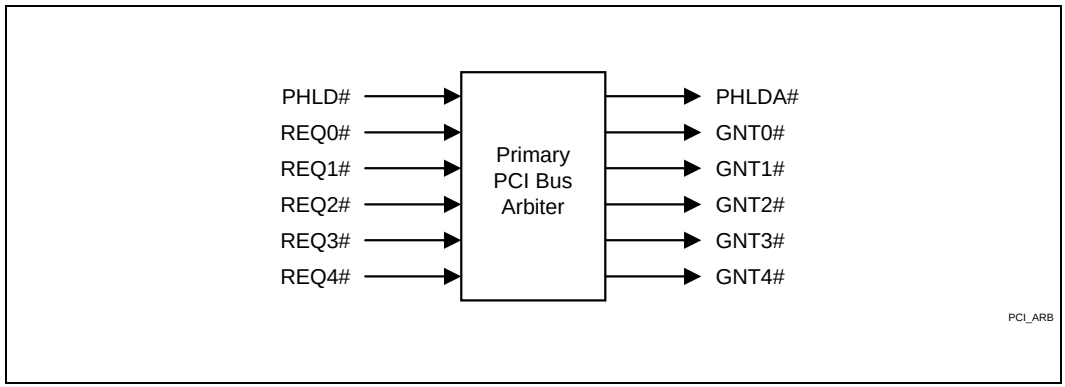


Figure 10. PCI Bus Arbiter

The PCI arbiter is based on a round robin scheme. PAC PCI Master interface (i.e., the Host) competes for PCI bus ownership only when it needs to perform CPU-to-PCI or A.G.P.-to-PCI transactions. Since most CPU-to-DRAM and A.G.P.-to-DRAM accesses can occur concurrently with PCI traffic, they do not consume PCI bandwidth. The PAC PCI arbiter uses a complete bus lock mechanism to implement PCI exclusive access operations. The arbiter implements a fairness algorithm in compliance with the PCI Local Bus Specification. The PCI arbiter's bus parking policy allows the current PCI bus owner, except for the I/O bridge, to maintain ownership of the bus as long as no request is present from any other agent.

Multi-Transaction Timer (MTT) Mechanism

The PAC PCI arbiter implements an additional control for providing a guaranteed slice of PCI bus bandwidth for bus agents which perform accesses to fragmented blocks of data and/or have real-time data transfer requirements. This mechanism is called the Multi-Transaction Timer (MTT).

The MTT is a programmable timer that facilitates a guaranteed time slot within which a PCI initiator can execute multiple back-to-back transfers, within the same arbitration cycle, to nonconsecutive regions in memory.

This capability, supported at the AGPset level, enables the implementation of lower cost peripherals. The bandwidth guarantee permits the reduction of on-chip data buffering in peripherals used for multimedia and similar applications (e.g., video capture subsystems, ATM interface, Serial Bus host controllers, RAID SCSI controllers, etc.).

PCI Bus Arbitration Policy and I/O Bridge Support

PAC supports the PIIX4 I/O bridge via the PHLD# and PHLDA# signals, with or without an external I/O APIC. PIIX4 is a special case of a PCI initiator. Because it functions as a bridge to a standard I/O expansion bus (i.e., ISA bus), it imposes specific arbitration and buffer management requirements to enable optimal concurrency between buses.

PAC and PIIX4 support the *passive release* mechanism. This mechanism avoids the shortcoming of early I/O bridges that did not allow other PCI agents to access the PCI bus while an ISA initiator owned the ISA bus. Since ISA initiators occupied the ISA bus for long and non-deterministic periods of time, PCI agents experienced the same long and non-deterministic latencies.

The PAC does not support internal disabling of PCI master bus request signals (REQX# or PHLD#). The system designer must externally disable PCI master requests if they desire to support processor states which do not allow for snooping of host bus transactions (such as SLEEP).

PAC Configuration Examples

PAC supports two PAC-PIIX4-I/O APIC configurations. This section illustrates detailed signal connections for these: PAC and PIIX4 with and without an I/O APIC:

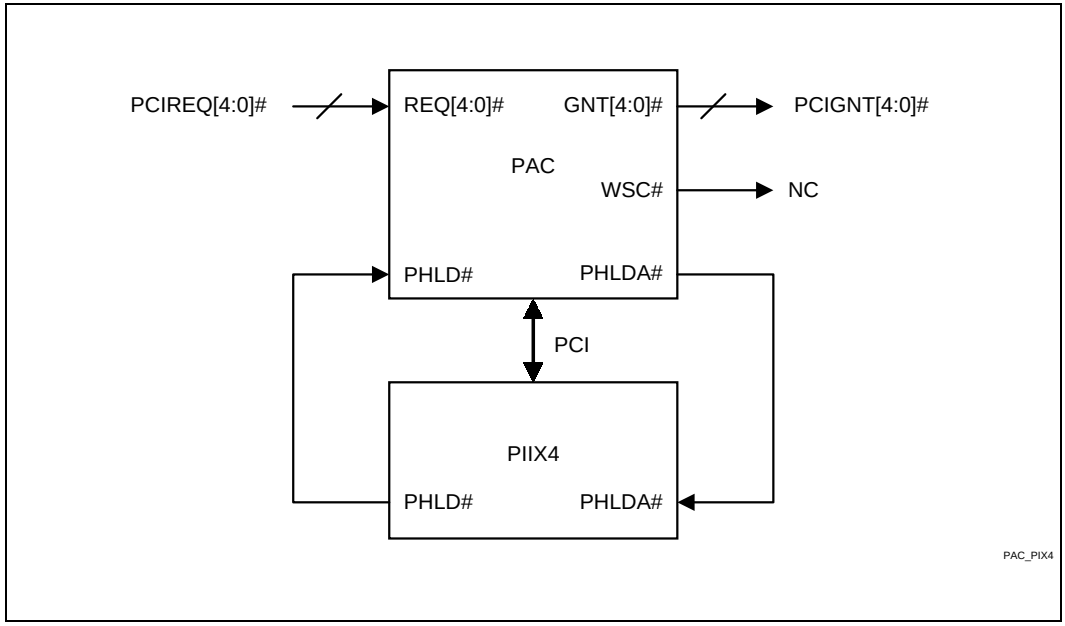


Figure 11. PAC and PIIX4

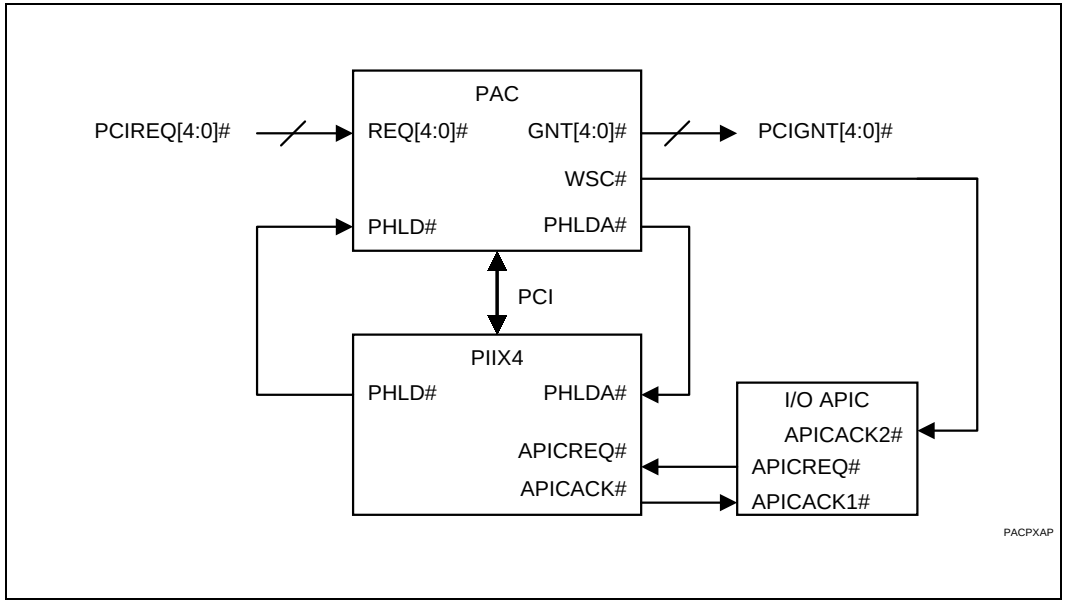


Figure 12. PAC and PIIX4 with an I/O APIC

4.8. System Clocking and Reset

4.8.1. HOST FREQUENCY SUPPORT

The Pentium II processor uses a clock ratio scheme where the host bus clock frequency is multiplied by a ratio to produce the processor's core frequency. PAC supports a host bus frequency of 66 MHz. The external synthesizer is responsible for generating the host clock. The Pentium II processor samples four signals: LINT[1:0], (INTR, NMI), IGNNE#, and A20M# on the inactive to active edge of RESET to set the ratio.

4.8.2. CLOCK GENERATION AND DISTRIBUTION

PAC receives two outputs of a clock synthesizer on the HCLKIN and PCLKIN pins. PAC uses these signals to clock internal logic and provide clocking control to PAC's interfaces.

The clock skew between two host clock outputs of the synthesizer must be less than 250 ps (@1.25V). The clock skew between two PCI clock outputs of the synthesizer must be less than 500 ps (@1.5V). In addition, the host clocks should always lead the PCI clocks by a minimum of 1 ns and a maximum of 4 ns. PAC requires a 45%/55% maximum output duty cycle. A maximum of 250 ps jitter must be maintained on the host clocks going from cycle to cycle.

PAC does not support stopping of the HCLKIN or PCLKIN clock signals during operation. If either clock is stopped, the PAC must be reset to ensure proper operation.

4.8.3. SYSTEM RESET

There are two types of system reset. A “hard” reset causes the entire system to reset and is initiated by the PIIX4. A hard reset can be initiated by either PWROK being asserted (from the power supply/reset button) or by writing to the PIIX4 (I/O address CF9h). A “soft” reset only resets the CPU.

A soft reset can be initiated by either PAC or the PIIX4. There are several ways to initiate a soft reset. PIIX4 can initiate a soft reset via a write to the PIIX4 Reset Control Register or an I/O write to port 92h. Additionally, the PIIX4 initiates a soft reset when RCIN# is asserted from the keyboard controller. PAC initiates a soft reset when the RCPU bit is written. Both the PIIX4 and PAC initiate soft reset via the INIT signal to the processor. Thus, the INIT signal from the PIIX4 should be tied to the INIT signal from PAC and routed to the CPU(s).

4.8.4. PAC RESET STRUCTURE

The system reset structure is shown in Figure 13.

4.8.5. HARD RESET

Hard Reset is defined as a reset where all the components in the entire system are reset. There are two sources of hard reset in the system:

- During Power-up, PWROK asserted (typically by the power supply) 1 ms after the system power has stabilized.
- I/O write to the PIIX4 Reset Control register (I/O address CF9h).

PIIX4 generates a hard reset for the system when the PWROK signal is sampled inactive (low). PIIX4 generates PCIRST# for both the A.G.P. and PCI bus. PAC uses the PCIRST# input connected to the RSTIN# pin to generate CPURST# (for the Pentium II processor(s)), and CRESET# (to the frequency control logic and I/OAPIC). PAC asserts CPURST# and CRESET# when RSTIN# is sampled low, and continues assert CPURST# for 1 msec, and CRESET# for 1 msec plus 2 HCLKINs, after the rising edge of the RSTIN# signal. The assertion of CPURST# must be synchronous to the HCLKIN.

PIIX4 can be programmed to generate a hard reset through the Reset Control register (I/O Address CF9h). PIIX4 drives PCIRST# low for 1 msec and the reset continues as described above.

PAC configuration straps on the ECCERR#, MECC[0] and CKE pins are sampled on the rising edge of RSTIN#.

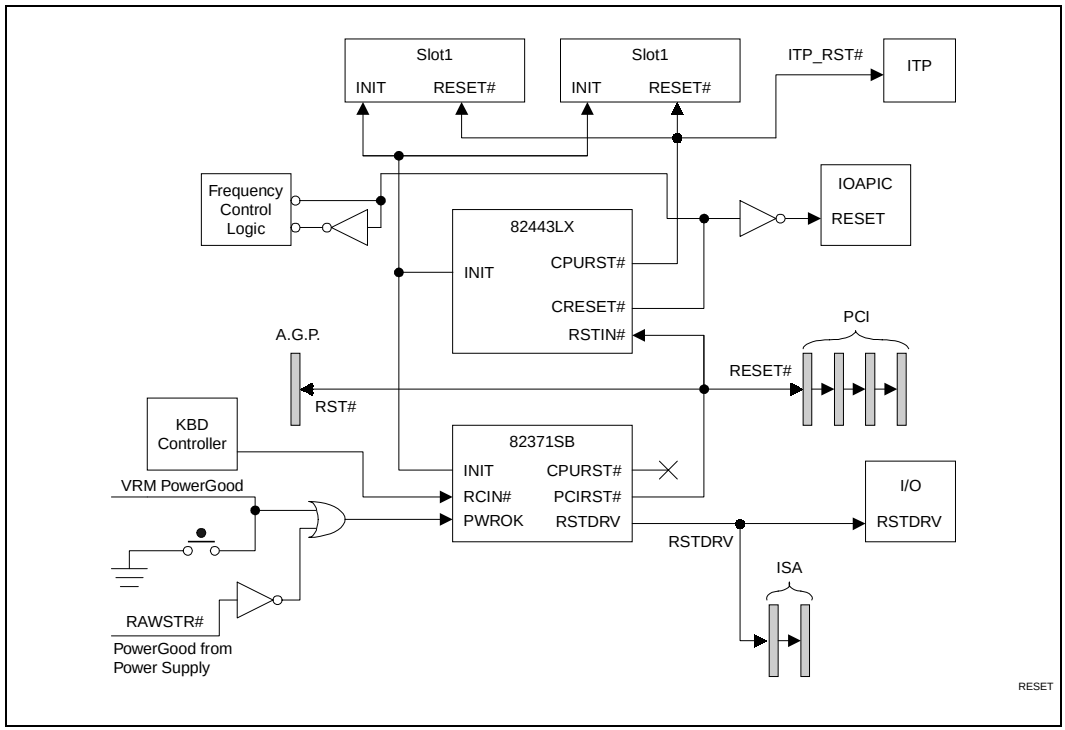


Figure 13. Reset Structure for 440LX AGPset with PIIX4

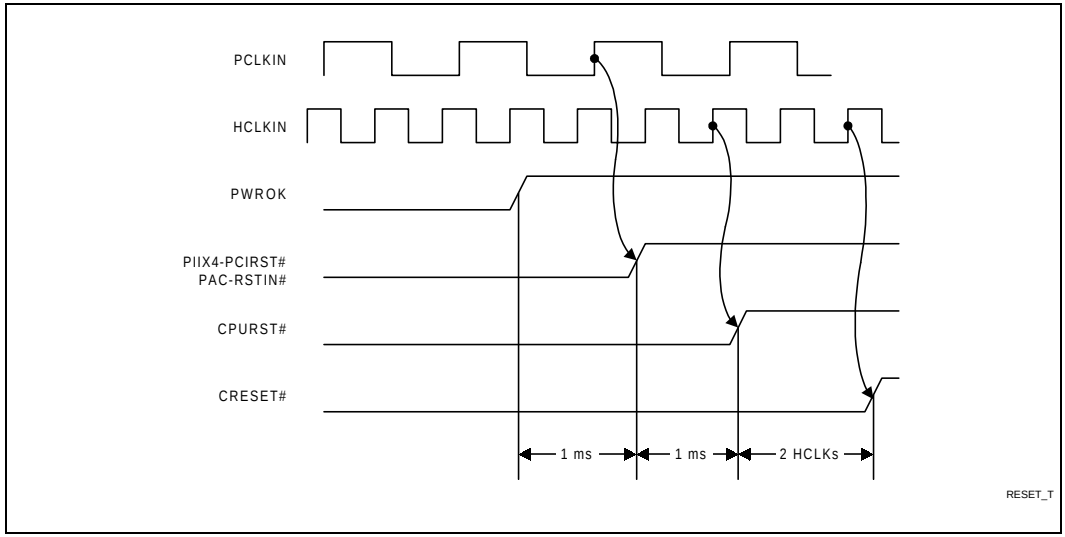


Figure 14. PAC Hard Reset Timing

4.8.6. SOFT RESET

A soft reset is defined as only resetting the CPU (no other devices in the system are reset). There are five sources of soft reset in the system:

- CPU shutdown bus cycle
- I/O write to the PAC Reset Control Register (offset 93h)
- I/O write to the keyboard controller
- I/O write to the PIIX4 port 92h
- I/O write to the PIIX4 Reset Control Register (I/O address CF9h)

When PAC detects a CPU shutdown bus cycle, it terminates the Host bus cycle with a TDRY#, with a no data response type as defined in the Pentium II processor datasheet. PAC then asserts the INIT# output for a minimum of 4 host clocks.

PAC can be programmed to generate a soft reset through the Reset Control Register (configuration offset 93h). PAC asserts INIT# for a minimum of 4 host clocks if bit 3=0, bit 1=1 and bit 2 is written from a 0 to a 1. A soft reset from the keyboard controller will be signaled into the PIIX4 through the RCIN# signal on the PIIX4 The PIIX4 will then generate the INIT signal active. A write to I/O port 92h, bit 0, also causes PIIX4 to assert INIT. A write to the PIIX4 Reset Control Register also causes PIIX4 to assert INIT.

The system combines PAC INIT# output with the PIIX4 INIT output as shown above to generate the INIT# signal for the CPU(s).

4.8.7. CPU BIST

PAC can be programmed to activate BIST mode of the CPU through the Reset Control Register (configuration offset 93h). If PAC activates the CPU's BIST function, a hard reset must then be initiated (after BIST completion). The BIST mode sets the IOQ depth of the processor and PAC to 1. This is not a valid operating condition for PAC.

5.0. ELECTRICAL CHARACTERISTICS

This chapter contains the electrical and thermal specifications for the 82443LX PCI AGP Compliant Controller (PAC). The specifications include: absolute maximum ratings, thermal characterhistics, DC characteristics, AC characteristics, and timing waveforms.

The Pentium® II processor bus introduces a variation of the low voltage GTL (Gunning Transceiver Logic) for signaling. For reliable operation, unused input pins must be tied to an appropriate signal level. Unused GTL+ inputs should be connected to VTT. Unused active low 3.3V tolerant inputs should be connected to 3.3V. Unused active high inputs should be connected to ground (VSS).

5.1. Absolute Maximum Ratings

Case Temperature under Bias ..... $0^{o}C$ to $+100^{o}C$
Storage Temperature ..... $-55^{o}C$ to $+150^{o}C$
Voltage on GTL+ & 3.3V tolerant Pins with Respect to Ground[2] ..... -0.3 to VCC + 0.3 V
Voltage on PCI and 5.0V tolerant Pins with Respect to Ground ..... -0.3 to VCC_{PCI}[1] + 0.3 V
3.3V Supply Voltage with Respect to Vss (VCC) ..... -0.3 to + 4.3 V
5.0V Supply Voltage with Respect to Vss (5V_BIAS) ..... -0.5 to + 6.5 V

[1] VCC_{PCI} and VCC_{AGP} are the voltage levels on the PCI bus and AGP interface respectively. To ensure long term reliability of the device, worst case AC operating conditions would include supporting an overvoltage of +11.0V and undervoltage of -5.5V

[2] Minimum D.C. input is -0.3V. During transitions the inputs may undershoot to -0.8V or overshoot to 0.8V over max VIH for a maximum period of 20 ns.

WARNING: Stressing the device beyond the "Absolute Maximum Ratings" may cause permanent damage. These are stress ratings only. Operating beyond the "Operating Conditions" is not recommended and extended exposure beyond "Operating Conditions" may affect reliability.

5.2. Power Characteristics

Table 19. Power Characteristics

Functional Operating Range (V_{TT} = 1.5V ± 10%, Vcc = 3.3V ±5%; T_{CASE} = 0°C to +100°C)

Symbol	Parameter	Min	Max	Unit	Notes
P_{LX}	Thermal Power Dissipation for 82443LX		3.0	W	Note 1, @ 66 MHz/ 33MHz
I_{LEAK}	5.0V to 3.3V Power Supply Leakage Current		20	uA	Note 2
I_{DDQ}	Quiescent Power Supply Current for 82443LX		30	mA	Note 3, @ 0 MHz/0 MHz
I_{CC-LX}	Power Supply Current for 82443LX		1300	mA	Note 4, @ 66 MHz/33 MHz

NOTES:

1. This specification is a combination of core power (I_{cc}) and power dissipated in the GTL+ outputs and I/O.
2. This parameter is specified at V_{cc5} (5V_BIAS) - $V_{cc3} \leq 2.25V$. In addition, to insure a proper power sequencing and protect the PAC internal circuitry, a 1 KΩ series resistor is recommended on the REV5V pin of PAC to 5V power source, and Zener diode is also recommended between 5V and 3.3V power source.
3. This is the maximum supply current consumption when all interfaces are idle and the clock inputs are turned off, typically with HCLKIN/PCLKIN running at 66/33 MHz the I_{DDQ} is 300mA
4. The I_{cc} specification does not include the GTL+ output current to ground Signal Groups

5.3. Signal Groupings

To ease discussion of the AC and DC characteristics, signals on the 440LX have been combined into groups of similar characteristics. These will be referred to in all subsequent discussion. Memory interface signals: **RCSA[7:6]#/MAB[3:2]#, RCSB[7:0]#/MAB[13:6]#, SRAS[3]#/MAB[5]#, SCAS[3]#/MAB[4]#** are dual function signals. These signals will have difference functions depending upon the selection of *Configuration #1 Mode* or *Configuration #2 Mode*.

Signal functionality in each configuration below is in **BOLD** type.

Configuration #1: RCSA[7:6]#/MAB[3:2]#, **RCSB[7:0]#**/MAB[13:6]#, **SRAS[3]#**/MAB[5]#, **SCAS[3]#**/MAB[4]#

Configuration #2: RCSA[7:6]#/**MAB[3:2]#,** RCSB[7:0]#/**MAB[13:6]#,** SRAS[3]#/**MAB[5]#,** SCAS[3]#/**MAB[4]#**

The following notations are used to describe the types of buffers used in Table 20:

GTL+ Open Drain GTL+ interface signal. Refer to the GTL+ I/O Specification for complete details

PCI PCI bus interface signals. These signals are compliant with the PCI 5.0V Signaling Environment DC and AC Specifications

A.G.P. A.G.P. interface signals. These signals are compatible with A.G.P. Signaling Environment DC and AC Specifications

LVTTL Low Voltage TTL compatible signals. These are also 3.3V inputs and outputs.

Table 20. Signal Groups

Signal Group	Signal Type	Signals
(a)	GTL+ I/O	A[31:3]#, HD[63:0]#, ADS#, BNR#, DBSY#, DRDY#, HIT#, HITM#, HREQ[4:0]#, HTRDY#, RS[2:0]#,
(b)	GTL+ Output	CPURST#, BPRI#, DEFER#, BREQ0#
(c)	GTL+ Input	HLOCK#
(d)	LVTTL Input	PCLKIN
(e)	LVTTL(2.5V) Input	HCLKIN
(f)	LVTTL Output	RCSA[5:0]#, CDQA[7:0]#, CDQB[1]#, CDQB[5]#, SRAS[2:0]#, SCAS[2:0]#, MAA[13:0], MAB[1:0], WE[3:0]#, CRESET#, INIT#
(g)	LVTTL Output **Memory Configuration #1**	RCSA[7:6]#/MAB[3:2]#, RCSB[7:0]#/MAB[13:6]#, SRAS[3]#/MAB[5]#, SCAS[3]#/MAB[4]#
(h)	LVTTL Output **Memory Configuration #2**	RCSA[7:6]#/MAB[3:2]#, RCSB[7:0]#/MAB[13:6]#, SRAS[3]#/MAB[5]#, SCAS[3]#/MAB[4]#
(i)	LVTTL I/O	MD[63:0], MECC[7:0], CKE
(j)	PCI Output	(8mA)(PIIX 3 compatibility??)PHLDA#, WSC#, GNT[4:0]#
(k)	PCI I/O 5.0V tolerant	AD[31:0], DEVSEL#, FRAME#, IRDY#, C/BE[3:0]#, PAR, PERR#, PLOCK#, TRDY#, STOP#, SERR#
(l)	PCI Input 5.0V tolerant	PHLD#, REQ[4:0]#
(m)	GTL Reference	GTL_REFV
(s)	A.G.P. Reference	VREFAGP
(n)	A.G.P. Input	PIPE#, SBA[7:0], SBSTB, GREQ#, RBF#, GSERR#
(o)	A.G.P. Output	ST[2:0], , GGNT#
(p)	A.G.P. I/O	GAD[31:0], GDEVSEL#, GFRAME#, GIRDY#, GTRDY#, GC/BE[3:0]#, GPAR, GPERR#, GSTOP#, ADSTB-A, ADSTB-B
(q)	TTL Input	RSTIN#, TESTIN#
(r)	TTL Output	ECCERR#

5.4. D.C. Characteristics

Table 21. D.C. Characteristics

Functional Operating Range (V_{TT} = 1.5V ± 10%, Vcc = 3.3V ±5%; T_{CASE} = 0°C to +100°C)

Symbol	Signal Group	Parameter	Min	Max	Unit	Notes
VIL1	(d),(i)	LVTTL Input Low Voltage	- 0.3	0.8	V	1
VIH1	(d),(i)	LVTTL Input High Voltage	2.0	Vcc + 0.3	V	2
VIL2	(k),(l)	PCI Input Low Voltage	-0.3	0.8	V	1
VIH2	(k),(l)	PCI Input High Voltage	2.0	Vcc + 0.3	V	2
VIL3	(a),(c)	GTL+ Input Low Voltage	-0.3	V_{REF} - 0.2	V	1
VIH3	(a),(c)	GTL+ Input High Voltage	V_{REF} + 0.2	1.8	V	2
VIL4	(p),(n)	A.G.P. Input Low Voltage	-0.5	$0.3V_{CC}$	V	
VIH4	(p),(n)	A.G.P. Input High Voltage	$0.5V_{CC}$	V_{CC} + 0.5	V	
VIL5	(q)	TTL Input Low Voltage	-0.3	0.8	V	1
VIH5	(q)	TTL Input High Voltage	2.0	Vcc + 0.3	V	2
VIL6	(e)	2.5V LVTTL Input Low Voltage	-0.3	0.7	V	3
VIH6	(e)	2.5V LVTTL Input High Voltage	1.7	2.625	V	3
VREFAGP	(s)	A.G.P. Reference Voltage			V	4
VREF	(m)	GTL+ Reference Voltage	$2/3V_{TT}$ - 2%	$2/3V_{TT}$ + 2%	V	5
VOL1	(f)(g)(h)(i)	LVTTL Output Low Voltage		0.4	V	
VOH1	(f)(g)(h)(i)	LVTTL Output High Voltage	2.4		V	
VOL2	(j),(k)	PCI Output Low Voltage		0.4	V	
VOH2	(j),(k)	PCI Output High Voltage	2.4		V	
VOL3	(a),(b)	GTL+ Output Low Voltage		0.55	V	
VOH4	(o),(p)	A.G.P. Output Low Voltage		$0.1V_{CC}$	V	
VOH4	(o),(p)	A.G.P. Output High Voltage	$0.9V_{CC}$		V	
VOL5	(r)	TTL Output Low Voltage		0.4	V	
VOH5	(r)	TTL Output High Voltage	2.4		V	
IOL1	(f)(g)(h)(i)	LVTTL Output Low Current		3	mA	
IOH1	(f)(g)(h)(i)	LVTTL Output High Current	-2		mA	
IOL2	(j),(k)	PCI Output Low Current		3	mA	

Table 21. D.C. Characteristics

Functional Operating Range (V_{TT} = 1.5V ± 10%, Vcc = 3.3V ±5%; T_{CASE} = 0°C to +100°C)

Symbol	Signal Group	Parameter	Min	Max	Unit	Notes
IOH2	(j),(k)	PCI Output High Current	-2		mA	
IOL3	(o),(p)	A.G.P. Output Low Current		1.5	mA	
IOH3	(o),(p)	A.G.P. Output High Current	-0.5		mA	
IOL4	(a),(b)	GTL+ Output Low Current	32	36	mA	
IOL5	(r)	TTL Output Low Current		3	mA	
IOH5	(r)	TTL Output High Current	-2		mA	
IIH1	(a),(c),(d),(e),(i),(k),(l),(q)	Input Leakage Current		+ 10	uA	
IIL1	(a),(c),(d),(e),(i),(k),(l),(q)	Input Leakage Current		- 10	uA	
IIH2	(n),(p)	A.G.P. Input Leakage Current		70	uA	V_{IN} = 2.7v
IIL2	(n),(p)	A.G.P. Input Leakage Current		+/- 10	uA	$0 < V_{IN} < V_{CC}$
ILO1	(a)(b)	GTL+ Output Leakage Current		±15	uA	6
ILO2	(f),(g),(h),(i),(j),(k),(o),(p)(r)	Non-GTL+ Output Leakage Current		±15	uA	6
CIN COUT	(n),(p),(k),(l),(i),(a),(c)	A.G.P. Input Capacitance PCI Input Capacitance DRAM Input Capacitance GTL+ Input Capacitance		5 to 8 6 to 9 5 to 8 5 to 8	pF	F_C = 1 MHz

NOTES:

1. Minimum D.C. input is -0.3V. During transitions the inputs may undershoot to -0.8V for a maximum period of 20ns.
2. During transitions, the inputs may overshoot to 0.8V over max VIH for a maximum period of 20ns.
3. This applies to the 2.5V of HCLK IN pin
4. VREFAGP = 0.4V of Vcc,
5. VREF ranges from 0.9V to 1.1V in the system with the part installed. The system board without the part installed must guarantee a maximum of ±2% deviation
6. ($0 \leq Vout \leq 3.3V +5\%$)

5.5. AC Characteristics

All the clock-to-output values are specified into 0 pF load, unless otherwise specified.

Table 22. HOST CLOCK TIMING, 66 MHz

Functional Operating Range (V_{TT} = 1.5V ± 10%, Vcc = 3.3V ±5%; T_{CASE} = 0°C to +100°C)

Symbol	Parameter	Min	Max	Units	Figure
t1	HCLKIN Period	15.0	20.0	ns	15
t2	HCLKIN Period Stability		± 250	ps	
t3	HCLKIN High Time	5.3		ns	15
t4	HCLKIN Low Time	5.0		ns	15
t5	HCLKIN Rise Time	0.4	1.6	ns	15
t6	HCLKIN Fall Time	0.4	1.6	ns	15

Table 23. CPU INTERFACE TIMING, 66 MHz

Functional Operating Range (V_{TT} = 1.5V ± 10%, Vcc = 3.3V ±5%; T_{CASE} = 0°C to +100°C)

Symbol	Parameter	Min	Max	Units	Figures
t7	Valid Delay from HCLKIN Rising (tco)	1.25	7.25	ns	17
t8	Input Setup Time to HCLKIN Rising (tsu)	5.0		ns	18
t9	Input Hold Time from HCLKIN Rising (thld)	0.0		ns	18

Table 24. DRAM INTERFACE TIMING, 66 MHz (Configuration #1)

Functional Operating Range (V_{TT} = 1.5V ± 10%, Vcc = 3.3V ±5%; T_{CASE} = 0°C to +100°C)

Symbol	Parameter	Min	Max	Units	Figure	Notes
t10	WE# Valid Delay from HCLKIN Rising	1.5	7.0	ns	17	0 pF
t11	MAA[13:2]#, MAB[1:0]# Valid Delay from HCLKIN Rising, SDRAM Read/Write cycles	1.5	7.0	ns	17	0 pF
t12	SRAS[2:0]#, SRAS[3]#/MAB[5] Valid Delay from HCLKIN Rising	1.5	7.0	ns	17	0 pF
t13	SCAS[2:0]#, SCAS[3]#/MAB[4] Valid Delay from HCLKIN Rising	1.5	7.0	ns	17	0 pF
t14	RCSA[5:0]#, RCSA[7:6]#/MAB[3:2], RCSB[7:0]#/MAB[13:6] Valid Delay from HCLKIN Rising	1.5	7.0	ns	17	0 pF
t15	CDQA[7:0]#, CDQB[1]#, CDQB[5]# Valid Delay from HCLKIN Rising	1.5	6.5	ns	17	0 pF
t16	MD[63:0], MECC[7:0] Valid Delay from HCLKIN Rising	1.0	6.0	ns	17	0 pF
t17	MD[63:0], MECC[7:0] Setup Time to HCLKIN Rising	1.0		ns	18	note1
t18	MD[63:0], MECC[7:0] Hold Time from HCLKIN Rising	2.0		ns	18	note1
t19	CKE Valid Delay from HCLKIN Rising	1.5	7.0	ns	17	0 pF

Table 25. DRAM INTERFACE TIMING, 66 MHz (Configuration #2)

Functional Operating Range (V_{TT} = 1.5V ± 10%, Vcc = 3.3V ±5%; T_{CASE} = 0°C to +100°C)

Symbol	Parameter	Min	Max	Units	Figure	Notes
t20	WE# Valid Delay from HCLKIN Rising	1.5	7.0	ns	17	0 pF
t21	MAA[13:0]#, MAB[13:0]# Valid Delay from HCLKIN Rising, SDRAM Read/Write cycles	1.5	7.0	ns	17	0 pF
t22	SRAS[2:0]#, SRAS[3]#/MAB[5] Valid Delay from HCLKIN Rising	1.5	7.0	ns	17	0 pF
t23	SCAS[2:0]#, SCAS[3]#/MAB[4] Valid Delay from HCLKIN Rising	1.5	7.0	ns	17v	0 pF
t24	RCSA[5:0]#, RCSA[7:6]#/MAB[3:2], RCSB[7:0]#/MAB[13:6] Valid Delay from HCLKIN Rising	1.5	7.0	ns	17	0 pF
t25	CDQA[7:0]#, CDQB[1]#, CDQB[5]# Valid Delay from HCLKIN Rising	1.5	6.5	ns	17	0 pF
t26	MD[63:0], MECC[7:0] Valid Delay from HCLKIN Rising	1.0	6.0	ns	17	0 pF
t27	MD[63:0], MECC[7:0] Setup Time to HCLKIN Rising	1.0		ns	18	note1
t28	MD[63:0], MECC[7:0] Hold Time from HCLKIN Rising	2.0		ns	18	note1
t29	CKE Valid Delay from HCLKIN Rising	1.5	7.0	ns	17	0 pF

NOTES:

1. When EDO is driving, this specification is based on a 100pF load. When SDRAM is driving, this specication is based on a 50pF load.

Table 26. PCI CLOCK TIMING, 33 MHz

Functional Operating Range (VTT = 1.5V ± 10%, Vcc = 3.3V ± 5%; TCASE = 0°C to +100°C)

Symbol	Parameter	Min	Max	Units	Figure	Notes
t30	PCLKIN Period	30		ns	16	
t31	PCLKIN Period Stability		500	ns		ps
t32	PCLKIN High Time	12.0		ns	16	
t33	PCLKIN Low Time	12.0		ns	16	
t34	HCLKIN Lead Time to PCLKIN	1	6	ns		
t35	PCLKIN Rise Time		3.0	ns	16	
t36	PCLKIN Fall Time		3.0	ns	16	

Table 27. PCI INTERFACE TIMING, 33 MHz

Functional Operating Range (VTT = 1.5V ± 10%, Vcc = 3.3V ± 5%; TCASE = 0°C to +100°C)

Symbol	Parameter	Min	Max	Units	Figures	Notes
t37	AD[31:0] Valid Delay from PCLKIN Rising	2	11	ns	17	Min: 0 pF Max: 50 pF
t38	AD[31:0] Setup Time to PCLKIN Rising	7		ns	18	
t39	AD[31:0] Hold Time from PCLKIN	0		ns	18	
t40	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, PERR# Valid Delay from PCLKIN Rising	2	11	ns	17	Min: 0 pF Max: 50 pF
t41	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, PERR# Output Enable Delay from PCLKIN Rising	2		ns		
t42	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, PERR# Float Delay from PCLKIN Rising	2	28	ns	19	
t43	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, PERR# Setup Time to PCLKIN Rising	7		ns	18	
t44	C/BE[3:0]#, FRAME#, TRDY#, IRDY#, STOP#, PLOCK#, PAR, DEVSEL#, SERR#, PERR# Hold Time from PCLKIN Rising	0		ns	18	
t45	PHLDA# Valid Delay from PCLKIN Rising	2	12	ns	17	Min: 0 pF Max: 50 pF
t46	WSC# Valid Delay from PCLKIN Rising	2	12	ns	17	Min: 0 pF Max: 50 pF
t47	PHOLD# Setup Time to PCLKIN Rising	12		ns	18	
t48	PHOLD# Hold Time from PCLKIN Rising	0		ns	18	
t49	GNT[3:1]#, GNT0# Valid Delay from PCLKIN Rising	2	12	ns	17	Min: 0 pF Max: 50 pF
t50	REQ[3:1]#,REQ4#, REQ0# Setup Time to PCLKIN Rising	12		ns	18	
t51	REQ[3:1]# ,REQ4#, REQ0# Hold Time from PCLKIN Rising	0		ns	18	

Table 28. A.G.P. INTERFACE TIMING, 66/133 MHz

Symbol	**Parameter**	**Min**	**Max**	**Units**	**Figures**	**Notes**
t52	GAD[31:0],GCBE#[3:0], SBA[7:0] Valid Delay from HCLKIN Rising	1.0	6.0	ns	17	10pF
t53	GAD[31:0],GCBE#[3:0], SBA[7:0] Setup Time to HCLKIN Rising	5.5		ns	18	10pF
t54	GAD[31:0],GCBE#[3:0], SBA[7:0] Hold Time from HCLKIN	0		ns	18	10pF
t55	GFRAME#, GTRDY#, GIRDY#, GSTOP#, GPAR, GDEVSEL#, GPERR#, GSERR#, PIPE#, DBF#, GREQ#, GGNT#, ST[2:0] Valid Delay from HCLKIN Rising	1.0	5.5	ns	17	10pF
t56	GFRAME#, GTRDY#, GIRDY#, GSTOP#, GPAR, GDEVSEL#, GPERR#, GSERR#, PIPE#, DBF#, GREQ#, GGNT#, ST[2:0] Float Delay from HCLKIN Rising	1.0	14.0	ns	19	10pF
t57	GFRAME#, GTRDY#, GIRDY#, GSTOP#, GPAR, GDEVSEL#, GPERR#, GSERR#, PIPE#, DBF#, GREQ#, GGNT#, ST[2:0] Setup Time to HCLKIN Rising	6.0		ns	18	10pF
t58	GFRAME#, GTRDY#, GIRDY#, GSTOP#, GPAR, GDEVSEL#, GPERR#, GSERR#, PIPE#, DBF#, GREQ#, GGNT#, ST[2:0] Hold Time from HCLKIN Rising	0		ns	18	10pF

Table 29. A.G.P. INTERFACE TIMING,133 MHz

Functional Operating Range (VTT = 1.5V ± 10%, Vcc = 3.3V ± 5%; TCASE = 0°C to +100°C)

Symbol	Parameter	Min	Max	Untis	Figures	Notes
t59	ADSTBx falling Valid Delay at transmitter from HCLKIN rising.	2	12	ns	22	tTSf, note1,2, 3
t60	ADSTBx rising Valid Delay at transmitter from HCLKIN rising.		20	ns	22	tTSr
t61	GAD[31:0],GC/BE[3:0]# Valid Delay before ADSTBx Rise/Fall	1.7		ns	22	tDvb
t62	GAD[31:0] GC/BE[3:0]# Valid Delay after ADSTBx Rise/Fall	1.7		ns	22	tDva
t63	GAD[31:0] GC/BE[3:0]# Float to Active Delay from HCLKIN rising.	-1	9	ns	21	tOND
t64	GAD[31:0], GC/BE[3:0]# Active to Float Delay from HCLKIN rising.	1	12	ns	21	tOFFD
t65	ADSTBx rising Delay Time at transmitter to ADSTBx floating.	6	10	ns	21	tOFFS
t66	ADSTBx active Setup Time at transmitter to ADSTBx falling.	6	10	ns	21	tONS
t67	ADSTBx rising Setup Time at receiver to HCLKIN rising.	6		ns	22	tRSsu
t68	ADSTBx falling Hold Time at receiver to HCLKIN rising.	1		ns	22	tRSh
t69	GAD[31:0],GC/BE[3:0]# Setup Time to ADSTBx Rise/Fall	1		ns	22	tDsu
t70	GAD[31:0] GC/BE[3:0]# Hold Time from ADSTBx Rise/Fall	1		ns	22	tDh
t71	SBSTB rising Setup Time at receiver to HCLKIN rising.	6		ns	22	tRSsu
t72	SBSTB falling Hold Time at receiver to HCLKIN rising.	1		ns	22	tRSh
t73	SBA[7:0] Setup Time at receiver to SBSTB Rise/Fall	1		ns	22	tDsu
t74	SBA[7:0] Hold Time at receiver from SBSTB Rise/Fall	1		ns	22	tDh

NOTES:

1. ADSTBx refers to ADSTBA and ADSTBB.
3. Specifications are based on a 10pF loading.

Table 30. MISCELLANEOUS SIGNALS

Functional Operating Range (VTT = 1.5V ± 10%, Vcc = 3.3V ± 5%; TCASE = 0°C to +100°C)

Symbol	Parameter	Min	Max	Units	Figure	Notes
t75	CRESET# Valid Delay time from HLCKIN Rising	1.5	7	ns	17	0pF
t76	RSTIN# Setup time to PCICLK Rising	5		ns	18	0pF
t77	RSTIN# Hold time from PCICLK Rising	1		ns	18	0pF
t78	CPURST# Setup time to HCLKIN Rising	5		ns	18	0pF
t79	CPURST# Hold time from HCLKIN Rising	1		ns	18	0pF
t80	TEST# Setup time to HCLKIN Rising	5		ns	18	0pF
t81	TEST# Hold time from HCLKIN Rising	1		ns	18	0pF
t82	INIT# Low Pulse Width	16		ns	20	HCLKs
t83	ECCERR# Valid Delay time from HCLKIN Rising	2.1	10.0	ns	17	0pF

5.6. 82443LX Timing Diagrams

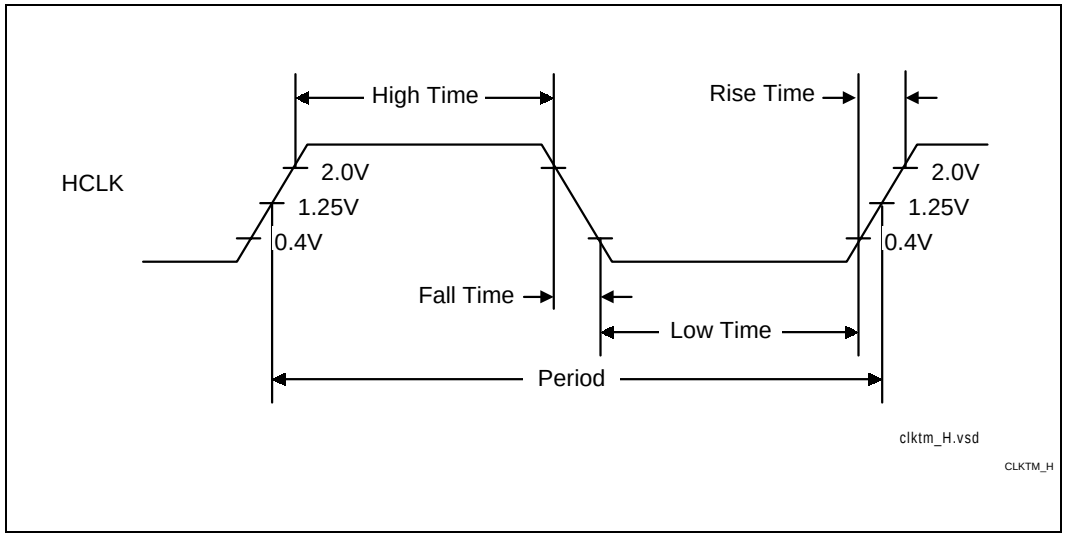


Figure 15. 2.5V Clocking Interface

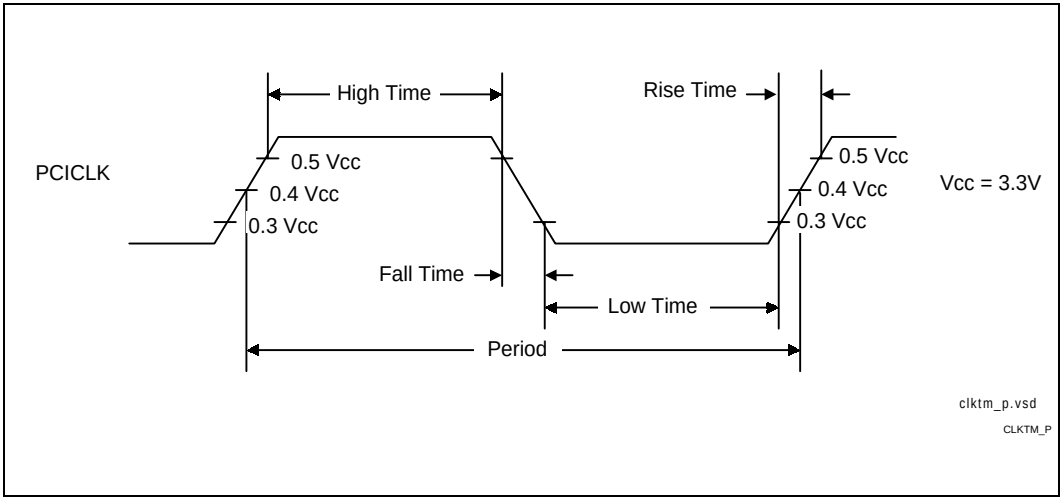
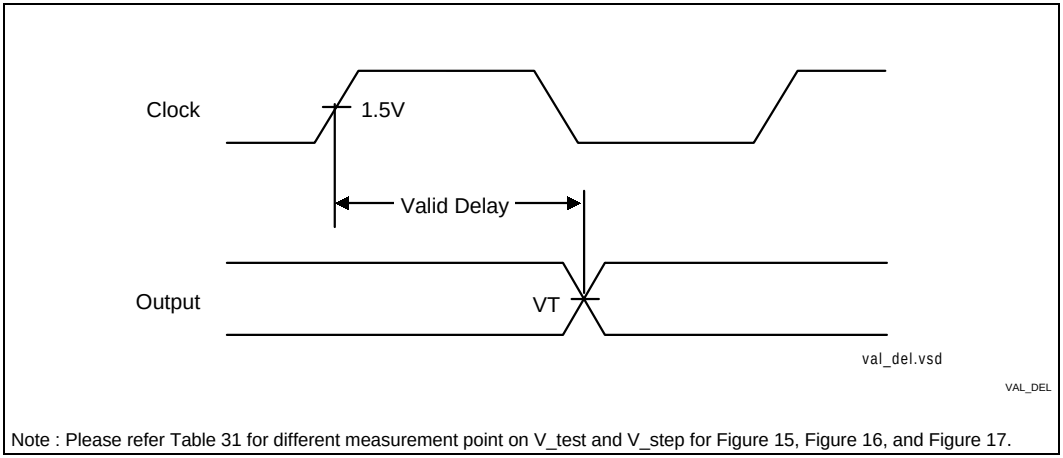


Figure 16. 3.3V Clocking Interface



Note : Please refer Table 31 for different measurement point on V_test and V_step for Figure 15, Figure 16, and Figure 17.

Figure 17. Valid Delay From Rising Clock Edge

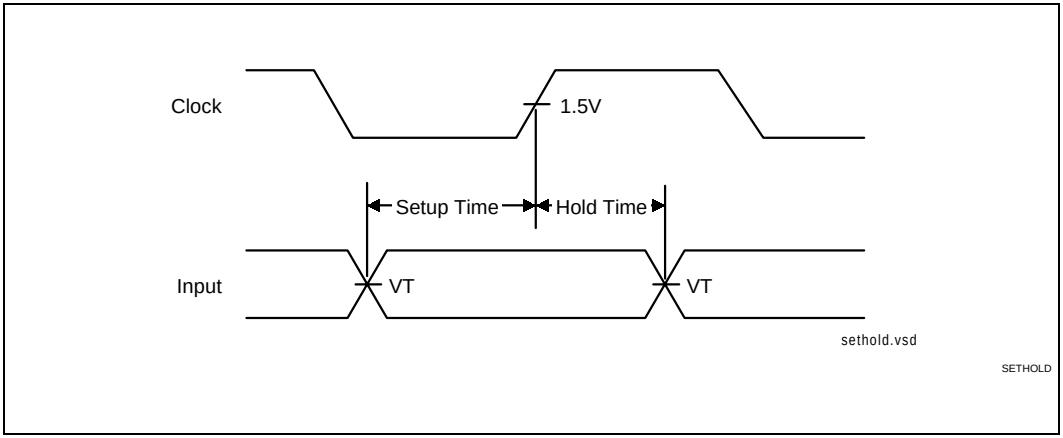


Figure 18. Setup and Hold Time to Clock

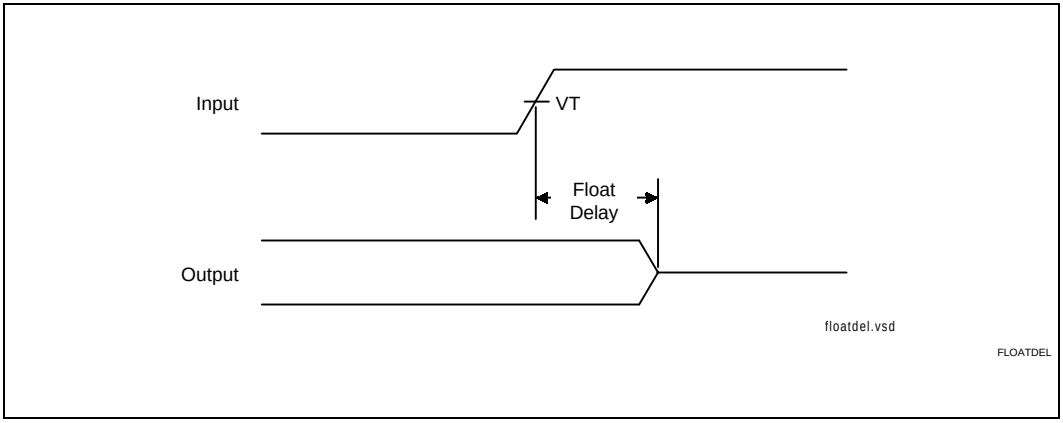


Figure 19. Float Delay

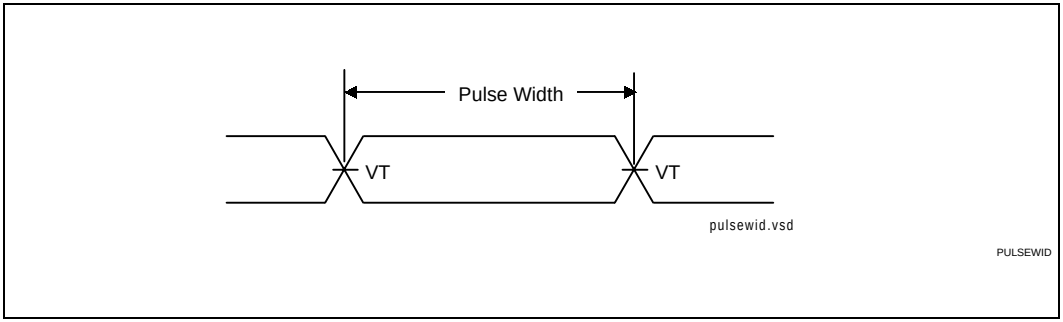


Figure 20. Pulse Width

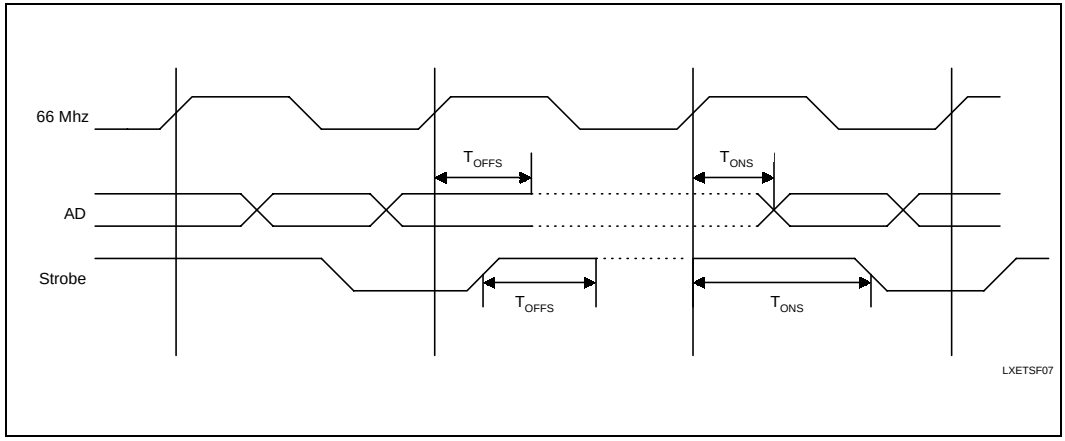


Figure 21. Strobe/Data Turnaround Timings

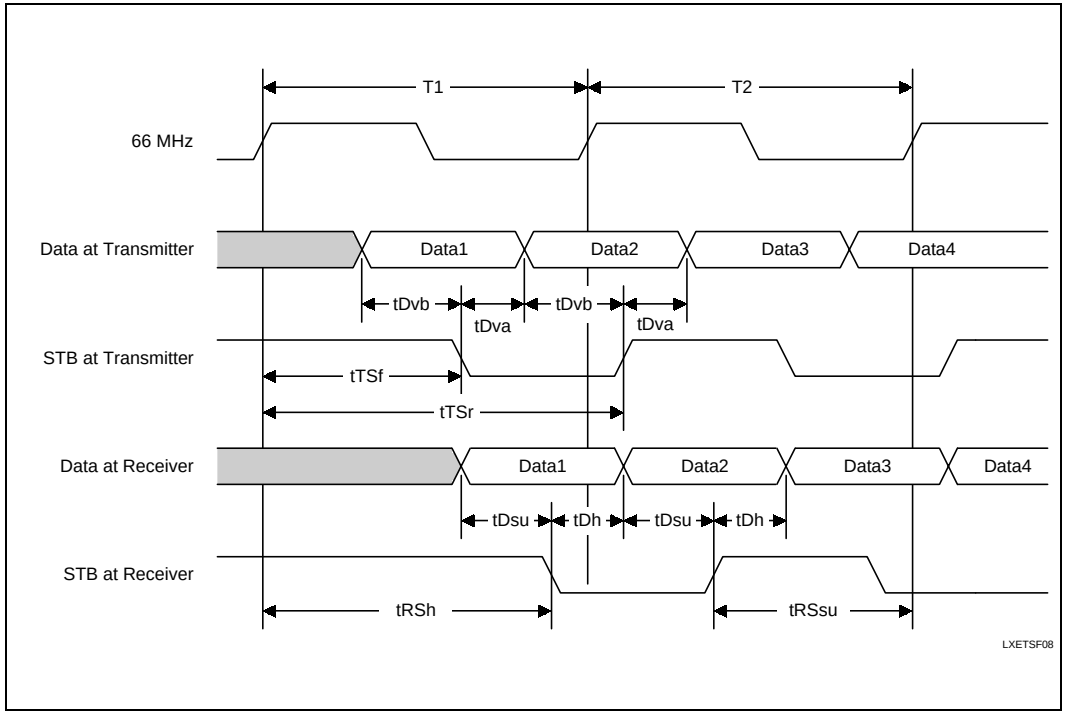


Figure 22. A.G.P. 133 Timing Diagram

Table 31. AC Timing Measurement Points

Clock	V_test	V_step	Notes
CPU interface HCLK (2.5V)	1.25V	1.0V for GTL+ signal group 1.25V for CMOS, APIC signals	
DRAM interface HCLK (2.5V)	1.25V	1.4V for SDRAM 1.5V for EDO	1
PCI interface PCICLK(3.3V)	1.5V	n/a	2
AGP device HCLK (2.5)	0.4Vcc	0.4Vcc	3

NOTES:

1. DRAM interface AC timing measurement is relative to 2.5V of HCLK, since the HCLK input to PAC is a 2.5V signal. The DRAM AC timing in Table 24 and Table 25 are valid for both SDRAM and EDO.
2. Although the PCICLK is a 3.3V clock, the PCI interface of PAC operates in a 5V PCI environment. Via PCI 2.1 spec, the V_test is1.5V.
3. Although the HCLK input of PAC is a 2.5V clock, the AGP interface of PAC operates in a 3.3V environment.

5.7. DRAM TIMING RELATIONSHIPS WITH REGISTER SETTINGS

This section shows the DRAM timing relationship with respect to bit settings in the DRAM Timing (DRAMT) register (address offset 58h). The values in this register affect both leadoff and burst timings. The CPU to DRAM memory read performance summary for EDO and SDRAM are shown in Table 32 and Table 33.

NOTE

1. PH is page hit.
2. RM is row miss.
3. PM is page miss.
4. The leadoff clock counts of a back-to-back burst cycle is also shown as a pipeline leadoff
5. All leadoff counts will add one more clock when ECC is enabled.

Table 32. EDO Timing Performance Summary

	Affect leadoff			Leadoff Clock Count		Burst Clock Count [4]	
Possible Valid Setting	**RCD [1] 1(2 clocks) 0(3 clocks)**	**MAWS [5] 1(fast) 0(slow)**	**RPT [6] 1(3 clocks) 0(4 clocks)**	**First Leadoff (PH/RM[2]/RM[3]/ PM)**	**Pipeline Leadoff (PH/RM[3]/PM)**	**Read**	**Write**
a	0	1	1	8/10/11/13	2/6/8	222 or 333	222 or 333
b	0	1	0	8/10/11/14	2/6/9	222 or 333	222 or 333
c	0	0	1	9/12/13/15	3/7/9	222 or 333	222 or 333
d	0	0	0	9/12/13/16	3/7/10	222 or 333	222 or 333

NOTES:

1. RAS to CAS delay, RCD (bit 1 of Register DRAMT), is always set to 0 for a 3 clock delay to have a positive tRAC margin.
2. Row miss numbers assume that no RAS# is currently active .
3. One more clock should be added if the current RAS# has to be negated and the new RAS# has to be asserted.
4. The EDO burst timing is also determined by the setting DRAMT bits [3,4].
5. MAWS is the EDO Memory Address Wait State. The setting of MAWS affects all cases. When MAWS is set to 0 (slow), an extra clock is added for each CAS# and RAS# assertion.
6. RPT is EDO RAS Precharge time. This only affects a page miss.

Table 33. SDRAM Timing Performance Summary

	Affects Leadoff			Leadoff Clock Count		Burst Clock Count
Possible Valid Setting	SCLT [1] 1(2 clocks) 0(3 clocks)	SRCD [2] 1(2 clocks) 0(3 clocks)	SRPT [3] 1(2 clocks) 0(3 clocks)	First Leadoff PH/RM[4]/RM[5]/ PM	Pipeline Leadoff PH/RM[5]/PM	Read & Write
a.	1	1	1	8/10/11/12	2/4/5	111
b	1	1	0	8/10/11/13	2/4/6	111
c	0	1	1	9/11/12/13	1/5/6	111
d	1	0	1	8/11/12/13	2/5/6	111
e	0	1	0	9/11/12/14	1/5/7	111
f	0	0	0	9/12/13/15	1/6/8	111
g	1	0	0	8/11/12/14	2/5/7	111
h	0	0	1	9/12/13/14	1/6/7	111

NOTES:

1. SCLT is SDRAM CAS Latency. The setting of SCLT affects all cases(page hit, page miss, and row miss).
2. SRCD is SDRAM RAS to CAS delay. The setting of this bit affects both page miss and row miss.
3. SRPT is SDRAM RAS precharge time. The setting of this bit affects only page miss.
4. Row miss numbers assume that no RAS# is currently active.
5. Row miss numbers assume that the current RAS# has to be negated and the new RAS# has to be asserted.
6. The same MAWS control bit for EDO timing in register 58h of PAC (device 0) has a different timing effect for SDRAM. All the clock counts are based on MAWS = 1 (fast). When MAWS = 0 (slow), an extra clock is added before each CS# assertion.

Following are the waveforms illustrating the page hit, page miss and row miss with different settings of SCLT, SRCD, SRPT, and MAWS=1.

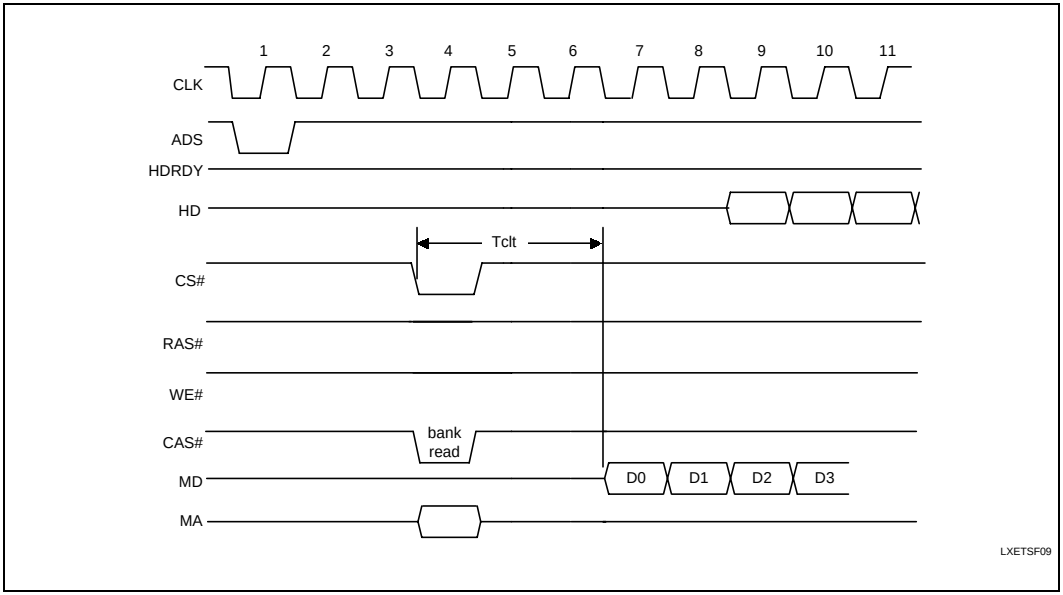


Figure 23. Page Hit with SCLT=0, SRCD=1, SRPT=1

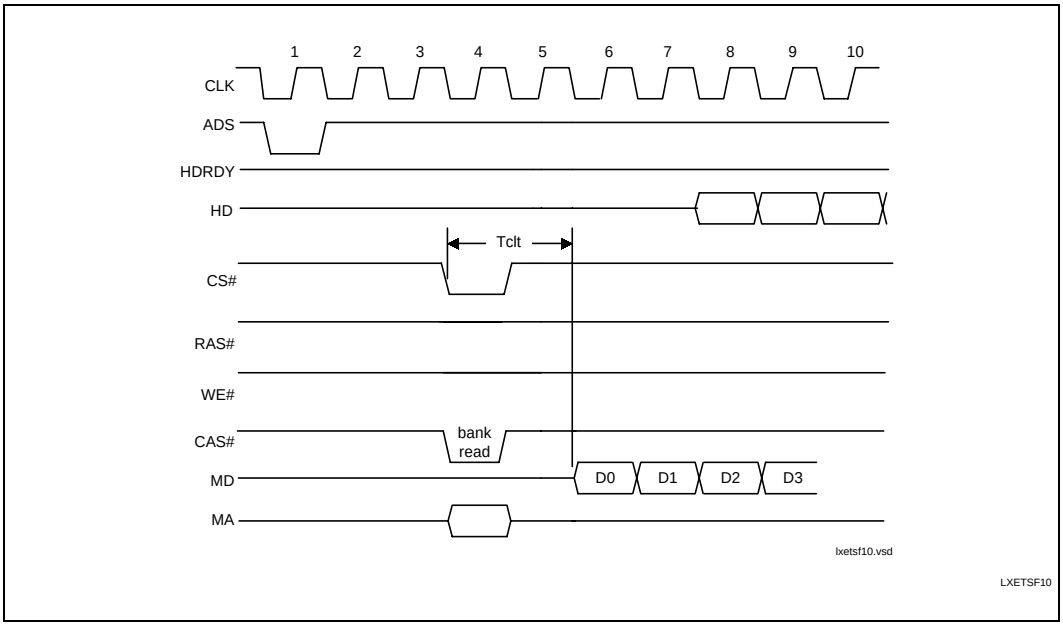


Figure 24. Page Hit with SCLT=1, SRCD=1, SRPT=1

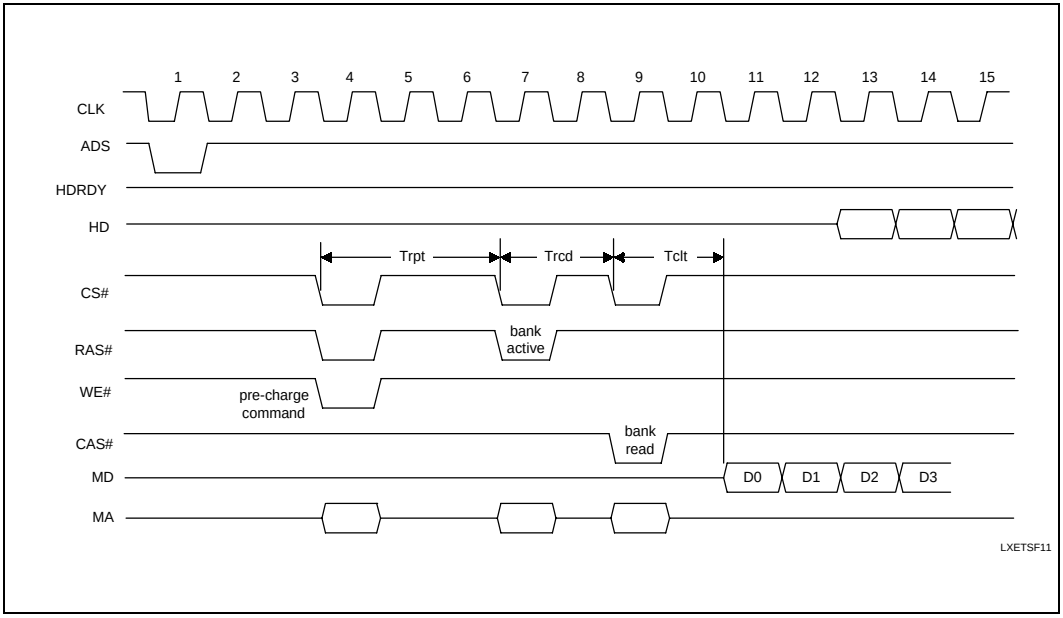


Figure 25. Page Miss with SCLT=1, SRCD=1, SRPT=0

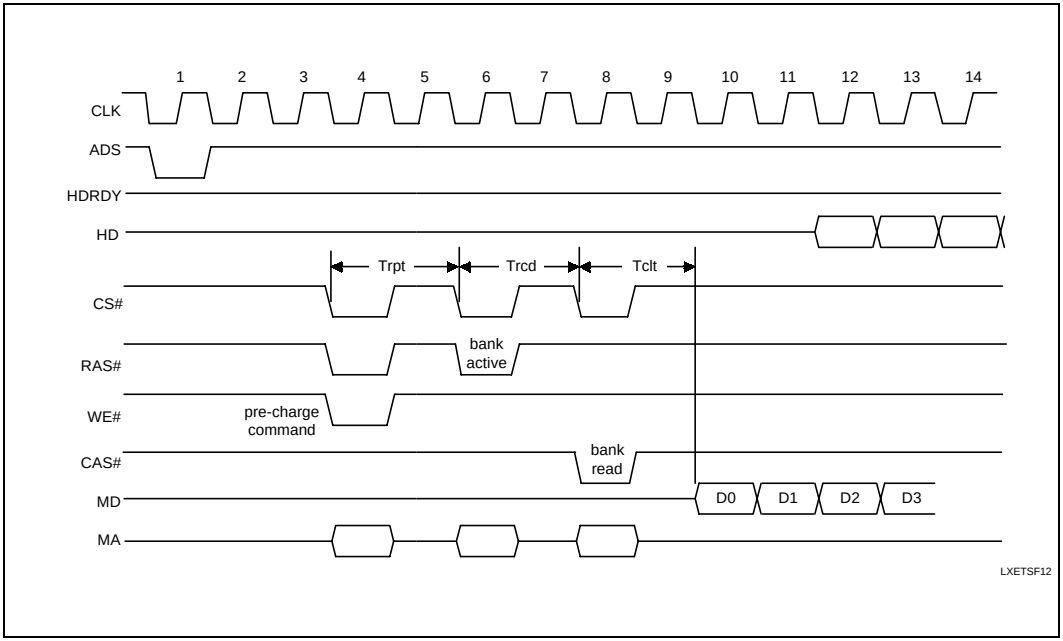


Figure 26. Page Miss with SCLT=1, SRCD=1, SRPT=1

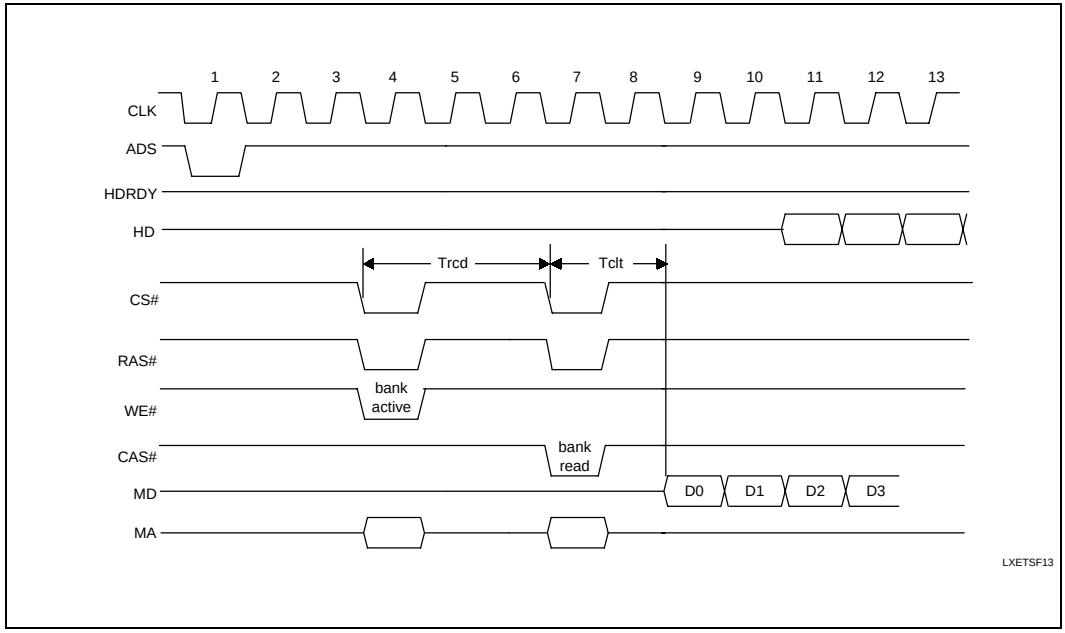


Figure 27. Row Miss-4 with SCLT=1, SRCD=0, SRPT=1

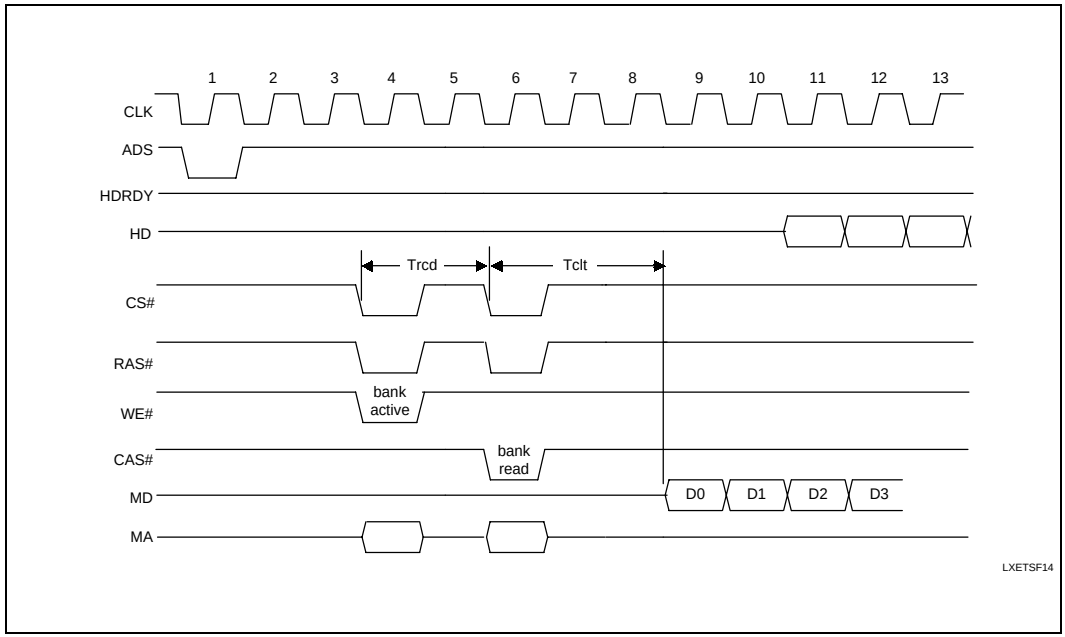


Figure 28. Row Miss-4 with SCLT=0, SRCD=1, SRPT=1

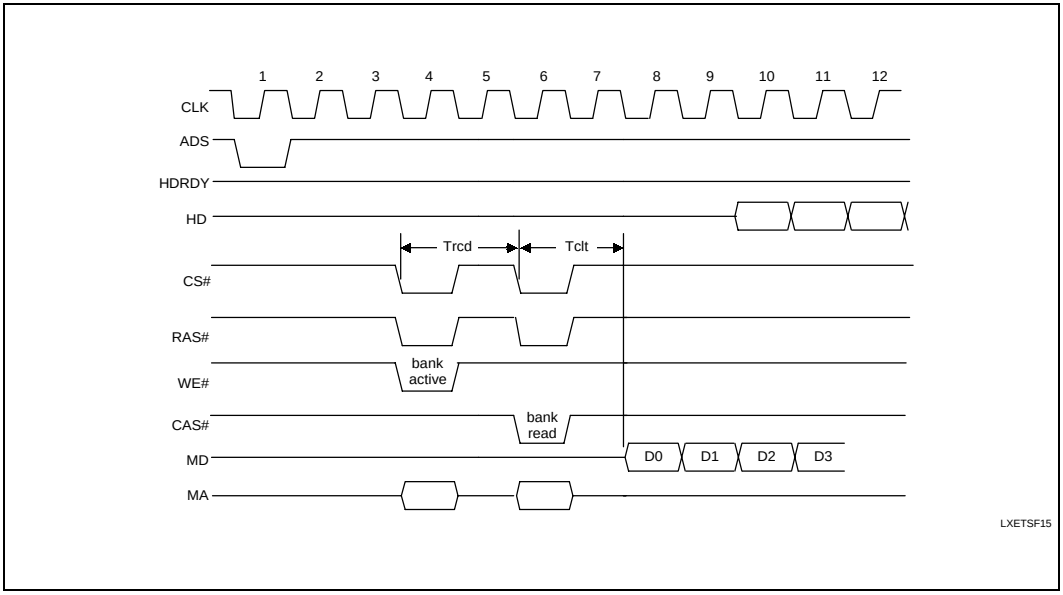


Figure 29. Row Miss-4 with SCLT=1, SRCD=1, SRPT=1

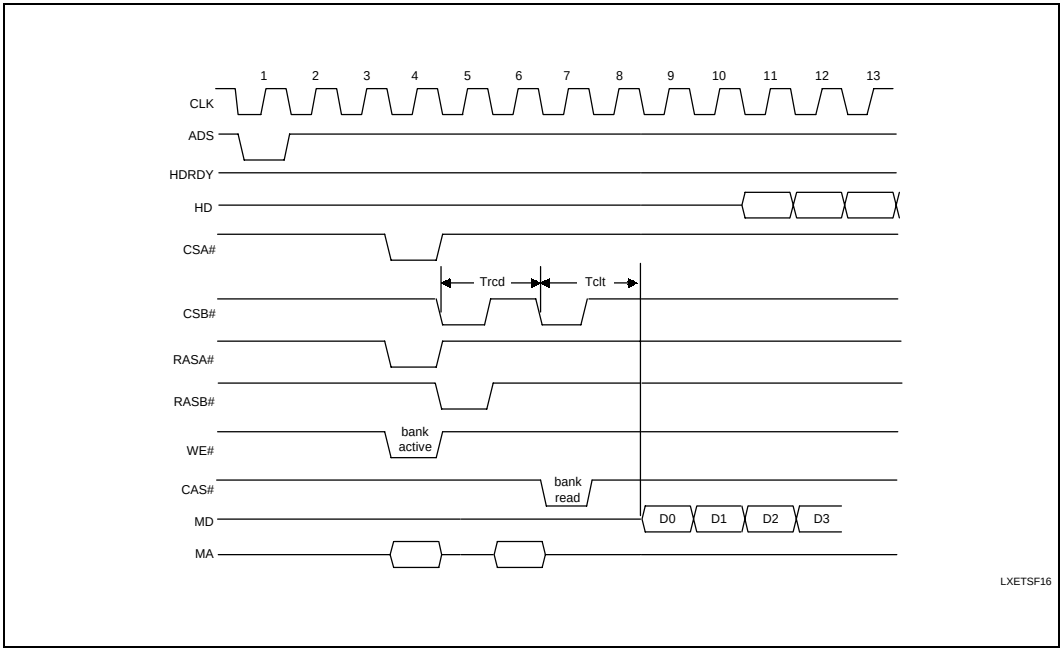


Figure 30. Row Miss-5 with SCLT=1, SRCD=1, SRPT=1

5.8. AC TIMING REQUIREMENT FOR STRAPPING OPTIONS

Figure 31 shows the setup and hold time requirement for the PAC to sample the strapping options. Except for A7#, all other straps (ECCERR#, MECC[0], CKE) are sampled on the rising edge of RSTIN#. Sampling of the strapping options requires a minimum of 1 HCLK for setup time and a minimum of 1 HCLK for hold time. A7# is sampled on the rising edge of CPURST# and requires a 1 HLCK minimum setup time and a 2 HCLK minimum hold time.

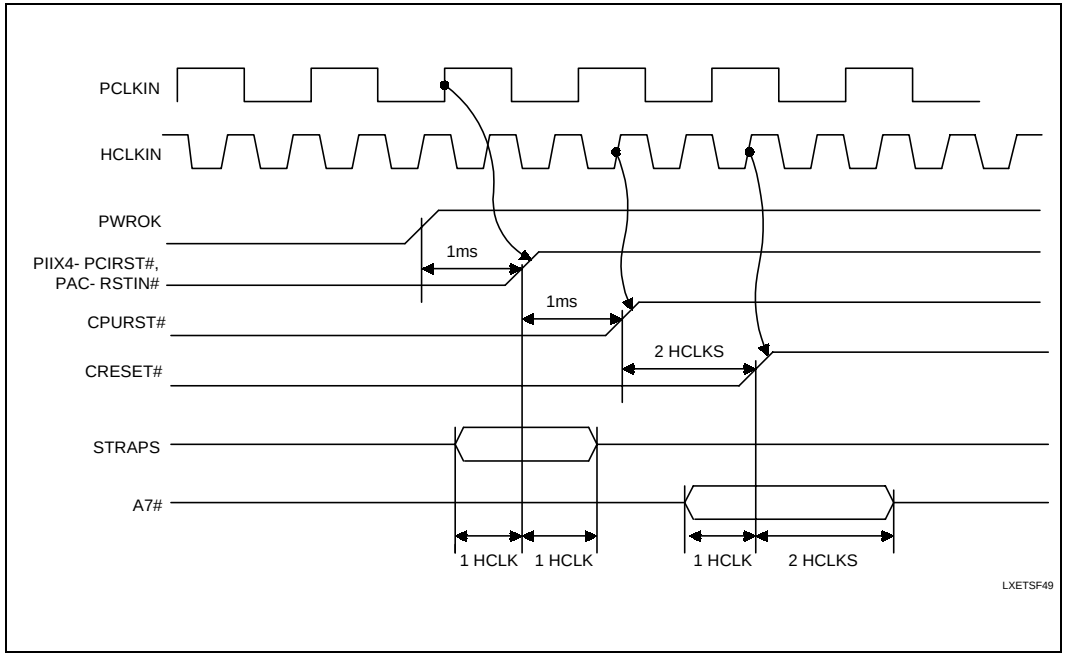


Figure 31. Power on Reset/Strapping Timing Diagram

6.0. PIN ASSIGNMENT

(see following pages)

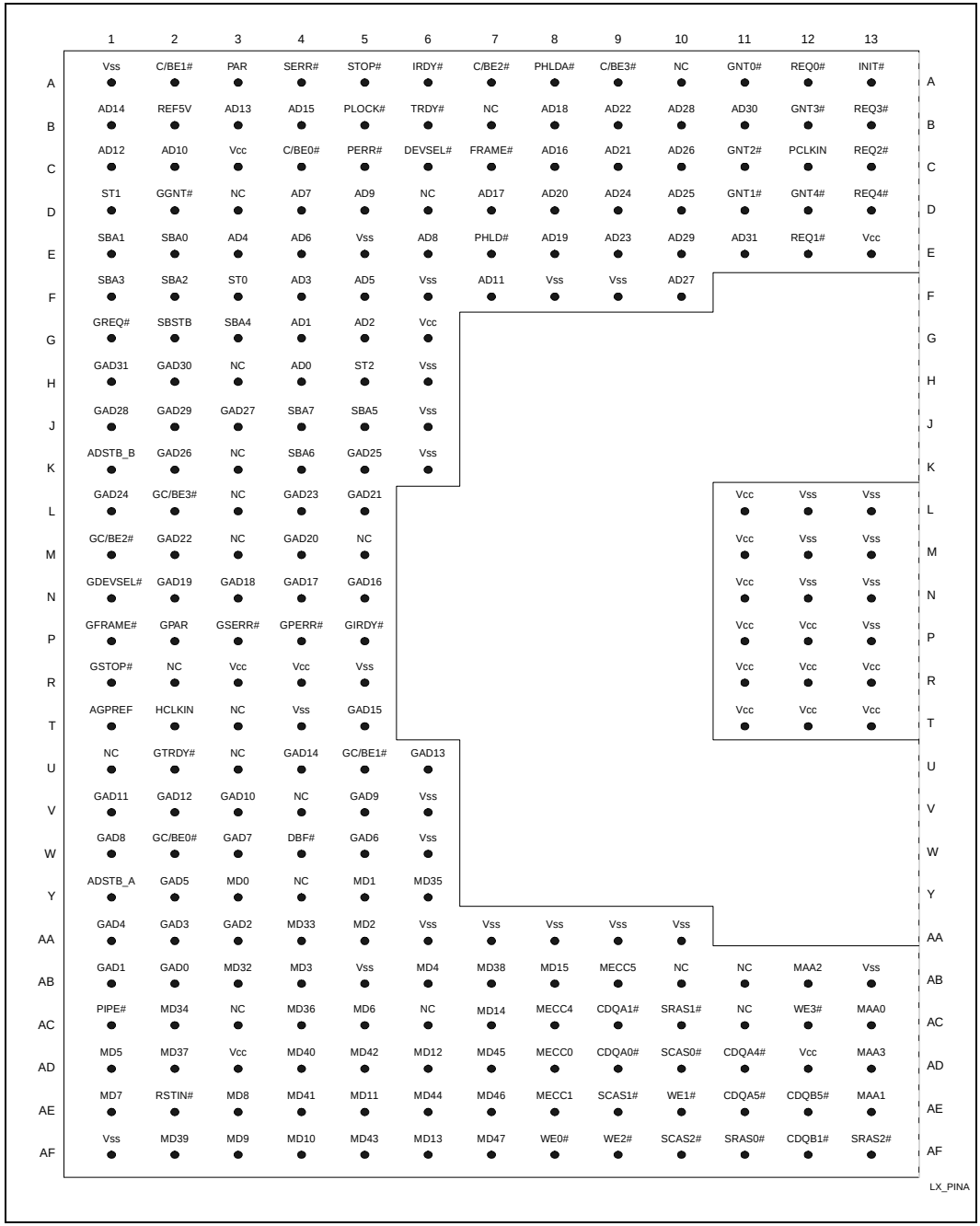


Figure 32. PAC Pinout (Top View)

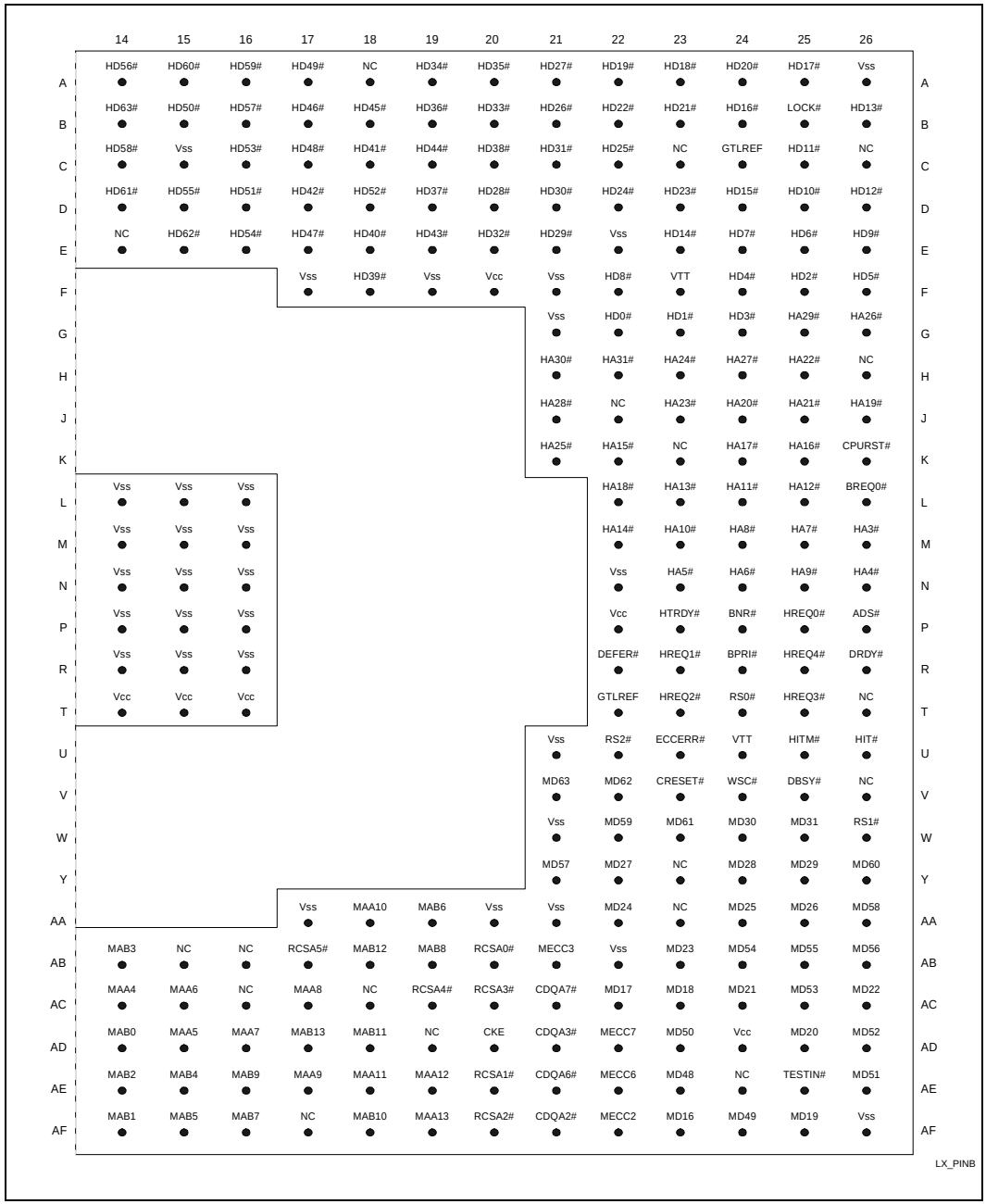


Figure 33. PAC Pinout (Top View)

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
AD0	H4	I/O
AD1	G4	I/O
AD2	G5	I/O
AD3	F4	I/O
AD4	E3	I/O
AD5	F5	I/O
AD6	E4	I/O
AD7	D4	I/O
AD8	E6	I/O
AD9	D5	I/O
AD10	C2	I/O
AD11	F7	I/O
AD12	C1	I/O
AD13	B3	I/O
AD14	B1	I/O
AD15	B4	I/O
AD16	C8	I/O
AD17	D7	I/O
AD18	B8	I/O
AD19	E8	I/O
AD20	D8	I/O
AD21	C9	I/O
AD22	B9	I/O
AD23	E9	I/O
AD24	D9	I/O
AD25	D10	I/O
AD26	C10	I/O
AD27	F10	I/O
AD28	B10	I/O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
AD29	E10	I/O
AD30	B11	I/O
AD31	E11	I/O
ADSTB_A	Y1	I/O
ADSTB_B	K1	I/O
ADS#	P26	I/O
AGPREF	T1	I
BNR#	P24	I/O
BPRI#	R24	O
BREQ0#	L26	O
C/BE0#	C4	I/O
C/BE1#	A2	I/O
C/BE2#	A7	I/O
C/BE3#	A9	I/O
CDQA0#	AD9	O
CDQA1#	AC9	O
CDQA2#	AF21	O
CDQA3#	AD21	O
CDQA4#	AD11	O
CDQA5#	AE11	O
CDQA6#	AE21	O
CDQA7#	AC21	O
CDQB1#	AF12	O
CDQB5#	AE12	O
CKE	AD20	O
CPURST#	K26	I
CRESET#	V23	O
DBSY#	V25	I/O
DEFER#	R22	I/O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
DRDY#	R26	I/O
DEVSEL#	C6	I/O
ECCERR#	U23	O
FRAME#	C7	I/O
GAD0	AB2	I/O
GAD1	AB1	I/O
GAD2	AA3	I/O
GAD3	AA2	I/O
GAD4	AA1	I/O
GAD5	Y2	I/O
GAD6	W5	I/O
GAD7	W3	I/O
GAD8	W1	I/O
GAD9	V5	I/O
GAD10	V3	I/O
GAD11	V1	I/O
GAD12	V2	I/O
GAD13	U6	I/O
GAD14	U4	I/O
GAD15	T5	I/O
GAD16	N5	I/O
GAD17	N4	I/O
GAD18	N3	I/O
GAD19	N2	I/O
GAD20	M4	I/O
GAD21	L5	I/O
GAD22	M2	I/O
GAD23	L4	I/O
GAD24	L1	I/O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
GAD25	K5	I/O
GAD26	K2	I/O
GAD27	J3	I/O
GAD28	J1	I/O
GAD29	J2	I/O
GAD30	H2	I/O
GAD31	H1	I/O
GC/BE0#	W2	I/O
GC/BE1#	U5	I/O
GC/BE2#	M1	I/O
GC/BE3#	L2	I/O
GDEVSEL#	N1	I/O
GFRAME#	P1	I/O
GGNT#	D2	O
GIRDY#	P5	I/O
GNT0#	A11	O
GNT1#	D11	O
GNT2#	C11	O
GNT3#	B12	O
GNT4#	D12	O
GPAR#	P2	I/O
GPERR#	P4	I/O
GREQ#	G1	I
GSERR#	P3	I
GSTOP#	R1	I/O
GTLREF	C24	I
GTLREF	T22	I
GTRDY#	U2	I/O
HA3	M26	I/O
HA4	N26	I/O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
HA5	N23	I/O
HA6	N24	I/O
HA7	M25	I/O
HA8	M24	I/O
HA9	N25	I/O
HA10	M23	I/O
HA11	L24	I/O
HA12	L25	I/O
HA13	L23	I/O
HA14	M22	I/O
HA15	K22	I/O
HA16	K25	I/O
HA17	K24	I/O
HA18	L22	I/O
HA19	J26	I/O
HA20	J24	I/O
HA21	J25	I/O
HA22	H25	I/O
HA23	J23	I/O
HA24	H23	I/O
HA25	K21	I/O
HA26	G26	I/O
HA27	H24	I/O
HA28	J21	I/O
HA29	G25	I/O
HA30	H21	I/O
HA31	H22	I/O
HCLKIN	T2	I
HD0	G22	I/O
HD1	G23	I/O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
HD2	F25	I/O
HD3	G24	I/O
HD4	F24	I/O
HD5	F26	I/O
HD6	E25	I/O
HD7	E24	I/O
HD8	F22	I/O
HD9	E26	I/O
HD10	D25	I/O
HD11	C25	I/O
HD12	D26	I/O
HD13	B26	I/O
HD14	E23	I/O
HD15	D24	I/O
HD16	B24	I/O
HD17	A25	I/O
HD18	A23	I/O
HD19	A22	I/O
HD20	A24	I/O
HD21	B23	I/O
HD22	B22	I/O
HD23	D23	I/O
HD24	D22	I/O
HD25	C22	I/O
HD26	B21	I/O
HD27	A21	I/O
HD28	D20	I/O
HD29	E21	I/O
HD30	D21	I/O
HD31	C21	I/O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
HD32	E20	I/O
HD33	B20	I/O
HD34	A19	I/O
HD35	A20	I/O
HD36	B19	I/O
HD37	D19	I/O
HD38	C20	I/O
HD39	F18	I/O
HD40	E18	I/O
HD41	C18	I/O
HD42	D17	I/O
HD43	E19	I/O
HD44	C19	I/O
HD45	B18	I/O
HD46	B17	I/O
HD47	E17	I/O
HD48	C17	I/O
HD49	A17	I/O
HD50	B15	I/O
HD51	D16	I/O
HD52	D18	I/O
HD53	C16	I/O
HD54	E16	I/O
HD55	D15	I/O
HD56	A14	I/O
HD57	B16	I/O
HD58	C14	I/O
HD59	A16	I/O
HD60	A15	I/O
HD61	D14	I/O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
HD62	E15	I/O
HD63	B14	I/O
HIT#	U26	I/O
HITM#	U25	I/O
HREQ0#	P25	I/O
HREQ1#	R23	I/O
HREQ2#	T23	I/O
HREQ3#	T25	I/O
HREQ4#	R25	I/O
HTRDY#	P23	I/O
INIT#	A13	O
IRDY#	A6	I/O
LOCK#	B25	I
MAA0	AC13	O
MAA1	AE13	O
MAA2	AB12	O
MAA3	AD13	O
MAA4	AC14	O
MAA5	AD15	O
MAA6	AC15	O
MAA7	AD16	O
MAA8	AC17	O
MAA9	AE17	O
MAA10	AA18	O
MAA11	AE18	O
MAA12	AE19	O
MAA13	AF19	O
MAB0	AD14	O
MAB1	AF14	O
MD00	Y3	I/O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
MD01	Y5	I/O
MD02	AA5	I/O
MD03	AB4	I/O
MD04	AB6	I/O
MD05	AD1	I/O
MD06	AC5	I/O
MD07	AE1	I/O
MD08	AE3	I/O
MD09	AF3	I/O
MD10	AF4	I/O
MD11	AE5	I/O
MD12	AD6	I/O
MD13	AF6	I/O
MD14	AC7	I/O
MD15	AB8	I/O
MD16	AF23	I/O
MD17	AC22	I/O
MD18	AC23	I/O
MD19	AF25	I/O
MD20	AD25	I/O
MD21	AC24	I/O
MD22	AC26	I/O
MD23	AB23	I/O
MD24	AA22	I/O
MD25	AA24	I/O
MD26	AA25	I/O
MD27	Y22	I/O
MD28	Y24	I/O
MD29	Y25	I/O
MD30	W24	I/O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
MD31	W25	I/O
MD32	AB3	I/O
MD33	AA4	I/O
MD34	AC2	I/O
MD35	Y6	I/O
MD36	AC4	I/O
MD37	AD2	I/O
MD38	AB7	I/O
MD39	AF2	I/O
MD40	AD4	I/O
MD41	AE4	I/O
MD42	AD5	I/O
MD43	AF5	I/O
MD44	AE6	I/O
MD45	AD7	I/O
MD46	AE7	I/O
MD47	AF7	I/O
MD48	AE23	I/O
MD49	AF24	I/O
MD50	AD23	I/O
MD51	AE26	I/O
MD52	AD26	I/O
MD53	AC25	I/O
MD54	AB24	I/O
MD55	AB25	I/O
MD56	AB26	I/O
MD57	Y21	I/O
MD58	AA26	I/O
MD59	W22	I/O
MD60	Y26	I/O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
MD61	W23	I/O
MD62	V22	I/O
MD63	V21	I/O
MECC0	AD8	I/O
MECC1	AE8	I/O
MECC2	AF22	I/O
MECC3	AB21	I/O
MECC4	AC8	I/O
MECC5	AB9	I/O
MECC6	AE22	I/O
MECC7	AD22	I/O
PAR	A3	I/O
PCLKIN	C12	I
PERR#	C5	I/O
PHLD#	E7	I
PHLDA#	A8	O
PIPE#	AC1	I
PLOCK#	B5	I/O
RCSA0#	AB20	O
RCSA1#	AE20	O
RCSA2#	AF20	O
RCSA3#	AC20	O
RCSA4#	AC19	O
RCSA5#	AB17	O
RCSA6#/ MAB2	AE14	O
RCSA7#/ MAB3	AB14	O
RCSB0#/ MAB6	AA19	O
RCSB1#/ MAB7	AF16	O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
RCSB2#/ MAB8	AB19	O
RCSB3#/ MAB9	AE16	O
RCSB4#/ MAB10	AF18	O
RCSB5#/ MAB11	AD18	O
RCSB6#/ MAB12	AB18	O
RCSB7#/ MAB13	AD17	O
RBF#	W4	I
REF5V	B2	I
REQ0#	A12	I
REQ1#	E12	I
REQ2#	C13	I
REQ3#	B13	I
REQ4#	D13	I
RS0#	T24	I/O
RS1#	W26	I/O
RS2#	U22	I/O
RSTIN#	AE2	I
SBA0	E2	I
SBA1	E1	I
SBA2	F2	I
SBA3	F1	I
SBA4	G3	I
SBA5	J5	I
SBA6	K4	I
SBA7	J4	I
SBSTB	G2	I

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
SCAS0#	AD10	O
SCAS1#	AE9	O
SCAS2#	AF10	O
SCAS3#/ MAB4	AE15	O
SRAS3#/ MAB5	AF15	O
SERR#	A4	O
SRAS0#	AF11	O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
SRAS1#	AC10	O
SRAS2#	AF13	O
ST0	F3	O
ST1	D1	O
ST2	H5	O
STOP#	A5	I/O
TESTIN#	AE25	I
TRDY#	B6	I/O

Table 34. 82443LX Pin Assignment

Name	Ball #	Type
WE0#	AF8	O
WE1#	AE10	O
WE2#	AF9	O
WE3#	AC12	O
WSC#	V24	O

Table 35. 82443LX Pinout (Power, Ground, and No Connects)

Name	Ball #
V_{CC}	AD3, C3, R3, R4, G6, L11, M11, N11, P11, R11, T11, P12, R12, T12, AD12, E13, R13, T13, T14, T15, T16, F20, P22, AD24
V_{SS}	A1, AF1, T4, E5, AB5, R5, F6, H6, J6, K6, V6, W6, AA6, AA7, F8, AA8, F9, AA9, AA10, L12, M12, N12, L13, M13, N13, P13, AB13, L14, M14, N14, P14, R14, C15, L15, M15, N15, P15, R15, L16, M16, N16, P16, R16, F17, AA17, F19, AA20, F21, G21, U21, W21, AA21, E22, N22, AB22, A26, AF26, W21
V_{TT}	U24, F23
NC	U1, R2, D3, H3, K3, L3, M3, T3, U3, AC3, V4, Y4, M5, D6, AC6, B7, A10, AB10, AB11, AC11, E14, AB15, AB16, AC16, AF17, A18, AC18, AD19, J22, C23, K23, Y23, AA23, AE24, C26, H26, T26, V26

NOTES:

1. NC=No Connect
2. V_{TT}=GTL+

7.0. PACKAGE SPECIFICATIONS

This specification outlines the mechanical dimensions for PAC. The package is a 492 ball grid array (BGA).

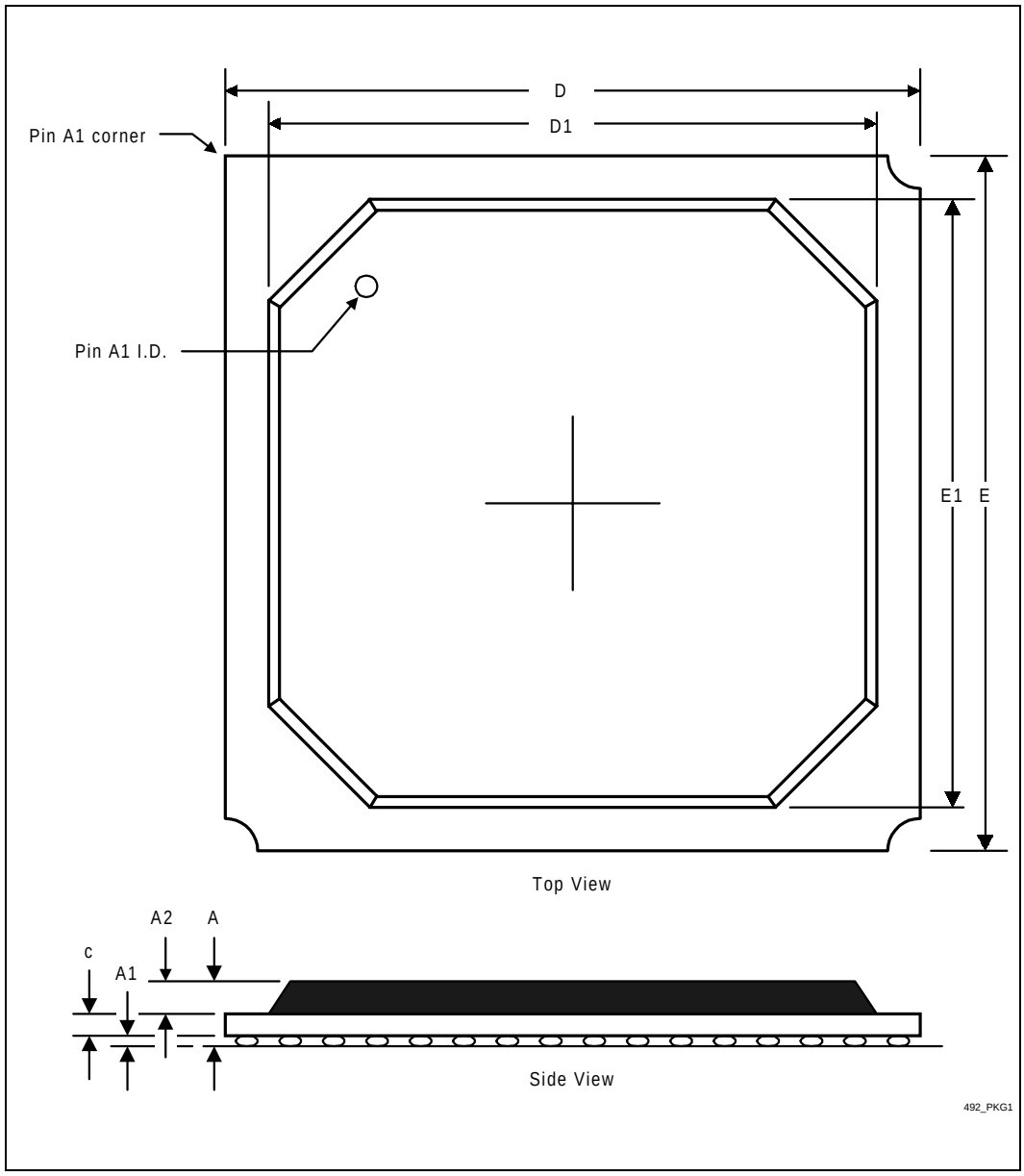


Figure 34. PAC Package Dimensions (492 BGA)

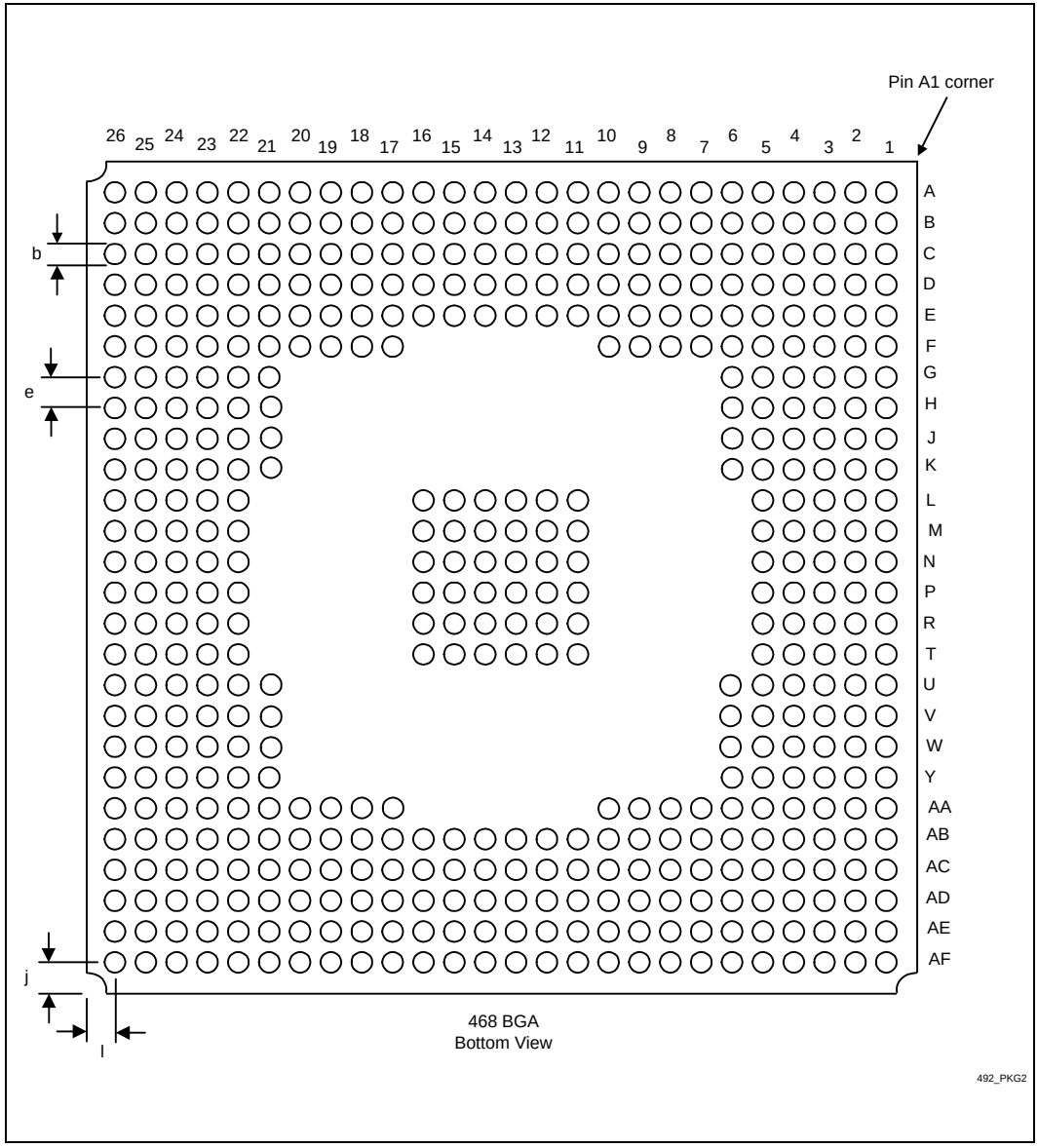


Figure 35. PAC Package Dimensions (492 BGA)

Table 36. PAC Package Dimensions (468 BGA)

Symbol	e=1.27 mm (solder ball pitch)			Note
	Min	Nom	Max	
A	2.14	2.33	2.52	
A1	0.50	0.60	0.70	
A2	1.12	1.17	1.22	
D	34.80	35.00	35.20	
D1	29.75	30.00	30.25	
E	34.80	35.00	35.20	
E1	29.75	30.00	30.25	
I	1.63 REF.			
J	1.63 REF.			
M	26 x 26 Matrix			
N	4.92			
b	0.60	0.75	0.90	
c	0.52	0.56	0.60	

8.0. TESTABILITY

The test modes described below are provided in PAC for Automated Test Equipment (ATE) board level testing.

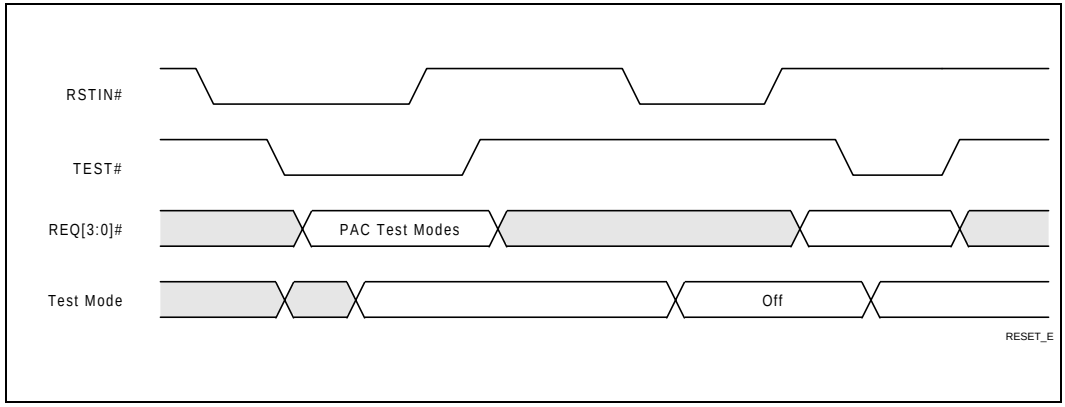


Figure 36. Reset Enabled Test Mode

8.1. 82443LX (PAC) Test Modes

To enable a test mode, the TESTIN# input signal is asserted (low), and a 4-bit value is presented on the REQ[3:0]# input pins. The following table shows the REQ[3:0]# encodings for test modes:

Table 37. PAC Test Mode Select

PCI REQ[3:0]	Test Mode Enabled
0010	Tri-State All Outputs
0101	NAND Chain Test
1111	Disable All Test Modes

8.1.1. NAND CHAIN TEST MODE

This test mode is used during board level connectivity test. This allows ATE to test the connectivity of PAC signal pins. Special attention should be taken to channel sharing, and the NAND chain element assignment, so that signal sharing the same tester channel don't end up on the same chain.

Table 38. NAND Chain Outputs

Pins for NAND Chain	Purpose
SBA[0]	NAND Chain 0 Output
SBA[1]	NAND Chain 1 Output
SBA[2]	NAND Chain 2 Output
SBA[3]	NAND Chain 3 Output
SBA[4]	NAND Chain 4 Output
SBA[5]	NAND Chain 5 Output
SBA[6]	NAND Chain 6 Output
SBA[7]	NAND Chain 7 Output

The 82443LX NAND chain pin assignments are shown in the table below:

Table 39. The 82443LX NAND Chain Pin Assignments

NANDtree0	NANDtree1	NANDtree2	NANDtree3	NANDtree4	NANDtree5	NANDtree6	NANDtree7
GAD24	GAD21	GAD30	GAD25	SBSTB	MECC4	GREQ#	A10
GAD20	GAD29	GAD28	GAD27	ADSTB_B	MECC5	GC/BE3#	A7
GAD22	GAD23	GAD26	GAD31	GDEVSEL	SCAS0#	GC/BE2#	A8
GAD18	GAD17	MD0	MD34	ADSTB_A	SCAS1#	GFRAME	A14
GAD16	GAD19	MD5	MD32	MECC0	WE1#	GPAR#	A12
GAD12	GAD11	MD1	MD37	SRAS1#	WE3#	GPERR#	A13
GAD8	GAD15	MD2	MD33	CDQA1#	SCAS2#	GSERR#	A16
GAD10	GAD5	MD3	MD35	MECC1	CDQA4#	GIRDY#	A19
GAD14	GAD13	MD7	MD36	CDQA0#	CDQB5#	GSTOP#	A11
GAD4	GAD9	MD6	MD40	WE0#	CDQB1#	GTRDY#	A21
GAD0	GAD7	MD4	MD39	WE2#	SCAS3#	GC/BE0#	A18
GAD2	GAD1	MD8	MD38	CDQA5#	RCSB1#	GC/BE1#	A20
GAD6	GAD3	MD14	MD42	SRAS0#	RCSB3#	RBF#	A22
HD5	HD32	MD9	MD41	SRAS2#	RCSB4#	PIPE#	A17
HD9	HD39	MD10	MD45	RCSA6#	RCSB7#	CKE	A26
HD2	HD43	MD15	MD44	RCSA7#	RCSB5#	ECCERR	A15

Table 39. The 82443LX NAND Chain Pin Assignments

NANDtree0	NANDtree1	NANDtree2	NANDtree3	NANDtree4	NANDtree5	NANDtree6	NANDtree7
HD6	HD37	MD12	MD43	SRAS3#	RCSB6#	WSC#	A29
HD4	HD38	MD11	MD46	RCSA5#	CDQA6#	RS2	A25
HD12	HD44	MD13	MD47	RCSA2#	MECC6	RS1	A23
HD10	HD40	MAA2	AB1	CDQA2#	RCSB2#	DBSY#	A27
HD3	HD33	MAA3	AB0	RCSA1#	MECC7	HITM#	A31
HD7	HD52	MAA0	MAA9	MECC2	RCSB0#	HREQ3	A24
HD11	HD47	MAA1	MAA11	RCSA4#	CDQA7#	HIT#	A30
HD1	HD35	MAA4	MAA8	CDQA3#	DEFER#	HREQ2	A28
HD15	HD36	MAA5	MAA13	RCSA3#	ADS#	HREQ4	HLOCK#
HD14	HD42	MAA6	MAA12	MECC3	A4	RS0	INIT
HD0	HD41	MAA7	MAA10	RCSA0#	A9	DRDY#	REQ4#
HD13	HD34	MD16	MD48	CPURST#	A5	BNR#	PCLKIN#
HD8	HD45	MD17	MD49	REQ3#	A6	HTRDY#	REQ2#
HD23	HD48	MD19	MD50	GNT0#	A3	HREQ1	REQ1#
HD30	HD46	MD18	MD51	GNT1#	BREQ0#	HREQ0	REQ0#
HD17	HD57	MD21	MD57	PHLDA#	GNT4#	BPRI	AD30
HD29	HD53	MD23	MD52	AD25	GNT3#	AD7	AD28
HD24	HD49	MD24	MD54	AD24	GNT2#	AD3	C/BE3#
HD16	HD54	MD20	MD53	IRDY#	PERR#	AD14	AD31
HD28	HD59	MD27	MD63	AD29	PAR#	AD5	AD22
HD20	HD50	MD22	MD59	AD27	PHLD#	AD6	AD26
HD25	HD51	MD25	MD61	AD23	AD13	AD1	AD21
HD21	HD60	MD26	MD55	STOP#	AD8	AD10	AD18
HD18	HD62	MD30	MD56	AD16	AD9	AD2	C/BE2#
HD31	HD58	MD29	MD62	TRDY#	C/BE0#	AD12	AD17
HD22	HD61	MD28	MD58	AD20	C/BE1#	AD0	AD19
HD26	HD63	CRESET#	MD60	PLOCK#	AD11	AD4	DEVSEL#
HD19	HD56	MD31		SERR#	GGNT#	ST1	FRAME#
HD27	HD55			ST2		ST0	AD15