NEC

User's Manual

V850ES/KF1, V850ES/KG1, V850ES/KJ1

32-Bit Single-Chip Microcontrollers

Hardware

V850ES/KF1:
μPD703208
μPD703208(A)/(A1)/(A2)
μPD703208Y
μPD703208Y(A)/(A1)/(A2)
μPD703209
μPD703209(A)/(A1)/(A2)
μPD703209Y
μPD703209Y(A)/(A1)/(A2)
μPD703210
μPD703210(A)/(A1)/(A2)
μPD703210Y
μPD703210Y(A)/(A1)/(A2)
μPD70F3210
μPD70F3210(A)
μPD70F3210Y
μPD70F3210Y(A)

V850ES/KG1:
μPD703212
μPD703212(A)/(A1)/(A2)
μPD703212Y
μPD703212Y(A)/(A1)/(A2)
μPD703213
μPD703213(A)/(A1)/(A2)
μPD703213Y
μPD703213Y(A)/(A1)/(A2)
μPD703214
μPD703214(A)/(A1)/(A2)
μPD703214Y
μPD703214Y(A)/(A1)/(A2)
μPD70F3214
μPD70F3214(A)
μPD70F3214Y
μPD70F3214Y(A)

V850ES/KJ1:
μPD703216
μPD703216(A)/(A1)/(A2)
μPD703216Y
μPD703216Y(A)/(A1)/(A2)
μPD703217
μPD703217(A)/(A1)/(A2)
μPD703217Y
μPD703217Y(A)/(A1)/(A2)
μPD70F3217
μPD70F3217(A)
μPD70F3217Y
μPD70F3217Y(A)

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[MEMO]

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note:

Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note:

No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note:

Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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PREFACE

Readers

This manual is intended for users who wish to understand the functions of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 and design application systems using these products.
The target products are as follows.

- Standard products: μPD703208, 703208Y, 703209, 703209Y, 703210, 703210Y, 703212, 703212Y, 703213, 703213Y, 703214, 703214Y, 703216, 703216Y, 703217, 703217Y, 70F3210, 70F3210Y, 70F3214, 70F3214Y, 70F3217, 70F3217Y
- Special products: μPD703208(A), 703208Y(A), 703209(A), 703209Y(A), 703210(A), 703210Y(A), 703212(A), 703212Y(A), 703213(A), 703213Y(A), 703214(A), 703214Y(A), 703216(A), 703216Y(A), 703217(A), 703217Y(A), 70F3210(A), 70F3210Y(A), 70F3214(A), 70F3214Y(A), 70F3217(A), 70F3217Y(A), 703208(A1), 703208Y(A1), 703209(A1), 703209Y(A1), 703210(A1), 703210Y(A1), 703212(A1), 703212Y(A1), 703213(A1), 703213Y(A1), 703214(A1), 703214Y(A1), 703216(A1), 703216Y(A1), 703217(A1), 703217Y(A1), 703208(A2), 703208Y(A2), 703209(A2), 703209Y(A2), 703210(A2), 703210Y(A2), 703212(A2), 703212Y(A2), 703213(A2), 703213Y(A2), 703214(A2), 703214Y(A2), 703216(A2), 703216Y(A2), 703217(A2), 703217Y(A2)

Purpose

This manual is intended to give users an understanding of the hardware functions of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 shown in the **Organization** below.

Organization

This manual is divided into two parts: Hardware (this manual) and Architecture (**V850ES Architecture User's Manual**).

Hardware	Architecture
• Pin functions	• Data types
• CPU function	• Register set
• On-chip peripheral functions	• Instruction format and instruction set
• Flash memory programming	• Interrupts and exceptions
• Electrical specifications	• Pipeline operation

How to Read This Manual It is assumed that the readers of this manual have general knowledge in the fields of electrical engineering, logic circuits, and microcontrollers.

Cautions

1. **The application examples in this manual apply to "standard" quality grade products for general electronic systems. When using an example in this manual for an application that requires a "special" quality grade product, thoroughly evaluate the component and circuit to be actually used to see if they satisfy the special quality grade.**
2. **When using this manual as a manual for a special grade product, read the part numbers as follows.**

μPD703208	→	μPD703208(A), 703208(A1), 703208(A2)
μPD703208Y	→	μPD703208Y(A), 703208Y(A1), 703208Y(A2)
μPD703209	→	μPD703209(A), 703209(A1), 703209(A2)
μPD703209Y	→	μPD703209Y(A), 703209Y(A1), 703209Y(A2)
μPD703210	→	μPD703210(A), 703210(A1), 703210(A2)
μPD703210Y	→	μPD703210Y(A), 703210Y(A1), 703210Y(A2)
μPD703212	→	μPD703212(A), 703212(A1), 703212(A2)
μPD703212Y	→	μPD703212Y(A), 703212Y(A1), 703212Y(A2)
μPD703213	→	μPD703213(A), 703213(A1), 703213(A2)
μPD703213Y	→	μPD703213Y(A), 703213Y(A1), 703213Y(A2)
μPD703214	→	μPD703214(A), 703214(A1), 703214(A2)
μPD703214Y	→	μPD703214Y(A), 703214Y(A1), 703214Y(A2)
μPD703216	→	μPD703216(A), 703216(A1), 703216(A2)
μPD703216Y	→	μPD703216Y(A), 703216Y(A1), 703216Y(A2)
μPD703217	→	μPD703217(A), 703217(A1), 703217(A2)
μPD703217Y	→	μPD703217Y(A), 703217Y(A1), 703217Y(A2)
μPD70F3210	→	μPD70F3210(A)
μPD70F3210Y	→	μPD70F3210Y(A)
μPD70F3214	→	μPD70F3214(A)
μPD70F3214Y	→	μPD70F3214Y(A)
μPD70F3217	→	μPD70F3217(A)
μPD70F3217Y	→	μPD70F3217Y(A)

To find the details of a register where the name is known
→ Refer to **APPENDIX A REGISTER INDEX**.

To understand the details of an instruction function
→ Refer to the **V850ES Architecture User's Manual**.

Register format
→ The name of the bit whose number is in angle brackets (<>) in the figure of the register format of each register is defined as a reserved word in the device file.

To understand the overall functions of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1
→ Read this manual according to the **CONTENTS**.

To know the electrical specifications of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1
→ Refer to **CHAPTER 26 ELECTRICAL SPECIFICATIONS.**

The mark ★ shows major revised points.

Conventions

Data significance:	Higher digits on the left and lower digits on the right	
Active low representation:	$\overline{xxx}$ (overscore over pin or signal name)	
Memory map address:	Higher addresses on the top and lower addresses on the bottom	
Note:	Footnote for item marked with **Note** in the text	
Caution:	Information requiring particular attention	
Remark:	Supplementary information	
Numeric representation:	Binary	... xxxx or xxxxB
	Decimal	... xxxx
	Hexadecimal	... xxxxH

Prefix indicating power of 2 (address space, memory capacity):

K (kilo):	$2^{10} = 1,024$
M (mega):	$2^{20} = 1,024^2$
G (giga):	$2^{30} = 1,024^3$

Related Documents

The related documents indicated in this publication may include preliminary versions. However, preliminary versions are not marked as such.

Documents related to V850ES/KF1, V850ES/KG1, and V850ES/KJ1

Document Name	Document No.
V850ES Architecture User's Manual	U15943E
V850ES/KF1, V850ES/KG1, V850ES/KJ1 Hardware User's Manual	This manual

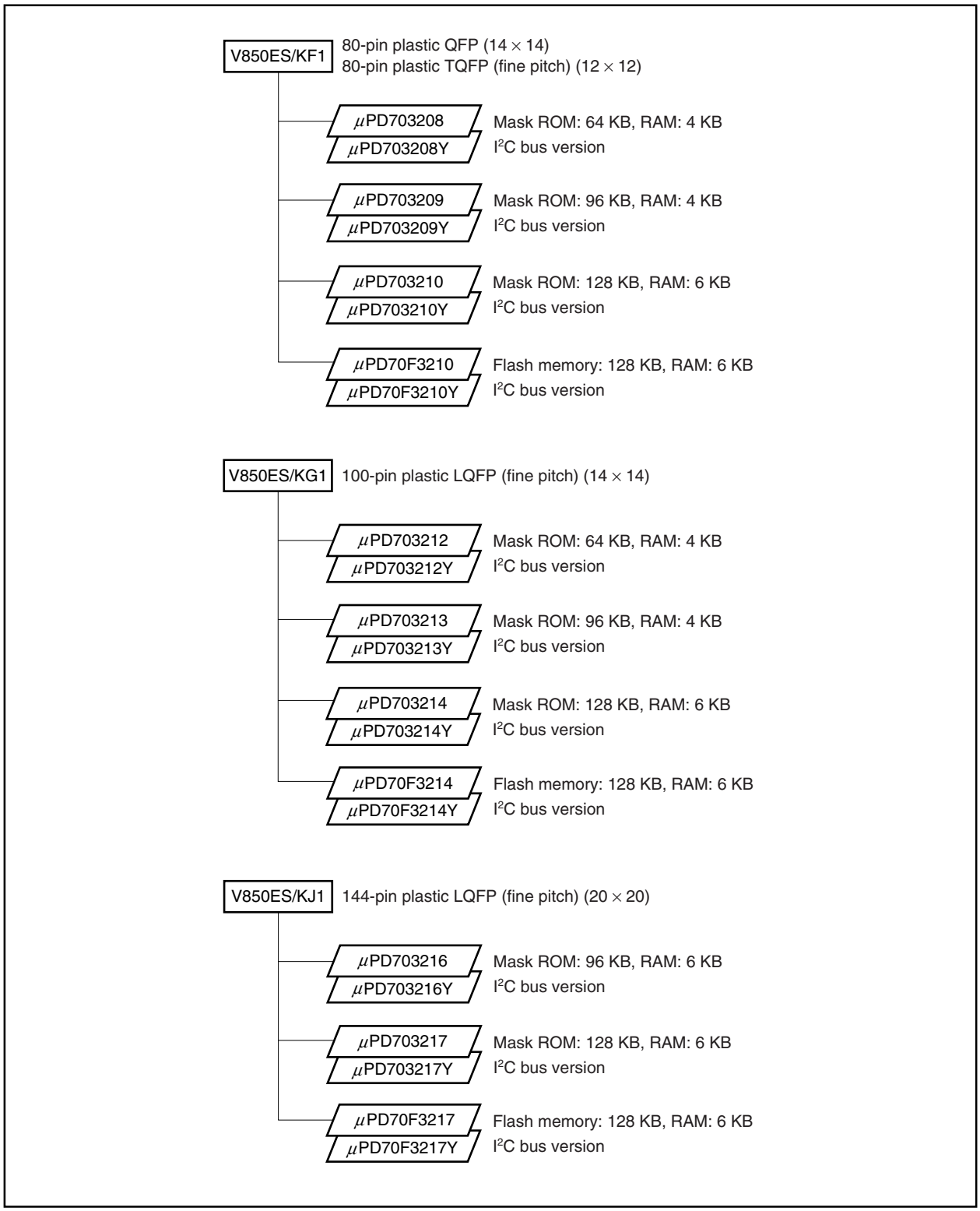
Documents related to development tools (user's manuals)

Document Name		Document No.
IE-V850ES-G1 (In-Circuit Emulator)		U16313E
IE-703217-G1-EM1 (In-Circuit Emulator Option Board)		U16594E
CA850 Ver. 2.50 C Compiler Package	Operation	U16053E
	C Language	U16054E
	Assembly Language	U16042E
PM plus Ver. 5.10		U16569E
ID850 Ver. 2.50 Integrated Debugger	Operation	U16217E
SM850 Ver. 2.50 System Simulator	Operation	U15182E
SM850 Ver. 2.00 or Later System Simulator	External Part User Open Interface Specifications	U14873E
RX850 Ver. 3.13 or Later Real-Time OS	Fundamental	U13430E
	Installation	U13410E
	Technical	U13431E
RX850 Pro Ver. 3.15 Real-Time OS	Fundamental	U13773E
	Installation	U13774E
	Technical	U13772E
RD850 Ver. 3.01 Task Debugger		U13737E
RD850 Pro Ver. 3.01 Task Debugger		U13916E
AZ850 Ver. 3.0 System Performance Analyzer		U14410E
PG-FP3 Flash Memory Programmer		U13502E
PG-FP4 Flash Memory Programmer		U15260E

CONTENTS

1.1 K1 Family Product Lineup

1.1.1 V850ES/Kx1 Series lineup



The following shows the function list of the V850ES/Kx1.

Part No. \ Function		Timer					Serial Interface				A/D	D/A	RTO	I/O	Other
		8-Bit	16-Bit	TMH	Watch	WDT	CSI	CSIA	UART	I^2C					
V850ES/KF1	μPD703208	2 ch	2 ch	2 ch	1 ch	2 ch	2 ch	1 ch	2 ch	–	8 ch	–	6 ch	67	–
	μPD703208Y									1 ch					
	μPD703209									–					
	μPD703209Y									1 ch					
	μPD703210									–					
	μPD703210Y									1 ch					
	μPD70F3210									–					
	μPD70F3210Y									1 ch					
V850ES/KG1	μPD703212	2 ch	4 ch	2 ch	1 ch	2 ch	2 ch	2 ch	2 ch	–	8 ch	2 ch	6 ch	84	–
	μPD703212Y									1 ch					
	μPD703213									–					
	μPD703213Y									1 ch					
	μPD703214									–					
	μPD703214Y									1 ch					
	μPD70F3214									–					
	μPD70F3214Y									1 ch					
V850ES/KJ1	μPD703216	2 ch	6 ch	2 ch	1 ch	2 ch	3 ch	2 ch	3 ch	–	16 ch	2 ch	12 ch	128	–
	μPD703216Y									2 ch					
	μPD703217									–					
	μPD703217Y									2 ch					
	μPD70F3217									–					
	μPD70F3217Y									2 ch					

Remark In this manual, the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 product names are used as follows.

- Mask ROM versions
  V850ES/KF1: μPD703208, 703208Y, 703209, 703209Y, 703210, 703210Y
  V850ES/KG1: μPD703212, 703212Y, 703213, 703213Y, 703214, 703214Y
  V850ES/KJ1: μPD703216, 703216Y, 703217, 703217Y
- Flash memory versions
  V850ES/KF1: μPD70F3210, 70F3210Y
  V850ES/KG1: μPD70F3214, 70F3214Y
  V850ES/KJ1: μPD70F3217, 70F3217Y
- I^2C bus versions
  V850ES/KF1: μPD703208Y, 703209Y, 703210Y, 70F3210Y
  V850ES/KG1: μPD703212Y, 703213Y, 703214Y, 70F3214Y
  V850ES/KJ1: μPD703216Y, 703217Y, 70F3217Y

★ **1.1.2 78K0/Kx1 Series lineup**

The lineup of products in the 78K0/Kx1 Series is shown below.

78K0/KB1: 30-pin (7.62 mm 0.65 mm pitch)

- μPD78F0103 Flash memory: 24 KB, RAM: 768 bytes
  - μPD780103 Mask ROM: 24 KB, RAM: 768 bytes
    - μPD780102 Mask ROM: 16 KB, RAM: 768 bytes
      - μPD780101 Mask ROM: 8 KB, RAM: 512 bytes

78K0/KC1: 44-pin (10x10 mm 0.8 mm pitch)

- μPD78F0114 Flash memory: 32 KB, RAM: 1 KB
  - μPD780114 Mask ROM: 32 KB, RAM: 1 KB
    - μPD780113 Mask ROM: 24 KB, RAM: 1 KB
      - μPD780112 Mask ROM: 16 KB, RAM: 512 bytes
        - μPD780111 Mask ROM: 8 KB, RAM: 512 bytes

78K0/KD1: 52-pin (10x10 mm 0.65 mm pitch)

- μPD78F0124 Flash memory: 32 KB, RAM: 1 KB
  - μPD780124 Mask ROM: 32 KB, RAM: 1 KB
    - μPD780123 Mask ROM: 24 KB, RAM: 1 KB
      - μPD780122 Mask ROM: 16 KB, RAM: 512 bytes
        - μPD780121 Mask ROM: 8 KB, RAM: 512 bytes

78K0/KE1: 64-pin (10x10 mm 0.5 mm pitch, 12x12 mm 0.65 mm pitch, 14x14 mm 0.8 mm pitch)

- μPD78F0134 Flash memory: 32 KB, RAM: 1 KB
  - μPD780134 Mask ROM: 32 KB, RAM: 1 KB
    - μPD780133 Mask ROM: 24 KB, RAM: 1 KB
      - μPD780132 Mask ROM: 16 KB, RAM: 512 bytes
        - μPD780131 Mask ROM: 8 KB, RAM: 512 bytes
- μPD78F0138 Flash memory: 60 KB, RAM: 2 KB
  - μPD780138 Mask ROM: 60 KB, RAM: 2 KB
    - μPD780136 Mask ROM: 48 KB, RAM: 2 KB

78K0/KF1: 80-pin (12x12 mm 0.5 mm pitch, 14x14 mm 0.65 mm pitch)

- μPD78F0148 Flash memory: 60 KB, RAM: 2 KB
  - μPD780148 Mask ROM: 60 KB, RAM: 2 KB
    - μPD780146 Mask ROM: 48 KB, RAM: 2 KB
      - μPD780144 Mask ROM: 32 KB, RAM: 1 KB
        - μPD780143 Mask ROM: 24 KB, RAM: 1 KB

The following shows the function list of the 78K0/Kx1 Series.

Item \ Product Name		78K0/KB1	78K0/KC1	78K0/KD1	78K0/KE1	78K0/KF1
Package		30-pin	44-pin	52-pin	64-pin	80-pin
Internal memory	Mask ROM	8 KB / 16 KB / 24 KB / –	8 KB / 16 KB / 24 KB / 32 KB / –	8 KB / 16 KB / 24 KB / 32 KB / –	8 KB / 16 KB / 24 KB / 32 KB / 48 KB / 60 KB / –	24 KB / 32 KB / 48 KB / 60 KB / –
	Flash memory	– / 24 KB	– / 32 KB	– / 32 KB	– / 32 KB / 60 KB	– / 60 KB
	RAM	512 bytes / 768 bytes	512 bytes / 1 KB	512 bytes / 1 KB	512 bytes / 1 KB / 2 KB	1 KB / 2 KB
Supply voltage		V_{DD} = 2.7 to 5.5 V				
Minimum instruction execution time		0.2 μs (10 MHz, when V_{DD} = 4.0 to 5.5 V) 0.24 μs (8.38 MHz, when V_{DD} = 3.3 to 5.5 V) 0.4 μs (5 MHz, when V_{DD} = 2.7 to 5.5 V)		<REGC pin connected to V_{DD}> 0.2 μs (10 MHz, when V_{DD} = 4.0 to 5.5 V) 0.24 μs (8.38 MHz, when V_{DD} = 3.3 to 5.5 V) 0.4 μs (5 MHz, when V_{DD} = 2.7 to 5.5 V)	
Clock	X1 input	2 to 10 MHz				
	Sub	–	32.768 kHz			
	RC	–				
	Ring-OSC	240 kHz (TYP.)				
Port	CMOS I/O	17	19	26	38	54
	CMOS input	4	8			
	CMOS output	1				
	N-ch open-drain I/O	–	4			
Timer	16-bit (TM0)	1 ch			2 ch	1 ch / 2 ch
	8-bit (TM5)	1 ch	2 ch			
	8-bit (TMH)	2 ch				
	Watch	–	1 ch			
	WDT	1 ch				
Serial interface	3-wire CSI[Note]	1 ch			2 ch	1 ch / 2 ch
	Automatic transmit/ receive 3-wire CSI	–				1 ch
	UART[Note]	–	1 ch			
	UART supporting LIN-bus	1 ch				
10-bit A/D converter		4 ch	8 ch			
Interrupt	External	6	7	8	9	9
	Internal	11 / 12	15		16 / 19	17 / 20
Key return input		–	4 ch	8 ch		
Reset	$\overline{\text{RESET}}$ pin	Provided				
	POC	2.85 V±0.15 V/3.5 V±0.20 V (selectable by a mask option)				
	LVI	3.1 V/3.3 V±0.15 V/3.5 V/3.7 V/3.9 V/4.1 V/4.3 V±0.2 V (selectable by software)				
	Clock monitor	Provided				
	WDT	Provided				
Multiplier/divider		–			16 bits × 16 bits, 32 bits ÷ 16 bits	
ROM correction		–			Provided	–
Standby function		HALT/STOP mode				
Operating ambient temperature		Standard products, special grade (A) products: –40 to +85°C Special grade (A1) products: –40 to +110°C (Mask ROM version), –40 to +105°C (Flash memory version) Special grade (A2) products: –40 to +125°C (Mask ROM version)				

Note If the pin is an alternate-function pin, either function is selected for use.

1.2 V850ES/KF1

1.2.1 Features (V850ES/KF1)

- Minimum instruction execution time: 50 ns (operation at main clock (fxx) = 20 MHz)
- General-purpose registers: 32 bits × 32 registers
- CPU features: Signed multiplication (16 × 16 → 32): 1 to 2 clocks
  (Instructions without creating register hazards can be continuously executed in parallel)
  Saturated operations (overflow and underflow detection functions are included)
  32-bit shift instruction: 1 clock
  Bit manipulation instructions
  Load/store instructions with long/short format
- Memory space: 64 MB of linear address space
  Memory block division function: 2 MB, 64 KB (Total of 2 blocks)
  - External bus interface
    μPD703208, 703208Y (Mask ROM: 64 KB/RAM: 4 KB)
    μPD703209, 703209Y (Mask ROM: 96 KB/RAM: 4 KB)
    μPD703210, 703210Y (Mask ROM: 128 KB/RAM: 6 KB)
    μPD70F3210, 70F3210Y (Flash memory: 128 KB/RAM: 6 KB)
  - Internal memory
    16-bit data bus
- Interrupts and exceptions
  Non-maskable interrupts: 3 sources
  Maskable interrupts: 30 sources (μPD703208, 703209, 703210, 70F3210)
  31 sources (μPD703208Y, 703209Y, 703210Y, 70F3210Y)
  Software exceptions: 32 sources
  Exception trap: 1 source
- I/O lines: Total: 67
- Key interrupt function
- Timer function
  16-bit timer/event counter: 2 channels
  8-bit timer/event counter: 2 channels
  8-bit timer H: 2 channels
  8-bit interval timer BRG: 1 channel
  Watch timer/interval timer: 1 channel
  Watchdog timers
    Watchdog timer 1 (also usable as oscillation stabilization timer): 1 channel
    Watchdog timer 2: 1 channel
- Serial interface (SIO)
  Asynchronous serial interface (UART): 2 channels
  3-wire serial I/O (CSI0): 2 channels
  3-wire serial I/O (with automatic transmit/receive function) (CSIA): 1 channel
  I^2C bus interface (I^2C): 1 channel
  (μPD703208Y, 703209Y, 703210Y, 70F3210Y)
- A/D converter: 10-bit resolution × 8 channels
- Real-time output port: 6 bits × 1 channel
- Power-save functions: HALT/IDLE/STOP modes, subclock/sub-IDLE modes

- ROM correction: 4 correction addresses specifiable
- Packages: 80-pin plastic QFP (14 × 14)
  80-pin plastic TQFP (fine pitch) (12 × 12)

1.2.2 Applications (V850ES/KF1)

- Automotive
  - System control of body electrical system (power windows, keyless entry reception, etc.)
  - Submicrocontroller of control system
- Home audio, car audio
- AV equipment
- PC peripheral devices (keyboards, etc.)
- Household appliances
  - Outdoor units of air conditioners
  - Microwave ovens, rice cookers
- Industrial devices
  - Pumps
  - Vending machines
  - FA

1.2.3 Ordering information (V850ES/KF1)

(1) Standard products, (A) grade products

Part Number	Package	Quality Grade
μPD703208GC-×××-8BT	80-pin plastic QFP (14 × 14)	Standard
μPD703208YGC-×××-8BT	80-pin plastic QFP (14 × 14)	Standard
μPD703208GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Standard
μPD703208YGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Standard
μPD703209GC-×××-8BT	80-pin plastic QFP (14 × 14)	Standard
μPD703209YGC-×××-8BT	80-pin plastic QFP (14 × 14)	Standard
μPD703209GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Standard
μPD703209YGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Standard
μPD703210GC-×××-8BT	80-pin plastic QFP (14 × 14)	Standard
μPD703210YGC-×××-8BT	80-pin plastic QFP (14 × 14)	Standard
μPD703210GK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Standard
μPD703210YGK-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Standard
μPD70F3210GC-8BT	80-pin plastic QFP (14 × 14)	Standard
μPD70F3210YGC-8BT	80-pin plastic QFP (14 × 14)	Standard
μPD70F3210GK-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Standard
μPD70F3210YGK-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Standard
μPD703208GC(A)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703208YGC(A)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703208GK(A)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703208YGK(A)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703209GC(A)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703209YGC(A)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703209GK(A)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703209YGK(A)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703210GC(A)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703210YGC(A)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703210GK(A)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703210YGK(A)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD70F3210GC(A)-8BT	80-pin plastic QFP (14 × 14)	Special
μPD70F3210YGC(A)-8BT	80-pin plastic QFP (14 × 14)	Special
μPD70F3210GK(A)-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD70F3210YGK(A)-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special

Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

★ **(2) (A1) grade products, (A2) grade products**

Part Number	Package	Quality Grade
μPD703208GC(A1)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703208YGC(A1)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703208GK(A1)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703208YGK(A1)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703209GC(A1)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703209YGC(A1)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703209GK(A1)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703209YGK(A1)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703210GC(A1)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703210YGC(A1)-×××-8BT	80-pin plastic QFP (14 × 14)	Special
μPD703210GK(A1)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703210YGK(A1)-×××-9EU	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703208GC(A2)-×××-8BT[Note]	80-pin plastic QFP (14 × 14)	Special
μPD703208YGC(A2)-×××-8BT[Note]	80-pin plastic QFP (14 × 14)	Special
μPD703208GK(A2)-×××-9EU[Note]	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703208YGK(A2)-×××-9EU[Note]	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703209GC(A2)-×××-8BT[Note]	80-pin plastic QFP (14 × 14)	Special
μPD703209YGC(A2)-×××-8BT[Note]	80-pin plastic QFP (14 × 14)	Special
μPD703209GK(A2)-×××-9EU[Note]	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703209YGK(A2)-×××-9EU[Note]	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703210GC(A2)-×××-8BT[Note]	80-pin plastic QFP (14 × 14)	Special
μPD703210YGC(A2)-×××-8BT[Note]	80-pin plastic QFP (14 × 14)	Special
μPD703210GK(A2)-×××-9EU[Note]	80-pin plastic TQFP (fine pitch) (12 × 12)	Special
μPD703210YGK(A2)-×××-9EU[Note]	80-pin plastic TQFP (fine pitch) (12 × 12)	Special

Note Under development

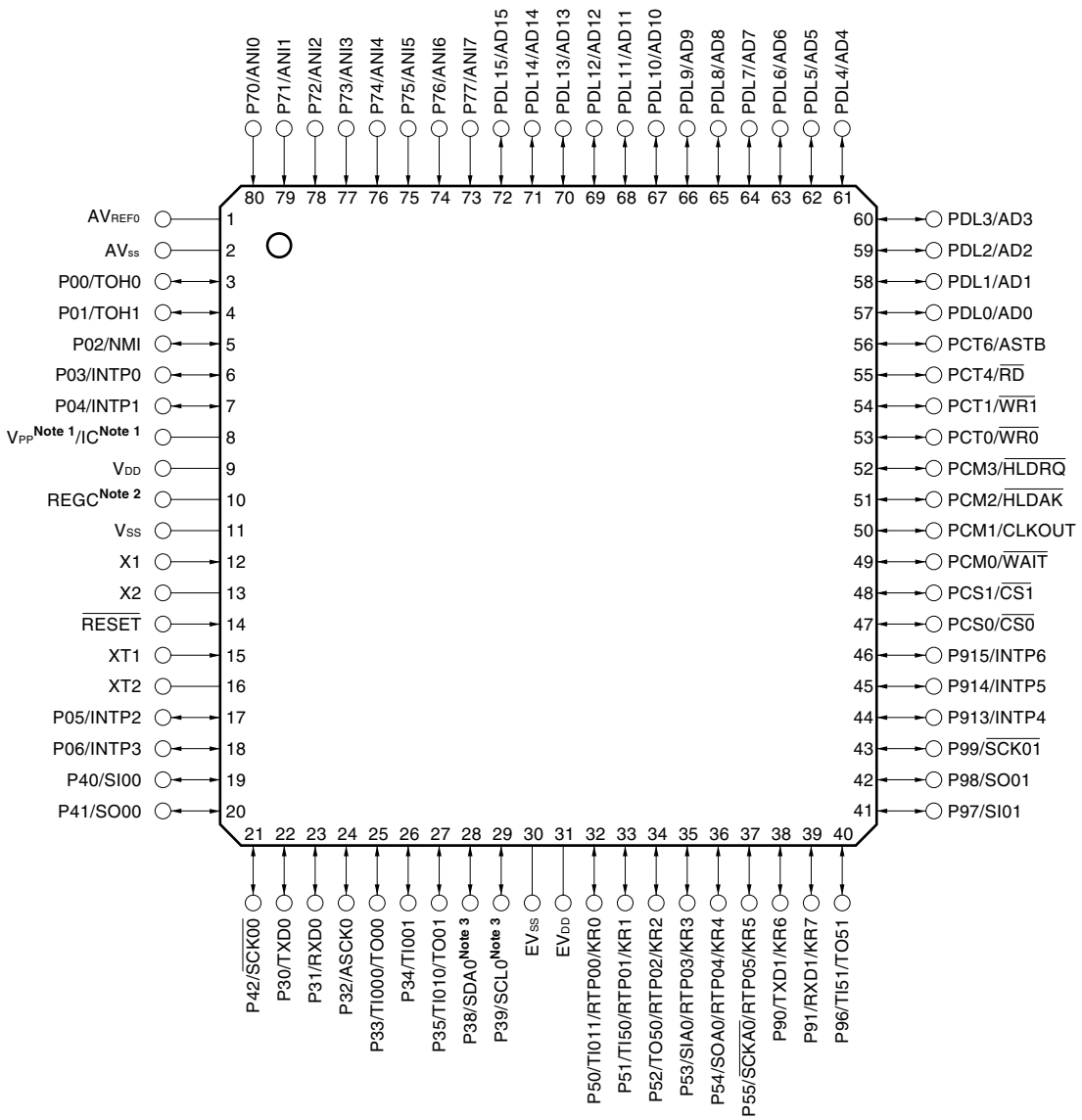
Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

1.2.4 Pin configuration (top view) (V850ES/KF1)

80-pin plastic QFP (14 × 14)
80-pin plastic TQFP (fine pitch) (12 × 12)

- μPD703208GC-×××-8BT
- μPD703208YGC-×××-8BT
- μPD703208GK-×××-9EU
- μPD703208YGK-×××-9EU
- μPD703209GC-×××-8BT
- μPD703209YGC-×××-8BT
- μPD703208GK(A)-×××-9EU
- μPD703208YGK(A)-×××-9EU
- μPD703209GC(A)-×××-8BT
- μPD703209YGC(A)-×××-8BT
- μPD703209GK(A)-×××-9EU
- μPD703209YGK(A)-×××-9EU
- μPD703209GK-×××-9EU
- μPD703209YGK-×××-9EU
- μPD703210GC-×××-8BT
- μPD703210YGC-×××-8BT
- μPD703210GK-×××-9EU
- μPD703210YGK-×××-9EU
- μPD703210GC(A)-×××-8BT
- μPD703210YGC(A)-×××-8BT
- μPD703210GK(A)-×××-9EU
- μPD703210YGK(A)-×××-9EU
- μPD70F3210GC(A)-8BT
- μPD70F3210YGC(A)-8BT
- μPD70F3210GC-8BT
- μPD70F3210YGC-8BT
- μPD70F3210GK-9EU
- μPD70F3210YGK-9EU
- μPD703208GC(A)-×××-8BT
- μPD703208YGC(A)-×××-8BT
- μPD70F3210GK(A)-9EU
- μPD70F3210YGK(A)-9EU
- μPD703208GC(A1)-×××-8BT
- μPD703208YGC(A1)-×××-8BT
- μPD703208GK(A1)-×××-9EU
- μPD703208YGK(A1)-×××-9EU
- μPD703209GC(A1)-×××-8BT
- μPD703209YGC(A1)-×××-8BT
- μPD703209GK(A1)-×××-9EU
- μPD703209YGK(A1)-×××-9EU
- μPD703210GC(A1)-×××-8BT
- μPD703210YGC(A1)-×××-8BT
- μPD703210GK(A1)-×××-9EU
- μPD703210YGK(A1)-×××-9EU
- μPD703208GC(A2)-×××-8BT
- μPD703208YGC(A2)-×××-8BT
- μPD703208GK(A2)-×××-9EU
- μPD703208YGK(A2)-×××-9EU
- μPD703209GC(A2)-×××-8BT
- μPD703209YGC(A2)-×××-8BT
- μPD703209GK(A2)-×××-9EU
- μPD703209YGK(A2)-×××-9EU
- μPD703210GC(A2)-×××-8BT
- μPD703210YGC(A2)-×××-8BT
- μPD703210GK(A2)-×××-9EU
- μPD703210YGK(A2)- ×××-9EU



Notes 1. IC: Connect directly to V_{SS} (μPD703208, 703208Y, 703209, 703209Y, 703210, 703210Y).
V_{PP}: Connect to V_{SS} in normal operation mode (μPD70F3210, 70F3210Y).

2. When using a regulator, connect the REGC pin to V_{SS} via a 10 pF capacitor.
When not using a regulator, connect the REGC pin directly to V_{DD}.

3. SCL0 and SDA0 can be used only in the μPD703208Y, 703209Y, 703210Y, and 70F3210Y.

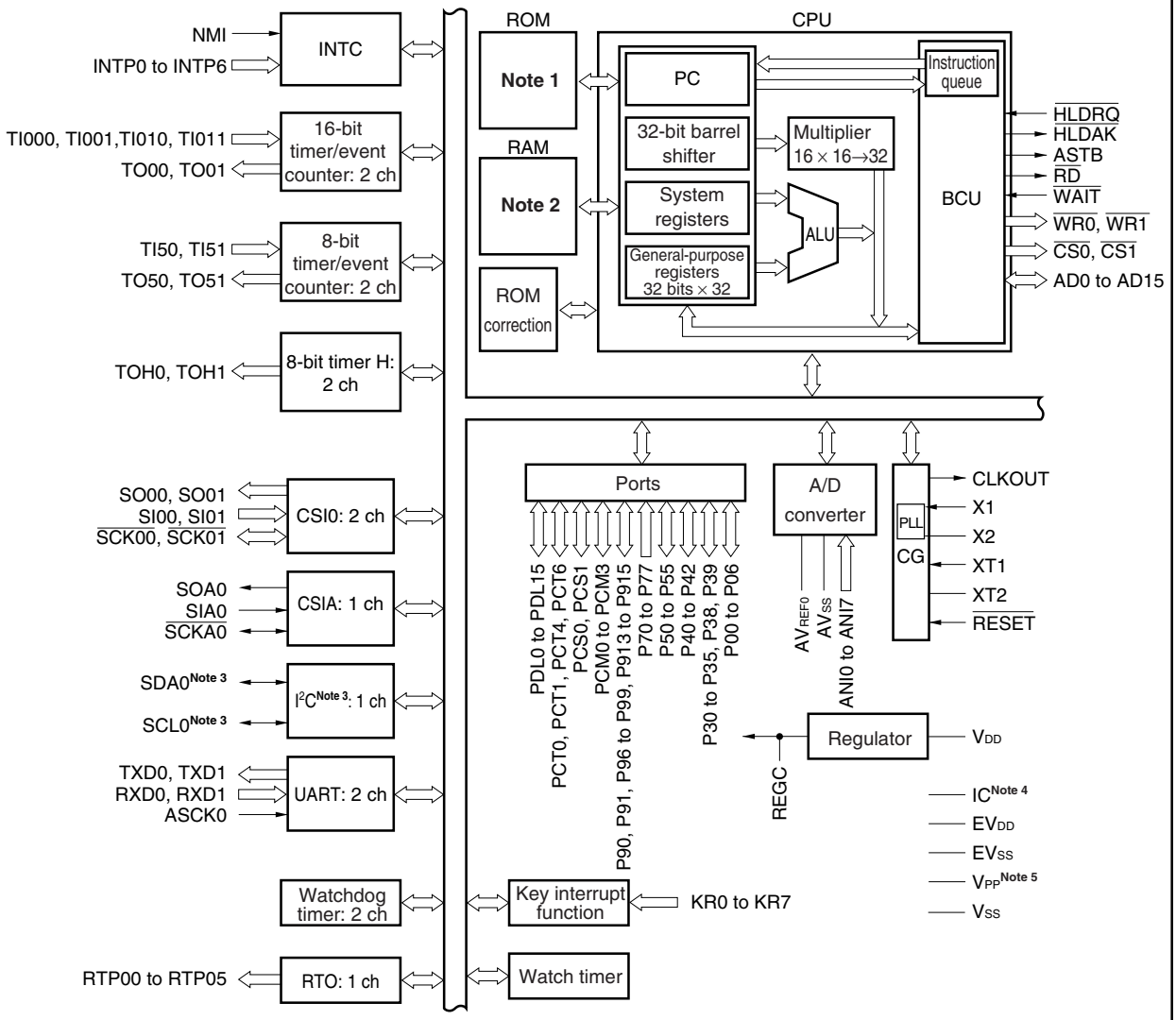
Caution Make EV_{DD} the same potential as V_{DD}.

Pin identification (V850ES/KF1)

AD0 to AD15:	Address/data bus	$\overline{RD}$:	Read strobe
ANI0 to ANI7:	Analog input	REGC:	Regulator control
ASCK0:	Asynchronous serial clock	$\overline{RESET}$:	Reset
ASTB:	Address strobe	RTP00 to RTP05:	Real-time output port
AV_{REF0}:	Analog reference voltage	RXD0, RXD1:	Receive data
AV_{SS}:	Ground for analog	$\overline{SCK00}$, $\overline{SCK01}$,	
CLKOUT:	Clock output	$\overline{SCKA0}$:	Serial clock
$\overline{CS0}$, $\overline{CS1}$:	Chip select	SCL0:	Serial clock
EV_{DD}:	Power supply for port	SDA0:	Serial data
EV_{SS}:	Ground for port	SI00, SI01,	
$\overline{HLDAK}$:	Hold acknowledge	SIA0:	Serial input
$\overline{HLDRQ}$:	Hold request	SO00, SO01,	
IC:	Internally connected	SOA0:	Serial output
INTP0 to INTP6:	External interrupt input	TI000, TI001,	
KR0 to KR7:	Key return	TI010, TI011,	
NMI:	Non-maskable interrupt request	TI50, TI51:	Timer input
P00 to P06:	Port 0	TO00, TO01,	
P30 to P35, P38, P39:	Port 3	TO50, TO51,	
P40 to P42:	Port 4	TOH0, TOH1:	Timer output
P50 to P55:	Port 5	TXD0, TXD1:	Transmit data
P70 to P77:	Port 7	V_{DD}:	Power supply
P90, P91, P96 to P99,:	Port 9	V_{PP}:	Programming power supply
P913 to P915		V_{SS}:	Ground
PCM0 to PCM3:	Port CM	$\overline{WAIT}$:	Wait
PCS0, PCS1:	Port CS	$\overline{WR0}$:	Lower byte write strobe
PCT0, PCT1,		$\overline{WR1}$:	Upper byte write strobe
PCT4, PCT6:	Port CT	X1, X2:	Crystal for main clock
PDL0 to PDL15:	Port DL	XT1, XT2:	Crystal for subclock

1.2.5 Function block configuration (V850ES/KF1)

(1) Internal block diagram



Notes 1. μPD703208, 703208Y: 64 KB (mask ROM)
μPD703209, 703209Y: 96 KB (mask ROM)
μPD703210, 703210Y: 128 KB (mask ROM)
μPD70F3210, 70F3210Y: 128 KB (flash memory)

2. μPD703208, 703208Y, 703209, 703209Y: 4 KB
μPD703210, 703210Y, 70F3210, 70F3210Y: 6 KB

3. Only in the μPD703208Y, 703209Y, 703210Y, and 70F3210Y

4. Only in the μPD703208, 703208Y, 703209, 703209Y, 703210, and 703210Y

5. Only in the μPD70F3210 and 70F3210Y

(2) Internal units

(a) CPU

The CPU uses five-stage pipeline control to enable single-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other types of instruction processing.

Other dedicated on-chip hardware, such as a multiplier (16 bits × 16 bits → 32 bits) and a barrel shifter (32 bits) help accelerate complex processing.

(b) Bus control unit (BCU)

The BCU starts a required external bus cycle based on the physical address obtained by the CPU.

When an instruction is fetched from external memory space and the CPU does not send a bus cycle start request, the BCU generates a prefetch address and prefetches the instruction code. The prefetched instruction code is stored in an internal instruction queue.

(c) ROM

This consists of a 128 KB, 96 KB, or 64 KB mask ROM or flash memory mapped to the address spaces from 0000000H to 001FFFFH, 0000000H to 0017FFFH, or 0000000H to 000FFFFH, respectively.

ROM can be accessed by the CPU in one clock cycle during instruction fetch.

(d) RAM

This consists of a 6 KB or 4 KB RAM mapped to the address spaces from 3FFD800H to 3FFEFFFH or 3FFE000H to 3FFEFFFH, respectively.

RAM can be accessed by the CPU in one clock cycle during data access.

(e) Interrupt controller (INTC)

This controller handles hardware interrupt requests (NMI, INTP0 to INTP6) from on-chip peripheral hardware and external hardware. Eight levels of interrupt priorities can be specified for these interrupt requests, and multiplexed servicing control can be performed.

(f) Clock generator (CG)

A main clock oscillator and subclock oscillator are provided and generate the main clock oscillation frequency (f_X) and subclock frequency (f_{XT}), respectively.

There are two modes: In the clock-through mode, f_X is used as the main clock frequency (f_{XX}) as is. In the PLL mode, f_X is used multiplied by 4.

The CPU clock frequency (f_{CPU}) can be selected from among f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, and f_{XT}.

(g) Timer/counter

Two 16-bit timer/event counter channels and two 8-bit timer/event counter channels are incorporated, enabling measurement of pulse intervals and frequency as well as programmable pulse output.

Two 8-bit timer/event counters can be connected in cascade to configure a 16-bit timer.

Two 8-bit timer channels enabling programmable pulse output are provided on chip.

(h) Watch timer

This timer counts the reference time (0.5 seconds) for counting the clock from the subclock (32.768 kHz) or f_{BRG} (32.768 kHz) from the clock generator. At the same time, the watch timer can be used as an interval timer.

(i) Watchdog timer

Two watchdog timer channels are provided on chip to detect program loops and system abnormalities. Watchdog timer 1 can be used as an interval timer. When used as a watchdog timer, it generates a non-maskable interrupt request signal (INTWDT1) or system reset signal (WDTRES1) after an overflow occurs. When used as an interval timer, it generates a maskable interrupt request (INTWDTM1) after an overflow occurs.

Watchdog timer 2 operates by default following reset release.

It generates a non-maskable interrupt request signal (INTWDT2) or system reset signal (WDTRES2) after an overflow occurs.

(j) Serial interface

The V850ES/KF1 includes four kinds of serial interfaces: an asynchronous serial interface (UARTn), a clocked serial interface (CSI0n), a clocked serial interface with an automatic transmit/receive function (CSIA0), and an I^2C bus interface (I^2C0). The μPD703208, 703209, 703210, and 70F3210 can simultaneously use up to five channels, and the μPD703208Y, 703209Y, 703210Y, and 70F3210Y up to six channels.

For UARTn, data is transferred via the TXDn and RXDn pins.

For CSI0n, data is transferred via the SO0n, SI0n, and $\overline{\text{SCK0n}}$ pins.

For CSIA0, data is transferred via the SOA0, SIA0, and $\overline{\text{SCKA0}}$ pins.

For I^2C0, data is transferred via the SDA0 and SCL0 pins.

I^2C0 is provided only in the μPD703208Y, 703209Y, 703210Y, and 70F3210Y.

Remark n = 0, 1

(k) A/D converter

This 10-bit A/D converter includes 8 analog input pins. Conversion is performed using the successive approximation method.

(l) ROM correction

This function is used to replace part of a program in the mask ROM with that contained in the internal RAM. Up to four correction addresses can be specified.

(m) Key interrupt function

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins.

(n) Real-time output function

This function transfers 6-bit data set beforehand to output latches upon occurrence of a timer compare register match signal.

For the V850ES/KF1, a 1-channel 6-bit data real-time output function is provided on chip.

(o) Ports

As shown below, the following ports have general-purpose port functions and control pin functions.

Port	I/O	Alternate Function
P0	7-bit I/O	NMI, external interrupt, timer output
P3	8-bit I/O	Serial interface, timer I/O
P4	3-bit I/O	Serial interface
P5	6-bit I/O	Serial interface, timer I/O, key interrupt function, real-time output function
P7	8-bit input	A/D converter analog input
P9	9-bit I/O	Serial interface, timer I/O, external interrupt, key interrupt function
PCM	4-bit I/O	External bus control signal
PCS	2-bit I/O	Chip select output
PCT	4-bit I/O	External bus control signal
PDL	16-bit I/O	External address/data bus

1.3 V850ES/KG1

1.3.1 Features (V850ES/KG1)

- Minimum instruction execution time: 50 ns (operation at main clock (fxx) = 20 MHz)
- General-purpose registers: 32 bits × 32 registers
- CPU feature: Signed multiplication (16 × 16 → 32): 1 to 2 clocks
  (Instructions without creating register hazards can be continuously executed in parallel)
  Saturated operations (overflow and underflow detection functions are included)
  32-bit shift instruction: 1 clock
  Bit manipulation instructions
  Load/store instructions with long/short format
- Memory space: 64 MB of linear address space
  Memory block division function: 2 MB, 2 MB (Total of 2 blocks)
  - External bus interface
    μPD703212, 703212Y (Mask ROM: 64 KB/RAM: 4 KB)
    μPD703213, 703213Y (Mask ROM: 96 KB/RAM: 4 KB)
    μPD703214, 703214Y (Mask ROM: 128 KB/RAM: 6 KB)
    μPD70F3214, 70F3214Y (Flash memory: 128 KB/RAM: 6 KB)
  - Internal memory
    16-bit data bus
    Address bus: Separate output possible
- Interrupts and exceptions
  Non-maskable interrupts: 3 sources
  Maskable interrupts: 35 sources (μPD703212, 703213, 703214, 70F3214)
  36 sources (μPD703212Y, 703213Y, 703214Y, 70F3214Y)
  Software exceptions: 32 sources
  Exception trap: 1 source
- I/O lines: Total: 84
- Key interrupt function
- Timer function
  16-bit timer/event counter: 4 channels
  8-bit timer/event counter: 2 channels
  8-bit timer H: 2 channels
  8-bit interval timer BRG: 1 channel
  Watch timer/interval timer: 1 channel
  Watchdog timers
    Watchdog timer 1 (also usable as oscillation stabilization timer): 1 channel
    Watchdog timer 2: 1 channel
- Serial interface
  Asynchronous serial interface (UART): 2 channels
  3-wire serial I/O (CSI0): 2 channels
  3-wire serial I/O (with automatic transmit/receive function) (CSIA): 2 channels
  I^2C bus interface (I^2C): 1 channel
  (μPD703212Y, 703213Y, 703214Y, 70F3214Y)
- A/D converter: 10-bit resolution × 8 channels
- D/A converter: 8-bit resolution × 2 channels
- Real-time output port: 6 bits × 1 channel

- Power-save functions: HALT/IDLE/STOP modes, subclock/sub-IDLE modes
- ROM correction: 4 correction addresses specifiable
- Packages: 100-pin plastic LQFP (fine pitch) (14 × 14)

1.3.2 Applications (V850ES/KG1)

- Automotive
  - System control of body electrical system (power windows, keyless entry reception, etc.)
  - Submicrocontroller of control system
- Home audio, car audio
- AV equipment
- PC peripheral devices (keyboards, etc.)
- Household appliances
  - Outdoor units of air conditioners
  - Microwave ovens, rice cookers
- Industrial devices
  - Pumps
  - Vending machines
  - FA

1.3.3 Ordering information (V850ES/KG1)

(1) Standard products, (A) grade products

Part Number	Package	Quality Grade
μPD703212GC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μPD703212YGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μPD703213GC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μPD703213YGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μPD703214GC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μPD703214YGC-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μPD70F3214GC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μPD70F3214YGC-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Standard
μPD703212GC(A)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703212YGC(A)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703213GC(A)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703213YGC(A)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703214GC(A)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703214YGC(A)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD70F3214GC(A)-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD70F3214YGC(A)-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special

Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

★ **(2) (A1) grade products, (A2) grade products**

Part Number	Package	Quality Grade
μPD703212GC(A1)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703212YGC(A1)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703213GC(A1)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703213YGC(A1)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703214GC(A1)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703214YGC(A1)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703212GC(A2)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703212YGC(A2)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703213GC(A2)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703213YGC(A2)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703214GC(A2)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special
μPD703214YGC(A2)-×××-8EU	100-pin plastic LQFP (fine pitch) (14 × 14)	Special

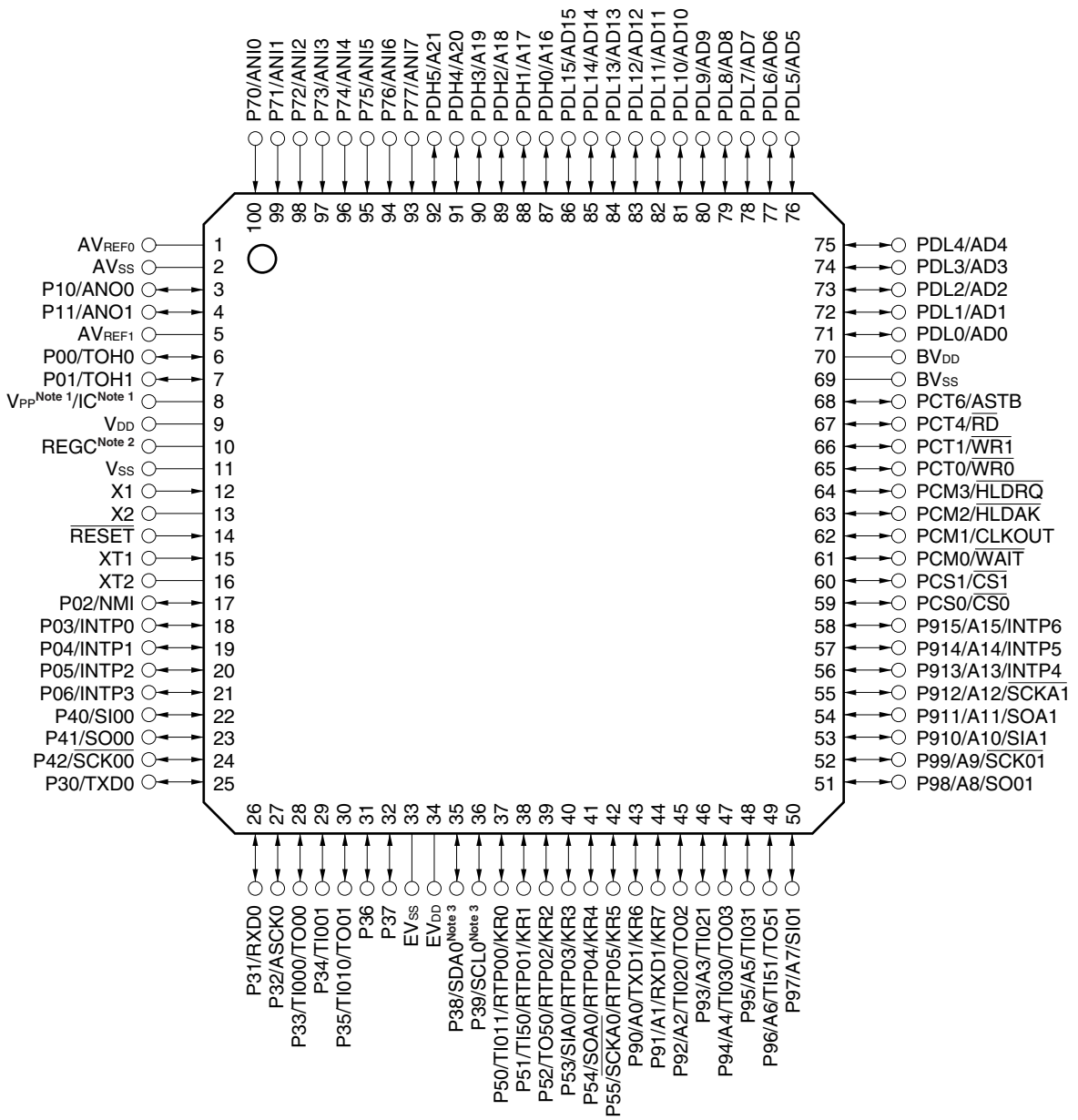
Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

1.3.4 Pin configuration (top view) (V850ES/KG1)

100-pin plastic LQFP (fine pitch) (14 × 14)

μPD703212GC-×××-8EU
μPD703212YGC-×××-8EU
μPD703213GC-×××-8EU
μPD703213YGC-×××-8EU
μPD703214GC-×××-8EU
μPD703214YGC-×××-8EU
μPD70F3214GC-8EU
μPD70F3214YGC-8EU
μPD703212GC(A)-×××-8EU
μPD703212YGC(A)-×××-8EU
μPD703213GC(A)-×××-8EU
μPD703213YGC(A)-×××-8EU
μPD703214GC(A)-×××-8EU
μPD703214YGC(A)-×××-8EU
μPD70F3214GC(A)-8EU
μPD70F3214YGC(A)-8EU
μPD703212GC(A1)-×××-8EU
μPD703212YGC(A1)-×××-8EU
μPD703213GC(A1)-×××-8EU
μPD703213YGC(A1)-×××-8EU
μPD703214GC(A1)-×××-8EU
μPD703214YGC(A1)-×××-8EU
μPD703212GC(A2)-×××-8EU
μPD703212YGC(A2)-×××-8EU
μPD703213GC(A2)-×××-8EU
μPD703213YGC(A2)-×××-8EU
μPD703214GC(A2)-×××-8EU
μPD703214YGC(A2)-×××-8EU



Notes 1. IC: Connect directly to V_{SS} (μPD703212, 703212Y, 703213, 703213Y, 703214, 703214Y).
V_{PP}: Connect to V_{SS} in normal operation mode (μPD70F3214, 70F3214Y).

2. When using a regulator, connect the REGC pin to V_{SS} via a 10 pF capacitor.
When not using a regulator, connect the REGC pin directly to V_{DD}.

3. SCL0 and SDA0 can be used only in the μPD703212Y, 703213Y, 703214Y, and 70F3214Y.

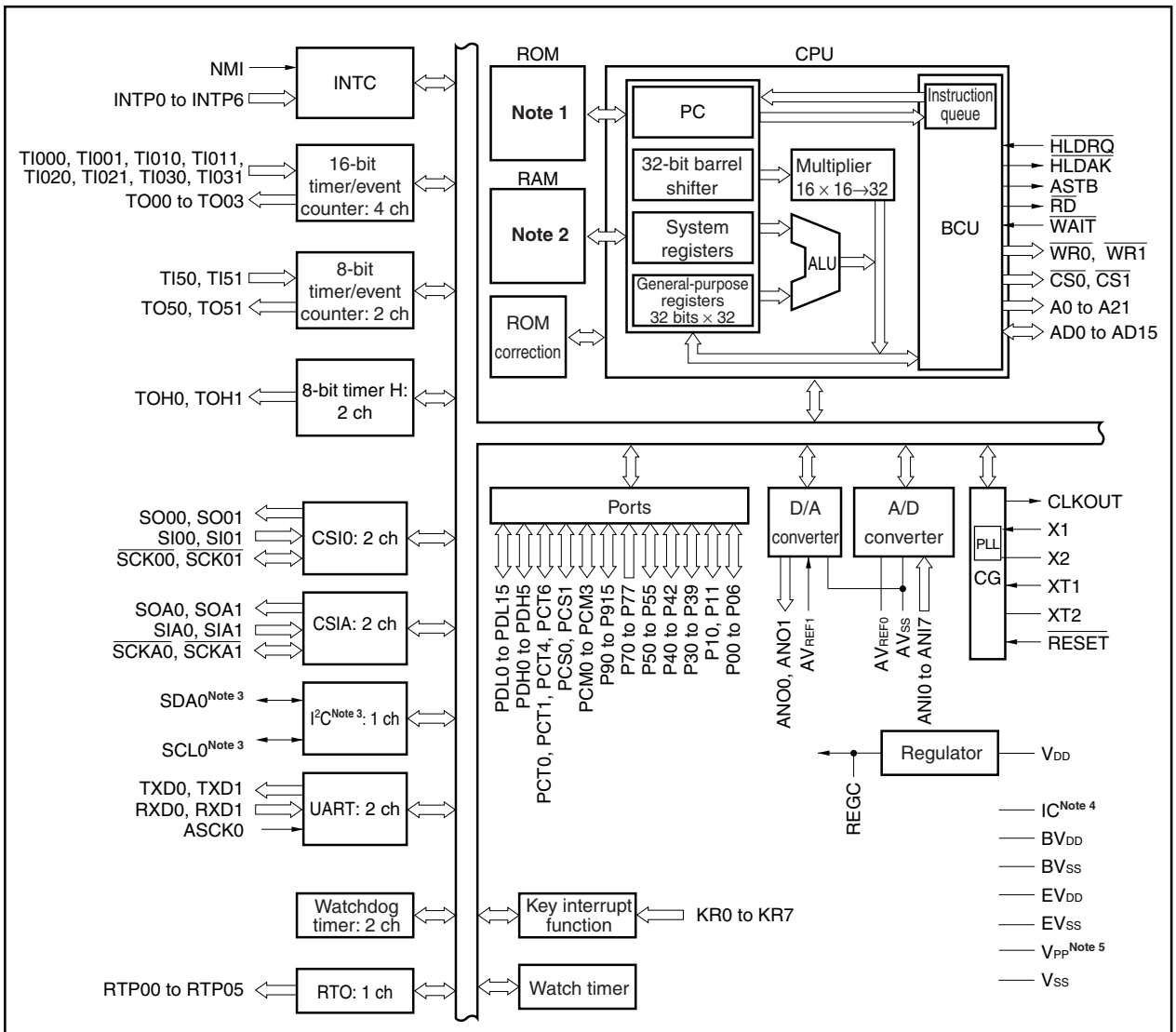
Caution Make EV_{DD} the same potential as V_{DD}.
BV_{DD} can be used when $V_{DD} = EV_{DD} \geq BV_{DD}$.

Pin identification (V850ES/KG1)

A0 to A21:	Address bus
AD0 to AD15:	Address/data bus
ANI0 to ANI7:	Analog input
ANO0, ANO1:	Analog output
ASCK0:	Asynchronous serial clock
ASTB:	Address strobe
AV_{REF0}, AV_{REF1}:	Analog reference voltage
AV_{SS}:	Ground for analog
BV_{DD}:	Power supply for bus interface
BV_{SS}:	Ground for bus interface
CLKOUT:	Clock output
$\overline{CS0}$, $\overline{CS1}$:	Chip select
EV_{DD}:	Power supply for port
EV_{SS}:	Ground for port
$\overline{HLDAK}$:	Hold acknowledge
$\overline{HLDRQ}$:	Hold request
IC:	Internally connected
INTP0 to INTP6:	External interrupt input
KR0 to KR7:	Key return
NMI:	Non-maskable interrupt request
P00 to P06:	Port 0
P10, P11:	Port 1
P30 to P39:	Port 3
P40 to P42:	Port 4
P50 to P55:	Port 5
P70 to P77:	Port 7
P90 to P915:	Port 9
PCM0 to PCM3:	Port CM
PCS0, PCS1:	Port CS
PCT0, PCT1, PCT4, PCT6:	Port CT
PDH0 to PDH5:	Port DH
PDL0 to PDL15:	Port DL
$\overline{RD}$:	Read strobe
REGC:	Regulator control
$\overline{RESET}$:	Reset
RTP00 to RTP05:	Real-time output port
RXD0, RXD1:	Receive data
$\overline{SCK00}$, $\overline{SCK01}$, $\overline{SCKA0}$, $\overline{SCKA1}$:	Serial clock
SCL0:	Serial clock
SDA0:	Serial data
SI00, SI01, SIA0, SIA1:	Serial input
SO00, SO01, SOA0, SOA1:	Serial output
TI000, TI001, TI010, TI011, TI020, TI021, TI030, TI031, TI50, TI51:	Timer input
TO00 to TO03, TO50, TO51, TOH0, TOH1:	Timer output
TXD0, TXD1:	Transmit data
V_{DD}:	Power supply
V_{PP}:	Programming power supply
V_{SS}:	Ground
$\overline{WAIT}$:	Wait
$\overline{WR0}$:	Lower byte write strobe
$\overline{WR1}$:	Upper byte write strobe
X1, X2:	Crystal for main clock
XT1, XT2:	Crystal for subclock

1.3.5 Function block configuration (V850ES/KG1)

(1) Internal block diagram



Notes 1. μPD703212, 703212Y: 64 KB (mask ROM)
μPD703213, 703213Y: 96 KB (mask ROM)
μPD703214, 703214Y: 128 KB (mask ROM)
μPD70F3214, 70F3214Y: 128 KB (flash memory)

2. μPD703212, 703212Y, 703213, 703213Y: 4 KB
μPD703214, 703214Y, 70F3214, 70F3214Y: 6 KB

3. Only in the μPD703212Y, 703213Y, 703214Y, and 70F3214Y

4. Only in the μPD703212, 703212Y, 703213, 703213Y, 703214, and 703214Y

5. Only in the μPD70F3214 and 70F3214Y

(2) Internal units

(a) CPU

The CPU uses five-stage pipeline control to enable single-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other types of instruction processing.

Other dedicated on-chip hardware, such as a multiplier (16 bits × 16 bits → 32 bits) and a barrel shifter (32 bits) help accelerate complex processing.

(b) Bus control unit (BCU)

The BCU starts a required external bus cycle based on the physical address obtained by the CPU.

When an instruction is fetched from external memory space and the CPU does not send a bus cycle start request, the BCU generates a prefetch address and prefetches the instruction code. The prefetched instruction code is stored in an internal instruction queue.

(c) ROM

This consists of a 128 KB, 96 KB, or 64 KB mask ROM or flash memory mapped to the address spaces from 0000000H to 001FFFFH, 0000000H to 0017FFFH, or 0000000H to 000FFFFH, respectively.

ROM can be accessed by the CPU in one clock cycle during instruction fetch.

(d) RAM

This consists of a 6 KB or 4 KB RAM mapped to the address spaces from 3FFD800H to 3FFEFFFH or 3FFE000H to 3FFEFFFH, respectively.

RAM can be accessed by the CPU in one clock cycle during data access.

(e) Interrupt controller (INTC)

This controller handles hardware interrupt requests (NMI, INTP0 to INTP6) from on-chip peripheral hardware and external hardware. Eight levels of interrupt priorities can be specified for these interrupt requests, and multiplexed servicing control can be performed.

(f) Clock generator (CG)

A main clock oscillator and subclock oscillator are provided and generate the main clock oscillation frequency (f_X) and subclock frequency (f_{XT}), respectively.

There are two modes: In the clock-through mode, f_X is used as the main clock frequency (f_{XX}) as is. In the PLL mode, f_X is used multiplied by 4.

The CPU clock frequency (f_{CPU}) can be selected from among f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, and f_{XT}.

(g) Timer/counter

Four 16-bit timer/event counter channels and two 8-bit timer/event counter channels are incorporated, enabling measurement of pulse intervals and frequency as well as programmable pulse output.

Two 8-bit timer/event counters can be connected in cascade to configure a 16-bit timer.

Two 8-bit timer channels enabling programmable pulse output are provided on chip.

(h) Watch timer

This timer counts the reference time (0.5 seconds) for counting the clock from the subclock (32.768 kHz) or f_{BRG} (32.768 kHz) from the clock generator. At the same time, the watch timer can be used as an interval timer.

(i) Watchdog timer

Two watchdog timer channels are provided on chip to detect program loops and system abnormalities. Watchdog timer 1 can be used as an interval timer. When used as a watchdog timer, it generates a non-maskable interrupt request signal (INTWDT1) or system reset (WDTRES1) after an overflow occurs. When used as an interval timer, it generates a maskable interrupt request signal (INTWDTM1) after an overflow occurs.

Watchdog timer 2 operates by default following reset release.

It generates a non-maskable interrupt request signal (INTWDT2) or system reset signal (WDTRES2) after an overflow occurs.

(j) Serial interface (SIO)

The V850ES/KG1 includes four kinds of serial interfaces: an asynchronous serial interface (UARTn), a clocked serial interface (CSI0n), a clocked serial interface with an automatic transmit/receive function (CSIAn), and an I^2C bus interface (I^2C0). The μPD703212, 703213, 703214, and 70F3214 can simultaneously use up to six channels, and the μPD703212Y, 703213Y, 703214Y, and 70F3214Y up to seven channels.

For UARTn, data is transferred via the TXDn and RXDn pins.

For CSI0n, data is transferred via the SO0n, SI0n, and $\overline{SCK0n}$ pins.

For CSIA0, data is transferred via the SOAn, SIAn, and $\overline{SCKAn}$ pins.

For I^2C0, data is transferred via the SDA0 and SCL0 pins.

I^2C0 is provided only in the μPD703212Y, 703213Y, 703214Y, and 70F3214Y.

Remark n = 0, 1

(k) A/D converter

This high-speed, high-resolution 10-bit A/D converter includes 8 analog input pins. Conversion is performed using the successive approximation method.

(l) D/A converter

Two 8-bit resolution D/A converter channels are included on chip. The D/A converter uses the R-2R ladder method.

(m) ROM correction

This function is used to replace part of a program in the mask ROM with that contained in the internal RAM. Up to four correction addresses can be specified.

(n) Key interrupt function

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins.

(o) Real-time output function

This function transfers 6-bit data set beforehand to output latches upon occurrence of a timer compare register match signal.

For the V850ES/KG1, a 1-channel 6-bit data real-time output function is provided on chip.

(p) Ports

As shown below, the following ports have general-purpose port functions and control pin functions.

Port	I/O	Alternate Function
P0	7-bit I/O	NMI, external interrupt, timer output
P1	2-bit I/O	D/A converter analog output
P3	10-bit I/O	Serial interface, timer I/O
P4	3-bit I/O	Serial interface
P5	6-bit I/O	Serial interface, timer I/O, key interrupt function, real-time output function
P7	8-bit input	A/D converter analog input
P9	16-bit I/O	External address bus, serial interface, timer I/O, external interrupt, key interrupt function
PCM	4-bit I/O	External bus control signal
PCS	2-bit I/O	Chip select output
PCT	4-bit I/O	External bus control signal
PDH	6-bit I/O	External address bus
PDL	16-bit I/O	External address/data bus

1.4 V850ES/KJ1

1.4.1 Features (V850ES/KJ1)

- Minimum instruction execution time: 50 ns (operation at main clock (fxx) = 20 MHz)
- General-purpose registers: 32 bits × 32 registers
- CPU features: Signed multiplication (16 × 16 → 32): 1 to 2 clocks
  (Instructions without creating register hazards can be continuously executed in parallel)
  Saturated operations (overflow and underflow detection functions are included)
  32-bit shift instruction: 1 clock
  Bit manipulation instructions
  Load/store instructions with long/short format
- Memory space: 64 MB of linear address space
  Memory block division function: 2 MB, 2 MB, 4 MB, 8 MB (Total of 4 blocks)
  - External bus interface
    μPD703216, 703216Y (Mask ROM: 96 KB/RAM: 6 KB)
    μPD703217, 703217Y (Mask ROM: 128 KB/RAM: 6 KB)
    μPD70F3217, 70F3217Y (Flash memory: 128 KB/RAM: 6 KB)
  - Internal memory
    16-bit data bus
    Address bus: Separate output possible
- Interrupts and exceptions
  Non-maskable interrupts: 3 sources
  Maskable interrupts: 43 sources (μPD703216, 703217, 70F3217)
  45 sources (μPD703216Y, 703217Y, 70F3217Y)
  Software exceptions: 32 sources
  Exception trap: 1 source
- I/O lines: Total: 128
- Key interrupt function
- Timer function
  16-bit timer/event counter: 6 channels
  8-bit timer/event counter: 2 channels
  8-bit timer H: 2 channels
  8-bit interval timer BRG: 1 channel
  Watch timer/interval timer: 1 channel
  Watchdog timers
    Watchdog timer 1 (also usable as oscillation stabilization timer): 1 channel
    Watchdog timer 2: 1 channel
- Serial interface
  Asynchronous serial interface (UART): 3 channels
  3-wire serial I/O (CSI0): 3 channels
  3-wire serial I/O (with automatic transmit/receive function) (CSIA): 2 channels
  I^2C bus interface (I^2C): 2 channels
  (μPD703216Y, 703217Y, 70F3217Y)
- A/D converter: 10-bit resolution × 16 channels
- D/A converter: 8-bit resolution × 2 channels
- Real-time output port: 6 bit × 2 channels

- Power-save functions: HALT/IDLE/STOP modes, subclock/sub-IDLE modes
- ROM correction: 4 correction addresses specifiable
- Packages: 144-pin plastic LQFP (fine pitch) (20 × 20)

1.4.2 Applications (V850ES/KJ1)

- Automotive
  - System control of body electrical system (power windows, keyless entry reception, etc.)
  - Submicrocontroller of control system
- Home audio, car audio
- AV equipment
- PC peripheral devices (keyboards, etc.)
- Household appliances
  - Outdoor units of air conditioners
  - Microwave ovens, rice cookers
- Industrial devices
  - Pumps
  - Vending machines
  - FA

1.4.3 Ordering information (V850ES/KJ1)

(1) Standard products, (A1) grade products

Part Number	Package	Quality Grade
μPD703216GJ-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Standard
μPD703216YGJ-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Standard
μPD703217GJ-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Standard
μPD703217YGJ-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Standard
μPD70F3217GJ-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Standard
μPD70F3217YGJ-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Standard
μPD703216GJ(A)-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD703216YGJ(A)-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD703217GJ(A)-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD703217YGJ(A)-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD70F3217GJ(A)-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD70F3217YGJ(A)-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special

Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

★ **(2) Standard products, (A1) grade products**

Part Number	Package	Quality Grade
μPD703216GJ(A1)-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD703216YGJ(A1)-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD703217GJ(A1)-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD703217YGJ(A1)-×××-UEN	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD703216GJ(A2)-×××-UEN[Note]	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD703216YGJ(A2)-×××-UEN[Note]	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD703217GJ(A2)-×××-UEN[Note]	144-pin plastic LQFP (fine pitch) (20 × 20)	Special
μPD703217YGJ(A2)-×××-UEN[Note]	144-pin plastic LQFP (fine pitch) (20 × 20)	Special

Note Under development

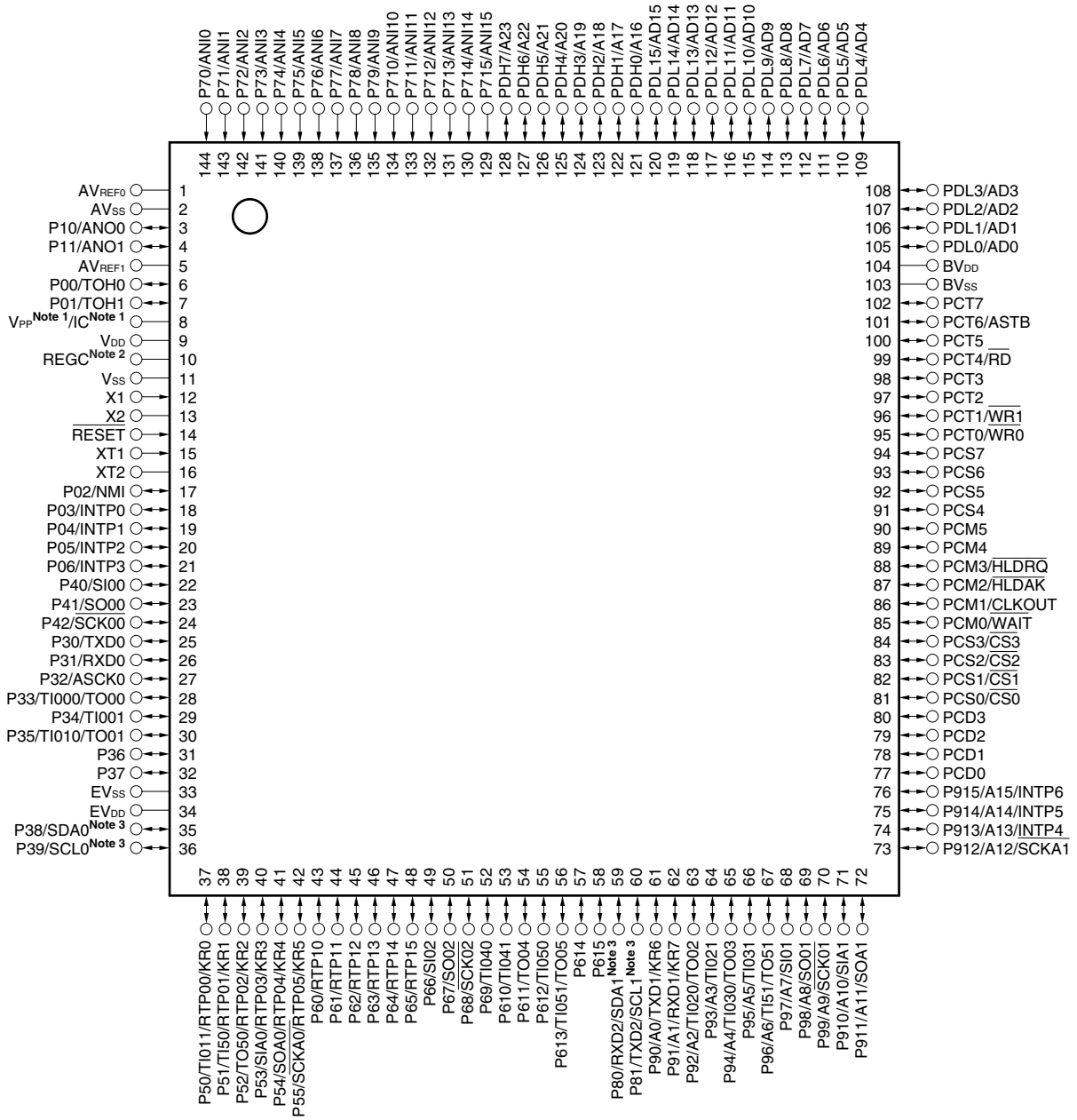
Remark ××× indicates ROM code suffix.

Please refer to "Quality Grades on NEC Semiconductor Devices" (Document No. C11531E) published by NEC Electronics Corporation to know the specification of the quality grade on the device and its recommended applications.

1.4.4 Pin configuration (top view) (V850ES/KJ1)

144-pin plastic LQFP (fine pitch) (20 × 20)

- μPD703216GJ-×××-UEN
- μPD703216YGJ-×××-UEN
- μPD703217GJ-×××-UEN
- μPD703217YGJ-×××-UEN
- μPD70F3217GJ-UEN
- μPD70F3217YGJ-UEN
- μPD703216GJ(A)-×××-UEN
- μPD703216YGJ(A)-×××-UEN
- μPD703217GJ(A)-×××-UEN
- μPD703217YGJ(A)-×××-UEN
- μPD70F3217GJ(A)-UEN
- μPD70F3217YGJ(A)-UEN
- μPD703216GJ(A1)-×××-UEN
- μPD703216YGJ(A1)-×××-UEN
- μPD703217GJ(A1)-×××-UEN
- μPD703217YGJ(A1)-×××-UEN
- μPD703216GJ(A2)-×××-UEN
- μPD703216YGJ(A2)-×××-UEN
- μPD703217GJ(A2)-×××-UEN
- μPD703217YGJ(A2)-×××-UEN



Notes 1. IC: Connect directly to V_{SS} (μPD703216, 703216Y, 703217, 703217Y).
V_{PP}: Connect to V_{SS} in normal operation mode (μPD70F3217, 70F3217Y).

2. When using a regulator, connect the REGC pin to V_{SS} via a 10 pF capacitor.
When not using a regulator, connect the REGC pin directly to V_{DD}.

3. SCL0, SDA0, SCL1, and SDA1 can be used only in the μPD703216Y, 703217Y, and 70F3217Y.

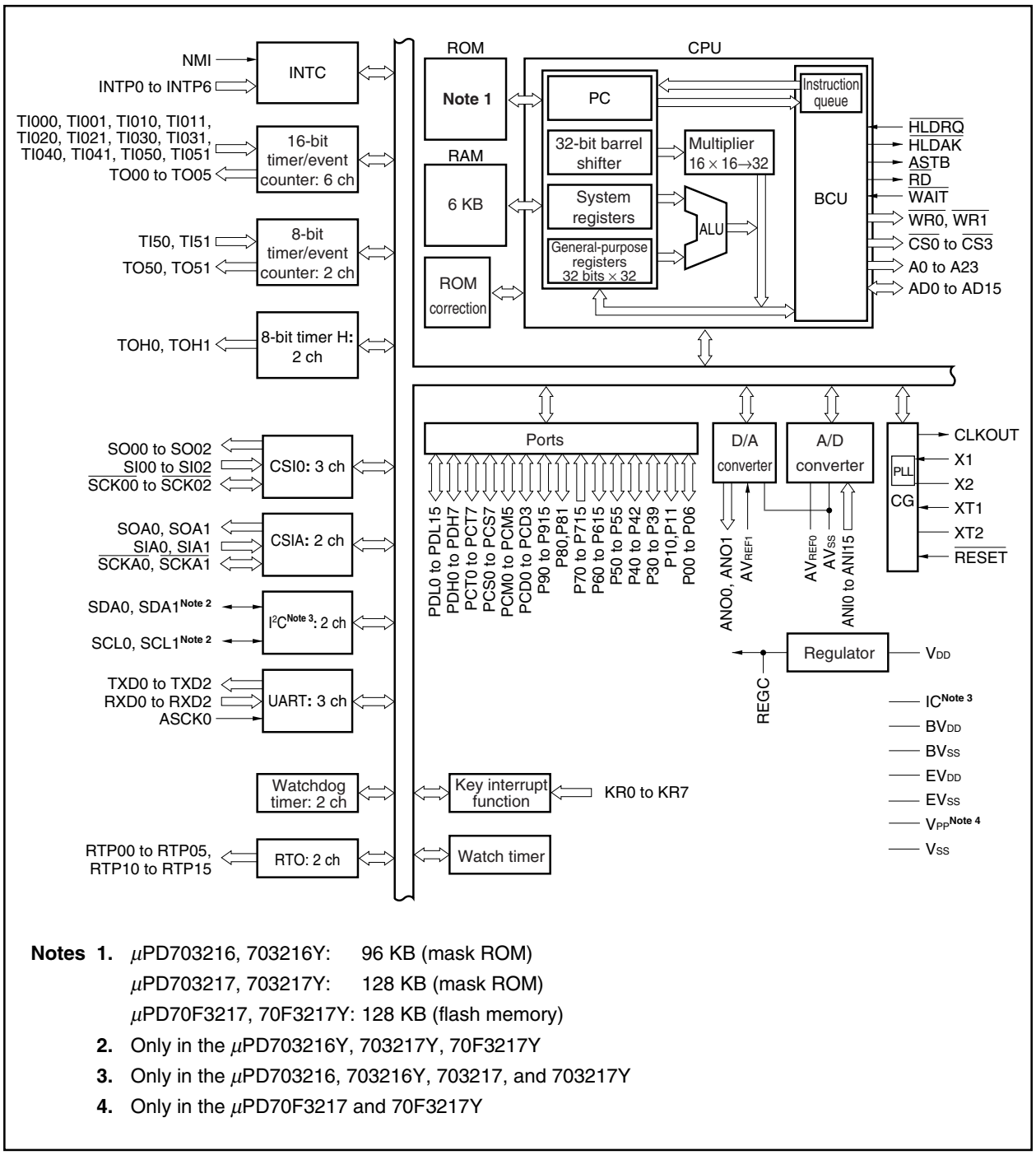
Caution Make EV_{DD} the same potential as V_{DD}.
BV_{DD} can be used when $V_{DD} = EV_{DD} \geq BV_{DD}$.

Pin identification (V850ES/KJ1)

A0 to A23:	Address bus	PDL0 to PDL15:	Port DL
AD0 to AD15:	Address/data bus	$\overline{RD}$:	Read strobe
ANI0 to ANI15:	Analog input	REGC:	Regulator control
ANO0, ANO1:	Analog output	$\overline{RESET}$:	Reset
ASCK0:	Asynchronous serial clock	RTP00 to RTP05,	
ASTB:	Address strobe	RTP10 to RTP15:	Real-time output port
AV_{REF0}, AV_{REF1}:	Analog reference voltage	RXD0 to RXD2:	Receive data
AV_{SS}:	Ground for analog	$\overline{SCK00}$ to $\overline{SCK02}$,	
BV_{DD}:	Power supply for bus interface	$\overline{SCKA0}$, $\overline{SCKA1}$:	Serial clock
BV_{SS}:	Ground for bus interface	SCL0, SCL1:	Serial clock
CLKOUT:	Clock output	SDA0, SDA1:	Serial data
$\overline{CS0}$ to $\overline{CS3}$:	Chip select	SI00 to SI02,	
EV_{DD}:	Power supply for port	SIA0, SIA1:	Serial input
EV_{SS}:	Ground for port	SO00 to SO02,	
$\overline{HLDAK}$:	Hold acknowledge	SOA0, SOA1:	Serial output
$\overline{HLDRQ}$:	Hold request	TI000, TI001,	
IC:	Internally connected	TI010, TI011,	
INTP0 to INTP6:	External interrupt input	TI020, TI021,	
KR0 to KR7:	Key return	TI030, TI031,	
NMI:	Non-maskable interrupt request	TI040, TI041,	
P00 to P06:	Port 0	TI050, TI051,	
P10, P11:	Port 1	TI50, TI51:	Timer input
P30 to P39:	Port 3	TO00 to TO05,	
P40 to P42:	Port 4	TO50, TO51,	
P50 to P55:	Port 5	TOH0, TOH1:	Timer output
P60 to P615:	Port 6	TXD0 to TXD2:	Transmit data
P70 to P715:	Port 7	V_{DD}:	Power supply
P80, P81:	Port 8	V_{PP}:	Programming power supply
P90 to P915:	Port 9	V_{SS}:	Ground
PCD0 to PCD3:	Port CD	$\overline{WAIT}$:	Wait
PCM0 to PCM5:	Port CM	$\overline{WR0}$:	Lower byte write strobe
PCS0 to PCS7:	Port CS	$\overline{WR1}$:	Upper byte write strobe
PCT0 to PCT7:	Port CT	X1, X2:	Crystal for main clock
PDH0 to PDH7:	Port DH	XT1, XT2:	Crystal for subclock

1.4.5 Function block configuration (V850ES/KJ1)

(1) Internal block diagram



Notes 1. μPD703216, 703216Y: 96 KB (mask ROM)
μPD703217, 703217Y: 128 KB (mask ROM)
μPD70F3217, 70F3217Y: 128 KB (flash memory)

2. Only in the μPD703216Y, 703217Y, 70F3217Y

3. Only in the μPD703216, 703216Y, 703217, and 703217Y

4. Only in the μPD70F3217 and 70F3217Y

(2) Internal units

(a) CPU

The CPU uses five-stage pipeline control to enable single-clock execution of address calculations, arithmetic logic operations, data transfers, and almost all other types of instruction processing.

Other dedicated on-chip hardware, such as a multiplier (16 bits × 16 bits → 32 bits) and a barrel shifter (32 bits) help accelerate complex processing.

(b) Bus control unit (BCU)

The BCU starts a required external bus cycle based on the physical address obtained by the CPU.

When an instruction is fetched from external memory space and the CPU does not send a bus cycle start request, the BCU generates a prefetch address and prefetches the instruction code. The prefetched instruction code is stored in an internal instruction queue.

(c) ROM

This consists of a 128 KB or 96 KB mask ROM or flash memory mapped to the address spaces from 0000000H to 001FFFFH or 0000000H to 0017FFFH, respectively.

ROM can be accessed by the CPU in one clock cycle during instruction fetch.

(d) RAM

This consists of a 6 KB RAM mapped to the address spaces from 3FFD800H to 3FFEFFFH.

RAM can be accessed by the CPU in one clock cycle during data access.

(e) Interrupt controller (INTC)

This controller handles hardware interrupt requests (NMI, INTP0 to INTP6) from on-chip peripheral hardware and external hardware. Eight levels of interrupt priorities can be specified for these interrupt requests, and multiplexed servicing control can be performed.

(f) Clock generator (CG)

A main clock oscillator and subclock oscillator are provided and generate the main clock oscillation frequency (f_X) and subclock frequency (f_{XT}), respectively.

There are two modes: In the clock-through mode, f_X is used as the main clock frequency (f_{XX}) as is. In the PLL mode, f_X is used multiplied by 4.

The CPU clock frequency (f_{CPU}) can be selected from among f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, and f_{XT}.

(g) Timer/counter

Six 16-bit timer/event counter channels and two 8-bit timer/event counter channels are incorporated, enabling measurement of pulse intervals and frequency as well as programmable pulse output.

Two 8-bit timer/event counters can be connected in cascade to configure a 16-bit timer.

Two 8-bit timer channels enabling programmable pulse output are provided on chip.

(h) Watch timer

This timer counts the reference time (0.5 seconds) for counting the clock from the subclock (32.768 kHz) or f_{BRG} (32.768 kHz) from the clock generator. At the same time, the watch timer can be used as an interval timer.

(i) Watchdog timer

Two watchdog timer channels are provided on chip to detect program loops and system abnormalities. Watchdog timer 1 can be used as an interval timer. When used as a watchdog timer, it generates a non-maskable interrupt request signal (INTWDT1) or system reset signal (WDTRES1) after an overflow occurs. When used as an interval timer, it generates a maskable interrupt request signal (INTWDTM1) after an overflow occurs.

Watchdog timer 2 operates by default following reset release.

It generates a non-maskable interrupt request signal (INTWDT2) or system reset signal (WDTRES2) after an overflow occurs.

(j) Serial interface (SIO)

The V850ES/KJ1 includes four kinds of serial interfaces: an asynchronous serial interface (UARTn), a clocked serial interface (CSI0n), a clocked serial interface with an automatic transmit/receive function (CSIAm), and an I^2C bus interface (I^2Cm). The μPD703216, 703217, and 70F3217 can simultaneously use up to eight channels, and the μPD703216Y, 703217Y, and 70F3217Y up to nine channels.

For UARTn, data is transferred via the TXDn and RXDn pins.

For CSI0n, data is transferred via the SO0n, SI0n, and $\overline{\text{SCK0n}}$ pins.

For CSIAm, data is transferred via the SOAm, SIAm, and $\overline{\text{SCKAm}}$ pins.

For I^2Cm, data is transferred via the SDAm and SCLm pins.

I^2Cm is provided only in the μPD703216Y, 703217Y, and 70F3217Y.

Remark n = 0 to 2
m = 0, 1

(k) A/D converter

This high-speed, high-resolution 10-bit A/D converter includes 16 analog input pins. Conversion is performed using the successive approximation method.

(l) D/A converter

Two 8-bit resolution D/A converter channels are included on chip. The D/A converter uses the R-2R ladder method.

(m) ROM correction

This function is used to replace part of a program in the mask ROM with that contained in the internal RAM. Up to four correction addresses can be specified.

(n) Key interrupt function

A key interrupt request signal (INTKR) can be generated by inputting a falling edge to the eight key input pins.

(o) Real-time output function

This function transfers 6-bit data set beforehand to output latches upon occurrence of a timer compare register match signal.

For the V850ES/KJ1, a 2-channel 6-bit data real-time output function is provided on chip.

(p) Ports

As shown below, the following ports have general-purpose port functions and control pin functions.

Port	I/O	Alternate Function
P0	7-bit I/O	NMI, external interrupt, timer output
P1	2-bit I/O	D/A converter analog output
P3	10-bit I/O	Serial interface, timer I/O
P4	3-bit I/O	Serial interface
P5	6-bit I/O	Serial interface, timer I/O, key interrupt function, real-time output function
P6	16-bit I/O	Serial interface, timer I/O, real-time output function
P7	16-bit input	A/D converter analog input
P8	2-bit I/O	Serial interface
P9	16-bit I/O	External address bus, serial interface, timer I/O, external interrupt, key interrupt function
PCD	4-bit I/O	–
PCM	6-bit I/O	External bus control signal
PCS	8-bit I/O	Chip select output
PCT	8-bit I/O	External bus control signal
PDH	8-bit I/O	External address bus
PDL	16-bit I/O	External address/data bus

★ 1.5 Overview of Functions

- V850ES/KF1

Part Number		μPD703208/μPD703208Y	μPD703209/μPD703209Y	μPD703210/μPD703210Y	μPD70F3210/μPD70F3210Y
Internal memory	ROM	64 KB	96 KB	128 KB	128 KB (flash memory)
	RAM	4 KB		6 KB	
Buffer RAM		32 bytes			
Memory space	Logical space	64 MB			
	External memory area	128 KB			
External bus interface		Address bus: 16 bits Data bus: 8/16 bits Multiplex bus mode			
General-purpose registers		32 bits × 32 registers			
Main clock (oscillation frequency)		Ceramic/crystal/external clock			
	When PLL not used	2 to 10 MHz: 2.7 to 5.5 V			
	When PLL used: REGC pin connected directly to V_{DD}	Standard products, (A) special grade products: 2 to 5 MHz: 4.5 to 5.5 V, 2 to 4 MHz: 4.0 to 5.5 V, 2 to 2.5 MHz: 2.7 to 5.5 V (A1) special grade products: 2 to 5 MHz: 4.5 to 5.5 V, 2 to 4 MHz: 4.0 to 5.5 V, 2 to 3 MHz: 3.5 to 5.5 V (A2) special grade products: 2 to 4 MHz: 4.0 to 5.5 V, 2 to 3 MHz: 3.5 to 5.5 V		
	When PLL used: 10 μF capacitor connected to REGC pin	Standard products, (A) special grade products, (A1) special grade products, (A2) special grade products: 2 to 4 MHz: 4.0 to 5.5 V			
Subclock (oscillation frequency)		Crystal/external clock (32.768 kHz)			
Minimum instruction execution time		When main clock operated at (f_{XX}) = 20 MHz			
DSP function		32 × 32 = 64: 200 to 250 ns (at 20 MHz) 32 × 32 + 32 = 32: 300 ns (at 20 MHz) 16 × 16 = 32: 50 to 100 ns (at 20 MHz) 16 × 16 + 32 = 32: 150 ns (at 20 MHz)			
I/O ports		67 Input: 8 I/O: 59 (among these, N-ch open-drain output selectable: 2, fixed to N-ch open-drain output: 6)			
Timer		16-bit timer/event counter: 2 channels 8-bit timer/event counter: 2 channels (16-bit timer/event counter: Usable as 1 channel) 8-bit timer: 2 channels Watchdog timer: 2 channels Watch timer: 1 channel 8-bit interval timer: 1 channel			
Real-time output port		4 bits × 1, 2 bits × 1, or 6 bits × 1			
A/D converter		10-bit resolution × 8 channels			
D/A converter		–			
Serial interface		CSI: 2 channels CSIA (with automatic transmit/receive function): 1 channel UART: 2 channels I^2C bus: 1 channel			
Interrupt sources		External: 9 (9)[Note 2], internal: 22/23[Note 1]			
Power save function		STOP/IDLE/HALT			
Operating supply voltage		Standard products, (A) special grade products: 4.5 to 5.5 V (at 20 MHz)/4.0 to 5.5 V (at 16 MHz)/2.7 to 5.5 V (at 10 MHz) (A1) special grade products (mask version only): 4.5 to 5.5 V (at 20 MHz)/4.0 to 5.5 V (at 16MHz)/3.5 to 5.5 V (at 12 MHz) (A2) special grade products (mask version only): 4.0 to 5.5 V (at 16 MHz)/3.5 to 5.5 V (at 12 MHz)			
Package		80-pin plastic TQFP (fine pitch) (12 × 12 mm), 80-pin plastic QFP (14 × 14 mm)			

Notes 1. Y products only.

2. The figure in parentheses indicates the number of external interrupts for which STOP mode can be released.

- V850ES/KG1

Part Number		μPD703212/μPD703212Y	μPD703213/μPD703213Y	μPD703214/μPD703214Y	μPD70F3214/μPD70F3214Y
Internal memory	ROM	64 KB	96 KB	128 KB	128 KB (flash memory)
	RAM	4 KB		6 KB	
Buffer RAM		64 bytes			
Memory space	Logical space	64 MB			
	External memory area	3 MB			
External bus interface		Address bus: 22 bits Data bus: 8/16 bits Multiplex bus mode/separate bus mode			
General-purpose registers		32 bits × 32 registers			
Main clock (oscillation frequency)		Ceramic/crystal/external clock			
	When PLL not used	2 to 10 MHz: 2.7 to 5.5 V			
	When PLL used, REGC pin connected directly to V_{DD}	Standard products, (A) special grade products: 2 to 5 MHz: 4.5 to 5.5 V, 2 to 4 MHz: 4.0 to 5.5 V, 2 to 2.5 MHz: 2.7 to 5.5 V (A1) special grade products: 2 to 5 MHz, 4.5 to 5.5 V, 2 to 4 MHz: 4.0 to 5.5 V, 2 to 3 MHz: 3.5 to 5.5 V (A2) special grade products: 2 to 4 MHz, 4.0 to 5.5 V, 2 to 3 MHz: 3.5 to 5.5 V			
	When PLL used, 10 μF capacitor connected to REGC pin	Standard products, (A) special grade products, (A1) special grade products, (A2) special grade products: 2 to 4 MHz: 4.0 to 5.5 V			
Subclock (oscillation frequency)		Crystal/external clock (32.768 kHz)			
Minimum instruction execution time		When main clock operated at (f_{XX}) = 20 MHz			
DSP function		32 × 32 = 64: 200 to 250 ns (at 20 MHz) 32 × 32 + 32 = 32: 300 ns (at 20 MHz) 16 × 16 = 32: 50 to 100 ns (at 20 MHz) 16 × 16 + 32 = 32: 150 ns (at 20 MHz)			
I/O port		84 • Input: 8 • I/O: 76 (among these, N-ch open-drain output selectable: 4, fixed to N-ch open-drain output: 8)			
Timer		16-bit timer/event counter: 4 channels 8-bit timer/event counter: 2 channels (16-bit timer/event counter: Usable as 1 channel) 8-bit timer: 2 channels Watchdog timer: 2 channels Watch timer: 1 channel 8-bit interval timer: 1 channel			
Real-time output port		4 bits × 1, 2 bits × 1, or 6 bits × 1			
A/D converter		10-bit resolution × 8 channels			
D/A converter		8-bit resolution × 2 channels			
Serial interface		CSI: 2 channels CSIA (with automatic transmit/receive function): 2 channels UART: 2 channels I^2C bus: 1 channel[Note 1]			
Interrupt sources		External: 9 (9)[Note 2], internal: 27/28[Note 1]			
Power save function		STOP/IDLE/HALT			
Operating supply voltage		Standard products, (A) special grade products: 4.5 to 5.5 V (at 20 MHz)/4.0 to 5.5 V/(at 16 MHz)/2.7 to 5.5 V (at 10 MHz) (A1) special grade products (mask version only): 4.5 to 5.5 V (at 20 MHz)/4.0 to 5.5 V/(at 16 MHz)/3.5 to 5.5 V (at 12 MHz) (A2) special grade products (mask version only): 4.0 to 5.5 V (at 16 MHz)/3.5 to 5.5 V/(at 12 MHz)			
Package		100-pin plastic TQFP (fine pitch) (14 × 14 mm)			

Notes 1. Y products only.

2. The figure in parentheses indicates the number of external interrupts for which STOP mode can be released.

- V850ES/KJ1

Part Number				μPD703216/μPD703216Y	μPD703217/μPD703217Y	μPD70F3217/μPD70F3217Y
Internal memory	ROM			96 KB	128 KB	128 KB (flash memory)
	High-speed RAM			6 KB		
Buffer RAM				64 bytes		
Memory space	Logical space			64 MB		
	External memory area			15 MB		
External bus interface				Address bus: 24 bits Data bus: 8/16 bits Multiplex bus mode/separate bus mode		
General-purpose registers				32 bits × 32 registers		
Main clock (oscillation frequency)				Ceramic/crystal/external clock		
		When PLL not used		2 to 10 MHz: 2.7 to 5.5 V		
		When PLL used	REGC pin connected directly to V_{DD}	Standard products, (A) special grade products: 2 to 5 MHz: 4.5 to 5.5 V, 2 to 4 MHz: 4.0 to 5.5 V, 2 to 2.5 MHz: 2.7 to 5.5 V (A1) special grade products: 2 to 5 MHz: 4.5 to 5.5 V, 2 to 4 MHz: 4.0 to 5.5 V, 2 to 3 MHz: 3.5 to 5.5 V (A2) special grade products: 2 to 4 MHz: 4.0 to 5.5 V, 2 to 3 MHz: 3.5 to 5.5 V		
			10 μF capacitor connected to REGC pin	Standard products, (A) special grade products, (A1) special grade products, (A2) special grade products: 2 to 4 MHz: 4.0 to 5.5 V		
Subclock (oscillation frequency)				Crystal/external clock (32.768 kHz)		
Minimum instruction execution time				When main clock operated at (f_{XX}) = 20 MHz		
DSP function				32 × 32 = 64: 200 to 250 ns (at 20 MHz) 32 × 32 + 32 = 32: 300 ns (at 20 MHz) 16 × 16 = 32: 50 to 100 ns (at 20 MHz) 16 × 16 + 32 = 32: 150 ns (at 20 MHz)		
I/O ports				128 • Input: 16 • I/O: 112 (among these, N-ch open-drain output selectable: 6, fixed to N-ch open-drain output: 12)		
Timer				16-bit timer/event counter: 6 channels 8-bit timer/event counter: 2 channels (16-bit timer/event counter: usable as 1 channel) 8-bit timer: 2 channels Watchdog timer: 2 channels Watch timer: 1 channel 8-bit interval timer: 1 channel		
Real-time output port				2 channels: 4 bits × 1, 2 bits × 1, or 6 bits × 1		
A/D converter				10-bit resolution × 16 channels		
D/A converter				8-bit resolution × 2 channels		
Serial interface				CSI: 3 channels CSIA (with automatic transmit/receive function): 2 channels UART: 3 channels/2 channels[Note 1] UART/I^2C bus: 1 channel[Note 1] Dedicated baud rate generator: 3 channels		
Interrupt sources				External: 9 (9)[Note 2], internal: 35/37[Note 1]		
Power save function				STOP/IDLE/HALT		
Operating supply voltage				Standard products, (A) special grade products: 4.5 to 5.5 V (at 20 MHz)/4.0 to 5.5 V (at 16 MHz)/2.7 to 5.5 V (at 10 MHz) (A1) special grade products (mask version only): 4.5 to 5.5 V (at 20 MHz)/4.0 to 5.5 V (at 16 MHz)/3.5 to 5.5 V (at 12 MHz) (A2) special grade products (mask version only): 4.0 to 5.5 V (at 16 MHz)/3.5 to 5.5 V (at 12 MHz)		
Package				144-pin plastic TQFP (fine pitch) (20 × 20 mm)		

Notes 1. Y products only.

2. The figure in parentheses indicates the number of external interrupts for which STOP mode can be released.

CHAPTER 2 PIN FUNCTIONS

The names and functions of the pins of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 are described below, divided into port pins and non-port pins.

The pin I/O buffer power supplies are divided into three systems; AV_{REF0}/AV_{REF1}, BV_{DD}, and EV_{DD}. The relationship between these power supplies and the pins is shown below.

Table 2-1. V850ES/KF1 Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF0}	Port 7
EV_{DD}	$\overline{RESET}$, ports 0, 3 to 5, 9, CM, CS, CT, DL

Table 2-2. V850ES/KG1 Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF0}	Port 7
AV_{REF1}	Port 1
BV_{DD}	Ports CM, CS, CT, DH, DL
EV_{DD}	$\overline{RESET}$, ports 0, 3 to 5, 9

Table 2-1. V850ES/KJ1 Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF0}	Port 7
AV_{REF1}	Port 1
BV_{DD}	Ports CD, CM, CS, CT, DH, DL
EV_{DD}	$\overline{RESET}$, ports 0, 3 to 6, 8, 9

2.1 List of Pin Functions

(1) Port pins

(1/4)

Pin Name	I/O	Pull-up Resistor	Function	Alternate Function	Products
P00	I/O	Yes	Port 0 I/O port Input/output can be specified in 1-bit units.	TOH0	All products
P01				TOH1	
P02				NMI	
P03				INTP0	
P04				INTP1	
P05				INTP2	
P06				INTP3	
P10	I/O	Yes	Port 1 I/O port Input/output can be specified in 1-bit units.	ANO0	KG1, KJ1
P11				ANO1	
P30	I/O	Yes	Port 3 I/O port Input/output can be specified in 1-bit units. P36 to P39 are fixed to open-drain output.	TXD0	All products
P31				RXD0	
P32				ASCK0	
P33				TI000/TO00	
P34				TI001	
P35				TI010/TO01	
P36		No[Note 1]		–	KG1, KJ1
P37				–	
P38				SDA0[Note 2]	All products
P39				SCL0[Note 2]	

Notes 1. An on-chip pull-up resistor can be provided by a mask option (only in the mask ROM versions).

2. Only in products with an I^2C bus

Remark KG1: V850ES/KG1, KJ1: V850ES/KJ1

(2/4)

Pin Name	I/O	Pull-up Resistor	Function	Alternate Function	Products
P40	I/O	Yes	Port 4 I/O port Input/output can be specified in 1-bit units. P41 and P42 can be specified as N-ch open-drain output in 1-bit units.	SI00	All products
P41				SO00	
P42				$\overline{\text{SCK00}}$	
P50	I/O	Yes	Port 5 I/O port Input/output can be specified in 1-bit units. P54 and P55 can be specified as N-ch open-drain output in 1-bit units.	TI011/RTP00/KR0	All products
P51				TI50/RTP01/KR1	
P52				TO50/RTP02/KR2	
P53				SIA0/RTP03/KR3	
P54				SOA0/RTP04/KR4	
P55				$\overline{\text{SCKA0}}$/RTP05/KR5	
P60	I/O	Yes	Port 6 I/O port Input/output can be specified in 1-bit units. P67 and P68 can be specified as N-ch open-drain output in 1-bit units. P614 and P615 are fixed to N-ch open-drain output.	RTP10	KJ1
P61				RTP11	
P62				RTP12	
P63				RTP13	
P64				RTP14	
P65				RTP15	
P66				SI02	
P67				SO02	
P68				$\overline{\text{SCK02}}$	
P69				TI040	
P610				TI041	
P611				TO04	
P612				TI050	
P613				TI051/TO05	
P614		No[Note]		–	
P615				–	
P70	Input	No	Port 7 Input port	ANI0	All products
P71				ANI1	
P72				ANI2	
P73				ANI3	
P74				ANI4	
P75				ANI5	
P76				ANI6	
P77				ANI7	
P78				ANI8	KJ1
P79				ANI9	
P710				ANI10	
P711				ANI11	
P712				ANI12	

Note An internal pull-up resistor can be provided by a mask option (only for the mask ROM versions).

Remark KJ1: V850ES/KJ1

(3/4)

Pin Name	I/O	Pull-up Resistor	Function	Alternate Function	Products
P713	Input	No	Port 7 Input port	ANI13	KJ1
P714				ANI14	
P715				ANI15	
P80	I/O	Yes	Port 8 I/O port Input/output can be specified in 1-bit units. N-ch open-drain output can be specified in 1-bit units.	RXD2/SDA1[Note]	KJ1
P81				TXD2/SCL1[Note]	
P90	I/O	Yes	Port 9 I/O port Input/output can be specified in 1-bit units. P98, P99, P911, and P912 can be specified as N-ch open-drain output in 1-bit units.	A0/TXD1/KR6	All products
P91				A1/RXD1/KR7	
P92				A2/TI020/TO02	KG1, KJ1
P93				A3/TI021	
P94				A4/TI030/TO03	
P95				A5/TI031	
P96				A6/TI51/TO51	All products
P97				A7/SI01	
P98				A8/SO01	
P99				A9/$\overline{\text{SCK01}}$	
P910				A10/SIA1	KG1, KJ1
P911				A11/SOA1	
P912				A12/$\overline{\text{SCKA1}}$	
P913				A13/INTP4	All products
P914				A14/INTP5	
P915				A15/INTP6	
PCD0	I/O	No	Port CD I/O port Input/output can be specified in 1-bit units.	–	KJ1
PCD1				–	
PCD2				–	
PCD3				–	
PCM0	I/O	No	Port CM I/O port Input/output can be specified in 1-bit units.	$\overline{\text{WAIT}}$	All products
PCM1				CLKOUT	
PCM2				$\overline{\text{HLDAK}}$	
PCM3				$\overline{\text{HLDQR}}$	
PCM4				–	KJ1
PCM5				–	
PCS0	I/O	No	Port CS I/O port Input/output can be specified in 1-bit units.	$\overline{\text{CS0}}$	All products
PCS1				$\overline{\text{CS1}}$	
PCS2				$\overline{\text{CS2}}$	KJ1
PCS3				$\overline{\text{CS3}}$	
PCS4				–	
PCS5				–	
PCS6				–	
PCS7				–	

Note Only in the μPD703216Y, 703217Y, and 70F3217Y

Remarks 1. KG1: V850ES/KG1, KJ1: V850ES/KJ1

2. The A0 to A15 pins are not provided in the V850ES/KF1.

(4/4)

Pin Name	I/O	Pull-up Resistor	Function	Alternate Function	Products
PCT0	I/O	No	Port CT I/O port Input/output can be specified in 1-bit units.	$\overline{WR0}$	All products
PCT1				$\overline{WR1}$	
PCT2				–	KJ1
PCT3				–	
PCT4				$\overline{RD}$	All products
PCT5				–	KJ1
PCT6				ASTB	All products
PCT7				–	KJ1
PDH0	I/O	No	Port DH I/O port Input/output can be specified in 1-bit units.	A16	KG1, KJ1
PDH1				A17	
PDH2				A18	
PDH3				A19	
PDH4				A20	
PDH5				A21	
PDH6				A22	KJ1
PDH7				A23	
PDL0	I/O	No	Port DL I/O port Input/output can be specified in 1-bit units.	AD0	All products
PDL1				AD1	
PDL2				AD2	
PDL3				AD3	
PDL4				AD4	
PDL5				AD5	
PDL6				AD6	
PDL7				AD7	
PDL8				AD8	
PDL9				AD9	
PDL10				AD10	
PDL11				AD11	
PDL12				AD12	
PDL13				AD13	
PDL14				AD14	
PDL15				AD15	

Remark KG1: V850ES/KG1, KJ1: V850ES/KJ1

(2) Non-port pins

(1/5)

Pin Name	I/O	Pull-up Resistor	Function	Alternate Function	Products
A0	Output	Yes	Address bus for external memory (when using a separate bus)	P90/TXD1/KR6	KG1, KJ1
A1				P91/RXD1/KR7	
A2				P92/TI020/TO02	
A3				P93/TI021	
A4				P94/TI030/TO03	
A5				P95/TI031	
A6				P96/TI51/TO51	
A7				P97/SI01	
A8				P98/SO01	
A9				P99/$\overline{\text{SCK01}}$	
A10				P910/SIA1	
A11				P911/SOA1	
A12				P912/$\overline{\text{SCKA1}}$	
A13				P913/INTP4	
A14				P914/INTP5	
A15				P915/INTP6	
A16	Output	No	Address bus for external memory	PDH0	KG1, KJ1
A17				PDH1	
A18				PDH2	
A19				PDH3	
A20				PDH4	
A21				PDH5	
A22				PDH6	KJ1
A23				PDH7	
AD0	I/O	No	Address/data bus for external memory	PDL0	All products
AD1				PDL1	
AD2				PDL2	
AD3				PDL3	
AD4				PDL4	
AD5				PDL5	
AD6				PDL6	
AD7				PDL7	
AD8				PDL8	
AD9				PDL9	
AD10				PDL10	
AD11				PDL11	
AD12				PDL12	
AD13				PDL13	
AD14				PDL14	
AD15				PDL15	

Remark KG1: V850ES/KG1, KJ1: V850ES/KJ1

(2/5)

Pin Name	I/O	Pull-up Resistor	Function	Alternate Function	Products
ANI0	Input	No	Analog voltage input for A/D converter	P70	All products
ANI1				P71	
ANI2				P72	
ANI3				P73	
ANI4				P74	
ANI5				P75	
ANI6				P76	
ANI7				P77	
ANI8				P78	KJ1
ANI9				P79	
ANI10				P710	
ANI11				P711	
ANI12				P712	
ANI13				P713	
ANI14				P714	
ANI15				P715	
ANO0	Output	Yes	Analog voltage output for D/A converter	P10	KG1, KJ1
ANO1				P11	
ASCK0	Input	Yes	UART0 serial clock input	P32	All products
ASTB	Output	No	Address strobe signal output for external memory	PCT6	All products
AV_{REF0}	–	–	Reference voltage for A/D converter and alternate-function ports	–	All products
AV_{REF1}	–	–	Reference voltage for D/A converter	–	KG1, KJ1
AV_{SS}	–	–	Ground potential for A/D and D/A converters	–	All products
BV_{DD}	–	–	Positive power supply for bus interface and alternate-function ports	–	KG1, KJ1
BV_{SS}	–	–	Ground potential for bus interface and alternate-function ports	–	KG1, KJ1
CLKOUT	Output	No	Internal system clock output	PCM1	All products
$\overline{CS0}$	Output	No	Chip select output	PCS0	All products
$\overline{CS1}$				PCS1	
$\overline{CS2}$				PCS2	KJ1
$\overline{CS3}$				PCS3	
EV_{DD}	–	–	Positive power supply for external	–	All products
EV_{SS}	–	–	Ground potential for external	–	All products
$\overline{HLDAK}$	Output	No	Bus hold acknowledge output	PCM2	All products
$\overline{HLDRQ}$	Input	No	Bus hold request input	PCM3	All products
IC[Note]	–	–	Internally connected	–	All products

Note Only in the mask ROM versions

Remark KG1: V850ES/KG1, KJ1: V850ES/KJ1

(3/5)

Pin Name	I/O	Pull-up Resistor	Function	Alternate Function	Products
INTP0	Input	Yes	External interrupt request input (maskable, analog noise elimination)	P03	All products
INTP1				P04	
INTP2				P05	
INTP3				P06	
INTP4				P913/A13	
INTP5				P914/A14	
INTP6				P915/A15	
KR0	Input	Yes	Key return input	P50/TI011/RTP00	All products
KR1				P51/TI50/RTP01	
KR2				P52/TO50/RTP02	
KR3				P53/SIA0/RTP03	
KR4				P54/SOA0/RTP04	
KR5				P55/$\overline{\text{SCKA0}}$/RTP05	
KR6				P90/A0/TXD1	
KR7				P91/A1/RXD1	
NMI	Input	Yes	External interrupt input (non-maskable, analog noise elimination)	P02	All products
$\overline{\text{RD}}$	Output	No	Read strobe signal output for external memory	PCT4	All products
REGC	–	–	Connecting capacitor for regulator output stabilization	–	All products
$\overline{\text{RESET}}$	Input	–	System reset input	–	All products
RTP00	Output	Yes	Real-time output port	P50/TI011/KR0	All products
RTP01				P51/TI50/KR1	
RTP02				P52/TO50/KR2	
RTP03				P53/SIA0/KR3	
RTP04				P54/SOA0/KR4	
RTP05				P55/$\overline{\text{SCKA0}}$/KR5	
RTP10				P60	KJ1
RTP11				P61	
RTP12				P62	
RTP13				P63	
RTP14				P64	
RTP15				P65	
RXD0	Input	Yes	Serial receive data input for UART0	P31	All products
RXD1			Serial receive data input for UART1	P91/A1/KR7	
RXD2			Serial receive data input for UART2	P80/SDA1[Note]	KJ1

Note Only in products with an I^2C bus

Remark KG1: V850ES/KG1, KJ1: V850ES/KJ1

(4/5)

Pin Name	I/O	Pull-up Resistor	Function	Alternate Function	Products
$\overline{SCK00}$	I/O	Yes	Serial clock I/O for CSI00 to CSI02, CSIA0, CSIA1 N-ch open-drain output can be specified in 1-bit units.	P42	All products
$\overline{SCK01}$				P99/A9	
$\overline{SCK02}$				P68	KJ1
$\overline{SCKA0}$				P55/RTP05/KR5	All products
$\overline{SCKA1}$				P912/A12	KG1, KJ1
SCL0[Note 1]	I/O	No[Note 2]	Serial clock I/O for I^2C0 Fixed to N-ch open-drain output	P39	All products
SCL1[Note 3]		Yes	Serial clock I/O (I^2C1) N-ch open-drain output can be specified	P81/TXD2	KJ1
SDA0[Note 1]	I/O	No[Note 2]	Serial transmit/receive data I/O for I^2C0 Fixed to N-ch open-drain output	P38	All products
SDA1[Note 3]		Yes	Serial transmit/receive data I/O for I^2C1 N-ch open-drain output can be specified	P80/RXD2	KJ1
SI00	Input	Yes	Serial receive data input for CSI00	P40	All products
SI01			Serial receive data input for CSI01	P97/A7	
SI02			Serial receive data input for CSI02	P66	KJ1
SIA0			Serial receive data input for CSIA0	P53/RTP03/KR3	All products
SIA1			Serial receive data input for CSIA1	P910/A10	KG1, KJ1
SO00	Output	Yes	Serial transmit data output for CSI00	P41	All products
SO01			Serial transmit data output for CSI01	P98/A8	
SO02			Serial transmit data output for CSI02	P67	KJ1
SOA0			Serial transmit data output for CSIA0	P54/RTP04/KR4	All products
SOA1			Serial transmit data output for CSIA1	P911/A11	KG1, KJ1
TI000	Input	Yes	External event/clock input for TM00	P33/TO00	All products
TI001			External event/clock input for TM00	P34	
TI010			External event/clock input for TM01	P35/TO01	
TI011			External event/clock input for TM01	P50/RTP00/KR0	
TI020			External event/clock input for TM02	P92/A2/TO02	KG1, KJ1
TI021			External event/clock input for TM02	P93/A3	
TI030			External event/clock input for TM03	P94/A4/TO03	
TI031			External event/clock input for TM03	P95/A5	
TI040			External event/clock input for TM04	P69	KJ1
TI041			External event/clock input for TM04	P610	
TI050			External event/clock input for TM05	P612	
TI051			External event/clock input for TM05	P613/TO05	
TI50			External event/clock input for TM50	P51/RTP01/KR1	All products
TI51			External event/clock input for TM51	P96/A6/TO51	

Notes 1. Only in products with an I^2C bus

2. An on-chip pull-up resistor can be provided by a mask option (only in the mask ROM and I^2C bus versions).

3. Only in the μPD703216Y, 703217Y, and 70F3217Y

Remark KG1: V850ES/KG1, KJ1: V850ES/KJ1

(5/5)

Pin Name	I/O	Pull-up Resistor	Function	Alternate Function	Products
TO00	Output	Yes	Timer output for TM00	P33/TI000	All products
TO01			Timer output for TM01	P35/TI010	
TO02			Timer output for TM02	P92/A2/TI020	KG1, KJ1
TO03			Timer output for TM03	P94/A4/TI030	
TO04			Timer output for TM04	P611	KJ1
TO05			Timer output for TM05	P613/TI051	
TO50			Timer output for TM50	P52/RTP02/KR2	All products
TO51			Timer output for TM51	P96/A6/TI51	
TOH0			Timer output for TMH0	P00	
TOH1			Timer output for TMH1	P01	
TXD0	Output	Yes	Serial transmit data output for UART0	P30	All products
TXD1			Serial transmit data output for UART1	P90/A0/KR6	
TXD2			Serial transmit data output for UART2	P81/SCL1[Note 1]	KJ1
V_{DD}	–	–	Positive power supply pin for internal	–	All products
V_{PP}	–	–	High-voltage application pin for program write/verify	–	All products[Note 2]
V_{SS}	–	–	Ground potential for internal	–	All products
$\overline{WAIT}$	Input	No	External wait input	PCM0	All products
$\overline{WR0}$	Output	No	Write strobe for external memory (lower 8 bits)	PCT0	All products
$\overline{WR1}$			Write strobe for external memory (higher 8 bits)	PCT1	All products
X1	Input	No	Connecting resonator for main clock	–	All products
X2	–	No		–	All products
XT1	Input	No	Connecting resonator for subclock	–	All products
XT2	–	No		–	All products

Notes 1. Only in the μPD703216Y, 703217Y, and 70F3217Y

2. Only in products with flash memory

Remark KG1: V850ES/KG1, KJ1: V850ES/KJ1

2.2 Pin Status

The address bus becomes undefined during accesses to the internal RAM and ROM. The data bus goes into the high-impedance state without data output. The external bus control signal becomes inactive.

During peripheral I/O access, the address bus outputs the addresses of the on-chip peripheral I/Os that are accessed. The data bus goes into the high-impedance state without data output. The external bus control signal becomes inactive.

★ **Table 2-4. Pin Operation Status in Operation Modes of V850ES/KF1**

Operating Status / Pin	Reset[Note 1]	HALT Mode	IDLE Mode/ STOP Mode	Idle State[Note 2]	Bus Hold
AD0 to AD15 (PDL0 to PDL15)	Hi-Z	Undefined	Hi-Z	Held	Hi-Z
$\overline{\text{WAIT}}$ (PCM0)	Hi-Z	–	–	–	–
CLKOUT (PCM1)	Hi-Z	Operating	L	Operating	Operating
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$ (PCS0, PCS1)	Hi-Z	H	H	Held	Hi-Z
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$ (PCT0, PCT1)	Hi-Z	H	H	H	Hi-Z
$\overline{\text{RD}}$ (PCT4)	Hi-Z	H	H	H	Hi-Z
ASTB (PCT6)	Hi-Z	H	H	H	Hi-Z
$\overline{\text{HLDAK}}$ (PCM2)	Hi-Z	Operating	H	H	L
$\overline{\text{HLDRQ}}$ (PCM3)	Hi-Z	Operating	–	–	Operating

Notes 1. Since the bus control pin is also used as a port pin, it is initialized to the port mode (input) after reset.

2. The pin statuses in the idle state inserted after the T3 state are listed.

Remark Hi-Z: High impedance
H: High-level output
L: Low-level output
–: Input without sampling (input acknowledgment not possible)

★ **Table 2-5. Pin Operation Status in Operation Modes of V850ES/KG1**

Operating Status / Pin	Reset[Note 1]	HALT Mode	IDLE Mode/ STOP Mode	Idle State[Note 2]	Bus Hold
AD0 to AD15 (PDL0 to PDL15)	Hi-Z	**Note 3**	Hi-Z	Held	Hi-Z
A0 to A15 (P90 to P915)	Hi-Z	Undefined[Note 4]	Hi-Z	Held	Hi-Z
A16 to A21 (PDH0 to PDH5)	Hi-Z	Undefined	Hi-Z	Held	Hi-Z
$\overline{\text{WAIT}}$ (PCM0)	Hi-Z	–	–	–	–
CLKOUT (PCM1)	Hi-Z	Operating	L	Operating	Operating
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$ (PCS0, PCS1)	Hi-Z	H	H	Held	Hi-Z
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$ (PCT0, PCT1)	Hi-Z	H	H	H	Hi-Z
$\overline{\text{RD}}$ (PCT4)	Hi-Z	H	H	H	Hi-Z
ASTB (PCT6)	Hi-Z	H	H	H	Hi-Z
$\overline{\text{HLDAK}}$ (PCM2)	Hi-Z	Operating	H	H	L
$\overline{\text{HLDRQ}}$ (PCM3)	Hi-Z	Operating	–	–	Operating

Notes 1. Since the bus control pin is also used as a port pin, it is initialized to the port mode (input) after reset.

2. The pin statuses in the idle state inserted after the T3 state in the multiplex bus mode and after the T2 state in the separate bus mode are listed.

3. In separate bus mode: Hi-Z
In multiplex bus mode: Undefined

4. Only in separate bus mode

Remark Hi-Z: High impedance
H: High-level output
L: Low-level output
–: Input without sampling (input acknowledgment not possible)

★ **Table 2-6. Pin Operation Status in Operation Modes of V850ES/KJ1**

Pin \ Operating Status	Reset[Note 1]	HALT Mode	IDLE Mode/ STOP Mode	Idle State[Note 2]	Bus Hold
AD0 to AD15 (PDL0 to PDL15)	Hi-Z	**Note 3**	Hi-Z	Held	Hi-Z
A0 to A15 (P90 to P915)	Hi-Z	Undefined[Note 4]	Hi-Z	Held	Hi-Z
A16 to A23 (PDH0 to PDH7)	Hi-Z	Undefined	Hi-Z	Held	Hi-Z
$\overline{\text{WAIT}}$ (PCM0)	Hi-Z	–	–	–	–
CLKOUT (PCM1)	Hi-Z	Operating	L	Operating	Operating
$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$ (PCS0 to PCS3)	Hi-Z	H	H	Held	Hi-Z
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$ (PCT0, PCT1)	Hi-Z	H	H	H	Hi-Z
$\overline{\text{RD}}$ (PCT4)	Hi-Z	H	H	H	Hi-Z
ASTB (PCT6)	Hi-Z	H	H	H	Hi-Z
$\overline{\text{HLDAK}}$ (PCM2)	Hi-Z	Operating	H	H	L
$\overline{\text{HLDRQ}}$ (PCM3)	Hi-Z	Operating	–	–	Operating

Notes 1. Since the bus control pin is also used as a port pin, it is initialized to the port mode (input) after reset.

2. The pin statuses in the idle state inserted after the T3 state in the multiplex bus mode and after the T2 state in the separate bus mode are listed.

3. In separate bus mode: Hi-Z
In multiplex bus mode: Undefined

4. Only in separate bus mode

Remark Hi-Z: High impedance
H: High-level output
L: Low-level output
–: Input without sampling (input acknowledgment not possible)

2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

(1/3)

Pin	Alternate Function	I/O Circuit Type	Recommended Connection	Product
P00	TOH0	5-A	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.	All products
P01	TOH1			
P02	NMI	5-W		
P03 to P06	INTP0 to INTP3			
P10	ANO0	12-B	Input: Independently connect to AV_{REF1} or AV_{SS} via a resistor. Output: Leave open.	KG1, KJ1
P11	ANO1			
P30	TXD0	5-A	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open	All products
P31	RXD0	5-W		
P32	ASCK0			
P33	TI000/TO00			
P34	TI001			
P35	TI010/TO01			
P36, P37	–	13-B		KG1, KJ1
P38	SDA0[Note]	13-AE		All products
P39	SCL0[Note]			
P40	SI00	5-W		All products
P41	SO00	10-E		
P42	$\overline{SCK00}$	10-F		
P50	TI011/RTP00/KR0	8-A		All products
P51	TI50/RTP01/KR1			
P52	TO50/RTP02/KR2			
P53	SIA0/RTP03/KR3			
P54	SOA0/RTP04/KR4	10-A		
P55	$\overline{SCKA0}$/RTP05/KR5			
P60 to P65	RTP10 to RTP15	5-A		KJ1
P66	SI02	5-W		
P67	SO02	10-E		
P68	$\overline{SCK02}$	10-F		
P69	TI040	5-W		
P610	TI041			
P611	TO04	5-A		
P612	TI050	5-W		
P613	TI051/TO05			
P614, P615	–	13-B		
P70 to P77	ANI0 to ANI7	9-C	Connect to AV_{REF0} or AV_{SS}.	All products
P78 to P715	ANI8 to ANI15			KJ1

Note Only in products with an I^2C bus.

Remark KG1: V850ES/KG1, KJ1: V850ES/KJ1

(2/3)

Pin	Alternate Function	I/O Circuit Type	Recommended Connection	Product
P80	RXD2/SDA1[Note]	10-F	Input: Independently connect to EV_{DD} or EV_{SS} via a resistor. Output: Leave open.	KJ1
P81	TXD2/SCL1[Note]			
P90	A0/TXD1/KR6	8-A		All products
P91	A1/RXD1/KR7			
P92	A2/TI020/TO02			KG1, KJ1
P93	A3/TI021	5-W		
P94	A4/TI030/TO03	8-A		
P95	A5/TI031	5-W		
P96	A6/TI51/TO51	8-A		All products
P97	A7/SI01	5-W		
P98	A8/SO01	10-E		
P99	A9/$\overline{SCK01}$	10-F		
P910	A10/SIA1	5-W		KG1, KJ1
P911	A11/SOA1	10-E		
P912	A12/$\overline{SCKA1}$	10-F		
P913	A13/INTP4	5-W		All products
P914, P915	A14/INTP5, A15/INTP6	8-A		
PCD0 to PCD3	–	5	Input: Independently connect to BV_{DD} or BV_{SS} via a resistor. (For the V850ES/KF1, independently connect to EV_{DD} or EV_{SS} via a resistor.) Output: Leave open	KJ1
PCM0	$\overline{WAIT}$	5		All products
PCM1	CLKOUT			
PCM2	$\overline{HLDAK}$			
PCM3	$\overline{HLDRQ}$			
PCM4,PCM5	–			KJ1
PCS0, PCS1	$\overline{CS0}$, $\overline{CS1}$	5		All products
PCS2, PCS3	$\overline{CS2}$, $\overline{CS3}$			KJ1
PCS4 to PCS7	–			
PCT0	$\overline{WR0}$	5		All products
PCT1	$\overline{WR1}$			
PCT2,PCT3	–			KJ1
PCT4	$\overline{RD}$			All products
PCT5	–			KJ1
PCT6	ASTB			All products
PCT7	–			KJ1
PDL0 to PDL15	AD0 to AD15	5		All products
PDH0 to PDH5	A16 to A21	5		KG1, KJ1
PDH6, PDH7	A22, A23			KJ1
AV_{REF0}	–	–	Directly connect to V_{DD}.	All products
AV_{REF1}	–	–	Directly connect to V_{DD}.	KG1, KJ1
AV_{SS}	–	–	–	All products

Note Only in the μPD703216Y, 703217Y, and 70F3217Y

Remark KG1: V850ES/KG1, KJ1: V850ES/KJ1

(3/3)

Pin	Alternate Function	I/O Circuit Type	Recommended Connection	Target Product
BV_{DD}	–	–	–	KG1, KJ1
BV_{SS}	–	–	–	KG1, KJ1
EV_{DD}	–	–	–	All products
EV_{SS}	–	–	–	All products
IC[Note 1]	–	–	Directly connect to EV_{SS} or V_{SS} or pull down with a 10 kΩ resistor.	All products
$\overline{RESET}$	–	2	–	All products
V_{PP}[Note 2]	–	–	Directly connect to EV_{SS} or V_{SS} or pull down with a 10 kΩ resistor.	All products
V_{DD}	–	–	–	All products
V_{SS}	–	–	–	All products
X1	–	–	–	All products
X2	–	–	–	All products
XT1	–	16	Directly connect to V_{SS}.	All products
XT2	–	16	Leave open.	All products

Notes 1. Only in products with a mask ROM

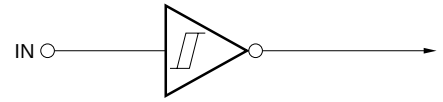
2. Only in products with flash memory

Remark KG1: V850ES/KG1, KJ1: V850ES/KJ1

2.4 Pin I/O Circuits

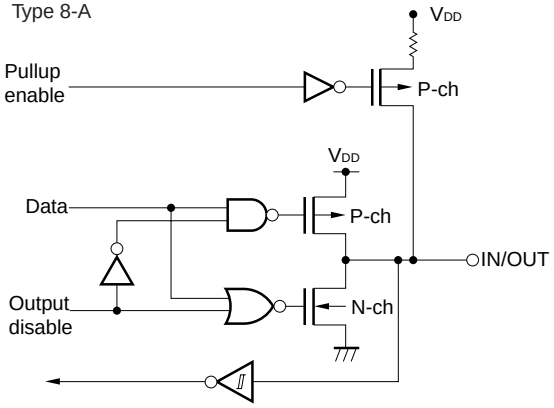
(1/2)

Type 2

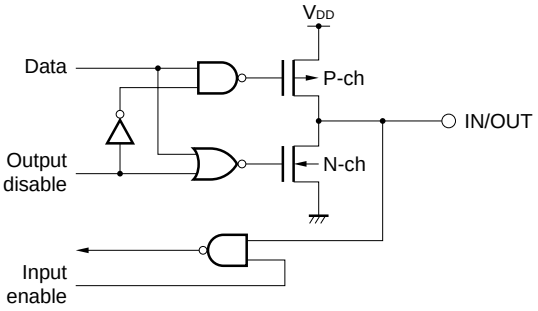


Schmitt-triggered input with hysteresis characteristics

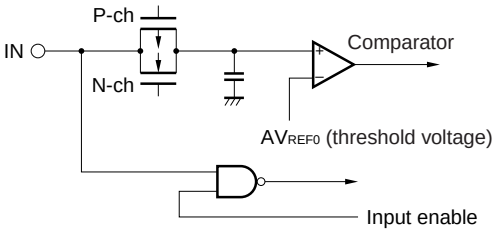
Type 8-A



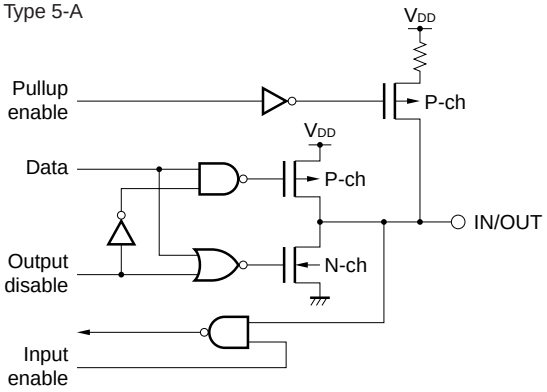
Type 5



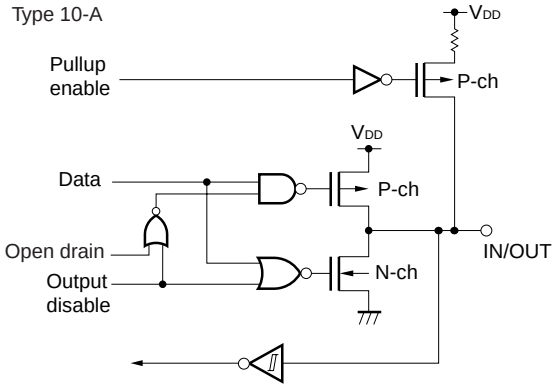
Type 9-C



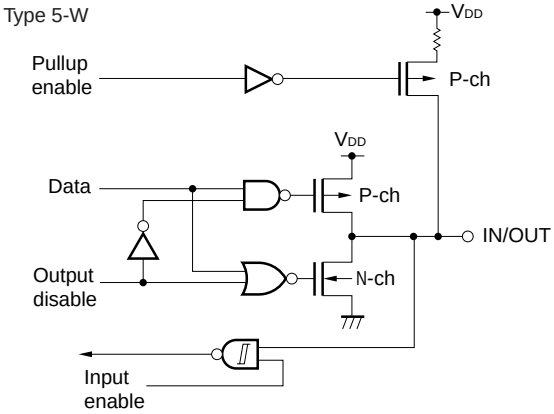
Type 5-A



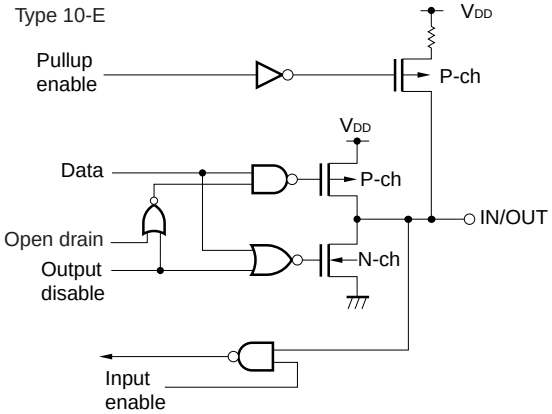
Type 10-A



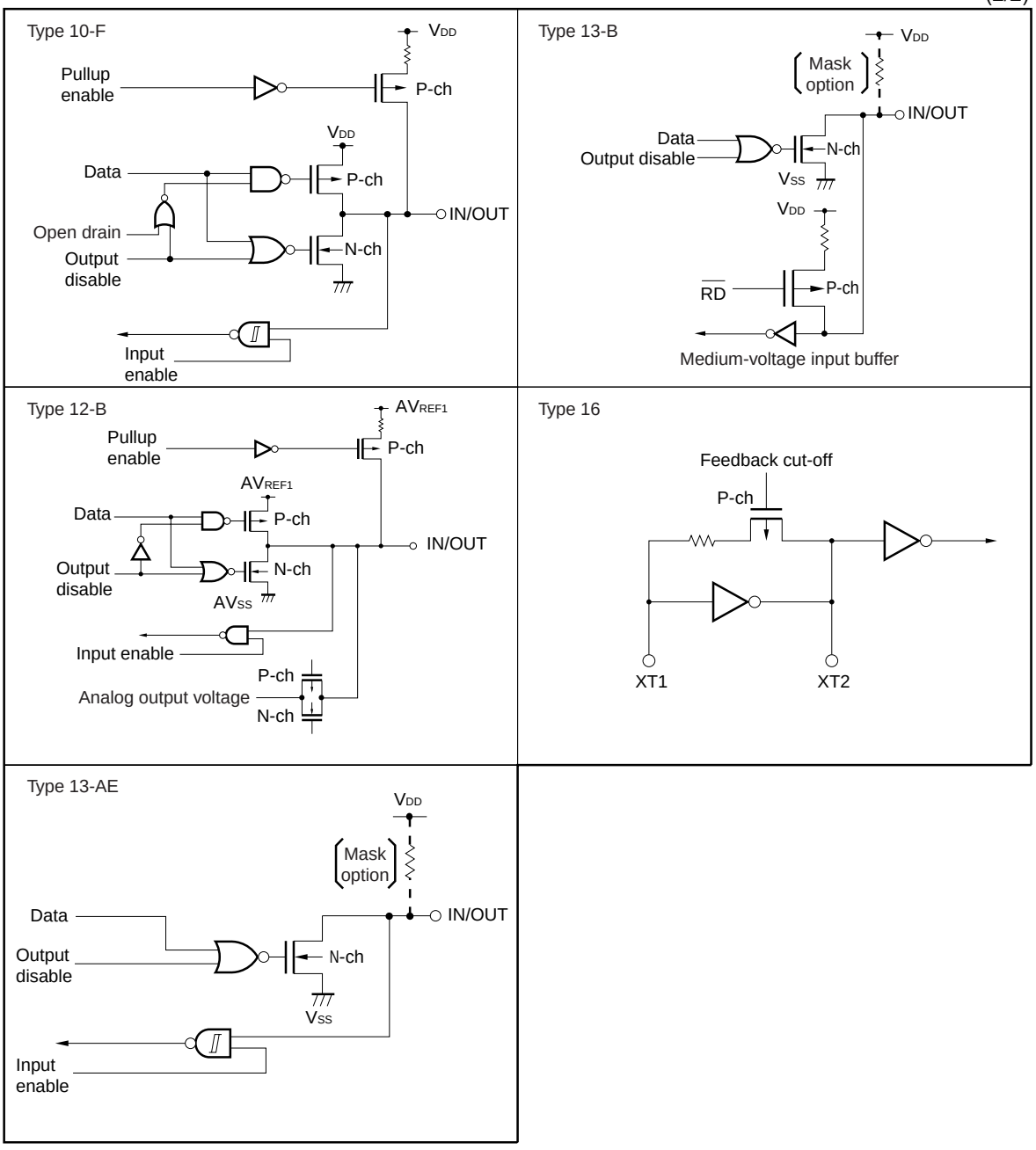
Type 5-W



Type 10-E



(2/2)



Remark Read V_{DD} as EV_{DD} or BV_{DD}. Also, read V_{SS} as EV_{SS} or BV_{SS}.

CHAPTER 3 CPU FUNCTIONS

The CPU of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 is based on the RISC architecture and executes most instructions in one clock cycle by using 5-stage pipeline control.

3.1 Features

- Number of instructions: 83
- Minimum instruction execution time: 50.0 ns (@ 20 MHz operation, 4.5 to 5.5 V, not using regulator)
  62.5 ns (@ 16 MHz operation, 4.0 to 5.5 V, using regulator)
  100 ns (@ 10 MHz operation: 2.7 to 5.5 V, not using regulator)
- Memory space Program (physical address) space: 64 MB linear
  Data (logical address) space: 4 GB linear
  - Memory block division function: 2 MB, 64 KB/Total of 2 blocks (V850ES/KF1)
    : 2 MB, 2 MB/Total of 2 blocks (V850ES/KG1)
    : 2 MB, 2 MB, 4 MB, 8 MB/Total of 4 blocks (V850ES/KJ1)
- General-purpose registers: 32 bits × 32
- Internal 32-bit architecture
- 5-stage pipeline control
- Multiply/divide instructions
- Saturated operation instructions
- 32-bit shift instruction: 1 clock
- Load/store instruction with long/short format
- Four types of bit manipulation instructions
  - SET1
  - CLR1
  - NOT1
  - TST1

3.2 CPU Register Set

The CPU registers of the V850ES/KF1, V850ES/KG1 and V850ES/KJ1 can be classified into two categories: a general-purpose program register set and a dedicated system register set. All the registers have 32-bit width.

For details, refer to the **V850ES Architecture User's Manual**.

(1) Program register set

31		0
r0	(Zero register)	
r1	(Assembler-reserved register)	
r2		
r3	(Stack pointer (SP))	
r4	(Global pointer (GP))	
r5	(Text pointer (TP))	
r6		
r7		
r8		
r9		
r10		
r11		
r12		
r13		
r14		
r15		
r16		
r17		
r18		
r19		
r20		
r21		
r22		
r23		
r24		
r25		
r26		
r27		
r28		
r29		
r30	(Element pointer (EP))	
r31	(Link pointer (LP))	

31		0
PC	(Program counter)	

(2) System register set

31		0
EIPC	(Interrupt status saving register)	
EIPSW	(Interrupt status saving register)	
FEPC	(NMI status saving register)	
FEPSW	(NMI status saving register)	
ECR	(Interrupt source register)	
PSW	(Program status word)	
CTPC	(CALLT execution status saving register)	
CTPSW	(CALLT execution status saving register)	
DBPC	(Exception/debug trap status saving register)	
DBPSW	(Exception/debug trap status saving register)	
CTBP	(CALLT base pointer)	

3.2.1 Program register set

The program register set includes general-purpose registers and a program counter.

(1) General-purpose registers (r0 to r31)

Thirty-two general-purpose registers, r0 to r31, are available. All of these registers can be used as a data variable or address variable.

However, r0 and r30 are implicitly used by instructions and care must be exercised when using these registers. r0 always holds 0 and is used for operations that use 0 and offset 0 addressing. r30 is used as a base pointer when performing memory access with the SLD and SST instructions.

Also, r1, r3 to r5, and r31 are implicitly used by the assembler and C compiler. Therefore, before using these registers, their contents must be saved so that they are not lost, and they must be restored to the registers after the registers have been used. There are cases when r2 is used by the real-time OS. If r2 is not used by the real-time OS, r2 can be used as a variable register.

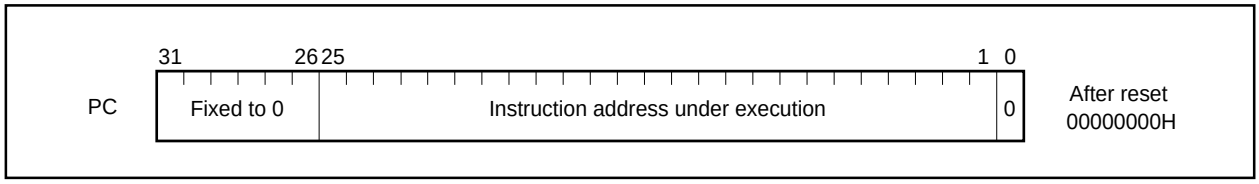
Table 3-1. Program Registers

Name	Usage	Operation
r0	Zero register	Always holds 0
r1	Assembler-reserved register	Working register for generating 32-bit immediate
r2	Address/data variable register (when r2 is not used by the real-time OS to be used)	
r3	Stack pointer	Used to generate stack frame when function is called
r4	Global pointer	Used to access global variable in data area
r5	Text pointer	Register to indicate the start of the text area (area for placing program code)
r6 to r29	Address/data variable register	
r30	Element pointer	Base pointer when memory is accessed
r31	Link pointer	Used by compiler when calling function
PC	Program counter	Holds instruction address during program execution

(2) Program counter (PC)

This register holds the address of the instruction under execution. The lower 26 bits of this register are valid, and bits 31 to 26 are fixed to 0. If a carry occurs from bit 25 to bit 26, it is ignored.

Bit 0 is fixed to 0, and branching to an odd address cannot be performed.



3.2.2 System register set

System registers control the status of the CPU and hold interrupt information.

Read from and write to system registers are performed by setting the system register numbers shown below with the system register load/store instructions (LDSR, STSR instructions).

Table 3-2. System Register Numbers

System Register No.	System Register Name	Operand Specification Enabled	
		LDSR Instruction	STSR Instruction
0	Interrupt status saving register (EIPC)[Note 1]	Yes	Yes
1	Interrupt status saving register (EIPSW)[Note 1]	Yes	Yes
2	NMI status saving register (FEPC)[Note 1]	Yes	Yes
3	NMI status saving register (FEPSW)[Note 1]	Yes	Yes
4	Interrupt source register (ECR)	No	Yes
5	Program status word (PSW)	Yes	Yes
6 to 15	Reserved numbers for future function expansion (The operation is not guaranteed if accessed.)	No	No
16	CALLT execution status saving register (CTPC)	Yes	Yes
17	CALLT execution status saving register (CTPSW)	Yes	Yes
18	Exception/debug trap status saving register (DBPC)	Yes[Note 2]	Yes
19	Exception/debug trap status saving register (DBPSW)	Yes[Note 2]	Yes
20	CALLT base pointer (CTBP)	Yes	Yes
21 to 31	Reserved numbers for future function expansion (The operation is not guaranteed if accessed.)	No	No

Notes 1. Since only one set of these registers is available, the contents of this register must be saved by the program when multiple interrupt servicing is enabled.

2. Can be accessed only during the period from the DBTRAP instruction to the DBRETI instruction.

Caution Even if bit 0 of EIPC, FEPC, or CTPC is set (1) by the LDSR instruction, bit 0 is ignored during return with the RETI instruction following interrupt servicing (because bit 0 of PC is fixed to 0). When setting a value to EIPC, FEPC, and CTPC, set an even number (bit 0 = 0).

(1) Interrupt status saving registers (EIPC, EIPSW)

There are two interrupt status saving registers, EIPC and EIPSW.

Upon occurrence of a software exception or a maskable interrupt, the contents of the program counter (PC) are saved to EIPC and the contents of the program status word (PSW) are saved to EIPSW (upon occurrence of a non-maskable interrupt (NMI), the contents are saved to the NMI status saving registers (FEPC, FEPSW)).

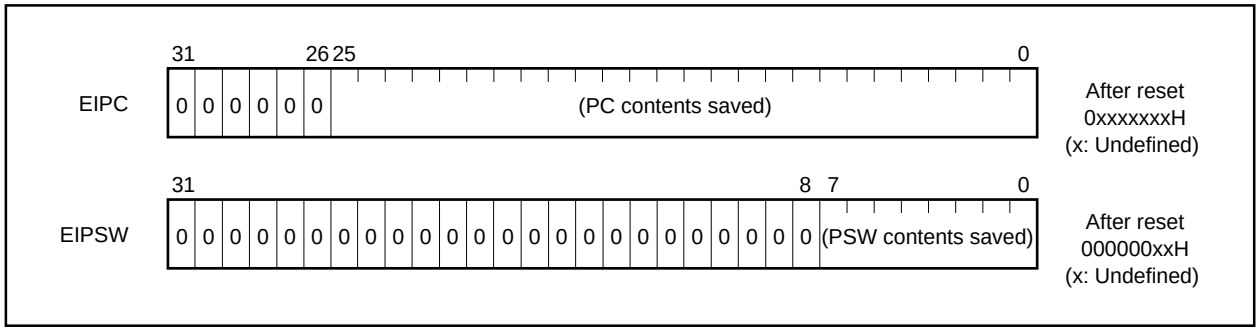
The address of the next instruction following the instruction executed when a software exception or maskable interrupt occurs is saved to EIPC, except for some instructions (refer to **19.9 Period in Which Interrupts Are Not Acknowledged by CPU**).

The current PSW contents are saved to EIPSW.

Since there is only one set of interrupt status saving registers, the contents of these registers must be saved by the program when multiple interrupt servicing is enabled.

Bits 31 to 26 of EIPC and bits 31 to 8 of EIPSW are reserved (fixed to 0) for future function expansion.

When the RETI instruction is executed, the values in EIPC and EIPSW are restored to the PC and PSW, respectively.



(2) NMI status saving registers (FEPC, FEPSW)

There are two NMI status saving registers, FEPC and FEPSW.

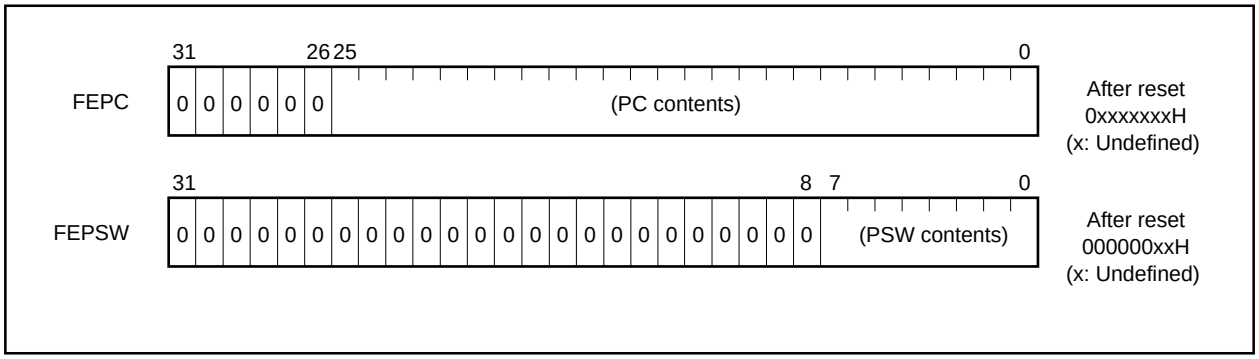
Upon occurrence of a non-maskable interrupt (NMI), the contents of the program counter (PC) are saved to FEPC and the contents of the program status word (PSW) are saved to FEPSW.

The address of the next instruction following the instruction executed when a non-maskable interrupt occurs is saved to FEPC, except for some instructions.

The current PSW contents are saved to FEPSW.

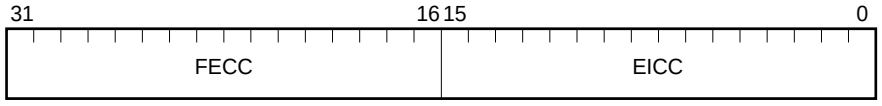
Since there is only one set of NMI status saving registers, the contents of these registers must be saved by the program when multiple interrupt servicing is performed.

Bits 31 to 26 of FEPC and bits 31 to 8 of FEPSW are reserved (fixed to 0) for future function expansion.



(3) Interrupt source register (ECR)

Upon occurrence of an interrupt or an exception, the interrupt source register (ECR) holds the source of an interrupt or an exception. The value held by ECR is the exception code coded for each interrupt source. This register is a read-only register, and thus data cannot be written to it using the LDSR instruction.



Bit position	Bit name	Description
31 to 16	FECC	Non-maskable interrupt (NMI) exception code
15 to 0	EICC	Exception, maskable interrupt exception code

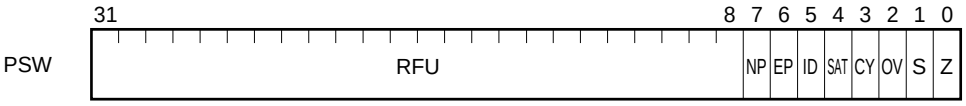
(4) Program status word (PSW)

The program status word (PSW) is a collection of flags that indicate the program status (instruction execution result) and the CPU status.

When the contents of this register are changed using the LDSR instruction, the new contents become valid immediately following completion of LDSR instruction execution. Interrupt request acknowledgment is held pending while a write to the PSW is being executed by the LDSR instruction.

Bits 31 to 8 are reserved (fixed to 0) for future function expansion.

(1/2)



Bit position	Flag name	Description
31 to 8	RFU	Reserved field. Fixed to 0.
7	NP	Indicates that non-maskable interrupt (NMI) servicing is in progress. This flag is set to 1 when an NMI request is acknowledged, and disables multiple interrupts. 0: NMI servicing not in progress 1: NMI servicing in progress
6	EP	Indicates that exception processing is in progress. This flag is set to 1 when an exception occurs. Moreover, interrupt requests can be acknowledged even when this bit is set. 0: Exception processing not in progress 1: Exception processing in progress
5	ID	Indicates whether maskable interrupt request acknowledgment is enabled. 0: Interrupt enabled 1: Interrupt disabled
4	SAT[Note]	Indicates that the result of executing a saturated operation instruction has overflowed and that the calculation result is saturated. Since this is a cumulative flag, it is set to 1 when the result of a saturated operation instruction becomes saturated, and it is not cleared to 0 even if the operation results of successive instructions do not become saturated. This flag is neither set nor cleared when arithmetic operation instructions are executed. 0: Not saturated 1: Saturated
3	CY	Indicates whether carry or borrow occurred as the result of an operation. 0: No carry or borrow occurred 1: Carry or borrow occurred
2	OV[Note]	Indicates whether overflow occurred during an operation. 0: No overflow occurred 1: Overflow occurred.
1	S[Note]	Indicates whether the result of an operation is negative. 0: Operation result is positive or 0. 1: Operation result is negative.
0	Z	Indicates whether operation result is 0. 0: Operation result is not 0. 1: Operation result is 0.

Remark **Note** is explained on the following page.

(2/2)

Note During saturated operation, the saturated operation results are determined by the contents of the OV flag and S flag. The SAT flag is set (to 1) only when the OV flag is set (to 1) during saturated operation.

Operation result status	Flag status			Saturated operation result
	SAT	OV	S	
Maximum positive value exceeded	1	1	0	7FFFFFFFH
Maximum negative value exceeded	1	1	1	80000000H
Positive (maximum value not exceeded)	Holds value before operation	0	0	Actual operation result
Negative (maximum value not exceeded)			1	

(5) CALLT execution status saving registers (CTPC, CTPSW)

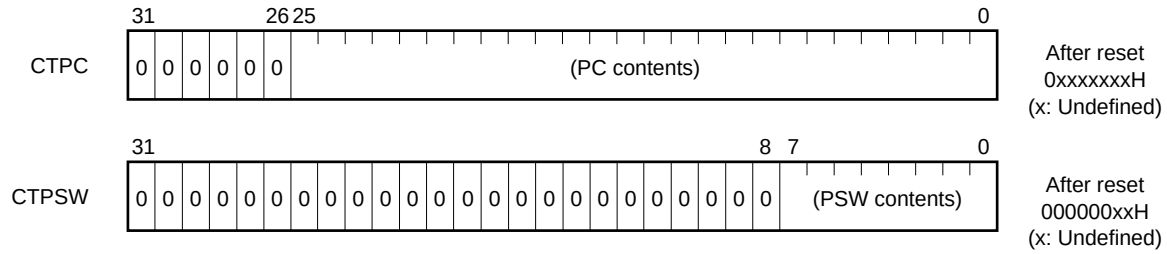
There are two CALLT execution status saving registers, CTPC and CTPSW.

When the CALLT instruction is executed, the contents of the program counter (PC) are saved to CTPC, and the program status word (PSW) contents are saved to CTPSW.

The contents saved to CTPC consist of the address of the next instruction after the CALLT instruction.

The current PSW contents are saved to CTPSW.

Bits 31 to 26 CTPC and bits 31 to 8 of CTPSW are reserved (fixed to 0) for future function expansion.



(6) Exception/debug trap status saving registers (DBPC, DBPSW)

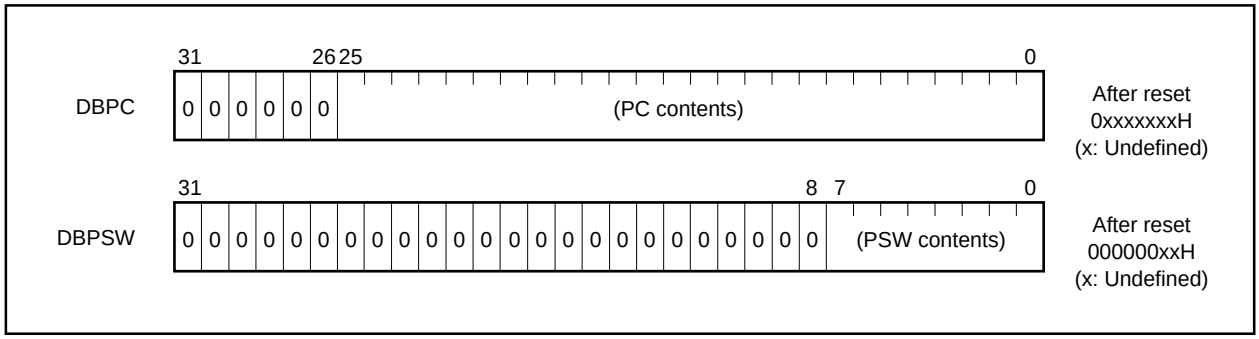
There are two exception/debug trap status saving registers, DBPC and DBPSW.

Upon occurrence of an exception trap or debug trap, the contents of the program counter (PC) are saved to DBPC, and the program status word (PSW) contents are saved to DBPSW.

The contents saved to DBPC consist of the address of the next instruction after the instruction executed when an exception trap or debug trap occurs.

The current PSW contents are saved to DBPSW.

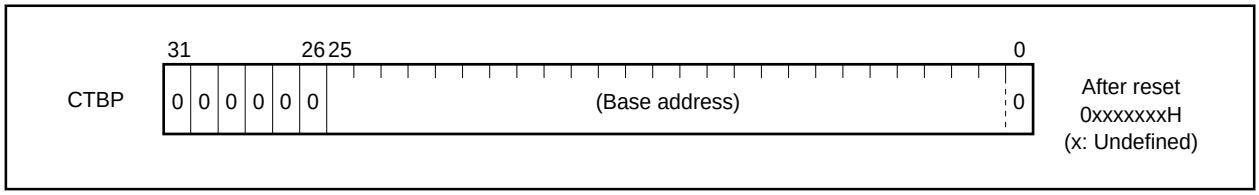
Bits 31 to 26 of DBPC and bits 31 to 8 of DBPSW are reserved (fixed to 0) for future function expansion.



(7) CALLT base pointer (CTBP)

The CALLT base pointer (CTBP) is used to specify table addresses and generate target addresses (bit 0 is fixed to 0).

Bits 31 to 26 are reserved (fixed to 0) for future function expansion.



3.3 Operation Modes

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 have the following operating modes.

(1) Normal operating mode

After the system has been released from the reset state, the pins related to the bus interface are set to the port mode, execution branches to the reset entry address of the internal ROM, and instruction processing is started.

(2) Flash memory programming mode

(μPD70F3210, 70F3210Y: V850ES/KF1
μPD70F3214, 70F3214Y: V850ES/KG1
μPD70F3217, 70F3217Y: V850ES/KJ1)

The internal flash memory can be written or erased when 10 V ±0.3 V is applied to the V_{PP} pin.

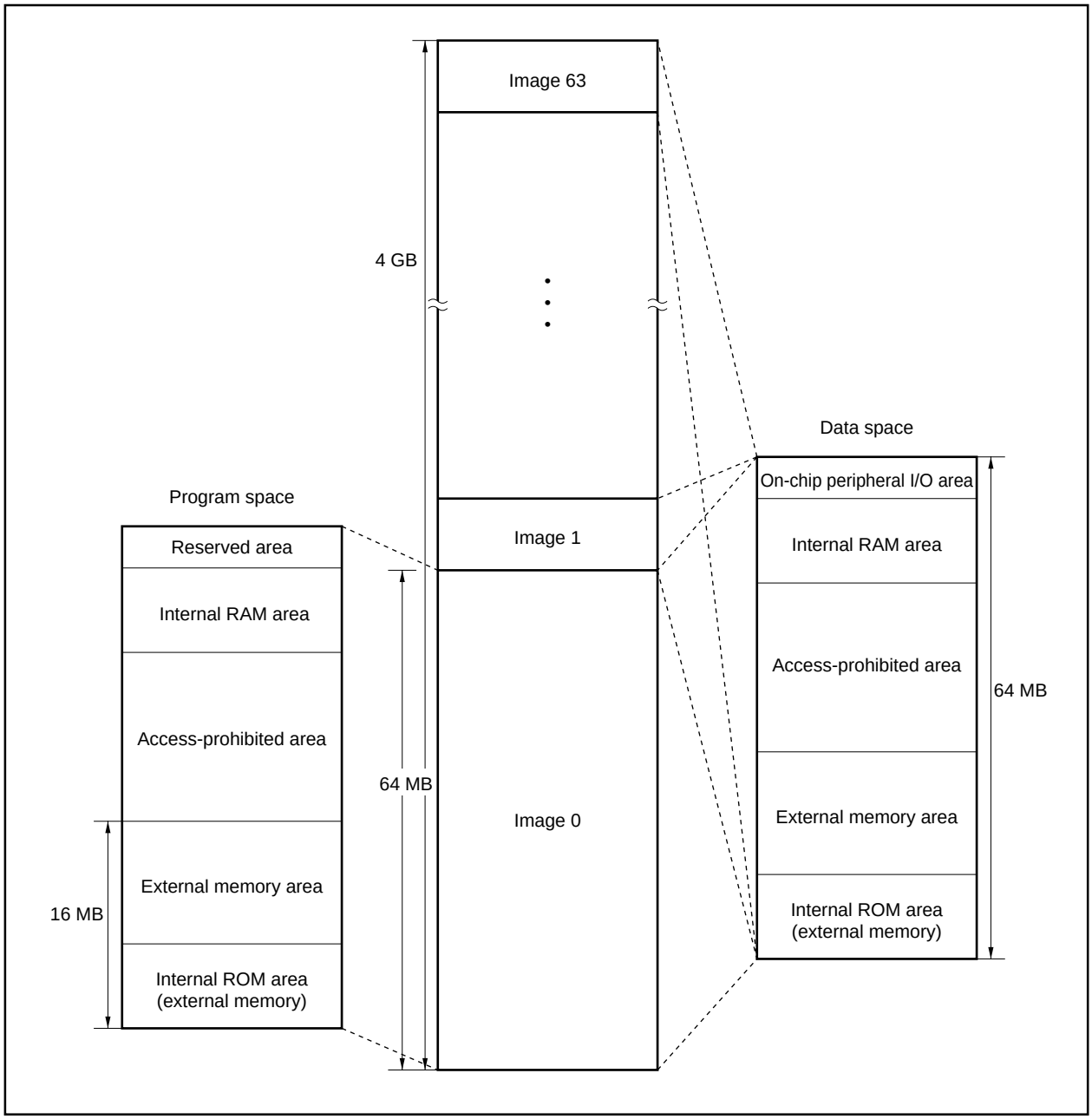
V_{PP}	Operating Mode
0	Normal operation mode
10±0.3 V	Flash memory programming mode
V_{DD}	Setting prohibited

3.4 Address Space

3.4.1 CPU address space

Up to 16 MB of external memory area in a linear address space (program area) of up to 16 MB, internal ROM area, and internal RAM area are supported for instruction address addressing. During operand addressing (data access), up to 4 GB of linear address space (data space) is supported. However, the 4 GB address space is viewed as 64 images of a 64 MB physical address space. In other words, the same 64 MB physical address space is accessed regardless of the value of bits 31 to 26.

Figure 3-1. Address Space Image



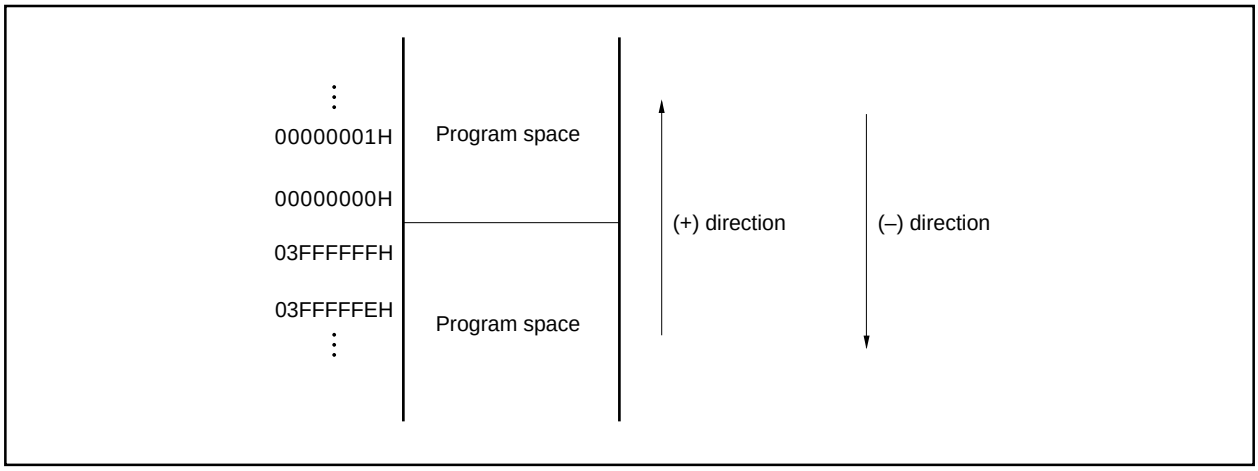
3.4.2 Wraparound of CPU address space

(1) Program space

Of the 32 bits of the program counter (PC), the higher 6 bits are fixed to 0 and only the lower 26 bits are valid. Even if a carry or borrow occurs from bit 25 to bit 26 as a result of branch address calculation, the higher 6 bits ignore this and remain 0.

Therefore, the lower-limit address of the program space, 00000000H, and the upper-limit address, 03FFFFFFH, are contiguous addresses, and the program space is wrapped around at the boundary of these addresses.

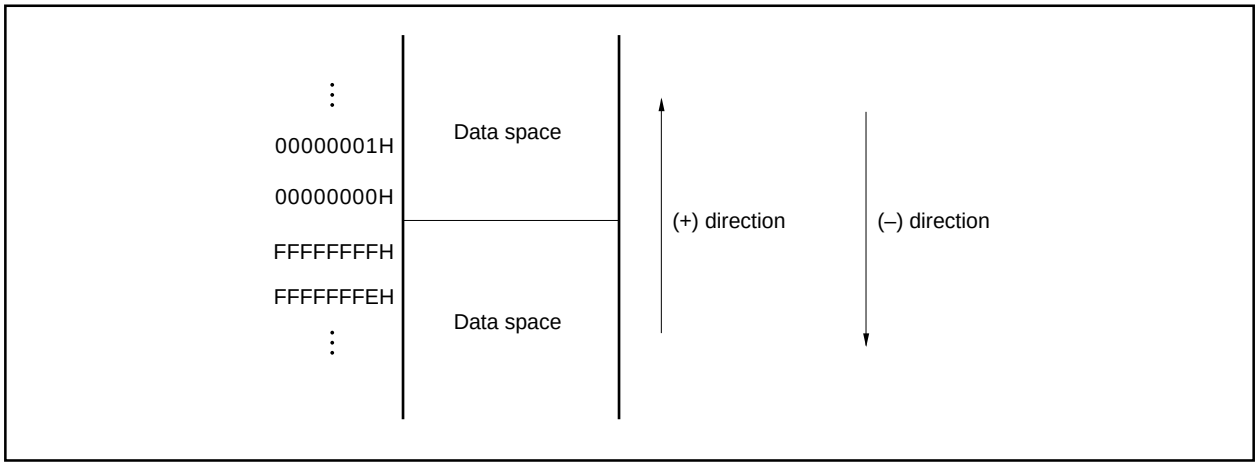
Caution No instructions can be fetched from the 4 KB area of 03FFF000H to 03FFFFFFH because this area is an on-chip peripheral I/O area. Therefore, do not execute any branch operation instructions in which the destination address will reside in any part of this area.



(2) Data space

The result of an operand address calculation that exceeds 32 bits is ignored.

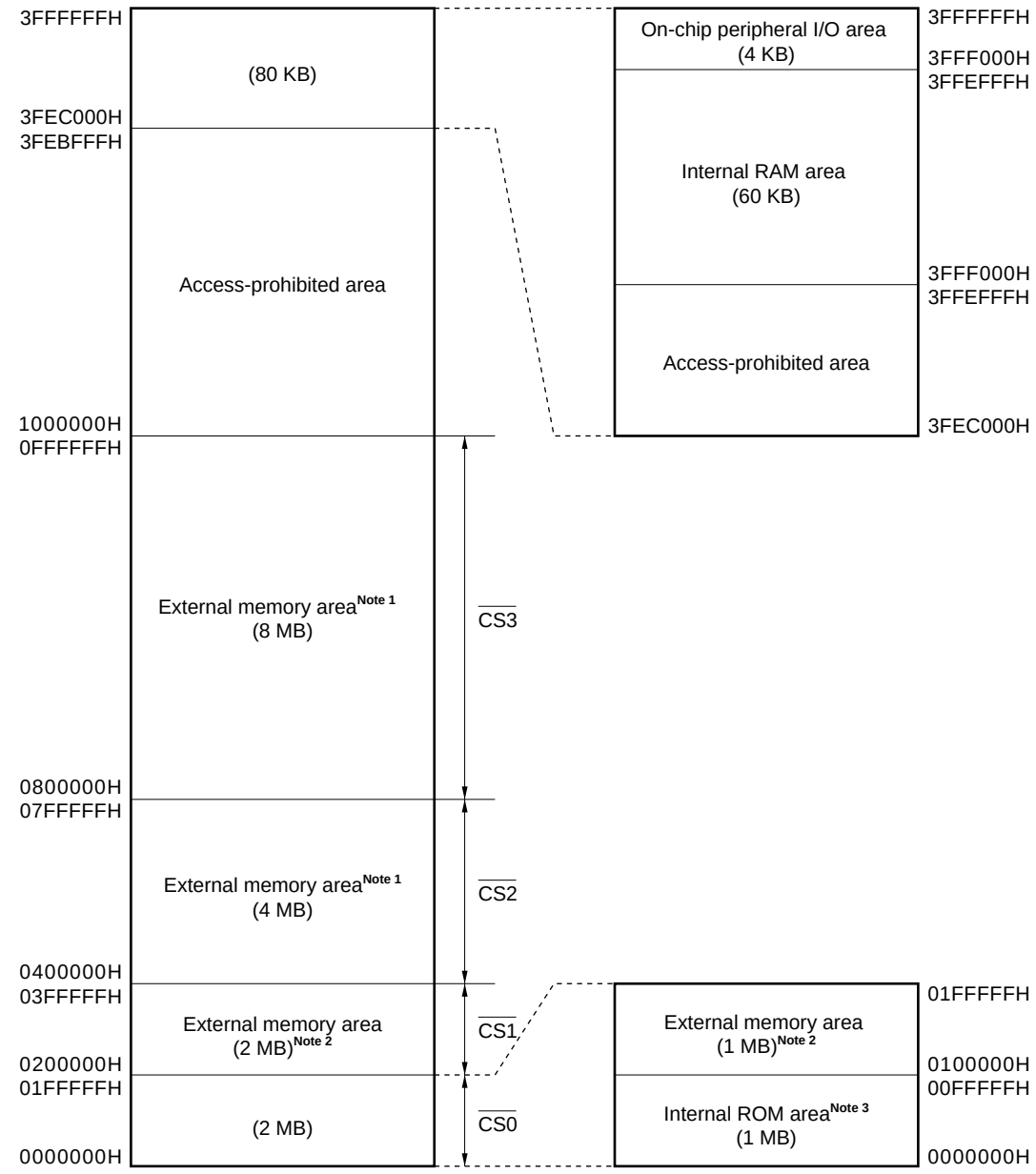
Therefore, the lower-limit address of the data space, address 00000000H, and the upper-limit address, FFFFFFFFH, are contiguous addresses, and the data space is wrapped around at the boundary of these addresses.



3.4.3 Memory map

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 have reserved areas as shown below.

Figure 3-2. Data Memory Map (Physical Addresses)

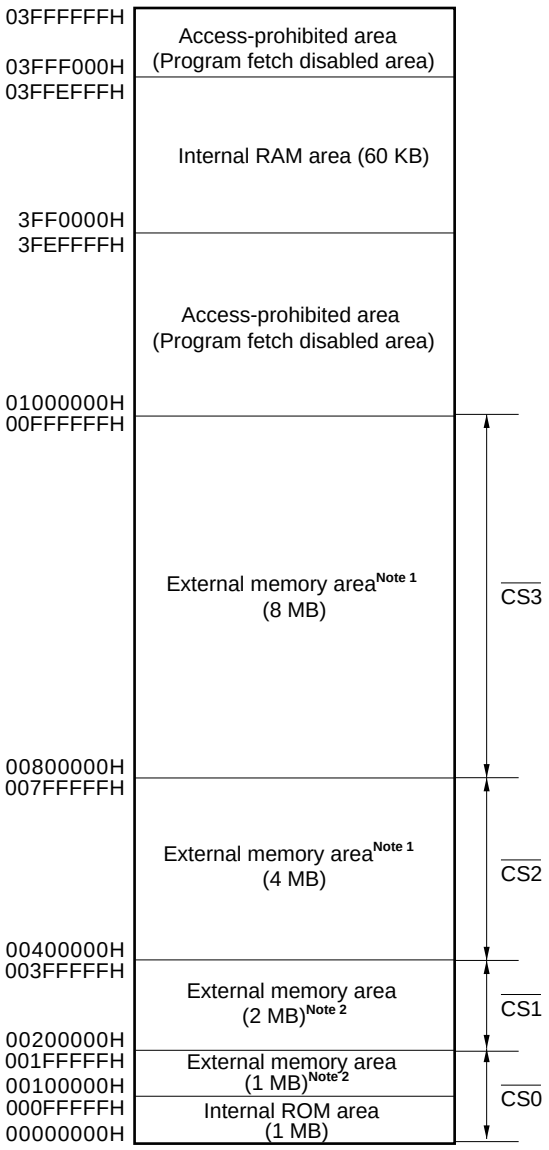


Notes 1. Only in the V850ES/KJ1. Access-prohibited area in the V850ES/KF1 and V850ES/KG1.

2. 64 KB in the V850ES/KF1

3. Fetch access and read access to addresses 0000000H to 00FFFFFH is performed for the internal ROM area, but in the case of data write access, it is performed for an external memory area.

Figure 3-3. Program Memory Map



Notes 1. Only in the V850ES/KJ1. Access-prohibited area in the V850ES/KF1 and V850ES/KG1.

2. 64 KB in the V850ES/KF1

3.4.4 Areas

(1) Internal ROM area

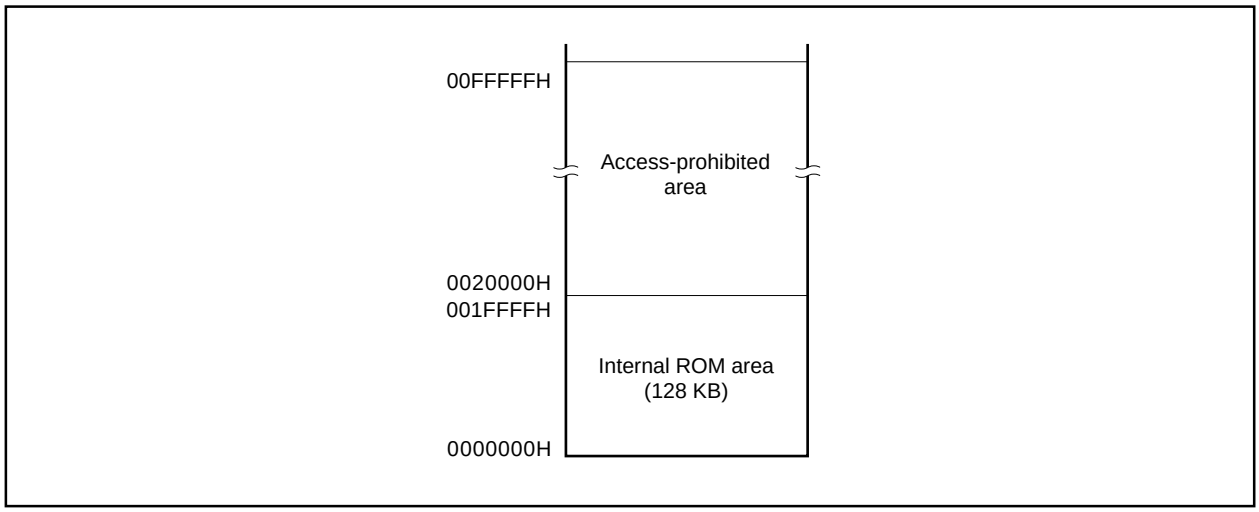
An area of 1 MB from 0000000H to 00FFFFFH is reserved for the internal ROM area.

(a) Internal ROM (128 KB)

A 128 KB area from 0000000H to 001FFFFH is provided in the following products.
Addresses 0020000H to 00FFFFFH are an access-prohibited area.

- V850ES/KF1 (μPD703210, 703210Y, 70F3210, 70F3210Y)
- V850ES/KG1 (μPD703214, 703214Y, 70F3214, 70F3214Y)
- V850ES/KJ1 (μPD703217, 703217Y, 70F3217, 70F3217Y)

Figure 3-4. Internal ROM/Internal Flash Memory Area (128 KB)

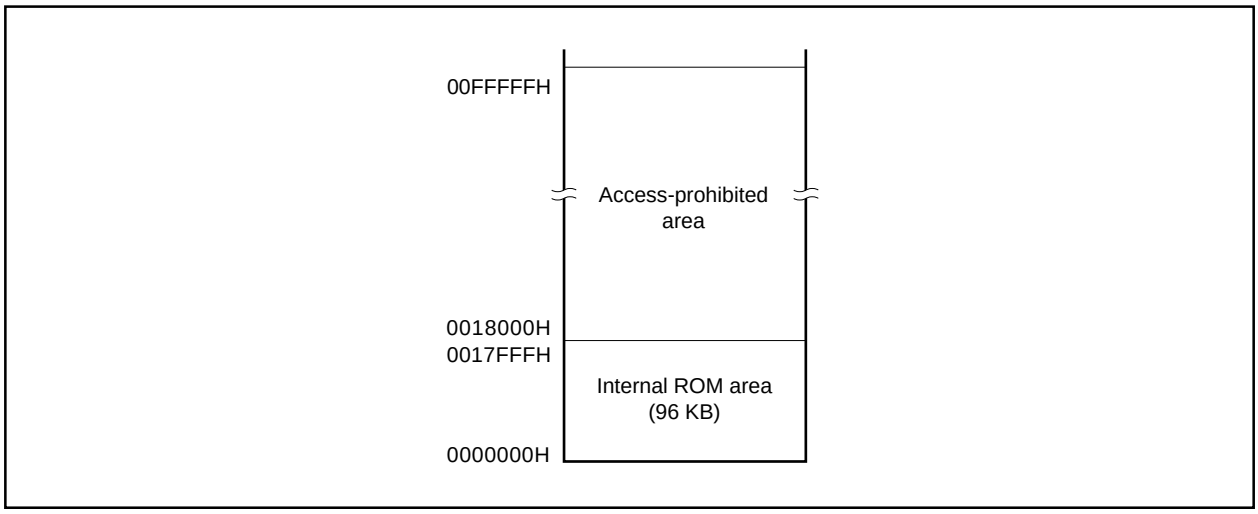


(b) Internal ROM (96 KB)

A 96 KB area from 0000000H to 0017FFFH is provided in the following products.
Addresses 0018000H to 00FFFFFH are an access-prohibited area.

- V850ES/KF1 (μPD703209, 703209Y)
- V850ES/KG1 (μPD703213, 703213Y)
- V850ES/KJ1 (μPD703216, 703216Y)

Figure 3-5. Internal ROM Area (96 KB)

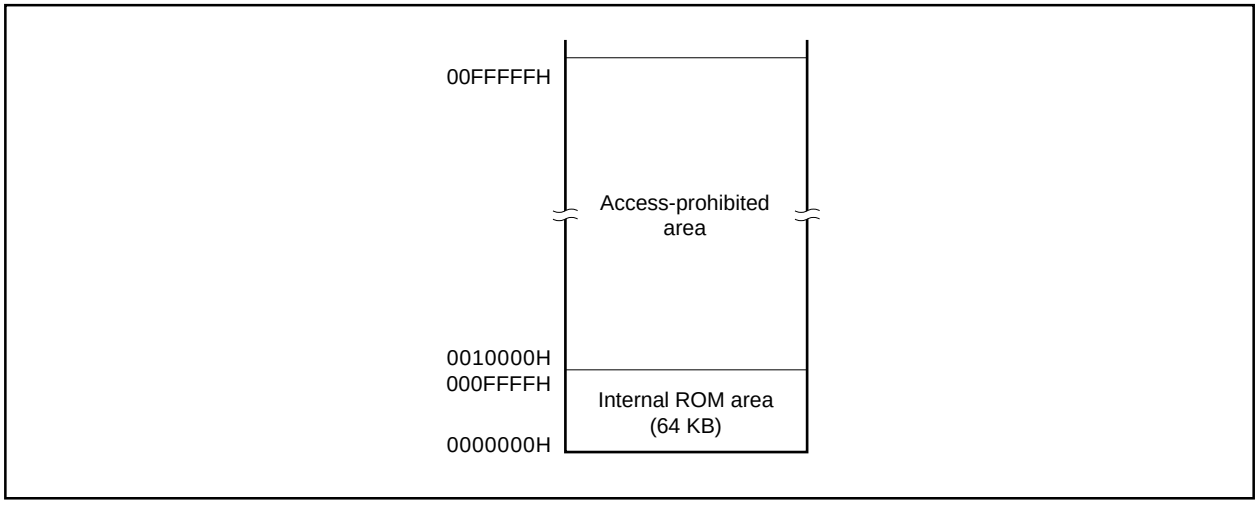


(c) Internal ROM (64 KB)

A 64 KB area from 000000H to 000FFFFH is provided in the following products.
Addresses 0010000 to 00FFFFFH are an access-prohibited area.

- V850ES/KF1 (μPD703208, 703208Y)
- V850ES/KG1 (μPD703212, 703212Y)

Figure 3-6. Internal ROM Area (64 KB)



(2) Internal RAM area

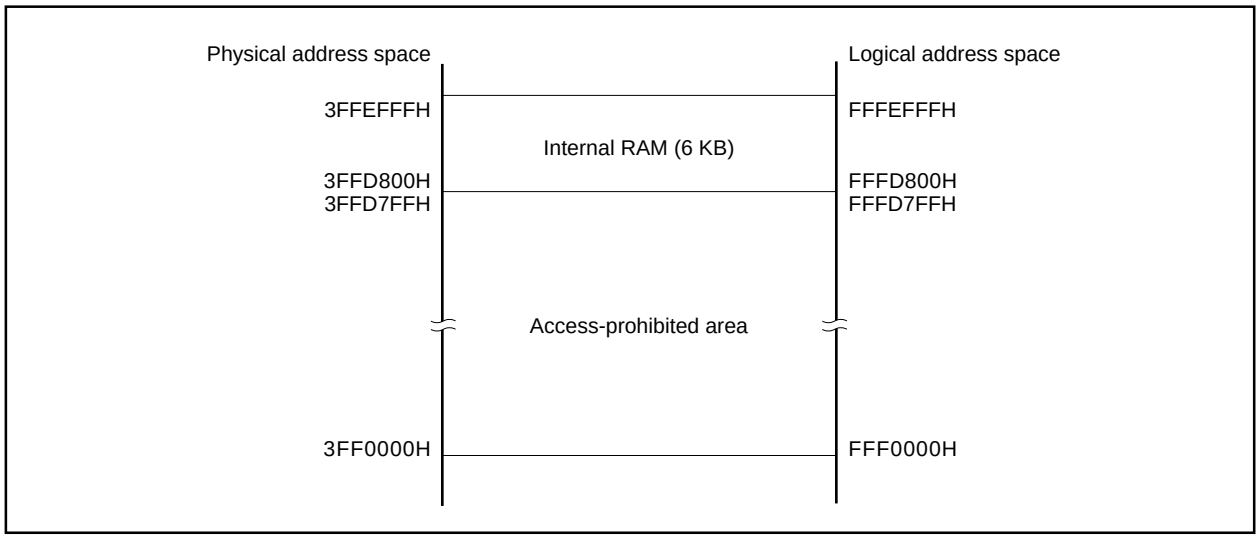
An area of 60 KB maximum from 3FF0000H to 3FFEFFFH is reserved for the internal RAM area.

(a) Internal RAM (6 KB)

A 6 KB area from 3FFD800H to 3FFEFFFH is provided as physical internal RAM.
Addresses 3FF0000H to 3FFD7FFH are an access-prohibited area.

- V850ES/KF1 (μPD703210, 703210Y, 70F3210, 70F3210Y)
- V850ES/KG1 (μPD703214, 703214Y, 70F3214, 70F3214Y)
- V850ES/KJ1 (μPD703216, 703216Y, 703217, 703217Y, 70F3217, 70F3217Y)

Figure 3-7. Internal RAM Area (6 KB)

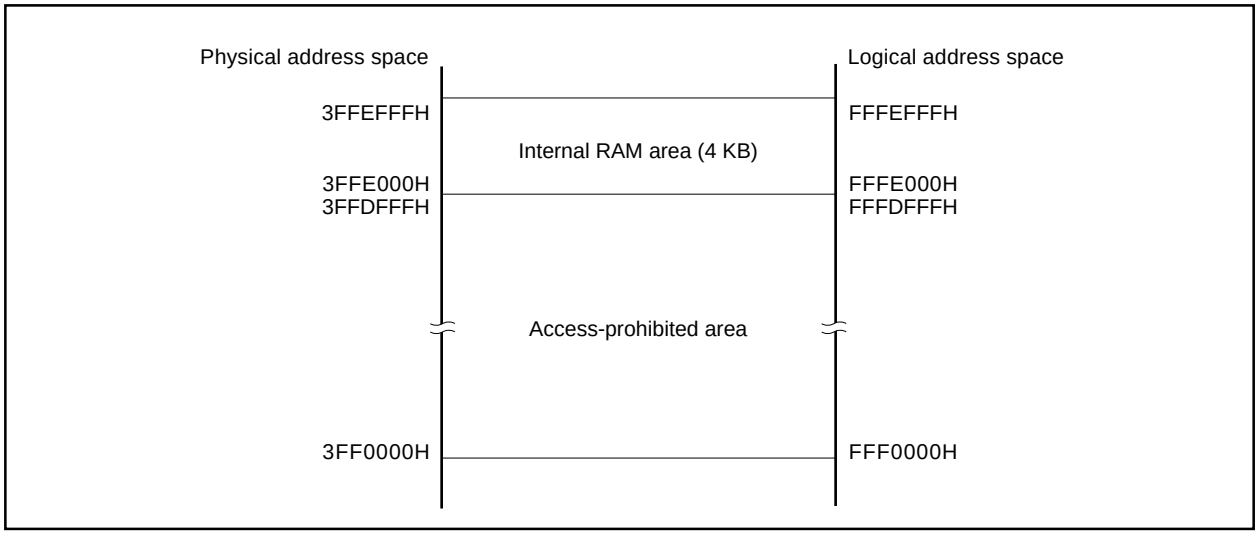


(b) Internal RAM area (4 KB)

A 4 KB area from 3FFE000H to 3FFEFFFH is provided as physical internal RAM in the following products. Addresses 3FF0000H to 3FFDFFFH are an access-prohibited area.

- V850ES/KF1 (μPD703218, 703218Y, 703219, 703219Y)
- V850ES/KG1 (μPD703212, 703212Y, 703213, 70F3213Y)

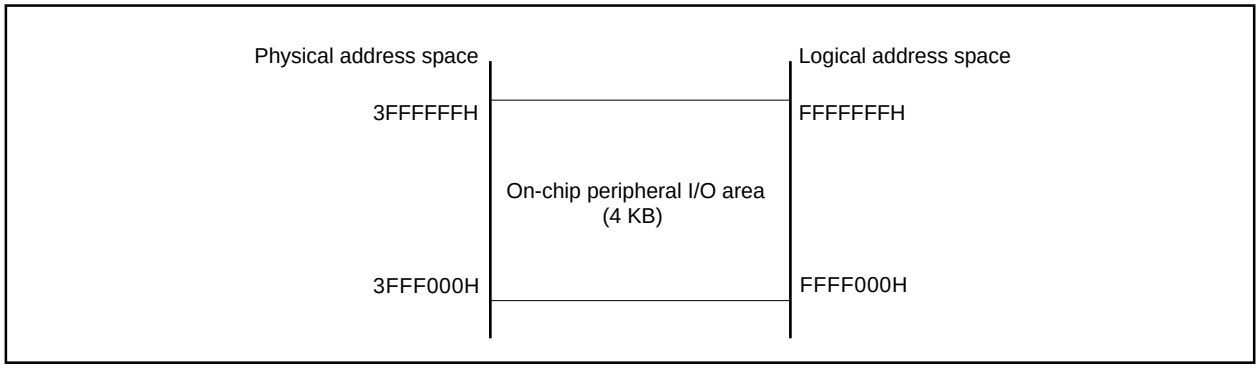
Figure 3-8. Internal RAM Area (4 KB)



(3) On-chip peripheral I/O area

A 4 KB area from 3FFF000H to 3FFFFFFH is reserved as the on-chip peripheral I/O area.

Figure 3-9. On-Chip Peripheral I/O Area



Peripheral I/O registers assigned with functions such as on-chip peripheral I/O operation mode specification and state monitoring are mapped to the on-chip peripheral I/O area. Program fetches are not allowed in this area.

Cautions 1. If word access of a register is attempted, halfword access to the word area is performed twice, first for the lower bits, then for the higher bits, ignoring the lower 2 address bits.

2. If a register that can be accessed in byte units is accessed in halfword units, the higher 8 bits become undefined if the access is a read operation. If a write access is performed, only the data in the lower 8 bits is written to the register.

3. Addresses that are not defined as registers are reserved for future expansion. If these addresses are accessed, the operation is undefined and not guaranteed.

(4) External memory area

15 MB (0100000H to 0FFFFFFH) are provided as the external memory area. For details, refer to **CHAPTER 5 BUS CONTROL FUNCTION**.

★ 3.4.5 Recommended use of address space

The architecture of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 requires that a register that serves as a pointer be secured for address generation when operand data in the data space is accessed. The address stored in this pointer ±32 KB can be directly accessed by an instruction for operand data. Because the number of general-purpose registers that can be used as a pointer is limited, however, by keeping the performance from dropping during address calculation when a pointer value is changed, as many general-purpose registers as possible can be secured for variables, and the program size can be reduced.

(1) Program space

Of the 32 bits of the PC (program counter), the higher 6 bits are fixed to 0, and only the lower 26 bits are valid. Regarding the program space, therefore, a 64 MB space of contiguous addresses starting from 00000000H unconditionally corresponds to the memory map.

To use the internal RAM area as the program space, access following addresses.

RAM Size	Access Address
4 KB	3FFE000H to 3FFEFFFH
6 KB	3FFD800H to 3FFEFFFH

(2) Data space

With the V850ES/KF1, V850ES/KG1, and V850ES/KJ1, it seems that there are sixty-four 64 MB address spaces on the 4 GB CPU address space. Therefore, the least significant bit (bit 25) of a 26-bit address is sign-extended to 32 bits and allocated as an address.

(a) Application example of wraparound

If R = r0 (zero register) is specified for the LD/ST disp16 [R] instruction, a range of addresses 00000000H ±32 KB can be addressed by sign-extended disp16. All the resources, including the internal hardware, can be addressed by one pointer.

The zero register (r0) is a register fixed to 0 by hardware, and practically eliminates the need for registers dedicated to pointers.

Example: μPD703217, 703217Y

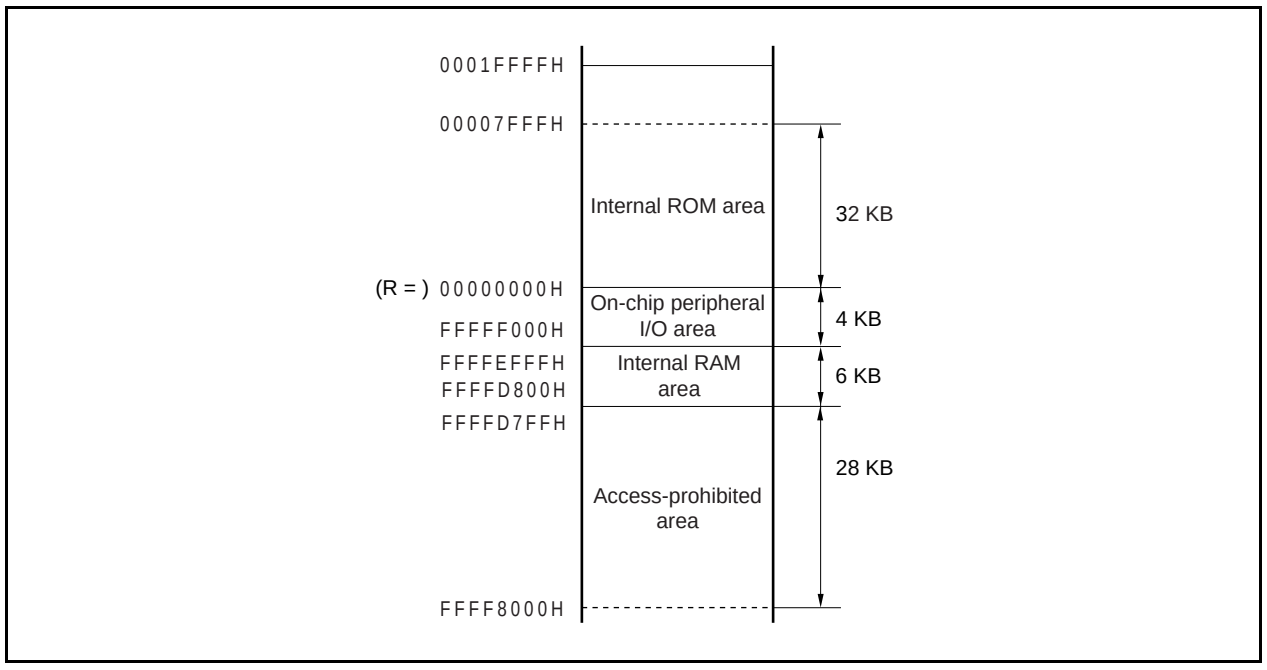
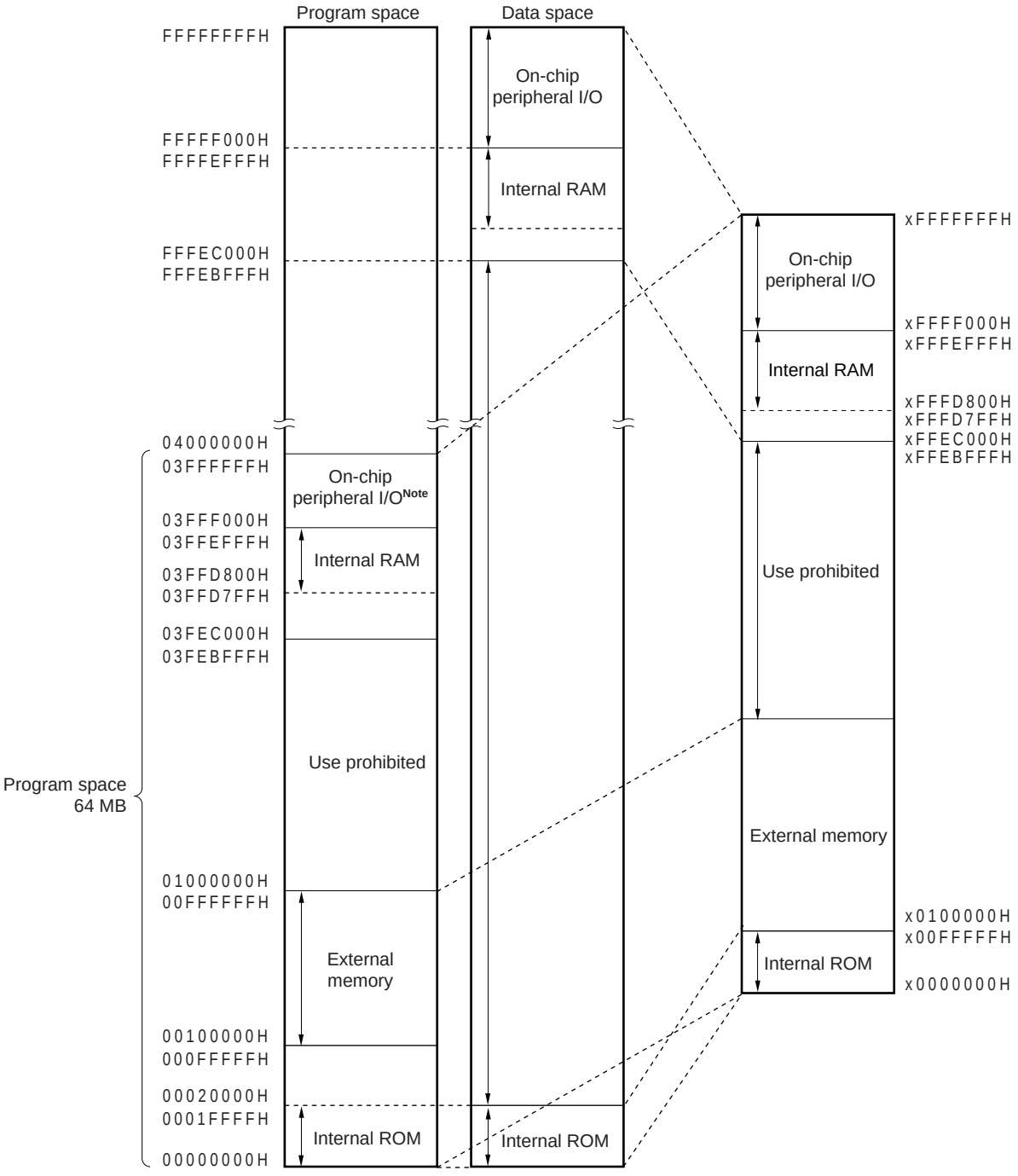


Figure 3-10. Recommended Memory Map



Note Access to this area is prohibited. To access the on-chip peripheral I/O in this area, specify addresses FFFF000H to FFFFFFFH.

Remarks 1. ↕ indicates the recommended area.

2. This figure is the recommended memory map of the μPD703217 and 703217Y.

3.4.6 Peripheral I/O registers

(1/12)

Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFF004H	Port DL register	PDL	R/W			√	0000H[Note 1]
FFFFF004H	Port DL register L	PDLL	R/W	√	√		0000H[Note 2]
FFFFF005H	Port DL register H	PDLH	R/W	√	√		0000H[Note 2]
FFFFF006H	Port DH register	PDH[Note 2]	R/W	√	√		0000H[Note 2]
FFFFF008H	Port CS register	PCS	R/W	√	√		0000H[Note 2]
FFFFF00AH	Port CT register	PCT	R/W	√	√		0000H[Note 2]
FFFFF00CH	Port CM register	PCM	R/W	√	√		0000H[Note 2]
FFFFF00EH	Port CD register	PCD[Note 3]	R/W	√	√		0000H[Note 2]
FFFFF024H	Port DL mode register	PMDL	R/W			√	FFFFH
FFFFF024H	Port DL mode register L	PMDLL	R/W	√	√		FFH
FFFFF025H	Port DL mode register H	PMDLH	R/W	√	√		FFH
FFFFF026H	Port DH mode register	PMDH[Note 3]	R/W	√	√		FFH
FFFFF028H	Port CS mode register	PMCS	R/W	√	√		FFH
FFFFF02AH	Port CT mode register	PMCT	R/W	√	√		FFH
FFFFF02CH	Port CM mode register	PMCM	R/W	√	√		FFH
FFFFF02EH	Port CD mode register	PMCD[Note 3]	R/W	√	√		FFH
FFFFF044H	Port DL mode control register	PMCDL	R/W			√	0000H
FFFFF044H	Port DL mode control register L	PMCDLL	R/W	√	√		00H
FFFFF045H	P ort DL mode control register H	PMCDLH	R/W	√	√		00H
FFFFF046H	Port DH mode control register	PMCDH[Note 2]	R/W	√	√		00H
FFFFF048H	Port CS mode control register	PMCCS	R/W	√	√		00H
FFFFF04AH	Port CT mode control register	PMCCT	R/W	√	√		00H
FFFFF04CH	Port CM mode control register	PMCCM	R/W	√	√		00H
FFFFF066H	Bus size configuration register	BSC	R/W			√	5555H
FFFFF06EH	System wait control register	VSWC	R/W	√	√		77H
FFFFF100H	Interrupt mask register 0	IMR0	R/W			√	FFFFH
FFFFF100H	Interrupt mask register 0L	IMR0L	R/W	√	√		FFH
FFFFF101H	Interrupt mask register 0H	IMR0H	R/W	√	√		FFH
FFFFF102H	Interrupt mask register 1	IMR1	R/W			√	FFFFH
FFFFF102H	Interrupt mask register 1L	IMR1L	R/W	√	√		FFH
FFFFF103H	Interrupt mask register 1H	IMR1H	R/W	√	√		FFH
FFFFF104H	Interrupt mask register 2	IMR2[Note 2]	R/W			√	FFFFH
FFFFF104H	Interrupt mask register 2L	IMR2L[Note 2]	R/W	√	√		FFH
FFFFF105H	Interrupt mask register 2H	IMR2H[Note 2]	R/W	√	√		FFH
FFFFF110H	Interrupt control register	WDT1IC	R/W	√	√		47H
FFFFF112H	Interrupt control register	PIC0	R/W	√	√		47H
FFFFF114H	Interrupt control register	PIC1	R/W	√	√		47H
FFFFF116H	Interrupt control register	PIC2	R/W	√	√		47H

Notes 1. The output latch is 00H or 0000H. When input, the pin status is read.

2. Only in the V850ES/KG1 and V850ES/KJ1

3. Only in the V850ES/KJ1

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFF118H	Interrupt control register	PIC3	R/W	√	√		47H
FFFFF11AH	Interrupt control register	PIC4	R/W	√	√		47H
FFFFF11CH	Interrupt control register	PIC5	R/W	√	√		47H
FFFFF11EH	Interrupt control register	PIC6	R/W	√	√		47H
FFFFF120H	Interrupt control register	TM0IC00	R/W	√	√		47H
FFFFF122H	Interrupt control register	TM0IC01	R/W	√	√		47H
FFFFF124H	Interrupt control register	TM0IC10	R/W	√	√		47H
FFFFF126H	Interrupt control register	TM0IC11	R/W	√	√		47H
FFFFF128H	Interrupt control register	TM5IC0	R/W	√	√		47H
FFFFF12AH	Interrupt control register	TM5IC1	R/W	√	√		47H
FFFFF12CH	Interrupt control register	CSI0IC0	R/W	√	√		47H
FFFFF12EH	Interrupt control register	CSI0IC1	R/W	√	√		47H
FFFFF130H	Interrupt control register	SREIC0	R/W	√	√		47H
FFFFF132H	Interrupt control register	SRIC0	R/W	√	√		47H
FFFFF134H	Interrupt control register	STIC0	R/W	√	√		47H
FFFFF136H	Interrupt control register	SREIC1	R/W	√	√		47H
FFFFF138H	Interrupt control register	SRIC1	R/W	√	√		47H
FFFFF13AH	Interrupt control register	STIC1	R/W	√	√		47H
FFFFF13CH	Interrupt control register	TMHIC0	R/W	√	√		47H
FFFFF13EH	Interrupt control register	TMHIC1	R/W	√	√		47H
FFFFF140H	Interrupt control register	CSIAIC0	R/W	√	√		47H
FFFFF142H	Interrupt control register	IICIC0 Note 1	R/W	√	√		47H
FFFFF144H	Interrupt control register	ADIC	R/W	√	√		47H
FFFFF146H	Interrupt control register	KRIC	R/W	√	√		47H
FFFFF148H	Interrupt control register	WTIIC	R/W	√	√		47H
FFFFF14AH	Interrupt control register	WTIC	R/W	√	√		47H
FFFFF14CH	Interrupt control register	BRGIC	R/W	√	√		47H
FFFFF14EH	Interrupt control register	TM0IC20 Note 2	R/W	√	√		47H
FFFFF150H	Interrupt control register	TM0IC21 Note 2	R/W	√	√		47H
FFFFF152H	Interrupt control register	TM0IC30 Note 2	R/W	√	√		47H
FFFFF154H	Interrupt control register	TM0IC31 Note 2	R/W	√	√		47H
FFFFF156H	Interrupt control register	CSIAIC1 Note 2	R/W	√	√		47H
FFFFF158H	Interrupt control register	TM0IC40 Note 3	R/W	√	√		47H
FFFFF15AH	Interrupt control register	TM0IC41 Note 3	R/W	√	√		47H
FFFFF15CH	Interrupt control register	TM0IC50 Note 3	R/W	√	√		47H
FFFFF15EH	Interrupt control register	TM0IC51 Note 3	R/W	√	√		47H
FFFFF160H	Interrupt control register	CSI0IC2 Note 3	R/W	√	√		47H
FFFFF162H	Interrupt control register	SREIC2 Note 3	R/W	√	√		47H
FFFFF164H	Interrupt control register	SRIC2 Note 3	R/W	√	√		47H

Notes 1. Only in products with an I^2C bus

2. Only in the V850ES/KG1 and V850ES/KJ1

3. Only in the V850ES/KJ1

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFF166H	Interrupt control register	STIC2[Note 1]	R/W	√	√		47H
FFFFF168H	Interrupt control register	IICIC1[Note 2]	R/W	√	√		47H
FFFFF1FAH	In-service priority register	ISPR	R	√	√		00H
FFFFF1FCH	Command register	PRCMD	W		√		Undefined
FFFFF1FEH	Power save control register	PSC	R/W	√	√		00H
FFFFF200H	A/D converter mode register	ADM	R/W	√	√		00H
FFFFF201H	Analog input channel specification register	ADS	R/W		√		00H
FFFFF202H	Power fail comparison mode register	PFM	R/W	√	√		00H
FFFFF203H	Power fail comparison threshold register	PFT	R/W		√		00H
FFFFF204H	A/D conversion result register	ADCR	R			√	Undefined
FFFFF205H	A/D conversion result register H	ADCRH	R		√		Undefined
FFFFF280H	D/A conversion value setting register 0	DACS0[Note 3]	R/W		√		00H
FFFFF282H	D/A conversion value setting register 1	DACS1[Note 3]	R/W		√		00H
FFFFF284H	D/A converter mode register	DAM[Note 3]	R/W	√	√		00H
FFFFF300H	Key return mode register	KRM	R/W	√	√		00H
FFFFF400H	Port 0 register	P0	R/W	√	√		00H[Note 4]
FFFFF402H	Port 1 register	P1[Note 3]	R/W	√	√		00H[Note 4]
FFFFF406H	Port 3 register	P3	R/W			√	0000H[Note 4]
FFFFF406H	Port 3 register L	P3L	R/W	√	√		00H[Note 4]
FFFFF407H	Port 3 register H	P3H	R/W	√	√		00H[Note 4]
FFFFF408H	Port 4 register	P4	R/W	√	√		00H[Note 4]
FFFFF40AH	Port 5 register	P5	R/W	√	√		00H[Note 4]
FFFFF40CH	Port 6 register	P6[Note 1]	R/W			√	0000H[Note 4]
FFFFF40CH	Port 6 register L	P6L[Note 1]	R/W	√	√		00H[Note 4]
FFFFF40DH	Port 6 register H	P6H[Note 1]	R/W	√	√		00H[Note 4]
FFFFF40EH	Port 7 register	P7[Note 5]	R		√		Undefined
FFFFF40EH	Port 7 register	P7[Note 1]	R			√	Undefined
FFFFF40EH	Port 7 register L	P7L[Note 1]	R		√		Undefined
FFFFF40FH	Port 7 register H	P7H[Note 1]	R		√		Undefined
FFFFF410H	Port 8 register	P8[Note 1]	R/W	√	√		00H[Note 4]
FFFFF412H	Port 9 register	P9	R/W			√	0000H[Note 4]
FFFFF412H	Port 9 register L	P9L	R/W	√	√		00H[Note 4]
FFFFF413H	Port 9 register H	P9H	R/W	√	√		00H[Note 4]
FFFFF420H	Port 0 mode register	PM0	R/W	√	√		FFH
FFFFF422H	Port 1 mode register	PM1[Note 3]	R/W	√	√		FFH
FFFFF426H	Port 3 mode register	PM3	R/W			√	FFFFH
FFFFF426H	Port 3 mode register L	PM3L	R/W	√	√		FFH
FFFFF427H	Port 3 mode register H	PM3H	R/W	√	√		FFH

Notes 1. Only in the V850ES/KJ1

2. Only in the μPD703216Y, 703217Y, and 70F3217Y

3. Only in the V850ES/KG1 and V850ES/KJ1

4. The output latch is 00H or 0000H. When input, the pin status is read.

5. Only in the V850ES/KF1 and V850ES/KG1

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFF428H	Port 4 mode register	PM4	R/W	√	√		FFH
FFFFF42AH	Port 5 mode register	PM5	R/W	√	√		FFH
FFFF42CH	Port 6 mode register	PM6Note	R/W			√	FFFFH
FFFFF42CH	Port 6 mode register L	PM6LNote	R/W	√	√		FFH
FFFFF42DH	Port 6 mode register H	PM6HNote	R/W	√	√		FFH
FFFFF430H	Port 8 mode register	PM8Note	R/W	√	√		FFH
FFFFF432H	Port 9 mode register	PM9	R/W			√	FFFFH
FFFFF432H	Port 9 mode register L	PM9L	R/W	√	√		FFH
FFFFF433H	Port 9 mode register H	PM9H	R/W	√	√		FFH
FFFFF440H	Port 0 mode control register	PMC0	R/W	√	√		00H
FFFFF446H	Port 3 mode control register	PMC3	R/W			√	0000H
FFFFF446H	Port 3 mode control register L	PMC3L	R/W	√	√		00H
FFFFF447H	Port 3 mode control register H	PMC3H	R/W	√	√		00H
FFFFF448H	Port 4 mode control register	PMC4	R/W	√	√		00H
FFFFF44AH	Port 5 mode control register	PMC5	R/W	√	√		00H
FFFFF44CH	Port 6 mode control register	PMC6Note	R/W			√	0000H
FFFFF44CH	Port 6 mode control register L	PMC6LNote	R/W	√	√		00H
FFFFF44DH	Port 6 mode control register H	PMC6HNote	R/W	√	√		00H
FFFFF450H	Port 8 mode control register	PMC8Note	R/W	√	√		00H
FFFFF452H	Port 9 mode control register	PMC9	R/W			√	0000H
FFFFF452H	Port 9 mode control register L	PMC9L	R/W	√	√		00H
FFFFF453H	Port 9 mode control register H	PMC9H	R/W	√	√		00H
FFFFF466H	Port 3 function control register	PFC3	R/W	√	√		00H
FFFFF46AH	Port 5 function control register	PFC5	R/W	√	√		00H
FFFFF46DH	Port 6 function control register	PFC6HNote	R/W	√	√		00H
FFFFF470H	Port 8 function control register	PFC8Note	R/W	√	√		00H
FFFFF472H	Port 9 function control register	PFC9	R/W			√	0000H
FFFFF472H	Port 9 function control register L	PFC9L	R/W	√	√		00H
FFFFF473H	Port 9 function control register H	PFC9H	R/W	√	√		00H
FFFFF484H	Data wait control register 0	DWC0	R/W			√	7777H
FFFFF488H	Address wait control register	AWC	R/W			√	FFFFH
FFFFF48AH	Bus cycle control register	BCC	R/W			√	AAAAH
FFFFF580H	8-bit timer H mode register 0	TMHMD0	R/W	√	√		00H
FFFFF581H	8-bit timer H carrier control register 0	TMCYC0	R/W	√	√		00H
FFFFF582H	8-bit timer H compare register 00	CMP00	R/W		√		00H
FFFFF583H	8-bit timer H compare register 01	CMP01	R/W		√		00H
FFFFF590H	8-bit timer H mode register 1	TMHMD1	R/W	√	√		00H
FFFFF591H	8-bit timer H carrier control register 1	TMCYC1	R/W	√	√		00H
FFFFF592H	8-bit timer H compare register 10	CMP10	R/W		√		00H
FFFFF593H	8-bit timer H compare register 11	CMP11	R/W		√		00H

Note Only in the V850ES/KJ1

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFF5C0H	16-bit timer counter 5	TM5	R			√	0000H
FFFFF5C0H	8-bit timer counter 50	TM50	R		√		00H
FFFFF5C1H	8-bit timer counter 51	TM51	R		√		00H
FFFFF5C2H	16-bit timer compare register 5	CR5	R/W			√	0000H
FFFFF5C2H	8-bit timer compare register 50	CR50	R/W		√		00H
FFFFF5C3H	8-bit timer compare register 51	CR51	R/W		√		00H
FFFFF5C4H	Timer clock selection register 5	TCL5	R/W			√	0000H
FFFFF5C4H	Timer clock selection register 50	TCL50	R/W	√	√		00H
FFFFF5C5H	Timer clock selection register 51	TCL51	R/W	√	√		00H
FFFFF5C6H	16-bit timer mode control register 5	TMC5	R/W			√	0000H
FFFFF5C6H	8-bit timer mode control register 50	TMC50	R/W	√	√		00H
FFFFF5C7H	8-bit timer mode control register 51	TMC51	R/W	√	√		00H
FFFFF600H	16-bit timer counter 00	TM00	R			√	0000H
FFFFF602H	16-bit timer capture/compare register 000	CR000	R/W			√	0000H
FFFFF604H	16-bit timer capture/compare register 001	CR001	R/W			√	0000H
FFFFF606H	16-bit timer mode control register 00	TMC00	R/W	√	√		00H
FFFFF607H	Prescaler mode register 00	PRM00	R/W	√	√		00H
FFFFF608H	Capture/compare control register 00	CRC00	R/W	√	√		00H
FFFFF609H	16-bit timer output control register 00	TOC00	R/W		√		00H
FFFFF610H	16-bit timer counter 01	TM01	R			√	0000H
FFFFF612H	16-bit timer capture/compare register 010	CR010	R/W			√	0000H
FFFFF614H	16-bit timer capture/compare register 011	CR011	R/W			√	0000H
FFFFF616H	16-bit timer mode control register 01	TMC01	R/W	√	√		00H
FFFFF617H	Prescaler mode register 01	PRM01	R/W	√	√		00H
FFFFF618H	Capture/compare control register 01	CRC01	R/W	√	√		00H
FFFFF619H	16-bit timer output control register 01	TOC01	R/W		√		00H
FFFFF620H	16-bit timer counter 02	TM02[Note]	R			√	0000H
FFFFF622H	16-bit timer capture/compare register 020	CR020[Note]	R/W			√	0000H
FFFFF624H	16-bit timer capture/compare register 021	CR021[Note]	R/W			√	0000H
FFFFF626H	16-bit timer mode control register 02	TMC02[Note]	R/W	√	√		00H
FFFFF627H	Prescaler mode register 02	PRM02[Note]	R/W	√	√		00H
FFFFF628H	Capture/compare control register 02	CRC02[Note]	R/W	√	√		00H
FFFFF629H	16-bit timer output control register 02	TOC02[Note]	R/W		√		00H
FFFFF630H	16-bit timer counter 03	TM03[Note]	R			√	0000H
FFFFF632H	16-bit timer capture/compare register 030	CR030[Note]	R/W			√	0000H
FFFFF634H	16-bit timer capture/compare register 031	CR031[Note]	R/W			√	0000H
FFFFF636H	16-bit timer mode control register 03	TMC03[Note]	R/W	√	√		00H
FFFFF637H	Prescaler mode register 03	PRM03[Note]	R/W	√	√		00H
FFFFF638H	Capture/compare control register 03	CRC03[Note]	R/W	√	√		00H
FFFFF639H	16-bit timer output control register 03	TOC03[Note]	R/W		√		00H

Note Only in the V850ES/KG1 and V850ES/KJ1

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit				After Reset
				1	8	16	32	
FFFFF640H	16-bit timer counter 04	TM04[Note]	R			√		0000H
FFFFF642H	16-bit timer capture/compare register 040	CR040[Note]	R/W			√		0000H
FFFFF644H	16-bit timer capture/compare register 041	CR041[Note]	R/W			√		0000H
FFFFF646H	16-bit timer mode control register 04	TMC04[Note]	R/W	√	√			00H
FFFFF647H	Prescaler mode register 04	PRM04[Note]	R/W	√	√			00H
FFFFF648H	Capture/compare control register 04	CRC04[Note]	R/W	√	√			00H
FFFFF649H	16-bit timer output control register 04	TOC04[Note]	R/W		√			00H
FFFFF650H	16-bit timer counter 05	TM05[Note]	R			√		0000H
FFFFF652H	16-bit timer capture/compare register 050	CR050[Note]	R/W			√		0000H
FFFFF654H	16-bit timer capture/compare register 051	CR051[Note]	R/W			√		0000H
FFFFF656H	16-bit timer mode control register 05	TMC05[Note]	R/W	√	√			00H
FFFFF657H	Prescaler mode register 05	PRM05[Note]	R/W	√	√			00H
FFFFF658H	Capture/compare control register 05	CRC05[Note]	R/W	√	√			00H
FFFFF659H	16-bit timer output control register 05	TOC05[Note]	R/W		√			00H
FFFFF680H	Watch timer operation mode register	WTM	R/W	√	√			00H
FFFFF6C0H	Oscillation stabilization time select register	OSTS	R/W		√			01H
FFFFF6C1H	Watchdog timer clock selection register	WDCS	R/W		√			00H
FFFFF6C2H	Watchdog timer mode register 1	WDTM1	R/W	√	√			00H
FFFFF6D0H	Watchdog timer mode register 2	WDTM2	R/W		√			67H
FFFFF6D1H	Watchdog timer enable register	WDTE	R/W		√			9AH
FFFFF6E0H	Real-time output buffer register L0	RTBL0	R/W	√	√			00H
FFFFF6E2H	Real-time output buffer register H0	RTBH0	R/W	√	√			00H
FFFFF6E4H	Real-time output port mode register 0	RTPM0	R/W	√	√			00H
FFFFF6E5H	Real-time output port control register 0	RTPC0	R/W	√	√			00H
FFFFF6F0H	Real-time output buffer register L1	RTBL1[Note]	R/W	√	√			00H
FFFFF6F2H	Real-time output buffer register H1	RTBH1[Note]	R/W	√	√			00H
FFFFF6F4H	Real-time output port mode register 1	RTPM1[Note]	R/W	√	√			00H
FFFFF6F5H	Real-time output port control register 1	RTPC1[Note]	R/W	√	√			00H
FFFFF802H	System status register	SYS	R/W	√	√			00H
FFFFF806H	PLL control register	PLLCTL	R/W	√	√			01H
FFFFF820H	Power save mode register	PSMR	R/W	√	√			00H
FFFFF828H	Processor clock control register	PCC	R/W	√	√			03H
FFFFF840H	Correction address register 0	CORAD0	R/W				√	00000000H
FFFFF840H	Correction address register 0L	CORAD0L	R/W			√		0000H
FFFFF842H	Correction address register 0H	CORAD0H	R/W			√		0000H
FFFFF844H	Correction address register 1	CORAD1	R/W				√	00000000H
FFFFF844H	Correction address register 1L	CORAD1L	R/W			√		0000H
FFFFF846H	Correction address register 1H	CORAD1H	R/W			√		0000H
FFFFF848H	Correction address register 2	CORAD2	R/W				√	00000000H
FFFFF848H	Correction address register 2L	CORAD2L	R/W			√		0000H
FFFFF84AH	Correction address register 2H	CORAD2H	R/W			√		0000H

Note Only in the V850ES/KJ1

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit				After Reset
				1	8	16	32	
FFFFF84CH	Correction address register 3	CORAD3	R/W				√	00000000H
FFFFF84CH	Correction address register 3L	CORAD3L	R/W			√		0000H
FFFFF84EH	Correction address register 3H	CORAD3H	R/W			√		0000H
FFFFF880H	Correction control register	CORCN	R/W	√	√			00H
FFFFF8B0H	Prescaler mode register	PRSM	R/W		√			00H
FFFFF8B1H	Prescaler compare register	PRSCM	R/W		√			00H
FFFFFA00H	Asynchronous serial interface mode register 0	ASIM0	R/W	√	√			01H
FFFFFA02H	Receive buffer register 0	RXB0	R		√			FFH
FFFFFA03H	Asynchronous serial interface status register 0	ASIS0	R		√			00H
FFFFFA04H	Transmit buffer register 9	TXB0	R/W		√			FFH
FFFFFA05H	Asynchronous serial interface transmission status register 0	ASIF0	R		√			00H
FFFFFA06H	Clock selection register 0	CKSR0	R/W	√	√			00H
FFFFFA07H	Baud rate generator control register 0	BRGC0	R/W	√	√			FFH
FFFFFA10H	Asynchronous serial interface mode register 1	ASIM1	R/W	√	√			01H
FFFFFA12H	Receive buffer register 1	RXB1	R		√			FFH
FFFFFA13H	Asynchronous serial interface status register 1	ASIS1	R		√			00H
FFFFFA14H	Transmit buffer register 1	TXB1	R/W		√			FFH
FFFFFA15H	Asynchronous serial interface transmission status register 1	ASIF1	R		√			00H
FFFFFA16H	Clock selection register 1	CKSR1	R/W	√	√			00H
FFFFFA17H	Baud rate generator control register 1	BRGC1	R/W	√	√			FFH
FFFFFA20H	Asynchronous serial interface mode register 2	ASIM2Note 1	R/W	√	√			01H
FFFFFA22H	Receive buffer register 2	RXB2Note 1	R		√			FFH
FFFFFA23H	Asynchronous serial interface status register 2	ASIS2Note 1	R		√			00H
FFFFFA24H	Transmit buffer register 2	TXB2Note 1	R/W		√			FFH
FFFFFA25H	Asynchronous serial interface transmission status register 2	ASIF2Note 1	R		√			00H
FFFFFA26H	Clock selection register 2	CKSR2Note 1	R/W	√	√			00H
FFFFFA27H	Baud rate generator control register 2	BRGC2Note 1	R/W	√	√			FFH
FFFFFC00H	External interrupt falling edge specification register 0	INTF0	R/W	√	√			00H
FFFFFC13H	External interrupt falling edge specification register 9H	INTF9H	R/W	√	√			00H
FFFFFC20H	External interrupt rising edge specification register 0	INTR0	R/W	√	√			00H
FFFFFC33H	External interrupt rising edge specification register 9H	INTR9H	R/W	√	√			00H
FFFFFC40H	Pull-up resistor option register 0	PU0	R/W	√	√			00H
FFFFFC42H	Pull-up resistor option register 1	PU1Note 2	R/W	√	√			00H
FFFFFC46H	Pull-up resistor option register 3	PU3	R/W	√	√			00H
FFFFFC48H	Pull-up resistor option register 4	PU4	R/W	√	√			00H
FFFFFC4AH	Pull-up resistor option register 5	PU5	R/W	√	√			00H

Notes 1. Only in the V850ES/KJ1

2. Only in the V850ES/KG1 and V850ES/KJ1

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFFC4CH	Pull-up resistor option register 6	PU6[Note]	R/W			√	0000H
FFFFFC4CH	Pull-up resistor option register 6L	PU6L[Note]	R/W	√	√		00H
FFFFFC4DH	Pull-up resistor option register 6H	PU6H[Note]	R/W	√	√		00H
FFFFFC50H	Pull-up resistor option register 8	PU8[Note]	R/W	√	√		00H
FFFFFC52H	Pull-up resistor option register 9	PU9	R/W			√	0000H
FFFFFC52H	Pull-up resistor option register 9L	PU9L	R/W	√	√		00H
FFFFFC53H	Pull-up resistor option register 9H	PU9H	R/W	√	√		00H
FFFFFC67H	Port 3 function register H	PF3H	R/W	√	√		00H
FFFFFC68H	Port 4 function register	PF4	R/W	√	√		00H
FFFFFC6AH	Port 5 function register	PF5	R/W	√	√		00H
FFFFFC6CH	Port 6 function register	PF6[Note]	R/W			√	0000H
FFFFFC6CH	Port 6 function register L	PF6L[Note]	R/W	√	√		00H
FFFFFC6DH	Port 6 function register H	PF6H[Note]	R/W	√	√		00H
FFFFFC70H	Port 8 function register	PF8[Note]	R/W	√	√		00H
FFFFFC73H	Port 9 function register H	PF9H	R/W	√	√		00H
FFFFFD00H	Clocked serial interface mode register 00	CSIM00	R/W	√	√		00H
FFFFFD01H	Clocked serial interface clock selection register 0	CSIC0	R/W	√	√		00H
FFFFFD02H	Clocked serial interface receive buffer register 0	SIRB0	R			√	0000H
FFFFFD02H	Clocked serial interface receive buffer register 0L	SIRB0L	R		√		00H
FFFFFD04H	Clocked serial interface transmit buffer register 0	SOTB0	R/W			√	0000H
FFFFFD04H	Clocked serial interface transmit buffer register 0L	SOTB0L	R/W		√		00H
FFFFFD06H	Clocked serial interface read-only receive buffer register 0	SIRBE0	R			√	0000H
FFFFFD06H	Clocked serial interface read-only receive buffer register 0L	SIRBE0L	R		√		00H
FFFFFD08H	Clocked serial interface first-stage transmit buffer register 0	SOTBF0	R/W			√	0000H
FFFFFD08H	Clocked serial interface first-stage transmit buffer register 0L	SOTBF0L	R/W		√		00H
FFFFFD0AH	Serial I/O shift register 0	SIO00	R/W			√	00H
FFFFFD0AH	Serial I/O shift register 0L	SIO00L	R/W		√		0000H
FFFFFD10H	Clocked serial interface mode register 01	CSIM01	R/W	√	√		00H
FFFFFD11H	Clocked serial interface clock selection register 1	CSIC1	R/W	√	√		00H
FFFFFD12H	Clocked serial interface receive buffer register 1	SIRB1	R			√	0000H
FFFFFD12H	Clocked serial interface receive buffer register 1L	SIRB1L	R		√		00H
FFFFFD14H	Clocked serial interface transmit buffer register 1	SOTB1	R/W			√	0000H
FFFFFD14H	Clocked serial interface transmit buffer register 1L	SOTB1L	R/W		√		00H
FFFFFD16H	Clocked serial interface read-only receive buffer register 1	SIRBE1	R			√	0000H
FFFFFD16H	Clocked serial interface read-only receive buffer register 1L	SIRBE1L	R		√		00H
FFFFFD18H	Clocked serial interface first-stage transmit buffer register 1	SOTBF1	R/W			√	0000H
FFFFFD18H	Clocked serial interface first-stage transmit buffer register 1L	SOTBF1L	R/W		√		00H
FFFFFD1AH	Serial I/O shift register 1	SIO01	R/W			√	00H
FFFFFD1AH	Serial I/O shift register 1L	SIO1L	R/W		√		0000H
FFFFFD20H	Clocked serial interface mode register 02	CSIM02[Note]	R/W	√	√		00H
FFFFFD21H	Clocked serial interface clock selection register 2	CSIC2[Note]	R/W	√	√		00H

Note Only in the V850ES/KJ1

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFFD22H	Clocked serial interface receive buffer register 2	SIRB2[Note 1]	R			√	0000H
FFFFFD22H	Clocked serial interface receive buffer register 2L	SIRB2L[Note 1]	R		√		00H
FFFFFD24H	Clocked serial interface transmit buffer register 2	SOTB2[Note 1]	R/W			√	0000H
FFFFFD24H	Clocked serial interface transmit buffer register 2L	SOTB2L[Note 1]	R/W		√		00H
FFFFFD26H	Clocked serial interface read-only receive buffer register 2	SIRBE2[Note 1]	R			√	0000H
FFFFFD26H	Clocked serial interface read-only receive buffer register 2L	SIRBE2L[Note 1]	R		√		00H
FFFFFD28H	Clocked serial interface first-stage transmit buffer register 2	SOTBF2[Note 1]	R/W			√	0000H
FFFFFD28H	Clocked serial interface first-stage transmit buffer register 2L	SOTBF2L[Note 1]	R/W		√		00H
FFFFFD2AH	Serial I/O shift register 2	SIO02[Note 1]	R/W			√	00H
FFFFFD2AH	Serial I/O shift register 2L	SIO02L[Note 1]	R/W		√		0000H
FFFFFD40H	Serial operation mode specification register 0	CSIMA0	R/W	√	√		00H
FFFFFD41H	Serial status register 0	CSIS0	R/W	√	√		00H
FFFFFD42H	Serial trigger register 0	CSIT0	R/W	√	√		00H
FFFFFD43H	Division value selection register 0	BRGCA0	R/W		√		03H
FFFFFD44H	Automatic data transfer address point specification register 0	ADTP0	R/W		√		00H
FFFFFD45H	Automatic data transfer interval specification register 0	ADTI0	R/W		√		00H
FFFFFD46H	Serial I/O shift register A0	SIOA0	R/W	√	√		00H
FFFFFD47H	Automatic data transfer address count register 0	ADTC0	R	√	√		00H
FFFFFD50H	Serial operation mode specification register 1	CSIMA1[Note 2]	R/W	√	√		00H
FFFFFD51H	Serial status register 1	CSIS1[Note 2]	R/W	√	√		00H
FFFFFD52H	Serial trigger register 1	CSIT1[Note 2]	R	√	√		00H
FFFFFD53H	Division value selection register 1	BRGCA1[Note 2]	R/W		√		03H
FFFFFD54H	Automatic data transfer address point specification register 1	ADTP1[Note 2]	R/W		√		00H
FFFFFD55H	Automatic data transfer interval specification register 1	ADTI1[Note 2]	R/W		√		00H
FFFFFD56H	Serial I/O shift register A1	SIOA1[Note 2]	R/W	√	√		00H
FFFFFD57H	Automatic data transfer address count register 1	ADTC1[Note 2]	R	√	√		00H
FFFFFD80H	IIC shift register 0	IIC0[Note 3]	R/W		√		00H
FFFFFD82H	IIC control register 0	IICC0[Note 3]	R/W	√	√		00H
FFFFFD83H	Slave address register 0	SVA0[Note 3]	R/W		√		00H
FFFFFD84H	IIC clock selection register 0	IICCL0[Note 3]	R/W	√	√		00H
FFFFFD85H	IIC function expansion register 0	IICX0[Note 3]	R/W	√	√		00H
FFFFFD86H	IIC status register 0	IICS0[Note 3]	R	√	√		00H
FFFFFD8AH	IIC flag register 0	IICF0[Note 3]	R/W	√	√		00H
FFFFFD90H	IIC shift register 1	IIC1[Note 4]	R/W		√		00H
FFFFFD92H	IIC control register 1	IICC01[Note 4]	R/W	√	√		00H
FFFFFD93H	Slave address register 1	SVA01[Note 4]	R/W		√		00H
FFFFFD94H	IIC clock selection register 1	IICCL01[Note 4]	R/W	√	√		00H
FFFFFD95H	IIC function expansion register 1	IICX1[Note 4]	R/W	√	√		00H

Notes 1. Only in the V850ES/KJ1

2. Only in the V850ES/KG1 and V850ES/KJ1

3. Only in products with an I^2C bus

4. Only in the μPD703216Y, 703217Y, and 70F3217Y

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFFD96H	IIC status register 1	IICS01[Note]	R	√	√		00H
FFFFFD9AH	IIC flag register 1	IICF1[Note]	R/W	√	√		00H
FFFFFE00H	CSIA0 buffer RAM 0	CSIA0B0	R/W			√	Undefined
FFFFFE00H	CSIA0 buffer RAM 0L	CSIA0B0L	R/W		√		Undefined
FFFFFE01H	CSIA0 buffer RAM 0H	CSIA0B0H	R/W		√		Undefined
FFFFFE02H	CSIA0 buffer RAM 1	CSIA0B1	R/W			√	Undefined
FFFFFE02H	CSIA0 buffer RAM 1L	CSIA0B1L	R/W		√		Undefined
FFFFFE03H	CSIA0 buffer RAM 1H	CSIA0B1H	R/W		√		Undefined
FFFFFE04H	CSIA0 buffer RAM 2	CSIA0B2	R/W			√	Undefined
FFFFFE04H	CSIA0 buffer RAM 2L	CSIA0B2L	R/W		√		Undefined
FFFFFE05H	CSIA0 buffer RAM2H	CSIA0B2H	R/W		√		Undefined
FFFFFE06H	CSIA0 buffer RAM 3	CSIA0B3	R/W			√	Undefined
FFFFFE06H	CSIA0 buffer RAM 3L	CSIA0B3L	R/W		√		Undefined
FFFFFE07H	CSIA0 buffer RAM 3H	CSIA0B3H	R/W		√		Undefined
FFFFFE08H	CSIA0 buffer RAM 4	CSIA0B4	R/W			√	Undefined
FFFFFE08H	CSIA0 buffer RAM 4L	CSIA0B4L	R/W		√		Undefined
FFFFFE09H	CSIA0 buffer RAM 4H	CSIA0B4H	R/W		√		Undefined
FFFFFE0AH	CSIA0 buffer RAM 5	CSIA0B5	R/W			√	Undefined
FFFFFE0AH	CSIA0 buffer RAM 5L	CSIA0B5L	R/W		√		Undefined
FFFFFE0BH	CSIA0 buffer RAM 5H	CSIA0B5H	R/W		√		Undefined
FFFFFE0CH	CSIA0 buffer RAM 6	CSIA0B6	R/W			√	Undefined
FFFFFE0CH	CSIA0 buffer RAM 6L	CSIA0B6L	R/W		√		Undefined
FFFFFE0DH	CSIA0 buffer RAM 6H	CSIA0B6H	R/W		√		Undefined
FFFFFE0EH	CSIA0 buffer RAM 7	CSIA0B7	R/W			√	Undefined
FFFFFE0EH	CSIA0 buffer RAM 7L	CSIA0B7L	R/W		√		Undefined
FFFFFE0FH	CSIA0 buffer RAM 7H	CSIA0B7H	R/W		√		Undefined
FFFFFE10H	CSIA0 buffer RAM 8	CSIA0B8	R/W			√	Undefined
FFFFFE10H	CSIA0 buffer RAM 8L	CSIA0B8L	R/W		√		Undefined
FFFFFE11H	CSIA0 buffer RAM 8H	CSIA0B8H	R/W		√		Undefined
FFFFFE12H	CSIA0 buffer RAM 9	CSIA0B9	R/W			√	Undefined
FFFFFE12H	CSIA0 buffer RAM 9L	CSIA0B9L	R/W		√		Undefined
FFFFFE13H	CSIA0 buffer RAM 9H	CSIA0B9H	R/W		√		Undefined
FFFFFE14H	CSIA0 buffer RAM A	CSIA0BA	R/W			√	Undefined
FFFFFE14H	CSIA0 buffer RAM AL	CSIA0BAL	R/W		√		Undefined
FFFFFE15H	CSIA0 buffer RAM AH	CSIA0BAH	R/W		√		Undefined
FFFFFE16H	CSIA0 buffer RAM B	CSIA0BB	R/W			√	Undefined
FFFFFE16H	CSIA0 buffer RAM BL	CSIA0BBL	R/W		√		Undefined
FFFFFE17H	CSIA0 buffer RAM BH	CSIA0BBH	R/W		√		Undefined
FFFFFE18H	CSIA0 buffer RAM C	CSIA0BC	R/W			√	Undefined
FFFFFE18H	CSIA0 buffer RAM CL	CSIA0BCL	R/W		√		Undefined
FFFFFE19H	CSIA0 buffer RAM CH	CSIA0BCH	R/W		√		Undefined

Note Only in the μPD703216Y, 703217Y, and 70F3217Y

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Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFFE1AH	CSIA0 buffer RAM D	CSIA0BD	R/W			√	Undefined
FFFFFE1AH	CSIA0 buffer RAM DL	CSIA0BDL	R/W		√		Undefined
FFFFFE1BH	CSIA0 buffer RAM DH	CSIA0BDH	R/W		√		Undefined
FFFFFE1CH	CSIA0 buffer RAM E	CSIA0BE	R/W			√	Undefined
FFFFFE1CH	CSIA0 buffer RAM EL	CSIA0BEL	R/W		√		Undefined
FFFFFE1DH	CSIA0 buffer RAM EH	CSIA0BEH	R/W		√		Undefined
FFFFFE1EH	CSIA0 buffer RAM F	CSIA0BF	R/W			√	Undefined
FFFFFE1EH	CSIA0 buffer RAM FL	CSIA0BFL	R/W		√		Undefined
FFFFFE1FH	CSIA0 buffer RAM FH	CSIA0BFH	R/W		√		Undefined
FFFFFE20H	CSIA1 buffer RAM 0	CSIA1B0Note	R/W			√	Undefined
FFFFFE20H	CSIA1 buffer RAM 0L	CSIA1B0LNote	R/W		√		Undefined
FFFFFE21H	CSIA1 buffer RAM 0H	CSIA1B0HNote	R/W		√		Undefined
FFFFFE22H	CSIA1 buffer RAM 1	CSIA1B1Note	R/W			√	Undefined
FFFFFE22H	CSIA1 buffer RAM 1L	CSIA1B1LNote	R/W		√		Undefined
FFFFFE23H	CSIA1 buffer RAM 1H	CSIA1B1HNote	R/W		√		Undefined
FFFFFE24H	CSIA1 buffer RAM 2	CSIA1B2Note	R/W			√	Undefined
FFFFFE24H	CSIA1 buffer RAM 2L	CSIA1B2LNote	R/W		√		Undefined
FFFFFE25H	CSIA1 buffer RAM 2H	CSIA1B2HNote	R/W		√		Undefined
FFFFFE26H	CSIA1 buffer RAM 3	CSIA1B3Note	R/W			√	Undefined
FFFFFE26H	CSIA1 buffer RAM 3L	CSIA1B3LNote	R/W		√		Undefined
FFFFFE27H	CSIA1 buffer RAM 3H	CSIA1B3HNote	R/W		√		Undefined
FFFFFE28H	CSIA1 buffer RAM 4	CSIA1B4Note	R/W			√	Undefined
FFFFFE28H	CSIA1 buffer RAM 4L	CSIA1B4LNote	R/W		√		Undefined
FFFFFE29H	CSIA1 buffer RAM 4H	CSIA1B4HNote	R/W		√		Undefined
FFFFFE2AH	CSIA1 buffer RAM 5	CSIA1B5Note	R/W			√	Undefined
FFFFFE2AH	CSIA1 buffer RAM 5L	CSIA1B5LNote	R/W		√		Undefined
FFFFFE2BH	CSIA1 buffer RAM 5H	CSIA1B5HNote	R/W		√		Undefined
FFFFFE2CH	CSIA1 buffer RAM 6	CSIA1B6Note	R/W			√	Undefined
FFFFFE2CH	CSIA1 buffer RAM 6L	CSIA1B6LNote	R/W		√		Undefined
FFFFFE2DH	CSIA1 buffer RAM 6H	CSIA1B6HNote	R/W		√		Undefined
FFFFFE2EH	CSIA1 buffer RAM 7	CSIA1B7Note	R/W			√	Undefined
FFFFFE2EH	CSIA1 buffer RAM 7L	CSIA1B7LNote	R/W		√		Undefined
FFFFFE2FH	CSIA1 buffer RAM 7H	CSIA1B7HNote	R/W		√		Undefined
FFFFFE30H	CSIA1 buffer RAM 8	CSIA1B8Note	R/W			√	Undefined
FFFFFE30H	CSIA1 buffer RAM 8L	CSIA1B8LNote	R/W		√		Undefined
FFFFFE31H	CSIA1 buffer RAM 8H	CSIA1B8HNote	R/W		√		Undefined
FFFFFE32H	CSIA1 buffer RAM 9	CSIA1B9Note	R/W			√	Undefined
FFFFFE32H	CSIA1 buffer RAM 9L	CSIA1B9LNote	R/W		√		Undefined
FFFFFE33H	CSIA1 buffer RAM 9H	CSIA1B9HNote	R/W		√		Undefined
FFFFFE34H	CSIA1 buffer RAM A	CSIA1BANote	R/W			√	Undefined
FFFFFE34H	CSIA1 buffer RAM AL	CSIA1BALNote	R/W		√		Undefined
FFFFFE35H	CSIA1 buffer RAM AH	CSIA1BAHNote	R/W		√		Undefined

Note Only in the V850ES/KG1 and V850ES/KJ1

(12/12)

Address	Function Register Name	Symbol	R/W	Operable Bit Unit			After Reset
				1	8	16	
FFFFFE36H	CSIA1 buffer RAM B	CSIA1BB[Note]	R/W			√	Undefined
FFFFFE36H	CSIA1 buffer RAM BL	CSIA1BBL[Note]	R/W		√		Undefined
FFFFFE37H	CSIA1 buffer RAM BH	CSIA1BBH[Note]	R/W		√		Undefined
FFFFFE38H	CSIA1 buffer RAM C	CSIA1BC[Note]	R/W			√	Undefined
FFFFFE38H	CSIA1 buffer RAM CL	CSIA1BCL[Note]	R/W		√		Undefined
FFFFFE39H	CSIA1 buffer RAM CH	CSIA1BCH[Note]	R/W		√		Undefined
FFFFFE3AH	CSIA1 buffer RAM D	CSIA1BD[Note]	R/W			√	Undefined
FFFFFE3AH	CSIA1 buffer RAM DL	CSIA1BDL[Note]	R/W		√		Undefined
FFFFFE3BH	CSIA1 buffer RAM DH	CSIA1BDH[Note]	R/W		√		Undefined
FFFFFE3CH	CSIA1 buffer RAM E	CSIA1BE[Note]	R/W			√	Undefined
FFFFFE3CH	CSIA1 buffer RAM EL	CSIA1BEL[Note]	R/W		√		Undefined
FFFFFE3DH	CSIA1 buffer RAM EH	CSIA1BEH[Note]	R/W		√		Undefined
FFFFFE3EH	CSIA1 buffer RAM F	CSIA1BF[Note]	R/W			√	Undefined
FFFFFE3EH	CSIA1 buffer RAM FL	CSIA1BFL[Note]	R/W		√		Undefined
FFFFFE3FH	CSIA1 buffer RAM FH	CSIA1BFH[Note]	R/W		√		Undefined
FFFFFFBEH	External bus interface mode control register	EXIMC[Note]	R/W	√	√		00H

Note Only in the V850ES/KG1 and V850ES/KJ1

3.4.7 Special registers

Special registers are registers that prevent invalid data from being written when an inadvertent program loop occurs.

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 have the following three special registers.

- Power save control register (PSC)
- Processor clock control register (PCC)
- Watchdog timer mode register (WDTM1)

Moreover, there is also a command register (PRCMD), which is a protection register for write operations to the special registers that prevents the application system from unexpectedly stopping due to an inadvertent program loop. Write access to the special registers is performed with a special sequence and illegal store operations are notified to the system status register (SYS).

(1) Setting data to special registers

Setting data to a special registers is done in the following sequence.

<1> Prepare the data to be set to the special register in a general-purpose register.

<2> Write the data prepared in step <1> to the PRCMD register.

<3> Write the setting data to the special register (using following instructions).

- Store instruction (ST/SST instruction)
- Bit manipulation instruction (SET1/CLR1/NOT1 instruction)

<4> to <8> Insert NOP instructions (5 instructions)[Note].

[Description Example] When using PSC register (standby mode setting)

```
   ST.B r11,PSMR[r0]    ; PSMR register setting (IDLE, STOP mode setting)
<1>MOV 0x02,r10
<2>ST.B r10,PRCMD[r0]   ; PRCMD register write
<3>ST.B r10,PSC[r0]     ; PSC register setting
<4>NOP[Note]            ; Dummy instruction
<5>NOP[Note]            ; Dummy instruction
<6>NOP[Note]            ; Dummy instruction
<7>NOP[Note]            ; Dummy instruction
<8>NOP[Note]            ; Dummy instruction
(next instruction)
```

No special sequence is required to read special registers.

Note When switching to the IDLE mode or the STOP mode (STP bit of PSC register = 1), 5 NOP instructions must be inserted immediately after switching is performed.

Cautions 1. Interrupts are not acknowledged for the store instruction for the PRCMD register. This is because continuous execution of store instructions by the program in steps <2> and <3> above is assumed. If another instruction is placed between step <2> and <3>, the above sequence may not be realized when an interrupt is acknowledged for that instruction, which may cause malfunction.

2. The data written to the PRCMD register is dummy data, but use the same register as the general-purpose register used for setting data to the special register (step <3>) when writing to the PRCMD register (step <2>). The same applies to when using a general-purpose register for addressing.

(2) Command register (PRCMD)

The PRCMD register is an 8-bit register used to prevent data from being written to registers that may have a large influence on the system, possibly causing the application system to unexpectedly stop, when an inadvertent program loop occurs. Only the first write operation to the special register following the execution of a previously executed write operation to the PRCMD register, is valid.

As a result, register values can be overwritten only using a preset sequence, preventing invalid write operations.

This register can only be written in 8-bit units (if it is read, an undefined value is returned).

After reset: Undefined W Address: FFFFF1FCH

	7	6	5	4	3	2	1	0
PRCMD	REG7	REG6	REG5	REG4	REG3	REG2	REG1	REG0

(3) System status register (SYS)

This register is allocated with status flags showing the operating state of the entire system.

This register can be read or written in 8-bit or 1-bit units.

After reset: 00H R/W Address: FFFFF802H

	7	6	5	4	3	2	1	<0>
SYS	0	0	0	0	0	0	0	PRERR

PRERR	Detection of protection error
0	Protection error has not occurred
1	Protection error has occurred

The operation conditions of the PRERR flag are described below.

(a) Set conditions (PRERR = 1)

(i) When a write operation to the special register takes place without write operation being performed to the PRCMD register (when step <3> is performed without performing step <2> as described in **3.4.7 (1) Setting data to special registers**).

(ii) When a write operation (including bit manipulation instruction) to an on-chip peripheral I/O register other than a special register is performed following write to the PRCMD register (when <3> in **3.4.7 (1) Setting data to special registers** is not a special register).

Remark Regarding the special registers other than the WDTM register (PCC and PSC registers), even if on-chip peripheral I/O register read (except bit manipulation instruction) (internal RAM access, etc.) is performed in between write to the PRCMD register and write to a special register, the PRERR flag is not set and setting data can be written to the special register.

(b) Clear conditions (PRERR = 0)

(i) When 0 is written to the PRERR flag of the SYS register

(ii) When system reset is performed

Cautions 1. If 0 is written to the PRERR bit of the SYS register that is not a special register immediately following write to the PRCMD register, the PRERR bit becomes 0 (write priority).

2. If data is written to the PRCMD register that is not a special register immediately following write to the PRCMD register, the PRERR bit becomes 1.

3.4.8 Cautions

Be sure to set the following register before using the V850ES/KF1, V850ES/KG1 and V850ES/KJ1.

- System wait control register (VSWC)

After setting the VSWC register, set the other registers as required.

When using an external bus, set the VSWC register and then set the various pins to the control mode by setting the port-related registers.

(1) System wait control register (VSWC)

The system wait control register (VSWC) controls the bus access wait time for the on-chip peripheral I/O registers.

Access to the on-chip peripheral I/O register lasts 3 clocks (during no wait), but in the V850ES/KF1, V850ES/KG1 and V850ES/KJ1, waits are required according to the operation frequency. Set the values shown below to the VSWC register according to the operation frequency that is used.

This register can be read or written in 8-bit units (Address: FFFFF06EH, After reset: 77H).

Operation Conditions	Operation Frequency (f_{CLK})	VSWC Setting
REGC = V_{DD} = 5 V±10%, In PLL mode (OSC = 2 to 5 MHz)	8 MHz ≤ f_{CLK} < 16.6 MHz	00H
	16.6 MHz ≤ f_{CLK} ≤ 20 MHz	01H
REGC = Capacity, V_{DD} = 4.0 to 5.5 V REGC = V_{DD} = 2.7 to 4.0 V	2 MHz ≤ f_{CLK} < 8.3 MHz	00H
	8.3 MHz ≤ f_{CLK} ≤ 16 MHz	01H
Other than above (REGC = V_{DD} = 4.0 to 5.5 V)	f_{CLK} ≤ 16 MHz	00H

(2) Access to special on-chip peripheral I/O register

This product has two types of internal system buses.

One type is for the CPU bus and the other is for the peripheral bus to interface with low-speed peripheral hardware.

Since the CPU bus clock and peripheral bus clock are asynchronous, if a conflict occurs during access between the CPU and peripheral hardware, illegal data may be passed unexpectedly. Therefore, when accessing peripheral hardware that may cause a conflict, the number of access cycles is changed so that the data is received/passed correctly in the CPU. As a result, the CPU does not shift to the next instruction processing and enters the wait status. When this wait status occurs, the number of execution clocks of the instruction is increased by the number of wait clocks.

Note this with caution when performing real-time processing.

When accessing a special on-chip peripheral I/O register, additional waits may be required further to the waits set by the VSWC register.

The access conditions at that time and the method to calculate the number of waits to be inserted (number of CPU clocks) are shown below.

Peripheral Function	Register Name	Access	k
Watchdog timer 1 (WDT1)	WDTM1	Write	2 to 4
	<Calculation of number of waits> {(1/fx) × 2/((2 + m)/f_{CPU})} + 1 fx: Oscillation frequency		
Watchdog timer 2 (WDT2)	WDTM2	Write	3 (fixed)
16-bit timer/event counters 00 to 05 (TM00 to TM05)Note 1	TMC00 to TMC05	Read-modify-write	1 (fixed) A wait occurs during write
Clocked serial interfaces 0 and 1 with automatic transmit/receive function (CSIA0, CSIA1)Note 3	CSIA0B0 to CSIA0BF, CSIA1B0 to CSIA1BF	WriteNote 2 (when performing continuous write)	0 to 18
	<Calculation of number of waits> {(1/f_{SCKA}) × 5 – (4 + m)/f_{CPU})}/{((2 + m)/f_{CPU})} However, 1 wait if f_{CPU} = fxx if the CKSAn1 and CKSAn0 bits of the CSISn register are 0. f_{SCKA}: CSIA selection clock frequency		
I^2C0Note 4, I^2C1Note 5	IICS0, IICS1	Read	1 (fixed)
Asynchronous serial interfaces 0 to 2 (UART0 to UART2)Note 6	ASIS0 to ASIS2	Read	1 (fixed)
Real-time output functions 0 and 1 (RTO0, RTO1)Note 7	RTBL0, RTBL1, RTBH0, RTBH1	Write (when bits RTPOE0 and RTPOE1 of RTPC0 and RTPC1 registers = 0)	1
A/D converter	ADM, ADS, PFM, PFT	Write	1 to 5
	ADCR, ADCRH	Read	1 to 5
	<Calculation of maximum number of waits> {(1/f_{AD}) × 2/[(2 + m)/f_{CPU}]} + 1 f_{AD}: A/D selection clock frequency		

Number of waits to be added = (2 + m) × k [clocks]

Notes 1. TM02 and TM03 are available only in the V850ES/KG1 and V850ES/KJ1; TM04 and TM05 are available only in the V850ES/KJ1.

2. If fetched from the on-chip RAM, the number of waits is as shown above.
If fetched from the external memory, the number of waits may be fewer than the number shown above.
The effect of the external memory access cycle differs depending on the wait settings, etc. However, the number of waits above is the maximum value.

3. CSIA1 is available only in the V850ES/KG1 and V850ES/KJ1.

4. I^2C0 is available only in the products with I^2C.

5. I^2C1 is available only in the V850ES/KJ1 (μPD703216Y, 703217Y, and 70F3217Y).

6. UART2 is available only in the V850ES/KJ1.

7. RTO1 is available only in the V850ES/KJ1.

Caution When the CPU operates on the subclock and no clock is input to the X1 pin, do not access a register in which a wait occurs using an access method that causes a wait. If a wait occurs, it can only be released by a reset.

Remark In the calculation for the number of waits:

f_{CPU}: CPU clock frequency

m: Set value of bits 2 to 0 of the VSWC register

f_{CLK}: Internal system clock

When $f_{CLK} < 16.6$ MHz: m = 0

When $f_{CLK} \geq 16.6$ MHz: m = 1

The digits below the decimal point are truncated if less than $(1/f_{CPU})/(2 + m)$ or rounded up if larger than $(1/f_{CPU})/(2 + m)$ when multiplied by $(1/f_{CPU})$.

CHAPTER 4 PORT FUNCTIONS

4.1 Features

4.1.1 V850ES/KF1

- Input-only ports: 8 pins
- I/O ports: 59 pins
  - Fixed to N-ch open-drain output: 2
  - Switchable to N-ch open-drain output: 6
- Input/output can be specified in 1-bit units

4.1.2 V850ES/KG1

- Input-only ports: 8 pins
- I/O ports: 76 pins
  - Fixed to N-ch open-drain output: 4 (medium voltage: 2)
  - Switchable to N-ch open-drain output: 8
- Input/output can be specified in 1-bit units

4.1.3 V850ES/KJ1

- Input-only ports: 16 pins
- I/O ports: 112 pins
  - Fixed to N-ch open-drain output: 6 (medium: 4)
  - Switchable to N-ch open-drain output: 12
- Input/output can be specified in 1-bit units

4.2 Basic Port Configuration

4.2.1 V850ES/KF1

The V850ES/KF1 incorporates a total of 67 I/O port pins consisting of ports 0, 3 to 5, 7, 9, CM, CS, CT, and DL (including 8 input-only port pins). The port configuration is shown below.

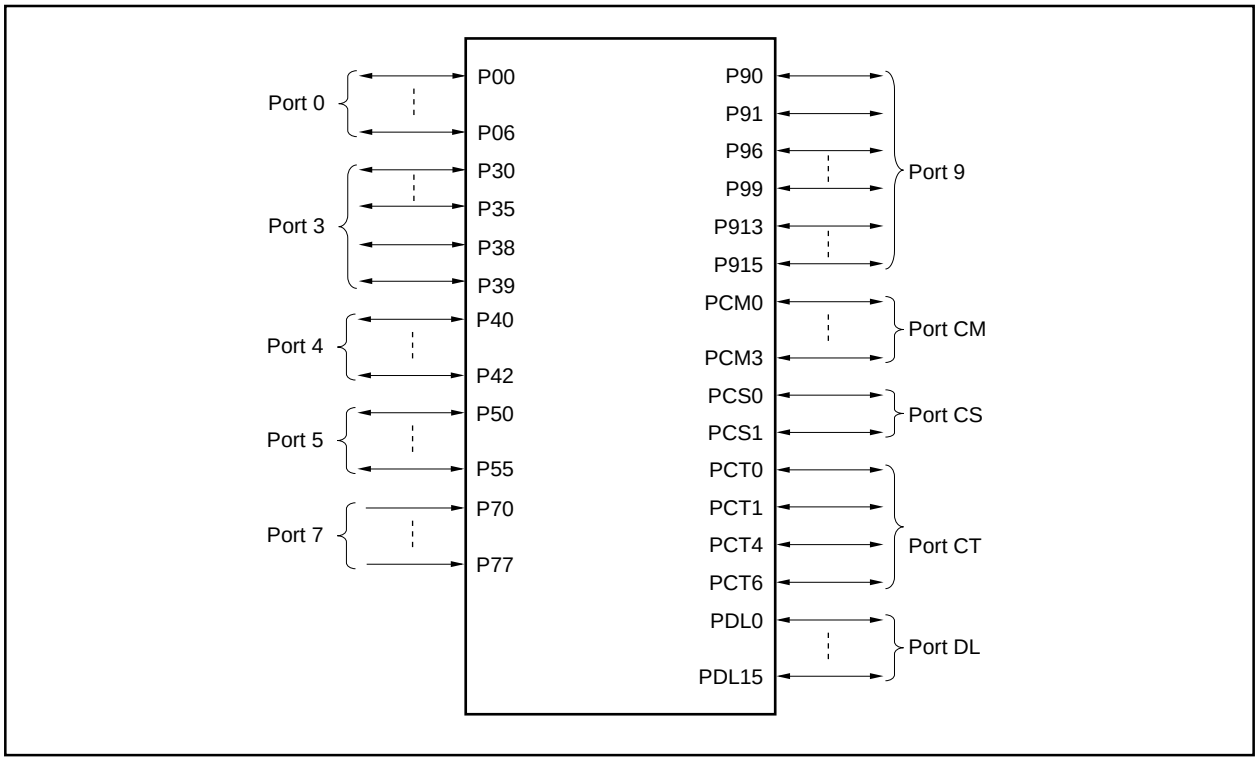


Table 4-1. V850ES/KF1 Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF0}	Port 7
EV_{DD}	$\overline{RESET}$, port 0, port 3 to port 5, port 9, port CM, port CS, port CT, port DL

4.2.2 V850ES/KG1

The V850ES/KG1 incorporates a total of 84 I/O port pins consisting of ports 0, 1, 3 to 5, 7, 9, CM, CS, CT, DH, and DL (including 8 input-only port pins). The port configuration is shown below.

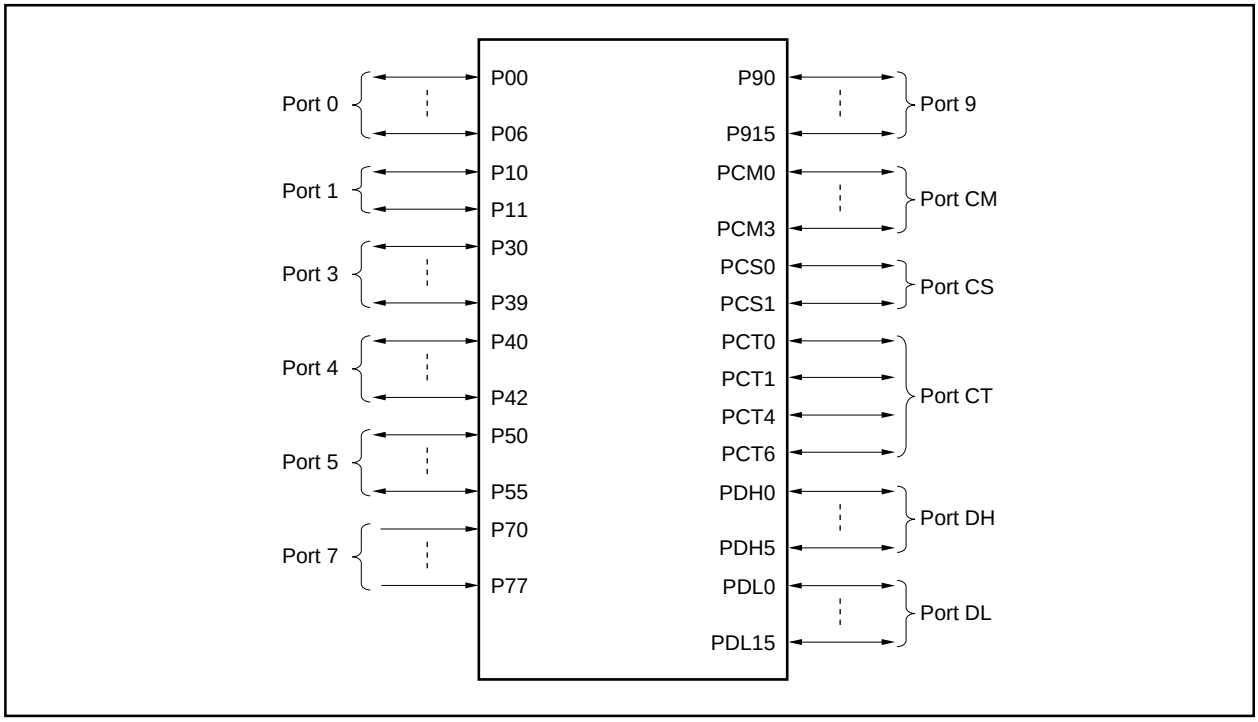


Table 4-2. V850ES/KG1 Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF0}	Port 7
AV_{REF1}	Port 1
BV_{DD}	Port CM, port CS, port CT, port DH, port DL
EV_{DD}	$\overline{RESET}$, port 0, port 3 to port 5, port 9

4.2.3 V850ES/KJ1

The V850ES/KJ1 incorporates a total of 128 I/O port pins consisting of ports 0, 1, 3 to 9, CD, CM, CS, CT, DH, and DL (including 16 input-only port pins). The port configuration is shown below.

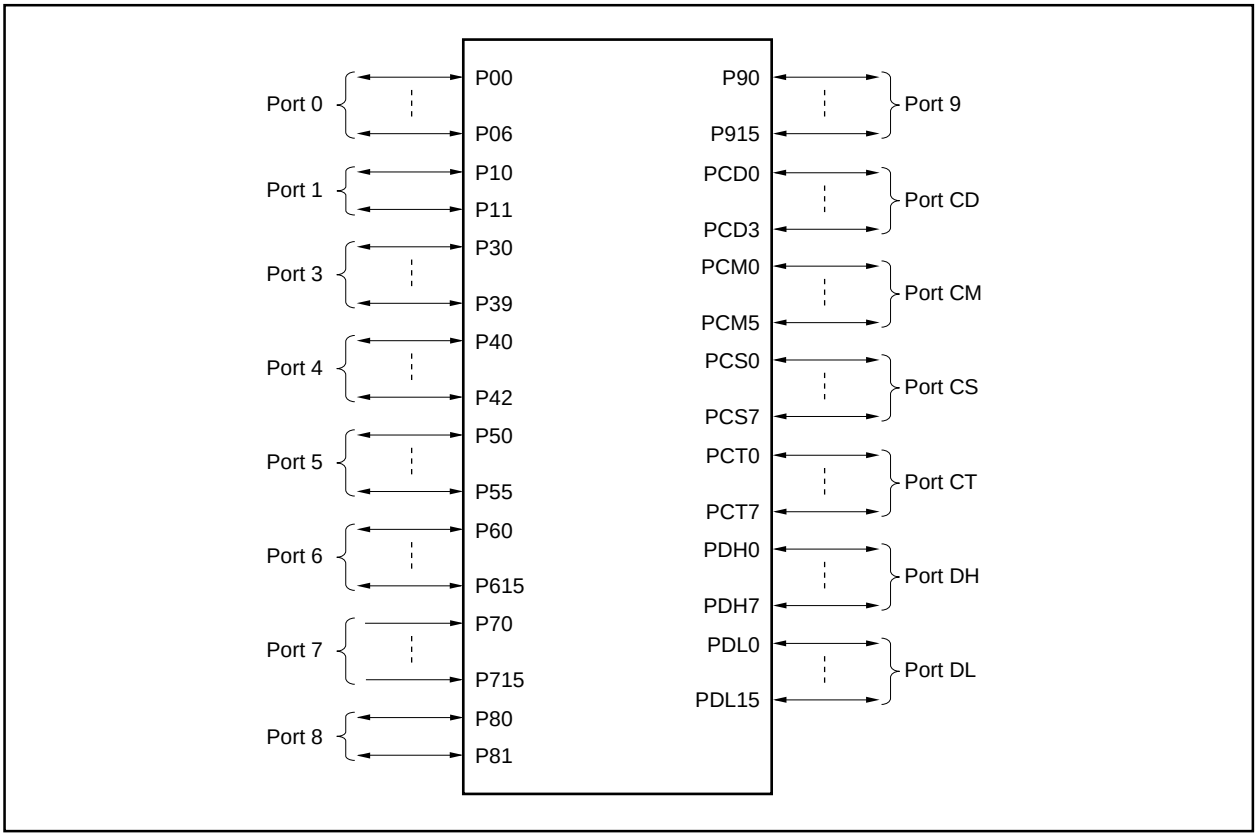


Table 4-3. V850ES/KJ1 Pin I/O Buffer Power Supplies

Power Supply	Corresponding Pins
AV_{REF0}	Port 7
AV_{REF1}	Port 1
BV_{DD}	Port CD, port CM, port CS, port CT, port DH, port DL
EV_{DD}	$\overline{RESET}$, port 0, port 3 to port 6, port 8, port 9

4.3 Port Configuration

Table 4-4. Port Configuration (V850ES/KF1)

Item	Configuration
Control registers	Port n register (Pn: n = 0, 3 to 5, 9, CM, CS, CT, DL) Port n mode register (PMn: n = 0, 3 to 5, 9, CM, CS, CT, DL) Port n mode control register (PMCn: n = 0, 3 to 5, 9, CM, CS, CT, DL) Port n function control register (PFCn: n = 3, 5, 9) Port n function register (PFn: n = 3 to 5, 9) Pull-up resistor option register (PUn: n = 0, 3 to 5, 9)
Ports	Input only: 8 I/O: 59
Pull-up resistors	Software control: 31

Table 4-5. Port Configuration (V850ES/KG1)

Item	Configuration
Control registers	Port n register (Pn: n = 0, 1, 3 to 5, 7, 9, CM, CS, CT, DL, DH) Port n mode register (PMn: n = 0, 1, 3 to 5, 9, CM, CS, CT, DL, DH) Port n mode control register (PMCn: n = 0, 3 to 5, 9, CM, CS, CT, DL, DH) Port n function control register (PFCn: n = 3, 5, 9) Port n function register (PFn: n = 3 to 5, 9) Pull-up resistor option register (PUn: n = 0, 1, 3 to 5, 9)
Ports	Input only: 8 I/O: 76
Pull-up resistors	Software control: 40

Table 4-6. Port Configuration (V850ES/KJ1)

Item	Configuration
Control registers	Port n register (Pn: n = 0, 1, 3 to 9, CD, CM, CS, CT, DL, DH) Port n mode register (PMn: n = 0, 1, 3 to 6, 8, 9, CD, CM, CS, CT, DL, DH) Port n mode control register (PMCn: n = 0, 3 to 6, 8, 9, CM, CS, CT, DL, DH) Port n function control register (PFCn: n = 3, 5, 6, 8, 9) Port n function register (PFn: n = 3 to 6, 8, 9) Pull-up resistor option register (PUn: n = 0, 1, 3 to 6, 8, 9)
Ports	Input only: 8 I/O: 112
Pull-up resistors	Software control: 56

(1) Port n register (Pn)

Data I/O with external devices is performed by writing to and reading from the port n register (Pn). The port n register is configured of a port latch that retains the output data and a circuit that reads the pin status.

Each bit of the port n register corresponds to one pin of port n and can be read/written in 1-bit units.

After reset: 00H[Note] (output latch) R/W

	7	6	5	7	3	2	1	0
Pn	Pn7	Pn6	Pn5	Pn4	Pn3	Pn2	Pn1	Pn0

Pnm	Control of output data (in output mode)
0	0 is output
1	1 is output

Note Input-only port pins are undefined.

Writing to and reading from the Pn register is executed as follows independent of the setting of the port n mode control register (PMCn).

Table 4-7. Reading to/Writing from Port n Register (Pn)

Setting of PMn Register	Writing to Pn Register	Reading from Pn Register
Output mode (PMnm = 0)	Write to the output latch[Note]. In the port mode (PMCn = 0), the contents of the output latch are output from the pin.	The value of the output latch is read.
Input mode (PMnm = 1)	Write to the output latch. The status of the pin is not affected[Note].	The pin status is read.

Note The value written to the output latch is retained until a value is next written to the output latch.

(2) Port n mode register (PMn)

PMn specifies the input mode/output mode of the port.

Each bit of the port n mode register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: FFH R/W

	7	6	5	4	3	2	1	0
PMn	PMn7	PMn6	PMn5	PMn4	PMn3	PMn2	PMn1	PMn0

PMnm	Control of I/O mode
0	Output mode
1	Input mode

(3) Port n mode control register (PMCn)

PMCn specifies the port mode/alternate function.

Each bit of the port n mode control register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PMCn	PMCn7	PMCn6	PMCn5	PMCn4	PMCn3	PMCn2	PMCn1	PMCn0

PMCnm	Specification of operation mode
0	Port mode
1	Alternate function mode

(4) Port n function control register (PFCn)

PFCn is a register that specifies the alternate function to be used when one pin has two or more alternate functions.

Each bit of the port n function control register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PFCn	PFCn7	PFCn6	PFCn5	PFCn4	PFCn3	PFCn2	PFCn1	PFCn0

PFCnm	Specification of alternate function
0	Alternate function 1
1	Alternate function 2

(5) Port n function register (PFn)

PFn is a register that specifies normal output/N-ch open-drain output.

Each bit of the port n function register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: 00H R/W

	7	6	5	4	3	2	1	0
PFn	PFn7	PFn6	PFn5	PFn4	PFn3	PFn2	PFn1	PFn0

PFnm	Control of normal output/N-ch open-drain output
0	Normal output (CMOS output)
1	N-ch open-drain output

Note The PFnm bit of the PFn register is valid only when the PMnm bit of the PMn register is 0 (output mode) regardless of the setting of the PMCn register. When the PMnm bit is 1 (input mode), the set value in the PFn register is invalid.

Example <1> When the value of the PFn register is valid
PFnm bit = 1 … N-ch open-drain output is specified.
PMnm bit = 0 … Output mode is specified.
PMCnm bit = 0 or 1

<2> When the value of the PFn register is invalid
PFnm bit = 0 … N-ch open-drain output is specified.
PMnm bit = 1 … Input mode is specified.
PMCnm bit = 0 or 1

(6) Pull-up resistor option register (PUn)

PUn is a register that specifies the connection of an on-chip pull-up resistor.

Each bit of the pull-up resistor option register corresponds to one pin of port n and can be specified in 1-bit units.

After reset: 00H R/W

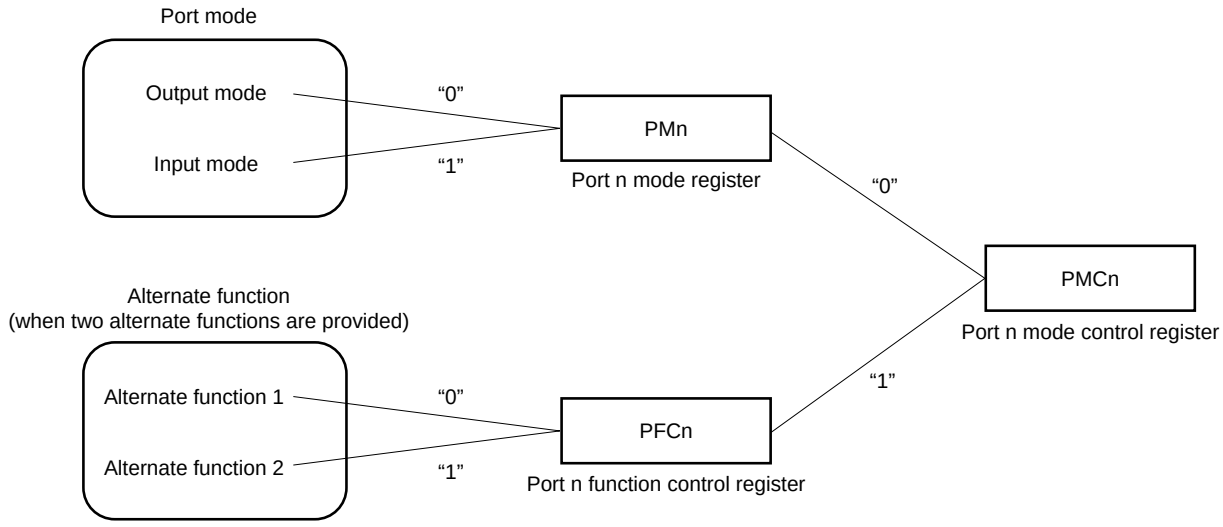
	7	6	5	4	3	2	1	0
PUn	PUn7	PUn6	PUn5	PUn4	PUn3	PUn2	PUn1	PUn0

PUnm	Control of on-chip pull-up resistor connection
0	Not connected
1	Connected

(7) Port settings

Set the ports as follows.

Figure 4-1. Register Settings and Pin Functions



Remark Switch to the alternate function using the following procedure.

<1> Set the PFCn register.
<2> Set the PMCn register
<3> Set external interrupt rising/falling edge specification register n (INTRn/INTFn) (when external interrupt pin is set)

If the PMCn register is set first, another unintended alternate function may be set while the PFCn register is being set.

4.3.1 Port 0

Input/output for port 0 can be controlled in 1-bit units.

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 have the same number of I/O port pins for port 0.

Product	I/O Port Pin Count
V850ES/KF1	7-bit I/O port
V850ES/KG1	7-bit I/O port
V850ES/KJ1	7-bit I/O port

Port 0 includes the following alternate functions.

Table 4-7. Alternate-Function Pins of Port 0

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port 0	P00	TOH0	Output	Yes	–	D-2
	P01	TOH1	Output			D-2
	P02	NMI	Input		Analog noise elimination	H-1
	P03	INTP0	Input			H-1
	P04	INTP1	Input			H-1
	P05	INTP2	Input			H-1
	P06	INTP3	Input			H-1

Note Software pull-up function

★ **Caution P02 to P06 have hysteresis characteristics when the alternate function is input, but not in the port mode.**

(1) Registers

(a) Port 0 register (P0)

After reset: 00H (output latch) R/W Address: FFFFF400H

	7	6	5	4	3	2	1	0
P0	0	P06	P05	P04	P03	P02	P01	P00

P0n	Control of output data (in output mode) (n = 0 to 6)
0	0 is output
1	1 is output

(b) Port 0 mode register (PM0)

After reset: FFH R/W Address: FFFFF420H

	7	6	5	4	3	2	1	0
PM0	1	PM06	PM05	PM04	PM03	PM02	PM01	PM00

PM0n	Control of I/O mode (n = 0 to 6)
0	Output mode
1	Input mode

(c) Port 0 mode control register (PMC0)

After reset: 00H R/W Address: FFFFF440H

	7	6	5	4	3	2	1	0
PMC0	0	PMC06	PMC05	PMC04	PMC03	PMC02	PMC01	PMC00

PMC06	Specification of P06 pin operation mode
0	I/O port
1	INTP3 input

PMC05	Specification of P05 pin operation mode
0	I/O port
1	INTP2 input

PMC04	Specification of P04 pin operation mode
0	I/O port
1	INTP1 input

PMC03	Specification of P03 pin operation mode
0	I/O port
1	INTP0 input

PMC02	Specification of P02 pin operation mode
0	I/O port
1	NMI input

PMC01	Specification of P01 pin operation mode
0	I/O port
1	TOH1 output

PMC00	Specification of P00 pin operation mode
0	I/O port
1	TOH0 output

(d) Pull-up resistor option register 0 (PU0)

After reset: 00H R/W Address: FFFFFC40H

	7	6	5	4	3	2	1	0
PU0	0	PU06	PU05	PU04	PU03	PU02	PU01	PU00

PU0n	Control of on-chip pull-up resistor connection (n = 0 to 6)
0	Not connected
1	Connected

4.3.2 Port 1

Input/output for port 1 can be controlled in 1-bit units.

The number of I/O port pins for port 1 differs according to the product.

Product	I/O Port Pin Count
V850ES/KF1	–
V850ES/KG1	2-bit I/O port
V850ES/KJ1	2-bit I/O port

Port 1 includes the following alternate functions.

Table 4-8. Alternate-Function Pins of Port 1 (V850ES/KG1, V850ES/KJ1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port 1	P10	ANO0	Output	Yes	–	A-2
	P11	ANO1	Output			A-2

Note Software pull-up function

(1) Registers

(a) Port 1 register (P1)

(i) V850ES/KG1, V850ES/KJ1

After reset: 00H (output latch) R/W Address: FFFFF402H

	7	6	5	4	3	2	1	0
P1	0	0	0	0	0	0	P11	P10

P1n	Control of output data (in output mode) (n = 0, 1)
0	0 is output
1	1 is output

(b) Port 1 mode register (PM1)

Caution When used as the ANO0 and ANO1 pins, set PM1 = FFH all together.

(i) V850ES/KG1, V850ES/KJ1

After reset: FFH R/W Address: FFFFF422H

	7	6	5	4	3	2	1	0
PM1	1	1	1	1	1	1	PM11	PM10

PM1n	Control of I/O mode (n = 0, 1)
0	Output mode
1	Input mode

(c) Pull-up resistor option register 1 (PU1)

(i) V850ES/KG1, V850ES/KJ1

After reset: 00H R/W Address: FFFFFC42H

	7	6	5	4	3	2	1	0
PU1	0	0	0	0	0	0	PU11	PU10

PU1n	Control of on-chip pull-up resistor connection (n = 0, 1)
0	Not connected
1	Connected

4.3.3 Port 3

Input/output for port 3 can be controlled in 1-bit units.

The number of I/O port pins differs according to the product.

Product	I/O Port Pin Count
V850ES/KF1	8-bit I/O port
V850ES/KG1	10-bit I/O port
V850ES/KJ1	10-bit I/O port

Port 3 includes the following alternate functions.

Table 4-9. Alternate-Function Pins of Port 3 (V850ES/KF1)

Pin Name		Alternate Function	I/O	PULL[Note 1]	Remark	Block Type
Port 3	P30	TXD0	Output	Yes	–	D-2
	P31	RXD0	Input			D-1
	P32	ASCK0	I/O			D-1
	P33	TI000/TO00	I/O			E-6
	P34	TI001	Input			D-1
	P35	TI010/TO01	I/O			E-6
	P38	SDA0[Note 2]	I/O	No[Note 3]	N-ch open-drain output	J
	P39	SCL0[Note 2]	I/O			J

Notes 1. Software pull-up function

2. Only in products with an I^2C bus

3. An on-chip pull-up resistor can be provided by a mask option (only for the mask ROM version of the V850ES/KF1).

★ **Caution P31 to P35, P38, and P39 have hysteresis characteristics when the alternate function is input, but not in the port mode.**

Table 4-10. Alternate-Function Pins of Port 3 (V850ES/KG1, V850ES/KJ1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port 3	P30	TXD0	Output	Yes	–	D-2
	P31	RXD0	Input			D-1
	P32	ASCK0	I/O			D-1
	P33	TI000/TO00	I/O			E-6
	P34	TI001	Input			D-1
	P35	TI010/TO01	I/O			E-6
	P36	–	–	No[Note 2]	N-ch open-drain output	J
	P37	–	–			J
	P38	SDA0[Note 3]	I/O			K
	P39	SCL0[Note 3]	I/O			K

Notes 1. Software pull-up function

2. An on-chip pull-up resistor can be provided by a mask option (only for the mask ROM versions of the V850ES/KG1 and V850ES/KJ1).

3. Only for products with an I^2C bus

★ **Caution P31 to P35, P38, and P39 have hysteresis characteristics when the alternate function is input, but not in the port mode.**

(1) Registers

(a) Port 3 register (P3)

(i) V850ES/KF1

After reset: 00H (output latch) R/W Address: P3 FFFFF406H,
P3L FFFFF406H, P3H FFFFF407H

	15	14	13	12	11	10	9	8
P3 (P3H[Note])	0	0	0	0	0	0	P39	P38

	7	6	5	4	3	2	1	0
(P3L)	0	0	P35	P34	P33	P32	P31	P30

P3n	Control of output data (in output mode) (n = 0 to 5, 8, 9)
0	0 is output
1	1 is output

(ii) V850ES/KG1, V850ES/KJ1

After reset: 00H R/W Address: P3 FFFFF406H,
P3L FFFFF406H, P3H FFFFF407H

	15	14	13	12	11	10	9	8
P3 (P3H[Note])	0	0	0	0	0	0	P39	P38

	7	6	5	4	3	2	1	0
(P3L)	P37	P36	P35	P34	P33	P32	P31	P30

P3n	Control of output data (in output mode) (n = 0 to 9)
0	0 is output
1	1 is output

Note When reading from or writing to bits 8 to 15 of the P3 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the P3H register.

Remark The port 3 register (P3) can be read/written in 16-bit units only.
However, when the higher 8 bits and the lower 8 bits of the P3 register are used as the P3H register and as the P3L register, respectively, this register can be read/written in 8-bit or 1-bit units.

(b) Port 3 mode register (PM3)

(i) V850ES/KF1

After reset: FFFFH R/W Address: PM3 FFFFF426H,
PM3L FFFFF426H, PM3H FFFFF427H

	15	14	13	12	11	10	9	8
PM3 (PM3H[Note])	1	1	1	1	1	1	PM39	PM38

	7	6	5	4	3	2	1	0
(PM3L)	1	1	PM35	PM34	PM33	PM32	PM31	PM30

PM3n	Control of I/O mode (n = 0 to 5, 8, 9)
0	Output mode
1	Input mode

(ii) V850ES/KG1, V850ES/KJ1

After reset: FFFFH R/W Address: PM3 FFFFF426H,
PM3L FFFFF426H, PM3H FFFFF427H

	15	14	13	12	11	10	9	8
PM3 (PM3H[Note])	1	1	1	1	1	1	PM39	PM38

	7	6	5	4	3	2	1	0
(PM3L)	PM37	PM36	PM35	PM34	PM33	PM32	PM31	PM30

PM3n	Control of I/O mode (n = 0 to 9)
0	Output mode
1	Input mode

Note When reading from or writing to bits 8 to 15 of the PM3 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PM3H register.

Remark When the higher 8 bits and the lower 8 bits of the PM3 register are used as the PM3H register and as the PM3L register, respectively, this register can be read/written in 8-bit or 1-bit units.

(c) Port 3 mode control register (PMC3)

(i) V850ES/KF1, V850ES/KG1, V850ES/KJ1

After reset: 0000H R/W Address: PMC3 FFFFF446H,
PMC3L FFFFF446H, PMC3H FFFFF447H

	15	14	13	12	11	10	9	8
PMC3 (PMC3H[Note 1])	0	0	0	0	0	0	PMC39[Note]	PMC38[Note]

	7	6	5	4	3	2	1	0
(PMC3L)	0	0	PMC35	PMC34	PMC33	PMC32	PMC31	PMC30

PMC39	Specification of P39 pin operation mode
0	I/O port
1	SCL0 I/O

PMC38	Specification of P38 pin operation mode
0	I/O port
1	SDA0 I/O

PMC35	Specification of P35 pin operation mode
0	I/O port
1	TI010/TO01 I/O

PMC34	Specification of P34 pin operation mode
0	I/O port
1	TI001 input

PMC33	Specification of P33 pin operation mode
0	I/O port
1	TI000/TO00 I/O

PMC32	Specification of P32 pin operation mode
0	I/O port
1	ASCK0 input

PMC31	Specification of P31 pin operation mode
0	I/O port
1	RXD0 input

PMC30	Specification of P30 pin operation mode
0	I/O port
1	TXD0 output

Notes 1. When reading from or writing to bits 8 to 15 of the PMC3 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PMC3H register.

2. Only in products with an I^2C bus. In all other products, set this bit to 0.

Remark This register can be read/written in 16-bit units only.
When the higher 8 bits and the lower 8 bits of the PMC3 register are used as the PMC3H register and as the PMC3L register, respectively, this register can be read/written in 8-bit or 1-bit units.

(d) Port 3 function register H (PF3H)

After reset: 00H R/W Address: FFFFFC67H

	7	6	5	4	3	2	1	0
PF3H	0	0	0	0	0	0	PF39	PF38

PF3n	Specification of normal port/alternate function (n = 8, 9)
0	When used as normal port (N-ch open-drain output)
1	When used as alternate-function (N-ch open-drain output)

Caution When using P38 and P39 as N-ch open-drain-output alternate-function pins, set in the following sequence.
Be sure to set the port latch to 1 before setting the pin to N-ch open-drain output.
P3n bit = 1 → PF3n bit = 1 → PMC3n bit = 1

(e) Port 3 function control register (PFC3)

(i) V850ES/KF1, V850ES/KG1, V850ES/KJ1

After reset: 00H R/W Address: FFFFF466H

	7	6	5	4	3	2	1	0
PFC3	0	0	PFC35	0	PFC33	0	0	0

PFC35	Specification of P35 pin operation mode in control mode
0	TI010 input
1	TO01 output

PFC33	Specification of P33 pin operation mode in control mode
0	TI000 input
1	TO00 output

Caution Always set bits 0 to 2, 4, 6, and 7 of the PFC3 register to 0.

(f) Pull-up resistor option register 3 (PU3)

(i) V850ES/KF1, V850ES/KG1, V850ES/KJ1

After reset: 00H R/W Address: FFFFFC46H

	7	6	5	4	3	2	1	0
PU3	0	0	PU35	PU34	PU33	PU32	PU31	PU30

PU3n	Control of on-chip pull-up resistor connection (n = 0 to 5)
0	Not connected
1	Connected

Caution An on-chip pull-up resistor can be provided for P3n by a mask option.
n = 8, 9: In the mask ROM version of the V850ES/KF1
n = 6 to 9: In the mask ROM versions of the V850ES/KG1 and V850ES/KJ1

4.3.4 Port 4

Input/output for port 4 can be controlled in 1-bit units.

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 have the same number of I/O port pins for port 4.

Product	I/O Port Pin Count
V850ES/KF1	3-bit I/O port
V850ES/KG1	3-bit I/O port
V850ES/KJ1	3-bit I/O port

Port 4 includes the following alternate functions.

Table 4-11. Alternate-Function Pins of Port 4

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port 4	P40	SI00	Input	Yes	–	D-1
	P41	SO00	Output		N-ch open-drain output can be selected.	F-1
	P42	$\overline{\text{SCK00}}$	I/O			F-2

Note Software pull-up function

★ **Caution P40 and P42 have hysteresis characteristics when the alternate function is input, but not in the port mode.**

(1) Registers

(a) Port 4 register (P4)

After reset: 00H (output latch) R/W Address: FFFFF408H

	7	6	5	4	3	2	1	0
P4	0	0	0	0	0	P42	P41	P40

P4n	Control of output data (in output mode) (n = 0 to 2)
0	0 is output
1	1 is output

(b) Port 4 mode register (PM4)

After reset: FFH R/W Address: FFFFF428H

	7	6	5	4	3	2	1	0
PM4	1	1	1	1	1	PM42	PM41	PM40

PM4n	Control of I/O mode (n = 0 to 2)
0	Output mode
1	Input mode

(c) Port 4 mode control register (PMC4)

After reset: 00H R/W Address: FFFFF448H

	7	6	5	4	3	2	1	0
PMC4	0	0	0	0	0	PMC42	PMC41	PMC40

PMC42	Specification of P42 pin operation mode
0	I/O port
1	$\overline{\text{SCK00}}$ I/O

PMC41	Specification of P41 pin operation mode
0	I/O port
1	SO00 output

PMC40	Specification of P40 pin operation mode
0	I/O port
1	SI00 input

(d) Port 4 function register (PF4)

After reset: 00H R/W Address: FFFFFC68H

	7	6	5	4	3	2	1	0
PF4	0	0	0	0	0	PF42	PF41	0

PF4n	Control of normal output/N-ch open-drain output
0	Normal output
1	N-ch open-drain output

Caution When using P41 and P42 as N-ch open-drain-output alternate-function pins, set in the following sequence.
Be sure to set the port latch to 1 before setting the pin to N-ch open-drain output.
P4n bit = 1 → PF4n bit = 1 → PMC4n bit = 1

(e) Pull-up resistor option register 4 (PU4)

After reset: 00H R/W Address: FFFFFC48H

	7	6	5	4	3	2	1	0
PU4	0	0	0	0	0	PU42	PU41	PU40

PU4n	Control of on-chip pull-up resistor connection (n = 0 to 2)
0	Not connected
1	Connected

4.3.5 Port 5

Input/output for port 5 can be controlled in 1-bit units.

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 have the same number of I/O port pins for port 5.

Product	I/O Port Pin Count
V850ES/KF1	6-bit I/O port
V850ES/KG1	6-bit I/O port
V850ES/KJ1	6-bit I/O port

Port 5 includes the following alternate functions.

Table 4-12. Alternate-Function Pins of Port 5

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port 5	P50	TI011/RTP00/KR0	I/O	Yes	–	E-5
	P51	TI50/RTP01/KR1	I/O			E-5
	P52	TO50/RTP02/KR2	I/O			E-4
	P53	SIA0/RTP03/KR3	I/O			E-5
	P54	SOA0/RTP04/KR4	I/O		N-ch open-drain output can be selected.	G-1
	P55	$\overline{\text{SCKA0}}$/RTP05/KR5	I/O			G-2

Note Software pull-up function

(1) Registers

(a) Port 5 register (P5)

After reset: 00H (output latch) R/W Address: FFFFF40AH

	7	6	5	4	3	2	1	0
P5	0	0	P55	P54	P53	P52	P51	P50

P5n	Control of output data (in output mode) (n = 0 to 5)
0	0 is output
1	1 is output

(b) Port 5 mode register (PM5)

After reset: FFH R/W Address: FFFFF42AH

	7	6	5	4	3	2	1	0
PM5	1	1	PM55	PM54	PM53	PM52	PM51	PM50

PM5n	Control of I/O mode (n = 0 to 5)
0	Output mode
1	Input mode

(c) Port 5 mode control register (PMC5)

After reset: 00H R/W Address: FFFFF44AH

	7	6	5	4	3	2	1	0
PMC5	0	0	PMC55	PMC54	PMC53	PMC52	PMC51	PMC50

PMC55	Specification of P55 pin operation mode
0	I/O port/KR5 input
1	$\overline{\text{SCKA0}}$/RTP05 I/O

PMC54	Specification of P54 pin operation mode
0	I/O port/KR4 input
1	SOA0/RTP04 output

PMC53	Specification of P53 pin operation mode
0	I/O port/KR3 input
1	SIA0/RTP03 I/O

PMC52	Specification of P52 pin operation mode
0	I/O port/KR2 input
1	TO50/RTP0 output

PMC51	Specification of P51 pin operation mode
0	I/O port/KR1 input
1	TI50/RTP01 I/O

PMC50	Specification of P50 pin operation mode
0	I/O port/KR0 input
1	TI011/RTP00 I/O

(d) Port 5 function register 5 (PF5)

After reset: 00H R/W Address: FFFFFC6AH

	7	6	5	4	3	2	1	0
PF5	0	0	PF55	PF54	0	0	0	0

PF5n	Control of normal output/N-ch open-drain output (n = 4, 5)
0	Normal output
1	N-ch open-drain output

Cautions 1. Always set bits 0 to 3, 6, and 7 of the PF5 register to 0.

2. When using P54 and P55 as N-ch open-drain-output alternate-function pins, set in the following sequence.

Be sure to set the port latch to 1 before setting the pin to N-ch open-drain output.

P5n bit = 1 → PF5n bit = 1 → PMC5n bit = 1

(e) Port 5 function control register (PFC5)

After reset: 00H R/W Address: FFFFF46AH

	7	6	5	4	3	2	1	0
PFC5	0	0	PFC55	PFC54	PFC53	PFC52	PFC51	PFC50

PFC55	Specification of P55 pin operation mode in control mode
0	$\overline{\text{SCKA0}}$ I/O
1	RTP05 output

PFC54	Specification of P54 pin operation mode in control mode
0	SOA0 output
1	RTP04 output

PFC53	Specification of P53 pin operation mode in control mode
0	SIA0 input
1	RTP03 output

PFC52	Specification of P52 pin operation mode in control mode
0	TO50 output
1	RTP02 output

PFC51	Specification of P51 pin operation mode in control mode
0	TI50 input
1	RTP01 output

PFC50	Specification of P50 pin operation mode in control mode
0	TI011 input
1	RTP00 output

(f) Pull-up resistor option register 5 (PU5)

After reset: 00H R/W Address: FFFFFC4AH

	7	6	5	4	3	2	1	0
PU5	0	0	PU55	PU54	PU53	PU52	PU51	PU50

PU5n	Control of on-chip pull-up resistor connection (n = 0 to 5)
0	Not connected
1	Connected

4.3.6 Port 6

Input/output for port 6 can be controlled in 1-bit units.

The number of I/O port pins for port 6 differs according to the product.

Product	I/O Port Pin Count
V850ES/KF1	–
V850ES/KG1	–
V850ES/KJ1	16-bit I/O port

Port 6 includes the following alternate functions.

Table 4-13. Alternate-Function Pins of Port 6 (V850ES/KJ1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port 6	P60	RTP10	Output	Yes	–	D-2
	P61	RTP11	Output			D-2
	P62	RTP12	Output			D-2
	P63	RTP13	Output			D-2
	P64	RTP14	Output			D-2
	P65	RTP15	Output			D-2
	P66	SI02	Input			D-1
	P67	SO02	Output		N-ch open-drain output	F-1
	P68	$\overline{\text{SCK02}}$	I/O			F-2
	P69	TI040	Input		–	D-1
	P610	TI041	Input			D-1
	P611	TO04	Output			D-2
	P612	TI050	Input			D-1
	P613	TI051/TO05	I/O			E-6
	P614	–	–	No		J
	P615	–	–			J

Note Software pull-up function

★ **Caution P66, P68, P69, P610, P612, and P613 have hysteresis characteristics when the alternate function is input, but not in the port mode.**

(1) Registers

(a) Port 6 register (P6)

(i) V850ES/KJ1

After reset: 00H (output latch) R/W Address: P6 FFFFF40CH,
P6L FFFFF40CH, P6H FFFFF40DH

	15	14	13	12	11	10	9	8
P6 (P6H[Note])	P615	P614	P613	P612	P611	P610	P69	P68

	7	6	5	4	3	2	1	0
(P6L)	P67	P66	P65	P64	P63	P62	P61	P60

P6n	Control of output data (in output mode) (n = 0 to 15)
0	0 is output
1	1 is output

Note When reading from or writing to bits 8 to 15 of the P6 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the P6H register.

Remark The port 6 register (P6) can be read/written in 16-bit units only. However, when the higher 8 bits and the lower 8 bits of the P6 register are used as the P6H register and as the P6L register, respectively, this register can be read/written in 8-bit or 1-bit units.

(b) Port 6 mode register (PM6)

(i) V850ES/KJ1

After reset: FFFFH R/W Address: PM6 FFFFF42CH,
PM6L FFFFF42CH, PM6H FFFFF42DH

	15	14	13	12	11	10	9	8
PM6 (PM6H[Note])	PM615	PM614	PM613	PM612	PM611	PM610	PM69	PM68

	7	6	5	4	3	2	1	0
(PM6L)	PM67	PM66	PM65	PM64	PM63	PM62	PM61	PM60

PM6n	Control of I/O mode (n = 0 to 15)
0	Output mode
1	Input mode

Note When reading from or writing to bits 8 to 15 of the PM6 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PM6H register.

Remark The PM6 register can be read/written in 16-bit units only.
However, when the higher 8 bits and the lower 8 bits of the PM6 register are used as the PM6H register and as the PM6L register, respectively, this register can be read/written in 8-bit or 1-bit units.

(c) Port 6 mode control register (PMC6)

(i) V850ES/KJ1

After reset: 0000H R/W Address: PMC6 FFFFF44CH,
PMC6L FFFFF44CH, PMC6H FFFFF44DH

	15	14	13	12	11	10	9	8
PMC6 (PMC6H[Note])	0	0	PMC613	PMC612	PMC611	PMC610	PMC69	PMC68

	7	6	5	4	3	2	1	0
(PMC6L)	PMC67	PMC66	PMC65	PMC64	PMC63	PMC62	PMC61	PMC60

PMC613	Specification of P613 pin operation mode
0	I/O port
1	TI051/TO05 I/O

PMC612	Specification of P612 pin operation mode
0	I/O port
1	TI050 input

PMC611	Specification of P611 pin operation mode
0	I/O port
1	TO04 output

PMC610	Specification of P610 pin operation mode
0	I/O port
1	TI041 input

PMC69	Specification of P69 pin operation mode
0	I/O port
1	TI040 input

PMC68	Specification of P68 pin operation mode
0	I/O port
1	$\overline{\text{SCK02}}$ I/O

PMC67	Specification of P67 pin operation mode
0	I/O port
1	SO02 output

PMC66	Specification of P66 pin operation mode
0	I/O port
1	SI02 input

PMC6n	Specification of P6n pin operation mode (n = 0 to 5)
0	I/O port
1	RTP1n output

Note When reading from or writing to bits 8 to 15 of the PMC6 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PMC6H register.

Remark The PMC6 register can be read/written in 16-bit units only.
However, when the higher 8 bits and the lower 8 bits of the PMC6 register are used as the PMC6H register and as the PMC6L register, respectively, this register can be read/written in 8-bit or 1-bit units.

(d) Port 6 function register (PF6)

(i) V850ES/KJ1

After reset: 0000H R/W Address: PF6 FFFFFC6CH,
PF6L FFFFFC6CH, PF6H FFFFFC6DH

	15	14	13	12	11	10	9	8
PF6 (PF6H[Note])	0	0	0	0	0	0	0	PF68

	7	6	5	4	3	2	1	0
(PF6L)	PF67	0	0	0	0	0	0	0

PF6n	Control of normal output/N-ch open-drain output (n = 7, 8)
0	Normal output
1	N-ch open-drain output

Note When reading from or writing to bits 8 to 15 of the PF6 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PF6H register.

Caution Always set PF6 register bits 0 to 6 and 9 to 15 to 0.

Remark The PF6 register can be read/written in 16-bit units only.
However, when the higher 8 bits and the lower 8 bits of the PF6 register are used as the PF6H register and as the PF6L register, respectively, this register can be read/written in 8-bit or 1-bit units.

(e) Port 6 function control register (PFC6H)

(i) V850ES/KJ1

After reset: 00H R/W Address: FFFFF46DH

	7	6	5	4	3	2	1	0
PFC6H	0	0	PFC613	0	0	0	0	0

PFC613	Specification of P613 pin operation mode in control mode
0	TI051 input
1	TO05 output

(f) Pull-up resistor option register 6 (PU6)

(i) V850ES/KJ1

After reset: 0000H R/W Address: PU6 FFFFFC4CH,
PU6L FFFFFC4CH, PU6H FFFFFC4DH

	15	14	13	12	11	10	9	8
PU6 (PU6H[Note])	0	0	PU613	PU612	PU611	PU610	PU69	PU68

	7	6	5	4	3	2	1	0
(PU6L)	PU67	PU66	PU65	PU64	PU63	PU62	PU61	PU60

PU6n	Control of on-chip pull-up resistor connection (n = 0 to 13)
0	Not connected
1	Connected

Note When reading from or writing to bits 8 to 15 of the PU6 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PU6H register.

Caution An on-chip pull-up resistor can be provided for P614 and P615 (only in the mask ROM version of the V850ES/KJ1).

Remark When the higher 8 bits and the lower 8 bits of the PU6 register are used as the PU6H register and as the PU6L register, respectively, this register can be read/written in 8-bit or 1-bit units.

4.3.7 Port 7

All the pins of port 7 are fixed to input.

The number of input port pins for port 7 differs according to the product.

Product	Input Port Pin Count
V850ES/KF1	8-bit input port
V850ES/KG1	8-bit input port
V850ES/KJ1	16-bit input port

Port 7 includes the following alternate functions.

Table 4-14. Alternate-Function Pins of Port 7 (V850ES/KF1, V850ES/KG1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port 7	P70	ANI0	Input	No	–	A-1
	P71	ANI1	Input			A-1
	P72	ANI2	Input			A-1
	P73	ANI3	Input			A-1
	P74	ANI4	Input			A-1
	P77	ANI5	Input			A-1
	P76	ANI6	Input			A-1
	P77	ANI7	Input			A-1

Note Software pull-up function

Table 4-15. Alternate-Function Pins of Port 7 (V850ES/KJ1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port 7	P70	ANI0	Input	No	–	A-1
	P71	ANI1	Input			A-1
	P72	ANI2	Input			A-1
	P73	ANI3	Input			A-1
	P74	ANI4	Input			A-1
	P77	ANI5	Input			A-1
	P76	ANI6	Input			A-1
	P77	ANI7	Input			A-1
	P78	ANI8	Input			A-1
	P79	ANI9	Input			A-1
	P710	ANI10	Input			A-1
	P711	ANI11	Input			A-1
	P712	ANI12	Input			A-1
	P713	ANI13	Input			A-1
	P714	ANI14	Input			A-1
	P715	ANI15	Input			A-1

Note Software pull-up function

(1) Registers

(a) Port 7 register (P7)

(i) V850ES/KF1, V850ES/KG1

After reset: Undefined R Address: FFFFF40EH

	7	6	5	4	3	2	1	0
P7	P77	P76	P75	P74	P73	P72	P71	P70

P7n	Input data read (n = 0 to 7)
0	Input low level
1	Input high level

(ii) V850ES/KJ1

After reset: Undefined R Address: FFFFF40EH (P7, P7L), FFFFF40FH (P7H)

	15	14	13	12	11	10	9	8
P7 (P7H[Note])	P715	P714	P713	P712	P711	P710	P79	P78

	7	6	5	4	3	2	1	0
(P7L)	P77	P76	P75	P74	P73	P72	P71	P70

P7n	Input data read (n = 0 to 12)
0	Input low level
1	Input high level

Note When reading from or writing to bits 8 to 15 of the P7 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the P7H register.

Remark The port 7 register (P7) of the V850ES/KJ1 can be read only in 16-bit units. However, when the higher 8 bits of the P7 register are used as the P7H register and the lower 8 bits as the P7L register, they can be read in 8-bit units.

4.3.8 Port 8

Input/output for port 8 can be controlled in 1-bit units.

The number of I/O port pins differs according to the product.

Product	I/O Port Pin Count
V850ES/KF1	–
V850ES/KG1	–
V850ES/KJ1	2-bit I/O port

Port 8 includes the following alternate functions.

Table 4-16. Alternate-Function Pins of Port 8 (V850ES/KJ1)

Pin Name		Alternate Function	I/O	PULL[Note 1]	Remark	Block Type
Port 8	P80	RXD2/SDA1[Note 2]	I/O	Yes	N-ch open-drain output can be selected.	G-5
	P81	TXD2/SCL1[Note 2]	I/O			G-6

Notes 1. Software pull-up function

2. Only in the μPD703216Y, 703217Y, and 70F3217Y

★ **Caution P80 and P81 have hysteresis characteristics when the alternate function is input, but not in the port mode.**

(1) Registers

(a) Port 8 register (P8)

(i) V850ES/KJ1

After reset: 00H (output latch) R/W Address: FFFFF410H

	7	6	5	4	3	2	1	0
P8	0	0	0	0	0	0	P81	P80

P8n	Control of output data (in output mode) (n = 0, 1)
0	0 is output
1	1 is output

(b) Port 8 mode register (PM8)

(i) V850ES/KJ1

After reset: FFH R/W Address: FFFFF430H

	7	6	5	4	3	2	1	0
PM8	1	1	1	1	1	1	PM81	PM80

PM8n	Control of I/O mode (n = 0, 1)
0	Output mode
1	Input mode

(c) Port 8 mode control register (PMC8)

(i) V850ES/KJ1

After reset: 00H R/W Address: FFFFF450H

	7	6	5	4	3	2	1	0
PMC8	0	0	0	0	0	0	PMC81	PMC80

PMC81	Specification of P81 pin operation mode
0	I/O port
1	TXD2/SCL1[Note] I/O

PMC80	Specification of P80 pin operation mode
0	I/O port
1	RXD2/SDA1[Note] I/O

Note Only in the μPD703216Y, 703217Y, and 70F3217Y.

(d) Port 8 function register (PF8)

(i) V850ES/KJ1

After reset: 00H R/W Address: FFFFFC70H

	7	6	5	4	3	2	1	0
PF8	0	0	0	0	0	0	PF81	PF80

PF8n	Control of normal output/N-ch open-drain output (n = 0, 1)
0	Normal output
1	N-ch open-drain output

Caution When using P80 and P81 as N-ch open-drain-output alternate-function pins, set in the following sequence.
Be sure to set the port latch to 1 before setting the pin to N-ch open-drain output.
P8n bit = 1 → PFC8n bit = 0/1 → PF8n bit = 1 → PMC8n bit = 1

(e) Port 8 function control register (PFC8)

(i) V850ES/KJ1

After reset: 00H R/W Address: FFFFF470H

	7	6	5	4	3	2	1	0
PFC8	0	0	0	0	0	0	PFC81	PFC80

PFC81	Specification of P81 pin operation mode in control mode
0	TXD2 output
1	SCL1[Note] I/O

PFC80	Specification of P80 pin operation mode in control mode
0	RXD2 input
1	SDA1[Note] I/O

Note Only in the μPD703216Y, 703217Y, and 70F3217Y. Set to 0 for all other products.

(f) Pull-up resistor option register 8 (PU8)

(i) V850ES/KJ1

After reset: 00H R/W Address: FFFFFC50H

	7	6	5	4	3	2	1	0
PU8	0	0	0	0	0	0	PU81	PU80

PU8n	Control of on-chip pull-up resistor connection (n = 0, 1)
0	Not connected
1	Connected

4.3.9 Port 9

Input/output for port 9 can be controlled in 1-bit units.

The number of I/O port pins for port 9 differs according to the product.

Product	I/O Port Pin Count
V850ES/KF1	9-bit I/O port
V850ES/KG1	16-bit I/O port
V850ES/KJ1	16-bit I/O port

Port 9 includes the following alternate functions.

Table 4-17. Alternate-Function Pins of Port 9 (V850ES/KF1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port 9	P90	TXD1/KR6	I/O	No	–	E-3
	P91	RXD1/KR7	Input			E-1
	P96	TI51/TO51	I/O			E-3
	P97	SI01	Input			E-2
	P98	SO01	Output		N-ch open-drain output can be specified.	G-4
	P99	$\overline{\text{SCK01}}$	I/O			G-3
	P913	INTP4	Input		Analog noise elimination	H-2
	P914	INTP5	Input			H-2
	P915	INTP6	Input			H-2

Note Software pull-up function

★ **Caution P97, P99, and P913 to P915 have hysteresis characteristics when the alternate function is input, but not in the port mode.**

Table 4-18. Alternate-Function Pins of Port 9 (V850ES/KG1, V850ES/KJ1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port 9	P90	A0/TXD1/KR6	I/O	No	–	E-3
	P91	A1/RXD1/KR7	I/O			E-1
	P92	A2/TI020/TO02	I/O			E-3
	P93	A3/TI021	I/O			E-2
	P94	A4/TI030/TO03	I/O			E-3
	P95	A5/TI031	I/O			E-2
	P96	A6/TI51/TO51	I/O			E-3
	P97	A7/SI01	I/O			E-2
	P98	A8/SO01	Output		N-ch open-drain output can be specified.	G-4
	P99	A9/$\overline{\text{SCK01}}$	I/O			G-3
	P910	A10/SIA1	I/O		–	E-2
	P911	A11/SOA1	Output		N-ch open-drain output can be specified.	G-4
	P912	A12/$\overline{\text{SCKA1}}$	I/O			G-3
	P913	A13/INTP4	I/O		Analog noise elimination	H-2
	P914	A14/INTP5	I/O			H-2
	P915	A15/INTP6	I/O			H-2

Note Software pull-up function

★ **Caution P93, P95, P97, P99, P910, and P912 to P915 have hysteresis characteristics when the alternate function is input, but not in the port mode.**

(1) Registers

(a) Port 9 register (P9)

(i) V850ES/KF1

After reset: 00H (output latch) R/W Address: P9 FFFFF412H,
P9L FFFFF412H, P9H FFFFF413H

	15	14	13	12	11	10	9	8
P9 (P9H[Note])	P915	P914	P913	0	0	0	P99	P98

	7	6	5	4	3	2	1	0
(P9L)	P97	P96	0	0	0	0	P91	P90

P9n	Control of output data (in output mode) (n = 0, 1, 6 to 9, 13 to 15)
0	0 is output
1	1 is output

(ii) V850ES/KG1, V850ES/KJ1

After reset: 00H (output latch) R/W Address: P9H FFFFF412H,
P9L FFFFF412H, P9H FFFFF413H

	15	14	13	12	11	10	9	8
P9 (P9H[Note])	P915	P914	P913	P912	P911	P910	P99	P98

	7	6	5	4	3	2	1	0
(P9L)	P97	P96	P95	P94	P93	P92	P91	P90

P9n	Control of output data (in output mode) (n = 0 to 15)
0	0 is output
1	1 is output

Note When reading from or writing to bits 8 to 15 of the P9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the P9H register.

Remark The port 9 register (P9) can be read/written in 16-bit units only. However, when the higher 8 bits and the lower 8 bits of the P9 register are used as the P9H register and as the P9L register, respectively, these registers can be read/written in 8-bit or 1-bit units.

(b) Port 9 mode register (PM9)

(i) V850ES/KF1

After reset: FFFFH R/W Address: PM9 FFFFF432H,
PM9L FFFFF432H, PM9H FFFFF433H

	15	14	13	12	11	10	9	8
PM9 (PM9H[Note])	PM915	PM914	PM913	1	1	1	PM99	PM98

	7	6	5	4	3	2	1	0
(PM9L)	PM97	PM96	1	1	1	1	PM91	PM90

PM9n	Control of I/O mode (n = 0, 1, 6 to 9, 13 to 15)
0	Output mode
1	Input mode

(ii) V850ES/KG1, V850ES/KJ1

After reset: FFFFH R/W Address: PM9 FFFFF432H,
PM9L FFFFF432H, PM9H FFFFF433H

	15	14	13	12	11	10	9	8
PM9 (PM9H[Note])	PM915	PM914	PM913	PM912	PM911	PM910	PM99	PM98

	7	6	5	4	3	2	1	0
(PM9L)	PM97	PM96	PM95	PM94	PM93	PM92	PM91	PM90

PM9n	Control of I/O mode (n = 0 to 5)
0	Output mode
1	Input mode

Note When reading from or writing to bits 8 to 15 of the PM9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PM9H register.

Remark The PM9 register can be read/written in 16-bit units only.
However, when the higher 8 bits and the lower 8 bits of the PM9 register are used as the PM9H register and as the PM9L register, respectively, this register can be read/written in 8-bit or 1-bit units.

(c) Port 9 mode control register (PMC9)

Caution When using port 9 as the A0 to A15 pins, set the PMC9 register to FFFFH in 16-bit units (only in V850ES/KG1, V850ES/KJ1).

(i) V850ES/KJ1

After reset: 0000H R/W Address: PMC9 FFFFF452H,
PMC9 FFFFF452H, PMC9H FFFFF453H

	15	14	13	12	11	10	9	8
PMC9 (PMC9H[Note])	PMC915	PMC914	PMC913	0	0	0	PMC99	PMC98

	7	6	5	4	3	2	1	0
(PMC9L)	PMC97	PMC96	0	0	0	0	PMC91	PMC90

PMC915	Specification of P915 pin operation mode
0	I/O port
1	INTP6 input

PMC914	Specification of P914 pin operation mode
0	I/O port
1	INTP5 input

PMC913	Specification of P612 pin operation mode
0	I/O port
1	INTP4 input

PMC99	Specification of P99 pin operation mode
0	I/O port
1	$\overline{\text{SCK01}}$ I/O

PMC98	Specification of P98 pin operation mode
0	I/O port
1	SO01 output

PMC97	Specification of P97 pin operation mode
0	I/O port
1	SI01 input

PMC96	Specification of P96 pin operation mode
0	I/O port/TI51 input
1	TO51 output

PMC91	Specification of P91 pin operation mode
0	I/O port/KR7 input
1	RXD1 input

PMC90	Specification of P90 pin operation mode
0	I/O port/KR6 input
1	TXD1 output

Note When reading from or writing to bits 8 to 15 of the PMC9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PMC9H register.

Remark The PMC9 register can be read/written in 16-bit units only.
However, when the higher 8 bits and the lower 8 bits of the PMC9 register are used as the PMC9H register and as the PMC9L register, respectively, these registers can be read/written in 8-bit or 1-bit units.

(1/2)

(ii) V850ES/KG1, V850ES/KJ1

After reset: 0000H R/W Address: PMC9 FFFFF452H,
PMC9L FFFFF452H, PMC9H FFFFF453H

	15	14	13	12	11	10	9	8
PMC9 (PMC9H[Note])	PMC915	PMC914	PMC913	PMC912	PMC911	PMC910	PMC99	PMC98

	7	6	5	4	3	2	1	0
(PMC9L)	PMC97	PMC96	PMC95	PMC94	PMC93	PMC92	PMC91	PMC90

PMC915	Specification of P915 pin operation mode
0	I/O port
1	A15/INTP6 I/O

PMC914	Specification of P914 pin operation mode
0	I/O port
1	A14/INTP5 I/O

PMC913	Specification of P913 pin operation mode
0	I/O port
1	A13/INTP4 I/O

PMC912	Specification of P912 pin operation mode
0	I/O port
1	A12/$\overline{\text{SCKA1}}$ I/O

PMC911	Specification of P911 pin operation mode
0	I/O port
1	A11/SOA1 output

PMC910	Specification of P910 pin operation mode
0	I/O port
1	A10/SIA1 I/O

PMC99	Specification of P99 pin operation mode
0	I/O port
1	A9/$\overline{\text{SCK01}}$ I/O

PMC98	Specification of P98 pin operation mode
0	I/O port
1	A8/SO01 output

Note When reading from or writing to bits 8 to 15 of the PMC9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PMC9H register.

Remark The PMC9 register can be read/written in 16-bit units only.
However, when the higher 8 bits and the lower 8 bits of the PMC9 register are used as the PMC9H register and as the PMC9L register, respectively, these registers can be read/written in 8-bit or 1-bit units.

(2/2)

PMC97	Specification of P97 pin operation mode
0	I/O port
1	A7/SI01 I/O

PMC96	Specification of P96 pin operation mode
0	I/O port/TI51
1	A6/TO51 output

PMC95	Specification of P95 pin operation mode
0	I/O port
1	A5/TI031 I/O

PMC94	Specification of P94 pin operation mode
0	I/O port/TI030 input
1	A4/TO03 output

PMC93	Specification of P93 pin operation mode
0	I/O port
1	A3/TI021 I/O

PMC92	Specification of P92 pin operation mode
0	I/O port/TI020 input
1	A2/TO02 output

PMC91	Specification of P91 pin operation mode
0	I/O port/KR7 input
1	A1/RXD1 I/O

PMC90	Specification of P90 pin operation mode
0	I/O port/KR6 input
1	A0/TXD1 output

(d) Port 9 function register H (PF9H)

(i) V850ES/KF1

After reset: 00H R/W Address: FFFFFC73H

	7	6	5	4	3	2	1	0
PF9H	0	0	0	0	0	0	PF99	PF98

PF9n	Control of normal output/N-ch open-drain output (n = 0, 1)
0	Normal output
1	N-ch open-drain output

(ii) V850ES/KG1, V850ES/KJ1

After reset: 00H R/W Address: FFFFFC73H

	7	6	5	4	3	2	1	0
PF9H	0	0	0	PF912	PF911	0	PF99	PF98

PF9n	Control of normal output/N-ch open-drain output (n = 0, 1, 4, 5)
0	Normal output
1	N-ch open-drain output

Caution When using P98, P99, P911, and P912 as N-ch open-drain-output alternate-function pins, set in the following sequence.
Be sure to set the port latch to 1 before setting the pin to N-ch open-drain output.
P9n bit = 1 → PFC9n bit = 0/1 → PF9n bit = 1 → PMC9n bit = 1

(e) Port 9 function control register (PFC9)

Cautions 1. When using port 9 as the A0 to A15 pins, set the PFC9 register to 0000H in 16-bit units (only in V850ES/KG1, V850ES/KJ1).
2. When the control mode is set by the PMC9n bit of the PMC9 register with the PFC9n bit of the PFC9 register maintaining the initial value (0), output becomes undefined. Therefore, to set control mode 2 of port 9, set the PFC9n bit to 1 first and then set the PMC9n bit to 1 (n = 0, 1, 6 to 9, 13 to 15) (V850ES/KF1 only).

(i) V850ES/KF1

After reset: 0000H R/W Address: PFC9 FFFFF472H,
PFC9L FFFFF472H, PFC9H FFFFF473H

	15	14	13	12	11	10	9	8
PFC9 (PFC9H[Note])	PFC910	PFC910	PFC910	0	0	0	PFC99	PFC98

	7	6	5	4	3	2	1	0
(PFC9L)	PFC97	PFC96	0	0	0	0	PFC91	PFC90

PFC915	Specification of P915 pin operation mode in control mode
1	INTP6 input

PFC914	Specification of P914 pin operation mode in control mode
1	INTP5 input

PFC913	Specification of P913 pin operation mode in control mode
1	INTP4 input

PFC99	Specification of P99 pin operation mode in control mode
1	$\overline{\text{SCK01}}$ I/O

PFC98	Specification of P98 pin operation mode in control mode
1	SO01 output

PFC97	Specification of P97 pin operation mode in control mode
1	SI01 input

PFC96	Specification of P96 pin operation mode in control mode
1	TO51 output

PFC91	Specification of P91 pin operation mode in control mode
1	RXD1 input

PFC90	Specification of P90 pin operation mode in control mode
1	TXD1 output

Note When reading from or writing to bits 8 to 15 of the PFC9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PFC9H register.

Remark The PFC9 register can be read/written in 16-bit units only.
However, when the higher 8 bits and the lower 8 bits of the PFC9 register are used as the PFC9H register and as the PFC9L register, respectively, these registers can be read/written in 8-bit or 1-bit units.

(1/2)

(ii) V850ES/KG1, V850ES/KJ1

After reset: 0000H R/W Address: PFC9 FFFFF472H,
PFC9L FFFFF472H, PFC9H FFFFF473H

	15	14	13	12	11	10	9	8
PFC9 (PFC9H[Note])	PFC915	PFC914	PFC913	PFC912	PFC911	PFC910	PFC99	PFC98

	7	6	5	4	3	2	1	0
(PFC9L)	PFC97	PFC96	PFC95	PFC94	PFC93	PFC92	PFC91	PFC90

PFC915	Specification of P915 pin operation mode in control mode
0	A15 output
1	INTP6 input

PFC914	Specification of P914 pin operation mode in control mode
0	A14 output
1	INTP5 input

PFC913	Specification of P913 pin operation mode in control mode
0	A13 output
1	INTP4 input

PFC912	Specification of P912 pin operation mode in control mode
0	A12 output
1	$\overline{\text{SCKA1}}$ I/O

PFC911	Specification of P911 pin operation mode in control mode
0	A11 output
1	SOA1 output

PFC910	Specification of P910 pin operation mode in control mode
0	A10 output
1	SIA1 input

PFC99	Specification of P99 pin operation mode in control mode
0	A9 output
1	$\overline{\text{SCK01}}$ I/O

PFC98	Specification of P98 pin operation mode in control mode
0	A8 output
1	SO01 output

Note When reading from or writing to bits 8 to 15 of the PFC9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PFC9H register.

Remark The PFC9 register can be read/written in 16-bit units only.
However, when the higher 8 bits and the lower 8 bits of the PFC9 register are used as the PFC9H register and as the PFC9L register, respectively, these registers can be read/written in 8-bit or 1-bit units.

(2/2)

PFC97	Specification of P97 pin operation mode in control mode
0	A7 output
1	SI01 input

PFC96	Specification of P96 pin operation mode in control mode
0	A6 output
1	TO51 output

PFC95	Specification of P95 pin operation mode in control mode
0	A5 output
1	TI031 input

PFC94	Specification of P94 pin operation mode in control mode
0	A4 output
1	TO03 output

PFC93	Specification of P93 pin operation mode in control mode
0	A3 output
1	TI021 input

PFC92	Specification of P92 pin operation mode in control mode
0	A2 output
1	TO02 output

PFC91	Specification of P91 pin operation mode in control mode
0	A1 output
1	RXD1 input

PFC90	Specification of P90 pin operation mode in control mode
0	A0 output
1	TXD1 output

(f) Pull-up resistor option register 9 (PU9)

(i) V850ES/KF1

After reset: 0000H R/W Address: PU9 FFFFFC52H,
PU9L FFFFFC52H, PU9H FFFFFC53H

	15	14	13	12	11	10	9	8
PU9 (PU9H[Note])	PU915	PU914	PU913	0	0	0	PU99	PU98

	7	6	5	4	3	2	1	0
(PU9L)	PU97	PU96	0	0	0	0	PU91	PU90

PU9n	Control of on-chip pull-up resistor connection (n = 0, 1, 6 to 9, 13 to 15)
0	Not connected
1	Connected

★ (ii) V850ES/KG1,V850ES/KJ1

After reset: 0000H R/W Address: PU9 FFFFFC52H,
PU9L FFFFFC52H, PU9H FFFFFC53H

	15	14	13	12	11	10	9	8
PU9 (PU9H[Note])	PU915	PU914	PU913	PU912	PU911	PU910	PU99	PU98

	7	6	5	4	3	2	1	0
(PU9L)	PU97	PU96	PU95	PU94	PU93	PU92	PU91	PU90

PU9n	Control of on-chip pull-up resistor connection (n = 0 to 15)
0	Not connected
1	Connected

Note When reading from or writing to bits 8 to 15 of the PU9 register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PU9H register.

Remark The PU9 register can be read/written in 16-bit units only.
However, when the higher 8 bits and the lower 8 bits of the PU9 register are used as the PU9H register and as the PU9L register, respectively, these registers can be read/written in 8-bit or 1-bit units.

4.3.10 Port CD

Input/output for port CD be controlled in 1-bit units.

The number of I/O port pins for port CD differs according to the product.

Product	I/O Port Pin Count
V850ES/KF1	–
V850ES/KG1	–
V850ES/KJ1	4-bit I/O port

Port CD does not have alternate-function pins.

Table 4-19. Alternate-Function Pins of Port CD (V850ES/KJ1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port CD	PCD0	–	–	No	–	B-1
	PCD1	–	–			B-1
	PCD2	–	–			B-1
	PCD3	–	–			B-1

Note Software pull-up function

(1) Registers

(a) Port CD register (PCD)

(i) V850ES/KJ1

After reset: 00H (output latch) R/W Address: FFFFF00EH

	7	6	5	4	3	2	1	0
PCD	0	0	0	0	PCD3	PCD2	PCD1	PCD0

PCDn	Control of output data (in output mode) (n = 0 to 3)
0	0 is output
1	1 is output

(b) Port CD mode register (PMCD)

(i) V850ES/KJ1

After reset: FFH R/W Address: FFFFF02EH

	7	6	5	4	3	2	1	0
PMCD	1	1	1	1	PMCD3	PMCD2	PMCD1	PMCD0

PMCDn	Control of I/O mode (n = 0 to 3)
0	Output mode
1	Input mode

4.3.11 Port CM

Input/output for port CM can be controlled in 1-bit units.

The number of I/O port pins for port CM differs according to the product.

Product	I/O Port Pin Count
V850ES/KF1	4-bit I/O port
V850ES/KG1	4-bit I/O port
V850ES/KJ1	6-bit I/O port

Port CM includes the following alternate functions.

Table 4-20. Alternate-Function Pins of Port CM (V850ES/KF1, V850ES/KG1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port CM	PCM0	$\overline{\text{WAIT}}$	Input	No	–	C-1
	PCM1	CLKOUT	Output			C-2
	PCM2	$\overline{\text{HLDAK}}$	Output			C-2
	PCM3	$\overline{\text{HLDQR}}$	Input			C-1

Note Software pull-up function

Table 4-21. Alternate-Function Pins of Port CM (V850ES/KJ1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port CM	PCM0	$\overline{\text{WAIT}}$	Input	No	–	C-1
	PCM1	CLKOUT	Output			C-2
	PCM2	$\overline{\text{HLDAK}}$	Output			C-2
	PCM3	$\overline{\text{HLDQR}}$	Input			C-1
	PCM4	–	–			B-1
	PCM5	–	–			B-1

Note Software pull-up function

(1) Registers

(a) Port CM register (PCM)

(i) V850ES/KF1, v850ES/KG1

After reset: 00H (output latch) R/W Address: FFFFF00CH

	7	6	5	4	3	2	1	0
PCM	0	0	0	0	PCM3	PCM2	PCM1	PCM0

PCMn	Control of output data (in output mode) (n = 0 to 3)
0	0 is output
1	1 is output

(ii) V850ES/KJ1

After reset: 00H (output latch) R/W Address: FFFFF00CH

	7	6	5	4	3	2	1	0
PCM	0	0	PCM5	PCM4	PCM3	PCM2	PCM1	PCM0

PCMn	Control of output data (in output mode) (n = 0 to 5)
0	0 is output
1	1 is output

(b) Port CM mode register (PMCM)

(i) V850ES/KF1, V850ES/KG1

After reset: FFH R/W Address: FFFFF02CH

	7	6	5	4	3	2	1	0
PMCM	1	1	1	1	PMCM3	PMCM2	PMCM1	PMCM0

PMCMn	Control of I/O mode (n = 0 to 3)
0	Output mode
1	Input mode

(ii) V850ES/KJ1

After reset: FFH R/W Address: FFFFF02CH

	7	6	5	4	3	2	1	0
PMCM	1	1	PMCM5	PMCM4	PMCM3	PMCM2	PMCM1	PMCM0

PMCMn	Control of I/O mode (n = 0 to 5)
0	Output mode
1	Input mode

(c) Port CM mode control register (PMCCM)

(i) V850ES/KF1, V850ES/KG1, V850ES/KJ1

After reset: 00H R/W Address: FFFFF04CH

	7	6	5	4	3	2	1	0
PMCCM	0	0	0	0	PMCCM3	PMCCM2	PMCCM1	PMCCM0

PMCCM3	Specification of PCM3 pin operation mode
0	I/O port
1	$\overline{\text{HLDQR}}$ input

PMCCM2	Specification of PCM2 pin operation mode
0	I/O port
1	$\overline{\text{HLDAK}}$ output

PMCCM1	Specification of PCM1 pin operation mode
0	I/O port
1	CLKOUT output

PMCCM0	Specification of PCM0 pin operation mode
0	I/O port
1	$\overline{\text{WAIT}}$ input

4.3.12 Port CS

Input/output of port CS can be controlled in 1-bit units.

The number of I/O port pins for port CS differs according to the product.

Product	I/O Port Pin Count
V850ES/KF1	2-bit I/O port
V850ES/KG1	2-bit I/O port
V850ES/KJ1	8-bit I/O port

Port CS includes the following alternate functions.

Table 4-22. Alternate-Function Pins of Port CS (V850ES/KF1, V850ES/KG1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port CS	PCS0	$\overline{CS0}$	Output	No	–	C-3
	PCS1	$\overline{CS1}$	Output			C-3

Note Software pull-up function

Table 4-23. Alternate-Function Pins of Port CS (V850ES/KJ1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port CS	PCS0	$\overline{CS0}$	Output	No	–	C-3
	PCS1	$\overline{CS1}$	Output			C-3
	PCS2	$\overline{CS2}$	Output			C-3
	PCS3	$\overline{CS3}$	Output			C-3
	PCS4	–	–			B-1
	PCS5	–	–			B-1
	PCS6	–	–			B-1
	PCS7	–	–			B-1

Note Software pull-up function

(1) Registers

(a) Port CS register (PCS)

(i) V850ES/KF1, V850ES/KG1

After reset: 00H (output latch) R/W Address: FFFFF008H

	7	6	5	4	3	2	1	0
PCS	0	0	0	0	0	0	PCS1	PCS0

PCSn	Control of output data (in output mode) (n = 0, 1)
0	0 is output
1	1 is output

(ii) V850ES/KJ1

After reset: 00H (output latch) R/W Address: FFFFF008H

	7	6	5	4	3	2	1	0
PCS	PCS7	PCS6	PCS5	PCS4	PCS3	PCS2	PCS1	PCS0

PCSn	Control of output data (in output mode) (n = 0 to 7)
0	0 is output
1	1 is output

(b) Port CS mode register (PMCS)

(i) V850ES/KF1, V850ES/KG1

After reset: FFH R/W Address: FFFFF028H

	7	6	5	4	3	2	1	0
PMCS	1	1	1	1	1	1	PMCS1	PMCS0

PMCSn	Control of I/O mode (n = 0, 1)
0	Output mode
1	Input mode

(ii) V850ES/KJ1

After reset: FFH R/W Address: FFFFF028H

	7	6	5	4	3	2	1	0
PMCS	PMCS7	PMCS6	PMCS5	PMCS4	PMCS3	PMCS2	PMCS1	PMCS0

PMCSn	Control of I/O mode (n = 0 to 7)
0	Output mode
1	Input mode

(c) Port CS mode control register (PMCCS)

(i) V850ES/KF1, V850ES/KG1

After reset: 00H R/W Address: FFFFF048H

	7	6	5	4	3	2	1	0
PMCCS	0	0	0	0	0	0	PMCCS1	PMCCS0

PMCCSn	Specification of PCSn pin operation mode (n = 0, 1)
0	I/O port
1	$\overline{\text{CSn}}$ output

(ii) V850ES/KJ1

After reset: 00H R/W Address: FFFFF048H

	7	6	5	4	3	2	1	0
PMCCS	0	0	0	0	PMCCS3	PMCCS2	PMCCS1	PMCCS0

PMCCSn	Specification of PCSn pin operation mode (n = 0 to 3)
0	I/O port
1	$\overline{\text{CSn}}$ output

4.3.13 Port CT

Input/output for port CT can be controlled in 1-bit units.

The number of I/O port pins for port CT differs according to the product.

Product	I/O Port Pin Count
V850ES/KF1	4-bit I/O port
V850ES/KG1	4-bit I/O port
V850ES/KJ1	8-bit I/O port

Port CT includes the following alternate functions.

Table 4-24. Alternate-Function Pins of Port CT (V850ES/KF1, V850ES/KG1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port CT	PCT0	$\overline{WR0}$	Output	No	–	C-3
	PCT1	$\overline{WR1}$	Output			C-3
	PCT4	$\overline{RD}$	Output			B-1
	PCT6	ASTB	Output			B-1

Note Software pull-up function

Table 4-25. Alternate-Function Pins of Port CT (V850ES/KJ1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port CT	PCT0	$\overline{WR0}$	Output	No	–	C-3
	PCT1	$\overline{WR1}$	Output			C-3
	PCT2	–	–			B-1
	PCT3	–	–			B-1
	PCT4	$\overline{RD}$	Output			C-3
	PCT5	–	–			B-1
	PCT6	ASTB	Output			C-3
	PCT7	–	–			B-1

Note Software pull-up function

(1) Registers

(a) Port CT register (PCT)

(i) V850ES/KF1, V850ES/KG1

After reset: 00H (output latch) R/W Address: FFFFF00AH

	7	6	5	4	3	2	1	0
PCT	0	PCT6	0	PCT4	0	0	PCT1	PCT0

PCTn	Control of output data (in output mode) (n = 0, 1, 4, 6)
0	0 is output
1	1 is output

(ii) V850ES/KJ1

After reset: 00H (output latch) R/W Address: FFFFF00AH

	7	6	5	4	3	2	1	0
PCT	PCT7	PCT6	PCT5	PCT4	PCT3	PCT2	PCT1	PCT0

PCTn	Control of output data (in output mode) (n = 0 to 7)
0	0 is output
1	1 is output

(b) Port CT mode register (PMCT)

(i) V850ES/KF1, V850ES/KG1

After reset: FFH R/W Address: FFFFF02AH

	7	6	5	4	3	2	1	0
PMCT	1	PMCT6	1	PMCT4	1	1	PMCT1	PMCT0

PMCTn	Control of I/O mode (n = 0, 1, 4, 6)
0	Output mode
1	Input mode

(ii) V850ES/KJ1

After reset: FFH R/W Address: FFFFF02AH

	7	6	5	4	3	2	1	0
PMCT	PMCT7	PMCT6	PMCT5	PMCT4	PMCT3	PMCT2	PMCT1	PMCT0

PMCTn	Control of I/O mode (n = 0 to 7)
0	Output mode
1	Input mode

(c) Port CT mode control register (PMCCT)

(i) V850ES/KF1, V850ES/KG1, V850ES/KJ1

After reset: 00H R/W Address: FFFFF04AH

	7	6	5	4	3	2	1	0
PMCCT	0	PMCCT6	0	PMCCT4	0	0	PMCCT1	PMCCT0

PMCCT6	Specification of PCT6 pin operation mode
0	I/O port
1	ASTB output

PMCCT4	Specification of PCT4 pin operation mode
0	I/O port
1	$\overline{RD}$ output

PMCCT1	Specification of PCT1 pin operation mode
0	I/O port
1	$\overline{WR1}$ output

PMCCT0	Specification of PCT0 pin operation mode
0	I/O port
1	$\overline{WR0}$ output

4.3.14 Port DH

Input/output for port DH can be controlled in 1-bit units.

The number of I/O port pins for port DH differs according to the product.

Product	I/O Port Pin Count
V850ES/KF1	–
V850ES/KG1	6-bit I/O port
V850ES/KJ1	8-bit I/O port

Port DH includes the following alternate functions.

Table 4-26. Alternate-Function Pins of Port DH (V850ES/KG1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port DH	PDH0	A16	Output	No	–	C-3
	PDH1	A17	Output			C-3
	PDH2	A18	Output			C-3
	PDH3	A19	Output			C-3
	PDH4	A20	Output			C-3
	PDH5	A21	Output			C-3

Note Software pull-up function

Table 4-27. Alternate-Function Pins of Port DH (V850ES/KJ1)

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port DH	PDH0	A16	Output	No	–	C-3
	PDH1	A17	Output			C-3
	PDH2	A18	Output			C-3
	PDH3	A19	Output			C-3
	PDH4	A20	Output			C-3
	PDH5	A21	Output			C-3
	PDH6	A22	Output			C-3
	PDH7	A23	Output			C-3

Note Software pull-up function

(1) Registers

(a) Port DH register (PDH)

(i) V850ES/KG1

After reset: 00H (output latch) R/W Address: FFFFF006H

	7	6	5	4	3	2	1	0
PDH	0	0	PDH5	PDH4	PDH3	PDH2	PDH1	PDH0

PDHn	Control of output data (in output mode) (n = 0 to 5)
0	0 is output
1	1 is output

(ii) V850ES/KJ1

After reset: 00H (output latch) R/W Address: FFFFF006H

	7	6	5	4	3	2	1	0
PDH	PDH7	PDH6	PDH5	PDH4	PDH3	PDH2	PDH1	PDH0

PDHn	Control of output data (in output mode) (n = 0 to 7)
0	0 is output
1	1 is output

(b) Port DH mode register (PMDH)

(i) V850ES/KG1

After reset: FFH R/W Address: FFFFF026H

	7	6	5	4	3	2	1	0
PMDH	1	1	PMDH5	PMDH4	PMDH3	PMDH2	PMDH1	PMDH0

PMDHn	Control of I/O mode (n = 0 to 5)
0	Output mode
1	Input mode

(ii) V850ES/KJ1

After reset: FFH R/W Address: FFFFF026H

	7	6	5	4	3	2	1	0
PMDH	PMDH7	PMDH6	PMDH5	PMDH4	PMDH3	PMDH2	PMDH1	PMDH0

PMDHn	Control of I/O mode (n = 0 to 7)
0	Output mode
1	Input mode

(c) Port DH mode control register (PMCDH)

(i) V850ES/KG1

After reset: 00H R/W Address: FFFFF046H

	7	6	5	4	3	2	1	0
PMCDH	0	0	PMCDH5	PMCDH4	PMCDH3	PMCDH2	PMCDH1	PMCDH0

PMCDHn	Specification of PDHn pin operation mode (n = 0 to 5)
0	I/O port
1	Am output (address bus output) (m = 16 to 21)

Caution When specifying the port mode/control mode (alternate function) for each bit, pay careful attention to the operation of the alternate functions.

(ii) V850ES/KJ1

After reset: 00H R/W Address: FFFFF046H

	7	6	5	4	3	2	1	0
PMCDH	PMCDH7	PMCDH6	PMCDH5	PMCDH4	PMCDH3	PMCDH2	PMCDH1	PMCDH0

PMCDHn	Specification of PDHn pin operation mode (n = 0 to 7)
0	I/O port
1	Am output (address bus output) (m = 16 to 23)

Caution When specifying the port mode/control mode (alternate function) for each bit, pay careful attention to the operation of the alternate functions.

4.3.15 Port DL

Input/output of port DL can be controlled in 1-bit units.

The number of I/O port pins for port DL is the same in each product.

Product	I/O Port Pin Count
V850ES/KF1	16-bit I/O port
V850ES/KG1	16-bit I/O port
V850ES/KJ1	16-bit I/O port

Port DL includes the following alternate functions.

Table 4-28. Alternate-Function Pins of Port DL

Pin Name		Alternate Function	I/O	PULL[Note]	Remark	Block Type
Port DL	PDL0	AD0	I/O	No	–	C-4
	PDL1	AD1	I/O			C-4
	PDL2	AD2	I/O			C-4
	PDL3	AD3	I/O			C-4
	PDL4	AD4	I/O			C-4
	PDL5	AD5	I/O			C-4
	PDL6	AD6	I/O			C-4
	PDL7	AD7	I/O			C-4
	PDL8	AD8	I/O			C-4
	PDLDL	AD9	I/O			C-4
	PDL10	AD10	I/O			C-4
	PDL11	AD11	I/O			C-4
	PDL12	AD12	I/O			C-4
	PDL13	AD13	I/O			C-4
	PDL14	AD14	I/O			C-4
	PDL15	AD15	I/O			C-4

Note Software pull-up function

(1) Registers

(a) Port DL register (PDL)

After reset: 00H (output latch) R/W Address: PDL FFFFF004H,
PDLL FFFFF004H, PDLH FFFFF005H

	15	14	13	12	11	10	9	8
PDL (PDLH[Note])	PDL15	PDL14	PDL13	PDL12	PDL11	PDL10	PDL9	PDL8

	7	6	5	4	3	2	1	0
(PDLL)	PDL7	PDL6	PDL5	PDL4	PDL3	PDL2	PDL1	PDL0

PDLn	Control of output data (in output mode) (n = 0 to 15)
0	0 is output
1	1 is output

Note When reading from or writing to bits 8 to 15 of the PDL register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PDLH register.

Remark The port DL register (PDL) can be read/written in 16-bit units only. However, when the higher 8 bits and the lower 8 bits of the PDL register are used as the PDLH register and as the PDLL register, respectively, these registers can be read/written in 8-bit or 1-bit units.

(b) Port DL mode register (PMDL)

After reset: FFFFH R/W Address: PMDL FFFFF024H,
PMDLL FFFFF024H, PMDLH FFFFF025H

	15	14	13	12	11	10	9	8
PMDL (PMDLH[Note])	PMDL15	PMDL14	PMDL13	PMDL12	PMDL11	PMDL10	PMDL9	PMDL8

	7	6	5	4	3	2	1	0
(PMDLL)	PMDL7	PMDL6	PMDL5	PMDL4	PMDL3	PMDL2	PMDL1	PMDL0

PMDLn	Control of I/O mode (n = 0 to 15)
0	Output mode
1	Input mode

Note When reading from or writing to bits 8 to 15 of the PMDL register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PMDLH register.

Remark The PMDL register can be read/written in 16-bit units only. However, when the higher 8 bits and the lower 8 bits of the PMDL register are used as the PMDLH register and as the PMDLL register, respectively, these registers can be read/written in 8-bit or 1-bit units.

(c) Port DL mode control register (PMCDL)

After reset: 0000H R/W Address: PMCDL FFFFF044H,
PMCDLL FFFFF044H, PMCDLH FFFFF045H

	15	14	13	12	11	10	9	8
PMCDL (PMCDLH[Note])	PMCDL15	PMCDL14	PMCDL13	PMCDL12	PMCDL11	PMCDL10	PMCDL9	PMCDL8

	7	6	5	4	3	2	1	0
(PMCDLL)	PMCDL7	PMCDL6	PMCDL5	PMCDL4	PMCDL3	PMCDL2	PMCDL1	PMCDL0

PMCDLn	Specification of PDLn pin operation mode (n = 0 to 15)
0	I/O port
1	ADn I/O (address/data bus I/O)

Note When reading from or writing to bits 8 to 15 of the PMCDL register in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the PMCDLH register.

Caution When specifying the port mode/control mode (alternate function) for each bit, pay careful attention to the operation of the alternate functions.

Remark The PMCDL register can be read/written in 16-bit units only.
However, when the higher 8 bits and the lower 8 bits of the PMCDL register are used as the PMCDLH register and as the PMCDLL register, respectively, these registers can be read/written in 8-bit or 1-bit units.

★ 4.4 Block Diagrams

Figure 4-2. Block Diagram of Type A-1

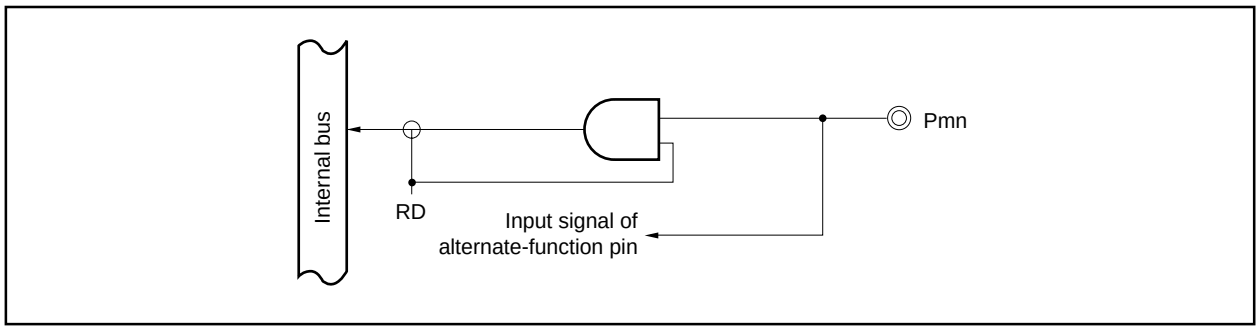


Figure 4-3. block Diagram of Type A-2

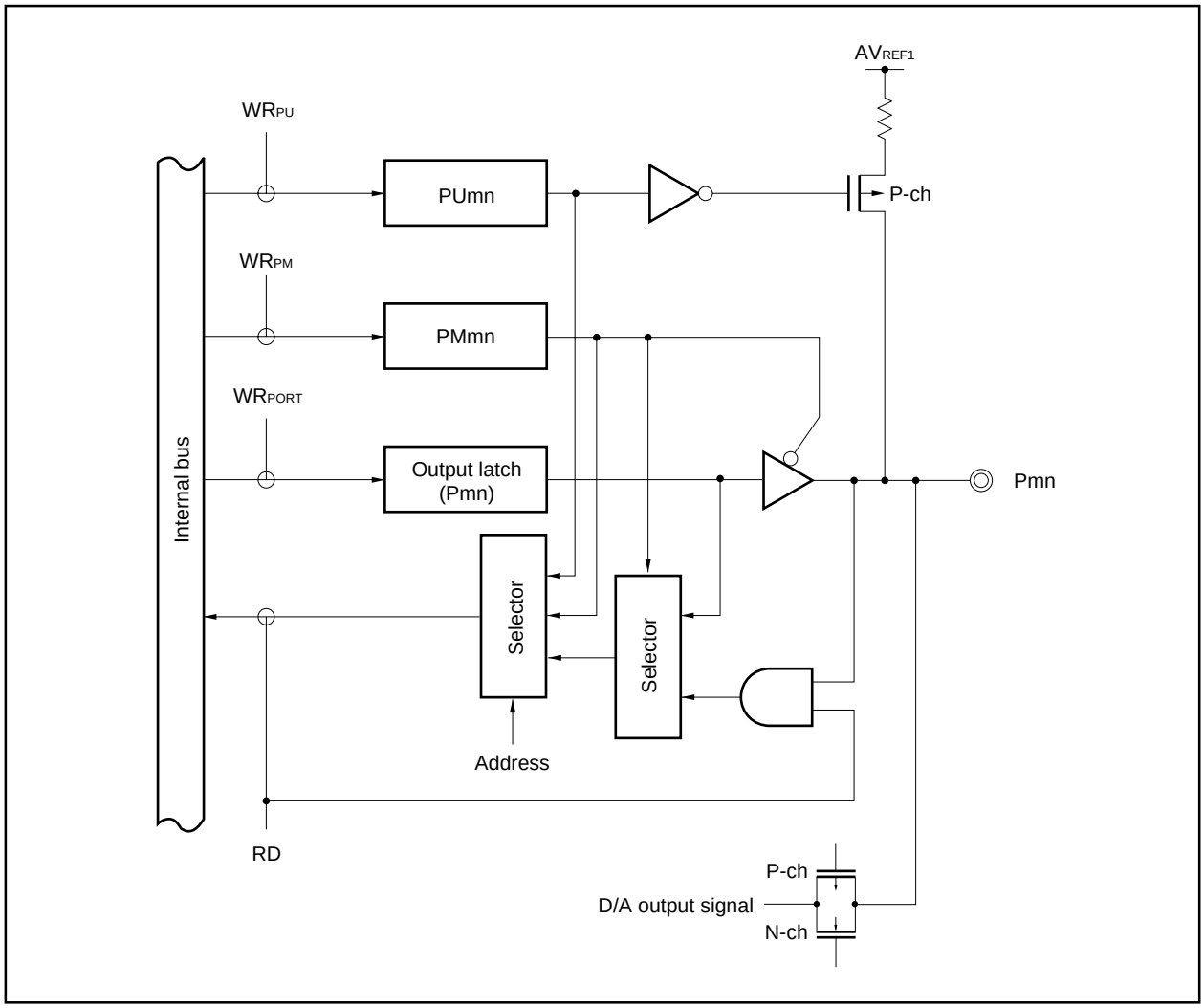


Figure 4-4. Block Diagram of Type B-1

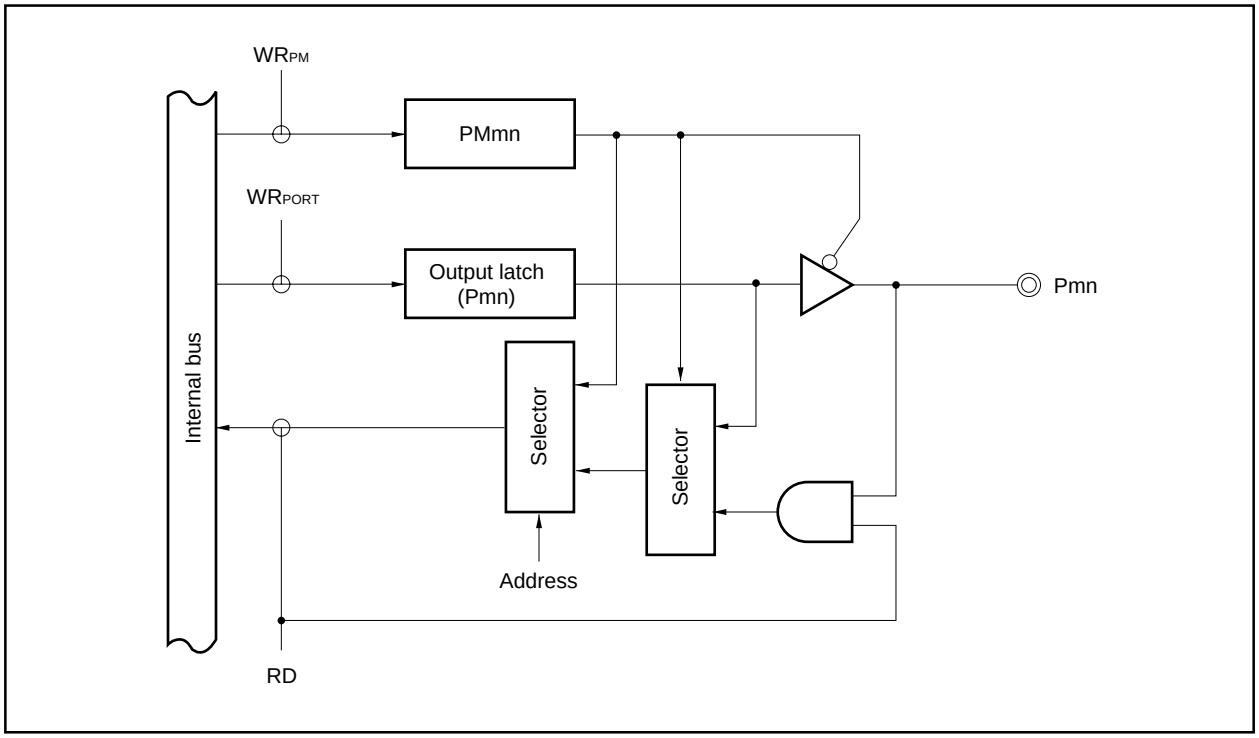


Figure 4-5. Block Diagram of Type C-1

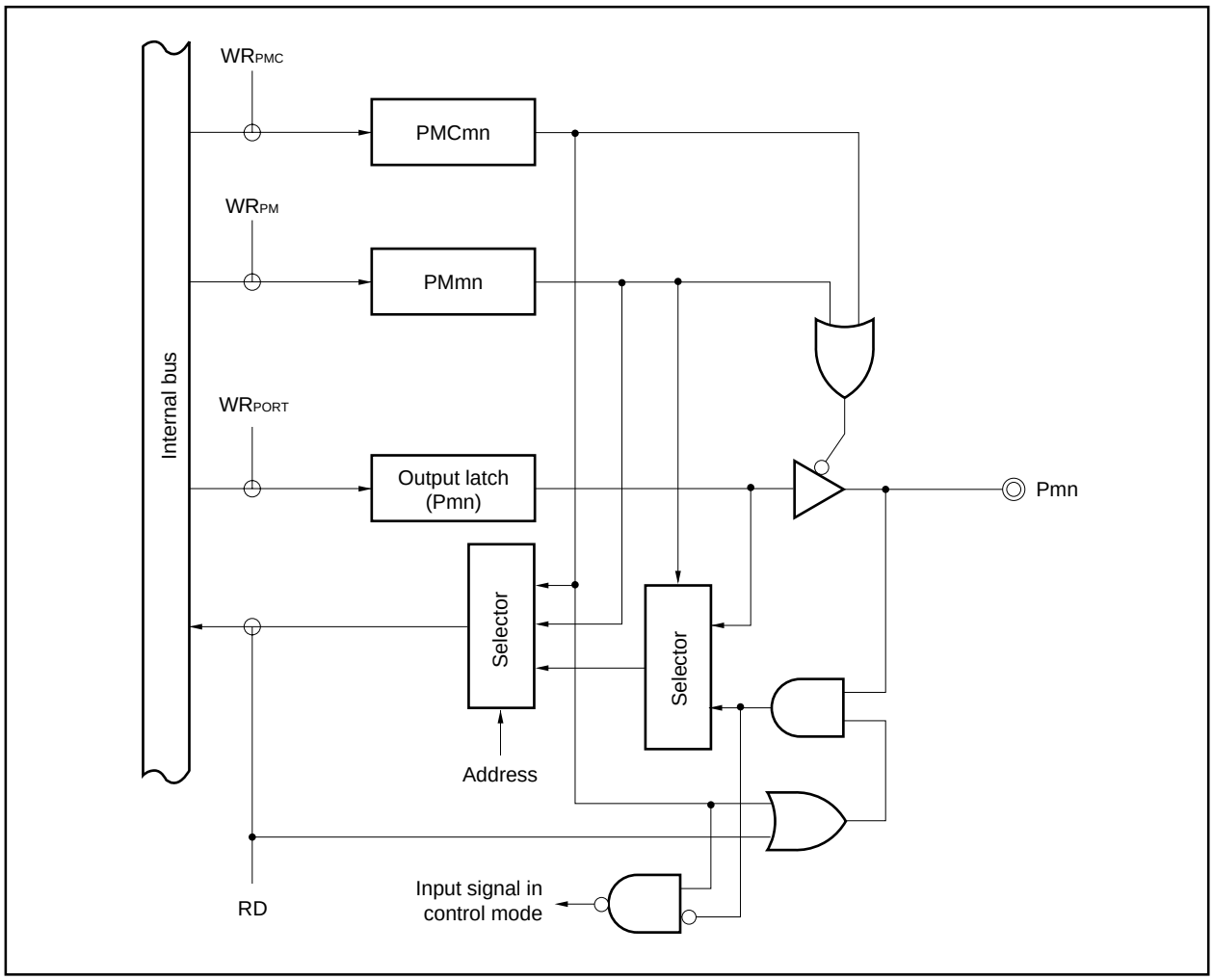


Figure 4-6. Block Diagram of Type C-2

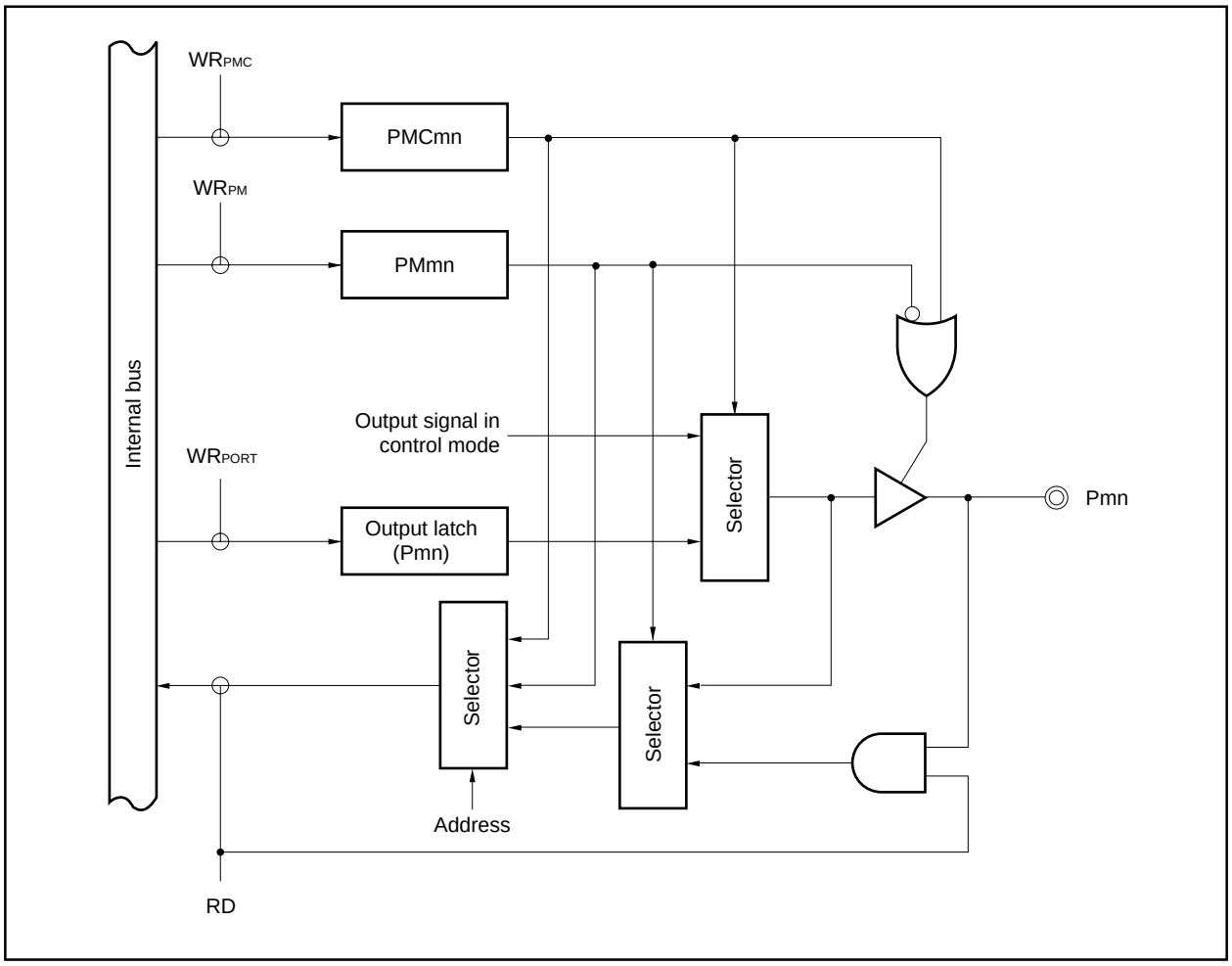


Figure 4-7. Block Diagram of Type C-3

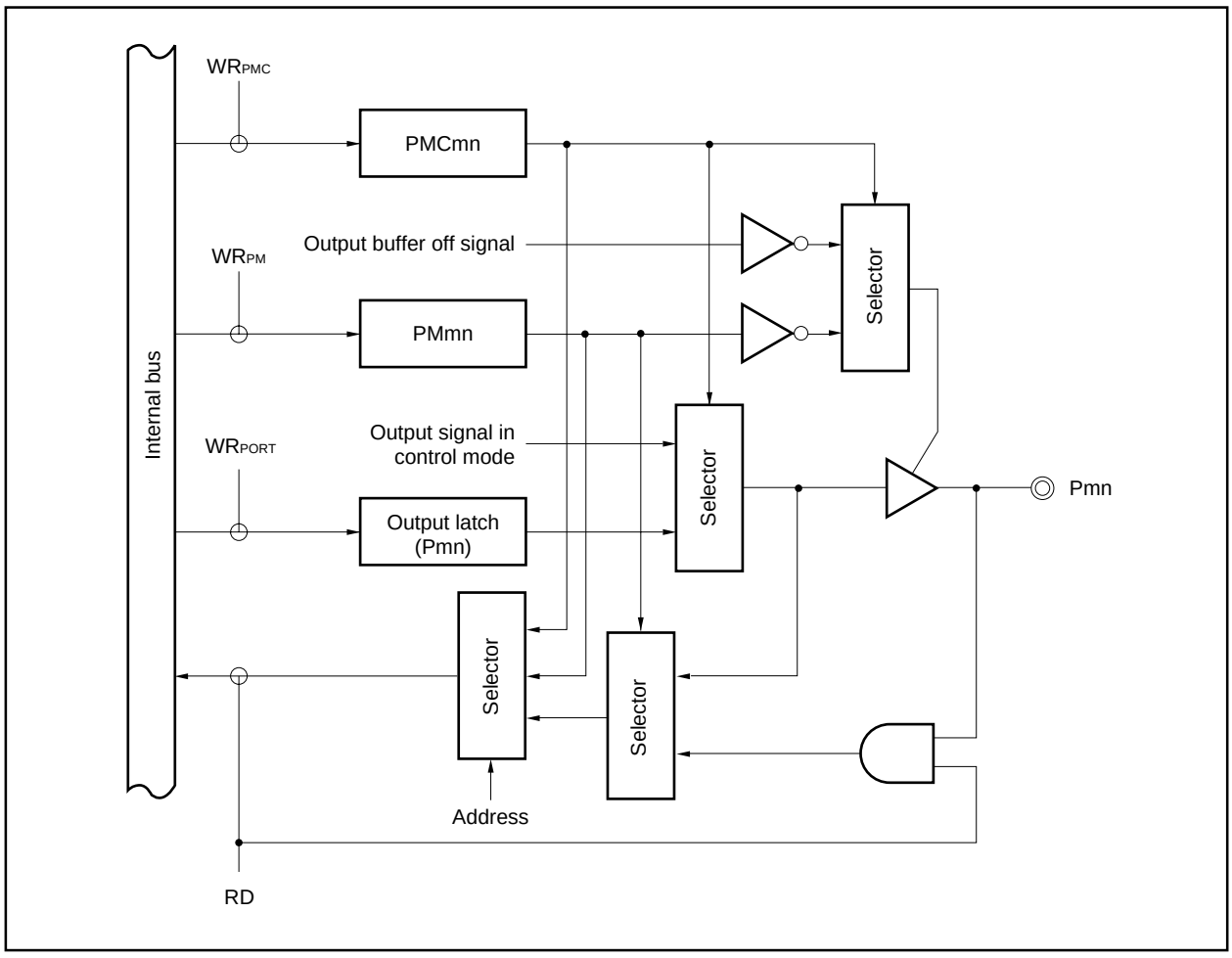


Figure 4-8. Block Diagram of Type C-4

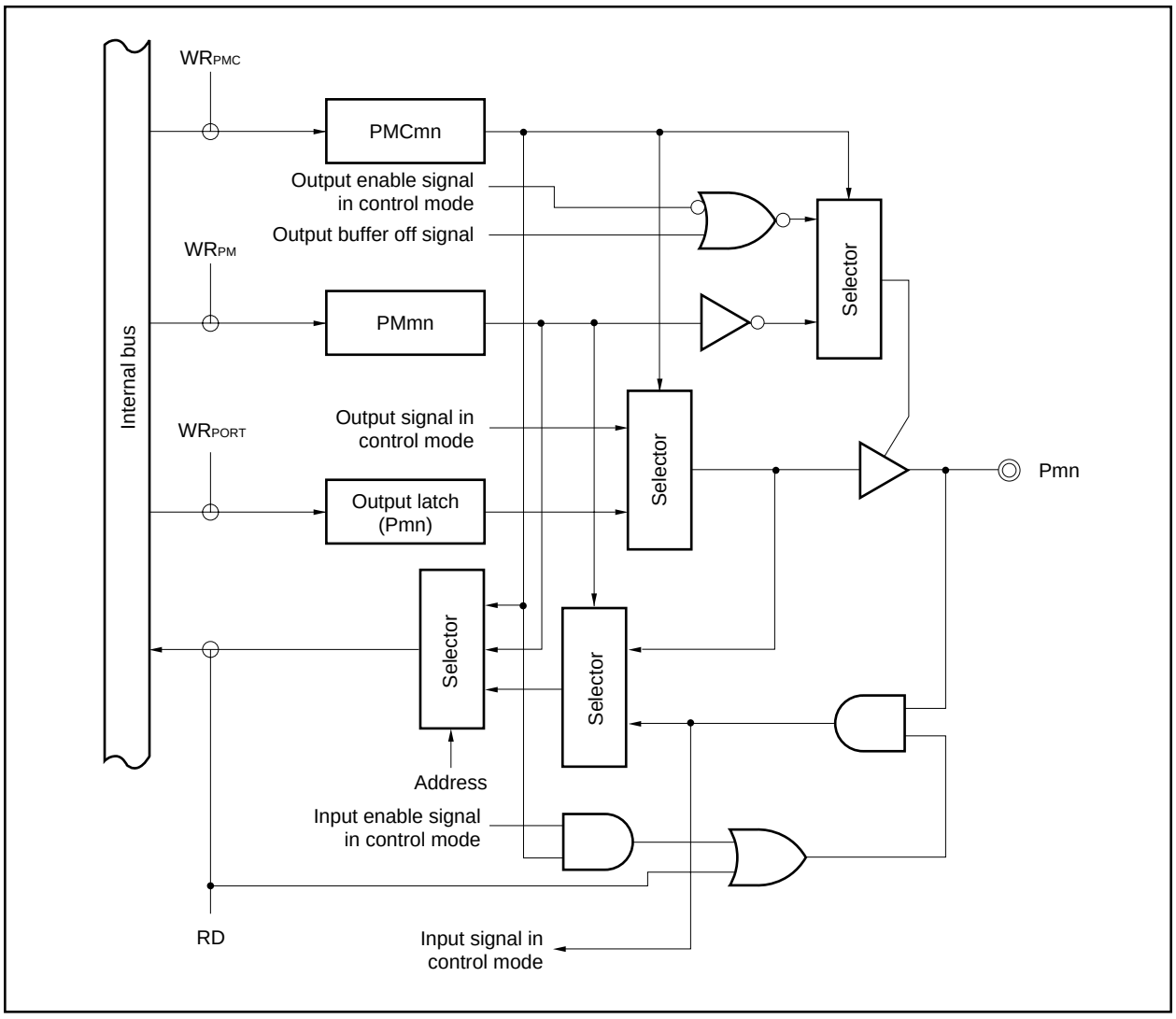


Figure 4-9. Block Diagram of Type D-1

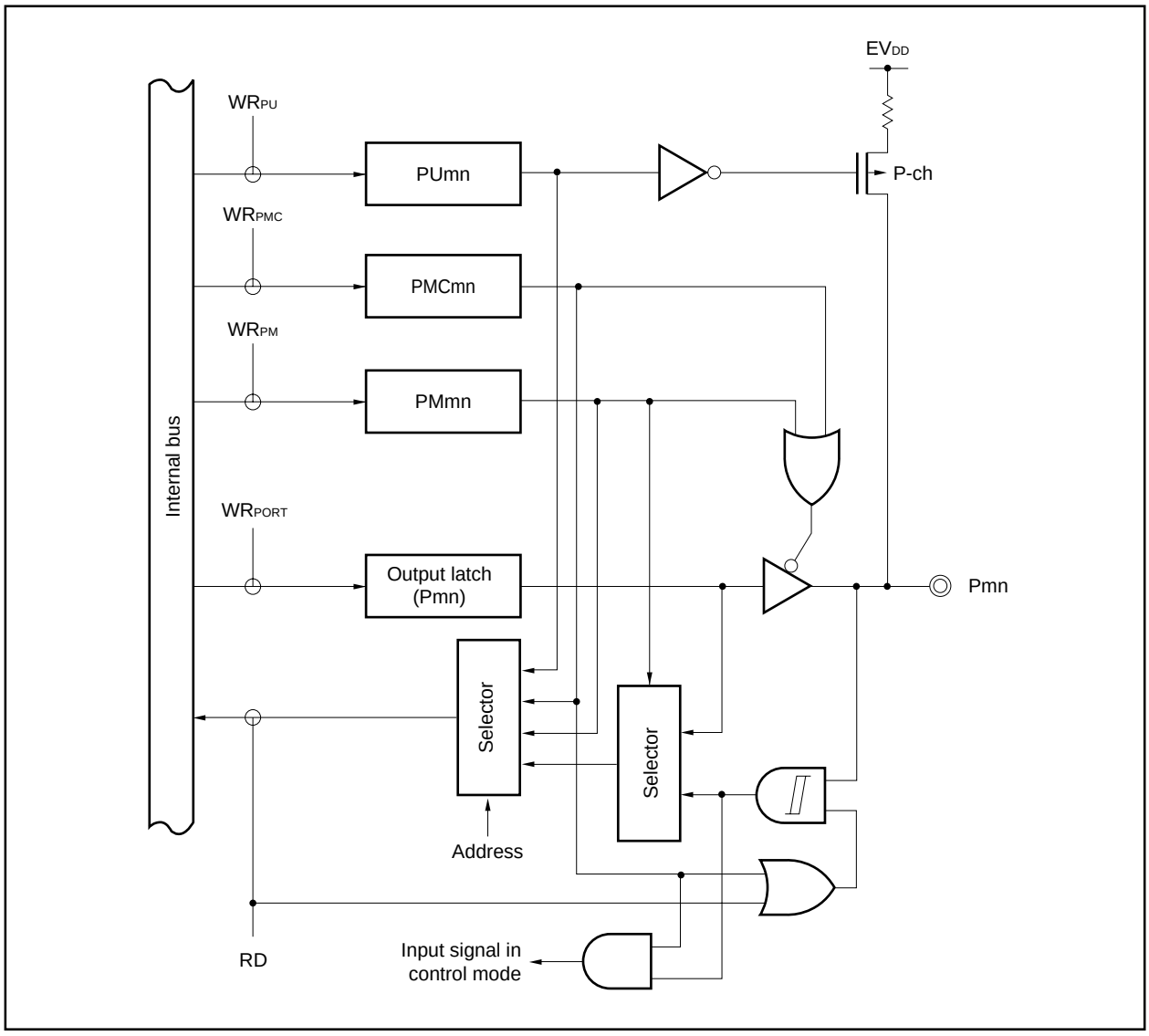


Figure 4-10. Block Diagram of Type D-2

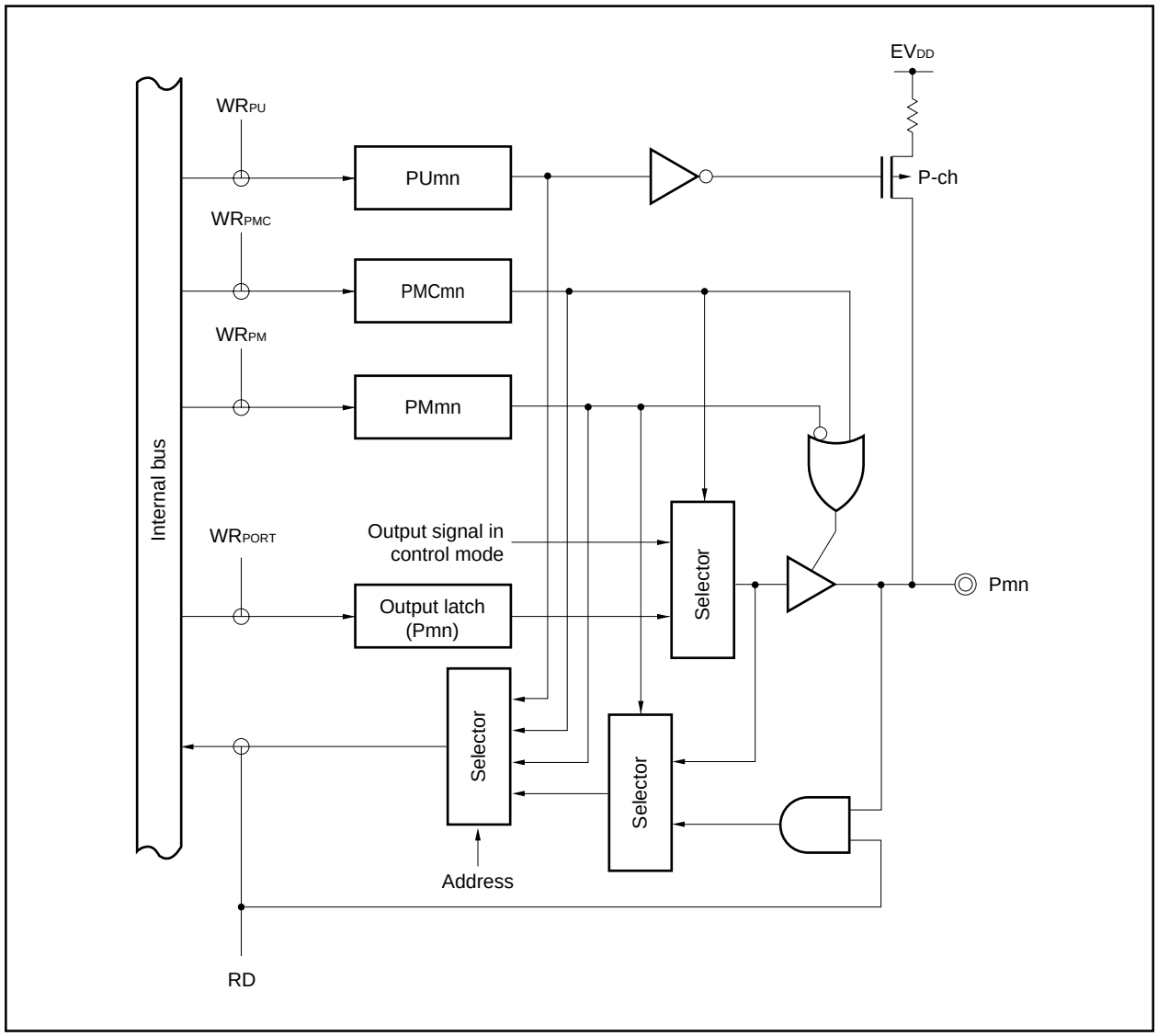


Figure 4-11. Block Diagram of Type E-1

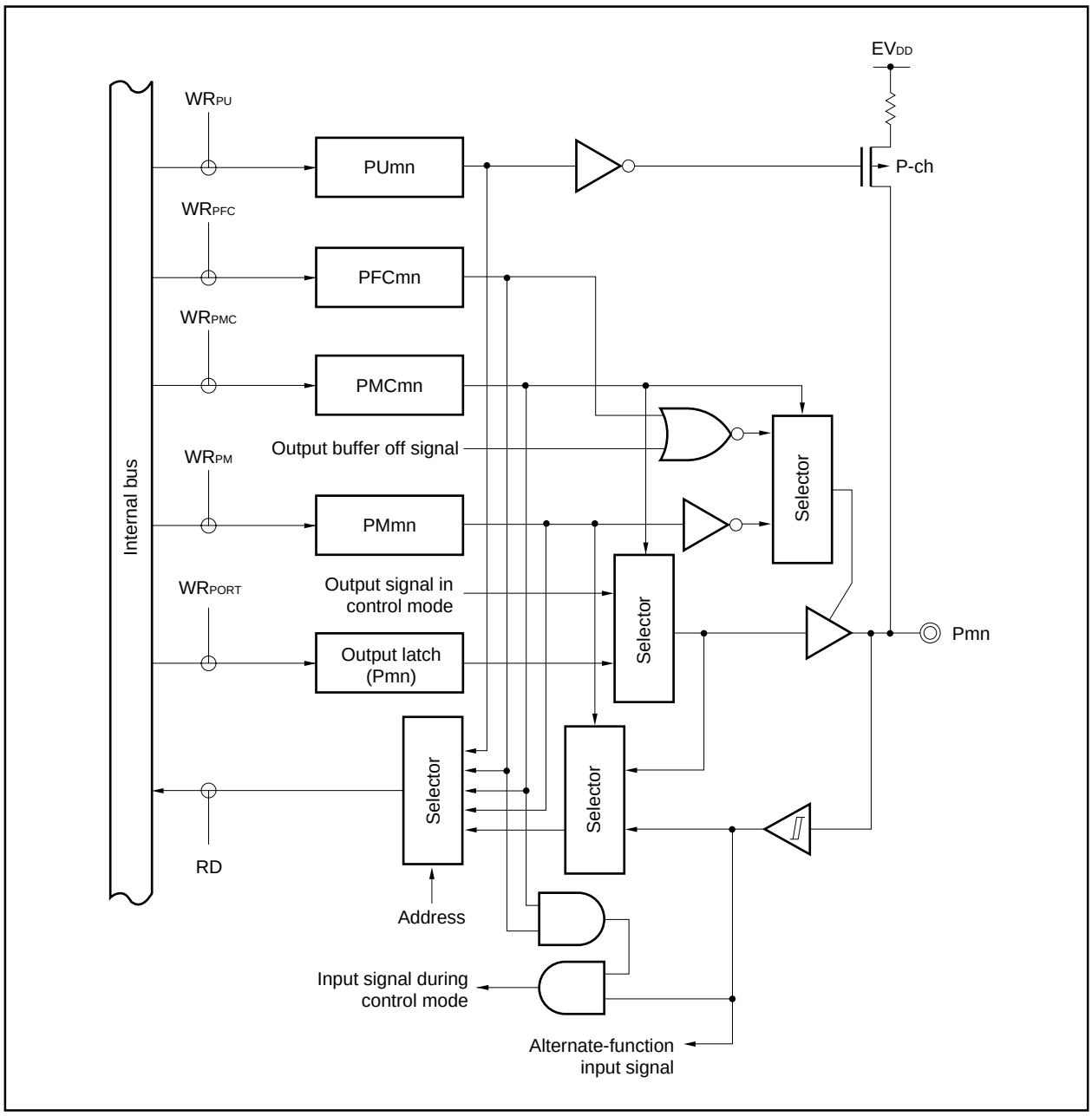


Figure 4-12. Block Diagram of Type E-2

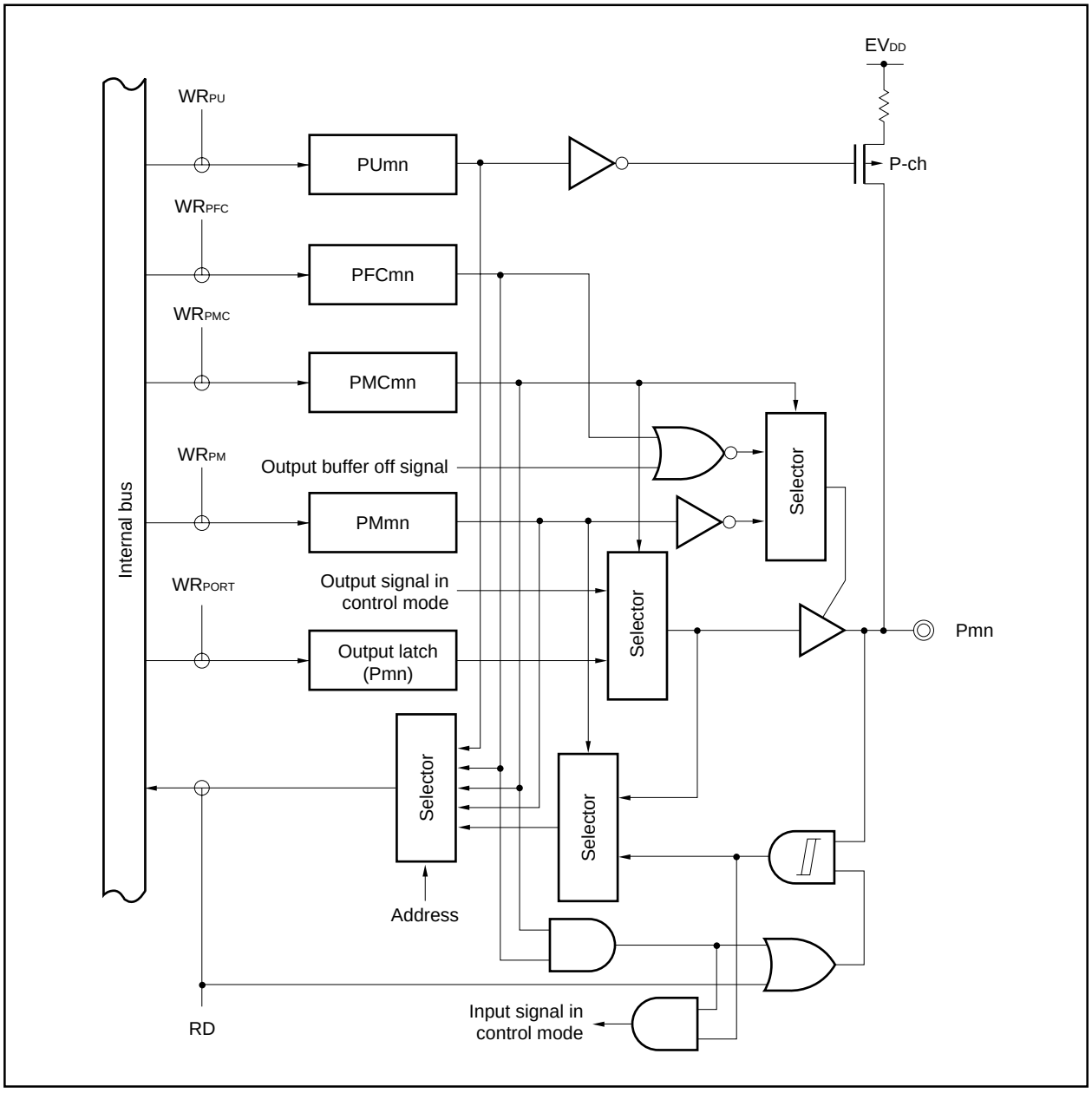


Figure 4-13. Block Diagram of Type E-3

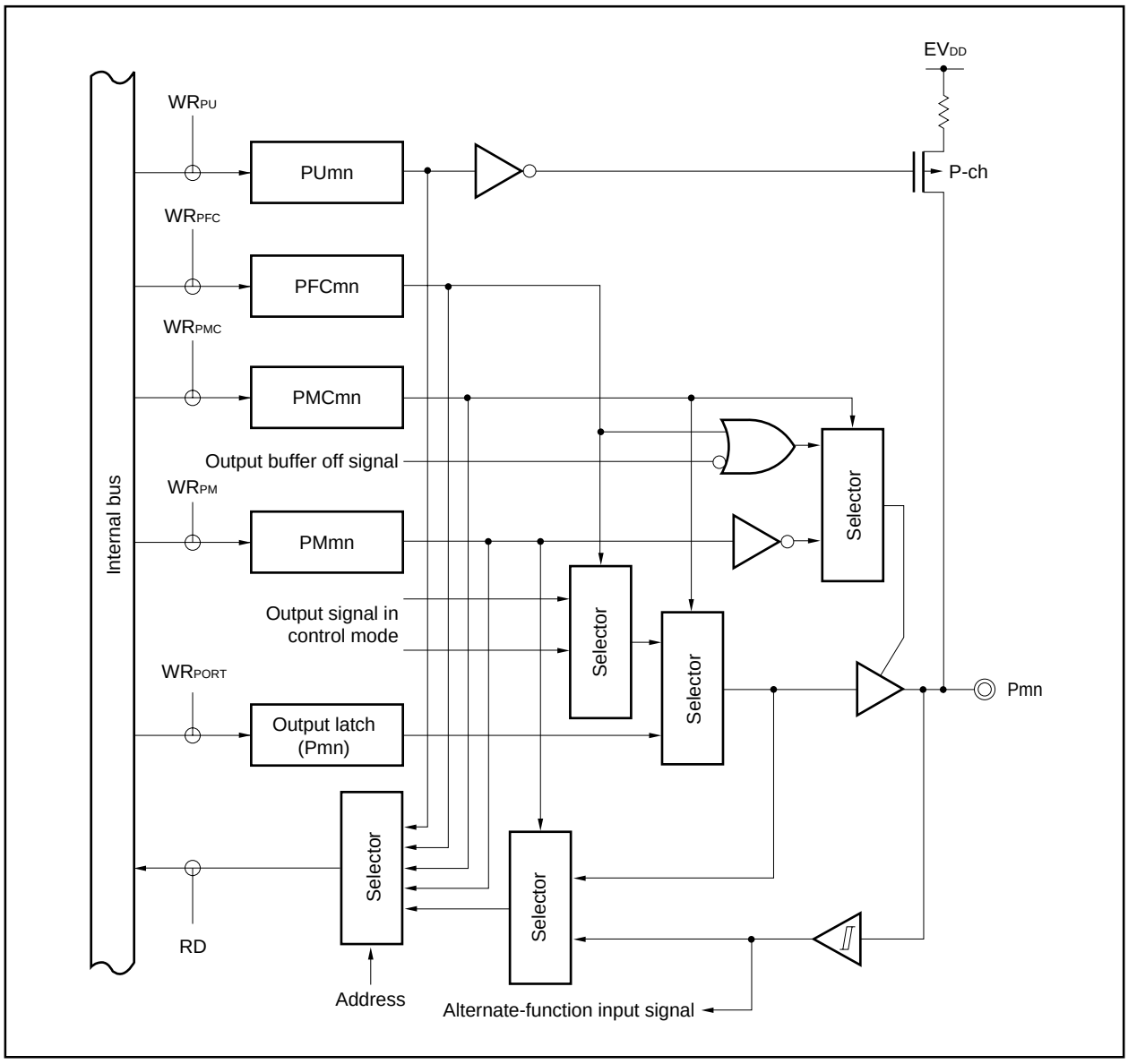


Figure 4-14. Block Diagram of Type E-4

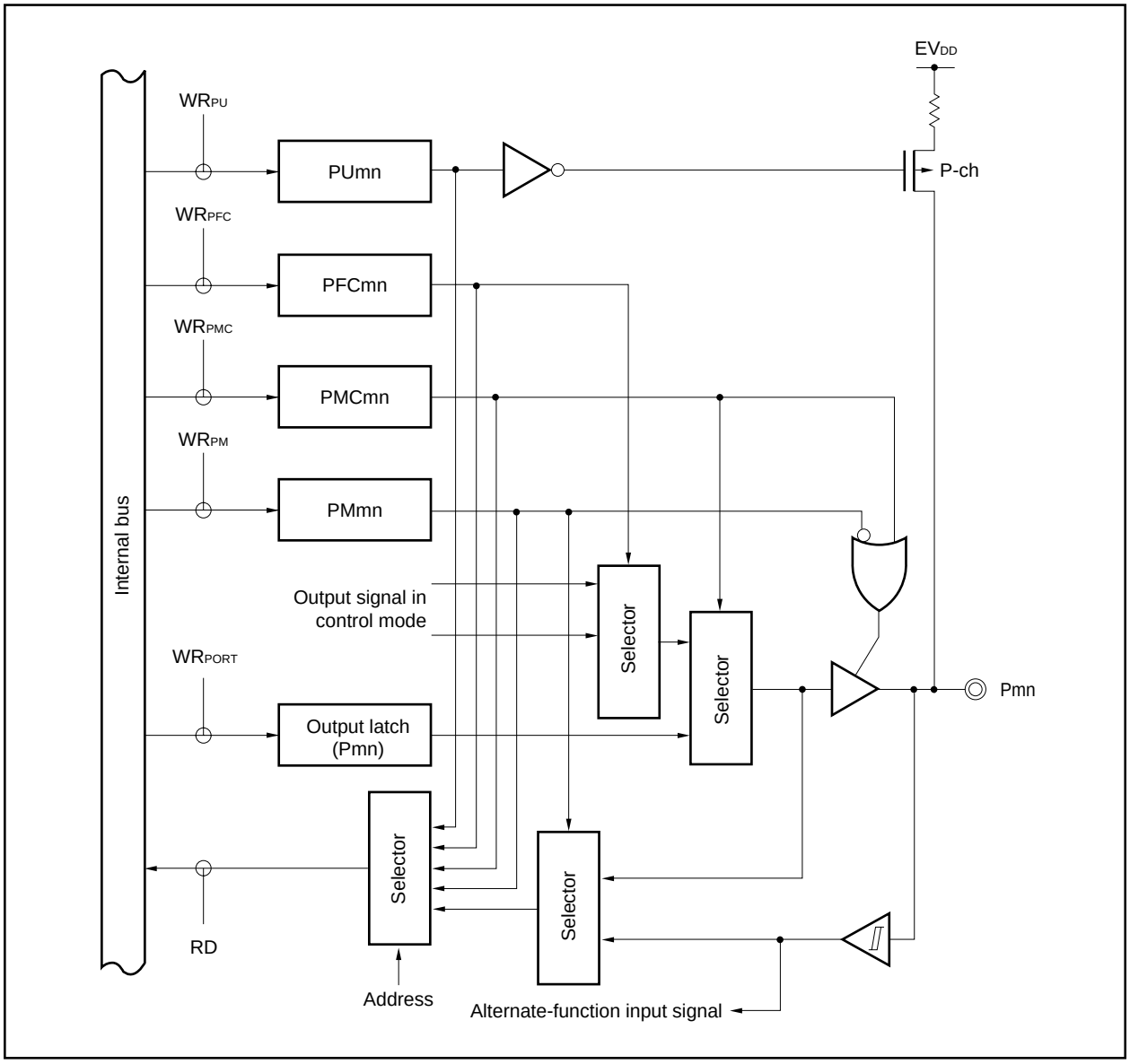


Figure 4-15. Block Diagram of Type E-5

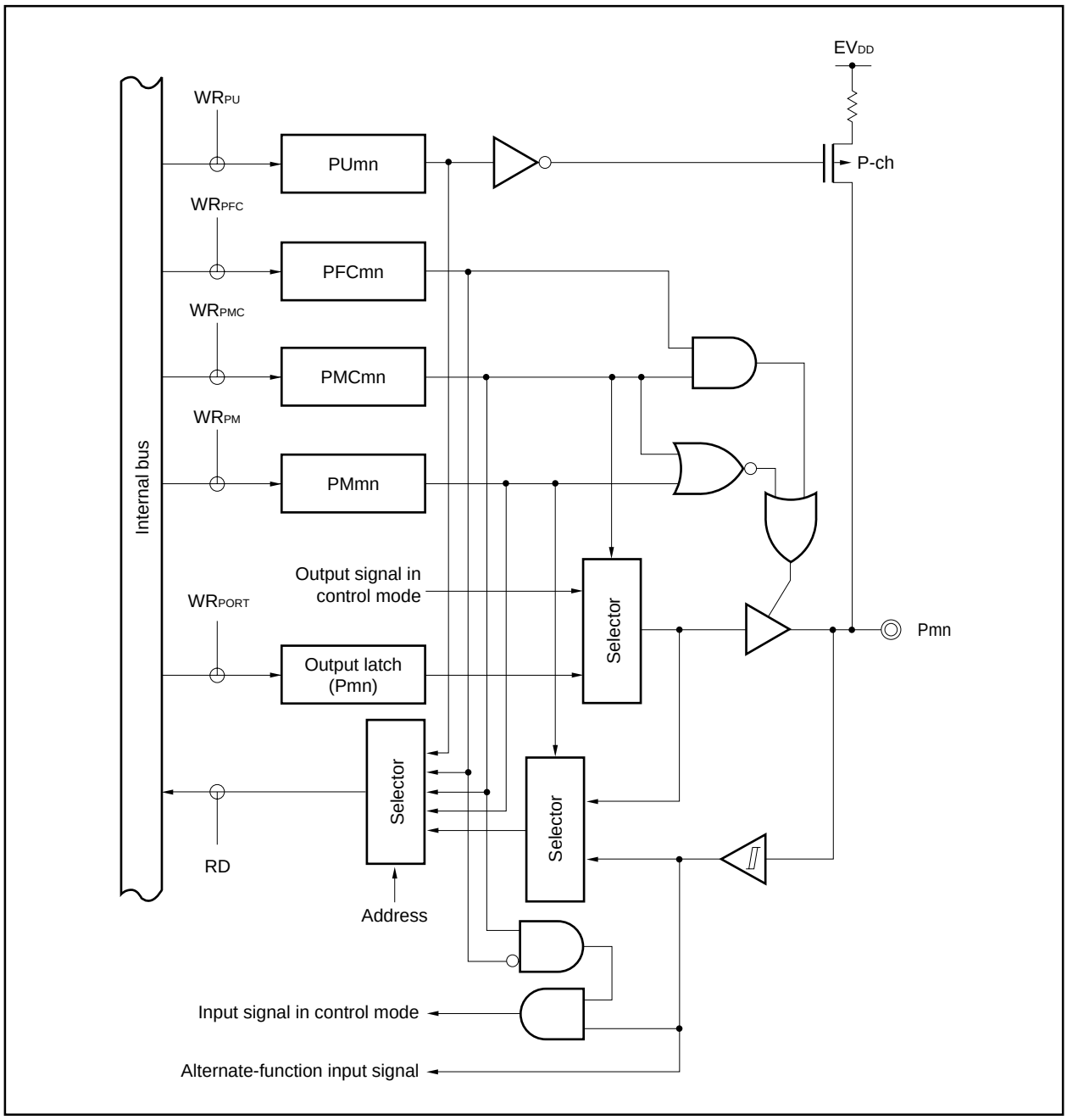


Figure 4-16. Block Diagram of Type E-6

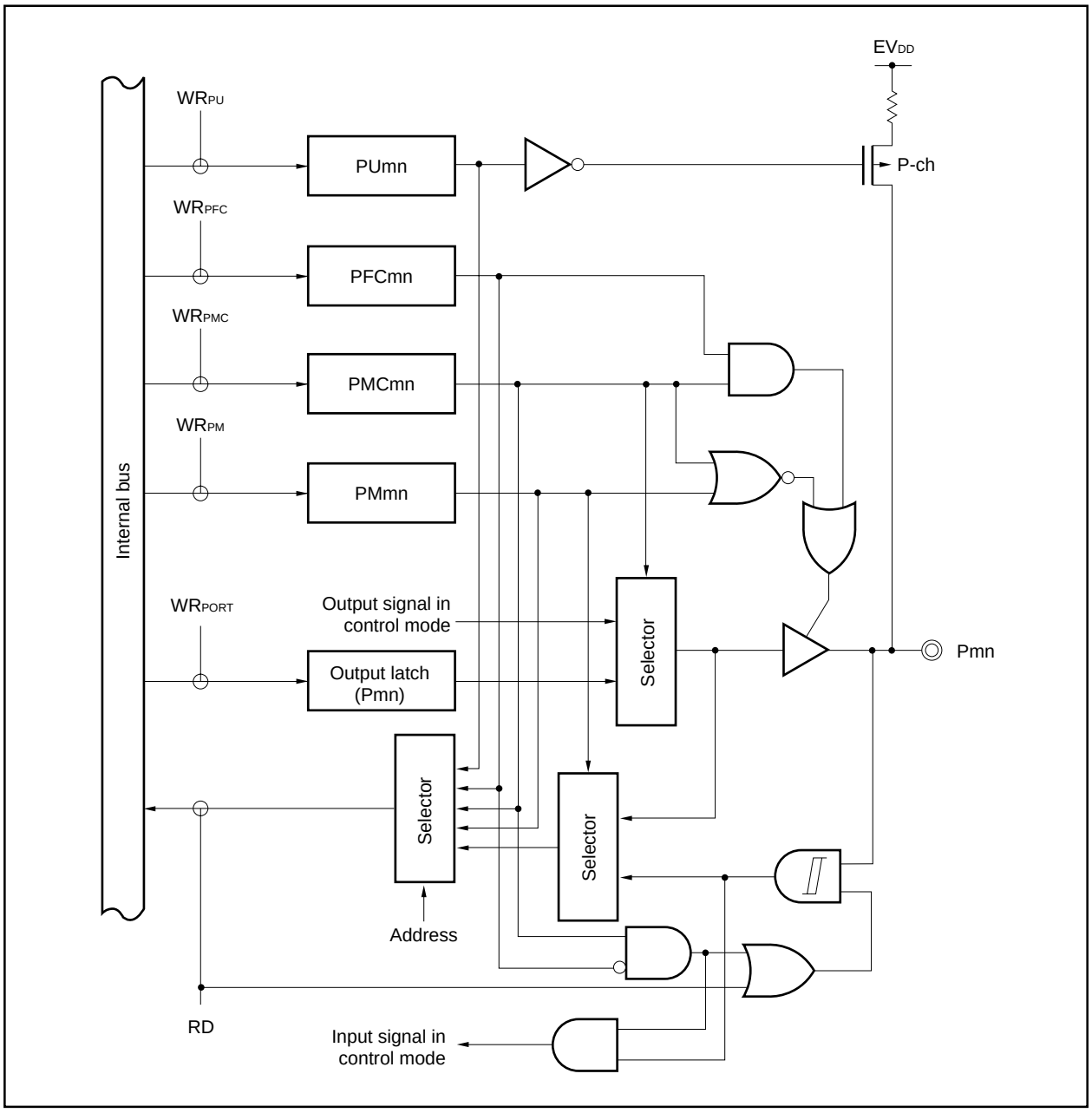


Figure 4-17. Block Diagram of Type F-1

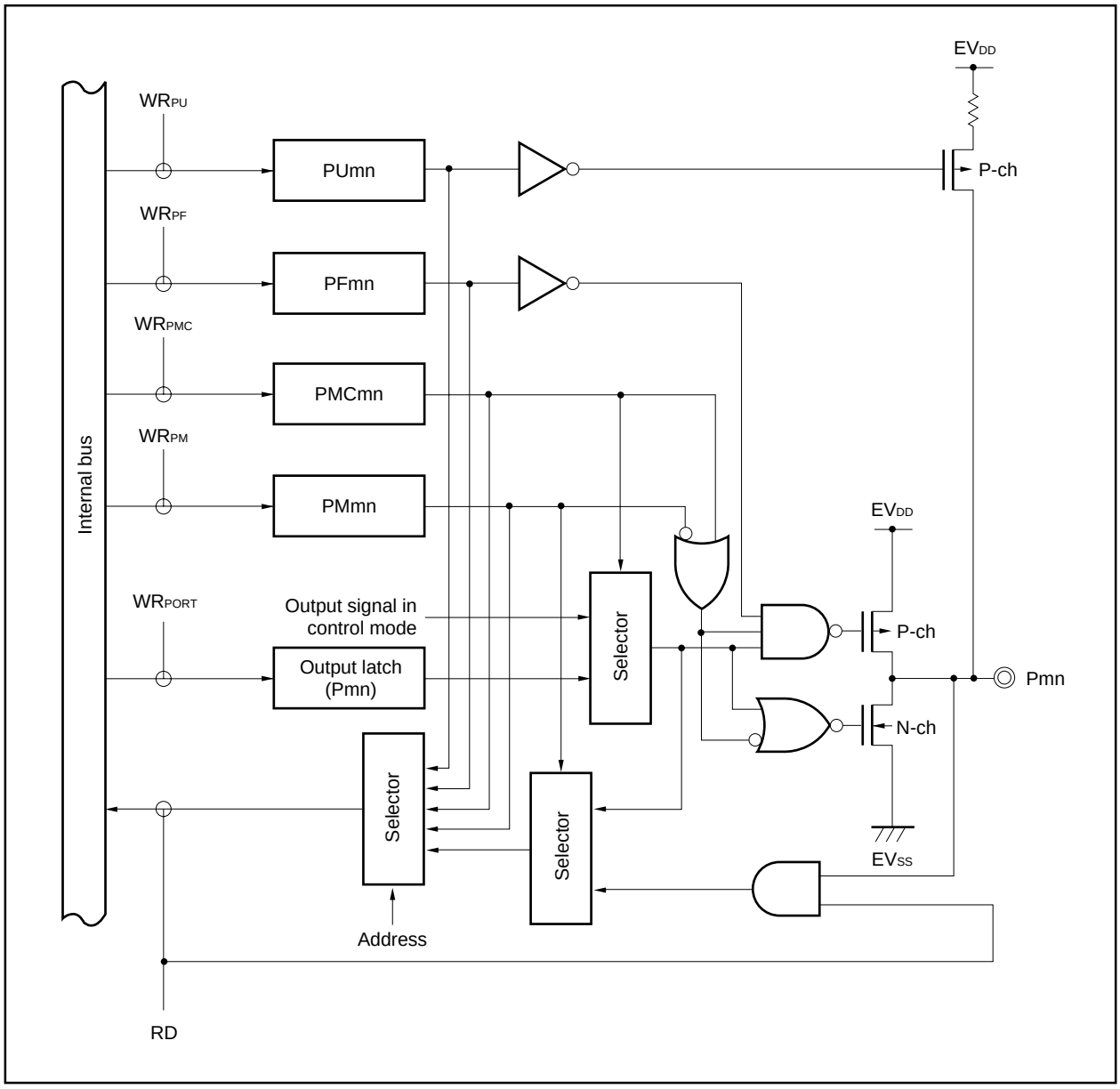


Figure 4-18. Block Diagram of Type F-2

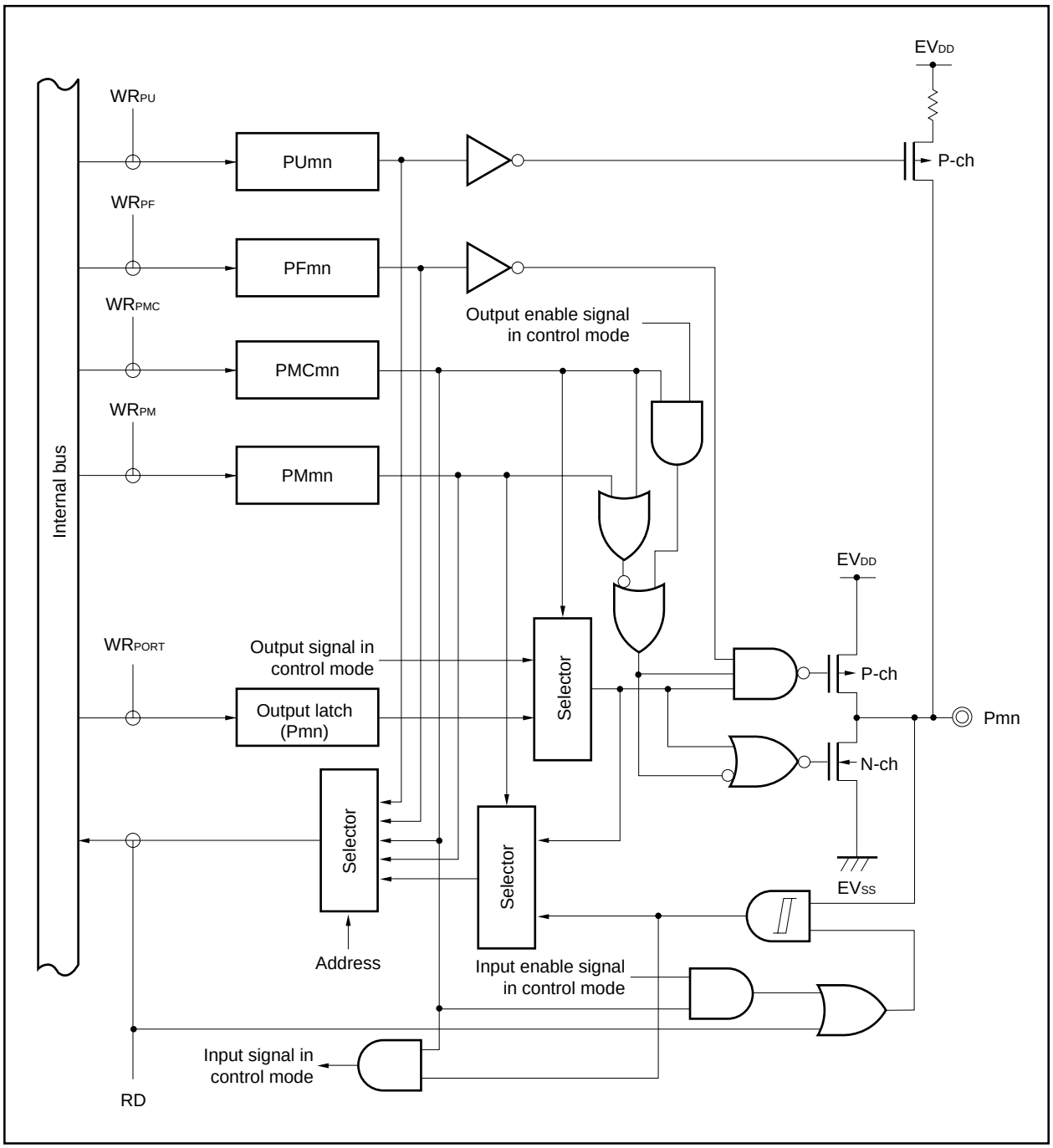


Figure 4-19. Block Diagram of Type G-1

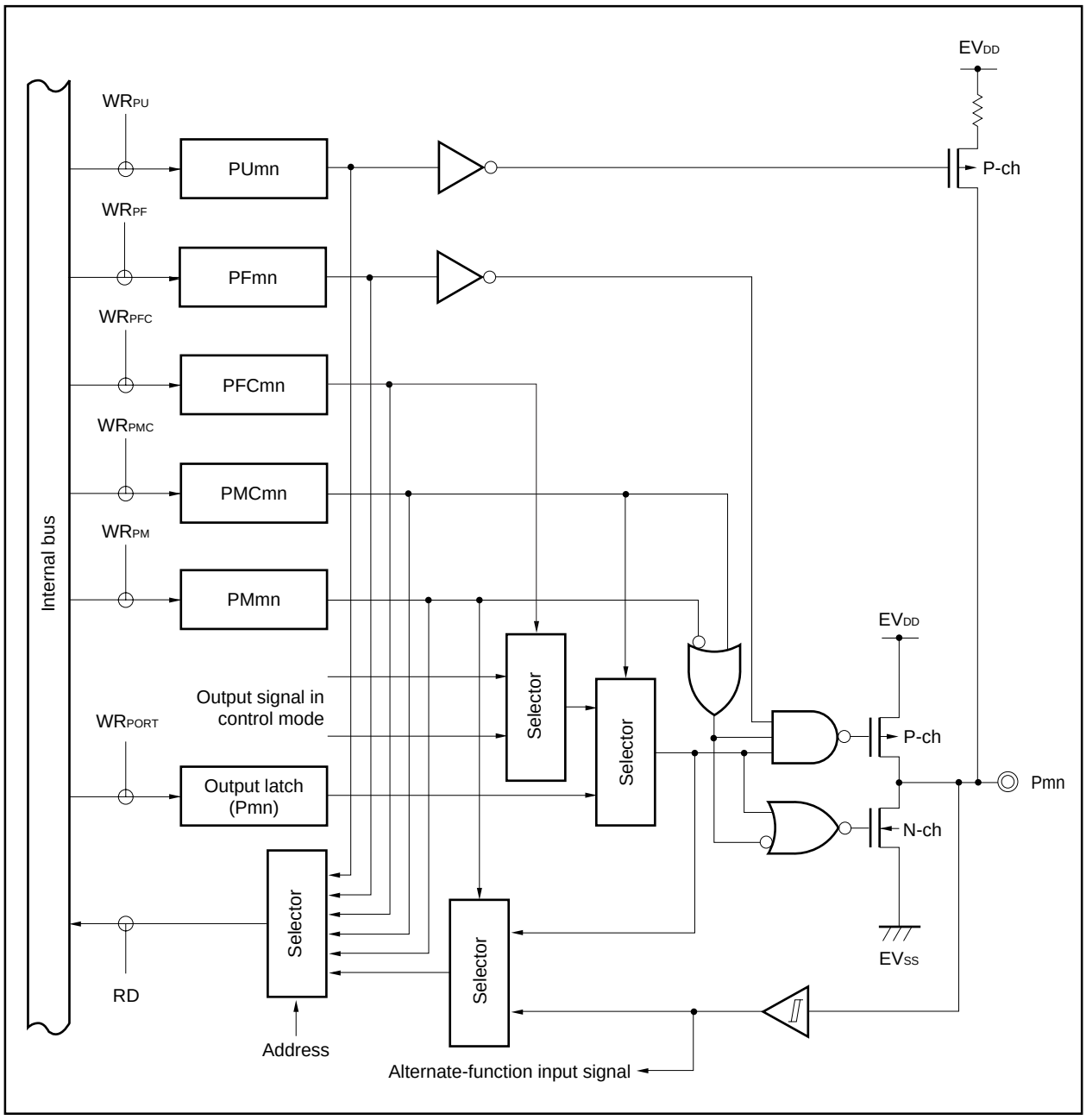


Figure 4-20. Block Diagram of Type G-2

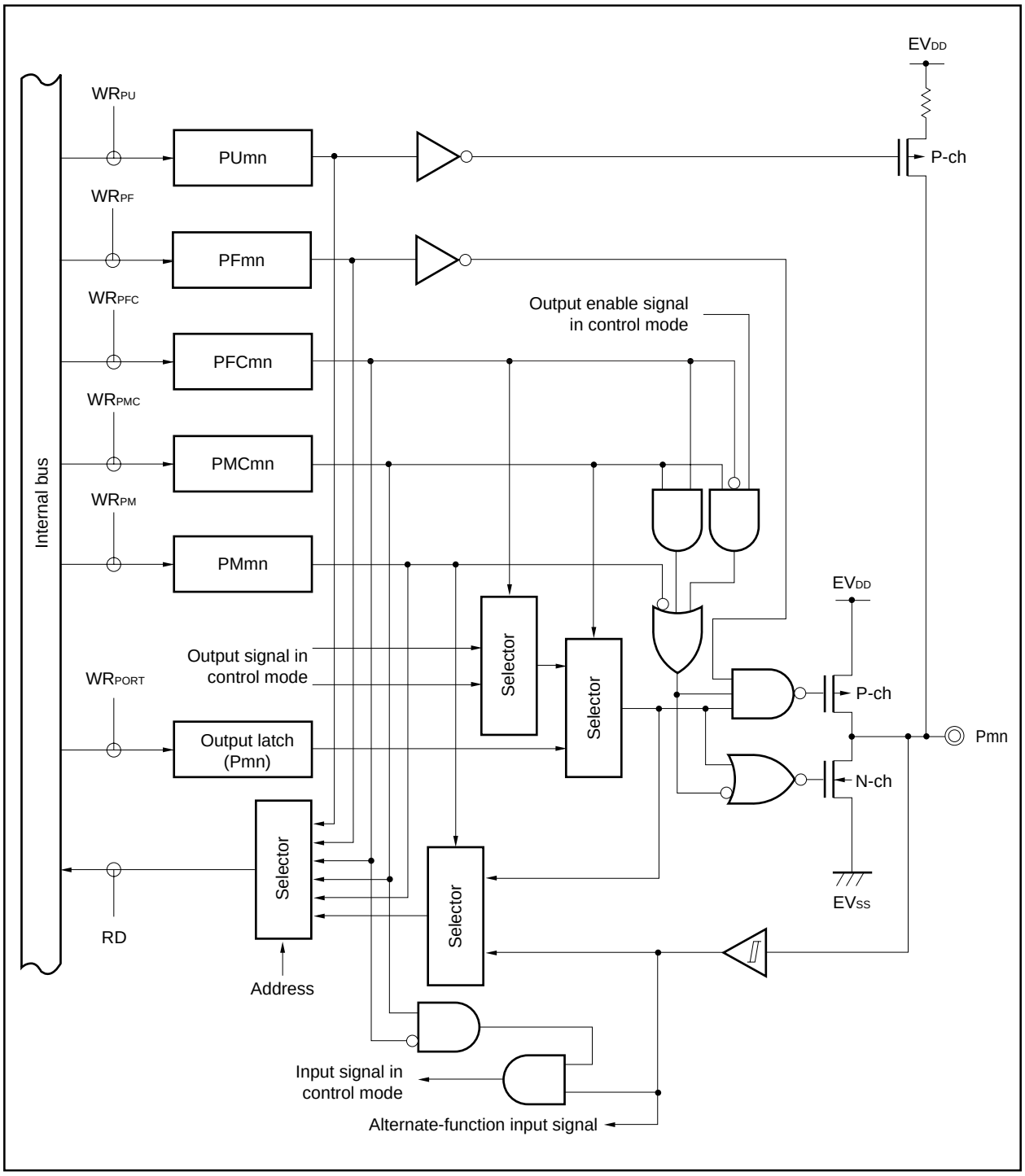


Figure 4-21. Block Diagram of Type G-3

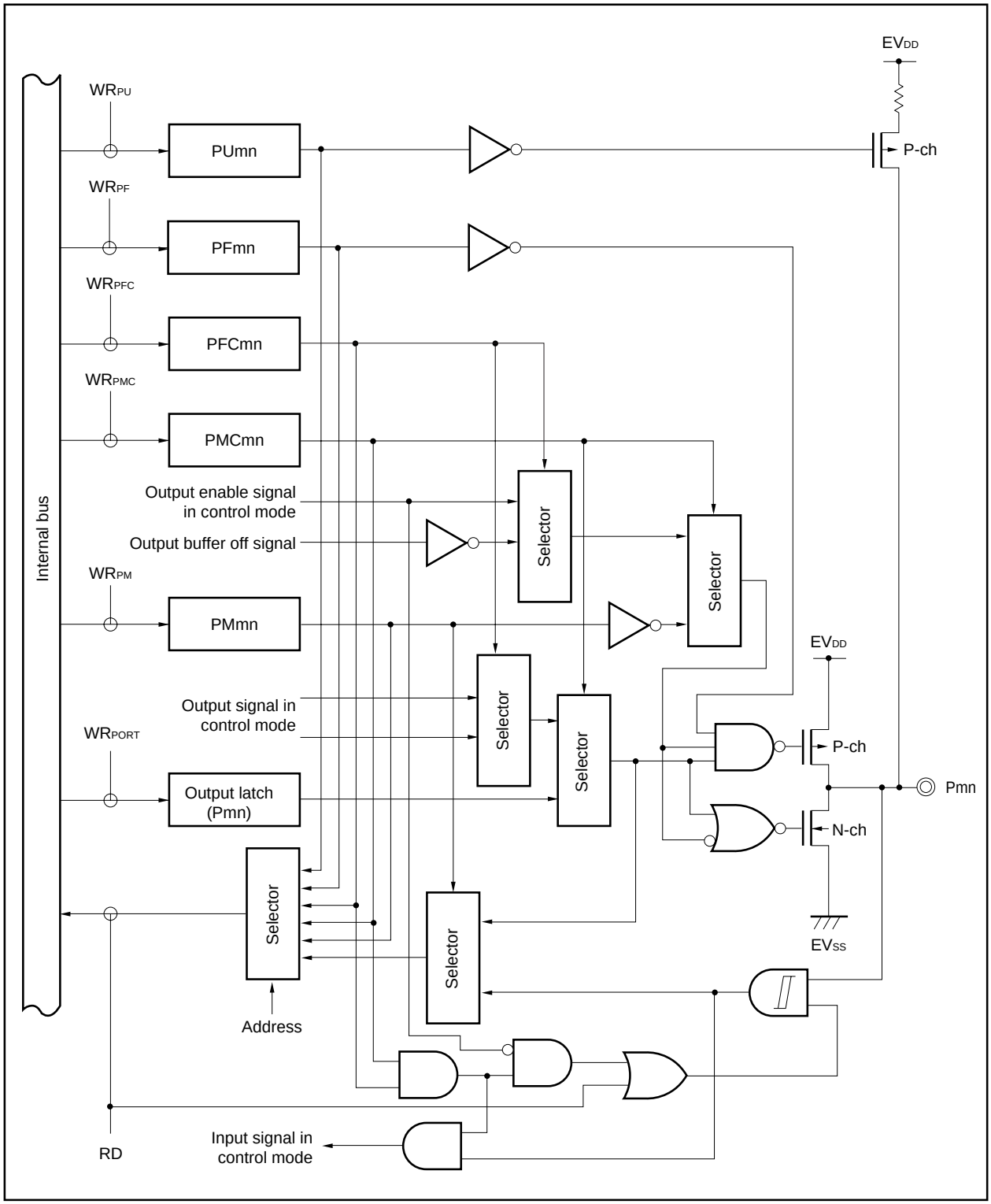


Figure 4-22. Block Diagram of Type G-4

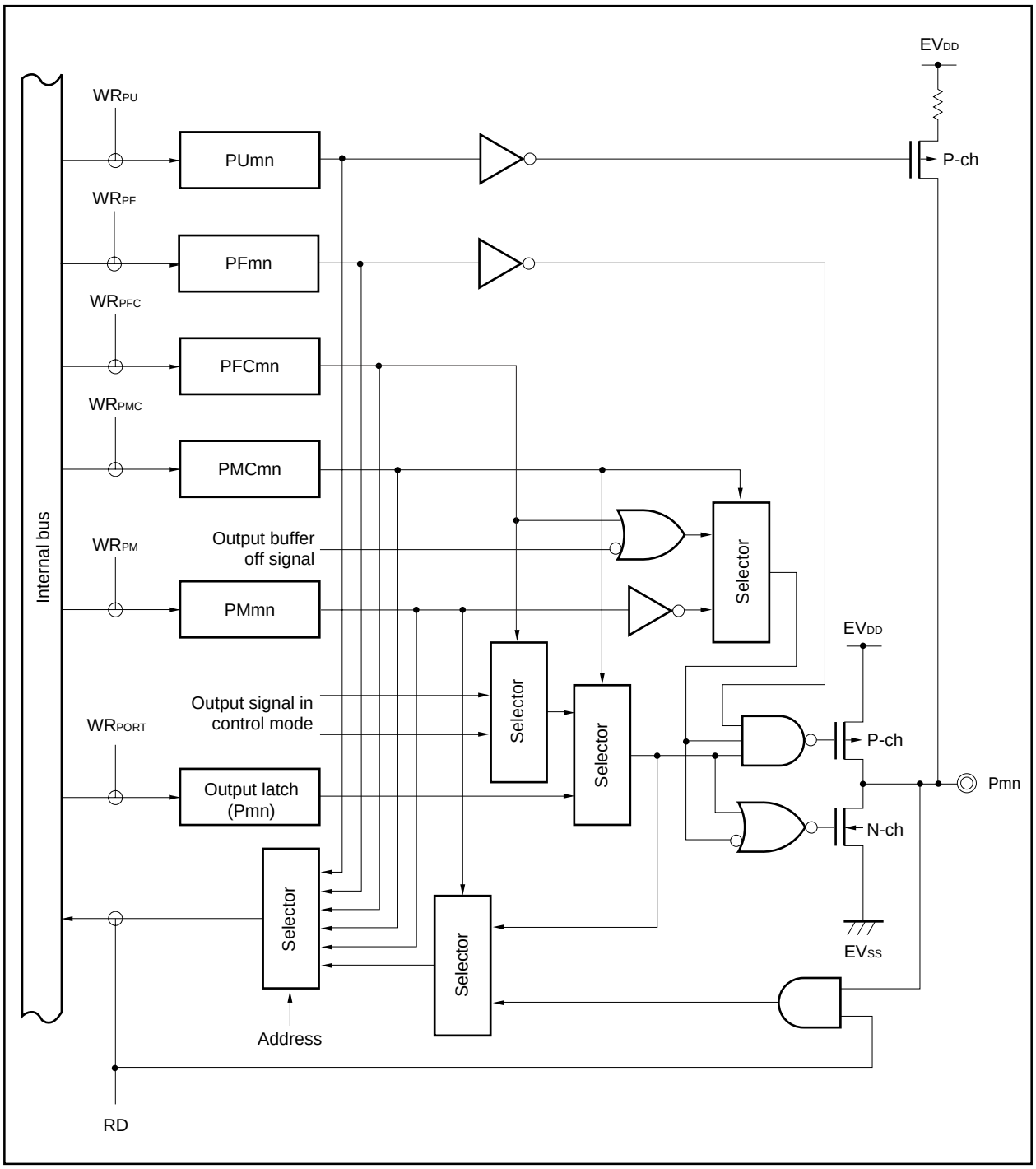


Figure 4-23. Block Diagram of Type G-5

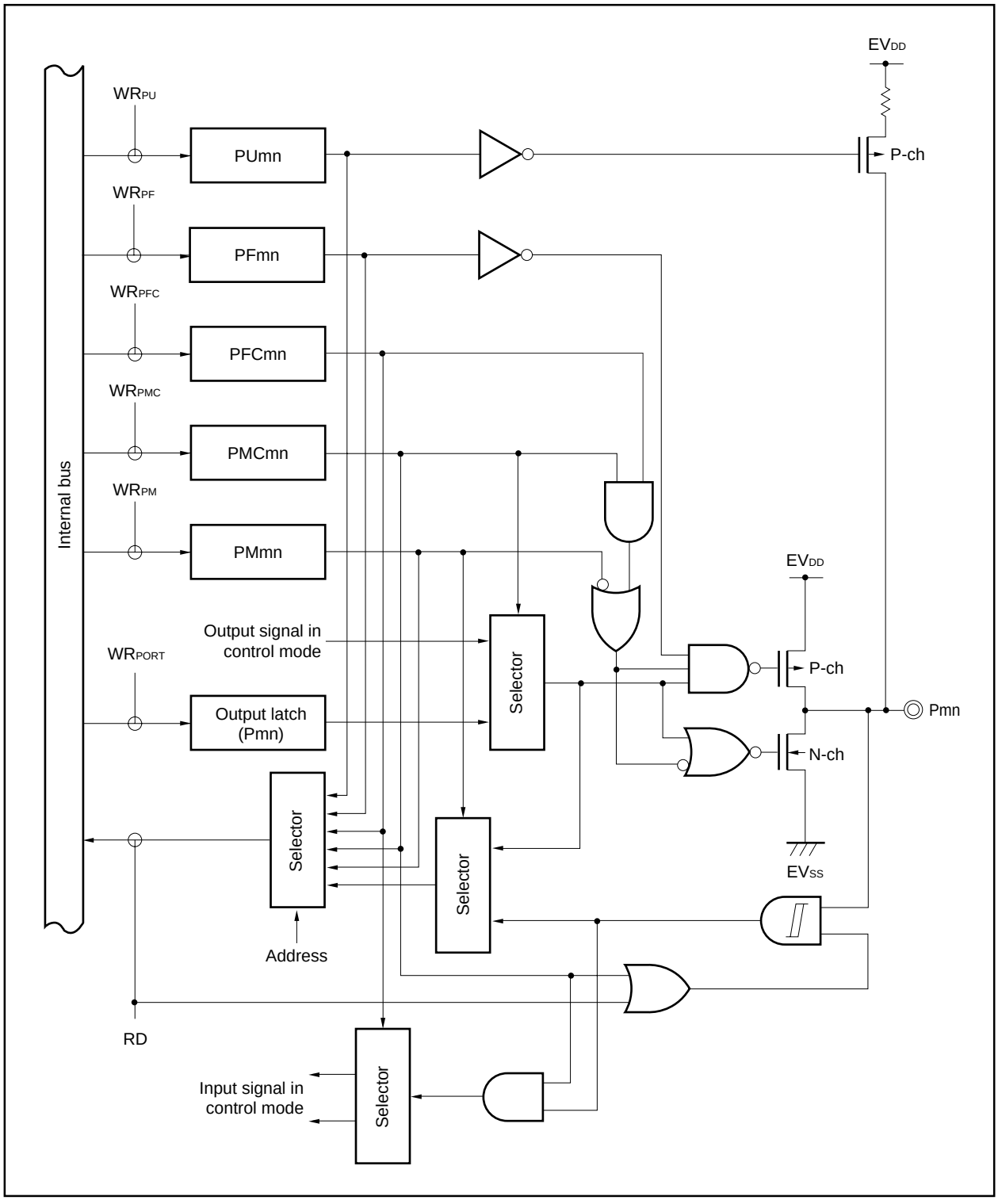


Figure 4-24. Block Diagram of Type G-6

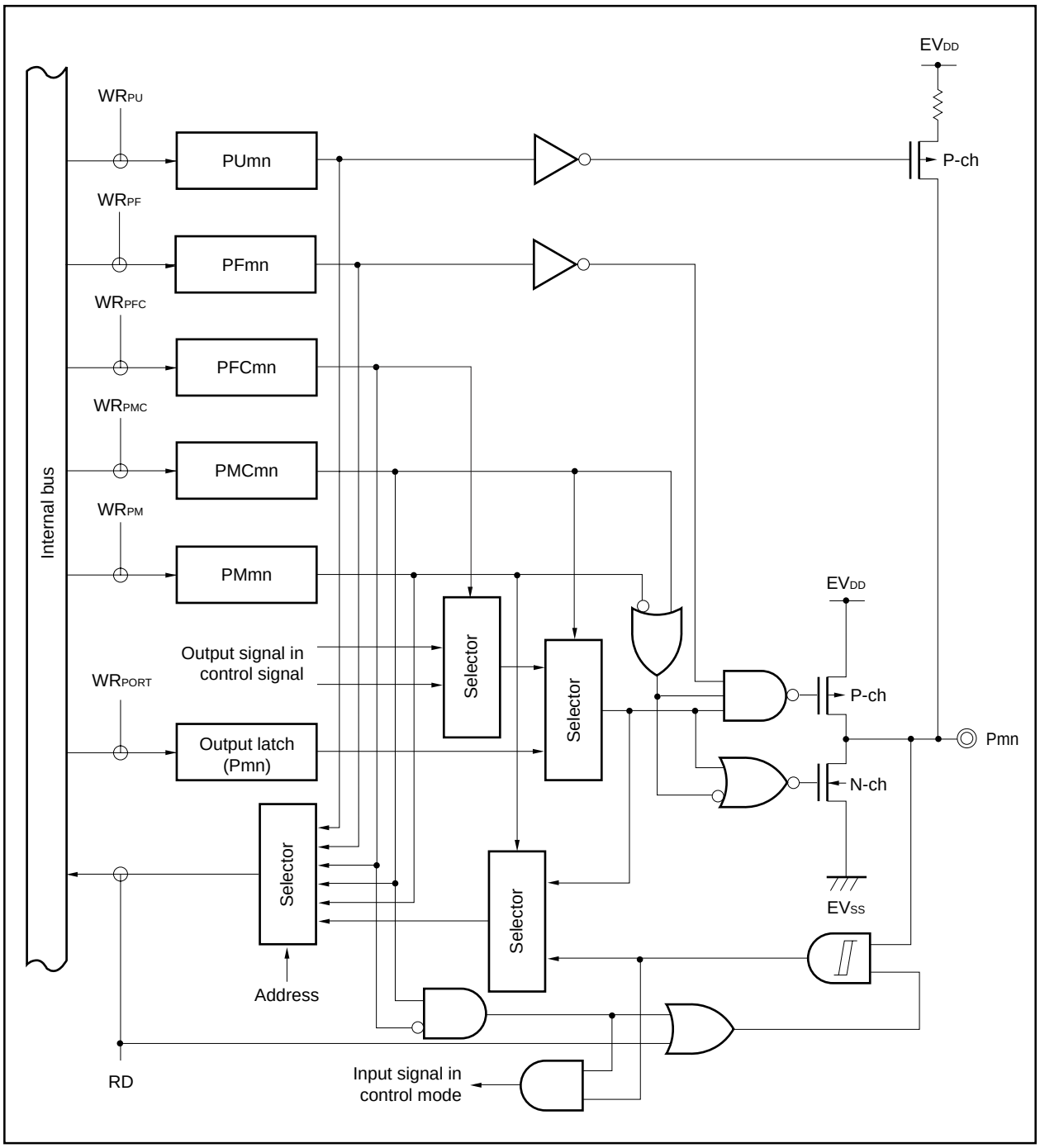
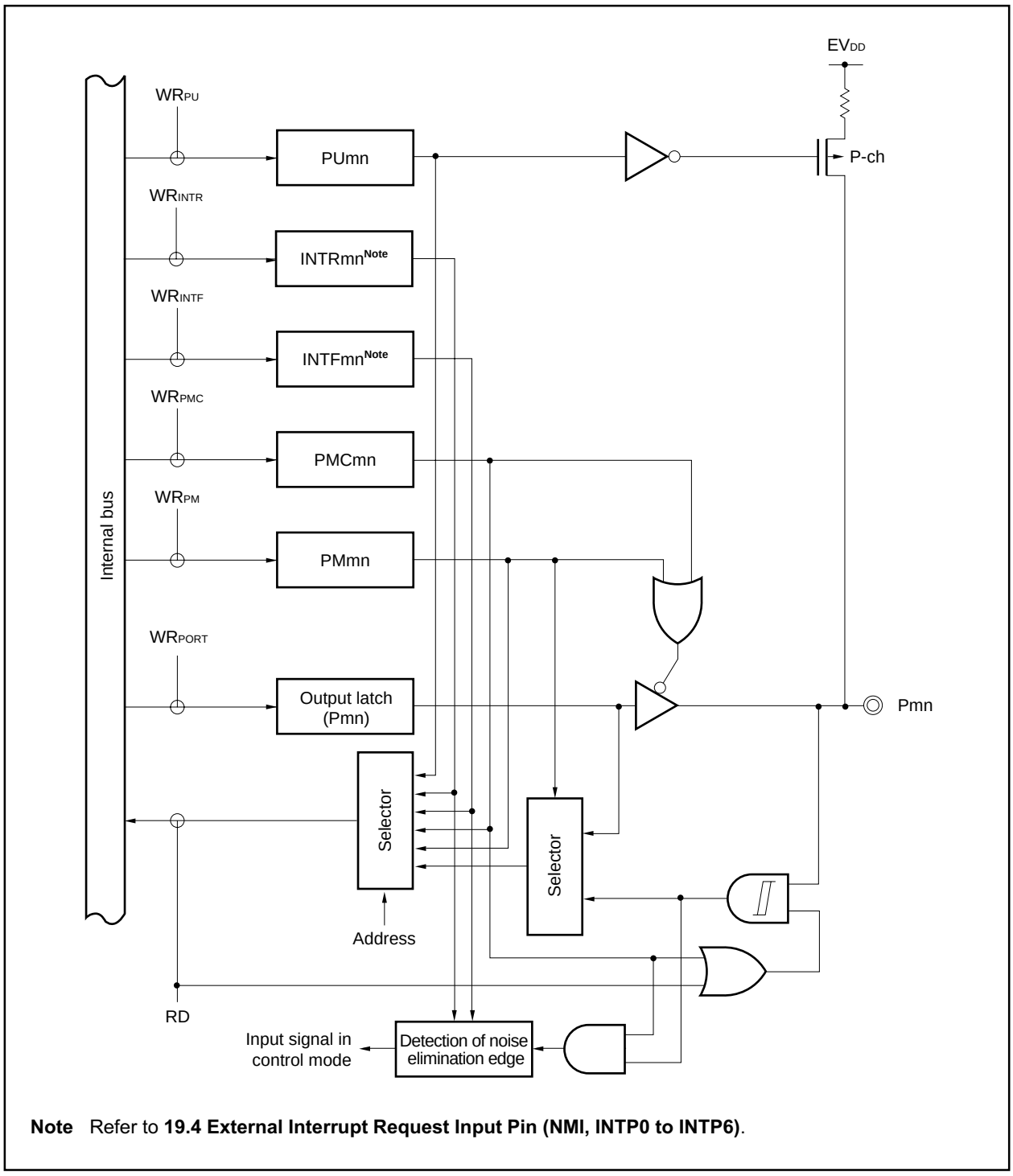
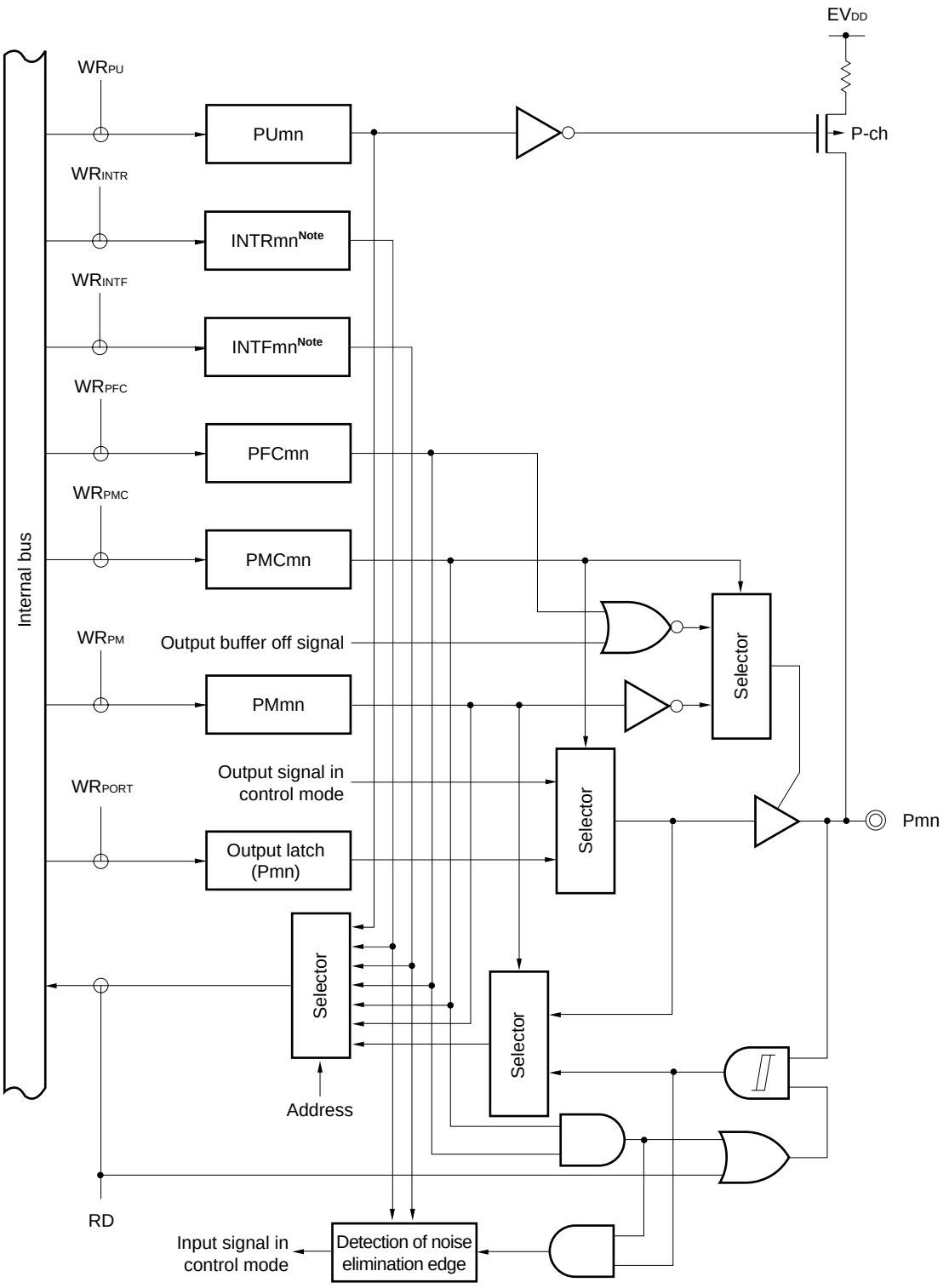


Figure 4-25. Block Diagram of Type H-1



Note Refer to **19.4 External Interrupt Request Input Pin (NMI, INTP0 to INTP6)**.

Figure 4-26. Block Diagram of Type H-2



Note Refer to **19.4 External Interrupt Request Input Pins (NMI, INTP0 to INTP6)**.

Figure 4-27. Block Diagram of Type J

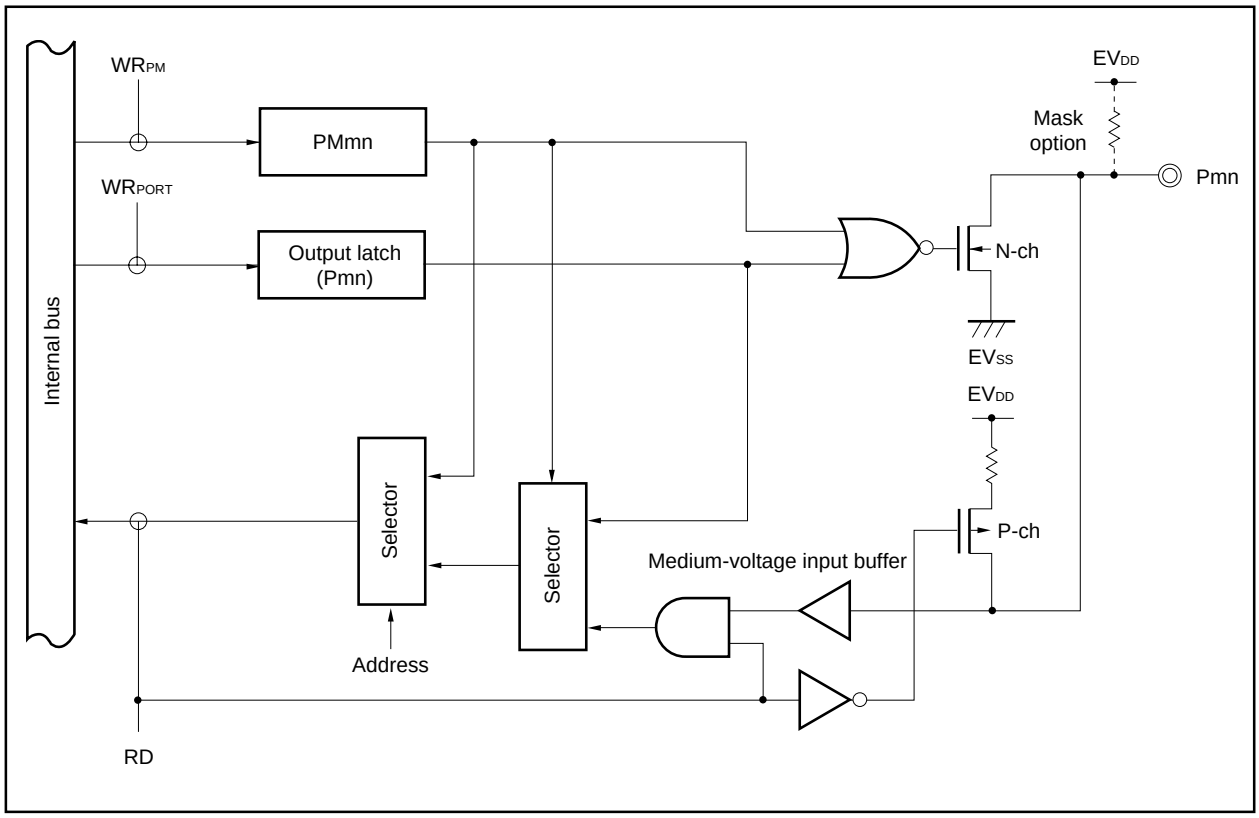
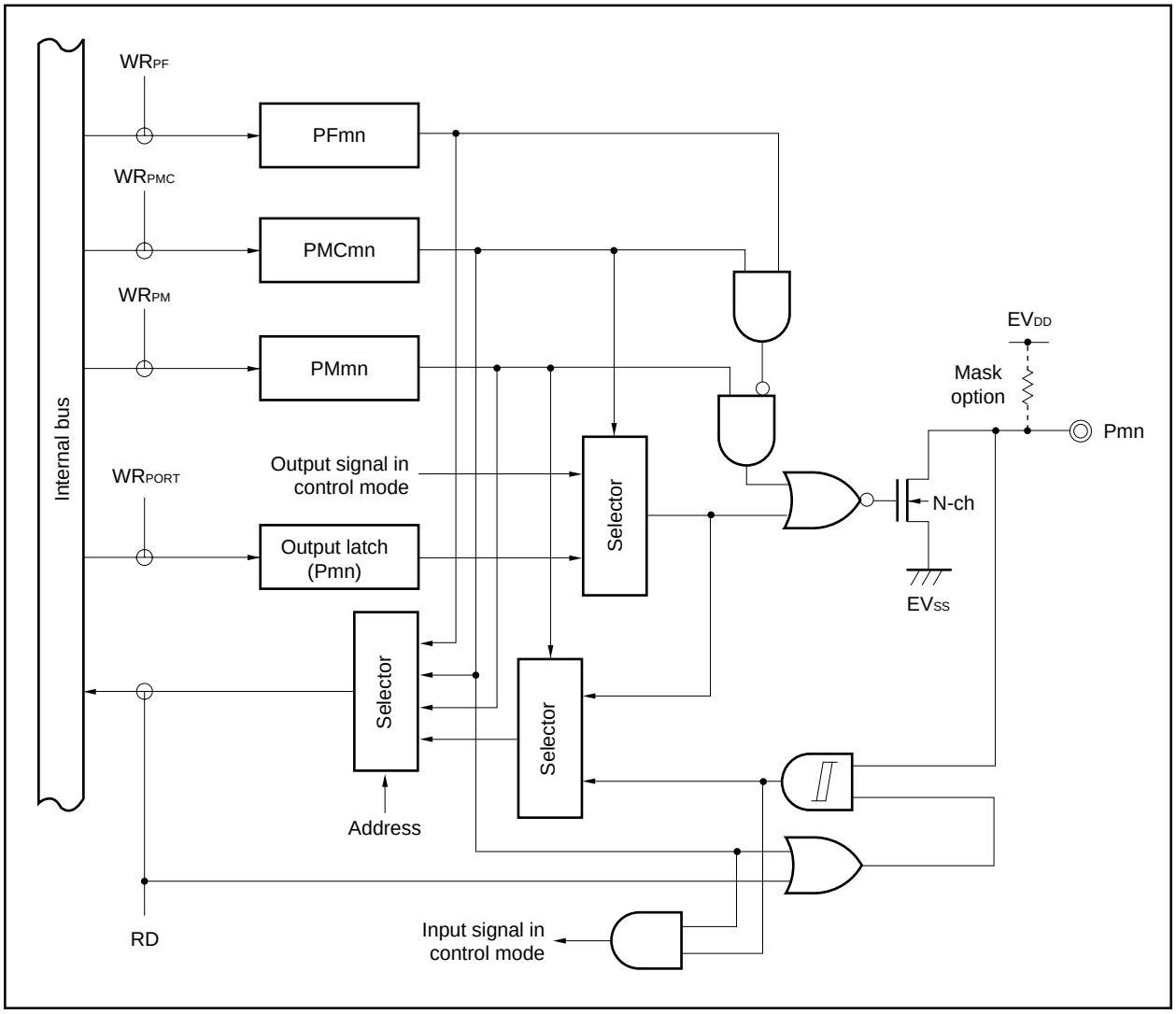


Figure 4-28. Block Diagram of Type K



4.5 Port Register Setting When Alternate Function Is Used

Table 4-29 shows the port register settings when each port is used for an alternate function.
When using a port pin as an alternate-function pin, refer to description of each pin.

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Table 4-29. Settings When Port Pins Are Used for Alternate Functions (1/7)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O					
P00	TOH0	Output	P00 = Setting not required	PM00 = Setting not required	PMC00 = 1	–	–
P01	TOH1	Output	P01 = Setting not required	PM01 = Setting not required	PMC01 = 1	–	–
P02	NMI	Input	P02 = Setting not required	PM02 = Setting not required	PMC02 = 1	–	–
P03	INTP0	Input	P03 = Setting not required	PM03 = Setting not required	PMC03 = 1	–	–
P04	INTP1	Input	P04 = Setting not required	PM04 = Setting not required	PMC04 = 1	–	–
P05	INTP2	Input	P05 = Setting not required	PM05 = Setting not required	PMC05 = 1	–	–
P06	INTP3	Input	P06 = Setting not required	PM06 = Setting not required	PMC06 = 1	–	–
P10	ANO0	Output	P10 = Setting not required	PM10 = 1 Note 1	–	–	–
P11	ANO1	Output	P11 = Setting not required	PM11 = 1 Note 1	–	–	–
P30	TXD0	Output	P30 = Setting not required	PM30 = Setting not required	PMC30 = 1	–	–
P31	RXD0	Input	P31 = Setting not required	PM31 = Setting not required	PMC31 = 1	–	–
P32	ASCK0	Input	P32 = Setting not required	PM32 = Setting not required	PMC32 = 1	–	–
P33	TI000	Input	P33 = Setting not required	PM33 = Setting not required	PMC33 = 1	PFC33 = 0	–
	TO00	Output	P33 = Setting not required	PM33 = Setting not required	PMC33 = 1	PFC33 = 1	–
P34	TI001	Input	P34 = Setting not required	PM34 = Setting not required	PMC34 = 1	–	–
P35	TI010	Input	P35 = Setting not required	PM35 = Setting not required	PMC35 = 1	PFC35 = 0	–
	TO01	Output	P35 = Setting not required	PM35 = Setting not required	PMC35 = 1	PFC35 = 1	–
P38	SDA0 Note 2	I/O	P38 = 1	PM38 = Setting not required	PMC38 = 1	–	PF38 (PF3) = 1
P39	SCL0 Note 2	I/O	P39 = 1	PM39 = Setting not required	PMC39 = 1	–	PF39 (PF3) = 1
P40	SI00	Input	P40 = Setting not required	PM40 = Setting not required	PMC40 = 1	–	–
P41	SO00	Output	P41 = Setting not required	PM41 = Setting not required	PMC41 = 1	–	PF41 (PF4) = Don't care
P42	$\overline{\text{SCK00}}$	I/O	P42 = Setting not required	PM42 = Setting not required	PMC42 = 1	–	PF42 (PF4) = Don't care

Notes 1. When setting the ANO0 and ANO1 pins, set PM1 register = FFH all together.

2. Only in products with an I^2C bus

Table 4-29. Settings When Port Pins Are Used for Alternate Functions (2/7)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O					
P50	TI011	Input	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFC50 = 0	–
	RTP00	Output	P50 = Setting not required	PM50 = Setting not required	PMC50 = 1	PFC50 = 1	–
	KR0	Input	P50 = Setting not required	PM50 = 1	PMC50 = 0	PFC50 = 0	KRM0 (KRM) = 1
P51	TI50	Input	P51 = Setting not required	PM51 = Setting not required	PMC51 = 1	PFC51 = 0	–
	RTP01	Output	P51 = Setting not required	PM51 = Setting not required	PMC51 = 1	PFC51 = 1	–
	KR1	Input	P51 = Setting not required	PM51 = 1	PMC51 = 0	PFC51 = 0	KRM1 (KRM) = 1
P52	TO50	Output	P52 = Setting not required	PM52 = Setting not required	PMC52 = 1	PFC52 = 0	–
	RTP02	Output	P52 = Setting not required	PM52 = Setting not required	PMC52 = 1	PFC52 = 1	–
	KR2	Input	P52 = Setting not required	PM52 = 1	PMC52 = 0	PFC52 = 0	KRM2 (KRM) = 1
P53	SIA0	Input	P53 = Setting not required	PM53 = Setting not required	PMC53 = 1	PFC53 = 0	–
	RTP03	Output	P53 = Setting not required	PM53 = Setting not required	PMC53 = 1	PFC53 = 1	–
	KR3	Input	P53 = Setting not required	PM53 = 1	PMC53 = 0	PFC53 = 0	KRM3 (KRM) = 1
P54	SOA0	Output	P54 = Setting not required	PM54 = Setting not required	PMC54 = 1	PFC54 = 0	PF54 (PF5) = Don't care
	RTP04	Output	P54 = Setting not required	PM54 = Setting not required	PMC54 = 1	PFC54 = 1	PF54 (PF5) = 0
	KR4	Input	P54 = Setting not required	PM54 = 1	PMC54 = 0	PFC54 = 0	PF54 (PF5) = 0, KRM4 (KRM) = 1
P55	$\overline{\text{SCKA0}}$	I/O	P55 = Setting not required	PM55 = Setting not required	PMC55 = 1	PFC55 = 0	PF55 (PF5) = Don't care
	RTP05	Output	P55 = Setting not required	PM55 = Setting not required	PMC55 = 1	PFC55 = 1	PF55 (PF5) = 0
	KR5	Input	P55 = Setting not required	PM55 = 1	PMC55 = 0	PFC55 = 0	PF55 (PF5) = 0, KRM5 (KRM) = 1

Table 4-29. Settings When Port Pins Are Used for Alternate Functions (3/7)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O					
P60	RTP10	Output	P60 = Setting not required	PM60 = Setting not required	PMC60 = 1	–	–
P61	RTP11	Output	P61 = Setting not required	PM61 = Setting not required	PMC61 = 1	–	–
P62	RTP12	Output	P62 = Setting not required	PM62 = Setting not required	PMC62 = 1	–	–
P63	RTP13	Output	P63 = Setting not required	PM63 = Setting not required	PMC63 = 1	–	–
P64	RTP14	Output	P64 = Setting not required	PM64 = Setting not required	PMC64 = 1	–	–
P65	RTP15	Output	P65 = Setting not required	PM65 = Setting not required	PMC65 = 1	–	–
P66	SI02	Input	P66 = Setting not required	PM66 = Setting not required	PMC66 = 1	–	–
P67	SO02	Output	P67 = Setting not required	PM67 = Setting not required	PMC67 = 1	–	PF67 (PF6) = Don't care
P68	$\overline{\text{SCK02}}$	I/O	P68 = Setting not required	PM68 = Setting not required	PMC68 = 1	–	PF68 (PF6) = Don't care
P69	TI040	Input	P69 = Setting not required	PM69 = Setting not required	PMC69 = 1	–	–
P610	TI041	Input	P610 = Setting not required	PM610 = Setting not required	PMC610 = 1	–	–
P611	TO04	Output	P611 = Setting not required	PM611 = Setting not required	PMC611 = 1	–	–
P612	TI050	Input	P612 = Setting not required	PM612 = Setting not required	PMC612 = 1	–	–
P613	TI051	Input	P613 = Setting not required	PM613 = Setting not required	PMC613 = 1	PFC613 = 0	–
	TO05	Output	P613 = Setting not required	PM613 = Setting not required	PMC613 = 1	PFC613 = 1	–

Table 4-29. Settings When Port Pins Are Used for Alternate Functions (4/7)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O					
P70	ANI0	Input	P70 = Setting not required	–	–	–	–
P71	ANI1	Input	P71 = Setting not required	–	–	–	–
P72	ANI2	Input	P72 = Setting not required	–	–	–	–
P73	ANI3	Input	P73 = Setting not required	–	–	–	–
P74	ANI4	Input	P74 = Setting not required	–	–	–	–
P75	ANI5	Input	P75 = Setting not required	–	–	–	–
P76	ANI6	Input	P76 = Setting not required	–	–	–	–
P77	ANI7	Input	P77 = Setting not required	–	–	–	–
P78	ANI8	Input	P78 = Setting not required	–	–	–	–
P79	ANI9	Input	P79 = Setting not required	–	–	–	–
P710	ANI10	Input	P710 = Setting not required	–	–	–	–
P711	ANI11	Input	P711 = Setting not required	–	–	–	–
P712	ANI12	Input	P712 = Setting not required	–	–	–	–
P713	ANI13	Input	P713 = Setting not required	–	–	–	–
P714	ANI14	Input	P714 = Setting not required	–	–	–	–
P715	ANI15	Input	P715 = Setting not required	–	–	–	–
P80	RXD2	Input	P80 = Setting not required	PM80 = Setting not required	PMC80 = 1	PFC80 = 0	PF80 (PF8) = 0
	SDA1[Note]	I/O	P80 = Setting not required	PM80 = Setting not required	PMC80 = 1	PFC80 = 1	PF80 (PF8) = 1
P81	TXD2	Output	P81 = Setting not required	PM81 = Setting not required	PMC81 = 1	PFC81 = 0	PF80 (PF8) = 0
	SCL1[Note]	I/O	P81 = Setting not required	PM81 = Setting not required	PMC81 = 1	PFC81 = 1	PF81 (PF8) = 1

Note Only in the μPD703216Y, 703217Y, and 70F3217Y

Table 4-29. Settings When Port Pins Are Used for Alternate Functions (5/7)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O					
P90	A0	Output	P90 = Setting not required	PM90 = Setting not required	PMC90 = 1	PFC90 = 0	**Note**
	TXD1	Output	P90 = Setting not required	PM90 = Setting not required	PMC90 = 1	PFC90 = 1	–
	KR6	Input	P90 = Setting not required	PM90 = 1	PMC90 = 0	PFC90 = 0	KRM6 (KRM) = 1
P91	A1	Output	P91 = Setting not required	PM91 = Setting not required	PMC91 = 1	PFC91 = 0	**Note**
	RXD1	Input	P91 = Setting not required	PM91 = Setting not required	PMC91 = 1	PFC91 = 1	–
	KR7	Input	P91 = Setting not required	PM91 = 1	PMC91 = 0	PFC91 = 0	KRM7 (KRM) = 1
P92	A2	Output	P92 = Setting not required	PM92 = Setting not required	PMC92 = 1	PFC92 = 0	**Note**
	TI020	Input	P92 = Setting not required	PM92 = Setting not required	PMC92 = 0	PFC92 = 0	–
	TO02	Output	P92 = 1	PM92 = Setting not required	PMC92 = 1	PFC92 = 1	–
P93	A3	Output	P93 = Setting not required	PM93 = Setting not required	PMC93 = 1	PFC93 = 0	**Note**
	TI021	Input	P93 = Setting not required	PM93 = Setting not required	PMC93 = 1	PFC93 = 1	–
P94	A4	Output	P94 = Setting not required	PM94 = Setting not required	PMC94 = 1	PFC94 = 0	**Note**
	TI030	Input	P94 = Setting not required	PM94 = 1	PMC94 = 0	PFC94 = 0	–
	TO03	Output	P94 = Setting not required	PM94 = Setting not required	PMC94 = 1	PFC94 = 1	–
P95	A5	Output	P95 = Setting not required	PM95 = Setting not required	PMC95 = 1	PFC95 = 0	**Note**
	TI031	Input	P95 = Setting not required	PM95 = Setting not required	PMC95 = 1	PFC95 = 1	–
P96	A6	Output	P96 = Setting not required	PM96 = Setting not required	PMC96 = 1	PFC96 = 0	**Note**
	TI51	Input	P96 = Setting not required	PM96 = 1	PMC96 = 0	PFC96 = 0	–
	TO51	Output	P96 = Setting not required	PM96 = Setting not required	PMC96 = 1	PFC96 = 1	–
P97	A7	Output	P97 = Setting not required	PM97 = Setting not required	PMC97 = 1	PFC97 = 0	**Note**
	SI01	Input	P97 = Setting not required	PM97 = Setting not required	PMC97 = 1	PFC97 = 1	
P98	A8	Output	P98 = Setting not required	PM98 = Setting not required	PMC98 = 1	PFC98 = 0	**Note**, PF98 (PF9) = 0
	SO01	Output	P98 = Setting not required	PM98 = Setting not required	PMC98 = 1	PFC98 = 1	PF98 (PF9) = Don't care
P99	A9	Output	P99 = Setting not required	PM99 = Setting not required	PMC99 = 1	PFC99 = 0	**Note**, PF98 (PF9) = 0
	$\overline{\text{SCK01}}$	I/O	P99 = Setting not required	PM99 = Setting not required	PMC99 = 1	PFC99 = 1	PF98 (PF9) = Don't care

Note When setting the A0 to A15 pins, set the PFC9 register to 0000H and the PMC9 register to FFFFH in 16-bit units.

Table 4-29. Settings When Port Pins Are Used for Alternate Functions (6/7)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O					
P910	A10	Output	P910 = Setting not required	PM910 = Setting not required	PMC910 = 1	PFC910 = 0	**Note**
	SIA1	Input	P910 = Setting not required	PM910 = Setting not required	PMC910 = 1	PFC910 = 1	–
P911	A11	Output	P911 = Setting not required	PM911 = Setting not required	PMC911 = 1	PFC911 = 0	**Note**, PF911 (PF9) = 0
	SOA1	Output	P911 = Setting not required	PM911 = Setting not required	PMC911 = 1	PFC911 = 1	PF911 (PF9) = Don't care
P912	A12	Output	P912 = Setting not required	PM912 = Setting not required	PMC912 = 1	PFC912 = 0	**Note**, PF912 (PF9) = 0
	$\overline{\text{SCKA1}}$	I/O	P912 = Setting not required	PM912 = Setting not required	PMC912 = 1	PFC912 = 1	PF912 (PF9) = Don't care
P913	A13	Output	P913 = Setting not required	PM913 = Setting not required	PMC913 = 1	PFC913 = 0	**Note**
	INTP4	Input	P913 = Setting not required	PM913 = Setting not required	PMC913 = 1	PFC913 = 1	–
P914	A14	Output	P914 = Setting not required	PM914 = Setting not required	PMC914 = 1	PFC914 = 0	**Note**
	INTP5	Input	P914 = Setting not required	PM914 = Setting not required	PMC914 = 1	PFC914 = 1	I–
P915	A15	Output	P915 = Setting not required	PM915 = Setting not required	PMC915 = 1	PFC915 = 0	**Note**
	INTP6	Input	P915 = Setting not required	PM915 = Setting not required	PMC915 = 1	PFC915 = 1	–
PCM0	$\overline{\text{WAIT}}$	Input	PCM0 = Setting not required	PMCM0 = Setting not required	PMCCM0 = 1	–	–
PCM1	CLKOUT	Output	PCM1 = Setting not required	PMCM1 = Setting not required	PMCCM1 = 1	–	–
PCM2	$\overline{\text{HLDAK}}$	Output	PCM2 = Setting not required	PMCM2 = Setting not required	PMCCM2 = 1	–	–
PCM3	$\overline{\text{HLDRQ}}$	Input	PCM3 = Setting not required	PMCM3 = Setting not required	PMCCM3 = 1	–	–
PCS0	$\overline{\text{CS0}}$	Output	PCS0 = Setting not required	PMCS0 = Setting not required	PMCCS0 = 1	–	–
PCS1	$\overline{\text{CS1}}$	Output	PCS1 = Setting not required	PMCS1 = Setting not required	PMCCS1 = 1	–	–
PCS2	$\overline{\text{CS2}}$	Output	PCS2 = Setting not required	PMCS2 = Setting not required	PMCCS2 = 1	–	–
PCS3	$\overline{\text{CS3}}$	Output	PCS3 = Setting not required	PMCS3 = Setting not required	PMCCS3 = 1	–	–
PCT0	$\overline{\text{WR0}}$	Output	PCT0 = Setting not required	PMCT0 = Setting not required	PMCCT0 = 1	–	–
PCT1	$\overline{\text{WR1}}$	Output	PCT1 = Setting not required	PMCT1 = Setting not required	PMCCT1 = 1	–	–
PCT4	$\overline{\text{RD}}$	Output	PCT4 = Setting not required	PMCT4 = Setting not required	PMCCT4 = 1	–	–
PCT6	ASTB	Output	PCT6 = Setting not required	PMCT6 = Setting not required	PMCCT6 = 1	–	–

Note When setting the A0 to A15 pins, set the PFC9 register to 0000H and the PMC9 register to FFFFH in 16-bit units.

Table 4-29. Settings When Port Pins Are Used for Alternate Functions (7/7)

Pin Name	Alternate Function		Pnx Bit of Pn Register	PMnx Bit of PMn Register	PMCnx Bit of PMCn Register	PFCnx Bit of PFCn Register	Other Bits (Registers)
	Function Name	I/O					
PDH0	A16	Output	PDH0 = Setting not required	PMDH0 = Setting not required	PMCDH0 = 1	–	–
PDH1	A17	Output	PDH1 = Setting not required	PMDH1 = Setting not required	PMCDH1 = 1	–	–
PDH2	A18	Output	PDH2 = Setting not required	PMDH2 = Setting not required	PMCDH2 = 1	–	–
PDH3	A19	Output	PDH3 = Setting not required	PMDH3 = Setting not required	PMCDH3 = 1	–	–
PDH4	A20	Output	PDH4 = Setting not required	PMDH4 = Setting not required	PMCDH4 = 1	–	–
PDH5	A21	Output	PDH5 = Setting not required	PMDH5 = Setting not required	PMCDH5 = 1	–	–
PDH6	A22	Output	PDH6 = Setting not required	PMDH6 = Setting not required	PMCDH6 = 1	–	–
PDH7	A23	Output	PDH7 = Setting not required	PMDH7 = Setting not required	PMCDH7 = 1	–	–
PDL0	AD0	I/O	PDL0 = Setting not required	PMDL0 = Setting not required	PMCDL0 = 1	–	–
PDL1	AD1	I/O	PDL1 = Setting not required	PMDL1 = Setting not required	PMCDL1 = 1	–	–
PDL2	AD2	I/O	PDL2 = Setting not required	PMDL2 = Setting not required	PMCDL2 = 1	–	–
PDL3	AD3	I/O	PDL3 = Setting not required	PMDL3 = Setting not required	PMCDL3 = 1	–	–
PDL4	AD4	I/O	PDL4 = Setting not required	PMDL4 = Setting not required	PMCDL4 = 1	–	–
PDL5	AD5	I/O	PDL5 = Setting not required	PMDL5 = Setting not required	PMCDL5 = 1	–	–
PDL6	AD6	I/O	PDL6 = Setting not required	PMDL6 = Setting not required	PMCDL6 = 1	–	–
PDL7	AD7	I/O	PDL7 = Setting not required	PMDL7 = Setting not required	PMCDL7 = 1	–	–
PDL8	AD8	I/O	PDL8 = Setting not required	PMDL8 = Setting not required	PMCDL8 = 1	–	–
PDL9	AD9	I/O	PDL9 = Setting not required	PMDL9 = Setting not required	PMCDL9 = 1	–	–
PDL10	AD10	I/O	PDL10 = Setting not required	PMDL10 = Setting not required	PMCDL10 = 1	–	–
PDL11	AD11	I/O	PDL11 = Setting not required	PMDL11 = Setting not required	PMCDL11 = 1	–	–
PDL12	AD12	I/O	PDL12 = Setting not required	PMDL12 = Setting not required	PMCDL12 = 1	–	–
PDL13	AD13	I/O	PDL13 = Setting not required	PMDL13 = Setting not required	PMCDL13 = 1	–	–
PDL14	AD14	I/O	PDL14 = Setting not required	PMDL14 = Setting not required	PMCDL14 = 1	–	–
PDL15	AD15	I/O	PDL15 = Setting not required	PMDL15 = Setting not required	PMCDL15 = 1	–	–

★ 4.6 Cautions

4.6.1 Cautions on bit manipulation instruction for port n register (Pn)

When a 1-bit manipulation instruction is executed on a port that provides both input and output functions, the value of the output latch of an input port that is not subject to manipulation may be written in addition to the targeted bit.

Therefore, it is recommended to rewrite the output latch when switching a port from input mode to output mode.

<Example> When P90 is an output port, P91 to P97 are input ports (all pin statuses are high level), and the value of the port latch is 0x00, if the output of output port 90 is changed from low level to high level via a bit manipulation instruction, the value of the port latch is 0xFF.

Explanation: The targets of writing to and reading from the Pn register of a port whose PMnm bit is 1 are the output latch and pin status, respectively.

A bit manipulation instruction is executed in the following order in the V850ES/Kx1.

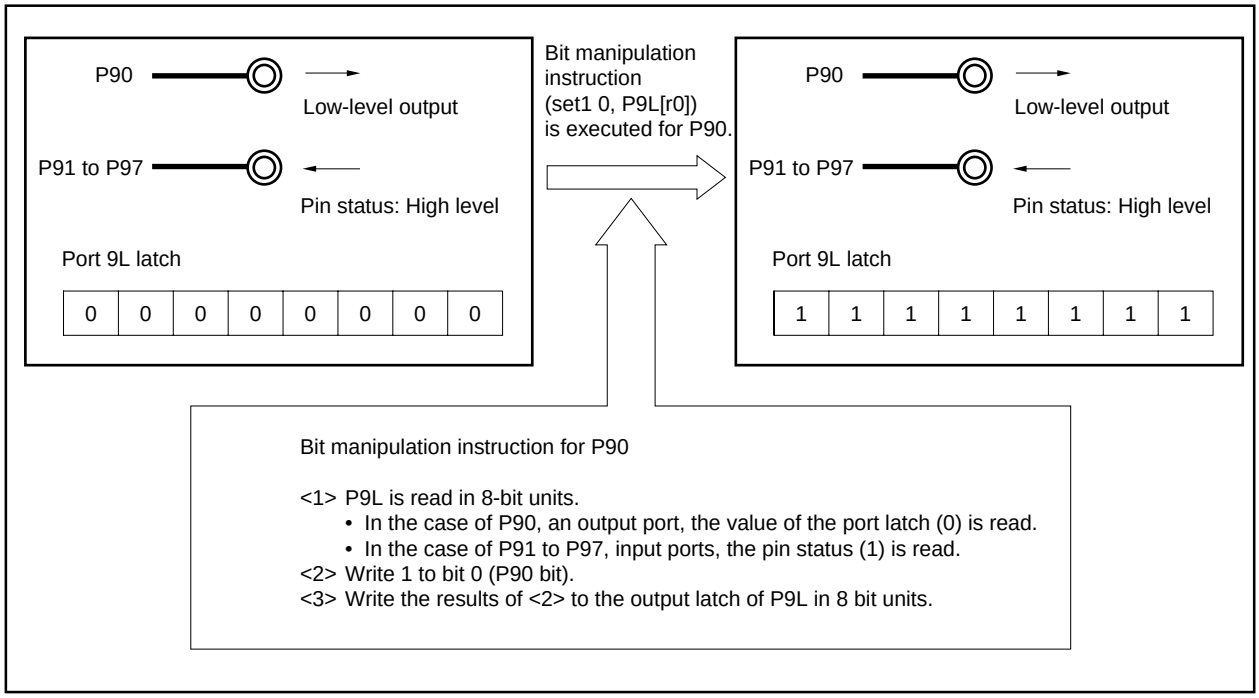
<1> The Pn register is read in 8-bit units.
<2> The targeted one bit is manipulated.
<3> The Pn register is written in 8-bit units.

In step <1>, the value of the output latch (0) of P90, which is an output port, is read, while the pin statuses of P91 to P97, which are input ports, are read. If the pin statuses of P91 to P97 are high level at this time, the read value is 0xFE.

The value is changed to 0xFF by the manipulation in <2>.

0xFF is written to the output latch by the manipulation in <3>.

Figure 4-29. Bit Manipulation Instruction (P90)



4.6.2 Hysteresis Characteristics

In port mode, the following ports do not have hysteresis characteristics.

P02 to P06
P31 to P35, P38, P39
P40, P42
P66, P68 to P610, P612, P613
P80, P81
P93, P95, P97, P99, P910, P912 to P915

CHAPTER 5 BUS CONTROL FUNCTION

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 are provided with an external bus interface function by which external memories such as ROM and RAM, and I/O can be connected.

5.1 Features

- Output is selectable from a multiplex bus with a minimum of 3 bus cycles and a separate bus with a minimum of 2 bus cycles (separate bus output is only available in the V850ES/KG1 and V850ES/KJ1)
- Chip select function for up to 4 spaces (V850ES/KF1, V850ES/KG1: 2 spaces, V850ES/KJ1: 4 spaces)
- 8-bit/16-bit data bus selectable (for each area selected by chip select function)
- Wait function
  - Programmable wait function of up to 7 states (selectable for each area selected by chip select function)
  - External wait function using $\overline{\text{WAIT}}$ pin
- Idle state function
- Bus hold function
- The bus can be controlled using a different voltage from the operating voltage by setting $BV_{DD} \leq V_{DD} = EV_{DD}$ (however, only in multiplex bus mode).

5.2 Bus Control Pins

The pins used to connect an external device are listed in the table below.

(1) Multiplex bus mode

Table 5-1. V850ES/KF1 Bus Control Pins

Bus Control Pin	Alternate-Function Pin	I/O	Function
AD0 to AD15	PDL0 to PDL15	I/O	Address/data bus
$\overline{\text{WAIT}}$	PCM0	Input	External wait control
CLKOUT	PCM1	Output	Internal system clock output
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	PCS0, PCS1	Output	Chip select
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$	PCT0, PCT1	Output	Write strobe signal
$\overline{\text{RD}}$	PCT4	Output	Read strobe signal
ASTB	PCT6	Output	Address strobe signal
$\overline{\text{HLDRQ}}$	PCM3	Input	Bus hold control
$\overline{\text{HLDAK}}$	PCM2	Output	

Table 5-2. V850ES/KG1 Bus Control Pins

Bus Control Pin	Alternate-Function Pin	I/O	Function
AD0 to AD15	PDL0 to PDL15	I/O	Address/data bus
A16 to A21	PDH0 to PDH5	Output	Address bus
$\overline{\text{WAIT}}$	PCM0	Input	External wait control
CLKOUT	PCM1	Output	Internal system clock output
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	PCS0 to PCS1	Output	Chip select
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$	PCT0, PCT1	Output	Write strobe signal
$\overline{\text{RD}}$	PCT4	Output	Read strobe signal
ASTB	PCT6	Output	Address strobe signal
$\overline{\text{HLDRQ}}$	PCM3	Input	Bus hold control
$\overline{\text{HLDAK}}$	PCM2	Output	

Table 5-3. V850ES/KJ1 Bus Control Pins

Bus Control Pin	Alternate-Function Pin	I/O	Function
AD0 to AD15	PDL0 to PDL15	I/O	Address/data bus
A16 to A23	PDH0 to PDH7	Output	Address bus
$\overline{\text{WAIT}}$	PCM0	Input	External wait control
CLKOUT	PCM1	Output	Internal system clock output
$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	PCS0 to PCS3	Output	Chip select
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$	PCT0, PCT1	Output	Write strobe signal
$\overline{\text{RD}}$	PCT4	Output	Read strobe signal
ASTB	PCT6	Output	Address strobe signal
$\overline{\text{HLDRQ}}$	PCM3	Input	Bus hold control
$\overline{\text{HLDAK}}$	PCM2	Output	

(2) Separate bus mode

Note that the separate bus mode is not available in the V850ES/KF1.

Table 5-4. V850ES/KG1 Bus Control Pins

Bus Control Pin	Alternate-Function Pin	I/O	Function
AD0 to AD15	PDL0 to PDL15	I/O	Data bus
A0 to A15	P90 to P915	Output	Address bus
A16 to A21	PDH0 to PDH5	Output	Address bus
$\overline{\text{WAIT}}$	PCM0	Input	External wait control
CLKOUT	PCM1	Output	Internal system clock output
$\overline{\text{CS0}}$, $\overline{\text{CS1}}$	PCS0, PCS1	Output	Chip select
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$	PCT0, PCT1	Output	Write strobe signal
$\overline{\text{RD}}$	PCT4	Output	Read strobe signal
$\overline{\text{HLDRQ}}$	PCM3	Input	Bus hold control
$\overline{\text{HLDAK}}$	PCM2	Output	

Table 5-5. V850ES/KJ1 Bus Control Pins

Bus Control Pin	Alternate-Function Pin	I/O	Function
AD0 to AD15	PDL0 to PDL15	I/O	Data bus
A0 to A15	P90 to P915	Output	Address bus
A16 to A23	PDH0 to PDH7	Output	Address bus
$\overline{\text{WAIT}}$	PCM0	Input	External wait control
CLKOUT	PCM1	Output	Internal system clock output
$\overline{\text{CS0}}$ to $\overline{\text{CS3}}$	PCS0 to PCS3	Output	Chip select
$\overline{\text{WR0}}$, $\overline{\text{WR1}}$	PCT0, PCT1	Output	Write strobe signal
$\overline{\text{RD}}$	PCT4	Output	Read strobe signal
$\overline{\text{HLDRQ}}$	PCM3	Input	Bus hold control
$\overline{\text{HLDAK}}$	PCM2	Output	

★ **5.2.1 Pin status when internal ROM, internal RAM, or on-chip peripheral I/O is accessed**

When the internal ROM, internal RAM, or on-chip peripheral I/O are accessed, the status of each pin is as follows.

Table 5-6. Pin Statuses When Internal ROM, Internal RAM, or On-Chip Peripheral I/O Is Accessed

Separate Bus Mode[Note 1]		Multiplex Bus Mode	
Address bus (A23 to A0[Note 2])	Undefined	Address bus (A23 to A16[Note 3])	Undefined
Data bus (AD15 to AD0)	Hi-Z	Address/data bus (AD15 to AD0)	Undefined
Control signal	Inactive	Control signal	Inactive

Notes 1. Separate bus mode cannot be used in the V850ES/KF1.

2. V850ES/KG1: A21 to A0
V850ES/KF1: No address bus is provided.

3. V850ES/KG1: A21 to A16
V850ES/KF1: No address bus is provided.

Caution When a write access is performed to the internal ROM area, address, data, and control signals are activated in the same way as access to the external memory area.

5.2.2 Pin status in each operation mode

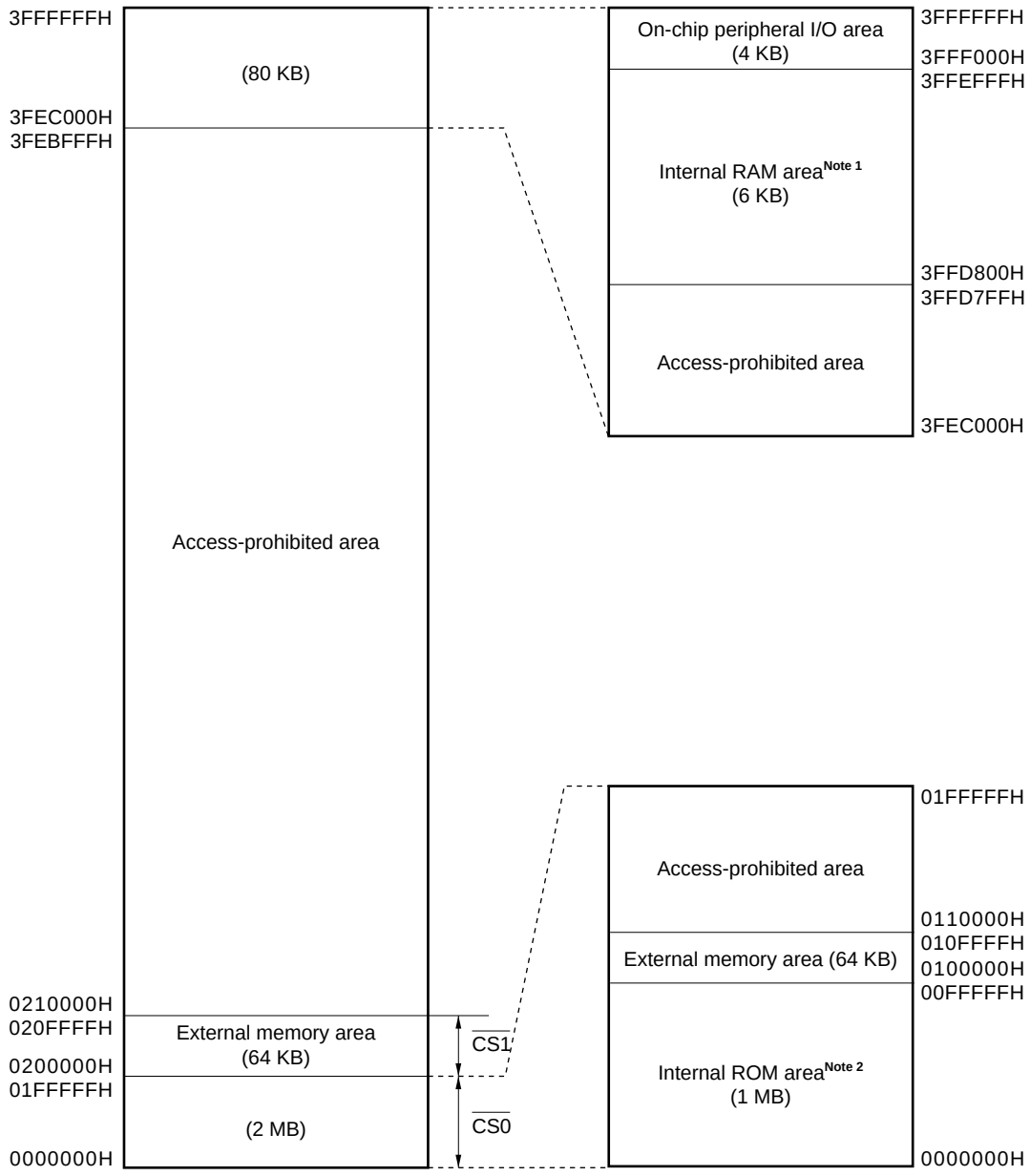
For the pin status of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 in each operation mode, refer to **2.2 Pin Status**.

5.3 Memory Block Function

(1) V850ES/KF1

The 64 MB memory space is divided into memory blocks of (lower) 2 MB and 64 KB. The programmable wait function and bus cycle operation mode for each of these blocks can be independently controlled in one-block units.

Figure 5-1. Data Memory Map: Physical Address (V850ES/KF1)



Notes 1. This area is the 4 KB space of 3FFE000H to 3FFEFFFH in the μPD703208, 703208Y, 703209, and 703209Y.

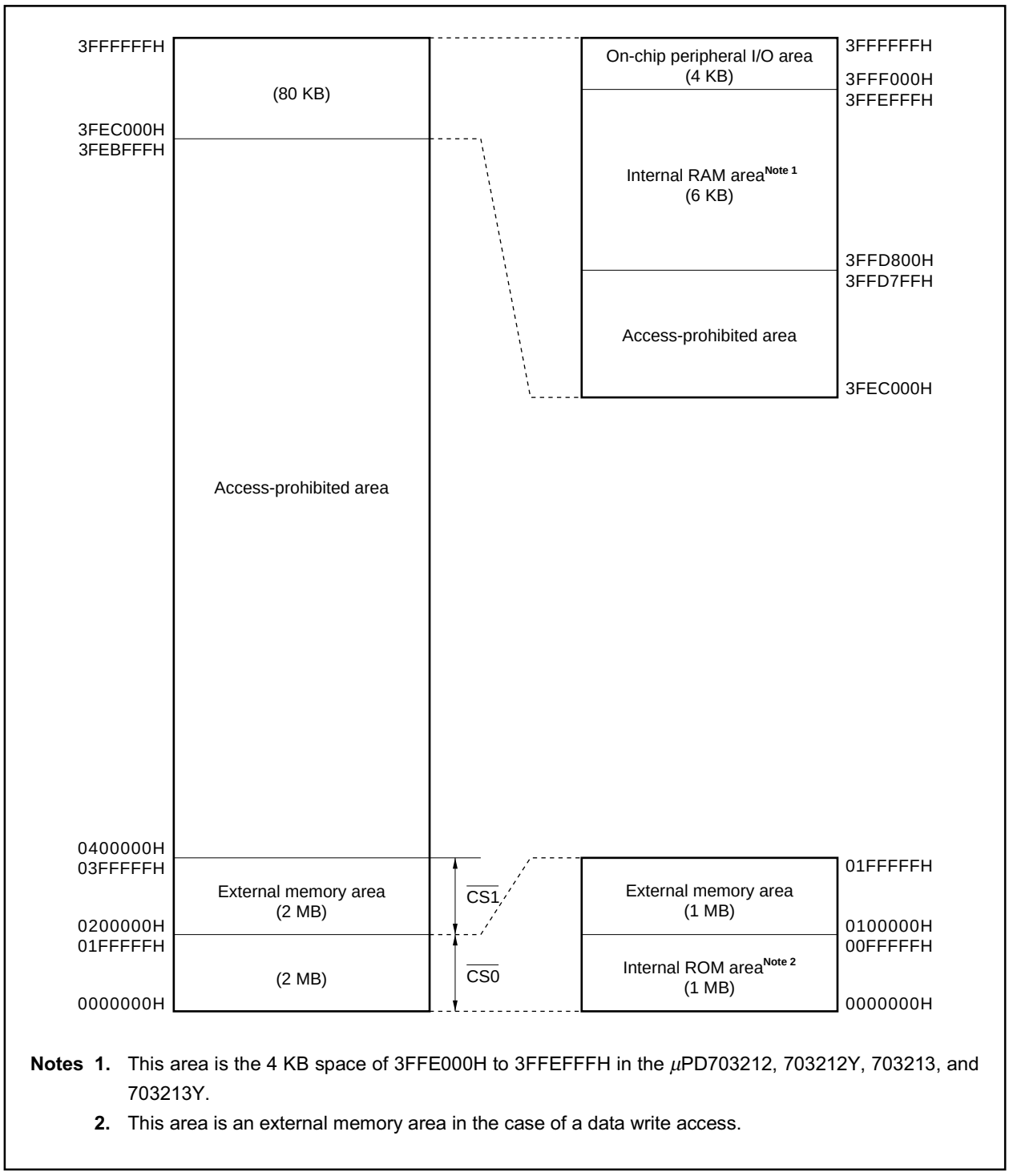
2. This area is an external memory area in the case of a data write access.

Caution A write access to addresses 0000000H to 000FFFFH is the same operation as a write access to addresses 0100000H to 010FFFFH.

(2) V850ES/KG1

The 64 MB memory space is divided into memory blocks of (lower) 2 MB and 2 MB. The programmable wait function and bus cycle operation mode for each of these blocks can be independently controlled in one-block units.

Figure 5-2. Data Memory Map: Physical Address (V850ES/KG1)



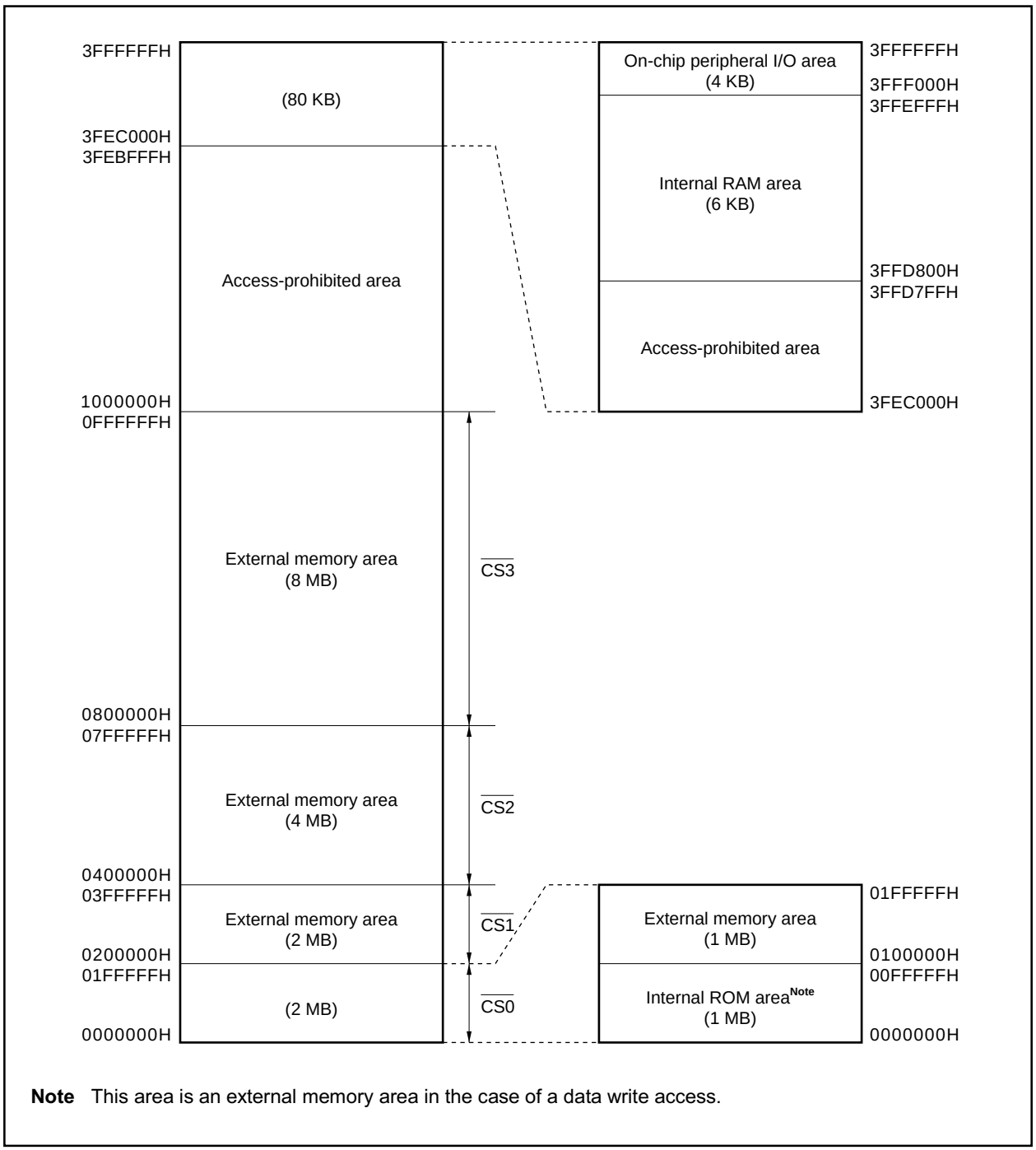
Notes 1. This area is the 4 KB space of 3FFE000H to 3FFEFFFH in the μPD703212, 703212Y, 703213, and 703213Y.

2. This area is an external memory area in the case of a data write access.

(3) V850ES/KJ1

The 64 MB memory space is divided into memory blocks of (lower) 2 MB, 2 MB, 4 MB, and 8 MB. The programmable wait function and bus cycle operation mode for each of these blocks can be independently controlled in one-block units.

Figure 5-3. Data Memory Map: Physical Address (V850ES/KJ1)



Note This area is an external memory area in the case of a data write access.

5.3.1 Chip select control function

Of the 64 MB (linear) address space, the lower 16 MB (0000000H to 0FFFFFFH) include four chip select control functions, $\overline{CS0}$ to $\overline{CS3}$. The areas that can be selected by $\overline{CS0}$ to $\overline{CS3}$ are fixed.

By using these chip select control functions, the memory block can be divided to enable effective use of the memory space. The allocation of the memory blocks is shown in the table below.

	V850ES/KF1	V850ES/KG1	V850ES/KJ1
$\overline{CS0}$	0000000H to 010FFFFH (1088 KB)	0000000H to 01FFFFFH (2 MB)	0000000H to 01FFFFFH (2 MB)
$\overline{CS1}$	0200000H to 020FFFFH (64 KB)	0200000H to 03FFFFFH (2 MB)	0200000H to 03FFFFFH (2 MB)
$\overline{CS2}$	–	–	0400000H to 07FFFFFH (4 MB)
$\overline{CS3}$	–	–	0800000H to 0FFFFFFH (8 MB)

5.4 External Bus Interface Mode Control Function

The V850ES/KG1 and V850ES/KJ1 include the following two external bus interface modes.

- Multiplex bus mode
- Separate bus mode

These two modes can be selected by using the external bus interface mode control register (EXIMC).

Remark Only the multiplex bus mode is available in the V850ES/KF1.

(1) External bus interface mode control register (EXIMC)

This register can be read or written in 8-bit or 1-bit units.

After reset, this register is cleared to 00H.

Caution The EXIMC register is only available in the V850ES/KG1 and V850ES/KJ1.

After reset: 00H R/W Address: FFFFFFBEH

	7	6	5	4	3	2	1	0
EXIMC	0	0	0	0	0	0	0	SMSEL

SMSEL	Mode selection
0	Multiplex bus mode
1	Separate bus mode

Caution Set the EXIMC register from the internal ROM or internal RAM area before external access.
After setting the EXIMC register, be sure to set a NOP instruction.

5.5 Bus Access

5.5.1 Number of clocks for access

The following table shows the number of basic clocks required for accessing each resource.

Bus Cycle Type \ Area (Bus Width)	Internal ROM (32 Bits)	Internal RAM (32 Bits)	External Memory (16 Bits)
Instruction fetch (normal access)	1	1 Note 1	3 + n Note 2
Instruction fetch (branch)	2	2 Note 1	3+ n Note 2
Operand data access	3	1	3 +n Note 2

Notes 1. If the access conflicts with a data access, the number of clock is increased by 1.

2. 2 + n clocks (n: Number of wait states) when the separate bus mode is selected (V850ES/KG1 and V850ES/KJ1).

Remark Unit: Clocks/access

5.5.2 Bus size setting function

The bus size of each external memory area selected by $\overline{CSn}$ can be set (to 8 bits or 16 bits) by using the BSC register.

The external memory area of the V850ES/KJ1 is selected by $\overline{CS0}$ to $\overline{CS3}$.

The external memory area of the V850ES/KG1 is selected by $\overline{CS0}$ and $\overline{CS1}$.

The external memory area of the V850ES/KF1 is selected by $\overline{CS0}$ and $\overline{CS1}$.

(1) Bus size configuration register (BSC)

This register can be read or written in 16-bit units.

Caution Write to the BSC register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the BSC register are complete.

After reset: 5555H R/W Address: FFFFF066H

	15	14	13	12	11	10	9	8
BSC	0	1	0	1	0	1	0	1

7	6	5	4	3	2	1	0
0	BS30 Note	0	BS20 Note	0	BS10	0	BS00
$\overline{CSn}$ signal	$\overline{CS3}$		$\overline{CS2}$		$\overline{CS1}$		$\overline{CS0}$

BSn0	Data bus width of CSn space (n = 0 to 3)
0	8 bits
1	16 bits

Note The BS30 and BS20 bits are only valid in the V850ES/KJ1. Changing these bits has no effect on the operation in the V850ES/KF1 and V850ES/KG1.

Caution Be sure to set bits 14, 12, 10, and 8 to 1, and clear bits 15, 13, 11, 9, 7, 5, 3, and 1 to 0.

5.5.3 Access by bus size

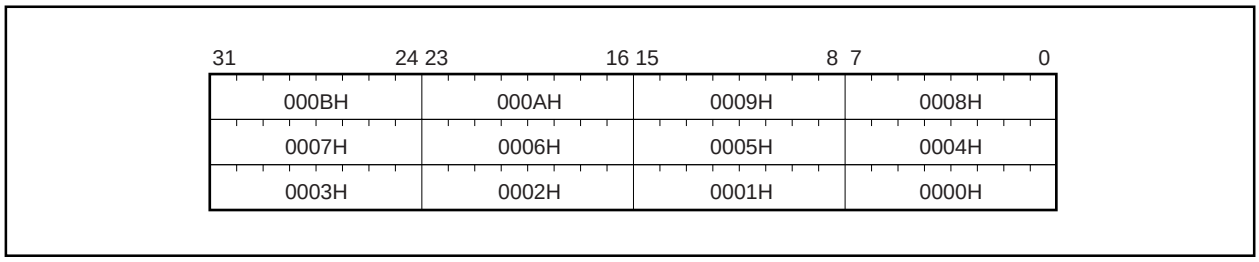
The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 access the on-chip peripheral I/O and external memory in 8-bit, 16-bit, or 32-bit units. The bus size is as follows.

- The bus size of the on-chip peripheral I/O is fixed to 16 bits.
- The bus size of the external memory is selectable from 8 bits or 16 bits (by using the BSC register).

The operation when each of the above is accessed is described below. All data is accessed starting from the lower side.

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 support only the little endian format.

Figure 5-4. Little Endian Address in Word



(1) Data space

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 have an address misalign function.

With this function, data can be placed at all addresses, regardless of the format of the data (word data or halfword data). However, if the word data or halfword data is not aligned at the boundary, a bus cycle is generated at least twice, causing the bus efficiency to drop.

(a) Halfword-length data access

A byte-length bus cycle is generated twice if the least significant bit of the address is 1.

(b) Word-length data access

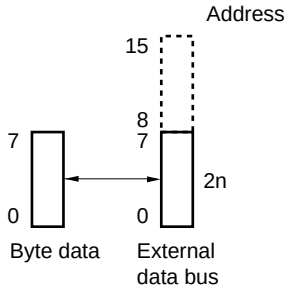
(i) A byte-length bus cycle, halfword-length bus cycle, and byte-length bus cycle are generated in that order if the least significant bit of the address is 1.

(ii) A halfword-length bus cycle is generated twice if the lower 2 bits of the address are 10.

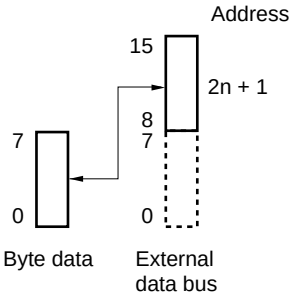
(2) Byte access (8 bits)

(a) 16-bit data bus width

<1> Access to even address (2n)

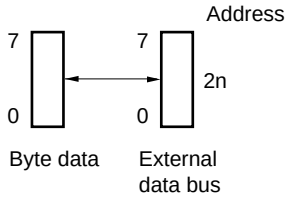


<2> Access to odd address (2n + 1)

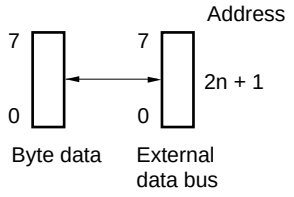


(b) 8-bit data bus width

<1> Access to even address (2n)

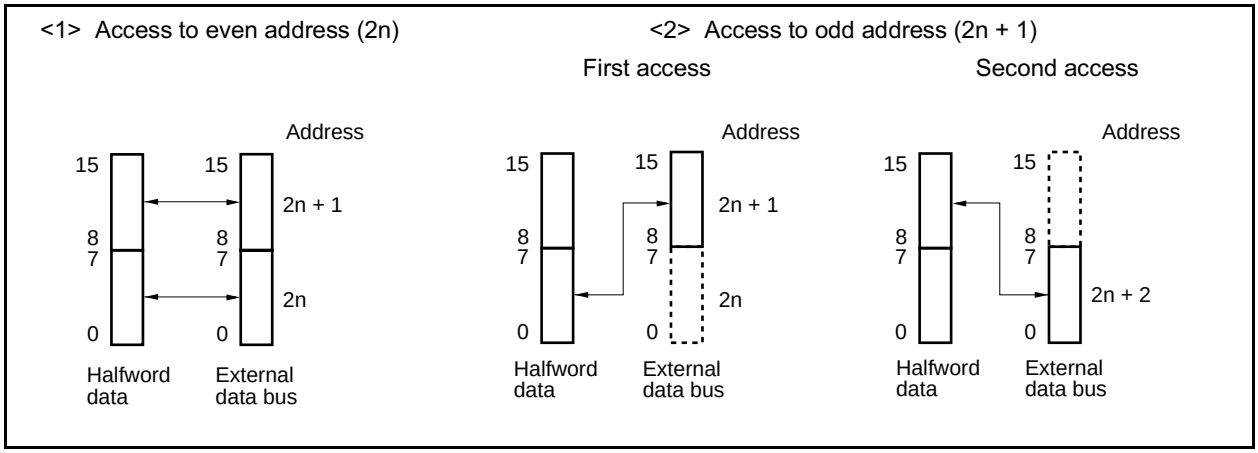


<2> Access to odd address (2n + 1)

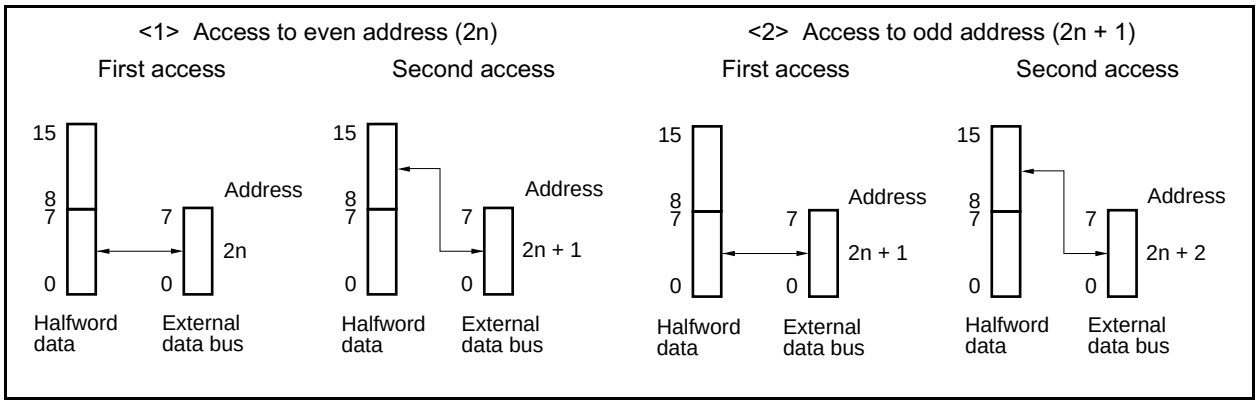


(3) Halfword access (16 bits)

(a) With 16-bit data bus width



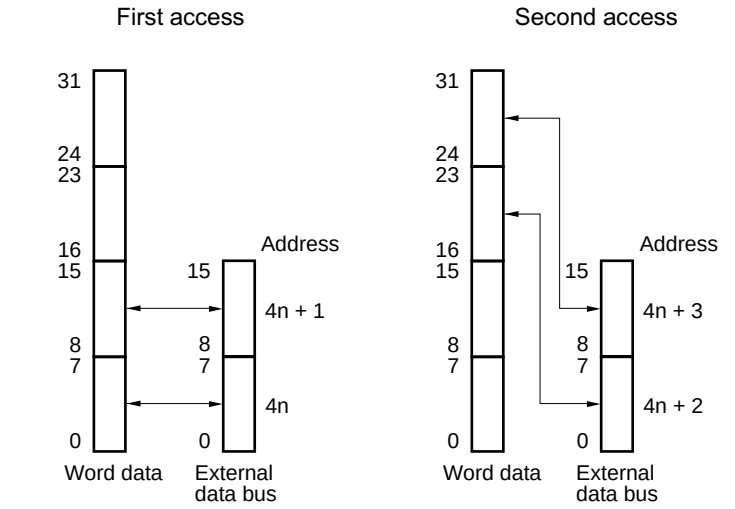
(b) 8-bit data bus width



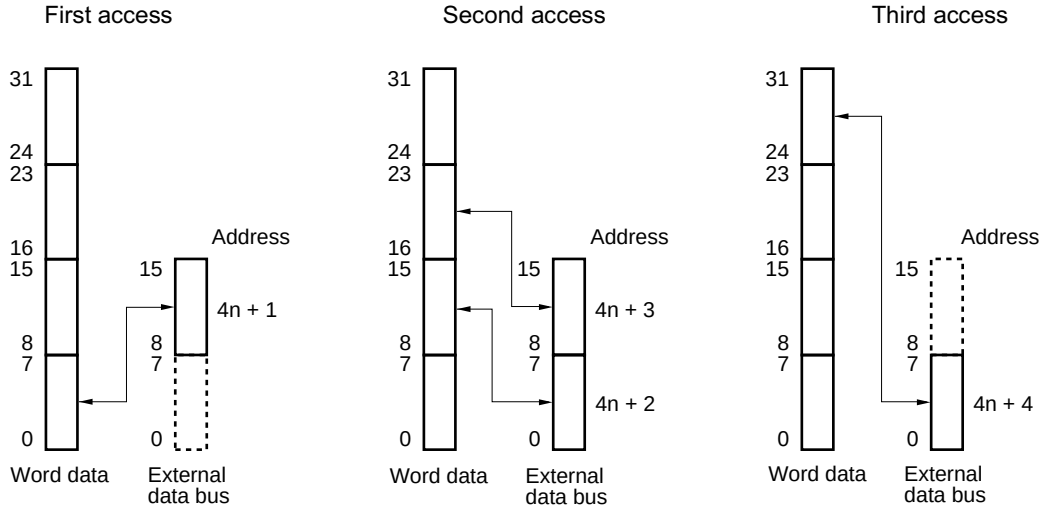
(4) Word access (32 bits)

(a) 16-bit data bus width (1/2)

<1> Access to address (4n)

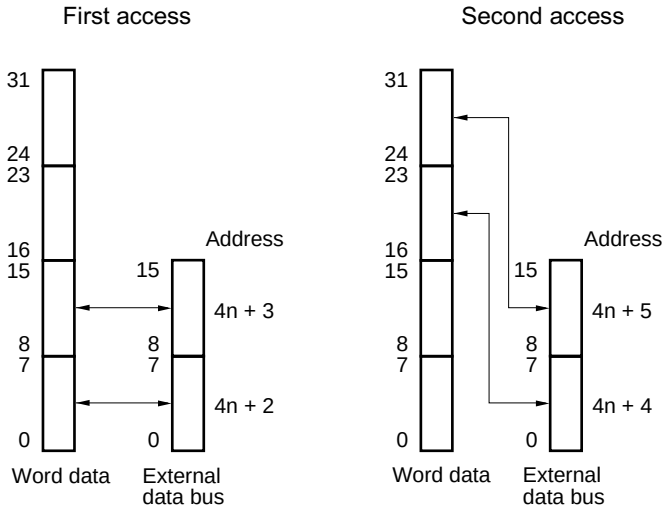


<2> Access to address (4n + 1)

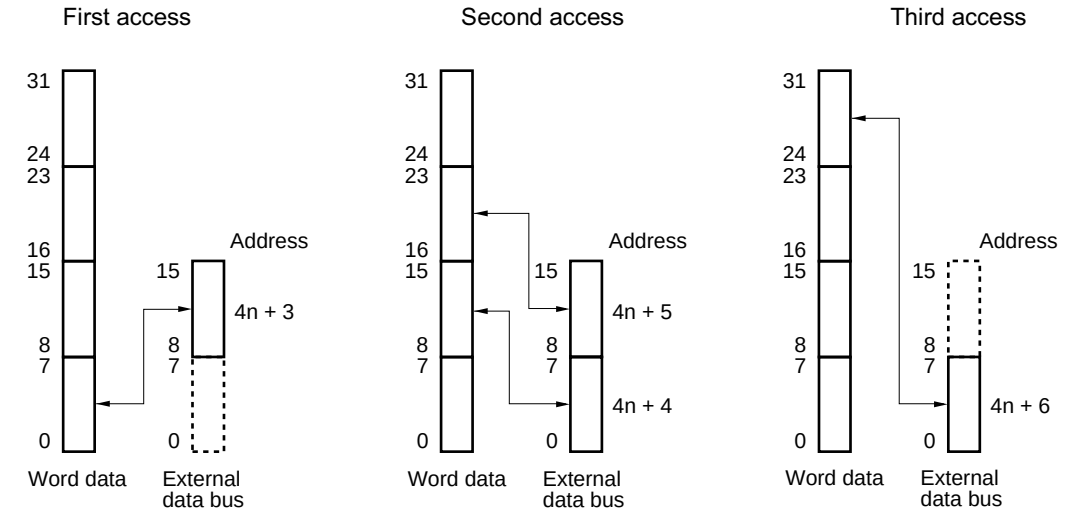


(a) 16-bit data bus width (2/2)

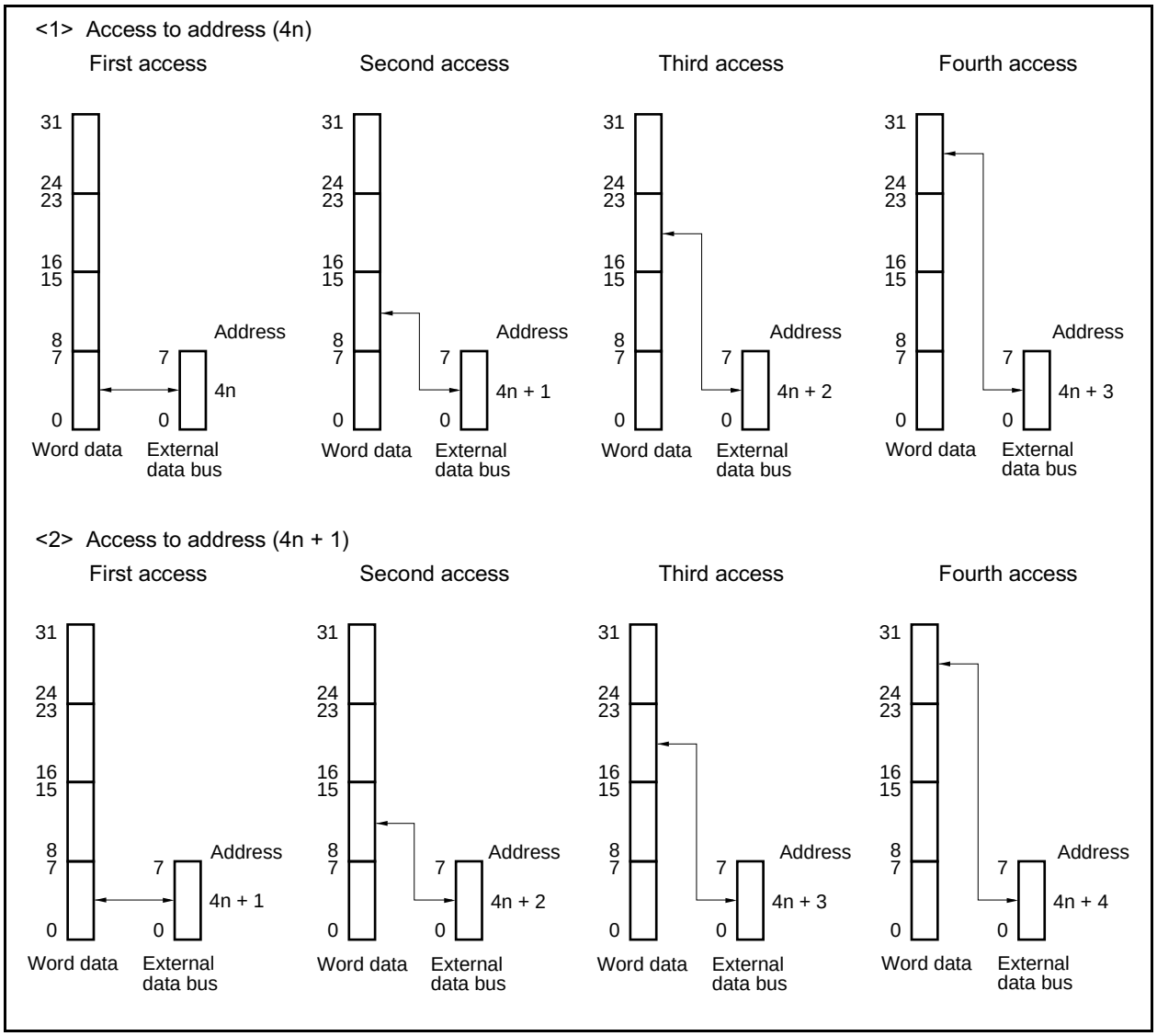
<3> Access to address (4n + 2)



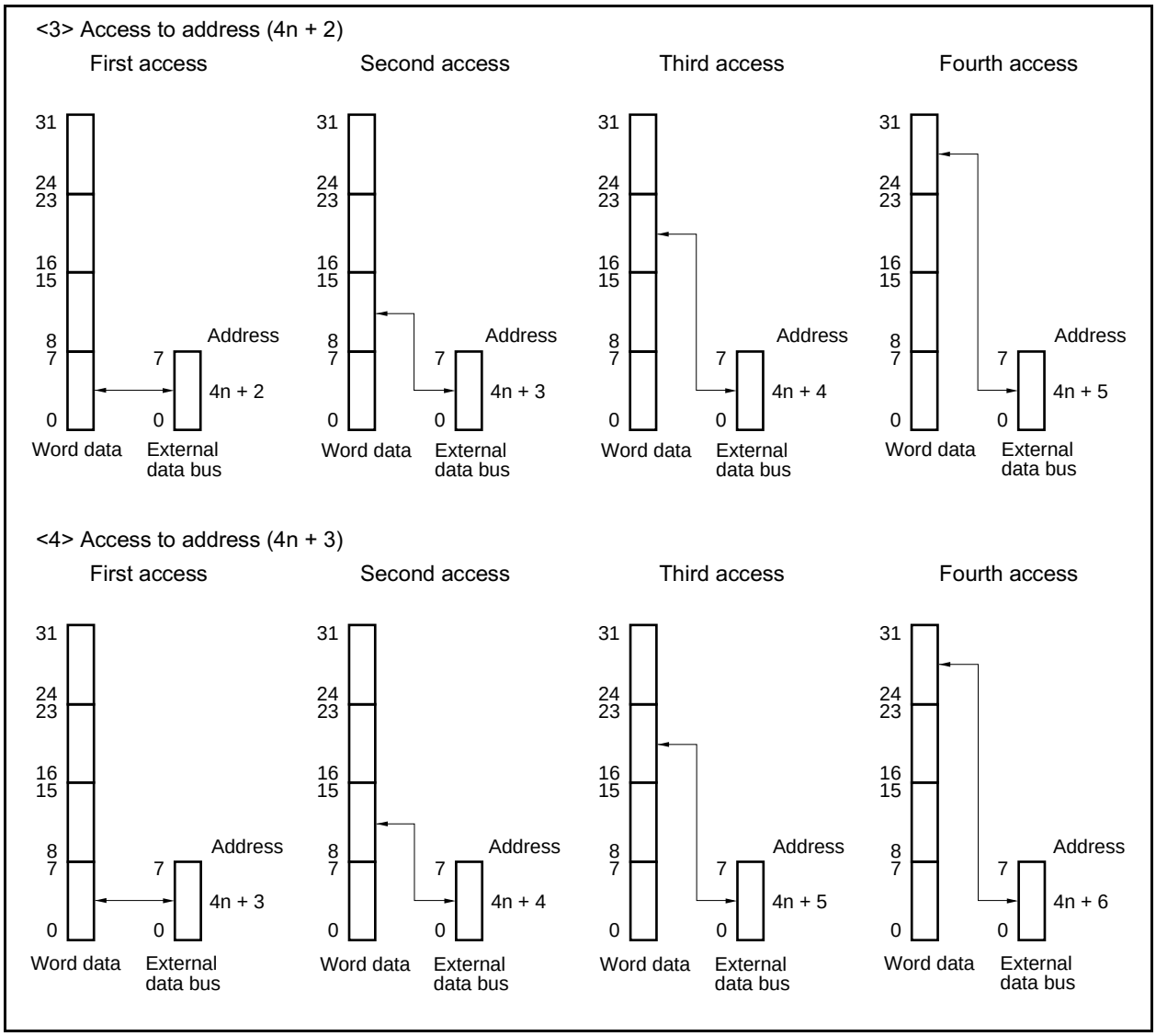
<4> Access to address (4n + 3)



(b) 8-bit data bus width (1/2)



(b) 8-bit data bus width (2/2)



5.6 Wait Function

5.6.1 Programmable wait function

(1) Data wait control register 0 (DWC0)

To realize interfacing with a low-speed memory or I/O, up to seven data wait states can be inserted in the bus cycle that is executed for each CS space.

The number of wait states can be programmed by using data wait control register 0 (DWC0). Immediately after system reset, 7 data wait states are inserted for all the blocks.

The DWC0 register can be read or written in 16-bit units.

Cautions 1. The internal ROM and internal RAM areas are not subject to programmable wait, and are always accessed without a wait state. The on-chip peripheral I/O area is also not subject to programmable wait, and only wait control from each peripheral function is performed.

2. Write to the DWC0 register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the DWC0 register are complete.

After reset: 7777H R/W Address: FFFFF484H

	15	14	13	12	11	10	9	8
DWC0	0	DW32[Note]	DW31[Note]	DW30[Note]	0	DW22[Note]	DW21[Note]	DW20[Note]
$\overline{CSn}$ signal			$\overline{CS3}$				$\overline{CS2}$	

	7	6	5	4	3	2	1	0
	0	DW12	DW11	DW10	0	DW02	DW01	DW00
$\overline{CSn}$ signal			$\overline{CS1}$				$\overline{CS0}$	

DWn2	DWn1	DWn0	Number of wait states inserted in CSn space (n = 0 to 3)
0	0	0	None
0	0	1	1
0	1	0	2
0	1	1	3
1	0	0	4
1	0	1	5
1	1	0	6
1	1	1	7

Note The DW32 to DW30 and DW22 to DW20 bits are only valid in the V850ES/KJ1. Changing these bits has no effect on the operation in the V850ES/KF1 and V850ES/KG1.

Caution Be sure to clear bits 15, 11, 7, and 3 to 0.

5.6.2 External wait function

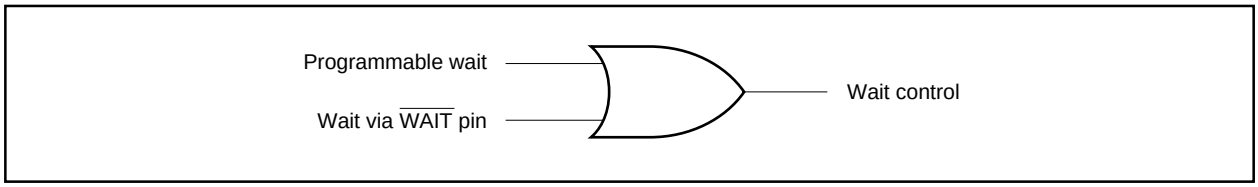
To synchronize an extremely slow external device, I/O, or asynchronous system, any number of wait states can be inserted in the bus cycle by using the external wait pin ($\overline{\text{WAIT}}$).

Access to each area of the internal ROM, internal RAM, and on-chip peripheral I/O is not subject to control by the external wait function, in the same manner as the programmable wait function.

The $\overline{\text{WAIT}}$ signal can be input asynchronously to CLKOUT, and is sampled at the falling edge of the clock in the T2 and TW states of the bus cycle in the multiplex bus mode. In the separate bus mode, it is sampled at the rising edge of the clock immediately after the T1 and TW states of the bus cycle. If the setup/hold time of the sampling timing is not satisfied, a wait state is inserted in the next state, or not inserted at all.

5.6.3 Relationship between programmable wait and external wait

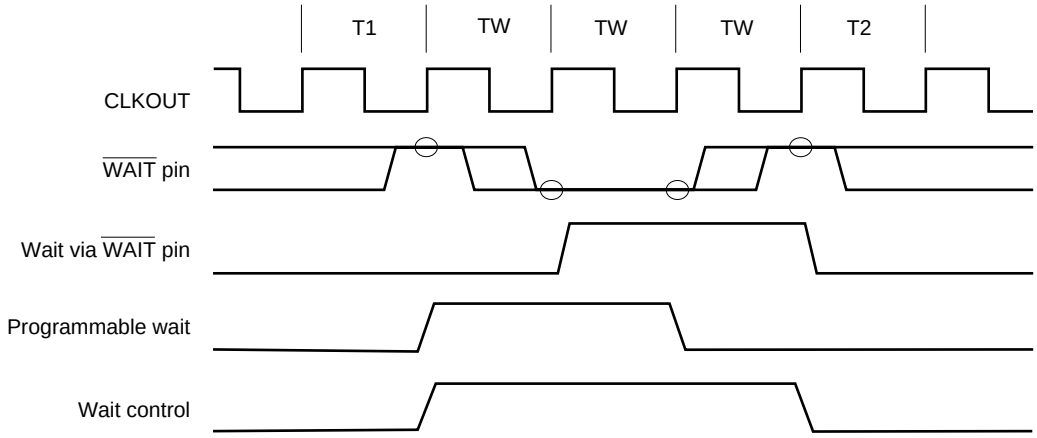
Wait cycles are inserted as the result of an OR operation between the wait cycles specified by the set value of the programmable wait and the wait cycles controlled by the $\overline{\text{WAIT}}$ pin. The number of wait cycles is determined by the side with the greatest number of cycles.



For example, if the timing of the programmable wait and the $\overline{\text{WAIT}}$ pin signal is as illustrated below, three wait states will be inserted in the bus cycle.

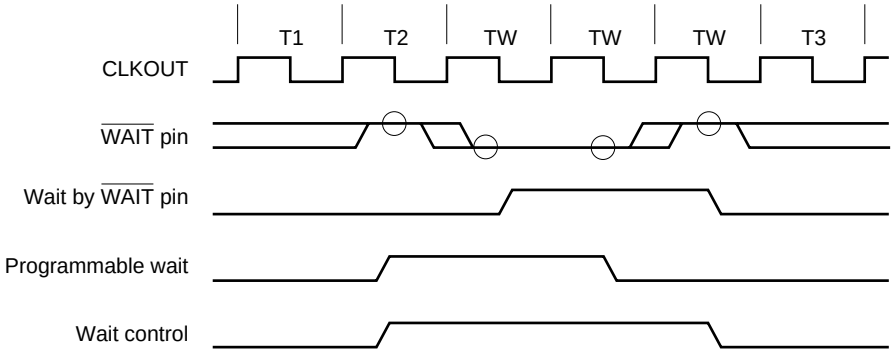
Figure 5-5. Example of Inserting Wait States

(a) In separate bus mode



Remark The circles indicate the sampling timing.

(b) In multiplex bus mode



Remark ○: Valid sampling timing

5.6.4 Programmable address wait function

Address-setup or address-hold waits to be inserted in each bus cycle can be set by using the address wait control register (AWC). Address wait insertion is set for each chip select area ($\overline{CS0}$ to $\overline{CS3}$).

If an address setup wait is inserted, it seems that the high-clock period of T1 state is extended by 1 clock. If an address hold wait is inserted, it seems that the low-clock period of T1 state is extended by 1 clock.

(1) Address wait control register (AWC)

This register can be read or written in 16-bit units.

Cautions 1. The internal ROM, internal RAM, and on-chip peripheral I/O areas are not subject to idle state insertion.

2. Write the AWC register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the AWC register are complete.

After reset: FFFFH R/W Address: FFFFF488H

	15	14	13	12	11	10	9	8
AWC	1	1	1	1	1	1	1	1

7	6	5	4	3	2	1	0
AHW3Note	ASW3Note	AHW2Note	ASW2Note	AHW1	ASW1	AHW0	ASW0

$\overline{CSn}$ signal: $\overline{CS3}$ ($\overline{CS3}$), $\overline{CS2}$ ($\overline{CS2}$), $\overline{CS1}$ ($\overline{CS1}$), $\overline{CS0}$ ($\overline{CS0}$)

AHWn	Specifies insertion of address hold wait (n = 0 to 3)
0	Not inserted
1	Inserted

ASWn	Specifies insertion of address setup wait (n = 0 to 3)
0	Not inserted
1	Inserted

Note The AHW3, AHW2, ASW3, and ASW2 bits are only valid in the V850ES/KJ1. Changing these bits has no effect on the operation in the V850ES/KF1 and V850ES/KG1.

Caution Be sure to set bits 15 to 8 to 1.

5.7 Idle State Insertion Function

To facilitate interfacing with low-speed memories, one idle state (TI) can be inserted after the T3 state in the bus cycle that is executed for each space selected by the memory block function in the multiplex address/data bus mode. In the separate bus mode, one idle state (TI) can be inserted after the T2 state. By inserting idle states, the data output float delay time of the memory can be secured during read access (an idle state cannot be inserted during write access).

Whether the idle state is to be inserted can be programmed by using the bus cycle control register (BCC).

An idle state is inserted for all the areas immediately after system reset.

(1) Bus cycle control register (BCC)

This register can be read or written in 16-bit units.

Cautions 1. The internal ROM, internal RAM, and on-chip peripheral I/O areas are not subject to idle state insertion.

2. Write to the BCC register after reset, and then do not change the set values. Also, do not access an external memory area until the initial settings of the BCC register are complete.

After reset: AAAAH R/W Address: FFFFF48AH

	15	14	13	12	11	10	9	8
BCC	1	0	1	0	1	0	1	0

7	6	5	4	3	2	1	0
BC31[Note]	0	BC21[Note]	0	BC11	0	BC01	0

$\overline{\text{CSn}}$ signal $\overline{\text{CS3}}$ $\overline{\text{CS2}}$ $\overline{\text{CS1}}$ $\overline{\text{CS0}}$

BCn1	Specifies insertion of idle state (n = 0 to 3)
0	Not inserted
1	Inserted

Note The BC31 and BC21 bits are only valid in the V850ES/KJ1. Changing these bits has no effect on the operation in the V850ES/KF1 and V850ES/KG1.

Caution Be sure to set bits 15, 13, 11, and 9 to 1, and clear bits 14, 12, 10, 8, 6, 4, 2, and 0 to 0.

5.8 Bus Hold Function

5.8.1 Functional outline

The $\overline{\text{HLDRQ}}$ and $\overline{\text{HLDAK}}$ functions are valid if the PCM2 and PCM3 pins are set in the control mode.

When the $\overline{\text{HLDRQ}}$ pin is asserted (low level), indicating that another bus master has requested bus mastership, the external address/data bus goes into a high-impedance state and is released (bus hold status). If the request for the bus mastership is cleared and the $\overline{\text{HLDRQ}}$ pin is deasserted (high level), driving these pins is started again.

During the bus hold period, execution of the program in the internal ROM and internal RAM is continued until a peripheral I/O register or the external memory is accessed.

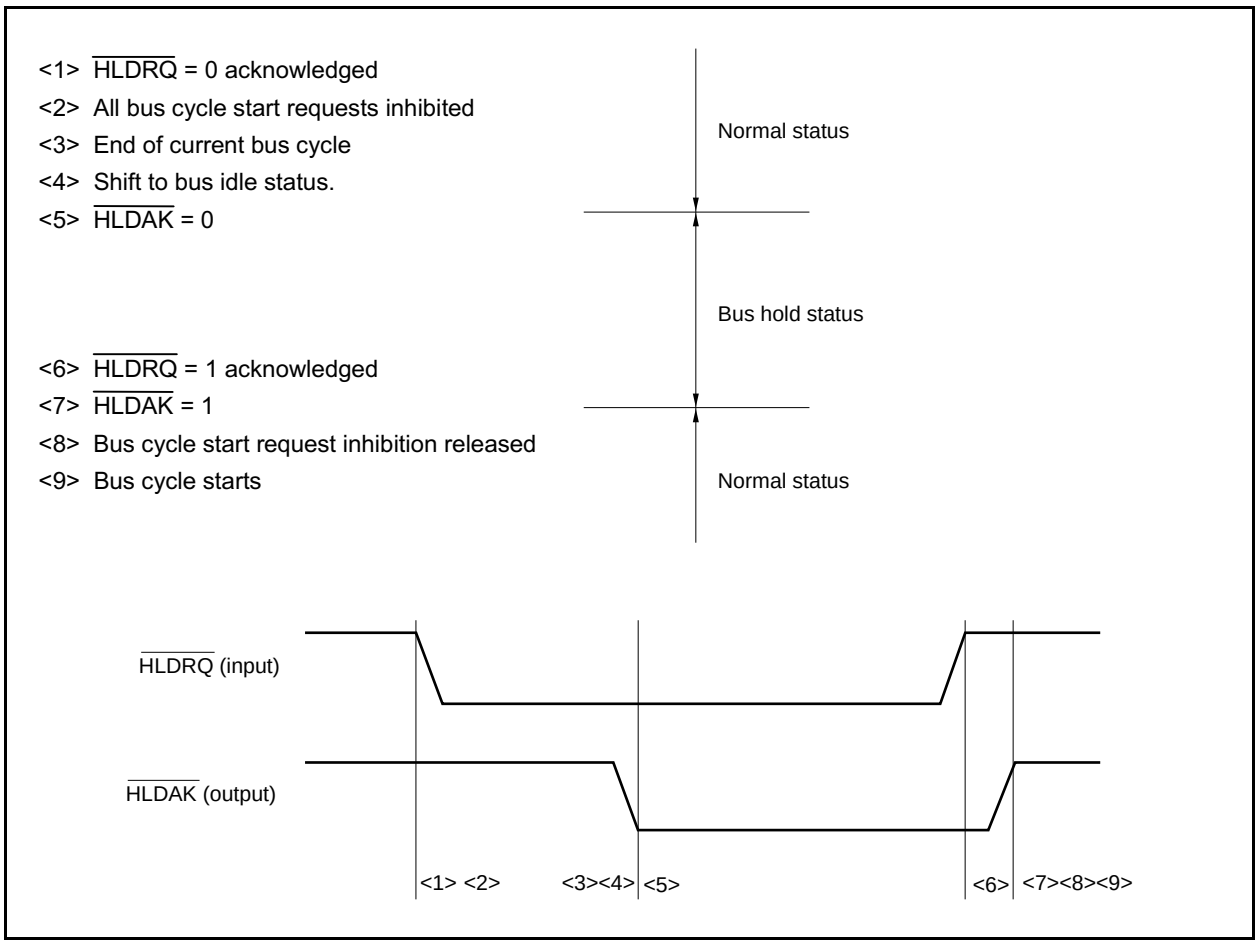
The bus hold status is indicated by assertion (low level) of the $\overline{\text{HLDAK}}$ pin. The bus hold function enables the configuration of multi-processor type systems in which two or more bus masters exist.

Note that the bus hold request is not acknowledged during a multiple-access cycle initiated by the bus sizing function or a bit manipulation instruction.

Status	Data Bus Width	Access Type	Timing in Which Bus Hold Request Not Acknowledged
CPU bus lock	16 bits	Word access to even address	Between first and second access
		Word access to odd address	Between first and second access
			Between second and third access
		Halfword access to odd address	Between first and second access
	8 bits	Word access	Between first and second access
			Between second and third access
			Between third and fourth access
		Halfword access	Between first and second access
Read-modify-write access of bit manipulation instruction	–	–	Between read access and write access

5.8.2 Bus hold procedure

The bus hold status transition procedure is shown below.



5.8.3 Operation in power save mode

Because the internal system clock is stopped in the STOP and IDLE modes, the bus hold status is not entered even if the $\overline{\text{HLDRQ}}$ pin is asserted.

In the HALT mode, the $\overline{\text{HLDAK}}$ pin is asserted as soon as the $\overline{\text{HLDRQ}}$ pin has been asserted, and the bus hold status is entered. When the $\overline{\text{HLDRQ}}$ pin is later deasserted, the $\overline{\text{HLDAK}}$ pin is also deasserted, and the bus hold status is cleared.

5.9 Bus Priority

Bus hold, instruction fetch (branch), instruction fetch (successive), and operand data accesses are executed in the external bus cycle.

Bus hold has the highest priority, followed by operand data access, instruction fetch (branch), and instruction fetch (successive).

An instruction fetch may be inserted between the read access and write access in a read-modify-write access.

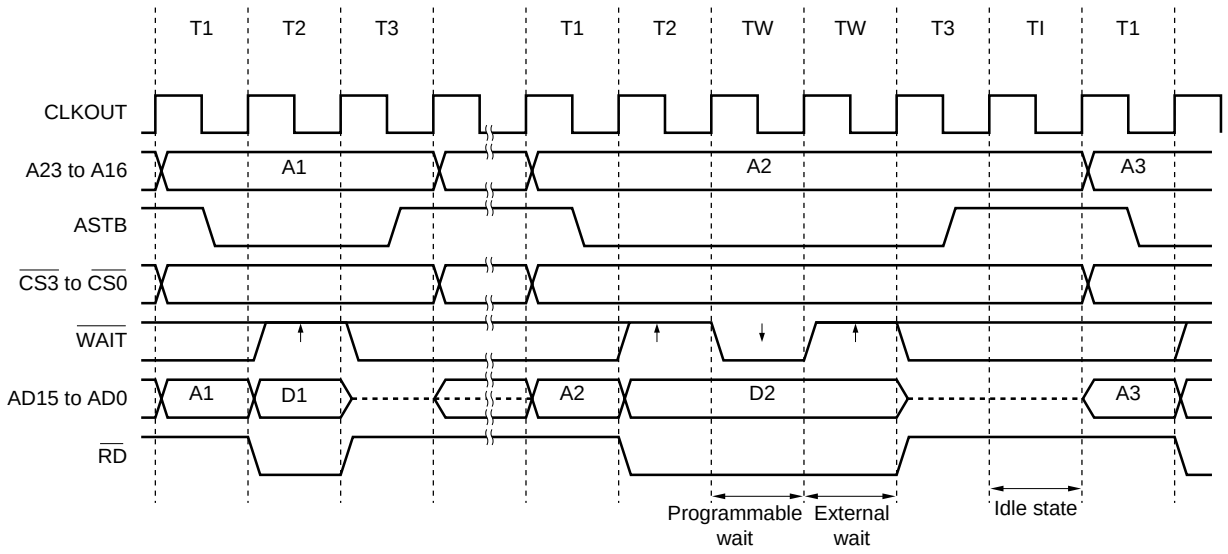
If an instruction is executed for two or more accesses, an instruction fetch and bus hold are not inserted between accesses due to bus size limitations.

Table 5-7. Bus Priority

Priority	External Bus Cycle	Bus Master
High	Bus hold	External device
↕	Operand data access	CPU
↕	Instruction fetch (branch)	CPU
Low	Instruction fetch (successive)	CPU

5.10 Bus Timing

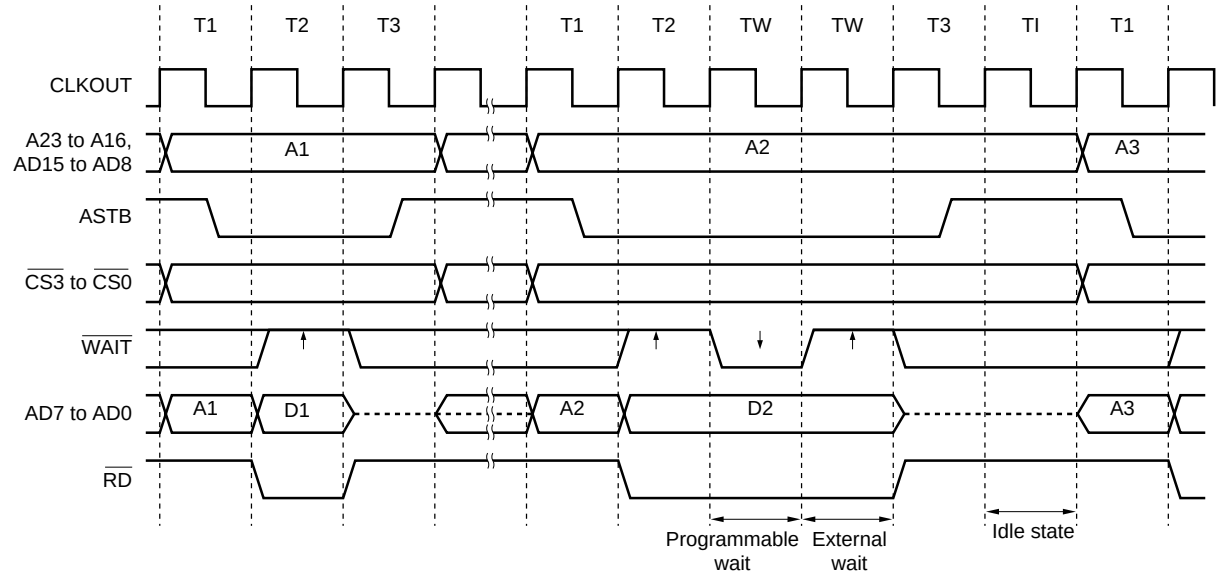
Figure 5-6. Multiplex Bus Read Timing (Bus Size: 16 Bits, 16-Bit Access)



8-bit access	Odd address	Even address
AD15 to AD8	Active	Hi-Z
AD7 to AD0	Hi-Z	Active

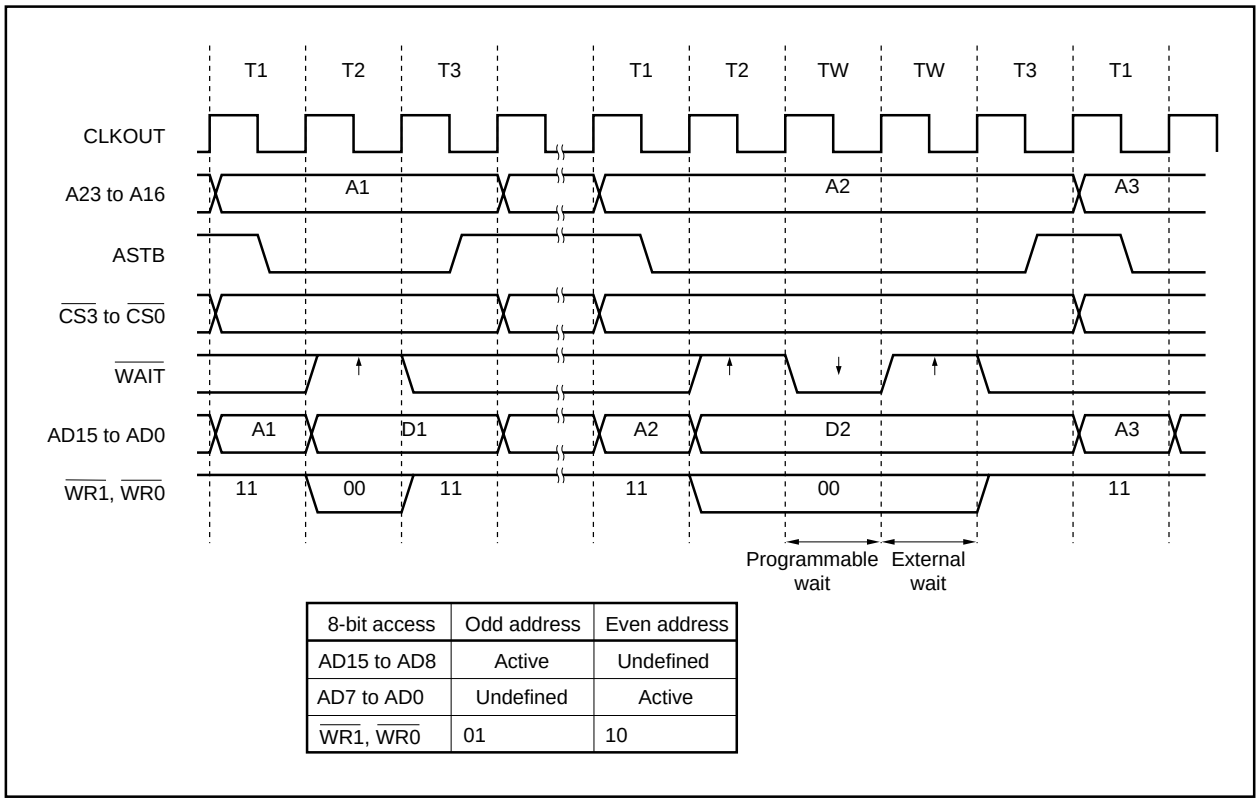
Remark The broken lines indicate high impedance.

Figure 5-7. Multiplex Bus Read Timing (Bus Size: 8 Bits)



Remark The broken lines indicate high impedance.

Figure 5-8. Multiplex Bus Write Timing (Bus Size: 16 Bits, 16-Bit Access)



8-bit access	Odd address	Even address
AD15 to AD8	Active	Undefined
AD7 to AD0	Undefined	Active
WR1, WR0	01	10

Figure 5-9. Multiplex Bus Write Timing (Bus Size: 8 Bits)

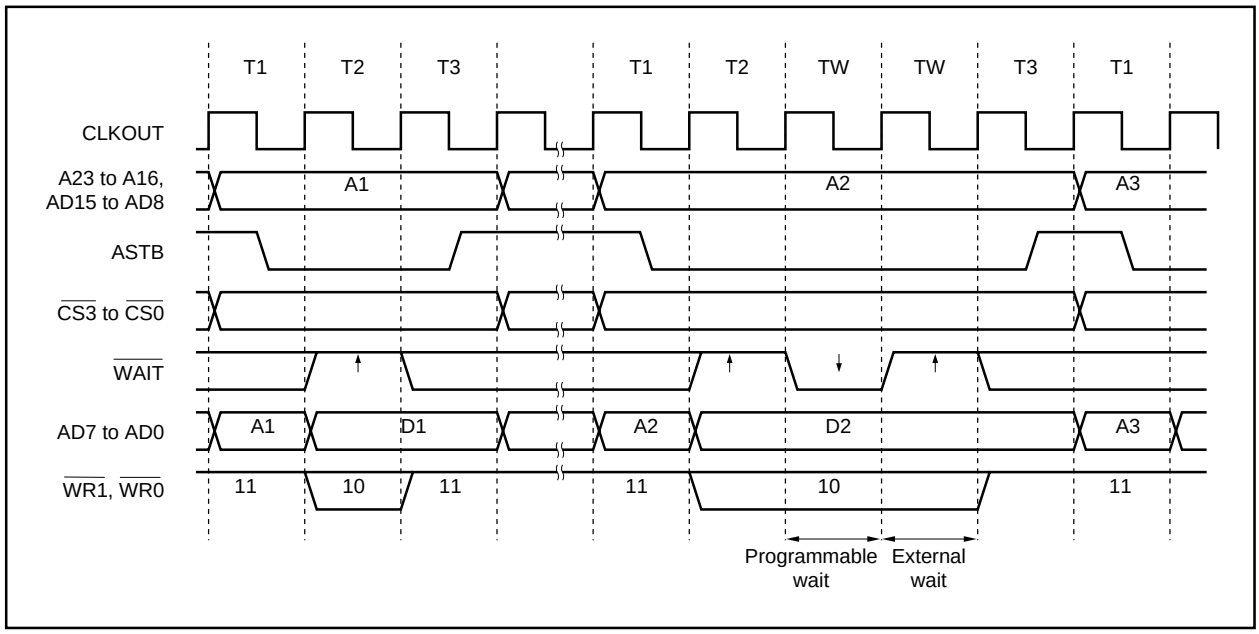
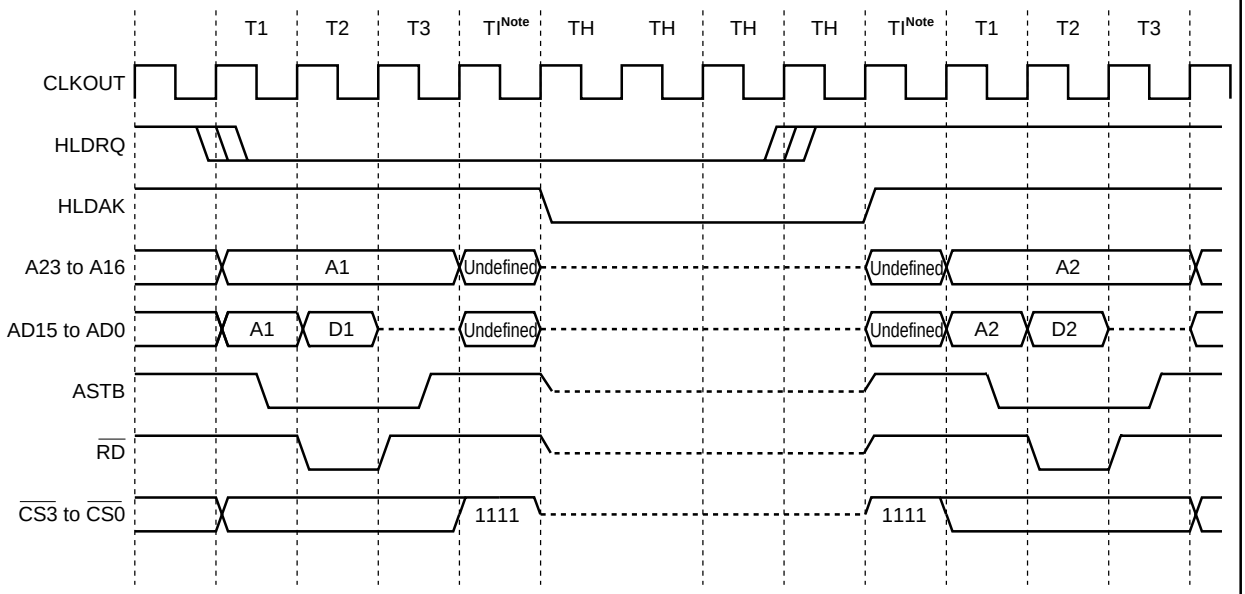


Figure 5-10. Multiplex Bus Hold Timing (Bus Size: 16 Bits, 16-Bit Access)

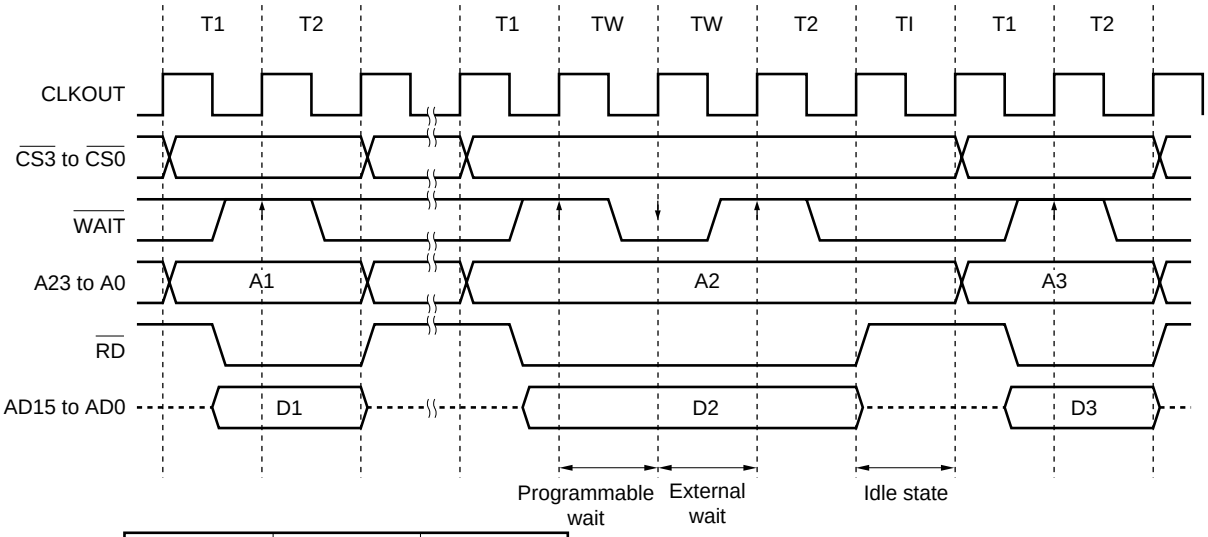


Note This idle state (TI) does not depend on the BCC register settings.

Remarks 1. Refer to **Tables 2-4** to **2-6** for the pin statuses in the bus hold mode.

2. The broken lines indicate high impedance.

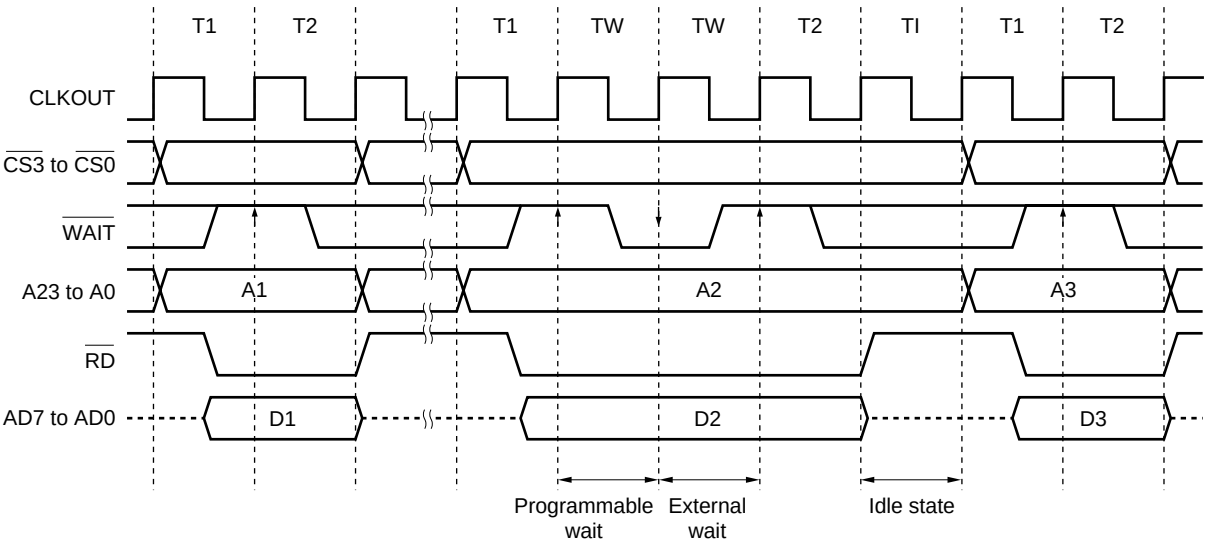
Figure 5-11. Separate Bus Read Timing (Bus Size: 16 Bits, 16-Bit Access)



8-bit access	Odd address	Even address
AD15 to AD8	Active	Hi-Z
AD7 to AD0	Hi-Z	Active

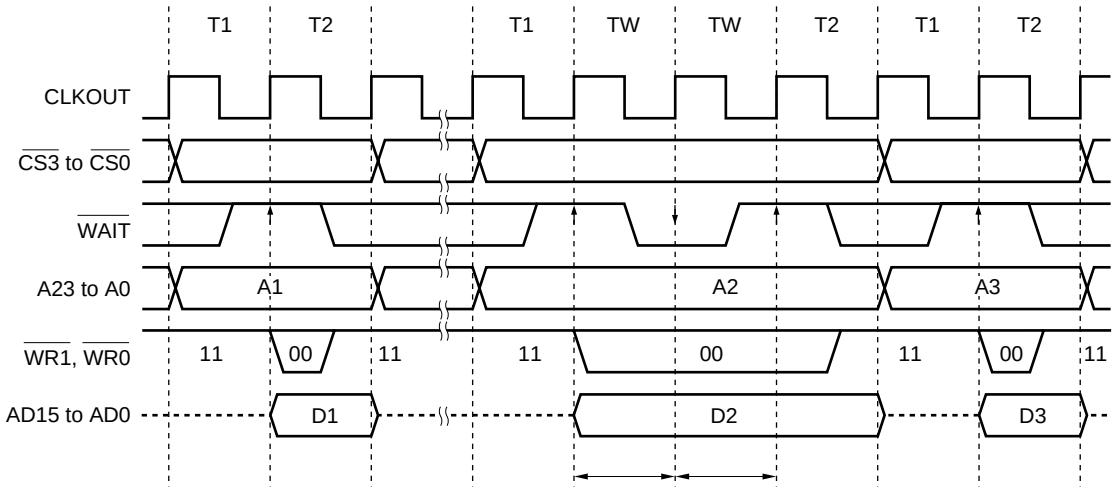
Remark The broken lines indicate high impedance.

Figure 5-12. Separate Bus Read Timing (Bus Size: 8 Bits)



Remark The broken lines indicate high impedance.

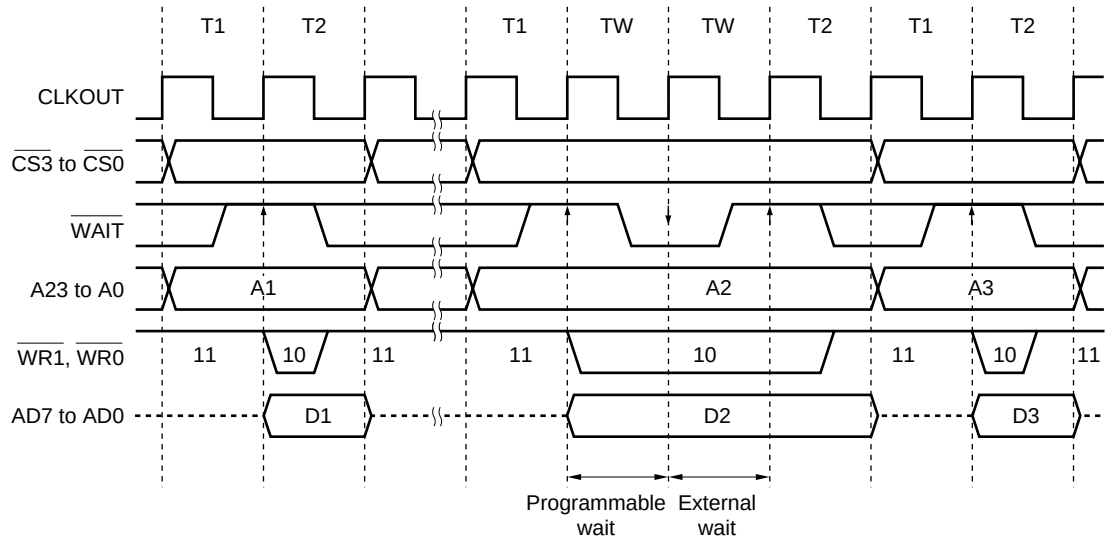
Figure 5-13. Separate Bus Write Timing (Bus Size: 16 Bits, 16-Bit Access)



8-bit access	Odd address	Even address
AD15 to AD8	Active	Undefined
AD7 to AD0	Undefined	Active
WR1, WR0	01	10

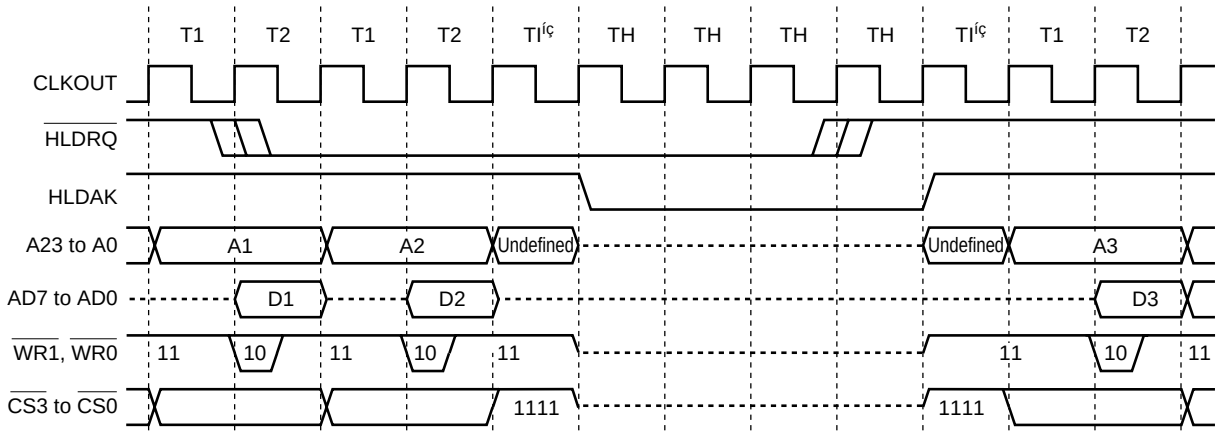
Remark The broken lines indicate high impedance.

Figure 5-14. Separate Bus Write Timing (Bus Size: 8 Bits)



Remark The broken lines indicate high impedance.

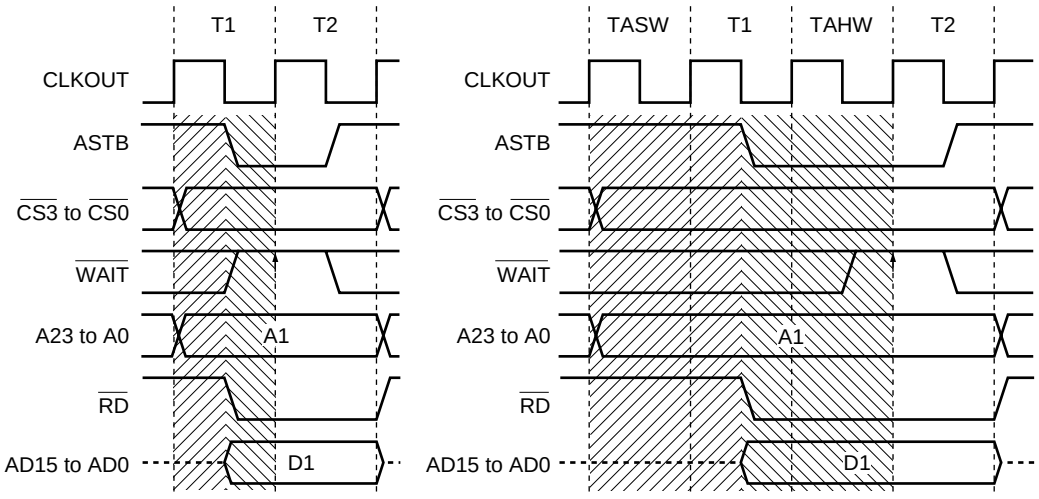
Figure 5-15. Separate Bus Hold Timing (Bus Size: 8 Bits, Write)



Note This idle state (TI) does not depend on the BCC register settings.

Remark The broken lines indicate high impedance.

Figure 5-16. Address Wait Timing (Separate Bus Read, Bus Size: 16 Bits, 16-Bit Access)



Remarks 1. TASW (address setup wait): Image of high-level width of T1 state expanded.

2. TAHW (address hold wait): Image of low-level width of T1 state expanded.

3. The broken lines indicate high impedance.

5.11 Cautions

With the external bus function, signals may not be output at the correct timing under the following conditions.

<Operating conditions>

○ Multiplex bus mode

<1> CLKOUT asynchronous (2.7 V ≤ V_{DD} = EV_{DD} = AV_{REF0} ≤ 5.5 V, 2.7 V ≤ BV_{DD} ≤ 5.5 V)
When 1/f_{CPU} < 84 ns

★ ○ Separate bus mode

<1> Read cycle, CLKOUT asynchronous (4.0 V ≤ V_{DD} = BV_{DD} = EV_{DD} = AV_{REF0} ≤ 5.5 V)
When 1/f_{CPU} < 100 ns

<2> Write cycle, CLKOUT asynchronous (4.0 V ≤ V_{DD} = BV_{DD} = EV_{DD} = AV_{REF0} ≤ 5.5 V)
When 1/f_{CPU} < 60 ns

<3> Read cycle, CLKOUT asynchronous (2.7 V ≤ V_{DD} = BV_{DD} = EV_{DD} = AV_{REF0} ≤ 5.5 V)
When 1/f_{CPU} < 200 ns

<4> Write cycle, CLKOUT asynchronous (2.7 V ≤ V_{DD} = BV_{DD} = EV_{DD} = AV_{REF0} ≤ 5.5 V)
When 1/f_{CPU} < 100 ns

<Countermeasure>

When used under the above conditions, be sure to insert an address setup/hold wait using the address wait control register (AWC) (n = 0 to 3).

○ When used in multiplex bus mode and under condition <1>

- 70 ns < 1/f_{CPU} < 84 ns
  Set an address setup wait (ASWn bit = 1).
- 62.5 ns < 1/f_{CPU} < 70 ns
  Set an address setup wait (ASWn bit = 1) and address hold wait (AHWn bit = 1).

○ When used in separate bus mode and under conditions <1> to <4>

Set an address setup wait (ASWn bit =1).

CHAPTER 6 CLOCK GENERATION FUNCTION

6.1 Overview

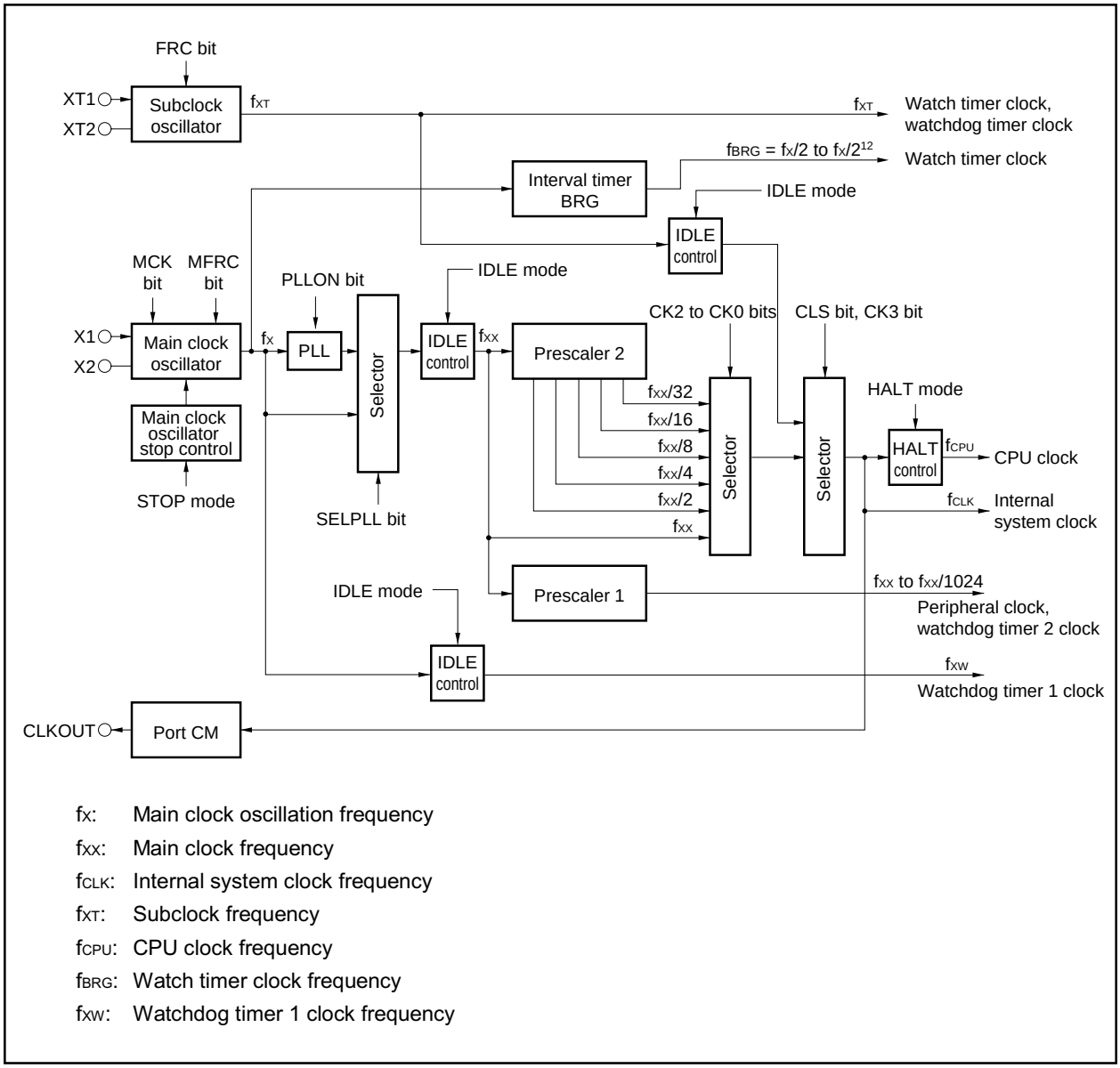
The following clock generation functions are available.

- ○ Main clock oscillator
  - f_X = 2 to 2.5 MHz (f_{XX} = 8 to 10 MHz, REGC = V_{DD} = 2.7 to 5.5 V, in PLL mode)
  - f_X = 2 to 5 MHz (f_{XX} = 8 to 20 MHz, REGC = V_{DD} = 4.5 to 5.5 V, in PLL mode)
  - f_X = 2 to 4 MHz (f_{XX} = 8 to 16 MHz, REGC = capacitor, V_{DD} = 4.0 to 5.5 V, in PLL mode)
  - f_X = 2 to 10 MHz (f_{XX} = 2 to 10 MHz, REGC = V_{DD} = 2.7 to 5.5 V, in clock-through mode)
- ○ Subclock oscillator
  - 32.768 kHz
- ○ Multiplication (×4) function by PLL (Phase Locked Loop)
  - Clock-through mode/PLL mode selectable
  - Usable voltage: V_{DD} = 2.7 to 5.5 V
- ○ Internal system clock generation
  - 7 steps (f_{XX}, $f_{XX}/2$, $f_{XX}/4$, $f_{XX}/8$, $f_{XX}/16$, $f_{XX}/32$, f_{XT})
- ○ Peripheral clock generation
- ○ Clock output function

Remark f_X: Main clock oscillation frequency
f_{XX}: Main clock frequency

6.2 Configuration

Figure 6-1. Clock Generator



fX: Main clock oscillation frequency
fXX: Main clock frequency
fCLK: Internal system clock frequency
fXT: Subclock frequency
fCPU: CPU clock frequency
fBRG: Watch timer clock frequency
fXW: Watchdog timer 1 clock frequency

(1) Main clock oscillator

The main clock oscillator oscillates the following frequencies (f_X):

- f_X = 2 to 2.5 MHz (REGC = V_{DD} = 2.7 to 5.5 V, in PLL mode)
- f_X = 2 to 5 MHz (REGC = V_{DD} = 4.5 V to 5.5 V, in PLL mode)
- f_X = 2 to 4 MHz (REGC = capacitor, V_{DD} = 4.0 to 5.5 V, in PLL mode)
- f_X = 2 to 10 MHz (REGC = V_{DD} = 2.7 to 5.5 V, in clock-through mode)

(2) Subclock oscillator

The subclock oscillator oscillates a frequency of 32.768 kHz (f_{XT}).

(3) Main clock oscillator stop control

This circuit generates a control signal that stops oscillation of the main clock oscillator.

Oscillation of the main clock oscillator is stopped in the STOP mode or when the MCK bit of the PCC register = 1 (valid only when the CLS bit of the PCC register = 1).

(4) Prescaler 1

This prescaler generates the clock (f_{XX} to f_{XX}/1024) to be supplied to the following on-chip peripheral functions: TM00 to TM05, TM50, TM51, TMH0, TMH1, CSI00 to CSI02, CSIA0, CSIA1, UART0 to UART2, I^2C0, I^2C1, ADC, DAC, and WDT2

(5) Prescaler 2

This circuit divides the CPU clock (f_{CPU}) and main clock (f_{XX}).

The clock generated by prescaler 2 (f_{XX} to f_{XX}/32) is supplied to the selector that generates the internal system clock (f_{CLK}).

f_{CLK} is the clock supplied to the INTC, ROM correction, ROM, and RAM blocks, and can be output from the CLKOUT
pin.

(6) Interval timer BRG

This circuit divides the clock (f_X) generated by the main clock oscillator to a specific frequency (32.768 kHz) and supplies that clock to the watch timer block.

For details, refer to **CHAPTER 10 INTERVAL TIMER, WATCH TIMER**.

(7) PLL

This circuit multiplies the clock (f_X) generated by the main clock oscillator.

It operates in two modes: clock-through mode in which f_X is output as is, and PLL mode in which a multiplied clock is output. These modes can be selected by using the SELPLL bit of the PLL control register (PLLCTL).

Operation of the PLL can be started or stopped by the PLLON bit of the PLLCTL register.

6.3 Control Registers

(1) Processor clock control register (PCC)

The processor clock control register (PCC) is a special register. Data can be written to this register only in combination of specific sequences (refer to **3.4.7 Special registers**).

This register can be read or written in 8-bit or 1-bit units.

(1/2)

After reset: 03H R/W After reset: FFFFF828H

	7	6	5	4	3	2	1	0
PCC	FRC	MCK	MFRC	CLS[Note]	CK3	CK2	CK1	CK0

FRC	Use of subclock on-chip feedback resistor
0	Used
1	Not used

MCK	Control of main clock oscillator
0	Oscillation enabled
1	Oscillation stopped

- Even if the MCK bit is set to 1 while the system is operating with the main clock as the CPU clock, the operation of the main clock does not stop. It stops after the CPU clock has been changed to the subclock.
- When the main clock is stopped and the device is operating on the subclock, clear the MCK bit to 0 and wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

MFRC	Use of main clock on-chip feedback resistor
0	Used
1	Not used

CLS[Note]	Status of CPU clock (f_{CPU})
0	Main clock operation
1	Subclock operation

Note The CLS bit is a read-only bit.

(2/2)

CK3	CK2	CK1	CK0	Clock selection (f_{CLK}/f_{CPU})
0	0	0	0	f_{XX}
0	0	0	1	$f_{XX}/2$
0	0	1	0	$f_{XX}/4$
0	0	1	1	$f_{XX}/8$ (default value)
0	1	0	0	$f_{XX}/16$
0	1	0	1	$f_{XX}/32$
0	1	1	×	Setting prohibited
1	×	×	×	f_{XT}

Cautions 1. Do not change the CPU clock (by using the CK3 to CK0 bits of the PCC register) while CLKOUT is being output.

2. Use a bit manipulation instruction to manipulate the CK3 bit. When using an 8-bit manipulation instruction, do not change the set values of the CK2 to CK0 bits.

3. When the CPU operates on the subclock and no clock is input to the X1 pin, do not access a register in which a wait occurs using an access method that causes a wait (refer to 3.4.8 (2) Access to special on-chip peripheral I/O register for details of the access methods). If a wait occurs, it can only be released by a reset.

Remark ×: Don't care

★ **(a) Example of setting main clock operation → subclock operation**

<1> CK3 bit ← 1: Use of a bit manipulation instruction is recommended. Do not change the CK2 to CK0 bits.

<2> Subclock operation: Read the CLS bit to check if subclock operation has started. It takes the following time after the CK3 bit is set until subclock operation is started.

Max.: $1/f_{XT}$ (1/subclock frequency)

<3> Set the MCK bit to 1 only when stopping the main clock.

Cautions 1. When stopping the main clock, stop the PLL.

2. If the following conditions are not satisfied, change the CK2 to CK0 bits so that the conditions are satisfied, then change to the subclock operation mode.

Main clock (f_{XX}) > Subclock (f_{XT}: 32.768 kHz) × 4

[Description example]

```
<1> _SET_SUB_RUN :
    st.b        r0, PRCMD[r0]
    set1        3, PCC[r0]          -- CK3 bit ← 1
<2> _CHECK_CLS :
    tst1        4, PCC[r0]          -- Wait until subclock operation starts.
    bz          _CHECK_CLS
<3> _STOP_MAIN_CLOCK :
    st.b        r0, PRCMD[r0]
    set1        6, PCC[r0]          -- MCK bit ← 1, main clock is stopped
```

★ **(b) Example of setting subclock operation → main clock operation**

<1> MCK bit ← 1: Main clock starts oscillating

<2> Insert waits by the program and wait until the oscillation stabilization time of the main clock elapses.

<3> CK3 bit ← 1: Use of a bit manipulation instruction is recommended. Do not change the CK2 to CK0 bits.

<4> Main clock operation: It takes the following time after the CK3 bit is set until main clock operation is started.

Max.: 1/f_{XT} (1/subclock frequency)

Therefore, insert one NOP instruction immediately after setting the CK3 bit to 0 or read the CLS bit to check if main clock operation has started.

[Description example]

```
<1> _START_MAIN_OSC :
    st.b        r0, PRCMD[r0]       -- Release of protection of special registers
    clr1        6, PCC[r0]          -- Main clock starts oscillating
<2> movea       0x55, r0, r11       -- Wait for oscillation stabilization time
    _WAIT_OST :
    nop
    nop
    nop
    addi        -1, r11, r11
    mp          r0, r11
    bne         _PROGRAM_WAIT
<3> st.b        r0, PRCMD[r0]
    clr1        3, PCC[r0]          -- CK3 ← 0
<4> _CHECK_CLS :
    tst1        4, PCC[r0]          -- Wait until main clock operation starts
    bnz         _CHECK_CLS
```

6.4 Operation

6.4.1 Operation of each clock

The following table shows the operation status of each clock.

Table 6-1. Operation Status of Each Clock

Register Setting and Operation Status / Target Clock	CLK bit = 0, MCK bit = 0					CLS bit = 1, MCK bit = 0		CLS bit = 1, MCK bit = 1	
	During reset	During oscillation stabilization time count	HALT mode	IDLE mode	STOP mode	Subclock mode	Sub-IDLE mode	Subclock mode	Sub-IDLE mode
Main clock oscillator (f_X)	×	○	○	○	×	○	○	×	×
Subclock oscillator (f_{XT})	○	○	○	○	○	○	○	○	○
CPU clock (f_{CPU})	×	×	×	×	×	○	×	○	×
Internal system clock (f_{CLK})	×	×	○	×	×	○	×	○	×
Peripheral clock (f_{XX} to f_{XX}/1024)	×	×	○	×	×	○	×	×	×
WT clock (main)	×	○	○	○	×	○	○	×	×
WT clock (sub)	○	○	○	○	○	○	○	○	○
WDT1 clock (f_{XW})	×	○	○	○	×	○	○	×	×
WDT2 clock (main)	×	×	○	×	×	○	×	×	×
WDT2 clock (sub)	○	○	○	○	○	○	○	○	○

Remark CLS bit: Bit 4 of the processor clock control register (PCC)
MCK bit: Bit 6 of the PCC register
○: Operable
×: Stopped

6.4.2 Clock output function

The clock output function is used to output the internal system clock (f_{CLK}) from the CLKOUT pin.

The internal system clock (f_{CLK}) is selected by using the CK3 to CK0 bits of the processor clock control register (PCC).

The CLKOUT pin functions alternately as the PCM1 pin and functions as a clock output pin if so specified by the control register of port CM.

The status of the CLKOUT pin is the same as the internal system clock in Table 6-1 and the pin can output the clock when it is in the operable status. It outputs a low level in the stopped status. However, the port mode (PCM1: input mode) is selected until the CLKOUT pin output is set after reset. Consequently, the CLKOUT pin goes into a high-impedance state.

6.4.3 External clock input function

An external clock can be directly input to the oscillator. Input the clock to the X1 pin and its inverse signal to the X2 pin. Set the MFRC bit of the PCC register to 1 (on-chip feedback resistor not used). Note, however, that oscillation stabilization time is inserted even in the external clock mode. Connect V_{DD} directly to the REGC pin.

6.5 PLL Function

6.5.1 Overview

The PLL function is used to output the operating clock of the CPU and peripheral macro at a frequency 4 times higher than the oscillation frequency, and select the clock-through mode.

When PLL function is used: Input clock = 2 to 5 MHz (f_{XX}: 8 to 20 MHz)
(usable voltage: V_{DD} = 2.7 to 5.5 V)
Clock-through mode: Input clock = 2 to 10 MHz (f_{XX}: 2 to 10 MHz)

6.5.2 Control register

(1) PLL control register (PLLCTL)

This 8-bit register controls the PLL function.
This register can be read or written in 8-bit or 1-bit units.
After reset, PLLCTL is set to 01H.

After reset: 01H R/W Address: FFFFF806H

	7	6	5	4	<3>	<2>	<1>	<0>
PLLCTL	0	0	0	0	RTOST1[Note]	RTOST0[Note]	SELPLL	PLLON

PLLON	PLL operation stop register
0	PLL stopped
1	PLL operating

SELPLL	PLL clock selection register
0	Clock-through operation
1	PLL operation

Note For the RTOST1 and RTOST2 bits, refer to **CHAPTER 12 REAL-TIME OUTPUT FUNCTION (RTO)**.

Caution Be sure to set bits 4 to 7 to 0.

6.5.3 Usage

(1) To use PLL

- After reset has been released, the PLL operates (PLLON = 1), but because the default mode is the clock-through mode (SELPLL = 0), select the PLL mode (SELPLL = 1).
- To set the STOP mode in which the main clock is stopped, or to set the IDLE mode, first select the clock-through mode and then stop the PLL. To return from the IDLE or STOP mode, first enable PLL operation (PLLON = 1), and then select the PLL mode (SELPLL = 1).
- To enable the PLL operation, first set PLLON to 1, wait for 200 μs, and then set PLLSEL to 1. To stop the PLL, first select the clock-through mode (SELPLL = 0), wait for 8 clocks or more, and then stop the PLL (PLLON = 0).

(2) When PLL is not used

- The clock-through mode (SELPLL = 0) is selected after the $\overline{\text{RESET}}$ has been released, but the PLL is operating (PLLON = 1) and must therefore be stopped (PLLON = 0).

Remark The PLL is operable in the IDLE mode. To realize low power consumption, stop the PLL. Be sure to stop the PLL when shifting to the STOP mode.

CHAPTER 7 16-BIT TIMER/EVENT COUNTERS 00 TO 05

The number of 16-bit timer/event counter 00 to 05 channels incorporated differs as follows depending on the product.

Product Name	V850ES/KF1	V850ES/KG1	V850ES/KJ1
Number of channels	2 channels (TM00, TM01)	4 channels (TM00 to TM03)	6 channels (TM00 to TM05)

7.1 Functions

16-bit timer/event counters 00 to 05 have the following functions.

(1) Interval timer
Generates an interrupt at predetermined time intervals.

(2) PPG output
Can output a rectangular wave with any frequency and any output pulse width.

(3) Pulse width measurement
Can measure the pulse width of a signal input from an external source.

(4) External event counter
Can measure the pulse width of a signal input from an external source.

(5) Square-wave output
Can output a square wave of any frequency.

(6) One-shot pulse output (16-bit timer/event counters 00, 01, 04 and 05 only)
Can output a one-shot pulse with any output pulse width.

7.2 Configuration

16-bit timer/event counters 00 to 05 consist of the following hardware.

Table 7-1. Configuration of 16-Bit Timer/Event Counters 00 to 05

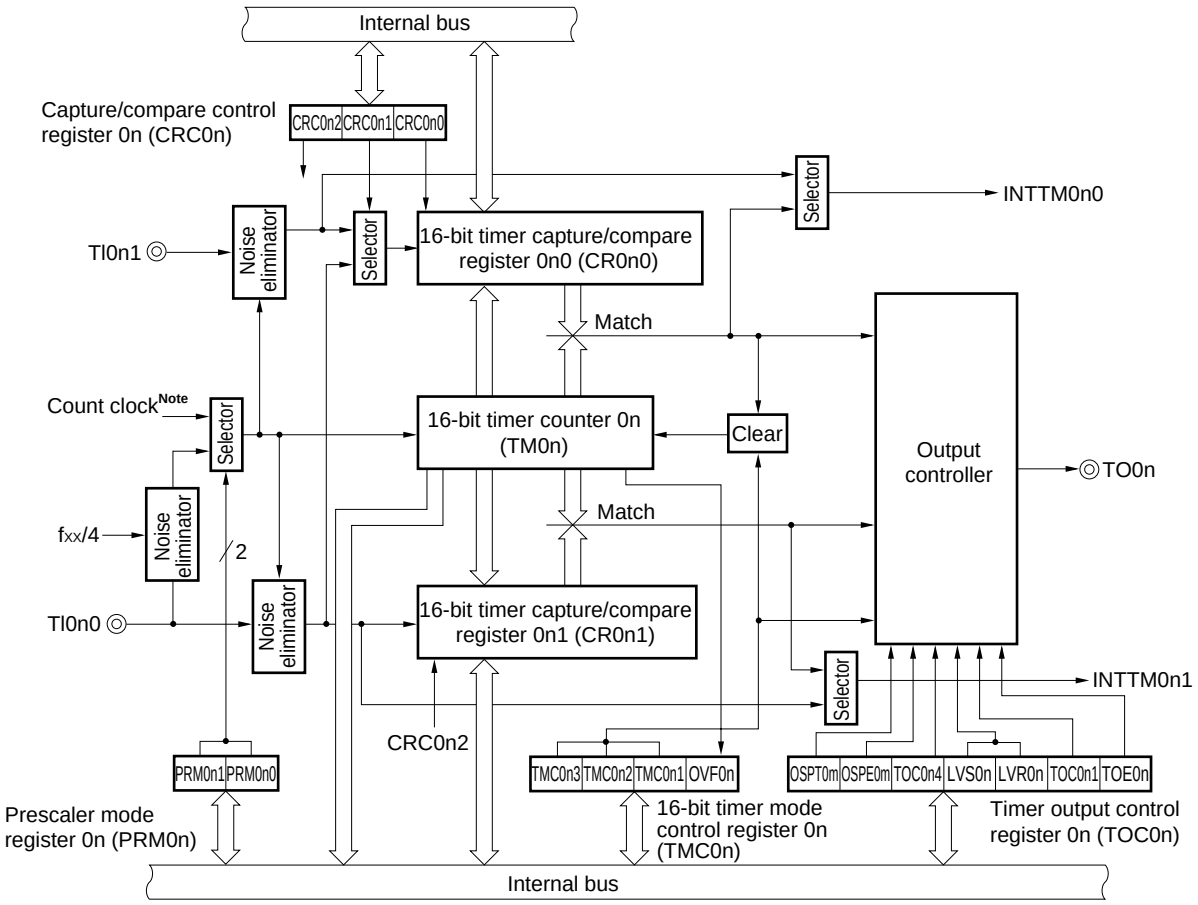
Item	Configuration
Timer/counters	16 bits × 1 (TM0n)
Registers	16-bit timer capture/compare register: 16 bits × 2 (CR0n0, CR0n1)
Timer inputs	2 (TI0N0, TI0n1)
Timer outputs	1 (TO0n), output controller
Control registers[Note]	16-bit timer mode control register n (TMC0n) Capture/compare control register n (CRC0n) 16-bit timer output control register (TOC0n) Prescaler mode register 0n (PRM0n)

Note To use the TI0n0, TI0n1, and TO0n pin functions, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

Remark n = 0 to 5

Figure 7-1 shows the block diagram.

Figure 7-1. Block Diagram of 16-Bit Timer/Event Counter 0n



Note Set by the PRM0n register.

Remarks 1. n = 0 to 5 m = 0, 1, 4, 5

2. fxx: Main clock frequency

(1) 16-bit timer counter 0n (TM0n)

The TM0n register is a 16-bit read-only register that counts count pulses. The counter is incremented in synchronization with the rising edge of the input clock.

After reset: 0000H R Address: TM00: FFFFF600H, TM01: FFFFF610H,
TM02: FFFFF620H, TM03: FFFFF630H,
TM04: FFFFF640H, TM05: FFFFF650H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
TM0n																

(n = 0 to 5)

The count value is reset to 0000H in the following cases.

<1> Reset
<2> If the TMC0n3 and TMC0n2 bits are cleared.
<3> If the valid edge of TI0n0 is input in the mode in which clear & start occurs when inputting the valid edge of TI0n0
<4> If the TM0n register and the CR0n0 register match each other in the mode in which clear & start occurs on CR0n0 register match
<5> If the OSPT0m bit is set or if the valid edge of TI0k0 is input in the one-shot pulse output mode

Remark n = 0 to 5
m = 0, 1, 4, 5
k = 4, 5

(2) 16-bit timer capture/compare register 0n0 (CR0n0)

The CR0n0 register is a 16-bit register that combines capture register and compare register functions.
The CRC0n.CRC0n0 bit is used to set whether to use the CR0n0 register as a capture register or as a compare register.
The CR0n0 register is set by a 16-bit memory manipulation instruction.
After reset, this register is cleared to 0000H.

After reset: 0000H R/W Address: CR000: FFFFF602H, CR010: FFFFF612H,
CR020: FFFFF622H, CR030: FFFFF632H,
CR040: FFFFF642H, CR050: FFFFF652H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR0n0																

(n = 0 to 5)

(a) When using the CR0n0 register as a compare register

The value set to the CR0n0 register and the count value set to the TM0n register are always compared and when these values match, an interrupt request signal (INTTM0n0) is generated. The values are retained until rewritten.

(b) When using the CR0n0 register as a capture register

The TM0n register count value is captured to the CR0n0 register by inputting a capture trigger.

The valid edge of the TI0n0 pin or TI0n1 pin can be selected as the capture trigger. The valid edge of the TI0n0 pin or TI0n1 pin is set with the PRM0n.ESn01 and PRM0n.ESn00 bits or PRM0n.ESn11 and PRM0n.ESn10 bits.

Table 7-2 shows the settings when the valid edge of the TI0n0 pin is specified as the capture trigger, and Table 7-3 shows the settings when the valid edge of the TI0n1 is specified as the capture trigger.

Table 7-2. Capture Trigger of CR0n0 Register and Valid Edge of TI0n0 Pin

Capture Trigger of CR0n0	Valid Edge of TI0n0 Pin		
		ESn01	ESn00
Falling edge	Rising edge	0	1
Rising edge	Falling edge	0	0
No capture operation	Both rising and falling edges	1	1

Remarks 1. n = 0 to 5

2. Setting the ESn01 and ESn00 bits to 10 is prohibited.

Table 7-3. Capture Trigger of CR0n0 Register and Valid Edge of TI0n1 Pin

Capture Trigger of CR0n0	Valid Edge of TI0n1 Pin		
		ESn11	ESn10
Falling edge	Falling edge	0	0
Rising edge	Rising edge	0	1
Both rising and falling edges	Both rising and falling edges	1	1

Remarks 1. n = 0 to 5

2. Setting the ESn11 and ESn10 bits to 10 is prohibited.

Cautions 1. Set a value other than 0000H to the CR0n0 register in the mode in which clear & start occurs upon a match of the values of the TM0n register and CR0n0 register. However, if 0000H is set to the CR0n0 register in the free-running mode or the TI0n0 valid edge clear mode, an interrupt request (INTTM0n0) is generated when the value changes from 0000H to 0001H after an overflow (FFFFH).

2. When the P33, P35, P613, P92, and P94 pins are used as the valid edges of TI000, TI010, TI020, TI030, and TI051, they cannot be used as timer outputs (TO00 to TO03, TO05). Moreover, when used as TO00 to TO03 and TO05, these pins cannot be used as the valid edge of TI000, TI010, TI020, TI030, and TI051.

3. If, when the CR0n0 register is used as a capture register, the register read interval and capture trigger input conflict, the read data becomes undefined (but the capture data itself is normal). Moreover, when the count stop input and capture trigger input conflict, the capture data becomes undefined.

4. The CR0n0 register cannot be rewritten during TM0n register operation.

(3) 16-bit timer capture/compare register 0n1 (CR0n1)

The CR0n1 register is a 16-bit register that combines capture register and compare register functions. Bit 2 (CRC0n2) of the CRC0n register is used to set whether to use the CR0n1 register as a capture register or as a compare register.

The CR0n1 register is set by a 16-bit memory manipulation instruction.

After reset, this register is cleared to 0000H.

After reset: 0000H R/W Address: CR001: FFFFF604H, CR011: FFFFF614H,
CR021: FFFFF624H, CR031: FFFFF634H,
CR041: FFFFF644H, CR051: FFFFF654H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
CR0n1																

(n = 0 to 5)

(a) When using the CR0n1 register as a compare register

The value set to the CR0n1 register and the count value of the TM0n register are always compared and when these values match, an interrupt request signal (INTTM0n1) is generated.

(b) When using the CR0n1 register as a capture register

The TM0n register count value is captured to the CR0n1 register by inputting a capture trigger.

The valid edge of the TI0n0 pin can be selected as the capture trigger. The valid edge of the TI0n0 pin is set with the PRM0n register.

Table 7-4 shows the settings when the valid edge of the TI0n0 pin is specified as the capture trigger.

Table 7-4. Capture Trigger of CR0n1 Register and Valid Edge of TI0n0 Pin

Capture Trigger of CR0n1 Register	Valid Edge of TI0n0 Pin		
		ESn01	ESn00
Falling edge	Falling edge	0	0
Rising edge	Rising edge	0	1
Both rising and falling edges	Both rising and falling edges	1	1

Remarks 1. n = 0 to 5

2. Setting the ESn01 and ESn00 bits to 10 is prohibited.

Cautions

1. **If 0000H is set to the CR0n1 register, an interrupt request (INTTM0n1) is generated after or overflow of the TM0n register, after clear & start on a match between the TM0n register and CR0n0 register, after clear by the TI0n0 valid edge, or after clear by a one-shot trigger.**
2. **When the P33, P35, P613, P92, and P94 pins are used as the valid edges of TI000, TI010, TI020, TI030, and TI051, they cannot be used as timer outputs (TO00 to TO03, TO05). Moreover, when used as TO00 to TO03 and TO05, these pins cannot be used as the valid edges of TI000, TI010, TI020, TI030, and TI051.**
3. **If, when the CR0n1 register is used as a capture register, the register read interval and capture trigger input conflict, the read data becomes undefined (but the capture data itself is normal). Moreover, when the count stop input and capture trigger input conflict, the capture data becomes undefined.**
4. **The CR0n1 register can be rewritten during TM0n register operation only in the PPG output mode. Refer to 7.4.2 PPG output operation.**

7.3 Control Registers

The registers that control 16-bit timer/event counters 00 to 05 are as follows.

- 16-bit timer mode control register 0n (TMC0n)
- Capture/compare control register 0n (CRC0n)
- 16-bit timer output control register 0n (TOC0n)
- Prescaler mode register 0n (PRM0n)

Remark To use the TI0n0, TI0n1, and TO0n pin functions, refer to **Table 4-28 Settings When Port Pins Are Used for Alternate Functions**.

(1) 16-bit timer mode control register 0n (TMC0n)

TMC0n is used to set the 16-bit timer operation mode, the 16-bit timer counter 0n (TM0n) clear mode, and the output timing, and to detect overflow.

The TMC0n register is set by an 8-bit or 1-bit memory manipulation instruction.

After reset, this register is cleared to 00H.

Caution 1. The TM0n register starts operating when a value other than 00 (operation stop mode) is set to the TMC0n3 and TMC0n2 bits of the TMC0n register. To stop the operation, set 00 to the TMC0n3 and TMC0n2 bits.

2. When the main clock is stopped and the CPU operates on the subclock, do not access the TMC0n register using an access method that causes a wait.
For details, refer to 3.4.8 (2).

Remark n = 0 to 5

After reset: 00H R/W Address: FFFFF606H, FFFFF616H, FFFFF626H
FFFFF636H, FFFFF646H, FFFFF656H

	7	6	5	4	3	2	1	<0>
TMC0n	0	0	0	0	TMC0n3	TMC0n2	TMC0n1[Note]	OVF0n

(n = 0 to 5
m = 4, 5)

TMC0n3	TMC0n2	TMC0n1[Note]	Selection of operation mode and clear mode	Selection of TO0n output inverse timing	Generation of interrupt
0	0	0	Operation stop (TM0n cleared to 0)	Unchanged	Not generated
0	0	1			
0	1	0	Free-running mode	Match of TM0n and CR0n0 or match of TM0n and CR0n1	Generated upon match of TM0n and CR0n0 and match of TM0n and CR0n1
0	1	1		Match of TM0m and CR0m0, match of TM0m and CR0m1, or valid edge of TI0m0	
1	0	0	Clear & start with valid edge of TI0n0	Match of TM0m and CR0m0 or match of TM0m and CR0m1	
1	0	1		Match of TM0m and CR0m0, match of TM0m and CR0m1, or valid edge of TI0m0	
1	1	0	Clear & start upon match of TM0n and CR0n0	Match of TM0n and CR0n0 or match of TM0n and CR0n1	
1	1	1		Match of TM0m and CR0m0, match of TM0m and CR0m1, or valid edge of TI0m0	

OVF0n	Detection of overflow of 16-bit timer register 0n
0	No overflow
1	Overflow

Note TM00 to TM03 must be set to 0.

Cautions 1. Write to bits other than the OVF0n flag after stopping the timer operation.

2. The valid edge of the TI0n0 pin is set by prescaler mode register 0n (PRM0n).

3. When the mode in which the timer is cleared and started upon match of TM0n and CR0n0 is selected, the setting value of CR0n0 is FFFFH, and when the value of TM0n changes from FFFFH to 0000H, the OVF0n flag is set to 1.

Remark TO0n: Output pin of 16-bit timer/event counter 0n
TI0n0: Input pin of 16-bit timer/event counter 0n
TM0n: 16-bit timer counter 0n
CR0n0: 16-bit timer capture/compare register 0n0
CR0n1: 16-bit timer capture/compare register 0n1

The following shows the I/O configuration of each channel and the selection of the TO0n output inversion timing (setting of the TMC0n1 bit).

★ **Table 7-5. I/O Configuration of Each Channel**

Channel	Output Pin	Input Pin	I/O Pin	Setting of TMC0n1 Bit
TM00	–	TI001	TI000/TO00	Always set to 0.
TM01	–	TI011	TI010/TO01	Always set to 0.
TM02	–	TI021	TI020/TO02	0 (read only)
TM03	–	TI031	TI030/TO03	0 (read only)
TM04	TO04	TI040, TI041	–	1/0
TM05	–	TI050	TI051/TO05	1/0

(2) Capture/compare control register 0n (CRC0n)

CRC0n controls the operation of 16-bit timer capture/compare registers 0n0 and 0n1 (CR0n0 and CR0n1).

The CRC0n register is set by an 8-bit or 1-bit memory manipulation instruction.

After reset, CRC0n is cleared to 00H.

After reset: 00H R/W Address: FFFFF608H, FFFFF618H, FFFFF628H
FFFFF638H, FFFFF648H, FFFFF658H

	7	6	5	4	3	2	1	0
CRC0n	0	0	0	0	0	CRC0n2	CRC0n1	CRC0n0

(n = 0 to 5)

CRC0n2	Selection of operation mode of CR0n1 register
0	Operation as compare register
1	Operation as capture register

CRC0n1	Selection of capture trigger of CR0n0 register
0	Capture at valid edge of TI0n1
1	Capture at inverse phase of valid edge of TI0n0

CRC0n0	Selection of operation mode of CR0n0 register
0	Operation as compare register
1	Operation as capture register

Cautions 1. Before setting the CRC0n register, be sure to stop the timer operation.

2. When the mode in which the timer is cleared and started upon match of the TM0n register and CR0n0 register is selected by 16-bit timer mode control register 0n (TMC0n), do not specify the CR0n0 register as the capture register.

3. When both the rising and falling edges are specified for the TI0n0 valid edge, capture operation is not performed.

4. To ensure reliable capture operation, a pulse longer than two cycles of the count clock selected by prescaler mode register 0n (PRM0n) is required.

Remark TI0n0, TI0n1: Input pins of 16-bit timer/event counter 0n.

(3) 16-bit timer output control register 0n (TOC0n)

TOC0n controls the operation of the 16-bit timer/event counter 0n output controller by setting or resetting the timer output F/F, enabling or disabling inverse output, enabling or disabling the timer of 16-bit timer/event counter 0n, enabling or disabling the one-shot pulse output operation, and selecting an output trigger for a one-shot pulse by software (16-bit timer/event counters 02 and 03 do not have a one-shot pulse output function).

The TOC0n register is set by an 8-bit memory manipulation instruction.

After reset, TOC0n is cleared to 00H.

(1/2)

After reset: 00H R/W Address: FFFFF609H, FFFFF619H, FFFFF629H FFFFF639H, FFFFF649H, FFFFF659H

	7	6	5	4	3	2	1	0
TOC0n	0	OSPT0m[Note 1]	OSPE0m[Note 1]	TOC0n4	LVS0n	LVR0n	TOC0n1	TOE0n

(n = 0 to 5
m = 0, 1, 4, 5
k = 4, 5)

OSPT0m[Note 1]	Output trigger for one-shot pulse by software
0	–
1	One-shot pulse output

OSPE0m[Note 1]	Control of one-shot pulse output operation
0	Successive pulse output
1	One-shot pulse output[Note 2]

TOC0n4	Control of timer output F/F upon match of CR0n1 register and TM0n register
0	Inversion operation disabled
1	Inversion operation enabled

Notes 1. TM02 and TM03 do not provide a one-shot pulse output function. Always clear bits 6 and 5 to 0. TM00 and TM01 are the alternate-function pins of the timer I/O pins, so only a software trigger is valid for one-shot pulse output. Clear the TMC011 and TMC001 bits of the TMC00 and TMC01 registers to 0.

2. The one-shot pulse output operates normally in the free-running mode and the mode in which clear & start occurs on the valid edge of TI0k0. In the mode in which clear & start occurs on match between the TM0m register and the CR0m0 register, one-shot pulse output is not performed because no overflow occurs.

(2/2)

LVS0n	LVR0n	Setting of status of timer output F/F
0	0	Unchanged
0	1	Reset timer output F/F (0)
1	0	Set timer output F/F (1)
1	1	Setting prohibited

TOC0n1	Control of timer output F/F upon match of CR0n0 register and TM0n register
0	Inversion operation disabled
1	Inversion operation enabled

TOE0n	Control of timer output
0	Output disabled (output is fixed to 0 level)
1	Output enabled

Cautions 1. Be sure to stop the timer operation before setting other than the TOC0n4 bit.

2. The LVS0n and LVR0n bits are 0 when read.

3. The OSPT0m bit is 0 when read because it is automatically cleared after data has been set.

4. Do not set (to 1) the OSPT0m bit other than for one-shot pulse output.

5. When performing successive writes to the OSPT0m bit, place an interval between writes of two or more cycles of the count clock selected by the PRM0n register.

6. Do not the LVS0n bit to 1 before setting the TOE0n bit.
Do not set the LVS0n bit and TOE0n bit to 1 at the same time.

★ **7. Do not set <1> and <2> below at the same time. Set as follows.**
<1> Set the TOC0n1, TOC0n4, TOE0n, and OSPE0m bits: Setting of timer output operation
<2> Set the LVS0n and LVR0n bits: Setting of timer output F/F

(4) Prescaler mode register 0n (PRM0n)

This register sets the count clock of 16-bit timer counter 0n (TM0n) and the valid edge of the TI0n0 and TI0n1 pin inputs. The PRM0n register is set by an 8-bit or 1-bit memory manipulation instruction.

After reset, PRM0n is cleared to 00H.

Cautions
1. **When setting the count clock to the TI0n0 valid edge, do not set the mode in which clear & start occurs on TI0n0 valid edge and do not set the TI0n0 valid edge as the capture trigger.**
2. **Before setting the PRM0n register, be sure to stop the timer operation.**
3. **If 16-bit timer counter 0n (TM0n) operation is enabled by specifying the rising edge of both edges for the valid edge of the TI0n0 pin or TI0n1 pin while the TI0n0 pin or TI0n1 pin is high level immediately after system reset, the rising edge is detected immediately after the rising edge or both edges is specified. Be careful when pulling up the TI0n0 pin or TI0n1 pin. However, the rising edge is not detected when operation is enabled after it has been stopped.**
4. **When the P33, P35, P613, P92, and P94 pins are used as the valid edges of TI000, TI010, TI020, TI030, and TI051, they cannot be used as timer outputs (TO00 to TO03, TO05). Moreover, when used as TO00 to TO03 and TO05, these pins cannot be used as the valid edges of TI000, TI010, TI020, TI030, and TI051.**

(a) Prescaler mode register 00 (PRM00)

After reset: 00H R/W Address: FFFFF607H

	7	6	5	4	3	2	1	0
PRM00	ES011	ES010	ES001	ES000	0	0	PRM001	PRM000

ES011	ES010	Selection of valid edge of TI001
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES001	ES000	Selection of valid edge of TI000
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

PRM001	PRM000	Selection of count clock[Note 1]			
		Count clock	f_{XX}		
			20 MHz	16 MHz	10 MHz
0	0	$f_{XX}/2$	100 ns	125 ns	200 ns
0	1	$f_{XX}/4$	200 ns	250 ns	400 ns
1	0	$f_{XX}/8$	400 ns	500 ns	800 ns
1	1	Valid edge of TI000[Note 2]	–	–	–

Notes 1. When the internal clock is selected, set so as to satisfy the following conditions.

V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz

V_{DD} = 2.7 to 4.0 V: Count clock ≤ 5 MHz

2. The external clock requires a pulse longer than two cycles of the internal clock ($f_{XX}/4$).

Remark f_{XX}: Main clock frequency

(b) Prescaler mode register 01 (PRM01)

After reset: 00H R/W Address: FFFFF617H

	7	6	5	4	3	2	1	0
PRM01	ES111	ES110	ES101	ES100	0	0	PRM011	PRM010

ES111	ES110	Selection of valid edge of TI011
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES101	ES100	Selection of valid edge of TI010
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

PRM011	PRM010	Selection of count clock[Note 1]			
		Count clock	f_{XX}		
			20 MHz	16 MHz	10 MHz
0	0	f_{XX}	Setting prohibited	Setting prohibited	100 ns
0	1	$f_{XX}/4$	200 ns	250 ns	400 ns
1	0	INTWT	–	–	–
1	1	Valid edge of TI010[Note 2]	–	–	–

Notes 1. When the internal clock is selected, set so as to satisfy the following conditions.

V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz

V_{DD} = 2.7 to 4.0 V: Count clock ≤ 5 MHz

2. The external clock requires a pulse longer than two cycles of the internal clock ($f_{XX}/4$).

Remark f_{XX}: Main clock frequency

(c) Prescaler mode register 02 (PRM02)

After reset: 00H R/W Address: FFFFF627H

	7	6	5	4	3	2	1	0
PRM02	ES211	ES210	ES201	ES200	0	0	PRM021	PRM020

ES211	ES210	Selection of valid edge of TI021
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES201	ES200	Selection of valid edge of TI020
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

PRM021	PRM020	Selection of count clock[Note 1]			
		Count clock	f_{XX}		
			20 MHz	16 MHz	10 MHz
0	0	$f_{XX}/2$	100 ns	125 ns	200 ns
0	1	$f_{XX}/4$	200 ns	250 ns	400 ns
1	0	$f_{XX}/8$	400 ns	500 ns	800 ns
1	1	Valid edge of TI020[Note 2]	–	–	–

Notes 1. When the internal clock is selected, set so as to satisfy the following conditions.

V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz

V_{DD} = 2.7 to 4.0 V: Count clock ≤ 5 MHz

2. The external clock requires a pulse longer than two cycles of the internal clock ($f_{XX}/4$).

Remark f_{XX}: Main clock frequency

(d) Prescaler mode register 03 (PRM03)

After reset: 00H R/W Address: FFFFF637H

	7	6	5	4	3	2	1	0
PRM03	ES311	ES310	ES301	ES300	0	0	PRM031	PRM030

ES311	ES310	Selection of valid edge of TI031
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES301	ES300	Selection of valid edge of TI030
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

PRM031	PRM030	Selection of count clock[Note 1]			
		Count clock	f_{XX}		
			20 MHz	16 MHz	10 MHz
0	0	$f_{XX}/4$	200 ns	250 ns	400 ns
0	1	$f_{XX}/16$	800 ns	1 μs	1.6 μs
1	0	$f_{XX}/512$	25.6 μs	32 μs	51.2 μs
1	1	Valid edge of TI030[Note 2]	–	–	–

Notes 1. When the internal clock is selected, set so as to satisfy the following conditions.

V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz

V_{DD} = 2.7 to 4.0 V: Count clock ≤ 5 MHz

2. The external clock requires a pulse longer than two cycles of the internal clock ($f_{XX}/4$).

Remark f_{XX}: Main clock frequency

(e) Prescaler mode register 04 (PRM04)

After reset: 00H R/W Address: FFFFF647H

	7	6	5	4	3	2	1	0
PRM04	ES411	ES410	ES401	ES400	0	0	PRM041	PRM040

ES411	ES410	Selection of valid edge of TI041
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES401	ES400	Selection of valid edge of TI040
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

PRM041	PRM040	Selection of count clock[Note 1]			
		Count clock	f_{XX}		
			20 MHz	16 MHz	10 MHz
0	0	$f_{XX}/2$	100 ns	125 ns	200 ns
0	1	$f_{XX}/4$	200 ns	250 ns	400 ns
1	0	$f_{XX}/8$	400 ns	500 ns	800 ns
1	1	Valid edge of TI040[Note 2]	–	–	–

Notes 1. When the internal clock is selected, set so as to satisfy the following conditions.

V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz

V_{DD} = 2.7 to 4.0 V: Count clock ≤ 5 MHz

2. The external clock requires a pulse longer than two cycles of the internal clock ($f_{XX}/4$).

Remark f_{XX}: Main clock frequency

(f) Prescaler mode register 05 (PRM05)

After reset: 00H R/W Address: FFFFF657H

	7	6	5	4	3	2	1	0
PRM05	ES511	ES510	ES501	ES500	0	0	PRM051	PRM050

ES511	ES510	Selection of valid edge of TI051
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

ES501	ES500	Selection of valid edge of TI050
0	0	Falling edge
0	1	Rising edge
1	0	Setting prohibited
1	1	Both rising and falling edges

PRM051	PRM050	Selection of count clock[Note 1]			
		Count clock	f_{XX}		
			20 MHz	16 MHz	10 MHz
0	0	f_{XX}	Setting prohibited	Setting prohibited	100 ns
0	1	$f_{XX}/4$	200 ns	250 ns	400 ns
1	0	$f_{XX}/256$	12.8 μs	16 μs	25.6 μs
1	1	Valid edge of TI050[Note 2]	–	–	–

Notes 1. When the internal clock is selected, set so as to satisfy the following conditions.

V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz

V_{DD} = 2.7 to 4.0 V: Count clock ≤ 5 MHz

2. The external clock requires a pulse longer than two cycles of the internal clock ($f_{XX}/4$).

Remark f_{XX}: Main clock frequency

7.4 Operation

7.4.1 Operation as interval timer (16 bits)

16-bit timer/event counter 0n can be made to operate as an interval timer by setting 16-bit timer mode control register 0n (TMC0n) and capture/compare control register 0n (CRC0n) as shown in **Figure 7-2** (n = 0 to 5).

Setting procedure

The basic operation setting procedure is as follows.

<1> Set the count clock using the PRM0n register.
<2> Set the CRC0n register (see **Figure 7-2** for the setting value).
<3> Set any value to the CR0n0 register.
<4> Set the TMC0n register: Start operation (see **Figure 7-2** for the setting value).

Caution The CR0n0 register cannot be rewritten during TM0n operation.

Remarks 1. For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

2. For INTTM0n0 interrupt enable, refer to **CHAPTER 19 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

The interval timer repeatedly generates interrupts at the interval of the preset count value in 16-bit timer capture/compare register 0n0 (CR0n0).

If the count value in 16-bit timer counter 0n (TM0n) matches the value set in the CR0n0 register, an interrupt request signal (INTTM0n0) is generated at the same time that the value of the TM0n register is cleared to 0 and counting is continued.

The count clock of 16-bit timer/event counter 0n can be selected with bits 0 and 1 of prescaler mode register 0n (PRM0n).

Remark n = 0 to 5

Figure 7-2. Control Register Setting Contents During Interval Timer Operation

(a) 16-bit timer mode control register 0n (TMC0n)

					TMC0n3	TMC0n2	TMC0n1	OVF0n
TMC0n	0	0	0	0	1	1	0/1	0

Clears & starts upon match between TM0n and CR0n0

(b) Capture/compare control register 0n (CRC0n)

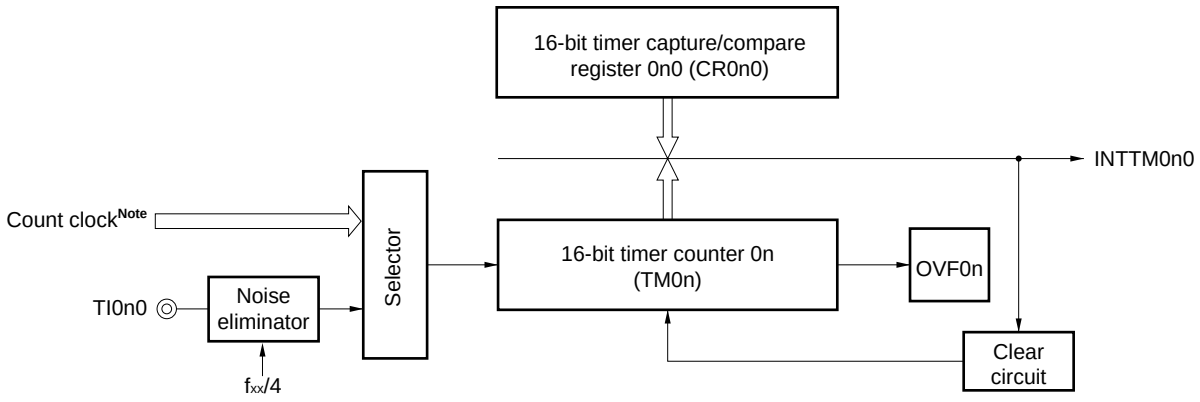
						CRC0n2	CRC0n1	CRC0n0
CRC0n	0	0	0	0	0	0/1	0/1	0

CR0n0 used as compare register

Remarks 1. 0/1: When these bits are reset to 0 or set to 1, other functions can be used together with the interval timer function. For details, refer to **7.3 (1) 16-bit timer mode control register 0n (TMC0n)** and **7.3 (2) Capture/compare control register 0n (CRC0n)**.

2. n = 0 to 5

Figure 7-3. Configuration of Interval Timer

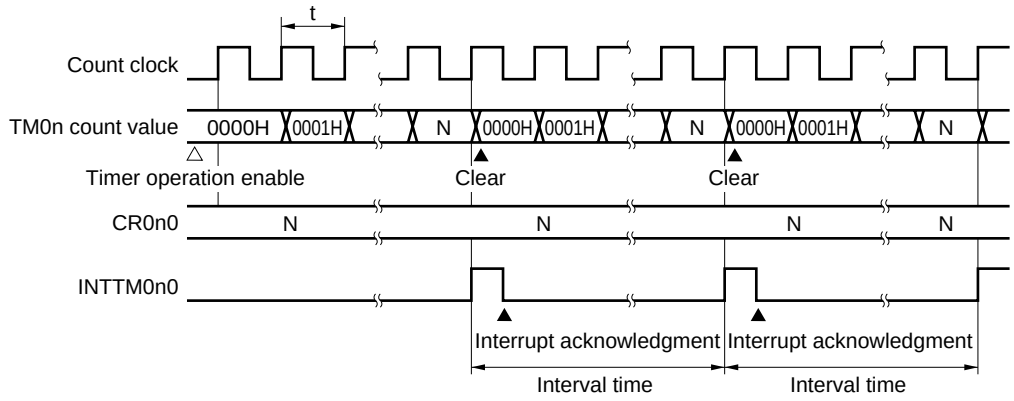


Note Set with PRM0n register.

Remarks 1. fxx: Main clock frequency

2. n = 0 to 5

★ **Figure 7-4. Timing of Interval Timer Operation**



Remarks 1. Interval time = (N + 1) × t: N = 0001H to FFFFH

2. n = 0 to 5

7.4.2 PPG output operation

16-bit timer/event counter 0n can be used for PPG (Programmable Pulse Generator) output by setting 16-bit timer mode control register 0n (TMC0n) and capture/compare control register 0n (CRC0n) as shown in **Figure 7-5**.

Setting procedure

The basic operation setting procedure is as follows.

<1> Set the CRC0n register (see **Figure 7-5** for the setting value).
<2> Set any value to the CR0n0 register.
<3> Set any value as a duty to the CR0n1 register.
<4> Set the TOC0n register (see **Figure 7-5** for the setting value).
<5> Set the count clock using the PRM0n register.
<6> Set the TMC0n register: Start operation (see **Figure 7-5** for the setting value).

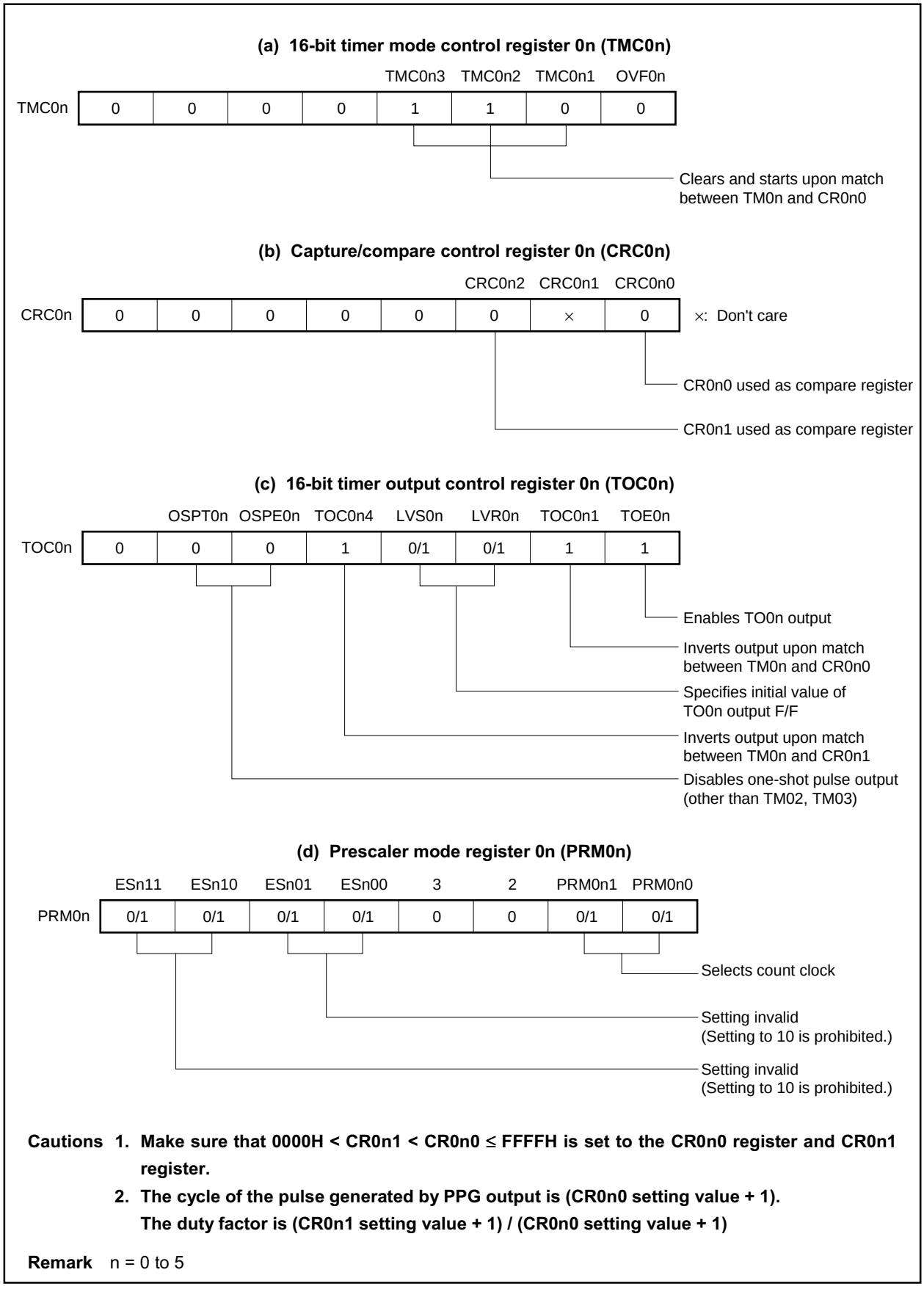
Note To change the duty value (CR0n1 register) during operation, refer to **Remark 2** in **Figure 7-7 PPG Output Operation Timing**.

Remarks 1. For the alternate-function pin (TO0n) settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Function**.

2. For INTTM0n0 interrupt enable, refer to **CHAPTER 19 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

The PPG output function outputs a rectangular wave from the TO0n pin with the cycle specified by the count value set in advance to 16-bit timer capture/compare register 0n0 (CR0n0) and the pulse width specified by the count value set in advance to 16-bit timer capture/compare register 0n1 (CR0n1).

Figure 7-5. Control Register Settings in PPG Output Operation

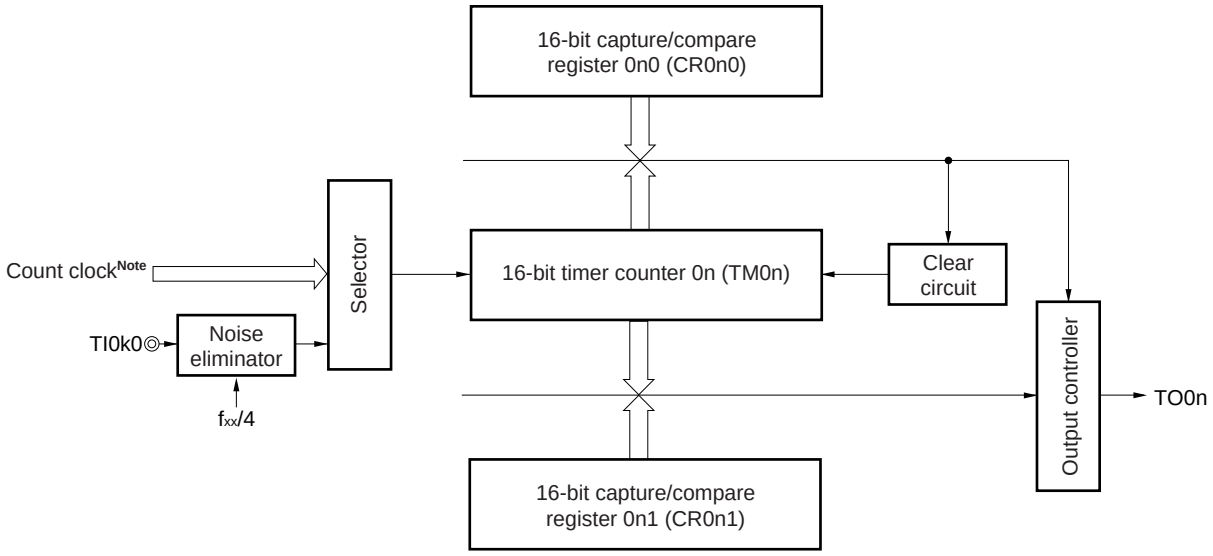


Cautions 1. Make sure that 0000H < CR0n1 < CR0n0 ≤ FFFFH is set to the CR0n0 register and CR0n1 register.

2. The cycle of the pulse generated by PPG output is (CR0n0 setting value + 1).
The duty factor is (CR0n1 setting value + 1) / (CR0n0 setting value + 1)

Remark n = 0 to 5

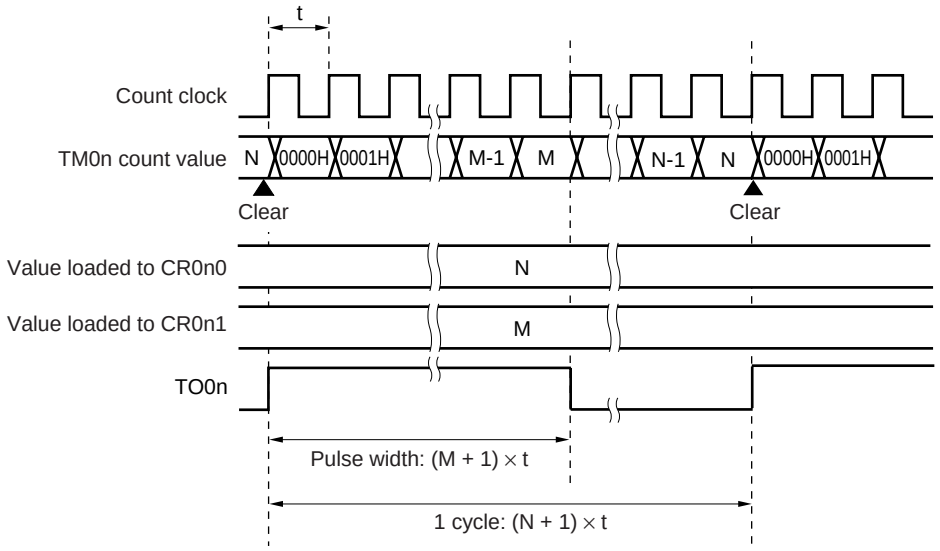
Figure 7-6. Configuration of PPG Output



Note The count clock is set by the PRM0n register.

Remark k = 4, 5
n =0 to 5

★ **Figure 7-7. PPG Output Operation Timing**



Caution CR0n0 cannot be rewritten during TM0n operation.

Remarks 1. 0000H < M < N ≤ FFFFH

2. Change the pulse width during TM0n operation (rewrite CR0n1) as follows in a PPG output operation.

<1> Disable the timer output inversion operation based on a match of TM0n and CR0n1 (TOC0n4 = 0).
<2> Disable the INTTM0n1 interrupt (TM0MKn1 =1).
<3> Rewrite CR0n1.
<4> Wait for a cycle of the TM0n count clock.
<5> Enable the timer output inversion operation based on a match of TM0n and CR0n1 (TOC0n4 = 1).
<6> Clear the interrupt request flag of INTTM0n1 (TM0IFn1 = 0).
<7> Enable the INTTM0n1 interrupt (TM0MKn1 = 0).

3. n = 0 to 5

7.4.3 Pulse width measurement

The 16-bit timer counter (TM0n) can be used to measure the pulse widths of the signals input to the TI0n0 and TI0n1 pins.

Measurement can be carried out with the TM0n register used as a free-running counter or by restarting the timer in synchronization with the edge of the signal input to the TI0n0 pin.

When an interrupt is generated, read the valid capture register value. After confirming the OVF flag, clear it by software and measure the pulse width.

Setting procedure

The basic operation setting procedure is as follows.

<1> Set the CRC0n register (see **Figures 7-9**, **7-12**, **7-14**, and **7-16** for the setting value).
<2> Set the count clock using the PRM0n register.
<3> Set the TMC0n register: Start operation (see **Figures 7-9**, **7-12**, **7-14**, and **7-16** for the setting value).

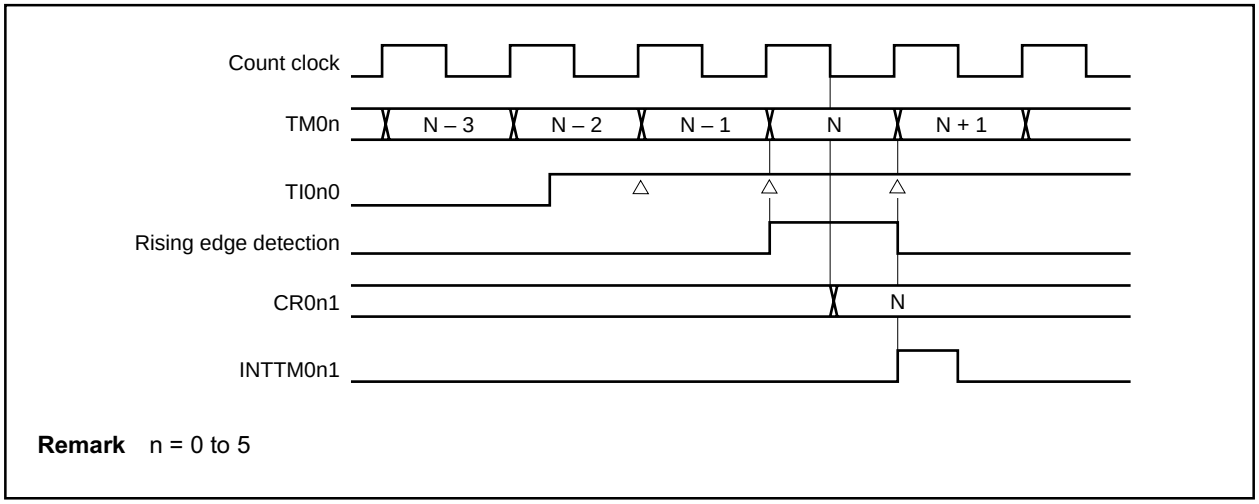
Note When using two capture registers, set the TI0n0 and TI0n1 pins.

Remarks 1. For the alternate-function pin (TI0n0, TI0n1) settings, refer **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

2. For INTTM0n0 and INTTM0n1 interrupt enable, refer to **CHAPTER 19 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

The valid edge is detected through sampling at a count clock cycle selected with the PRM0n register, and the capture operation is not performed until the valid edge is detected twice. As a result, noise with a short pulse width can be eliminated.

Figure 7-8. CR0n1 Capture Operation with Rising Edge Specified



Remark n = 0 to 5

(1) Pulse width measurement with free-running counter and one capture register

If the edge specified by prescaler mode register 0n (PRM0n) is input to the TI0n0 pin when 16-bit timer counter 0n (TM0n) is operated as a free-running counter (refer to **Figure 7-8**), the value of the TM0n register is loaded to 16-bit timer capture/compare register 0n1 (CR0n1) and an external interrupt request signal (INTTM0n1) is set.

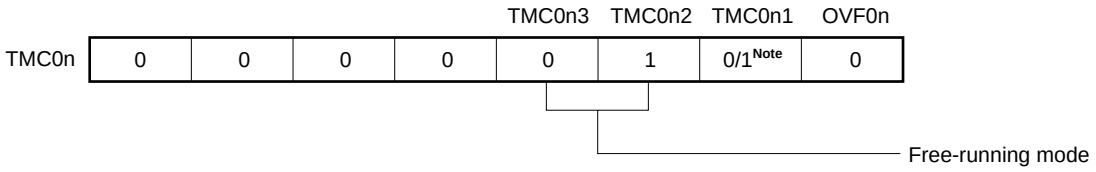
The edge is specified by using bits 4 and 5 (ESn00, ESn01) of the PRM0n register. The rising edge, falling edge, or both the rising and falling edges can be selected.

The valid edge is detected through sampling at a count clock cycle selected with the PRM0n register, and the capture operation is not performed until the valid edge is detected twice. As a result, noise with a short pulse width can be eliminated.

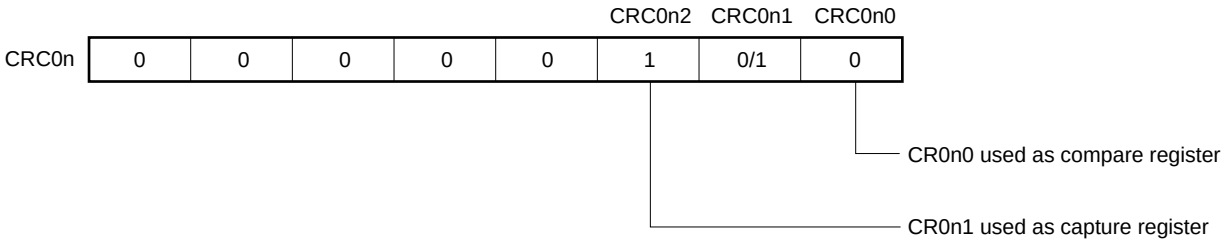
Remark n = 0 to 5

Figure 7-9. Control Register Settings for Pulse Width Measurement with Free-Running Counter and One Capture Register (When TI0n0 Pin and CR0n1 Registers Are Used)

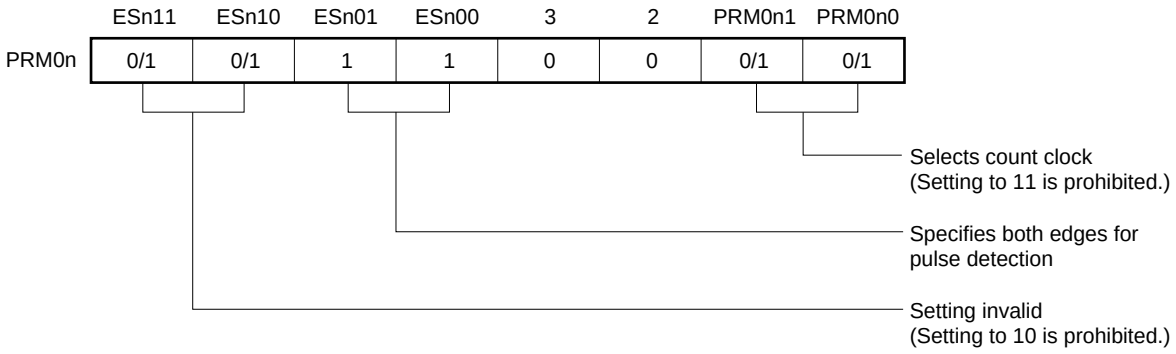
(a) 16-bit timer mode control register 0n (TMC0n)



(b) Capture/compare control register 0n (CRC0n)



(c) Prescaler mode register 0n (PRM0n)

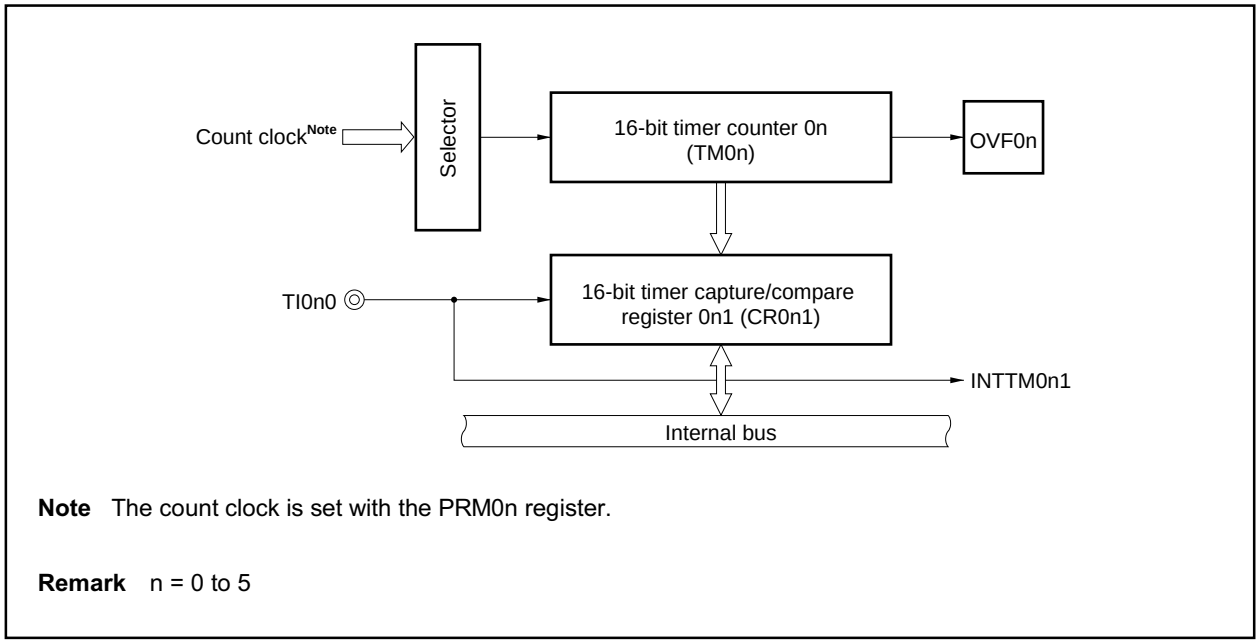


Note Always set TM00 to TM03 to 0.

Remarks 1. 0/1: When these bits are reset to 0 or set to 1, other functions can be used together with the pulse width measurement function. For details, refer to **7.3 (1) 16-bit timer mode control register 0n (TMC0n)** and **7.3 (2) Capture/compare control register 0n (CRC0n)**.

2. n = 0 to 5

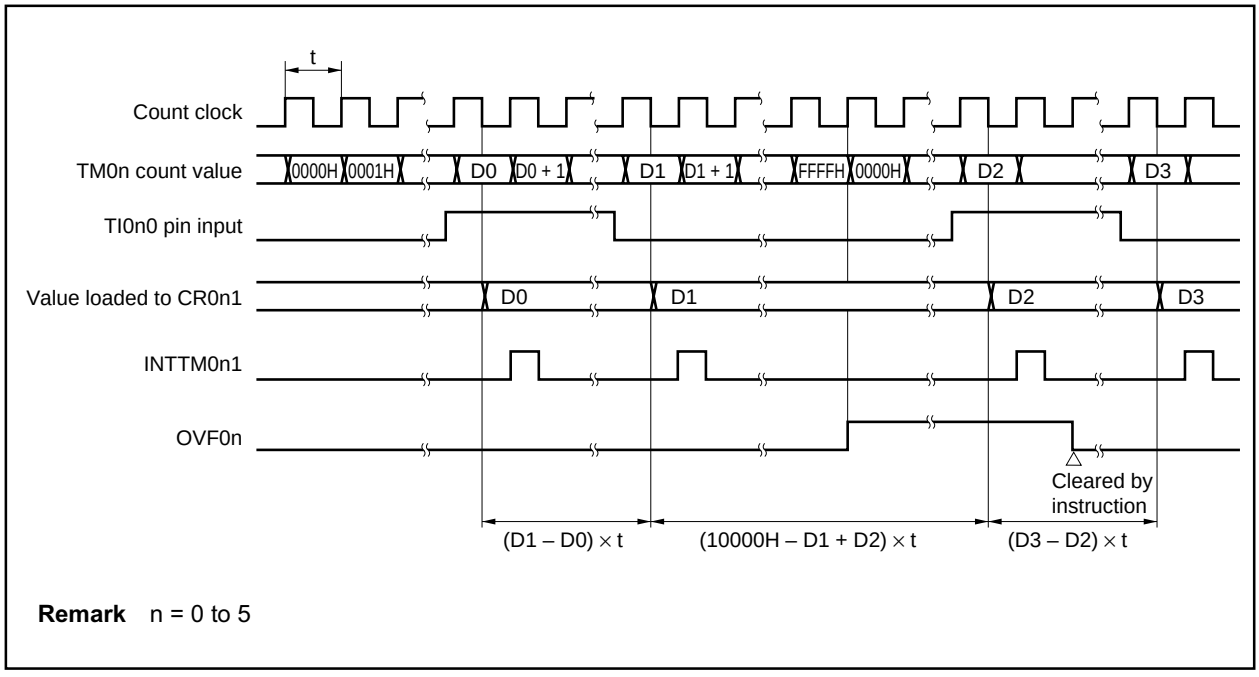
Figure 7-10. Configuration for Pulse Width Measurement with Free-Running Counter



Note The count clock is set with the PRM0n register.

Remark n = 0 to 5

Figure 7-11. Timing of Pulse Width Measurement with Free-Running Counter and One Capture Register (with Both Edges Specified)



Remark n = 0 to 5

(2) Measurement of two pulse widths with free-running counter

The pulse widths of two signals respectively input to the TI0n0 pin and the TI0n1 pin can be simultaneously measured when 16-bit timer counter 0n (TM0n) is used as a free-running counter (refer to **Figure 7-12**).

When the edge specified by bits 4 and 5 (ESn00, ESn01) of prescaler mode register 0n (PRM0n) is input to the TI0n0 pin, the value of the TM0n register is loaded to 16-bit timer capture/compare register 0n1 (CR0n1) and an external interrupt request signal (INTTM0n1) is set.

When the edge specified by bits 6 and 7 (ESn10 and ESn11) of the PRM0n register is input to the TI0n1 pin, the value of the TM0n register is loaded to 16-bit timer capture/compare register 0n0 and an external interrupt request signal (INTTM0n0) is set.

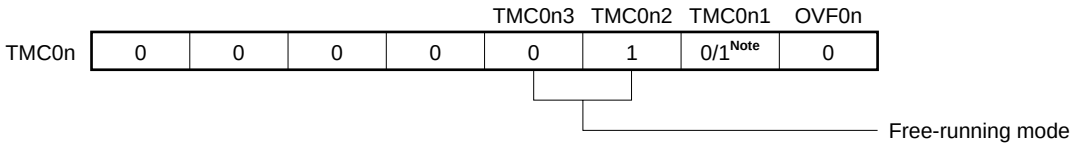
The edges of the TI0n0 and TI0n1 pins are specified by bits 4 and 5 (ESn00 and ESn01) and bits 6 and 7 (ESn10, ESn11) of the PRM0n register, respectively. Specify both rising and falling edges.

The valid edge of the TI0n0 pin is detected through sampling at the count clock cycle selected with the PRM0n register, and the capture operation is not performed until the valid level is detected twice. As a result, noise with a short pulse width can be eliminated.

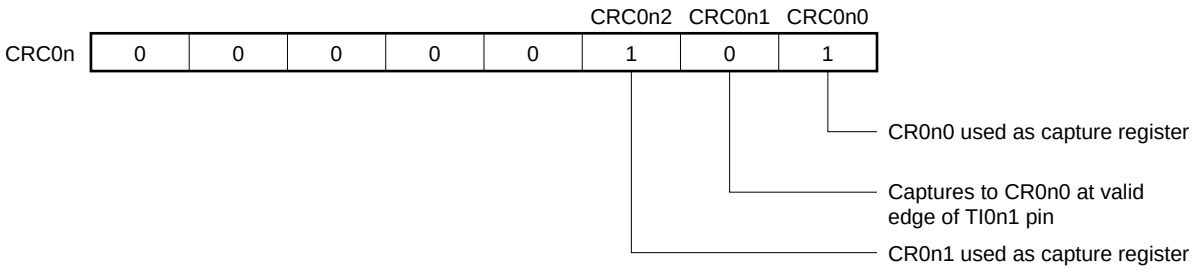
Remark n = 0 to 5

Figure 7-12. Control Register Settings for Measurement of Two Pulse Widths with Free-Running Counter

(a) 16-bit timer mode control register 0n (TMC0n)



(b) Capture/compare control register 0n (CRC0n)



(c) Prescaler mode register 0n (PRM0n)

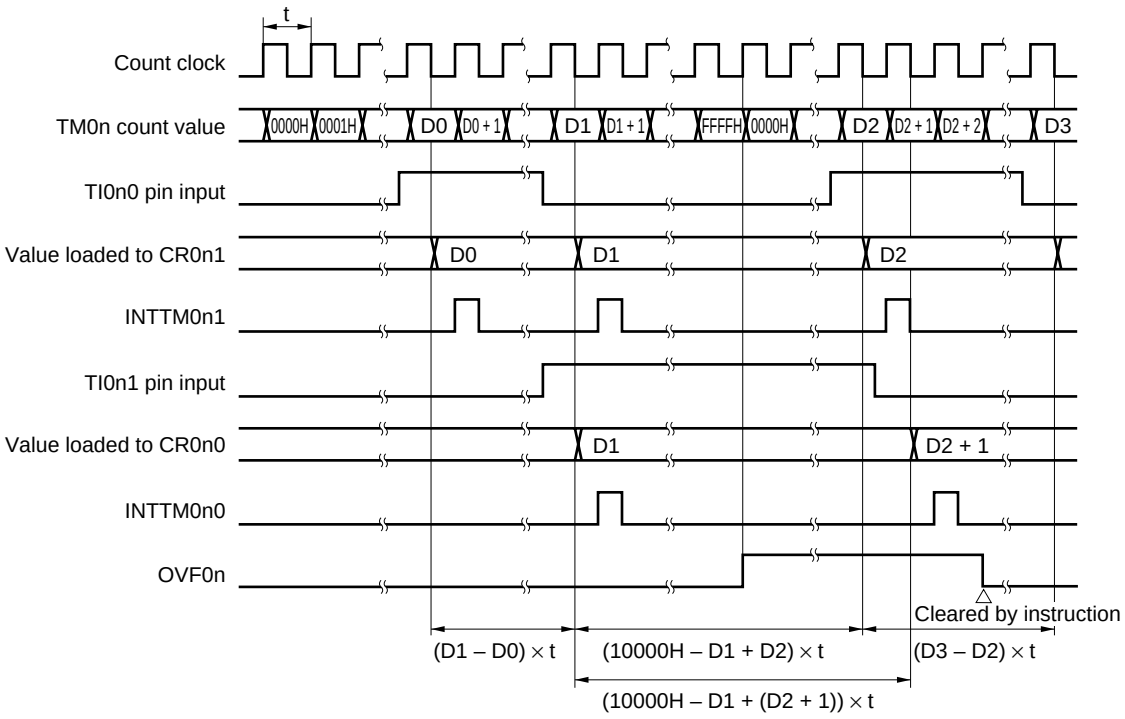
Note Always set TM00 to TM03 to 0.

Remarks 1. 0/1: When these bits are reset to 0 or set to 1, other functions can be used together with the pulse width measurement function. For details, refer to **7.3 (1) 16-bit timer mode control register 0n (TMC0n)**.

2. n = 0 to 5

- Capture operation (free-running mode)
  The following figure illustrates the operation of the capture register when the capture trigger is input.

Figure 7-13. Timing of Pulse Width Measurement with Free-Running Counter (with Both Edges Specified)



Remark n = 0 to 5

(3) Pulse width measurement with free-running counter and two capture registers

When 16-bit timer counter 0n (TM0n) is used as a free-running counter (refer to **Figure 7-14**), the pulse width of the signal input to the TI0n0 pin can be measured.

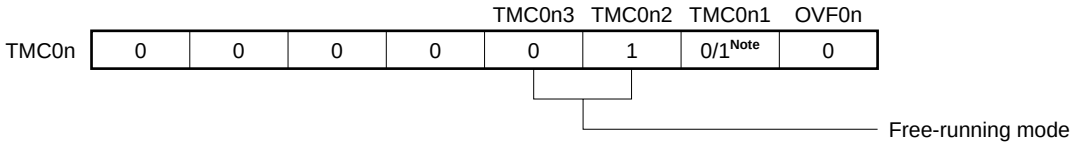
When the edge specified by bits 4 and 5 (ESn00 and ESn01) of prescaler mode register 0n (PRM0n) is input to the TI0n0 pin, the value of the TM0n register is loaded to 16-bit timer capture/compare register 0n1 (CR0n1) and an external interrupt request signal (INTTM0n1) is set.

The value of the TM0n register is also loaded to 16-bit timer capture/compare register 0n0 (CR0n0) when an edge inverse to the one that triggers capturing to the CR0n1 register is input.

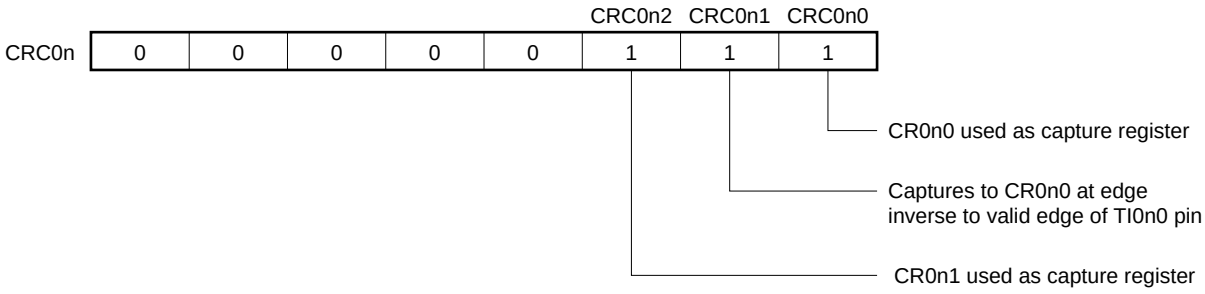
The valid edge of the TI0n0 pin is detected through sampling at a count clock cycle selected with the PRM0n register, and the capture operation is not performed until the valid edge is detected twice. As a result, noise with a short pulse width can be eliminated.

Figure 7-14. Control Register Settings for Pulse Width Measurement with Free-Running Counter and Two Capture Registers (with Rising Edge Specified)

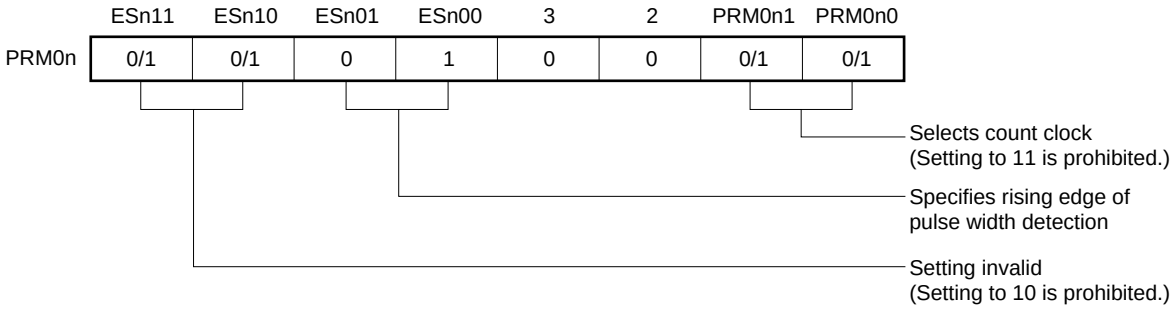
(a) 16-bit timer mode control register 0n (TMC0n)



(b) Capture/compare control register 0n (CRC0n)



(c) Prescaler mode register 0n (PRM0n)

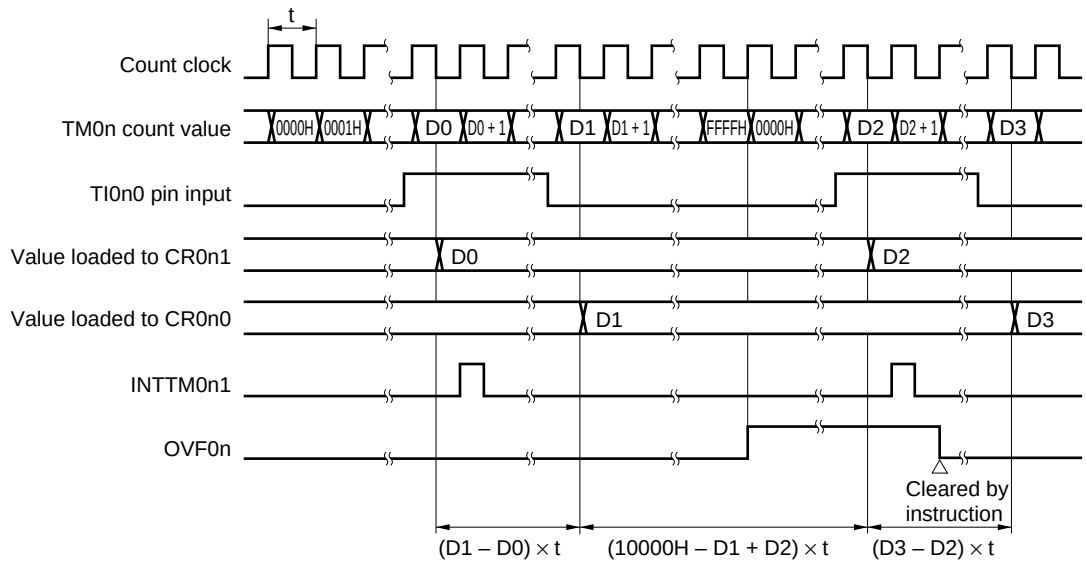


Note Always set TM00 to TM03 to 0.

Remarks 1. 0/1: When these bits are reset to 0 or set to 1, other functions can be used together with the pulse width measurement function. For details, refer to **7.3 (1) 16-bit timer mode control register 0n (TMC0n)**.

2. n = 0 to 5

Figure 7-15. Timing of Pulse Width Measurement with Free-Running Counter and Two Capture Registers (with Rising Edge Specified)



Remark n = 0 to 5

(4) Pulse width measurement by restarting

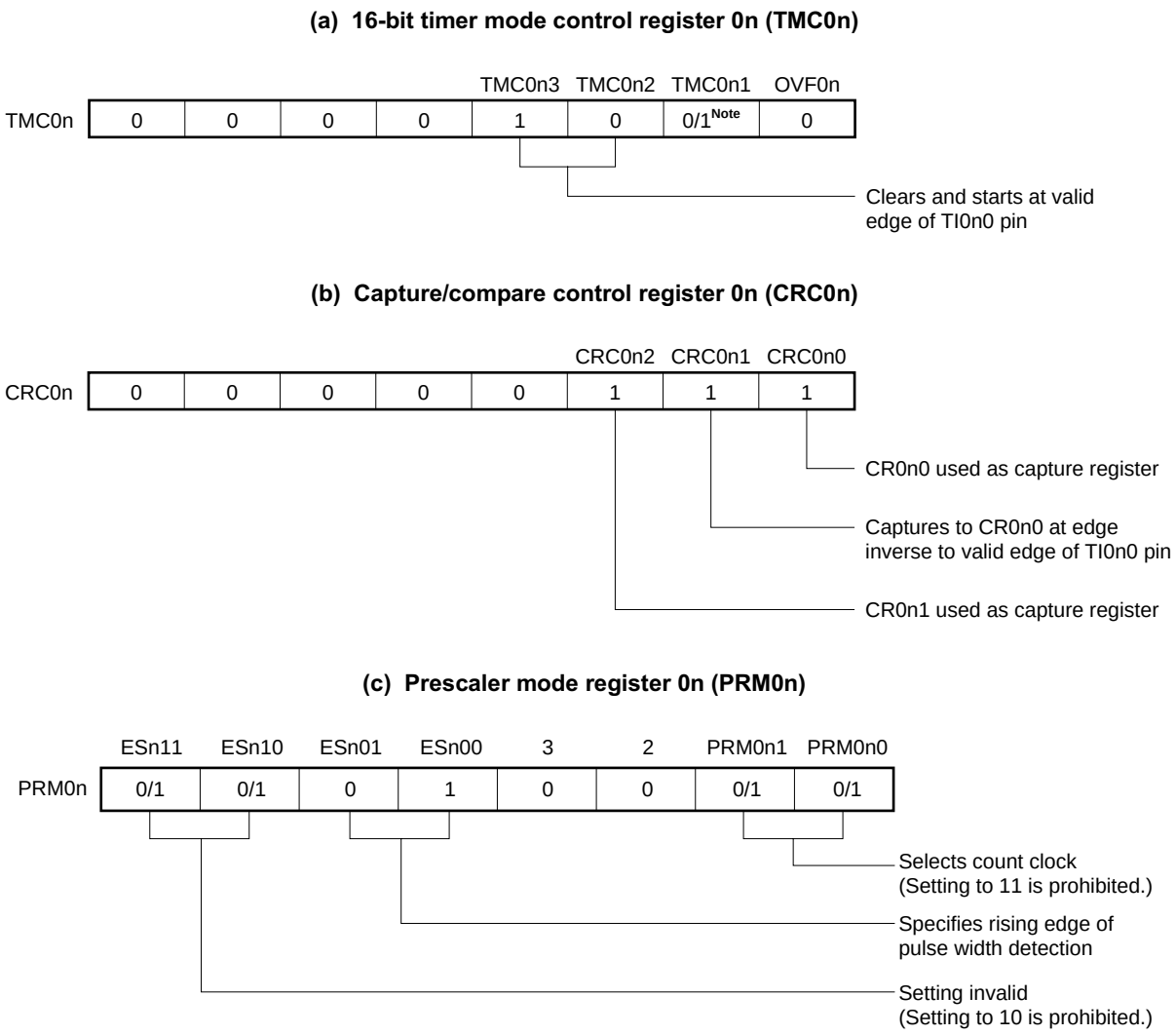
When the valid edge of the TI0n0 pin is detected, the pulse width of the signal input to the TI0n0 pin can be measured by clearing the TM0n register and then resuming counting after loading the count value of 16-bit timer counter 0n (TM0n) to 16-bit timer capture/compare register 0n1 (CR0n1) (refer to **Figure 7-17**).

The edge is specified by bits 4 and 5 (ESn00 and ESn01) of prescaler mode register 0n (PRM0n). The rising or falling edge can be specified.

The valid edge is detected through sampling at a count clock cycle selected with the PRM0n register and the capture operation is not performed until the valid level is detected twice.

As a result, noise with a short pulse can be eliminated.

Figure 7-16. Control Register Settings for Pulse Width Measurement by Restarting

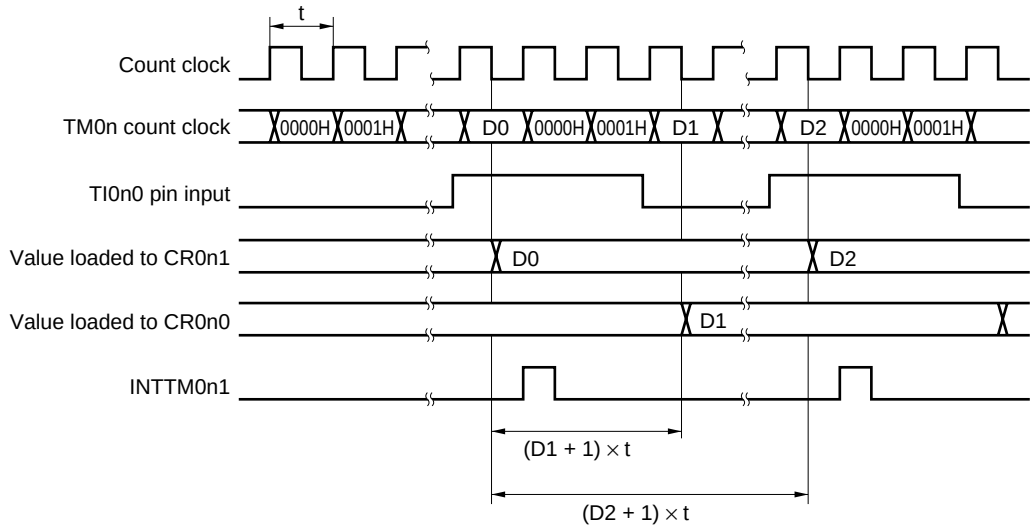


Note Always set TM00 to TM03 to 0.

Remarks 1. 0/1: When these bits are reset to 0 or set to 1, other functions can be used together with the pulse width measurement function. For details, refer to **7.3 (1) 16-bit timer mode control register 0n (TMC0n)**.

2. n = 0 to 5

Figure 7-17. Timing of Pulse Width Measurement by Restarting (with Rising Edge Specified)



Remark n = 0 to 5

7.4.4 Operation as external event counter

Setting procedure

The basic operation setting procedure is as follows.

<1> Set the CRC0n register (see **Figure 7-18** for the setting value).
<2> Set the count clock using the PRM0n register.
<3> Set any value (except for 0000H) to the CR0n0 register.
<4> Set the TMC0n register: Start operation (see **Figure 7-18** for the setting value).

Remarks 1. For the alternate-function pin (TI0n0) settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

2. For INTTM0n0 interrupt enable, refer to **CHAPTER 19 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

The external event counter counts the number of clock pulses input to the TI0n0 pin from an external source by using 16-bit timer counter 0n (TM0n).

Each time the valid edge specified by prescaler mode register 0n (PRM0n) has been input, the TM0n register is incremented.

When the count value of the TM0n register matches the value of 16-bit timer capture/compare register 0n0 (CR0n0), the TM0n register is cleared to 0 and an interrupt request signal (INTTM0n0) is generated.

Set the CR0n0 register to a value other than 0000H (one-pulse count operation is not possible).

The edge is specified by bits 4 and 5 (ESn00 and ESn01) of the PRM0n register. The rising, falling, or both the rising and falling edges can be specified.

The valid edge is detected through sampling at a count clock cycle of $f_{XX}/4$, and the capture operation is not performed until the valid level is detected twice. As a result, noise with a short pulse width can be eliminated.

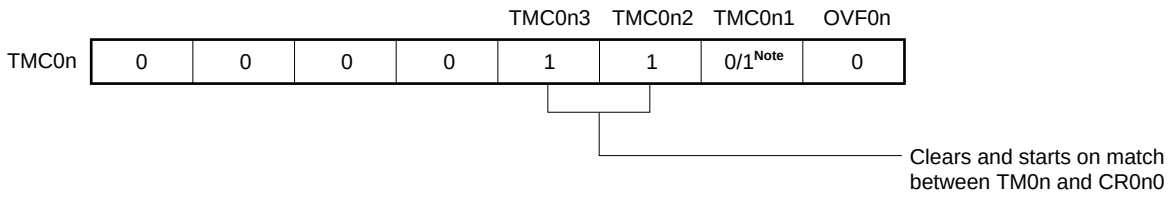
Cautions 1. When using the TM00 to TM03 registers as external event counters, the timer outputs (TO00 to TO03) cannot be used.

2. The value of the CR0n0 and CR0n1 registers cannot be changed during timer count operation.

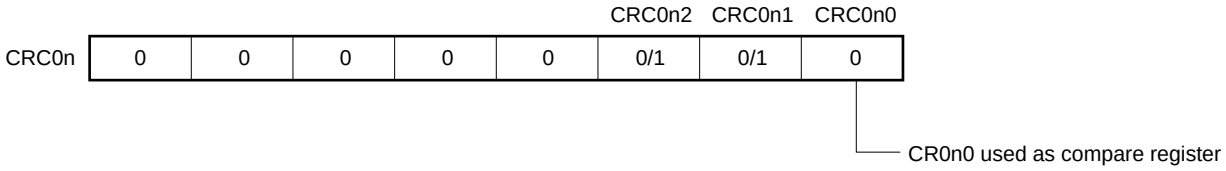
Remark n = 0 to 5

Figure 7-18. Control Register Settings in External Event Counter Mode

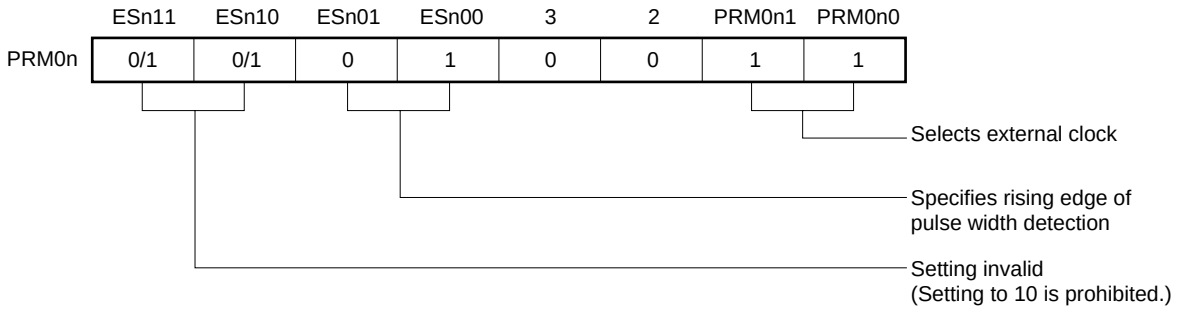
(a) 16-bit timer mode control register 0n (TMC0n)



(b) Capture/compare control register 0n (CRC0n)



(C) Prescaler mode register 0n (PRM0n)

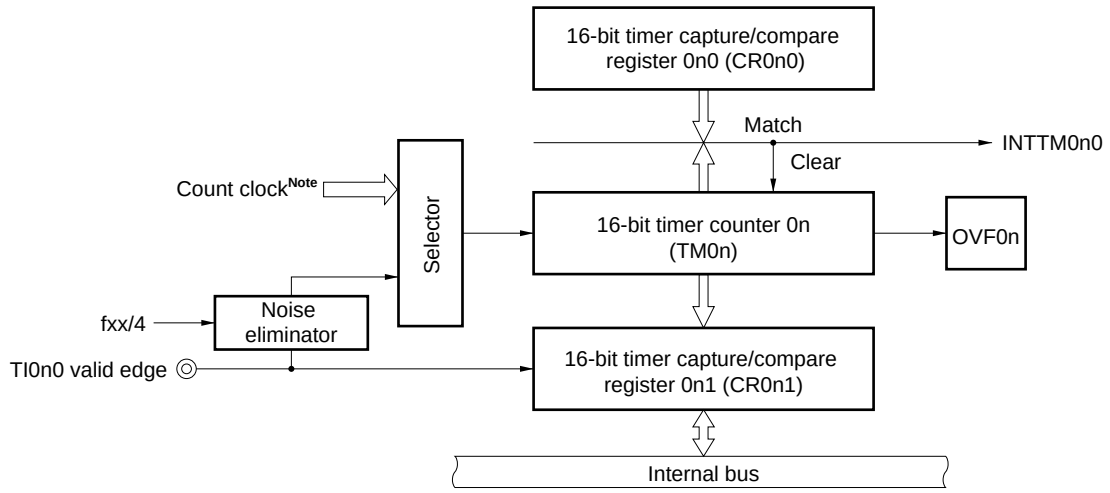


Note Always set TM00 to TM03 to 0.

Remarks 1. 0/1: When these bits are reset to 0 or set to 1, other functions can be used together with the external event counter function. For details, refer to **7.3 (1) 16-bit timer mode control register 0n (TMC0n)** and **7.3 (2) Capture/compare control register 0n (CRC0n)**.

2. n = 0 to 5

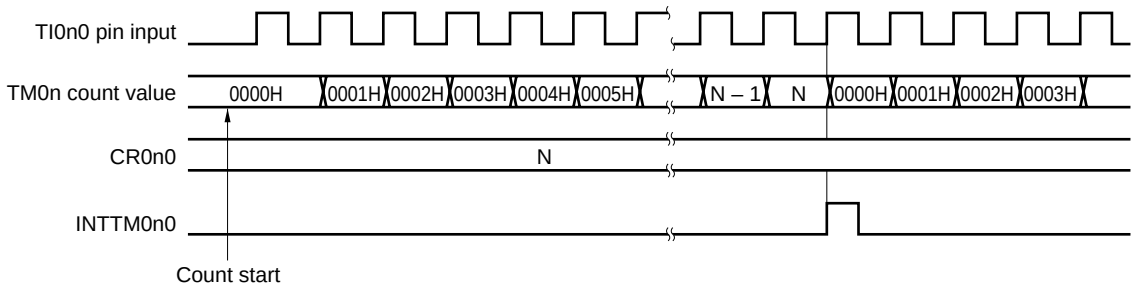
Figure 7-19. Configuration of External Event Counter



Note Set with the PRM0n register.

Remark n = 0 to 5

Figure 7-20. Timing of External Event Counter Operation (with Rising Edge Specified)



Cautions 1. Read the TM0n register when reading the count value of the external event counter.

2. Counting is not possible at the first valid edge after the external event counter mode is entered.

Remark n = 0 to 5

7.4.5 Square-wave output operation

Setting procedure

The basic operation setting procedure is as follows.

<1> Set the count clock using the PRM0n register.
<2> Set the CRC0n register (see **Figure 7-21** for the setting value).
<3> Set the TOC0n register (see **Figure 7-21** for the setting value).
<4> Set any value (except for 0000H) to the CR0n0 register.
<5> Set the TMC0n register: Start operation (see **Figure 7-21** for the setting value).

Remarks 1. For the alternate-function pin (TO0n) settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Function**.

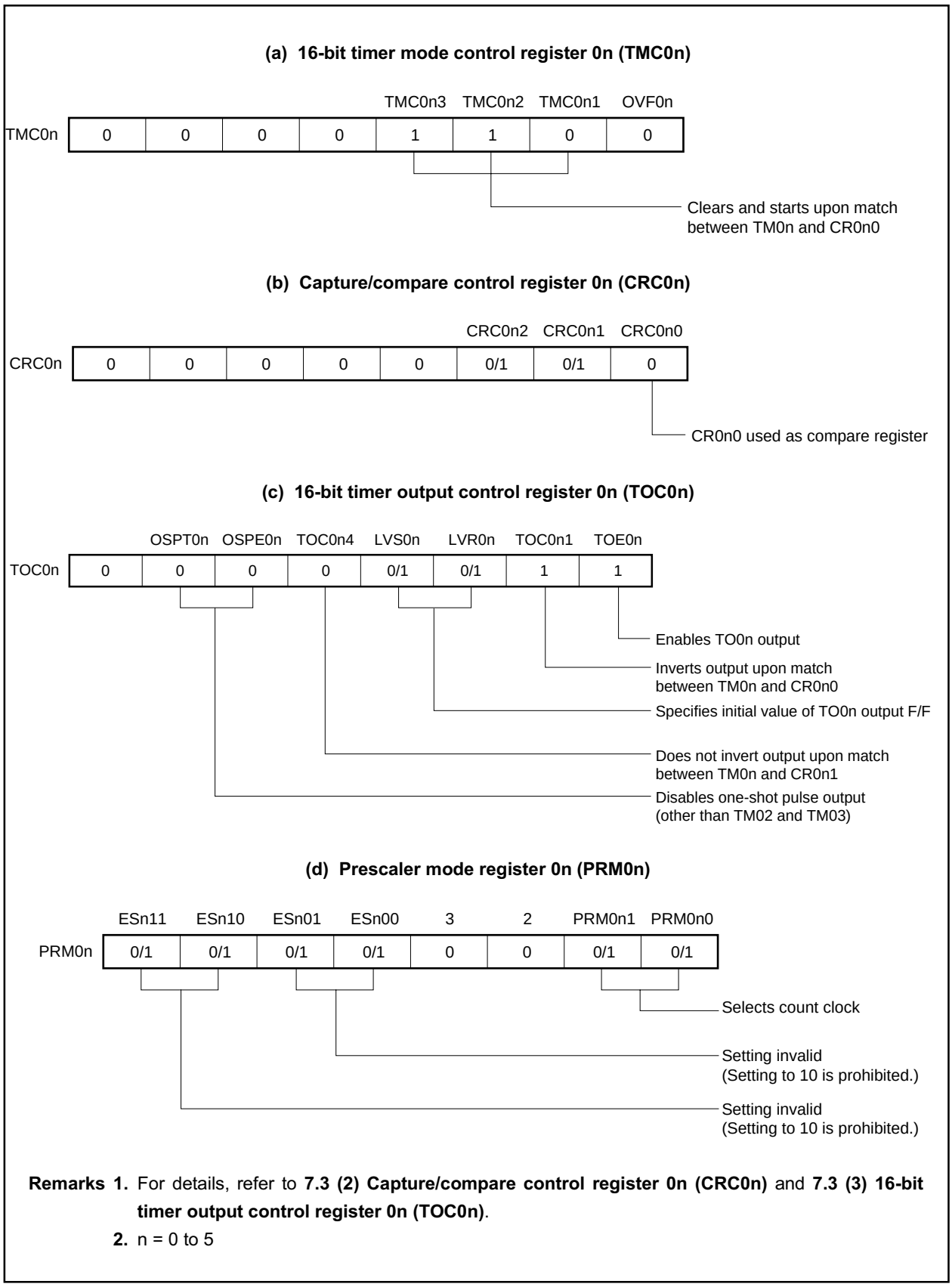
2. For INTTM0n0 interrupt enable, refer to **CHAPTER 19 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

16-bit timer/event counter 0n can be used to output a square wave with any frequency at an interval specified by the count value set in advance to 16-bit timer capture/compare register 0n0 (CR0n0).

By setting bits 0 (TOE0n) and 1 (TOC0n1) of 16-bit timer output control register 0n (TOC0n) to 1, the output status of the TO0n pin is inverted at an interval set in advance to the CR0n0 register. In this way, a square wave of any frequency can be output.

Caution The value of the CR0n0 and CR0n1 registers cannot be changed during timer count operation.

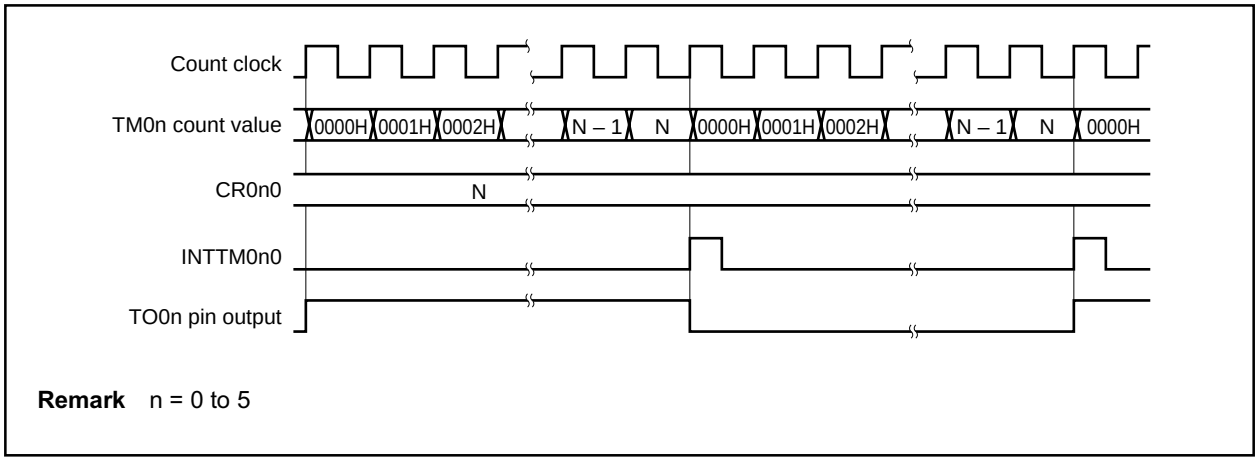
Figure 7-21. Control Register Settings in Square-Wave Output Mode



Remarks 1. For details, refer to **7.3 (2) Capture/compare control register 0n (CRC0n)** and **7.3 (3) 16-bit timer output control register 0n (TOC0n)**.

2. n = 0 to 5

Figure 7-22. Timing of Square-Wave Output Operation



Remark n = 0 to 5

7.4.6 One-shot pulse output operation

The one-shot pulse output is valid only for 16-bit timer/event counters 00, 01, 04, and 05.

16-bit timer/event counter 0n can output a one-shot pulse in synchronization with a software trigger or an external trigger (TI0k0 pin input).

Setting procedure

The basic operation setting procedure is as follows.

<1> Set the count clock using the PRM0m register.
<2> Set the CRC0m register (see **Figures 7-23** and **7-25** for the setting value).
<3> Set the TOC0m register (see **Figures 7-23** and **7-25** for the setting value).
<4> Set any value to the CR0m0 and CR0m1 registers.
<5> Set the TMC0m register: Start operation (see **Figures 7-23** and **7-25** for the setting value).

Remarks 1. For the alternate-function pin (TO0m) settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

2. For INTTM0m0 interrupt enable, refer to **CHAPTER 19 INTERRUPT/EXCEPTION PROCESSING FUNCTION**.

(1) One-shot pulse output with software trigger (16-bit timer/event counters 00, 01, 04, and 05 only)

A one-shot pulse can be output from the TO0m pin by setting 16-bit timer mode control register 0m (TMC0m), capture/compare control register 0m (CRC0m), and 16-bit timer output control register 0m (TOC0m) as shown in Figure 7-23, and by setting bit 6 (OSPT0m) of the TOC0m register to 1 by software.

By setting the OSPT0m bit to 1, 16-bit timer/event counter 0m is cleared and started, and its output becomes active at the count value (N) set in advance to 16-bit timer capture/compare register 0m1 (CR0m1). After that, the output becomes inactive at the count value (M) set in advance to 16-bit timer capture/compare register 0m0 (CR0m0)[Note].

Even after the one-shot pulse has been output, the TM0m register continues its operation. To stop the TM0m register, the TMC0m3 and TMC0m2 bits of the TMC0m register must be set to 00.

Note The case where N < M is described here. When N > M, the output becomes active with the CR0m0 register and inactive with the CR0m1 register.

Cautions 1. Do not set the OSPT0m bit while the one-shot pulse is being output. To output the one-shot pulse again, wait until the current one-shot pulse output is completed.

2. The value of the CR0m0 and CR0m1 registers cannot be changed during timer count operation.

Remark m = 0, 1, 4, 5
k = 4, 5

Figure 7-23. Control Register Settings for One-Shot Pulse Output with Software Trigger (1/2)

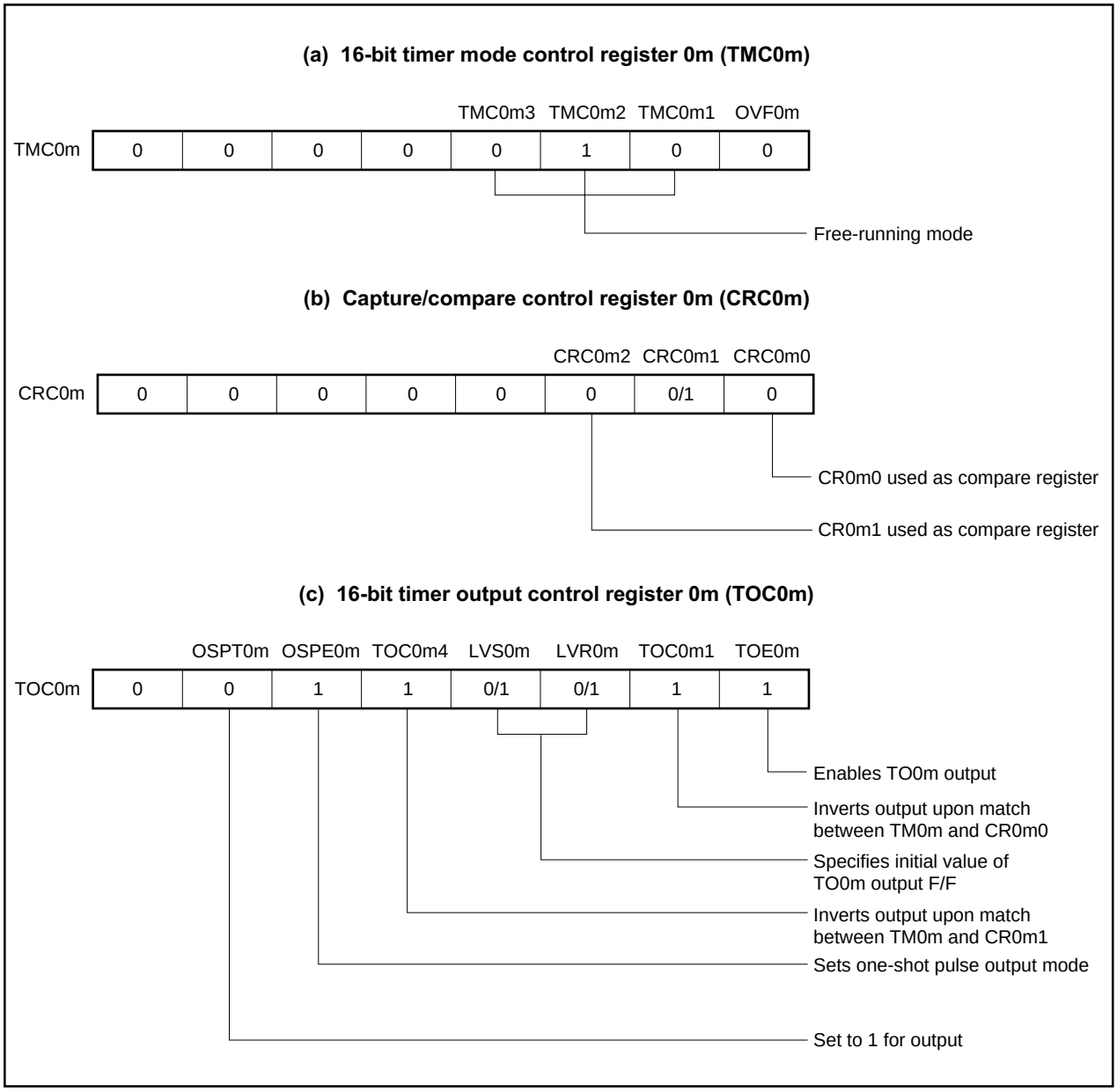


Figure 7-23. Control Register Settings for One-Shot Pulse Output with Software Trigger (2/2)

(d) Prescaler mode register 0m (PRM0m)

	ESm11	ESm10	ESm01	ESm00	3	2	PRM0m1	PRM0m0
PRM0m	0/1	0/1	0/1	0/1	0	0	0/1	0/1

Selects count clock

Setting invalid
(Setting to 10 is prohibited.)

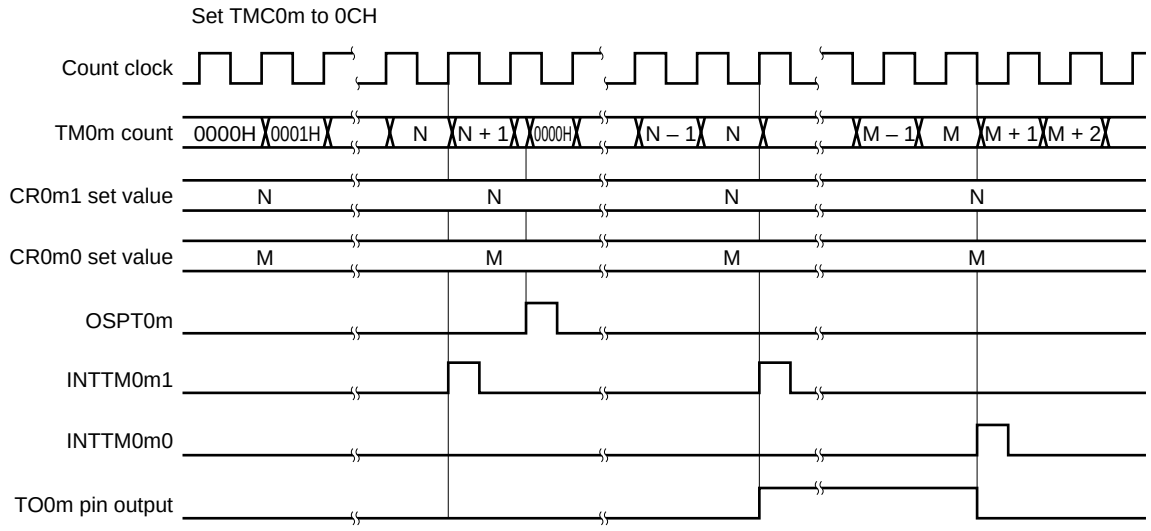
Setting invalid
(Setting to 10 is prohibited.)

Caution Do not set 0000H to the CR0m0 and CR0m1 registers.

Remarks 1. For details, refer to **7.3 (2) Capture/compare control register 0n (CRC0n)** and **7.3 (3) 16-bit timer output control register 0n (TOC0n)**.

2. m = 0, 1, 4, 5

Figure 7-24. Timing of One-Shot Pulse Output Operation with Software Trigger



Caution 16-bit timer counter 0m starts operating as soon as a value other than 00 (operation stop mode) is set to the TMC0m3 and TMC0m2 bits.

Remark m = 0, 1, 4, 5
N < M

(2) One-shot pulse output with external trigger (16-bit timer/event counters 04 and 05 only)

A one-shot pulse can be output from the TO0k pin by setting 16-bit timer mode control register 0k (TMC0k), capture/compare control register 0k (CRC0k), and 16-bit timer output control register 0k (TOC0k) as shown in Figure 7-25, and by using the valid edge of the TI0k0 pin as an external trigger.

The valid edge of the TI0k0 pin is specified by bits 4 and 5 (ESk00, ESk01) of prescaler mode register 0k (PRM0k). The rising, falling, or both the rising and falling edges can be specified.

When the valid edge of the TI0k0 pin is detected, the 16-bit timer/event counter is cleared and started, and the output becomes active at the count value set in advance to 16-bit timer capture/compare register 0k1 (CR0k1). After that, the output becomes inactive at the count value set in advance to 16-bit timer capture/compare register 0k0 (CR0k0)[Note].

Note The case where N < M is described here. When N > M, the output becomes active with the CR0k0 register and inactive with the CR0k1 register.

Cautions 1. Even if the external trigger is generated again while the one-shot pulse is output, it is ignored.

2. The value of the CR0k0 and CR0k1 registers cannot be changed during timer count operation.

Remark k = 4, 5

Figure 7-25. Control Register Settings for One-Shot Pulse Output with External Trigger (with Rising Edge Specified) (1/2)

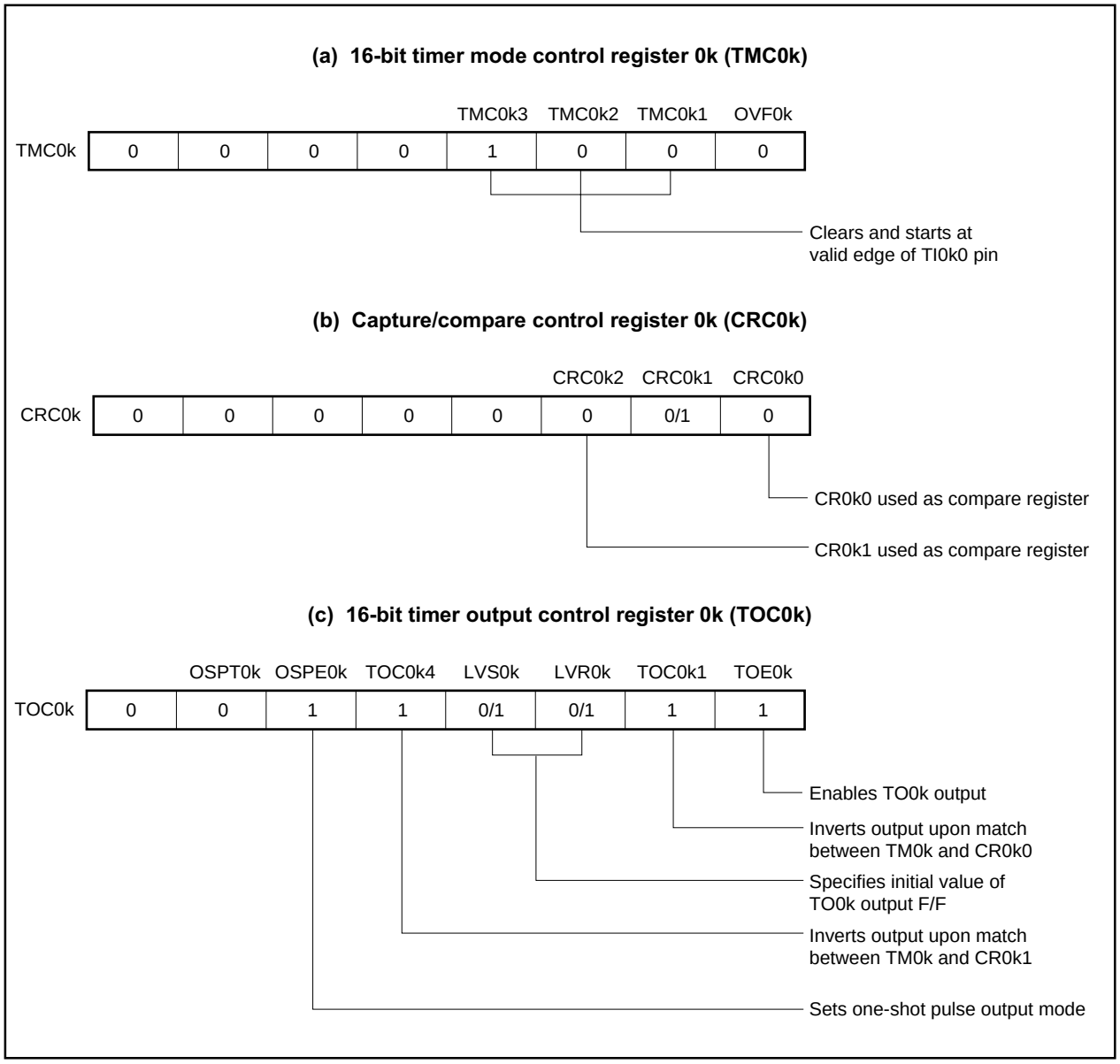


Figure 7-25. Control Register Settings for One-Shot Pulse Output with External Trigger (with Rising Edge Specified) (2/2)

(d) Prescaler mode register 0k (PRM0k)

	ESk11	ESk10	ESk01	ESk00	3	2	PRM0k1	PRM0k0
PRM0k	0/1	0/1	0	1	0	0	0/1	0/1

Selects count clock
(Setting to 11 is prohibited.)

Specifies rising edge of
pulse width detection.

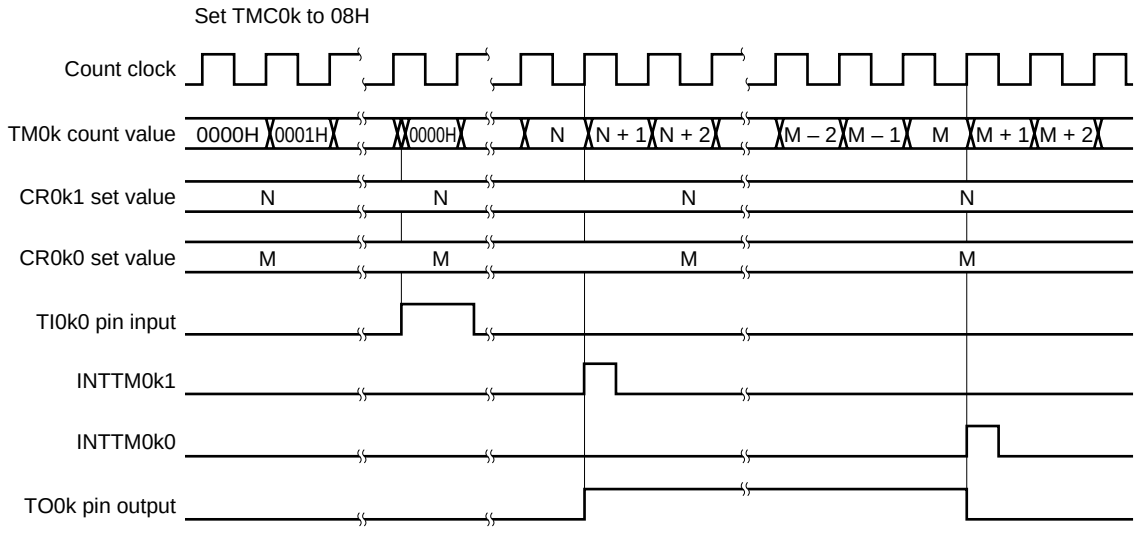
Setting invalid
(Setting to 10 is prohibited.)

Caution Do not set the CR0k0 and CR0k1 registers to 0000H.

Remarks 1. For details, refer to **7.3 (2) Capture/compare control register 0n (CRC0n)** and **7.3 (3) 16-bit timer output control register 0n (TOC0n)**.

2. k = 4, 5

Figure 7-26. Timing of One-Shot Pulse Output Operation with External Trigger (with Rising Edge Specified)



Caution 16-bit timer/event counter 0k starts operating as soon as a value other than 00 (operation stop mode) is set to the TMC0k2 and TMC0k3 bits.

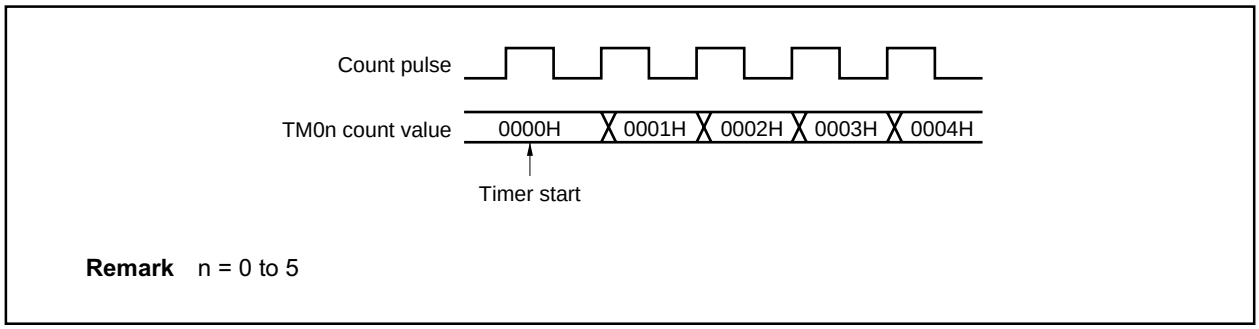
Remark k = 4, 5
N < M

7.4.7 Cautions

(1) Error on starting timer

An error of up to 1 clock occurs before the match signal is generated after the timer has been started. This is because 16-bit timer counter 0n (TM0n) is started asynchronously to the count pulse.

Figure 7-27. Start Timing of 16-Bit Timer Counter 0n



Remark n = 0 to 5

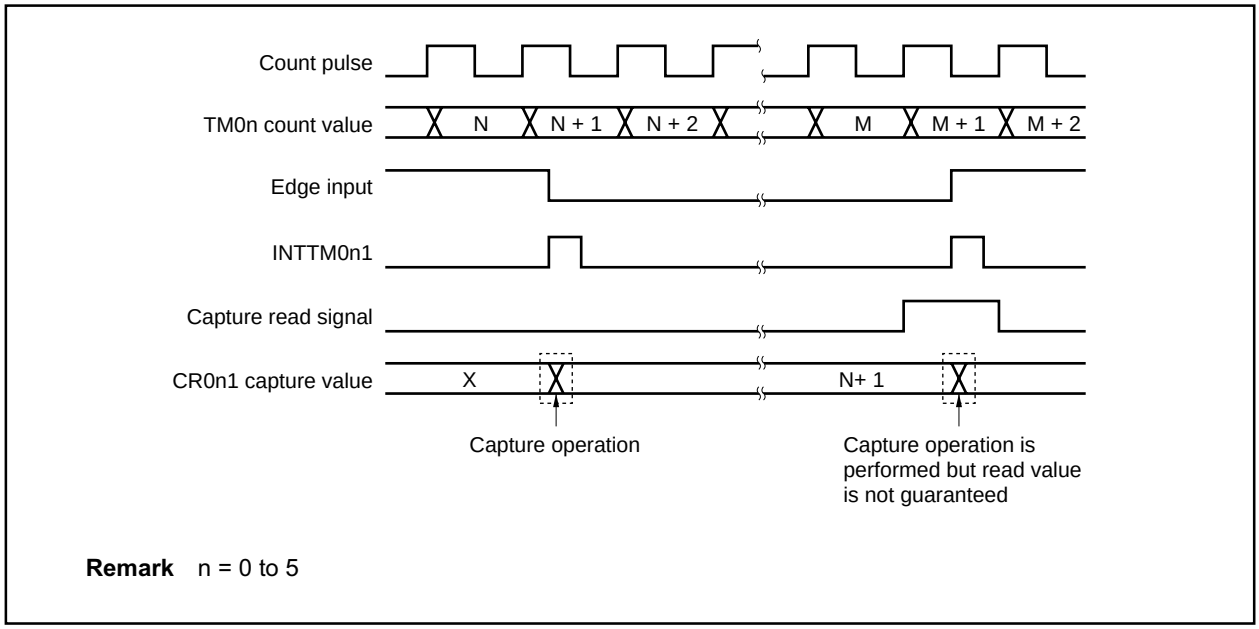
(2) Setting 16-bit timer capture/compare register (in the mode in which clear & start occurs upon match between TM0n register and CR0n0 register)

Set 16-bit timer capture/compare registers 0n0 and 0n1 (CR0n0 and CR0n1) to a value other than 0000H (when using these registers as event counters, one-pulse count operation is not possible).

(3) Data hold timing of capture register

<1> If the valid edge of the TI0n0 pin is input while 16-bit timer capture/compare register 0n1 (CR0n1) is read, the CR0n1 register performs capture operation, but the read value at this time is not guaranteed. However, the interrupt request signal (INTTM0n1) is generated as a result of detection of the valid edge.

Figure 7-28. Data Hold Timing of Capture Register



Remark n = 0 to 5

<2> The values of the CR0n0 and CR0n1 registers are not guaranteed after 16-bit timer/event counter 0n has stopped.

(4) Setting valid edge

Before setting the valid edge of the TI0n0 pin, stop the timer operation by setting bits 2 and 3 (TMC0n2 and TMC0n3) of 16-bit timer mode control register 0n to 0, 0. Set the valid edge by using bits 4 and 5 (ESn00 and ESn01) of prescaler mode register 0n (PRM0n).

(5) Re-triggering one-shot pulse

(a) One-shot pulse output by software (TM00, TM01, TM04, TM05)

When a one-shot pulse is output, do not set the OSPT0m bit to 1. Do not output the one-shot pulse again until INTTM0m0, which occurs upon match with the CR0m0 register, or INTTM0m1, which occurs upon match with the CR0m1 register, occurs.

Remark m = 4, 5

(b) One-shot pulse output with external trigger (TM04, TM05)

If the external trigger occurs again while a one-shot pulse is output, it is ignored.

(c) One-shot pulse output function

When using the one-shot pulse output of timer 0 with a software trigger, do not change the level of the TI0m0 pin or its alternate function port pin.

Because the external trigger is effective even in this case, the timer is cleared and started even with the TI0m0 pin or its alternate function port pin level, resulting in the output of a pulse at an undesired timing.

Remark m = 4, 5

(6) Operation of OVF0n flag

(a) Setting of OVF0n flag

The OVF0n flag is set to 1 in the following case in addition to when the TM0n register overflows.

Select the mode in which clear & start occurs upon match between the TM0n register and the CR0n0 register.

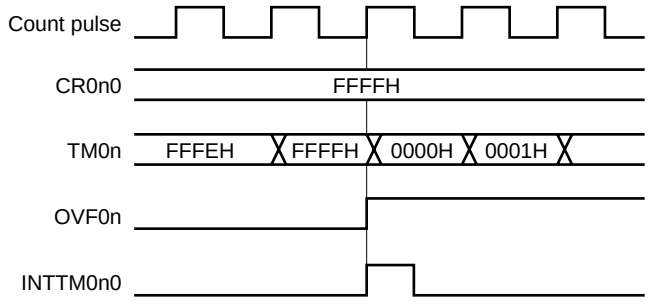
↓

Set the CR0n0 register to FFFFH

↓

When the TM0n register is cleared from FFFFH to 0000H upon match with the CR0n register

Figure 7-29. Operation Timing of OVF0n Flag



Remark n = 0 to 5

(b) Clearing of OVF0n flag

After the TM0n register overflows, clearing OVF0n flag is invalid and set again even if the OVF0n flag is cleared before the next count clock is counted (before TM0n register becomes 0001H).

Remark n = 0 to 5

(7) Timer operation

(a) CR0n1 register capture

Even if 16-bit timer counter 0n (TM0n) is read, the read data cannot be captured into 16-bit timer capture/compare register 0n1 (CR0n1).

(b) TI0n0, TI0n1 pin acknowledgment

Regardless of the CPU's operation mode, if the timer is stopped, signals input to the TI0n0 and TI0n1 pins are not acknowledged.

(c) One-shot pulse output (TM00, TM01, TM04, TM05)

One-shot pulse output operates normally in either the free-running mode or the mode in which clear & start occurs on the valid edge of the TI0k0 pin. Because no overflow occurs in the mode in which clear & start occurs upon match between the TM0m register and the CR0m0 register, one-shot pulse output is not possible.

Remark n = 0 to 5
m = 0, 1, 4, 5
k = 4, 5

(8) Capture operation

(a) If valid edge of TI0n0 is specified for count clock

If the valid edge of TI0n0 is specified for the count clock, the capture register that specified TI0n0 as the trigger does not operate normally.

(b) If both rising and falling edges are selected for valid edge of TI0n0

If both the rising and falling edges are selected for the valid edge of TI0n0, capture operation is not performed.

(c) To ensure that signals from TI0n1 and TI0n0 are correctly captured

For the capture trigger to capture the signals from TI0n1 and TI0n0 correctly, a pulse longer than two of the count clocks selected by prescaler mode register 0n (PRM0n) is required.

(d) Interrupt request input

Although a capture operation is performed at the falling edge of the count clock, an interrupt request signal (INTTM0n0, INTTM0n1) is generated at the rising edge of the next count clock.

Remark n = 0 to 5

(9) Compare operation

When set to the compare mode, the CR0n0 and CR0n1 registers do not perform capture operation even if a capture trigger is input.

Caution The value of the CR0n0 register cannot be changed during timer operation. The value of the CR0n1 register cannot be changed during timer operation other than in the PPG output mode. To change the CR0n1 register in the PPG output mode, refer to 7.4.2 PPG output operation.

Remark n = 0 to 5

(10) Edge detection

(a) Sampling clock for noise elimination

The sampling clock for noise elimination differs depending on whether the valid edge of TI0n0 is used for the count clock or as a capture trigger. In the former case, sampling is performed using $f_{XX}/4$, and in the latter case, sampling is performed using the count clock selected by prescaler mode register 0n (PRM0n). The first capture operation does not start until the valid edges are sampled and two valid levels are detected, thus eliminating noise with a short pulse width.

Remarks 1. f_{XX}: Main clock frequency

2. n = 0 to 5

CHAPTER 8 8-BIT TIMER/EVENT COUNTERS 50 AND 51

Two 8-bit timer/event counter 50 and 51 channels are incorporated in each product.

Product Name	V850ES/KF1	V850ES/KG1	V850ES/KJ1
Number of channels	2 channels (TM50, TM51)		

8.1 Functions

8-bit timer/event counter 5n has the following two modes (n = 0, 1).

- Mode using 8-bit timer/event counter alone (individual mode)
- Mode using cascade connection (16-bit resolution: cascade connection mode)

These two modes are described below.

(1) Mode using 8-bit timer/event counter alone (individual mode)

8-bit timer/event counter 5n operates as an 8-bit timer/event counter.
The following functions can be used.

- Interval timer
- External event counter
- Square-wave output
- PWM output

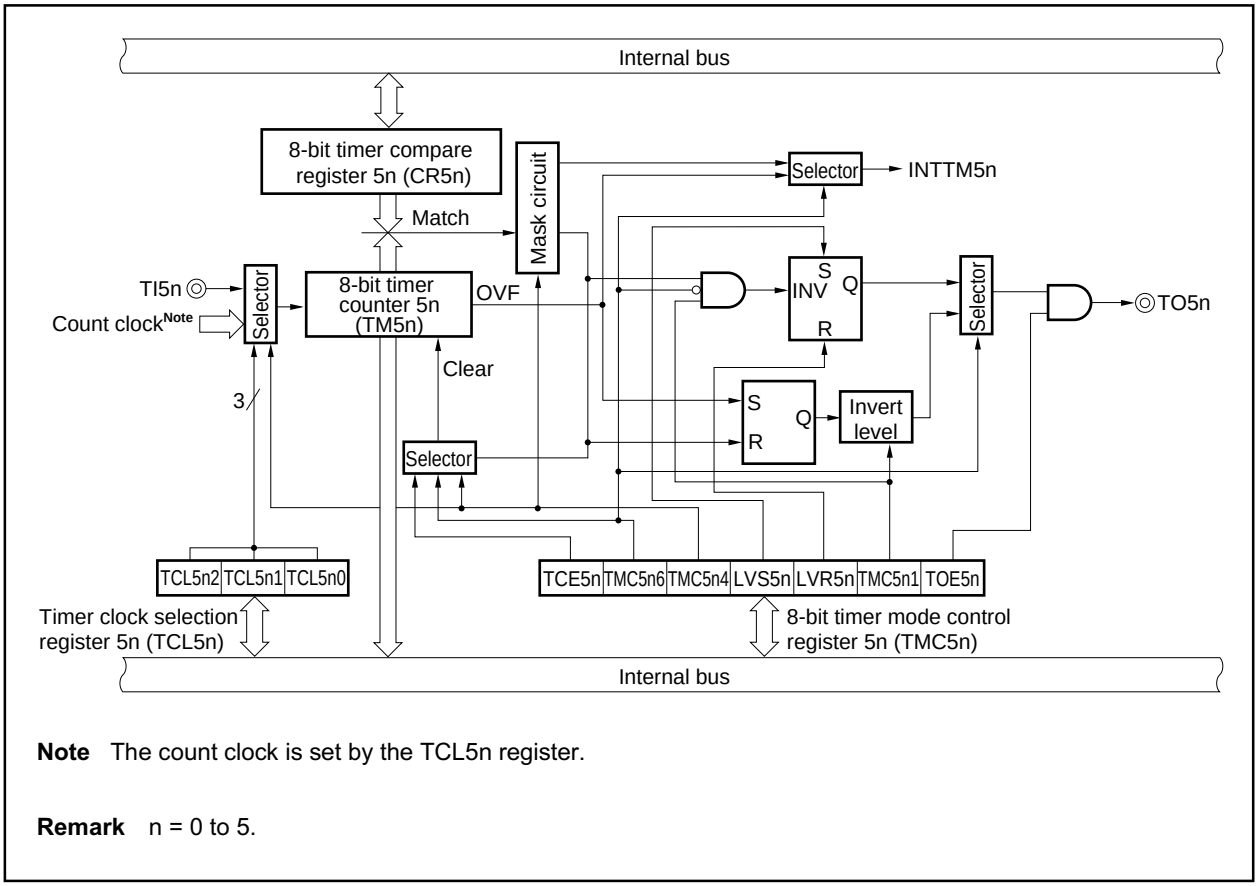
(2) Mode using cascade connection (16-bit resolution: cascade connection mode)

8-bit timer/event counters 50 and 51 operate as a 16-bit timer/event counter by connecting the TM50 and TM51 registers in cascade. The following functions can be used.

- Interval timer with 16-bit resolution
- External event counter with 16-bit resolution
- Square-wave output with 16-bit resolution

The block diagram of 8-bit timer/event counters 50 and 51 is shown next.

Figure 8-1. Block Diagram of 8-Bit Timer/Event Counters 50 and 51



Note The count clock is set by the TCL5n register.

Remark n = 0 to 5.

8.2 Configuration

8-bit timer/event counters 50 and 51 consist of the following hardware.

Table 8-1. Configuration of 8-Bit Timer/Event Counters 50 and 51

Item	Configuration
Timer registers	8-bit timer counters 50 and 51 (TM50, TM51) 16-bit timer counter 5 (TM5): Only when using cascade connection
Registers	8-bit timer compare registers 50, 51 (CR50, CR51) 16-bit timer compare register 5 (CR5): Only when using cascade connection
Timer output	TO50, TO51
Control registers Note	Timer clock selection registers 50, 51 (TCL50, TCL51) 8-bit timer mode control registers 50, 51 (TMC50, TMC51) 16-bit timer mode control register 5 (TMC5): Only when using cascade connection

Note When using the functions of the TI5n and TO5n pins, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

(1) 8-bit timer counters 50 and 51 (TM50, TM51)

The TM5n register is an 8-bit read-only register that counts the count pulses.

The counter is incremented in synchronization with the rising edge of the count clock.

Through cascade connection, the TM5n registers can be used as a 16-bit timer.

When using the TM50 register and the TM51 register in cascade as a 16-bit timer, these registers can be read by a 16-bit memory manipulation instruction. Therefore, read these registers twice and compare the values, taking into consideration that the reading occurs during a count change.

In the following cases, the count value becomes 00H.

After reset: 00H R Address: TM50: FFFFF5C0H, TM51: FFFFF5C1H

	7	6	5	4	3	2	1	0
TM5n (n = 0, 1)								

- Reset
- When the TCE5n bit of 8-bit timer mode control register 5n (TMC5n) is cleared
- The TM5n register and CR5n register match in the mode in which clear & start occurs on a match between the TM5n register and 8-bit timer compare register 5n (CR5n)

Caution When connected in cascade, these registers become 0000H even when the TCE50 bit in the lowest timer (TM50) is cleared.

Remark n = 0, 1

(2) 8-bit timer compare registers 50 and 51 (CR50, CR51)

The CR5n register can be read and written by an 8-bit memory manipulation instruction.

In a mode other than the PWM mode, the value set to the CR5n register is always compared to the count value of 8-bit counter 5n (TM5n), and if the two values match, an interrupt request signal (INTTM5n) is generated.

In the PWM mode, TM5n register overflow causes the TO5n pin output to change to the active level, and when the values of the TM5n register and the CR5n register match, the TO5n pin output changes to the inactive level.

The value of the CR5n register can be set in the range of 00H to FFH.

When using the TM50 register and TM51 register in cascade as a 16-bit timer, the CR50 register and CR51 register operate as 16-bit timer compare register 5 (CR5). The counter value and register value are compared in 16-bit lengths, and if they match, an interrupt request (INTTM50) is generated.

After reset: 00H R/W Address: CR50: FFFFF5C2H, CR51: FFFFF5C3H

	7	6	5	4	3	2	1	0
CR5n								

(n = 0, 1)

Cautions 1. In the mode in which clear & start occurs upon a match of the TM5n register and CR5n register (TMC5n6 =0), do not write a different value to the CR5n register during the count operation.

2. In the PWM mode, set the CR5n register rewrite interval to three or more count clocks (clock selected with timer clock selection register 5n (TCL5n)).

3. Before changing the value of the CR5n register when using a cascade connection, be sure to stop the timer operation.

Remark n = 0, 1

8.3 Control Registers

The following two registers are used to control 8-bit timer/event counter 5n.

- Timer clock selection register 5n (TCL5n)
- 8-bit timer mode control register 5n (TMC5n)

Remark To use the functions of the TI5n and TO5n pins, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

(1) Timer clock selection registers 50 and 51 (TCL50, TCL51)

These registers set the count clock of 8-bit timer/event counter 5n and the valid edge of the TI5n pin input.

The TCL5n register is set by an 8-bit memory manipulation instruction.

After reset, this register is cleared to 00H.

After reset: 00H R/W Address: TCL50 FFFFF5C4H, TCL51 FFFFF5C5H

	7	6	5	4	3	2	1	0
TCL5n	0	0	0	0	0	TCL5n2	TCL5n1	TCL5n0

(n = 0, 1)

TCL5n2	TCL5n1	TCL5n0	Count clock selection[Note]		
			Clock	f_{XX}	
				20 MHz	10 MHz
0	0	0	Falling edge of TI5n	–	–
0	0	1	Rising edge of TI5n	–	–
0	1	0	f_{XX}	Setting prohibited	100 ns
0	1	1	$f_{XX}/2$	100 ns	200 ns
1	0	0	$f_{XX}/4$	200 ns	0.4 μs
1	0	1	$f_{XX}/64$	3.2 μs	6.4 μs
1	1	0	$f_{XX}/256$	12.8 μs	25.6 μs
1	1	1	INTTM010	–	–

Note When the internal clock is selected, set so as to satisfy the following conditions.

V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz

V_{DD} = 2.7 to 4.0 V: Count clock ≤ 5 MHz

Caution Before overwriting the TCL5n register with different data, stop the timer operation.

Remark When TM50 and TM51 are connected in cascade, the TCL51 register settings are invalid.

(2) 8-bit timer mode control registers 50 and 51 (TMC50, TMC51)

The TMC5n register performs the following six settings.

- Controls counting by 8-bit timer counters 50 and 51 (TM50, TM51)
- Selects the operation mode of the TM50 and TM51 registers
- Selects the individual mode or cascade connection mode
- Sets the status of the timer output flip-flop
- Controls the timer output flip-flop or selects the active level in the PWM (free-running) mode
- Controls timer output

The TMC50 and TMC51 registers are set by an 8-bit or 1-bit memory manipulation instruction.

After reset, these registers are cleared to 00H.

After reset: 00H R/W Address: TMC50 FFFFF5C6H TMC51 FFFFF5C7H

TMC5n (n = 0, 1)

	<7>	6	5	4	3	2	1	<0>
TMC5n	TCE5n	TMC5n6	0	TMC514[Note]	LVS5n	LVR5n	TMC5n1	TOE5n

TCE5n	Control of count operation of 8-bit timer/event counter 5n
0	Counting is disabled after the counter is cleared to 0 (counter disabled)
1	Start count operation

TMC5n6	Selection of operation mode of 8-bit timer/event counter 5n
0	Mode in which clear & start occurs on match between TM5n register and CR5n register
1	PWM (free-running) mode

TMC514	Selection of individual mode or cascade connection mode for 8-bit timer/event counter 51
0	Individual mode
1	Cascade connection mode (connected with TM50)

LVS5n	LVR5n	Setting of status of timer output F/F
0	0	Unchanged
0	1	Reset timer output F/F to 0
1	0	Set timer output F/F to 1
1	1	Setting prohibited

TMC5n1	Other than PWM (free-running) mode (TMC5n6 = 0)	PWM (free-running) mode (TMC5n6 = 1)
	Controls timer F/F	Selects active level
0	Disable inversion operation	High active
1	Enable inversion operation	Low active

TOE5n	Timer output control
0	Disable output (TO5n pin is low level)
1	Enable output

Note Bit 4 of the TMC50 register is fixed to 0.

Cautions 1. Because the TO51 and TI51 pins are alternate functions of the same pin, only one can be used at one time.

2. The LVS5n and LVR5n bit settings are valid in modes other than the PWM mode.

★ **3. Do not set <1> to <4> below at the same time. Set as follows.**

<1> Set the TMC5n1, TMC5n6, and TMC514[Note] bits: Setting of operation mode

<2> Set the TOE5n bit for timer output enable: Timer output enable

<3> Set the LVS5n and LVR5n bits (Caution 2): Setting of timer output F/F

<4> Set the TCE5n bit

Remarks 1. In the PWM mode, the PWM output is set to the inactive level by TCE5n = 0.

2. When the LVS5n and LVR5n bits are read, 0 is read.

3. The values of the TMC5n6, LVS5n, LVR5n, TMC5n1, and TOE5n bits are reflected to the TO5n output regardless of the TCE5n value.

8.4 Operation

8.4.1 Operation as interval timer (8 bits)

8-bit timer/event counter 5n operates as an interval timer that repeatedly generates interrupts at the interval of the count value preset in 8-bit timer compare register 5n (CR5n). If the count value in 8-bit timer counter 5n (TM5n) matches the value set in the CR5n register, the value of the TM5n register is cleared to 0 and counting is continued, and at the same time, an interrupt request signal (INTTM5n) is generated.

Setting method

<1> Set each register.
- TCL5n register: Selects the count clock (t).
- CR5n register: Compare value (N)
- TMC5n register: Stops count operation and selects the mode in which clear & start occurs on a match between the TM5n register and CR5n register (TMC5n register = 0000xx00B, ×: don't care).

<2> When the TCE5n bit of the TMC5n register is set to 1, the count operation starts.

<3> When the values of the TM5n register and CR5n register match, INTTM5n is generated (TM5n register is cleared to 00H).

<4> Then, INTTM5n is repeatedly generated at the same interval. To stop counting, set TCE5n = 0.

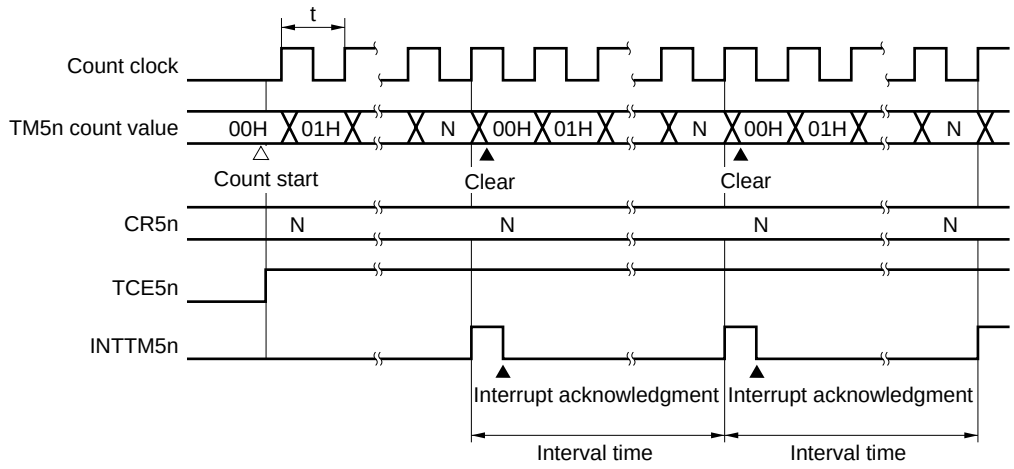
Interval time = (N + 1) × t: N = 00H to FFH

Caution During interval timer operation, do not rewrite the value of the CR5n register.

Remark n = 0, 1

Figure 8-2. Timing of Interval Timer Operation (1/2)

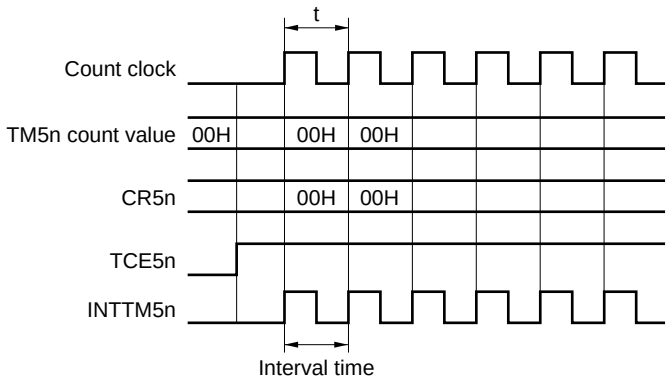
Basic operation



Remark n = 0, 1

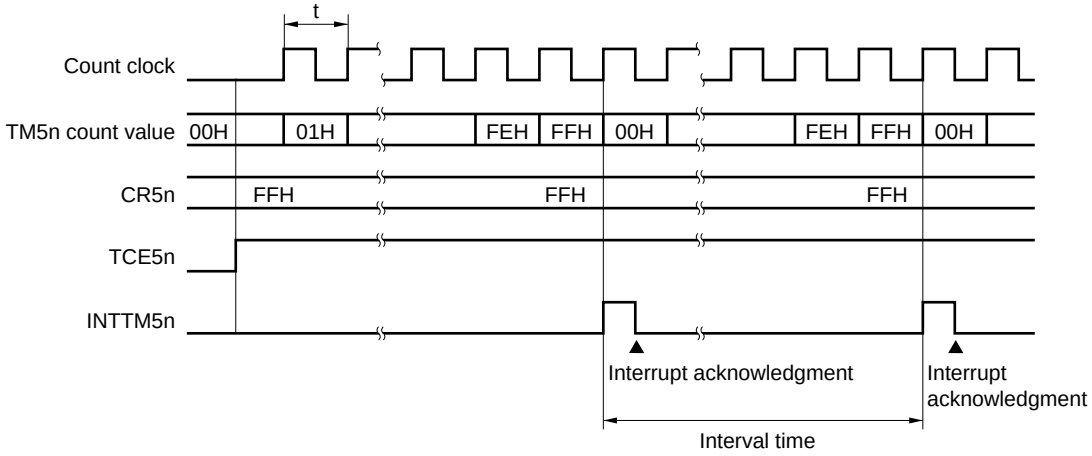
Figure 8-2. Timing of Interval Timer Operation (2/2)

When CR5n register = 00H



Remark n = 0, 1

When CR5n register = FFH



Remark n = 0, 1

8.4.2 Operation as external event counter (8 bits)

The external event counter counts the number of clock pulses input to the TI5n pin from an external source by using 8-bit timer counter 5n (TM5n).

Each time the valid edge specified by timer clock selection register 5n (TCL5n) is input to the TI5n pin, the TM5n register is incremented. Either the rising edge or the falling edge can be specified as the valid edge.

When the count value of the TM5n register matches the value of 8-bit timer compare register 5n (CR5n), the TM5n register is cleared to 0 and an interrupt request signal (INTTM5n) is generated.

Setting method

<1> Set each register.

- TCL5n register: Selects the TI5n input edge.
  Falling edge of TI5n pin → TLC5n = 00H
  Rising edge of TI5n pin → TCL5n = 01H
- CR5n register: Compare value (N)
- TMC5n register: Stops count operation, selects the mode in which clear & start occurs on a match between the TM5n register and CR5n register, disables timer output F/F inversion operation, and disables timer output.
  (TMC5n register = 0000xx00B, ×: don't care)
- For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions.**

<2> When the TCE5n bit of the TMC5n register is set to 1, the counter counts the number of pulses input from TI5n.

<3> When the values of the TM5n register and CR5n register match, INTTM5n is generated (TM5n register is cleared to 00H).

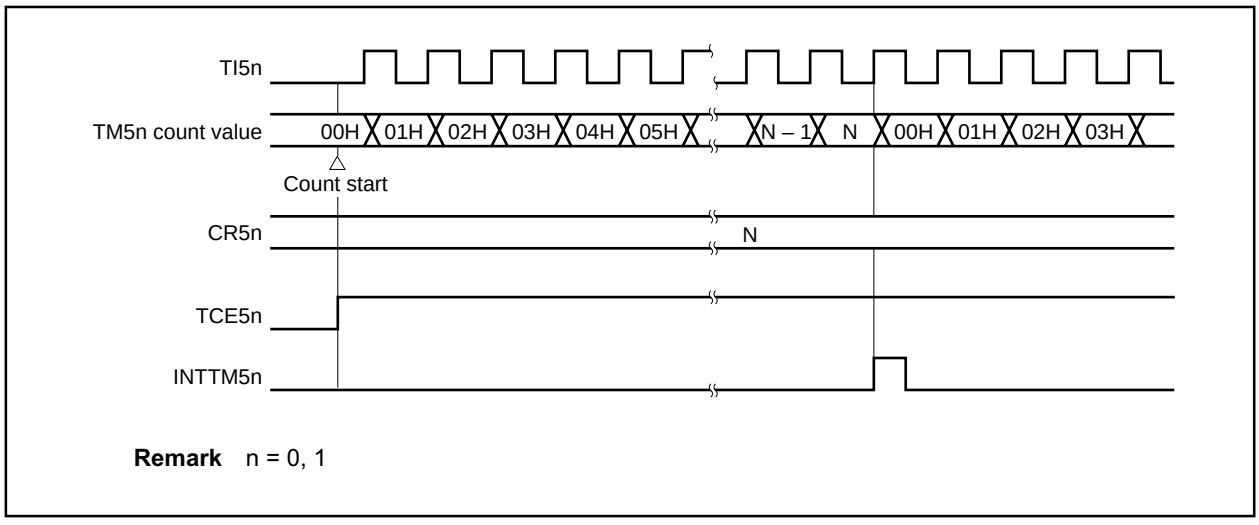
<4> Then, INTTM5n is generated each time the values of the TM5n register and CR5n register match.

INTTM5n is generated when the valid edge of TI5n is input N + 1 times: N = 00H to FFH

Caution During external event counter operation, do not rewrite the value of the CR5n register.

Remark n = 0, 1

Figure 8-3. Timing of External Event Counter Operation (with Rising Edge Specified)



Remark n = 0, 1

8.4.3 Square-wave output operation (8-bit resolution)

A square wave with any frequency can be output at an interval determined by the value preset in 8-bit timer compare register 5n (CR5n).

By setting the TOE5n bit of 8-bit timer mode control register 5n (TMC5n) to 1, the output status of the TO5n pin is inverted at an interval determined by the count value preset in the CR5n register. In this way, a square wave of any frequency can be output (duty = 50%) (n = 0, 1).

Setting method

<1> Set each register.
- TCL5n register: Selects the count clock (t).
- CR5n register: Compare value (N)
- TMC5n register: Stops count operation, selects the mode in which clear & start occurs on a match between the TM5n register and CR5n register, sets initial value of timer output, enables timer output F/F inversion operation, and enables timer output.
  (TMC5n register = 00001011B or 00000111B)
- For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions.**

<2> When the TCE5n bit of the TMC5n register is set to 1, counting starts.

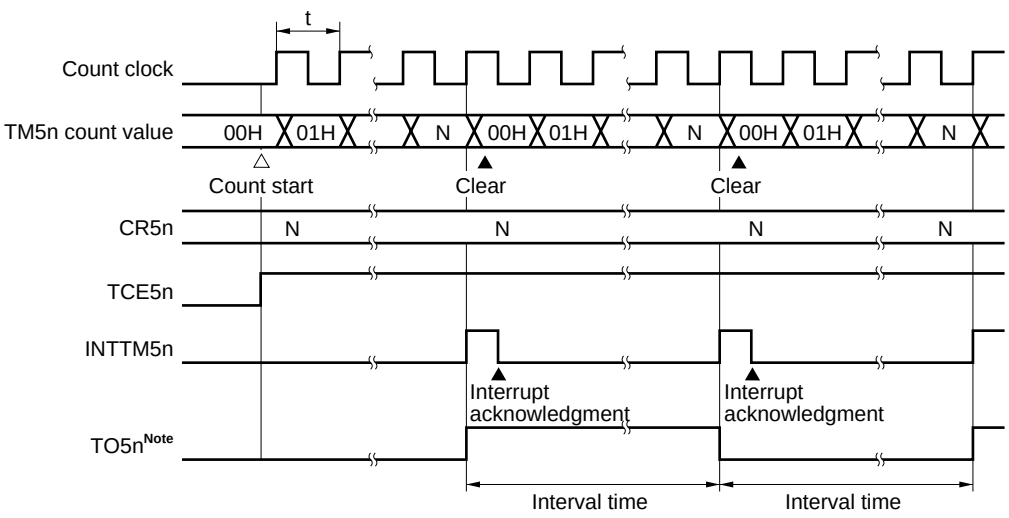
<3> When the values of the TM5n register and CR5n register match, the timer output F/F is inverted.
Moreover, INTTM5n is generated and the TM5n register is cleared to 00H.

<4> Then, the timer F/F is inverted during the same interval and a square wave is output from the TO5n pin.

Frequency = 1/2t(N + 1): N = 00H to FFH

Caution Do not rewrite the value of the CR5n register during square-wave output.

Figure 8-4. Timing of Square-Wave Output Operation



Note The initial value of the TO5n output can be set using the LVS5n and LVR5n bits of the TMC5n register.

Remark n = 0, 1

8.4.4 8-bit PWM output operation

By setting the TMC5n6 bit of 8-bit timer mode control register 5n (TMC5n) to 1, 8-bit timer/event counter 5n performs PWM output.

Pulses with a duty factor determined by the value set in 8-bit timer compare register 5n (CR5n) are output from the TO5n pin.

Set the width of the active level of the PWM pulse in the CR5n register. The active level can be selected using the TMC5n1 bit of the TMC5n register.

The count clock can be selected using timer clock selection register 5n (TCL5n).

PWM output can be enabled/disabled by the TOE5n bit of the TMC5n register.

Caution The CR5n register rewrite interval must be three or more operation clocks (set by the TCL5n register).

Use method

<1> Set each register.

- TCL5n register: Selects the count clock (t).
- CR5n register: Compare value (N)
- TMC5n register: Stops count operation, selects PWM mode, and leave timer output F/F unchanged, sets active level, and enables timer output.
  (TMC5n register = 01000001B or 01000011B)

- For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions.**

<2> When the TCE5n bit of the TMC5n register is set to 1, counting starts.

PWM output operation

<1> When counting starts, PWM output (output from the TO5n pin) outputs the inactive level until an overflow occurs.

<2> When an overflow occurs, the active level set by setting method <1> is output. The active level is output until the value of the CR5n register and the count value of 8-bit timer counter 5n (TM5n) match.

<3> When the value of the CR5n register and the count value match, the inactive level is output and continues to be output until an overflow occurs again.

<4> Then, steps <2> and <3> are repeated until counting is stopped.

<5> When counting is stopped by setting TCE5n to 0, PWM output becomes inactive.

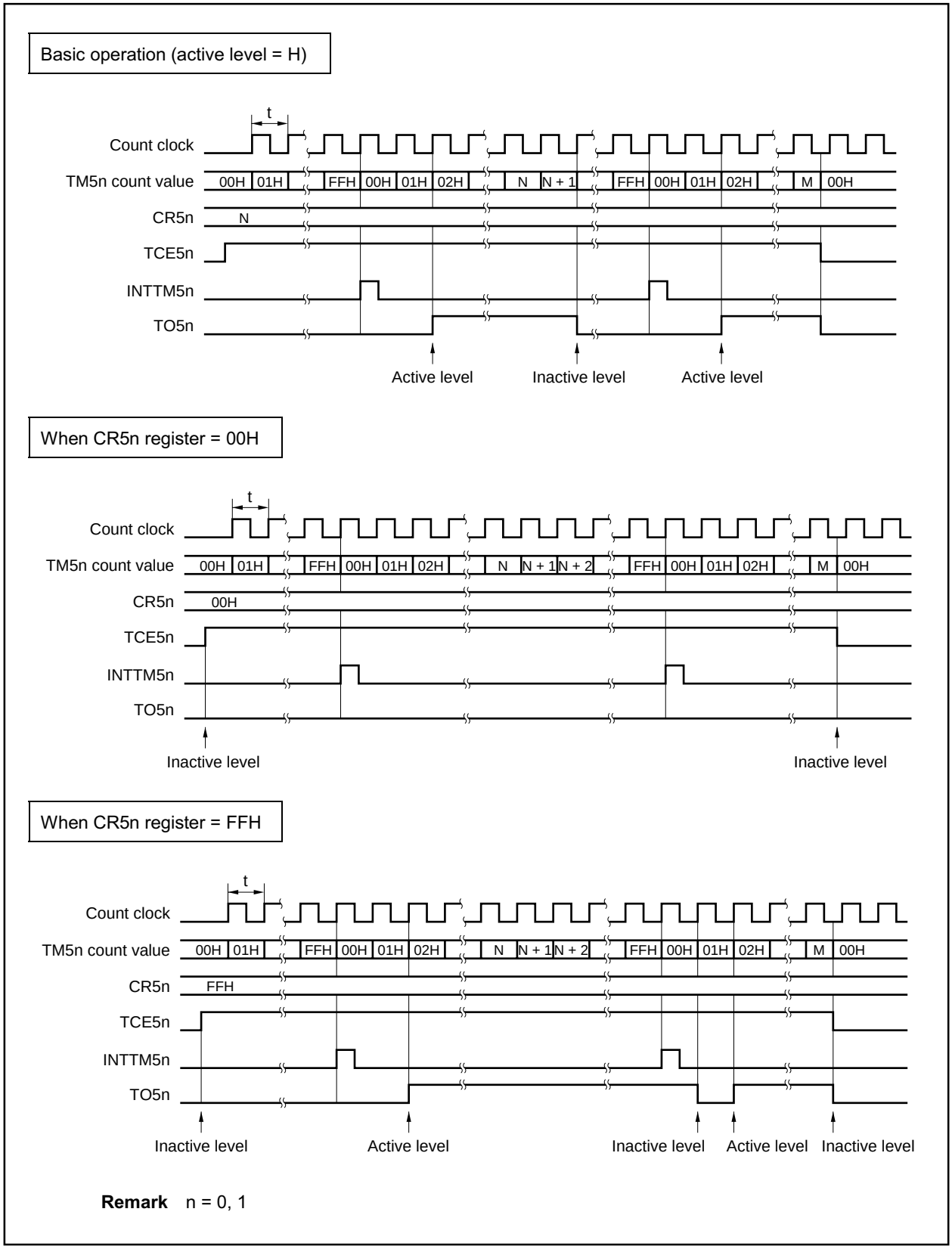
Cycle = 2^8t, active level width = Nt, duty = N/2^8: N = 00H to FFH

Remarks 1. n = 0, 1

2. For the detailed timing, refer to **Figure 8-5 Timing of PWM Output Operation** and **Figure 8-6 Timing of Operation Based on CR5n Register Transitions**.

(a) Basic operation of PWM output

Figure 8-5. Timing of PWM Output Operation



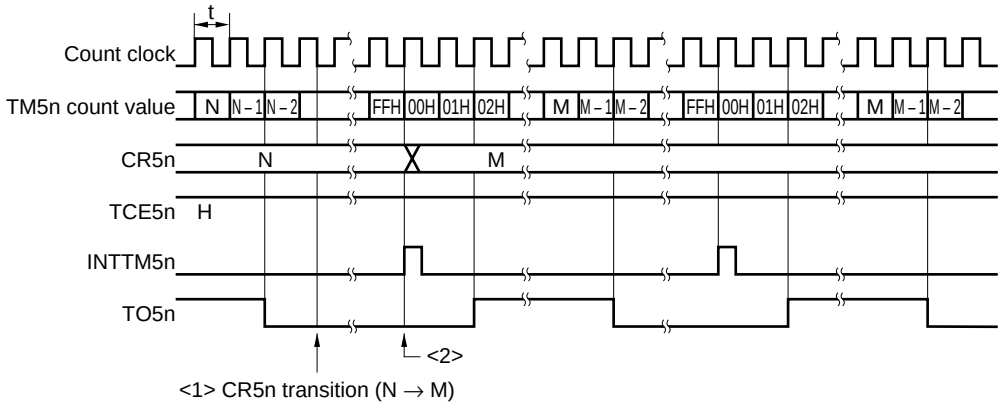
Remark n = 0, 1

(b) Operation based on CR5n register transitions

Figure 8-6. Timing of Operation Based on CR5n Register Transitions

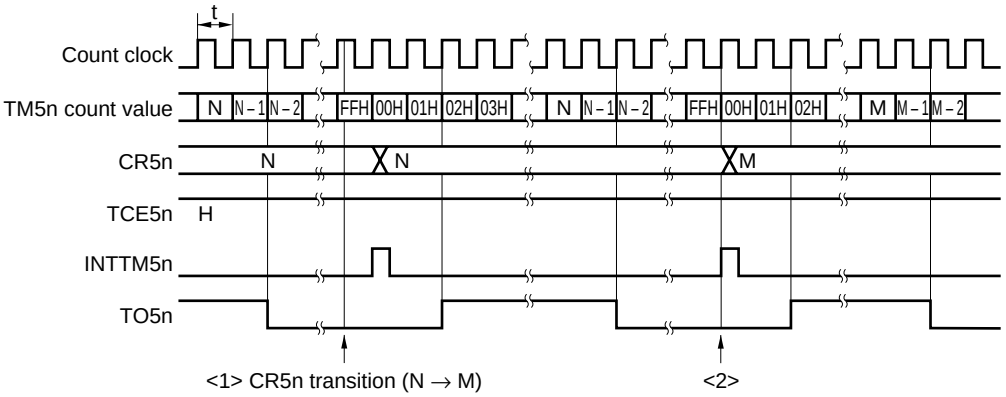
When the value of the CR5n register changes from N to M before the rising edge of the FFH clock

→ The value of the CR5n register is transferred at the overflow that occurs immediately after.



When the value of the CR5n register changes from N to M after the rising edge of the FFH clock

→ The value of the CR5n register is transferred at the second overflow.



Caution In the case of reload from the CR5n register between <1> and <2>, the value that is actually used differs (Read value: M; Actual value of CR5n register: N).

Remark n = 0, 1

8.4.5 Operation as interval timer (16 bits)

The 16-bit resolution timer/event counter mode is selected by setting the TMC514 bit of 8-bit timer mode control register 51 (TMC51) to 1.

8-bit timer/event counter 5n operates as an interval timer by repeatedly generating interrupts using the count value preset in 16-bit timer compare register 5 (CR5) as the interval.

Setting method

<1> Set each register.

- TCL50 register: Selects the count clock (t)
  (The TCL51 register does not need to be set in cascade connection)
- CR50 register: Compare value (N) ... Lower 8 bits (settable from 00H to FFH)
- CR51 register: Compare value (N) ... Higher 8 bits (settable from 00H to FFH)
- TMC50, TMC51 register: Selects the mode in which clear & start occurs on a match between TM5 register and CR5 register (×: don't care)
  (TMC50 register = 0000xx00B
  TMC51 register = 0001xx00B)

<2> Set the TCE51 bit of the TMC51 register to 1. Then set the TCE50 bit of the TMC50 register to 1 to start the count operation.

<3> When the values of the TM5 register and CR5 register connected in cascade match, INTTM50 is generated (the TM5 register is cleared to 0000H).

<4> INTTM50 is then generated repeatedly at the same interval.

Interval time = (N + 1) × t: N = 0000H to FFFFH

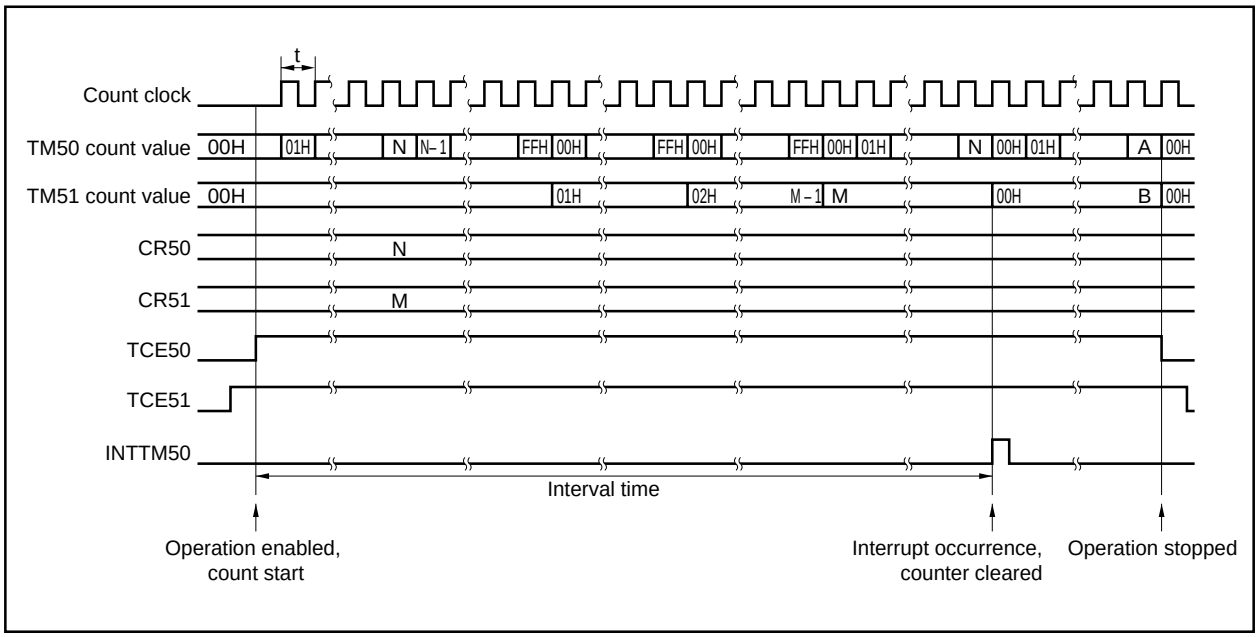
Cautions 1. To write using 8-bit access during cascade connection, set the TCE51 bit to 1 at operation start and then set the TCE50 bit to 1. When operation is stopped, set the TCE50 bit to 0 and then set the TCE51 bit to 0.

2. During cascade connection, TI50 input, TO50 output, and INTTM50 are used. Do not use TI51 input, TO51 output, and INTTM51; mask them instead (for details, refer to CHAPTER 19 INTERRUPT/EXCEPTION PROCESSING FUNCTION). Set bits LVS51, LVR51, TMC511, and TOE51 to 0.

3. Do not change the value of the CR5 register during timer operation.

Figure 8-35 shows a timing example of the cascade connection mode with 16-bit resolution.

Figure 8-7. Cascade Connection Mode with 16-Bit Resolution



8.4.6 Operation as external event counter (16 bits)

The 16-bit resolution timer/event counter mode is selected by setting the TMC514 bit of 8-bit timer mode control register 51 (TMC51) to 1.

The external event counter counts the number of clock pulses input to the TI50 pin from an external source using 16-bit timer counter 5 (TM5).

Setting method

<1> Set each register.

- TCL50 register: Selects the TI50 input edge.
  (The TCL51 register does not have to be set during cascade connection.)
  Falling edge of TI50 → TCL50 = 00H
  Rising edge of TI50 → TCL50 = 01H
- CR50 register: Compare value (N) ... Lower 8 bits (settable from 00H to FFH)
- CR51 register: Compare value (N) ... Higher 8 bits (settable from 00H to FFH)
- TMC50, TMC51 registers: Stops count operation, selects the clear & stop mode entered on a match between the TM5 register and CR5 register, disables timer output F/F inversion, and disables timer output.
  (×: don't care)
  (TMC50 register = 0000xx00B
  TMC51 register = 0001xx00B)
- For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions.**

<2> Set the TCE51 bit of the TMC51 register to 1. Then set the TCE50 bit of the TMC50 register to 1 and count the number of pulses input from TI50.

<3> When the values of the TM5 register and CR5 register connected in cascade match, INTTM50 is generated (the TM5 register is cleared to 0000H).

<4> INTTM50 is then generated each time the values of the TM5 register and CR5 register match.

INTTM50 is generated when the valid edge of TI50 is input N + 1 times: N = 0000H to FFFFH

Cautions 1. During external event counter operation, do not rewrite the value of the CR5n register.

2. To write using 8-bit access during cascade connection, set the TCE51 bit to 1 and then set the TCE50 bit to 1. When operation is stopped, set the TCE50 bit to 0 and then set the TCE51 bit to 0 (n = 0, 1).

3. During cascade connection, TI50 input and INTTM50 are used. Do not use TO51 output, and INTTM51; mask them instead (refer to CHAPTER 19 INTERRUPT/ EXCEPTION PROCESSING FUNCTION). Set bits LVS51, LVR51, TMC511, and TOE51 to 0.

4. Do not change the value of the CR5 register during external counter operation.

8.4.7 Square-wave output operation (16-bit resolution)

The 16-bit resolution timer/event counter mode is selected by setting the TMC514 bit of 8-bit timer mode control register 51 (TMC51) to 1.

8-bit timer/event counter 5n outputs a square wave of any frequency using the interval preset in 16-bit timer compare register 5 (CR5).

Setting method

<1> Set each register.

- TCL50 register: TCL50 selects the count clock (t)
  (The TCL51 register does not have to be set in cascade connection)
- CR50 register: Compare value (N) ... Lower 8 bits (settable from 00H to FFH)
- CR51 register: Compare value (N) ... Higher 8 bits (settable from 00H to FFH)
- TMC50, TCM51 registers: Stops count operation, selects the mode in which clear & start occurs on a match between the TM5 register and CR5 register.

LVS50	LVR50	Timer Output F/F Status Settings
1	0	High-level output
0	1	Low-level output

Enables timer output F/F inversion, and enables timer output.
(TMC50 register = 00001011B or 00000111B
TMC51 register = 00010000B)

- For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions.**

<2> Set the TCE51 bit of the TMC51 register to 1. Then set the TCE50 bit of the TMC50 register to 1 to start the count operation.

<3> When the values of the TM5 register and the CR5 register connected in cascade match, the TO50 timer output F/F is inverted. Moreover, INTTM50 is generated and the TM5 register is cleared to 0000H.

<4> Then, the timer F/F is inverted during the same interval and a square wave is output from the TO50 pin.

Frequency = 1/2t(N + 1): N = 0000H to FFFFH

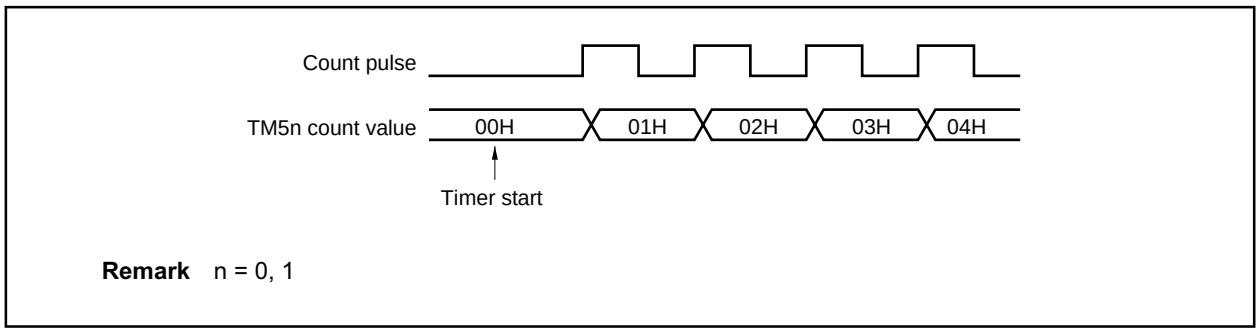
Caution Do not write a different value to the CR5 register.

8.4.8 Cautions

(1) Error on starting timer

An error of up to 1 clock occurs before the match signal is generated after the timer has been started. This is because 8-bit timer counter 5n (TM5n) is started asynchronously to the count pulse.

Figure 8-8. Start Timing of Timer 5n



Remark n = 0, 1

CHAPTER 9 8-BIT TIMERS H0 AND H1

Two 8-bit timer H0 and H1 channels are incorporated in each product.

Product Name	V850ES/KF1	V850ES/KG1	V850ES/KJ1
Number of channels	2 channels (TMH0, TMH1)		

9.1 Functions

8-bit timers H0 and H1 have the following functions.

- Interval timer
- PWM output
- Square ware output
- Carrier generator mode

9.2 Configuration

8-bit timers H0 and H1 consist of the following hardware.

Table 9-1. Configuration of 8-Bit Timers H0 and H1

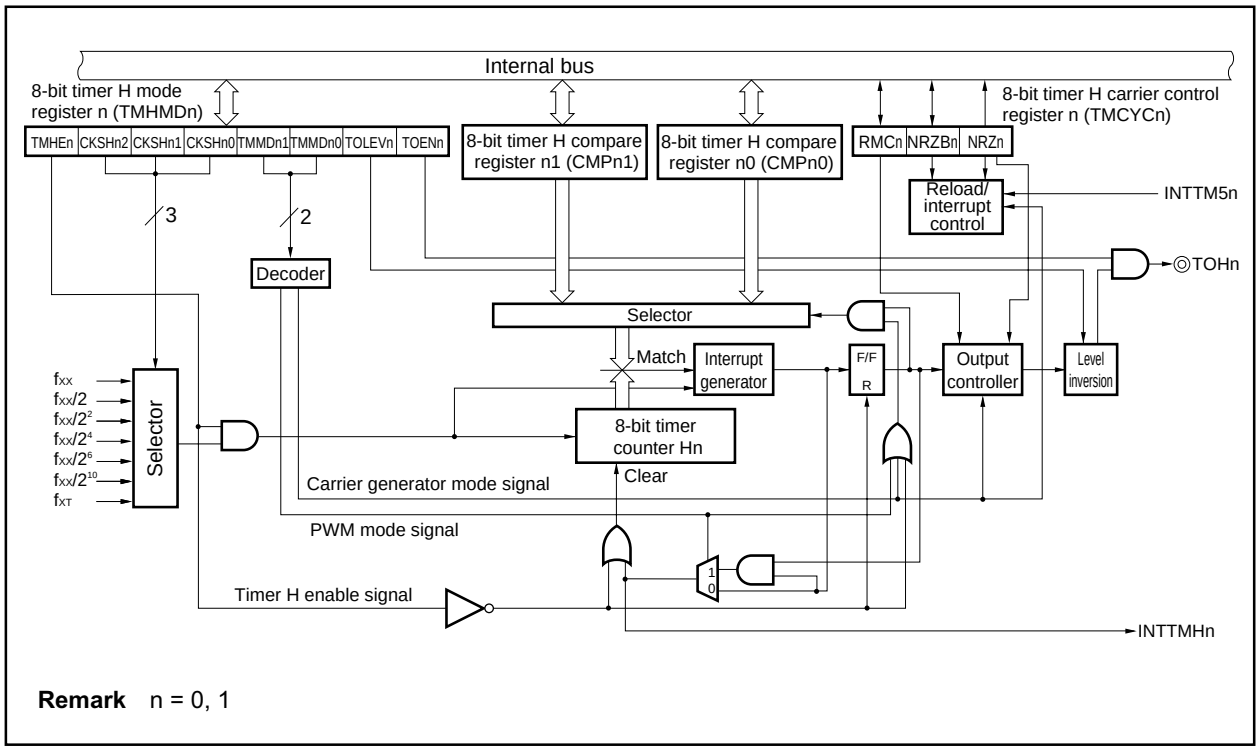
Item	Configuration
Timer registers	8-bit timer counter Hn: 1 each
Register	8-bit timer H compare register n0 (CMPn0): 1 each 8-bit timer H compare register n1 (CMPn1): 1 each
Timer outputs	1 each (TOHn)
Control registers[Note]	8-bit timer H mode register n (TMHMDn) 8-bit timer H carrier control register n (TMCYCn)

Note To use the TOHn pin function, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

Remark n = 0, 1

Figure 9-1 shows the block diagram.

Figure 9-1. Block Diagram of 8-Bit Timers H0 and H1



Remark n = 0, 1

(1) 8-bit timer H compare register n0 (CMPn0)

The CMPn0 register can be read and written by an 8-bit memory manipulation instruction.

After reset, CMPn0 is cleared to 00H.

After reset: 00H R/W Address: FFFFF582H, FFFFF592H

	7	6	5	4	3	2	1	0
CMPn0								

Caution Rewriting the CMPn0 register during timer count operation is prohibited.

Remark n = 0, 1

(2) 8-bit timer H compare register n1 (CMPn1)

The CPMn1 register can be read and written by an 8-bit memory manipulation instruction.

After reset, CMPn1 is cleared to 00H.

After reset: 00H R/W Address: FFFFF583H, FFFFF593H

	7	6	5	4	3	2	1	0
CMPn1								

The CMPn1 register can be rewritten during timer count operation.

In the carrier generator mode, after the CMPn1 register is set, if the count value of 8-bit timer counter Hn and the value of the CMPn1 register match, an interrupt request signal (INTTMHn) is generated. At the same time, the value of 8-bit timer counter Hn is cleared to 00H.

If the value of the CMPn1 register is rewritten during timer operation, the reload timing is when the count value of 8-bit timer counter Hn and the value of the CMPn1 register match. If the transfer timing and write to the CMPn1 register from the CPU conflict, transfer is not performed.

Caution In the PWM output mode and carrier generator mode, be sure to set the CMPn1 register when starting the timer count operation (TMHEn = 1) after the timer count operation was stopped (TMHEn = 0) (be sure to set again even if setting the same value to the CMPn1 register).

9.3 Control Registers

The registers that control 8-bit timers H0 and H1 are as follows.

- 8-bit timer H mode register n (TMHMDn)
- 8-bit timer H carrier control register n (TMCYCn)

Remarks 1. To use the TOHn pin function, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

2. n = 0, 1

(1) 8-bit timer H mode registers 0 and 1 (TMHMD0, TMHMD1)

These registers control the mode of the 8-bit timers H0 and H1.

TMHMD0 and TMHMD1 registers are set by an 8-bit or 1-bit memory manipulation instruction.

After reset, TMHMD0 and TMHMD1 are cleared to 00H.

(a) 8-bit timer H mode register 0 (TMHMD0)

After reset: 00H R/W Address: FFFFF580H

	<7>	6	5	4	3	2	1	<0>
TMHMD0	TMHE0	CKSH02	CKSH01	CKSH00	TMMD01	TMMD00	TOLEV0	TOEN0

TMHE0	8-bit timer H0 operation enable
0	Stop timer count operation (8-bit timer counter H0 = 00H)
1	Enable timer count operation (Counting starts when clock is input)

CKSH02	CKSH01	CKSH00	Selection of count clock			
			Count clock[Note]	20 MHz	f_{XX} = 16.0 MHz	f_{XX} = 10.0 MHz
0	0	0	f_{XX}	Setting prohibited	Setting prohibited	100 ns
0	0	1	$f_{XX}/2$	100 ns	125 ns	200 ns
0	1	0	$f_{XX}/4$	200 ns	250 ns	400 ns
0	1	1	$f_{XX}/16$	800 ns	1 μs	1.6 μs
1	0	0	$f_{XX}/64$	1.6 μs	4 μs	6.4 μs
1	0	1	$f_{XX}/1024$	51.2 μs	64 μs	102.4 μs
Other than above			Setting prohibited			

TMMD01	TMMD00	8-bit timer H0 operation mode
0	0	Interval timer mode
0	1	Carrier generator mode
1	0	PWM output mode
1	1	Setting prohibited

TOLEV0	Timer output level control (default)
0	Low level
1	High level

TOEN0	Timer output control
0	Disable output
1	Enable output

Note Set so as to satisfy the following conditions.

V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz

V_{DD} = 2.7 V to 4.0 V: Count clock ≤ 5 MHz

Cautions 1. When TMHE0 = 1, setting bits other than those of the TMHMD0 register is prohibited.

2. In the PWM output mode and carrier generator mode, be sure to set 8-bit timer H compare register 01 (CMP01) when starting the timer count operation (TMHE0 = 1) after the timer count operation was stopped (TMHE0 = 0) (be sure to set again even if setting the same value to the CMP01 register).

3. When using the carrier generator mode, set the TMH0 count clock frequency to six times the TM50 count clock frequency or higher.

(b) 8-bit timer H mode register 1 (TMHMD1)

After reset: 00H R/W Address: FFFFF590H

	<7>	6	5	4	3	2	1	<0>
TMHMD1	TMHE1	CKSH12	CKSH11	CKSH10	TMMD11	TMMD10	TOLEV1	TOEN1

TMHE1	8-bit timer H1 operation enable
0	Stop timer count operation (8-bit timer counter H1 = 00H)
1	Enable timer count operation (Counting starts when clock is input)

CKSH12	CKSH11	CKSH10	Selection of count clock			
			Count clock[Note]	f_{XX} = 20.0 MHz	f_{XX} = 16.0 MHz	f_{XX} = 10.0 MHz
0	0	0	f_{XX}	Setting prohibited	Setting prohibited	100 ns
0	0	1	$f_{XX}/2$	100 ns	125 ns	200 ns
0	1	0	$f_{XX}/4$	200 ns	250 ns	400 ns
0	1	1	$f_{XX}/16$	800 ns	1 μs	1.6 μs
1	0	0	$f_{XX}/64$	1.6 μs	4 μs	6.4 μs
1	0	1	f_{XT} (subclock)			
Other than above			Setting prohibited			

TMMD11	TMMD10	8-bit timer H1 operation mode
0	0	Interval timer mode
0	1	Carrier generator mode
1	0	PWM output mode
1	1	Setting prohibited

TOLEV1	Timer output level control (default)
0	Low level
1	High level

TOEN1	Timer output control
0	Disable output
1	Enable output

Note Set so as to satisfy the following conditions.
V_{DD} = 4.0 to 5.5 V: Count clock ≤ 10 MHz
V_{DD} = 2.7 V to 4.0 V: Count clock ≤ 5 MHz

Cautions 1. When TMHE1 = 1, setting bits other than those of the TMHMD1 register is prohibited.

2. In the PWM output mode and carrier generator mode, be sure to set 8-bit timer H compare register 11 (CMP11) when starting timer count operation (TMHE1 = 1) after the timer count operation was stopped (TMHE1 = 0) (be sure to set again even if setting the same value to the CMP11 register).

3. When using the carrier generator mode, set the TMH1 count clock frequency to six times the TM51 count clock frequency or higher.

(2) 8-bit timer H carrier control register n (TMCYCn)

This register controls the 8-bit timer Hn remote control output and carrier pulse output status.

TMCYCn register is set by an 8- bit or 1-bit memory manipulation instruction.

The NRZn bit is a read-only bit.

After reset, TMCYCn is cleared to 00H.

Remark n = 0, 1

After reset: 00H R/W Address: FFFFF581H, FFFFF591H

	7	6	5	4	3	2	1	0
TMCYCn	0	0	0	0	0	RMCn	NRZBn	NRZn

(n = 0, 1)

RMCn	NRZBn	Remote control output
0	0	Low level output
0	1	High level output
1	0	Low level output
1	1	Carrier pulse output

NRZn	Carrier pulse output status flag
0	Carrier output disabled status (low level status)
1	Carrier output enable status

9.4 Operation

9.4.1 Operation as interval timer/square wave output

When the count value of 8-bit timer counter Hn and the value of 8-bit timer H compare register n0 (CMPn0) match, an interrupt request signal (INTTMHn) is generated and 8-bit timer counter Hn is cleared to 00H.

8-bit timer H compare register n1 (CMPn1) cannot be used in the interval timer mode. Even if the CMPn1 register is set, this has no effect on the timer output because matches between 8-bit timer counter Hn and the CMPn1 register are not detected.

A square wave of the desired frequency (duty = 50%) is output from the TOHn pin, by setting the TOENn bit of 8-bit timer H mode register n (TMHMDn) to 1.

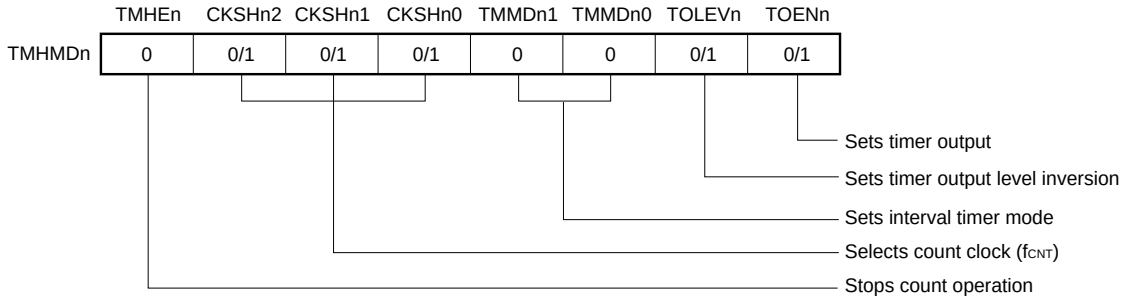
(1) Usage method

The INTTMHn signal is repeatedly generated in the same interval.

<1> Set each register.

Figure 9-2. Register Settings in Interval Timer Mode

(i) 8-bit timer H mode register n (TMHMDn) settings



(ii) CMPn0 register settings

- Compare value (N)

<2> When TMHEn = 1 is set, counting starts.

<3> When the count value of 8-bit timer counter Hn and the value of the CMPn0 register match, the INTTMHn signal is generated and 8-bit timer counter Hn is cleared to 00H.

Interval time = (N + 1)/f_{CNT}

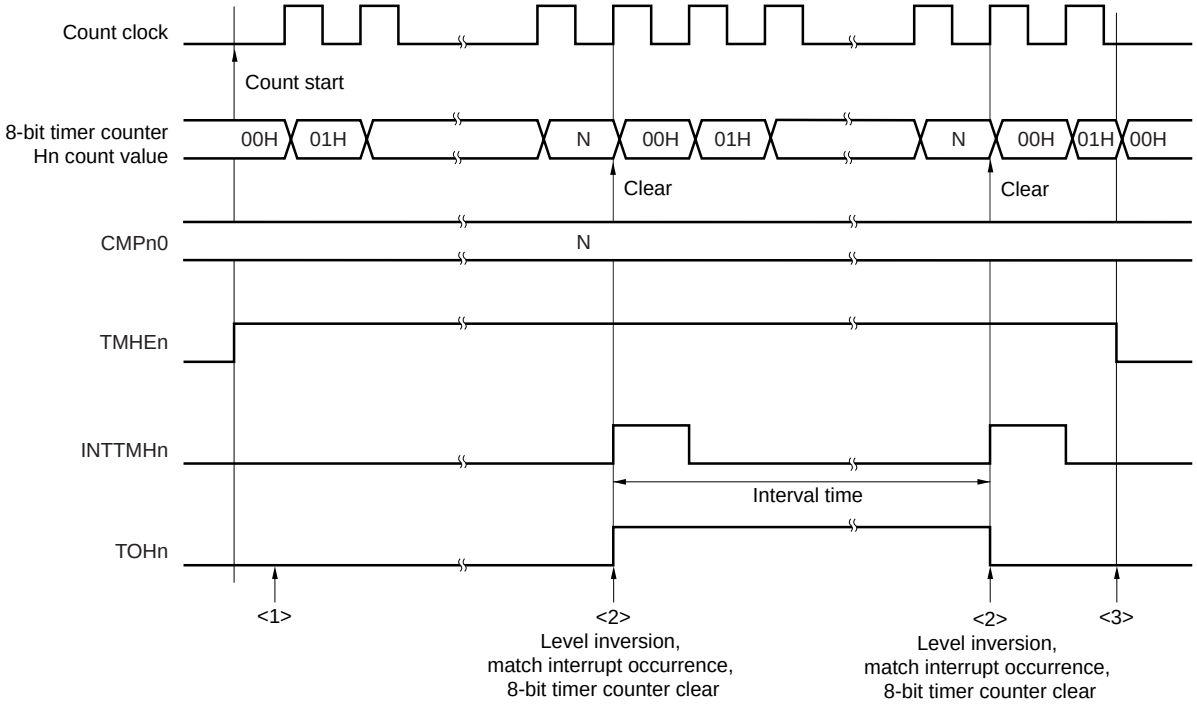
<4> Then, the INTTMHn signal is generated in the same interval. To stop the count operation, set the TMHEn bit to 0.

(2) Timing chart

The timing in the interval timer mode is as follows.

Figure 9-3. Timing of Interval Timer/Square Wave Output Operation (1/2)

Basic operation



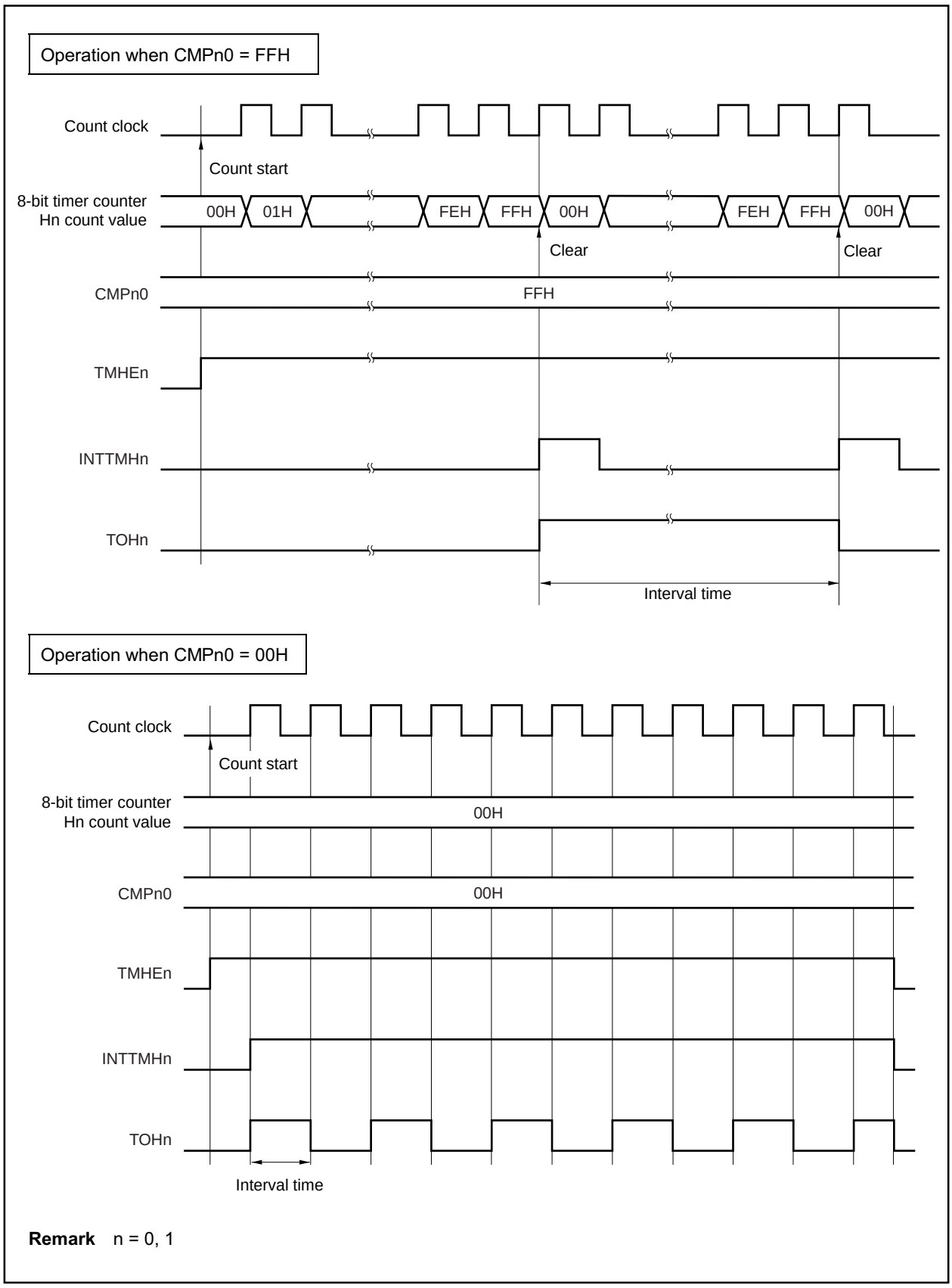
<1> When the TMHEn bit is changed from 0 to 1, the count operation is enabled. The count clock starts counting no more than one clock after operation has been enabled.

<2> When the count value of 8-bit timer counter Hn and the value of the CMPn0 register match, the value of 8-bit timer counter Hn is cleared, the TOHn output level is inverted, and the INTTMHn signal is output.

<3> The INTTMHn signal and TOHn output become inactive when the TMHEn bit is set to 0 during 8-bit timer Hn operation. If the level is already inactive, it remains unchanged.

Remark n = 0, 1

Figure 9-3. Timing of Interval Timer/Square Wave Output Operation (2/2)



Remark n = 0, 1

9.4.2 PWM output mode operation

In the PWM output mode, a pulse of any duty and cycle can be output.

8-bit timer H compare register n0 (CMPn0) controls the timer output (TOHn) cycle. Rewriting the CMPn0 register during timer operation is prohibited.

8-bit timer H compare register n1 (CMPn1) controls the timer output (TOHn) duty. The CMPn1 register can be rewritten during timer operation.

The operation in the PWM output mode is as follows.

After timer counting starts, when the count value of 8-bit timer counter Hn and the value of the CMPn0 register match, the TOHn output becomes active and 8-bit timer counter Hn is cleared to 00H. When the count value of 8-bit timer counter Hn and the CMPn1 register match, TOHn output becomes inactive.

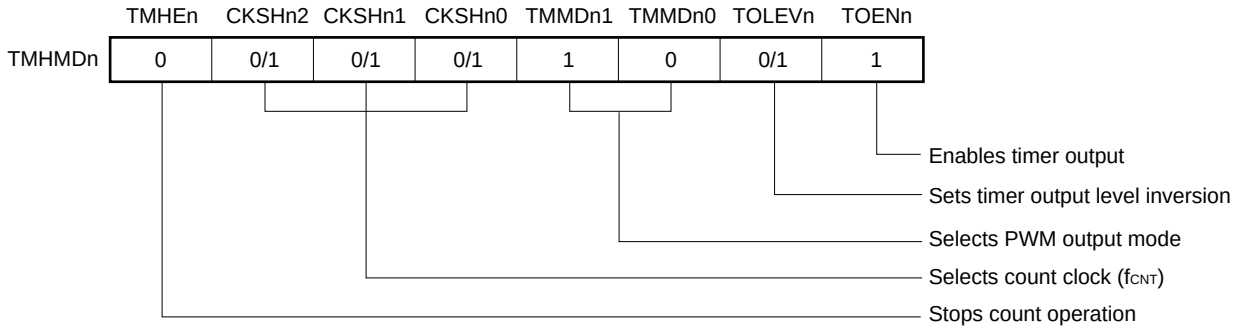
(1) Usage method

In the PWM output mode, a pulse of any duty and cycle can be output.

<1> Set each register.

Figure 9-4. Register Settings in PWM Output Mode

(i) 8-bit timer H mode register n (TMHMDn) settings



(ii) CMPn0 register setting

- Compare value (N): Sets cycle

(ii) CMPn1 register setting

- Compare value (N): Sets duty

Remarks 1. n = 0, 1

2. 00H ≤ CMPn1 (M) < CMPn0 (N) ≤ FFH

<2> When TMHEn = 1 is set, counting starts.

<3> After the count operation is enabled, the first compare register to be compared is the CMPn0 register. When the count value of 8-bit timer counter Hn and the value of the CMPn0 register match, 8-bit timer counter Hn is cleared, an interrupt request signal (INTTMHn) is generated, and the TOHn output becomes active. At the same time, the register that is compared with 8-bit timer counter Hn changes from the CMPn0 register to the CMPn1 register.

<4> When the count value of 8-bit timer counter Hn and the value of the CMPn1 register match, the TOHn output becomes inactive, and at the same time the register that is compared with 8-bit timer counter Hn changes from the CMPn1 register to the CMPn0 register. At this time, 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

<5> A pulse of any duty can be obtained through the repetition of steps <3> and <4> above.

<6> To stop the count operation, set TMHEn = 0.

Designating the setting value of the CMPn0 register as (N), the setting value of the CMPn1 register as (M), and the count clock frequency as f_{CNT}, the PWM pulse output cycle and duty are as follows.

PWM pulse output cycle = $(N + 1)/f_{CNT}$
Duty = inactive width: Active width = (M + 1) : (N + 1)

Cautions 1. In the PWM output mode, three operating clocks (signal selected by CKSHn0 to CKSHn2 bits of TMHMDn register) are required for actual transfer of the new value to the register after the CMPn1 register has been rewritten.

2. Be sure to set the CMPn1 register when starting the timer count operation (TMHEn = 1) after the timer count operation was stopped (TMHEn = 0) (be sure to set again even if setting the same value to the CMPn1 register).

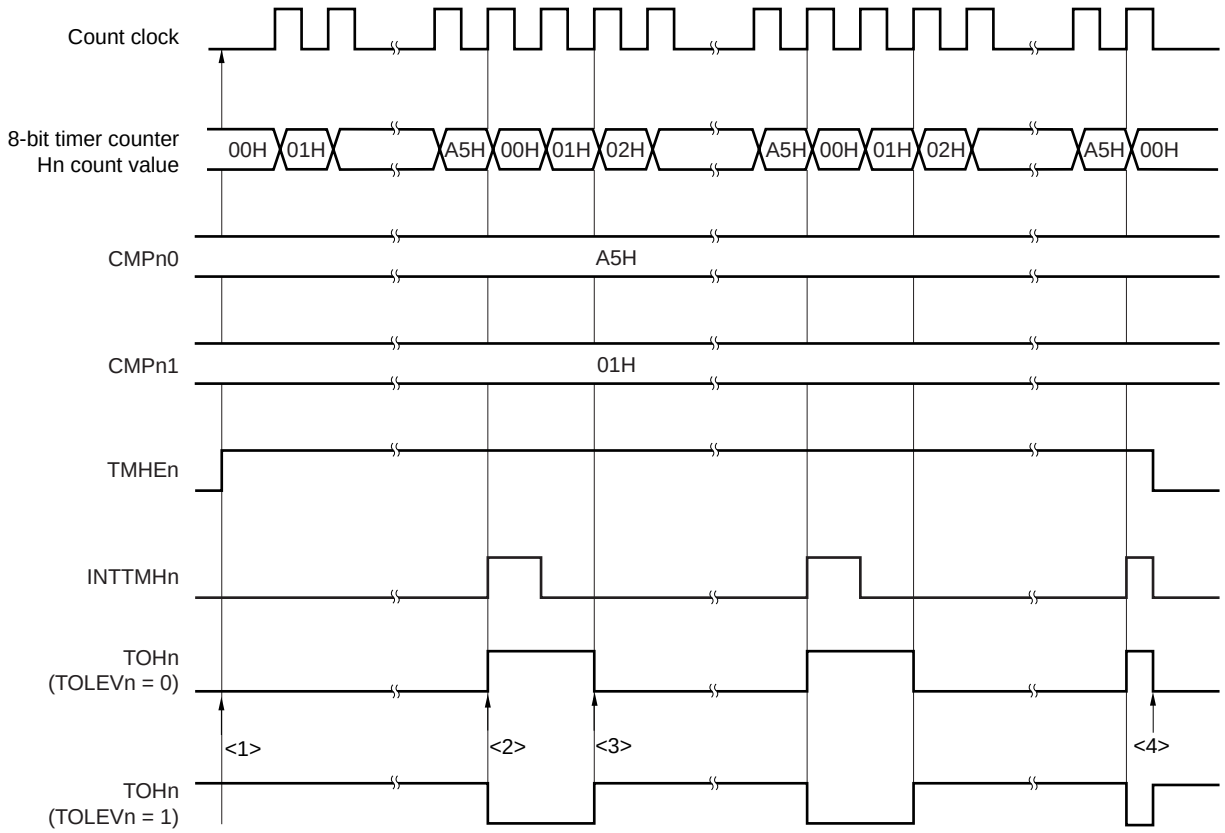
(2) Timing chart

The operation timing in the PWM output mode is as follows.

Caution The setting value (M) of the CMPn1 register and the setting value (N) of the CMPn0 register must always be set within the following range.
00H ≤ CMPn1 (M) < CMPn0 (N) ≤ FFH

Figure 9-5. Operation Timing in PWM Output Mode (1/4)

Basic operation



<1> When TMHEn = 1 is set, counting starts. At this time TOHn output stays inactive (TOLEVn = 0).

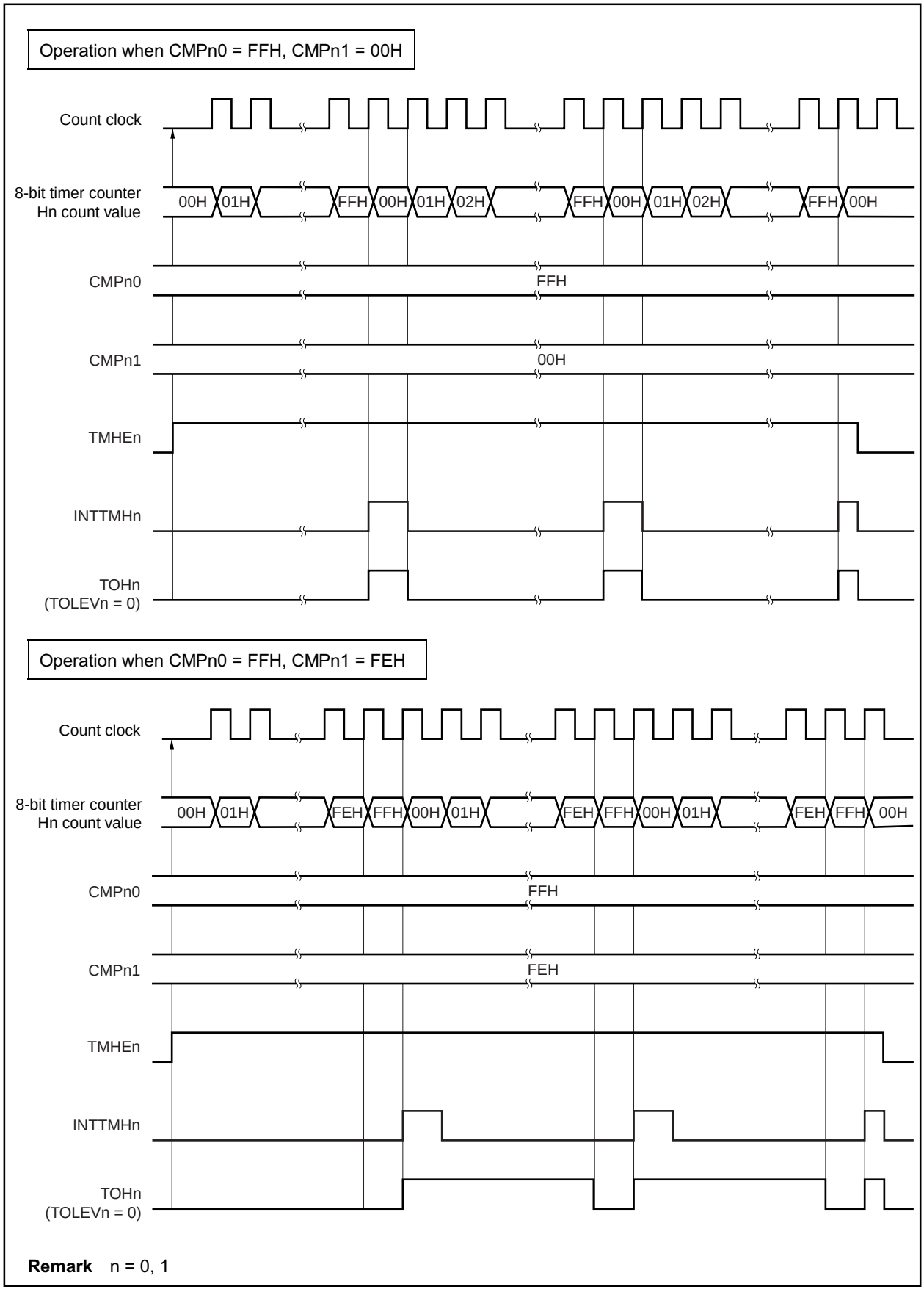
<2> When the count value of 8-bit timer counter Hn and the value of the CMPn0 register match, the TOHn output level is inverted, 8-bit timer counter Hn is cleared, and the INTTMHn signal is output.

<3> When the count value of 8-bit timer counter Hn and the value of the CMPn1 register match, the TOHn output level is inverted. At this time, the value of 8-bit timer counter Hn is not cleared and the INTTMHn signal is not output.

<4> When the TMHEn bit is set to 0 during 8-bit timer Hn operation, the INTTMHn signal and TOHn output becomes inactive.

Remark n = 0, 1

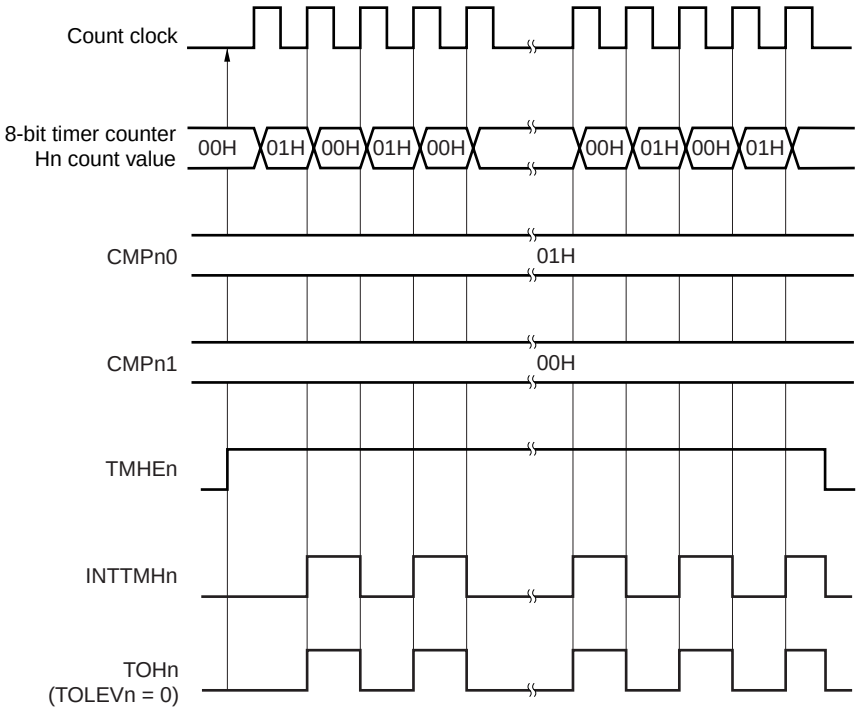
Figure 9-5. Operation Timing in PWM Output Mode (2/4)



Remark n = 0, 1

Figure 9-5. Operation Timing in PWM Output Mode (3/4)

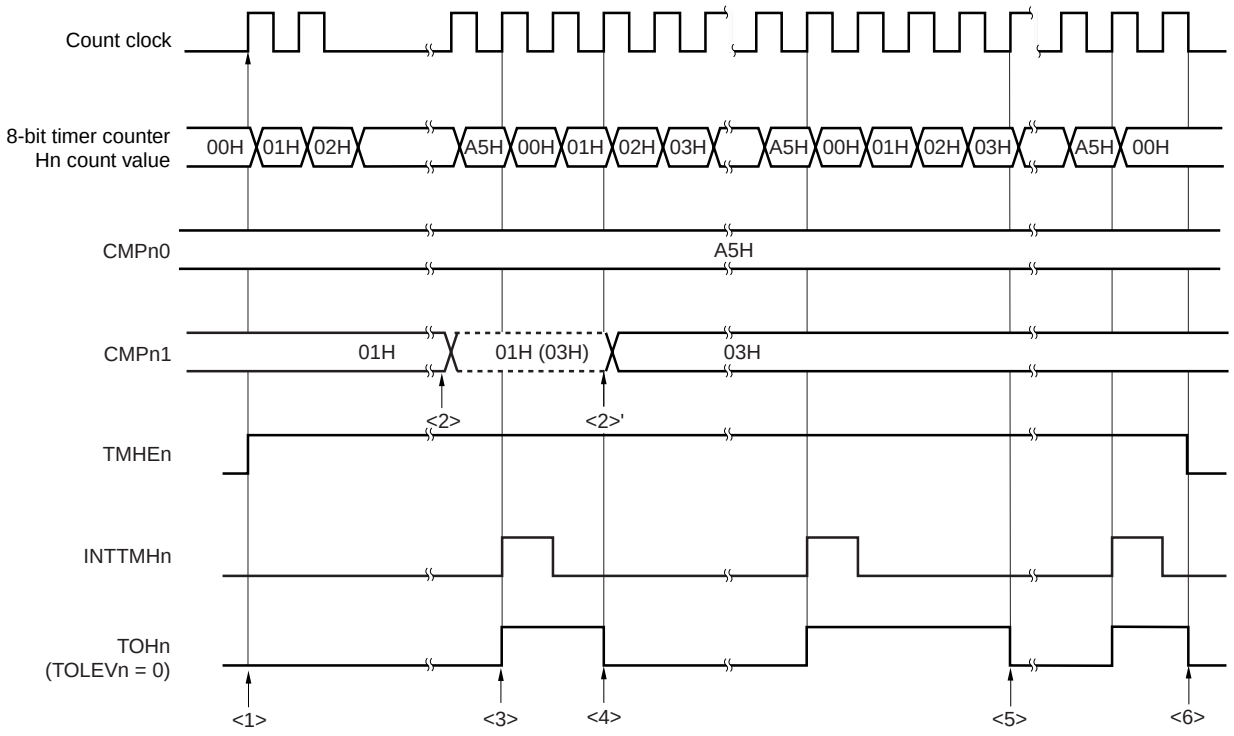
Operation when CMPn0 = 01H, CMPn1 = 00H



Remark n = 0, 1

Figure 9-5. Operation Timing in PWM Output Mode (4/4)

Operation based on CMPn1 transitions (CMPn1 = 01H → 03H, CMPn0 = A5H)



<1> When TMHEn = 1 is set, counting starts. At this time, the TOHn output remains inactive (TOLEVn = 0).

<2> The setting value of the CMPn1 register can be changed during count operation. This operation is asynchronous to the count clock.

<3> When the count value of 8-bit timer counter Hn and the value of the CMPn0 register match, 8-bit timer counter Hn is cleared, the TOHn output becomes active, and the INTTMHn signal is generated.

<4> Even if the value of the CMPn1 register is changed, that value is latched and not transferred to the register. When the count value of 8-bit timer counter Hn and the value of the CMPn1 register prior to the change match, the changed value is transferred to the CMPn1 register and the value of the CMPn1 register is changed (<2>').

However, three or more count clocks are required from the time the value of the CMPn1 register is changed until it is transferred to the register. Even if a match signal is generated within three count clocks, the changed value cannot be transferred to the register.

<5> When the count value of 8-bit timer counter Hn matches the changed value of the CMPn1 register, the TOHn output becomes inactive. 8-bit timer counter Hn is not cleared and the INTTMHn signal is not generated.

<6> When the TMHEn bit is set to 0 during 8-bit timer Hn operation, the INTTMHn signal and TOHn output become inactive.

9.4.3 Carrier generator mode operation

The carrier clock generated by 8-bit timer Hn is output using the cycle set with 8-bit timer/event counter 5n.

In the carrier generator mode, 8-bit timer/event counter 5n is used to control the extent to which the carrier pulse of 8-bit timer Hn is output, and the carrier pulse is output from the TOHn output.

(1) Carrier generation

In the carrier generator mode, 8-bit timer H compare register n0 (CMPn0) generates a waveform with the low-level width of the carrier pulse and 8-bit timer H compare register n1 (CMPn1) generates a waveform with the high-level width of the carrier pulse.

During 8-bit timer Hn operation, the CMPn1 register can be rewritten, but rewriting of the CMPn0 register is prohibited.

(2) Carrier output control

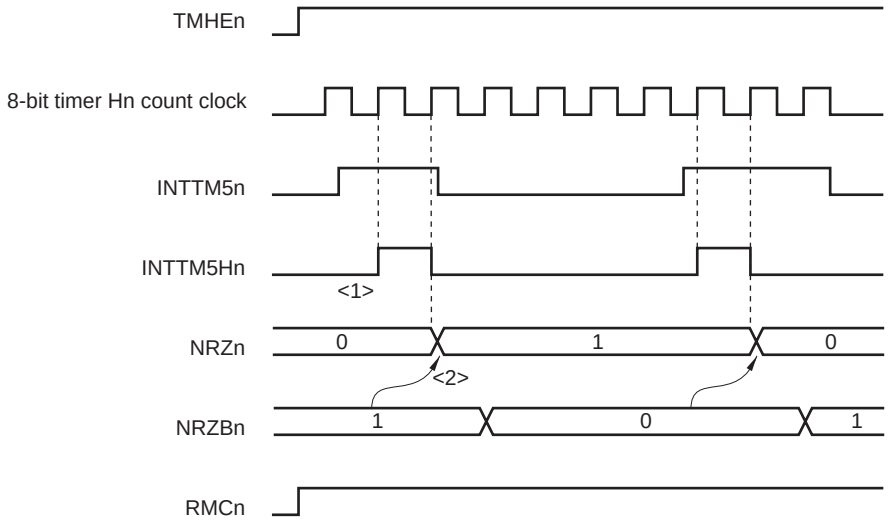
Carrier output control is performed with the interrupt request signal (INTTM5n) of 8-bit timer/event counter 5n and the NRZBn and RMCn bits of 8-bit timer H carrier control register (TMCYCn). The output relationships are as follows.

RMCn Bit	NRZBn Bit	Output
0	0	Low level output
0	1	High level output
1	0	Low level output
1	1	Carrier pulse output

Remark n = 0, 1

To control carrier pulse output during count operation, the NRZn and NRZBn bits of the TMCYCn register have a master and slave bit configuration. The NRZn bit is read-only while the NRZBn bit can be read and written. The INTTM5n signal is synchronized with the 8-bit timer Hn clock and output as the INTTM5Hn signal. The INTTM5Hn signal becomes the data transfer signal of the NRZn bit and the value of the NRZBn bit is transferred to the NRZn bit. The transfer timing from the NRZBn bit to the NRZn bit is as follows.

Figure 9-6. Transfer Timing



<1> The INTTM5n signal is synchronized with the count clock of 8-bit timer Hn and is output as the INTTM5Hn signal.

<2> The value of the NRZBn bit is transferred to the NRZn bit at the second clock from the rising edge of the INTTM5Hn signal.

Cautions 1. Do not rewrite the NRZBn bit again until at least the second clock after it has been rewritten, or else transfer from the NRZBn bit to the NRZn bit is not guaranteed.

2. When using 8-bit timer/event counter 5n in the carrier generator mode, an interrupt occurs at the timing of <1>. An interrupt occurs at a different timing when it is used in other than the carrier generator mode.

Remark n = 0, 1

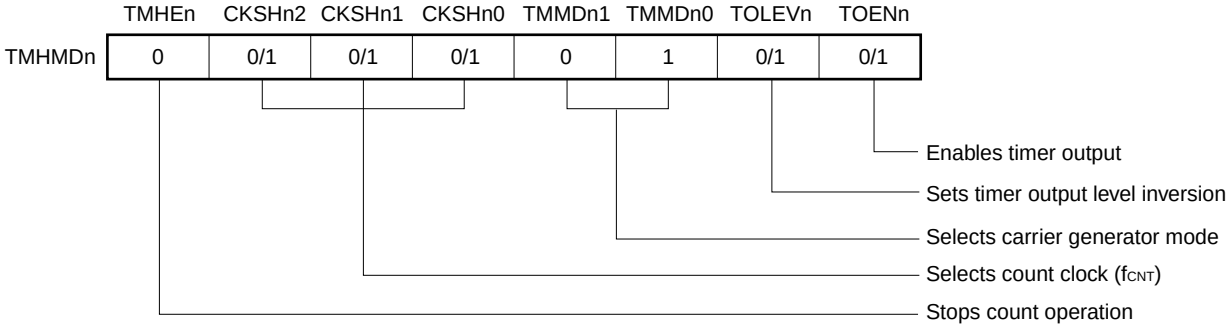
(3) Usage method

Any carrier clock can be output from the TOHn pin.

<1> Set each register.

Figure 9-7. Register Settings in Carrier Generator Mode

- 8-bit timer H mode register n (TMHMDn)



- CMPn0 register: Compare value
- CMPn1 register: Compare value
- TMCYCn register: RMCn = 1 ... Remote control output enable bit
  NRZBn = 0/1 ... Carrier output enable bit
- TCL5n, TMC5n registers: Refer to **8.3 Control Registers**.

Remark n = 0, 1

<2> When TMHEn = 1 is set, 8-bit timer Hn count operation starts.

<3> When the TCE5n bit of 8-bit timer mode control register 5n (TMC5n) is set to 1, 8-bit timer/event counter 5n count operation starts.

<4> After the count operation is enabled, the first compare register to be compared is the CMPn0 register. When the count value of 8-bit timer counter Hn and the value of the CMPn0 register match, the INTTMHn signal is generated, 8-bit timer counter Hn is cleared, and at the same time, the register that is compared with 8-bit timer counter Hn changes from the CMPn0 register to the CMPn1 register.

<5> When the count value of 8-bit timer counter Hn and the value of the CMPn1 register match, the INTTMHn signal is generated, 8-bit timer counter Hn is cleared, and at the same time, the register that is compared with 8-bit timer counter Hn changes from the CMPn1 register to the CMPn0 register.

<6> The carrier clock is obtained through the repetition of steps <4> and <5> above.

<7> The INTTM5n signal is synchronized with 8-bit timer Hn and output as the INTTM5Hn signal. This signal becomes the data transfer signal of the NRZBn bit and the value of the NRZBn bit is transferred to the NRZn bit.

<8> When the NRZn bit becomes high level, the carrier clock is output from the TOHn pin.

<9> Any carrier clock can be obtained through the repetition of the above steps. To stop the count operation, set TMHEn = 0.

Designating the setting value of the CMPn0 register as (N), the setting value of the CMPn1 register as (M), and the count clock frequency as f_{CNT}, the carrier clock output cycle and duty are as follows.

Carrier clock output cycle = (N + M + 2)/f_{CNT} Duty = High level width: Carrier clock output width = (M + 1) : (N + M + 2)

Caution Be sure to set the CMPn1 register when starting the timer count operation (TMHEn = 1) after the timer count operation was stopped (TMHEn = 0) (be sure to set again even if setting the same value to the CMPn1 register).

(4) Timing chart

The carrier output control timing is as follows.

Cautions 1. Set the values of the CMPn0 and CMPn1 registers in the range of 01H to FFH.

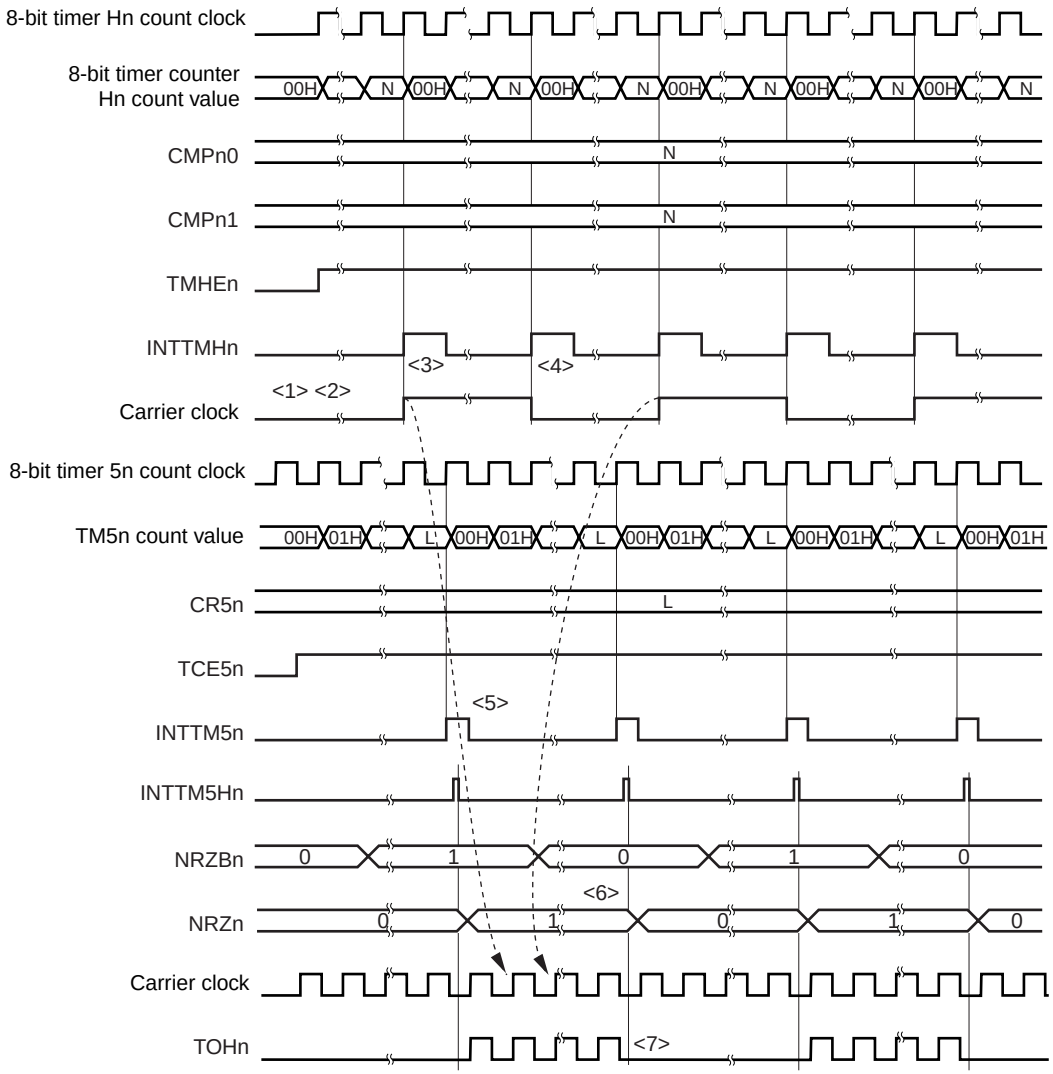
2. In the carrier generator mode, three operating clocks (signal selected by CKSHn0 to CKSHn2 bits of TMHMDn register) are required for actual transfer of the new value to the register after the CMPn1 register has been rewritten.

3. Be sure to perform the RMCn bit setting before the start of the count operation.

4. When using the carrier generator mode, set the TMHn count clock frequency to six times the TM5n count clock frequency or higher.

★ **Figure 9-8. Carrier Generator Mode (1/3)**

Operation when CMPn0 = N, CMPn1 = N is set



<1> When TMHEn = 0 and TCE5n = 0, the operation of 8-bit timer counter Hn is stopped.

<2> When TMHEn = 1 is set, 8-bit timer counter Hn starts counting. The carrier clock is maintained inactive at this time.

<3> When the count value of 8-bit timer counter Hn and the value of the CMPn0 register match, the first INTTMHn signal is generated, the carrier clock signal is inverted, and the register that is compared with 8-bit timer counter Hn changes from the CMPn0 register to the CMPn1 register. 8-bit timer counter Hn is cleared to 00H.

<4> When the count value of 8-bit timer counter Hn and the value of the CMPn1 register match, the INTTMHn signal is generated, the carrier clock signal is inverted, and the register that is compared with 8-bit timer counter Hn changes from the CMPn1 register to the CMPn0 register. 8-bit timer counter Hn is cleared to 00H. A carrier clock with a duty of 50% is generated through the repetition of steps <3> and <4>.

<5> The INTTM5n signal is synchronized with 8-bit timer Hn and output as the INTTM5Hn signal.

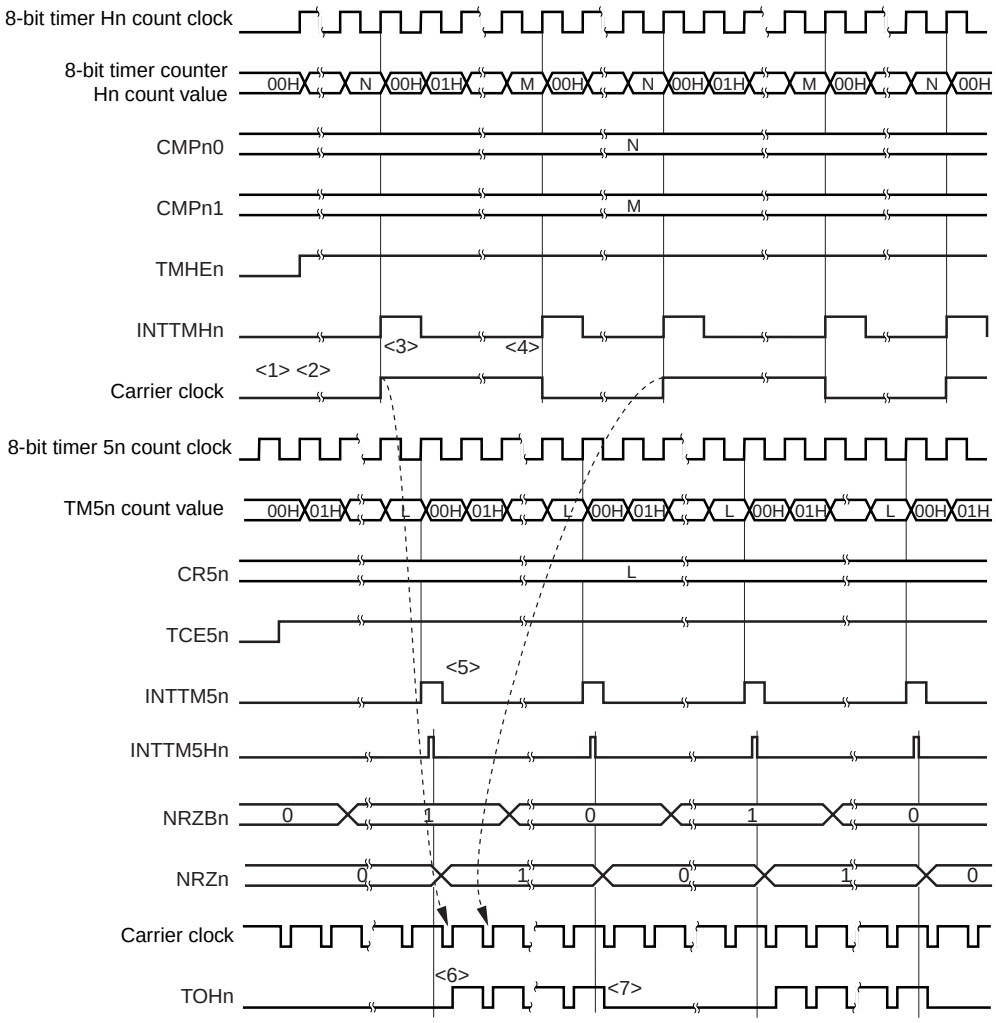
<6> The INTTM5n signal becomes the data transfer signal of the NRZBn bit, and the value of the NRZBn bit is transferred to the NRZn bit.

<7> The TOHn output is made low level by setting NRZn = 0.

Remark n = 0, 1

★ **Figure 9-8. Carrier Generator Mode (2/3)**

Operation when CMPn0 = N, CMPn1 = M is set



<1> When TMHEn = 0 and TCE5n = 0, the operation of 8-bit timer counter Hn is stopped.

<2> When TMHEn = 1 is set, 8-bit timer counter Hn starts counting. The carrier clock is maintained inactive at this time.

<3> When the count value of 8-bit timer counter Hn and the value of the CMPn0 register match, the first INTTMHn signal is generated, the carrier clock signal is inverted, and the register that is compared with 8-bit timer counter Hn changes from the CMPn0 register to the CMPn1 register. 8-bit timer counter Hn is cleared to 00H.

<4> When the count value of 8-bit timer counter Hn and the value of the CMPn1 register match, the INTTMHn signal is generated, the carrier clock signal is inverted, and the register that is compared with 8-bit timer counter Hn changes from the CMPn1 register to the CMPn0 register. 8-bit timer counter Hn is cleared to 00H. A carrier clock with a fixed duty (other than 50%) is generated through the repetition of steps <3> and <4>.

<5> The INTTM5n signal is generated. This signal is synchronized with 8-bit timer Hn and output as the INTTM5Hn signal.

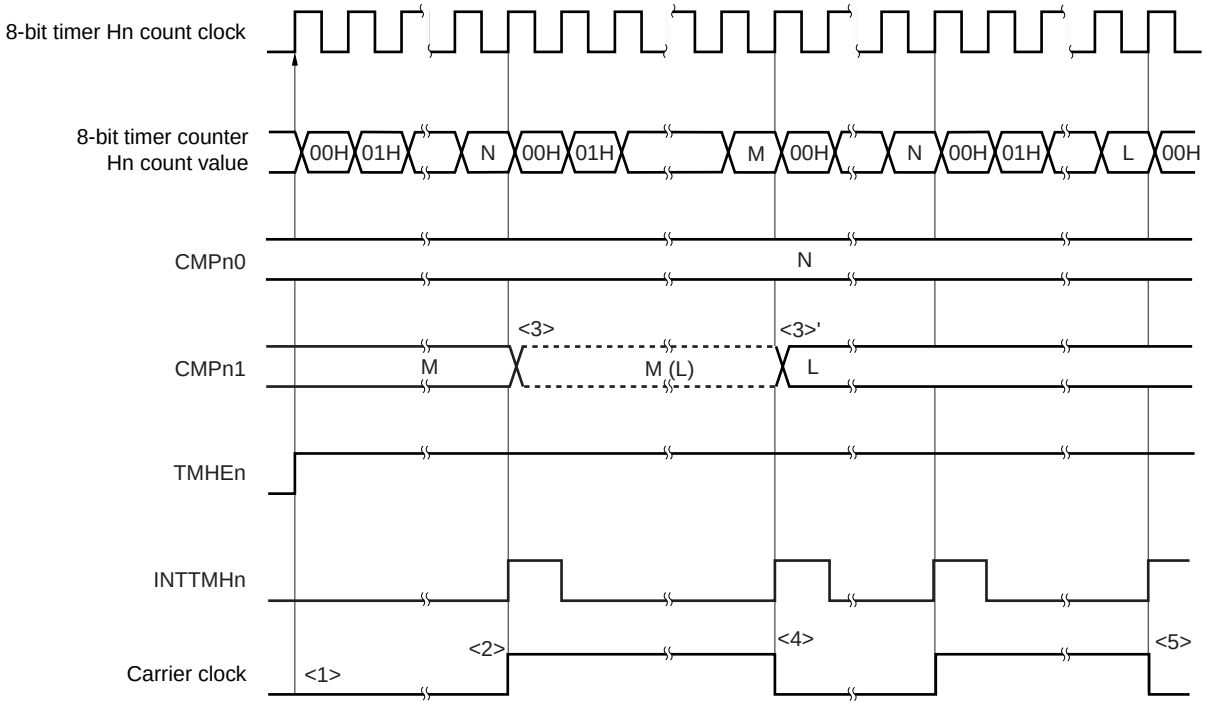
<6> The carrier is output from the rising edge of the first carrier clock by setting NRZn = 1.

<7> By setting NRZn = 0, the TOHn output is also maintained high level while the carrier clock is high level, and does not change to low level (the high level width of the carrier waveform is guaranteed through steps <6> and <7>).

Remark n = 0, 1

Figure 9-8. Carrier Generator Mode (3/3)

Operation based on CMPn1 transitions



<1> When TMHEn = 1 is set, counting starts. The carrier clock is maintained inactive at this time.

<2> When the count value of 8-bit timer counter Hn and the value of the CMPn0 register match, 8-bit timer counter Hn is cleared and the INTTMHn signal is output.

<3> The CMPn1 register can be rewritten during 8-bit timer Hn operation, but the changed value (L) is latched. The value of the CMPn1 register is changed when the count value of 8-bit timer counter Hn and the value of the CMPn1 register prior to the change (M) match (<3>').

<4> When the count value of 8-bit timer counter Hn and the value (M) of the CMPn1 register match, the INTTMHn signal is output, the carrier signal is inverted, and 8-bit timer counter Hn is cleared to 00H.

<5> The timing at which the count value of 8-bit timer counter Hn and the value of the CMPn1 register match again is the changed value (L).

Remark n = 0, 1

CHAPTER 10 INTERVAL TIMER, WATCH TIMER

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 include interval timer BRG and a watch timer. Interval timer BRG can also be used as the source clock of the watch timer. The watch timer can also be used as interval timer WT.

Two interval timer channels and one watch timer channel can be used at the same time.

10.1 Interval Timer BRG

10.1.1 Functions

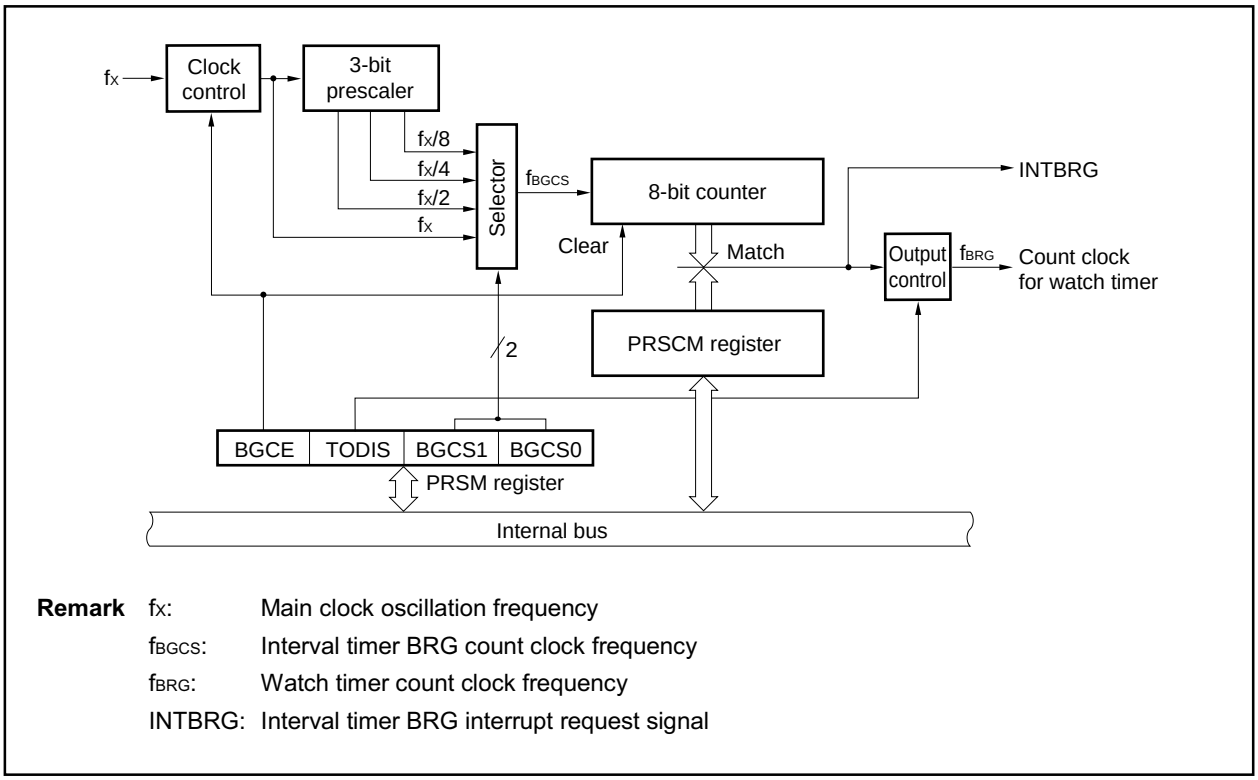
Interval timer BRG has the following functions.

- Interval timer BRG: An interrupt request signal (INTBRG) is generated at a specified interval.
- Generation of count clock for watch timer: When the main clock is used as the count clock for the watch timer, a count clock (f_{BRG}) is generated.

10.1.2 Configuration

The following shows the block diagram of interval timer BRG.

Figure 10-1. Block Diagram of Interval Timer BRG



Remark f_X: Main clock oscillation frequency
f_{BGCS}: Interval timer BRG count clock frequency
f_{BRG}: Watch timer count clock frequency
INTBRG: Interval timer BRG interrupt request signal

(1) Clock control

The clock control controls supply/stop of the operation clock of interval timer BRG.

(2) 3-bit prescaler

The 3-bit prescaler divides f_X to generate $f_X/2$, $f_X/4$, and $f_X/8$.

(3) Selector

The selector selects the count clock (f_{BGCS}) for interval timer BRG from f_X, $f_X/2$, $f_X/4$, and $f_X/8$.

(4) 8-bit counter

The 8-bit counter counts the count clock (f_{BGCS}).

(5) Output control

The output control controls supply of the count clock (f_{BRG}) for the watch timer.

(6) PRSCM register

The PRSCM register is an 8-bit compare register that sets the interval time.

(7) PRSM register

The PRSM register controls the operation of interval timer BRG, the selector, and clock supply to the watch timer.

10.1.3 Registers

Interval timer BRG includes the following registers.

(1) Interval timer BRG mode register (PRSM)

PRSM controls the operation of interval timer BRG, selection of count clock, and clock supply to the watch timer.

This register can be read/written in 8-bit or 1-bit units.

After reset, PRSM is cleared to 00H.

After reset: 00H R/W Address: FFFFF8B0H

	7	6	5	<4>	3	2	1	0
PRSM	0	0	0	BGCE	0	TODIS	BGCS1	BGCS0

BGCE	Control of interval timer operation
0	Operation stopped, 8-bit counter cleared to 01H
1	Operate

TODIS	Control of clock supply for watch timer
0	Clock for watch timer not supplied
1	Clock for watch timer supplied

BGCS1	BGCS0	Selection of input clock (f_{BGCS})[Note]			
			10 MHz	5 MHz	4 MHz
0	0	f_X	100 ns	200 ns	250 ns
0	1	$f_X/2$	200 ns	400 ns	500 ns
1	0	$f_X/4$	400 ns	800 ns	1 μs
1	1	$f_X/8$	800 ns	1.6 μs	2 μs

Note Set these bits so that the following conditions are satisfied.

V_{DD} = 4.0 to 5.5 V: $f_{BGCS} \leq$ 10 MHz

V_{DD} = 2.7 to 4.0 V: $f_{BGCS} \leq$ 5 MHz

Cautions 1. Do not change the values of the TODIS, BGCS1, and BGCS0 bits while interval timer BRG is operating (BGCE bit = 1). Set the TODIS, BGCS1, and BGCS0 bits before setting (1) the BGCE bit.

2. When the BGCE bit is cleared (to 0), the 8-bit counter is cleared.

(2) Interval timer BRG compare register (PRSCM)

PRSCM is an 8-bit compare register.

This register can be read/written in 8-bit units.

After reset, PRSCM is cleared to 00H.

After reset: 00H R/W Address: FFFFF8B1H

	7	6	5	4	3	2	1	0
PRSCM	PRSCM7	PRSCM6	PRSCM5	PRSCM4	PRSCM3	PRSCM2	PRSCM1	PRSCM0

Caution Do not rewrite the PRSCM register while interval timer BRG is operating (PRSM.BGCE bit = 1). Set the PRSCM register before setting (1) the BGCE bit.

10.1.4 Operation

(1) Operation of interval timer BRG

Set the count clock by using the BGCS1 and BGCS0 bits of PRSM and the 8-bit compare value by using the PRSCM register.

When the PRSM.BGCE bit is set (1), interval timer BRG starts operating.

Each time the count value of the 8-bit counter and the set value in the PRSCM register match, an interrupt request signal (INTBRG) is generated. At the same time, the 8-bit counter is cleared to 00H and counting is continued.

The interval time can be obtained from the following equation.

Interval time = $2^m \times N/f_X$

Remark m: Division value (set values of BGCS1 and BGCS0 bits) = 0 to 3
N: Set value in PRSCM register = 1 to 256 (when the set value in the PRSCM register is 00H, N = 256)
f_X: Main clock oscillation frequency

(2) Count clock supply for watch timer

Set the count clock by using the BGCS1 and BGCS0 bits of PRSM and the 8-bit compare value by using the PRSCM register, so that the count clock frequency (f_{BRG}) of the watch timer is 32.768 kHz. Set (1) the PRSM.TODIS bit at the same time.

When the PRSM.BGCE bit is set (1), f_{BRG} is supplied to the watch timer.

f_{BRG} is obtained from the following equation.

$f_{BRG} = f_X/(2^{m+1} \times N)$

To set f_{BRG} to 32.768 kHz, perform the following calculation to set the BGCS1 and BGCS0 bits and the PRSCM register.

<1> Set N = f_X/65,536 (round off the decimal) to set m = 0.
<2> If N is even, N = N/2 and m = m + 1
<3> Repeat step <2> until N is even or m = 3
<4> Set N to the PRSCM register and m to the BGCS1 and BGCS0 bits.

Example: When f_X = 4.00 MHz

N = 4,000,000/65,536 = 61 (round off the decimal), m = 0
<2>, <3> Since N is odd, the values remain as N = 61, m = 0
<4> The set value in the PRSCM register: 3DH (61), the set values in the BGCS1 and BGCS0 bits: 00

Remark m: Divided value (set value in the BGCS1 and BGCS0 bits) = 0 to 3
N: Set value in PRSCM register = 1 to 256 (when the set value in the PRSCM register is 00H, N = 256)
f_X: Main clock oscillation frequency

10.2 Watch Timer

10.2.1 Functions

The watch timer has the following functions.

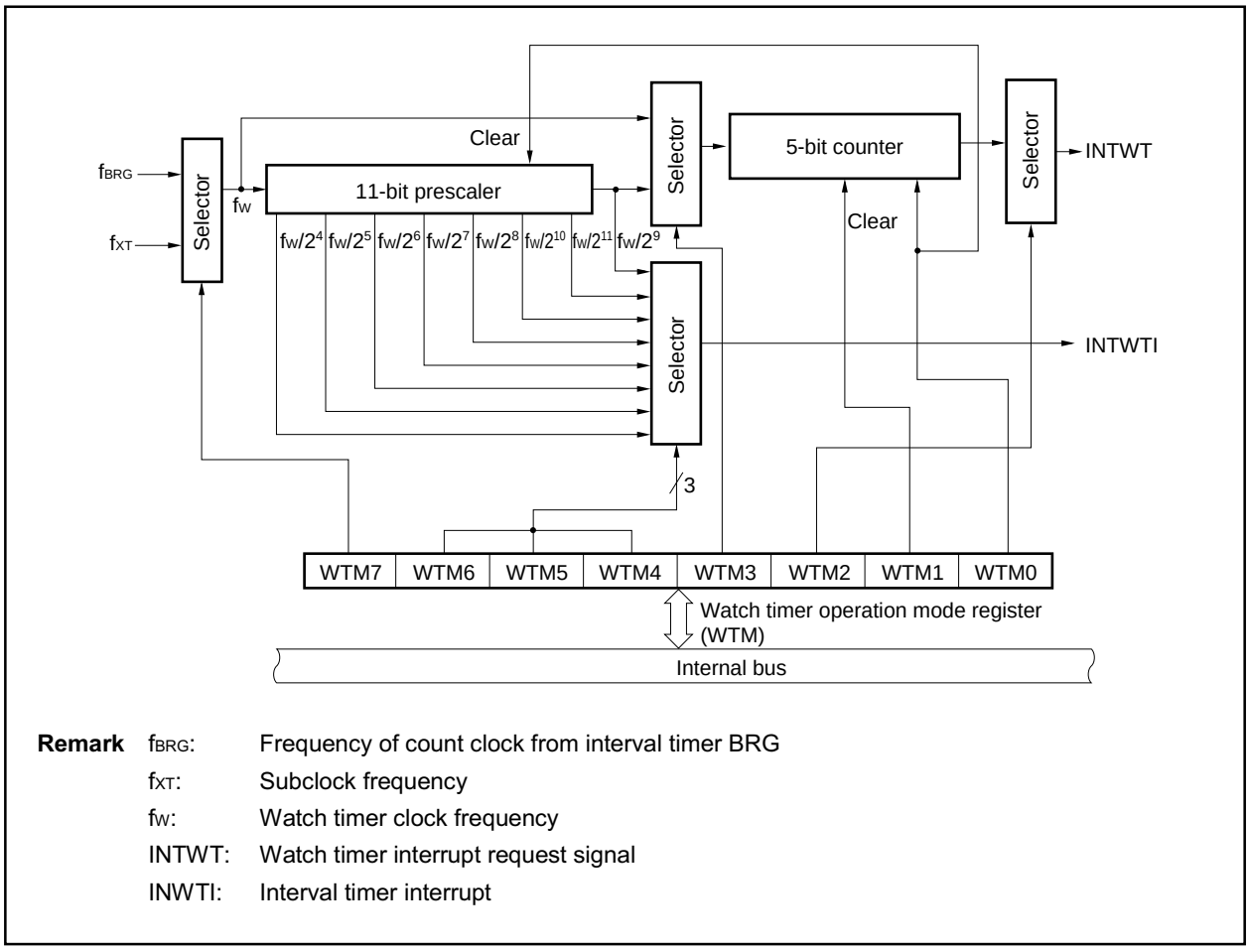
- Watch timer: An interrupt request signal (INTWT) is generated at time intervals of 0.5 or 0.25 seconds by using the main clock or subclock.
- Interval timer: An interrupt request signal (INTWTI) is generated at the preset time interval.

The watch timer and interval timer functions can be used at the same time.

10.2.2 Configuration

The following shows the block diagram of the watch timer.

Figure 10-2. Block Diagram of Watch Timer



Remark f_{BRG}: Frequency of count clock from interval timer BRG
f_{XT}: Subclock frequency
f_W: Watch timer clock frequency
INTWT: Watch timer interrupt request signal
INWTI: Interval timer interrupt

(1) 11-bit prescaler

The 11-bit prescaler generates a clock of $f_W/2^4$ to $f_W/2^{11}$ by dividing f_W.

(2) 5-bit counter

The 5-bit counter generates the watch timer interrupt request signal (INTWT) at intervals of $2^4/f_W$, $2^5/f_W$, $2^{13}/f_W$, or $2^{14}/f_W$ by counting f_W or $f_W/2^9$.

(3) Selectors

The watch timer has the following four selectors.

- Selector that selects the main clock (the clock from interval timer BRG (f_{BRG})) or the subclock (f_{XT}) as the clock for the watch timer.
- Selector that selects f_W or $f_W/2^9$ as the count clock frequency of the 5-bit counter
- Selector that selects $2^4/f_W$ or $2^{13}/f_W$, or $2^5/f_W$ or $2^{14}/f_W$ as the INTWT signal generation time interval.
- Selector that selects the generation time interval of the interval timer WT interrupt request signal (INTWTI) from $2^4/f_W$ to $2^{11}/f_W$.

(4) 8-bit counter

The 8-bit counter counts the count clock (f_{BGCS}).

(5) WTM register

The WTM register is an 8-bit register that controls the operation of the watch timer/interval timer WT and sets the interval of interrupt request signal generation.

10.2.3 Registers

The watch timer includes the following register.

(1) Watch timer operation mode register (WTM)

This register enables or disables the count clock and operation of the watch timer, sets the interval time of the 11-bit prescaler, controls the operation of the 5-bit counter, and sets the timer of watch timer interrupt request signal (INTWT) generation.

The WTM register is set by an 8-bit or 1-bit memory manipulation instruction.

After reset, WTM is cleared to 00H.

After reset: 00H R/W Address: FFFFF680H

	7	6	5	4	3	2	<1>	<0>
WTM	WTM7	WTM6	WTM5	WTM4	WTM3	WTM2	WTM1	WTM0

WTM7	WTM6	WTM5	WTM4	Selection of interval time of prescaler
0	0	0	0	$2^4/f_W$ (488 μs: $f_W = f_{XT}$)
0	0	0	1	$2^5/f_W$ (977 μs: $f_W = f_{XT}$)
0	0	1	0	$2^6/f_W$ (1.95 ms: $f_W = f_{XT}$)
0	0	1	1	$2^7/f_W$ (3.91 ms: $f_W = f_{XT}$)
0	1	0	0	$2^8/f_W$ (7.81 ms: $f_W = f_{XT}$)
0	1	0	1	$2^9/f_W$ (15.6 ms: $f_W = f_{XT}$)
0	1	1	0	$2^{10}/f_W$ (31.3 ms: $f_W = f_{XT}$)
0	1	1	1	$2^{11}/f_W$ (62.5 ms: $f_W = f_{XT}$)
1	0	0	0	$2^4/f_W$ (488 μs: $f_W = f_{BRG}$)
1	0	0	1	$2^5/f_W$ (977 μs: $f_W = f_{BRG}$)
1	0	1	0	$2^6/f_W$ (1.95 ms: $f_W = f_{BRG}$)
1	0	1	1	$2^7/f_W$ (3.91 ms: $f_W = f_{BRG}$)
1	1	0	0	$2^8/f_W$ (7.81 ms: $f_W = f_{BRG}$)
1	1	0	1	$2^9/f_W$ (15.6 ms: $f_W = f_{BRG}$)
1	1	1	0	$2^{10}/f_W$ (31.3 ms: $f_W = f_{BRG}$)
1	1	1	1	$2^{11}/f_W$ (62.5 ms: $f_W = f_{BRG}$)

WTM7	WTM3	WTM2	Selection of set time of watch flag
0	0	0	$2^{14}/f_W$ (0.5 s: $f_W = f_{XT}$)
0	0	1	$2^{13}/f_W$ (0.25 s: $f_W = f_{XT}$)
0	1	0	$2^5/f_W$ (977 μs: $f_W = f_{XT}$)
0	1	1	$2^4/f_W$ (488 μs: $f_W = f_{XT}$)
1	0	0	$2^{14}/f_W$ (0.5 s: $f_W = f_{BRG}$)
1	0	1	$2^{13}/f_W$ (0.25 s: $f_W = f_{BRG}$)
1	1	0	$2^5/f_W$ (977 μs: $f_W = f_{BRG}$)
1	1	1	$2^4/f_W$ (488 μs: $f_W = f_{BRG}$)

WTM1	Control of 5-bit counter operation
0	Clear after operation stops
1	Start

WTM0	Watch timer operation enable
0	Stop operation (clear both prescaler and 5-bit counter)
1	Enable operation

Caution Rewrite the WTM2 to WTM7 bits while both the WTM0 and WTM1 bits are 0.

Remarks 1. f_W: Watch timer clock frequency

2. Values in parentheses apply when f_W = 32.768 kHz

10.2.4 Operation

(1) Operation as watch timer

The watch timer generates an interrupt request at fixed time intervals. The watch timer operates using time intervals of 0.25 or 0.5 seconds with the subclock (32.768 kHz).

The count operation starts when bit 0 (WTM0) and bit 1 (WTM1) of the watch timer operation mode register (WTM) are set to 11. When these bits are set to 00, the 10-bit prescaler and 5-bit counter are cleared and the count operation stops.

The 5-bit counter can be cleared to synchronize the time by setting the WTM1 bit to 0 when the watch timer and interval timer WT operate simultaneously. At this time, an error of up to 15.6 ms may occur in the watch timer, but interval timer WT is not affected.

(2) Operation as interval timer

The watch timer can also be used as an interval timer that repeatedly generates an interrupt request signal (INTWTI) at intervals specified by a count value set in advance.

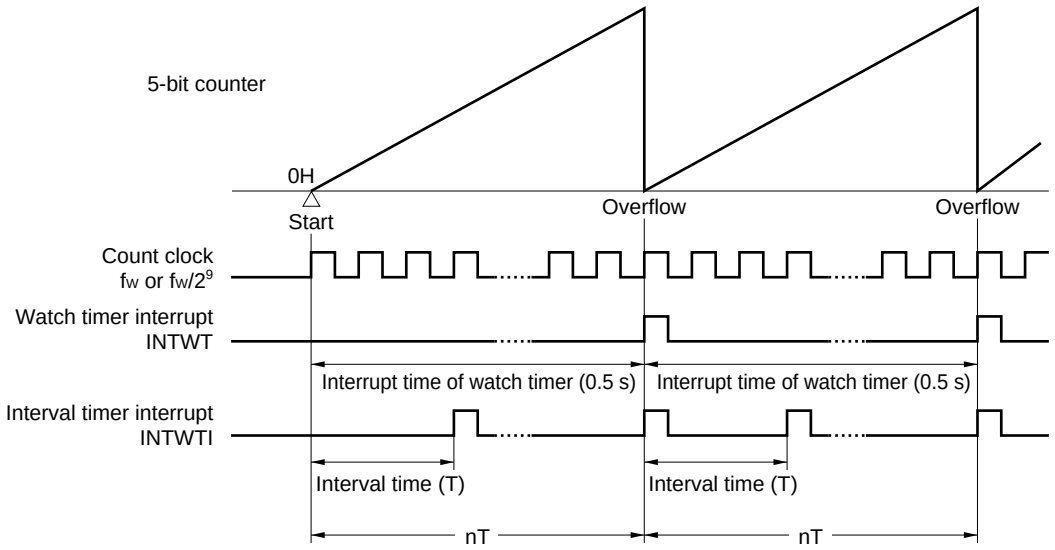
The interval time can be selected by bits 4 to 7 (WTM4 to WTM7) of the watch timer operation mode register (WTM).

Table 10-1. Interval Time of Interval Timer

WTM7	WTM6	WTM5	WTM4	Interval Time	
0	0	0	0	$2^4 \times 1/fw$	488 μs (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	0	0	1	$2^5 \times 1/fw$	977 μs (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	0	1	0	$2^6 \times 1/fw$	1.95 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	0	1	1	$2^7 \times 1/fw$	3.91 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	1	0	0	$2^8 \times 1/fw$	7.81 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	1	0	1	$2^9 \times 1/fw$	15.6 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	1	1	0	$2^{10} \times 1/fw$	31.3 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
0	1	1	1	$2^{11} \times 1/fw$	62.5 ms (operating at $f_W = f_{XT}$ = 32.768 kHz)
1	0	0	0	$2^4 \times 1/fw$	488 μs (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	0	0	1	$2^5 \times 1/fw$	977 μs (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	0	1	0	$2^6 \times 1/fw$	1.95 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	0	1	1	$2^7 \times 1/fw$	3.91 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	1	0	0	$2^8 \times 1/fw$	7.81 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	1	0	1	$2^9 \times 1/fw$	15.6 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	1	1	0	$2^{10} \times 1/fw$	31.3 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)
1	1	1	1	$2^{11} \times 1/fw$	62.5 ms (operating at $f_W = f_{BRG}$ = 32.768 kHz)

Remark f_W: Watch timer clock frequency

Figure 10-3. Operation Timing of Watch Timer/Interval Timer



Remarks 1. Assuming that the interrupt time of the watch timer is set to 0.5 seconds.

2. fw: Watch timer clock frequency

Values in parentheses apply when count clock fw = 32.768 kHz.

n: Number of interval timer WT operations

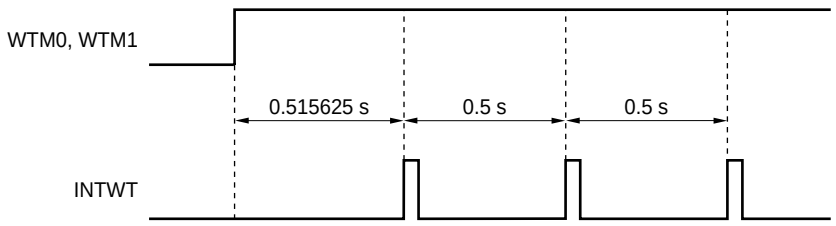
10.3 Cautions

(1) Operation as watch timer

Some time is required before the first watch timer interrupt request (INTWT) is generated after operation is enabled (WTM1 and WTM0 bits of WTM register = 1).

Figure 10-4. Example of Generation of Watch Timer Interrupt Request (INTWT) (When Interrupt Period = 0.5 s)

It takes 0.515625 seconds for the first INTWT to be generated ($2^9 \times 1/32768 = 0.015625$ s longer). INTWT is then generated every 0.5 seconds.



(2) When watch timer and interval timer BRG operate simultaneously

When using the subclock as the count clock for the watch timer, the interval time of interval timer BRG can be set to any value. Changing the interval time does not affect the watch timer (before changing the interval time, stop operation).

When using the main clock as the count clock for the watch timer, set the interval time of interval timer BRG to approximately 65,536 Hz. Do not change this value.

(3) When interval timer BRG and interval timer WT operate simultaneously

When using the subclock as the count clock for interval timer WT, the interval times of interval timers BRG and WT can be set to any values. They can also be changed later (before changing the value, stop operation).

When using the main clock as the count clock for interval timer WT, the interval time of interval timer BRG can be set to any value, but cannot be changed later (it can be changed only when interval timer WT stops operation). The interval time of interval timer WT can be set to $\times 2^5$ to $\times 2^{12}$ of the set value of interval timer BRG. It can also be changed later.

(4) When watch timer and interval timer WT operate simultaneously

The interval time of interval timer WT can be set to a value between 488 μs and 62.5 ms. It cannot be changed later.

Do not stop interval timer WT (clear (0) the WTM.WTM0 bit) while the watch timer is operating. If the WTM0 bit is set (1) after it had been cleared (0), the watch timer will have a discrepancy of up to 0.5 or 0.25 seconds.

(5) When watch timer, interval timer BRG, and interval timer WT operate simultaneously

When using the subclock as the count clock for the watch timer, the interval times of interval timers BRG and WT can be set to any values. The interval time of interval timer BRG can be changed later (before changing the value, stop operation).

When using the main clock as the count clock for the watch timer, set the interval time of interval timer BRG to approximately 65,536 Hz. It cannot be changed later. The interval time of interval timer WT can be set to a value between 488 μs and 62.5 ms. It cannot be changed later.

Do not stop interval timer BRG (clear (0) the PRSM.BGCE bit) or interval timer WT (clear (0) the WTM.WTM0 bit) while the watch timer is operating.

CHAPTER 11 WATCHDOG TIMER FUNCTIONS

11.1 Watchdog Timer 1

11.1.1 Functions

Watchdog timer 1 has the following operation modes.

- Watchdog timer
- Interval timer

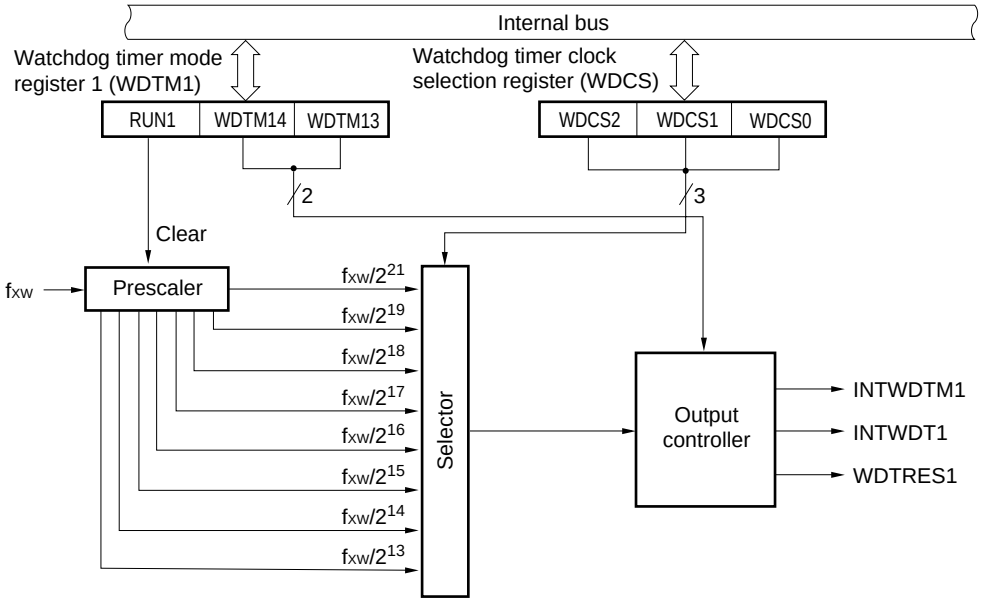
The following functions are realized from the above-listed operation modes.

- Generation of non-maskable interrupt request signal (INTWDT1) upon overflow of watchdog timer 1[Note]
- Generation of system reset signal (WDTRES1) upon overflow of watchdog timer 1
- Generation of maskable interrupt request signal (INTWDTM1) upon overflow of interval timer

Note For non-maskable interrupt servicing due to non-maskable interrupt request (INTWDT1, INTWDT2), refer to **19.10 Cautions**.

Remark Select whether to use watchdog timer 1 in the watchdog timer 1 mode or the interval timer mode with watchdog timer mode register 1 (WDTM1).

Figure 11-1. Block Diagram of Watchdog Timer 1



Remark INTWDTM1: Request signal for maskable interrupt through watchdog timer 1 overflow
INTWDT1: Request signal for non-maskable interrupt through watchdog timer 1 overflow
WDTRES1: Reset signal through watchdog timer 1 overflow
$f_{XW} = f_X$: Watchdog timer 1 clock frequency

11.1.2 Configuration

Watchdog timer 1 consists of the following hardware.

Table 11-1. Configuration of Watchdog Timer 1

Item	Configuration
Control register	Watchdog timer clock selection register (WDCS) Watchdog timer mode register 1 (WDTM1)

11.1.3 Watchdog timer 1 control register

The registers that control watchdog timer 1 are as follows.

- Watchdog timer clock selection register (WDCS)
- Watchdog timer mode register 1 (WDTM1)

(1) Watchdog timer clock selection register (WDCS)

This register sets the overflow time of watchdog timer 1 and the interval timer.

The WDCS register is set by an 8-bit or 1-bit memory manipulation instruction.

After reset, WDCS is cleared to 00H.

After reset: 00H R/W Address: FFFFF6C1H

	7	6	5	4	3	2	1	0
WDCS	0	0	0	0	0	WDCS2	WDCS1	WDCS0

WDCS2	WDCS1	WDCS0	Overflow time of watchdog timer 1/interval timer			
				f_{XW}		
				4 MHz	5 MHz	10 MHz
0	0	0	$2^{13}/f_{XW}$	2.048 ms	1.638 ms	0.819 ms
0	0	1	$2^{14}/f_{XW}$	4.096 ms	3.277 ms	1.638 ms
0	1	0	$2^{15}/f_{XW}$	8.192 ms	6.554 ms	3.277 ms
0	1	1	$2^{16}/f_{XW}$	16.38 ms	13.11 ms	6.554 ms
1	0	0	$2^{17}/f_{XW}$	32.77 ms	26.21 ms	13.11 ms
1	0	1	$2^{18}/f_{XW}$	65.54 ms	52.43 ms	26.2 ms
1	1	0	$2^{19}/f_{XW}$	131.1 ms	104.9 ms	52.43 ms
1	1	1	$2^{21}/f_{XW}$	524.3 ms	419.4 ms	209.7 ms

Remark $f_{XW} = f_X$: Watchdog timer 1 clock frequency

(2) Watchdog timer mode register 1 (WDTM1)

This register sets the watchdog timer 1 operation mode and enables/disables count operations.

This register is a special register that can be written only in a special sequence (refer to **3.4.7 Special registers**).

The WDTM1 register is set by an 8-bit or 1-bit memory manipulation instruction.

After reset, WDTM1 is cleared to 00H.

Caution When the main clock is stopped and the CPU is operating on the subclock, do not access the WDTM1 register using an access method that causes a wait.
For details, refer to 3.4.8 (2).

After reset: 00H R/W Address: FFFFF6C2H

	<7>	6	5	4	3	2	1	0
WDTM1	RUN1	0	0	WDTM14	WDTM13	0	0	0

RUN1	Selection of operation mode of watchdog timer 1[Note 1]
0	Stop counting
1	Clear counter and start counting

WDTM14	WDTM13	Selection of operation mode of watchdog timer 1[Note 2]
0	0	Interval timer mode
0	1	(Upon overflow, maskable interrupt INTWDTM1 is generated.)
1	0	Watchdog timer mode 1[Note 3]
		(Upon overflow, non-maskable interrupt INTWDT1 is generated.)
1	1	Watchdog timer mode 2
		(Upon overflow, reset operation WDTRES1 is started.)

Notes 1. Once the RUN1 bit is set (to 1), it cannot be cleared (to 0) by software.
Therefore, when counting is started, it cannot be stopped except through $\overline{\text{RESET}}$ input.

2. Once the WDTM13 and WDTM14 bits are set (to 1), they cannot be cleared (to 0) by software and can be cleared only through $\overline{\text{RESET}}$ input.

3. For non-maskable interrupt servicing due to non-maskable interrupt request (INTWDT1), refer to **19.10 Cautions**.

11.1.4 Operation

(1) Operation as watchdog timer 1

Watchdog timer 1 operation to detect a program loop is selected by setting bit 4 (WDTM14) of watchdog timer mode register 1 (WDTM1) to 1.

The count clock (program loop detection time interval) of watchdog timer 1 can be selected using bits WDCS0 to WDCS2 of the watchdog timer clock selection register (WDCS). The count operation is started by setting bit 7 (RUN1) of the WDTM1 register to 1. When, after the count operation is started, the RUN1 bit is again set to 1 within the set program loop detection time interval, watchdog timer 1 is cleared and the count operation starts again.

If the program loop detection time is exceeded without RUN1 bit being set to 1, reset (WDTRES1) through the value of bit WDTM13 of the WDTM1 register or a non-maskable interrupt request signal (INTWDT1) is generated.

The count operation of watchdog timer 1 stops in the STOP mode and IDLE mode. Set the RUN1 bit to 1 before the STOP mode or IDLE mode is entered in order to clear watchdog timer 1.

Because watchdog timer 1 operates in the HALT mode, make sure that an overflow will not occur during HALT.

Cautions 1. When the subclock is selected for the CPU clock, the count operation of watchdog timer 1 is stopped (the value of watchdog timer 1 is maintained).

2. For non-maskable interrupt servicing due to INTWDT1, refer to 19.10 Cautions.

Table 11-2. Program Loop Detection Time of Watchdog Timer 1

Clock	Program Loop Detection Time		
	f_{XW} = 4 MHz	f_{XW} = 5 MHz	f_{XW} = 10 MHz
$2^{13}/f_{XW}$	2.048 ms	1.638 ms	0.819 ms
$2^{14}/f_{XW}$	4.096 ms	3.277 ms	1.683 ms
$2^{15}/f_{XW}$	8.192 ms	6.554 ms	3.277 ms
$2^{16}/f_{XW}$	16.38 ms	13.11 ms	6.554 ms
$2^{17}/f_{XW}$	32.77 ms	26.21 ms	13.11 ms
$2^{18}/f_{XW}$	65.54 ms	52.43 ms	26.21 ms
$2^{19}/f_{XW}$	131.1 ms	104.9 ms	52.43 ms
$2^{21}/f_{XW}$	524.3 ms	419.4 ms	209.7 ms

Remark $f_{XW} = f_X$: Watchdog timer 1 clock frequency

(2) Operation as interval timer

Watchdog timer 1 can be made to operate as an interval timer that repeatedly generates interrupts using the count value set in advance as the interval, by setting bit 4 (WDTM14) of watchdog timer mode register 1 (WDTM1) to 0.

When watchdog timer 1 operates as an interval timer, the interrupt mask flag (WDTMK) and priority specification flags (WDTPR0 to WDTPR2) of the WDTIC register are valid and maskable interrupt request signals (INTWDTM1) can be generated. The default priority of the INTWDTM1 signal is set to the highest level among the maskable interrupt request signals.

The interval timer continues to operate in the HALT mode, but it stops operating in the STOP mode and the IDLE mode.

Cautions 1. Once the WDTM14 bit is set to 1 (thereby selecting the watchdog timer 1 mode), the interval timer mode is not entered as long as $\overline{\text{RESET}}$ is not input.

2. When the subclock is selected for the CPU clock, the count operation of the watchdog timer 1 stops (the value of the watchdog timer is maintained).

Table 11-3. Interval Time of Interval Timer

Clock	Interval Time		
	f_{XW} = 4 MHz	f_{XW} = 5 MHz	f_{XW} = 10 MHz
$2^{13}/f_{XW}$	2.048 ms	1.638 ms	0.819 ms
$2^{14}/f_{XW}$	4.096 ms	3.277 ms	1.638 ms
$2^{15}/f_{XW}$	8.192 ms	6.554 ms	3.277 ms
$2^{16}/f_{XW}$	16.38 ms	13.11 ms	6.554 ms
$2^{17}/f_{XW}$	32.77 ms	26.21 ms	13.11 ms
$2^{18}/f_{XW}$	65.54 ms	52.43 ms	26.21 ms
$2^{19}/f_{XW}$	131.1 ms	104.9 ms	52.43 ms
$2^{21}/f_{XW}$	524.3 ms	419.4 ms	209.7 ms

Remark $f_{XW} = f_X$: Watchdog timer 1 clock frequency

11.2 Watchdog Timer 2

11.2.1 Functions

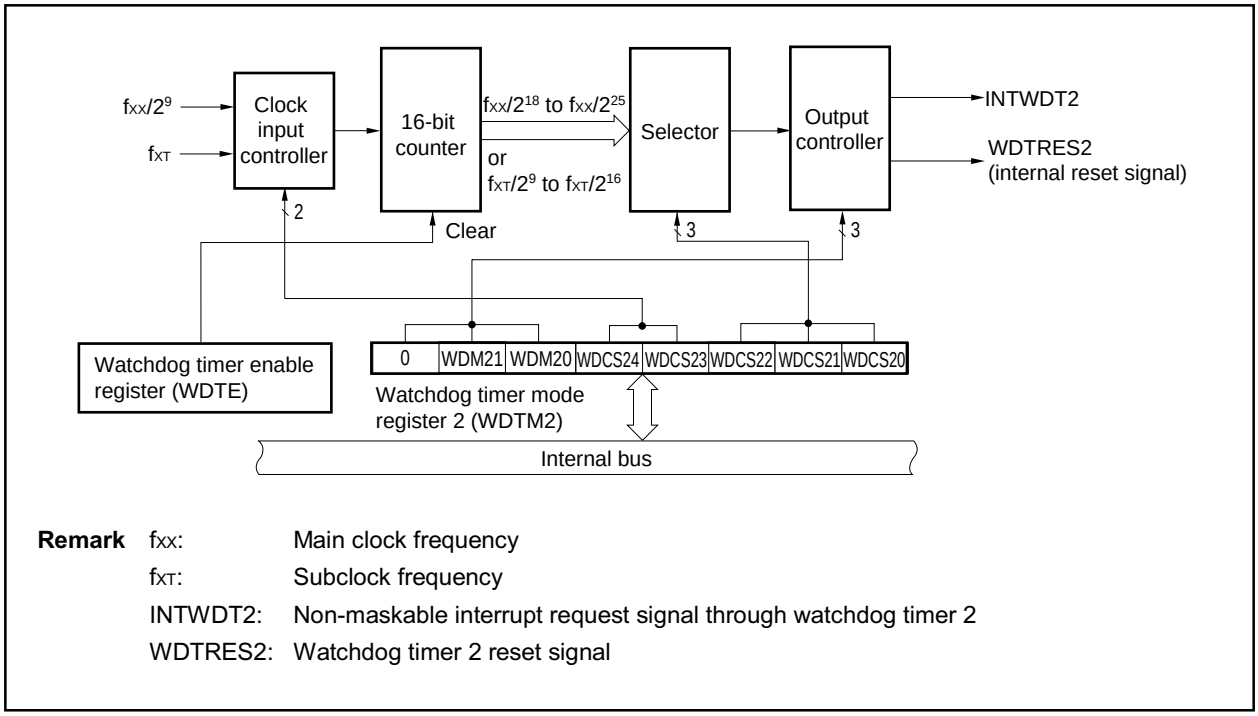
Watchdog timer 2 has the following functions.

- Default start watchdog timer[Note 1]
  → Reset mode: Reset operation upon overflow of watchdog timer 2 (generation of WDTRES2)
  → Non-maskable interrupt request mode: NMI operation upon overflow of watchdog timer 2 (generation of INTWDT2)[Note 2]
- Input selectable from main clock and subclock as the source clock

Notes 1. Watchdog timer 2 automatically starts in the reset mode following reset release.
When watchdog timer 2 is not used, either stop its operation before reset is executed through this function, or clear once watchdog timer 2 and stop it within the next interval time.
Also, write to the WDTM2 register for verification purposes only once, even if the default settings (reset mode, interval time: $f_{XX}/2^{25}$) need not be changed.

2. For non-maskable interrupt servicing due to a non-maskable interrupt request (INTWDT2), refer to **19.10 Cautions**.

Figure 11-2. Block Diagram of Watchdog Timer 2



Remark f_{XX}: Main clock frequency
f_{XT}: Subclock frequency
INTWDT2: Non-maskable interrupt request signal through watchdog timer 2
WDTRES2: Watchdog timer 2 reset signal

11.2.2 Configuration

Watchdog timer 2 consists of the following hardware.

Table 11-4. Configuration of Watchdog Timer 2

Item	Configuration
Control register	Watchdog timer mode register 2 (WDTM2) Watchdog timer enable register (WDTE)

11.2.3 Watchdog timer 2 control register

(1) Watchdog timer mode register 2 (WDTM2)

This register sets the overflow time and operation clock of watchdog timer 2.

WDTM2 is set with an 8-bit memory manipulation instruction. This register can be read any number of times, but it can be written only once following reset release.

After reset, WDTM2 is cleared to 67H.

Caution When the main clock is stopped and the CPU is operating on the subclock, do not access the WDTM2 register using an access method that causes a wait.
For details, refer to 3.4.8 (2).

After reset: 67H R/W Address: FFFFF6D0H

	7	6	5	4	3	2	1	0
WDTM2	0	WDM21	WDM20	WDCS24	WDCS23	WDCS22	WDCS21	WDCS20

WDM21	WDM20	Selection of operation mode of watchdog timer 2
0	0	Stops operation
0	1	Non-maskable interrupt request mode (generation of INTWDT2)
1	–	Reset mode (generation of WDTRES2)

Cautions 1. To stop the operation of watchdog timer 2, write "1FH" to the WDTM2 register.
2. For details about bits WDCS0 to WDCS4, refer to Table 11-5 Watchdog Timer 2 Clock Selection.
3. If the WDTM2 register is written twice after a reset, an overflow signal is forcibly output.

Table 11-5. Watchdog Timer 2 Clock Selection

WDCS24	WDCS23	WDCS22	WDCS21	WDCS20	Selected Clock	f_{XX} = 20 MHz	f_{XX} = 16 MHz	f_{XX} = 10 MHz
0	0	0	0	0	$2^{18}/f_{XX}$	13.1 ms	16.4 ms	26.2 ms
0	0	0	0	1	$2^{19}/f_{XX}$	26.2 ms	32.8 ms	52.4 ms
0	0	0	1	0	$2^{20}/f_{XX}$	52.4 ms	65.5 ms	104.9 ms
0	0	0	1	1	$2^{21}/f_{XX}$	104.9 ms	131.1 ms	209.7 ms
0	0	1	0	0	$2^{22}/f_{XX}$	209.7 ms	262.1 ms	419.4 ms
0	0	1	0	1	$2^{23}/f_{XX}$	419.4 ms	524.3 ms	838.9 ms
0	0	1	1	0	$2^{24}/f_{XX}$	838.9 ms	1048.6 ms	1677.7 ms
0	0	1	1	1	$2^{25}/f_{XX}$	1677.7 ms	2097.2 ms	3355.4 ms
0	1	0	0	0	$2^{9}/f_{XT}$	15.625 ms (f_{XT} = 32.768 kHz)		
0	1	0	0	1	$2^{10}/f_{XT}$	31.25 ms (f_{XT} = 32.768 kHz)		
0	1	0	1	0	$2^{11}/f_{XT}$	62.5 ms (f_{XT} = 32.768 kHz)		
0	1	0	1	1	$2^{12}/f_{XT}$	125 ms (f_{XT} = 32.768 kHz)		
0	1	1	0	0	$2^{13}/f_{XT}$	250 ms (f_{XT} = 32.768 kHz)		
0	1	1	0	1	$2^{14}/f_{XT}$	500 ms (f_{XT} = 32.768 kHz)		
0	1	1	1	0	$2^{15}/f_{XT}$	1000 ms (f_{XT} = 32.768 kHz)		
0	1	1	1	1	$2^{16}/f_{XT}$	2000 ms (f_{XT} = 32.768 kHz)		
1	×	×	×	×	Operation stopped			

(2) Watchdog timer enable register (WDTE)

The counter of watchdog timer 2 is cleared and counting restarted by writing “ACH” to WDTE.

WDTE is set by an 8-bit memory manipulation instruction.

After reset, WDTE is cleared to 9AH.

After reset: 9AH R/W Address: FFFFF6D1H

	7	6	5	4	3	2	1	0
WDTE								

Cautions 1. When a value other than “ACH” is written to the WDTE register, an overflow signal is forcibly output.

2. When a 1-bit memory manipulation instruction is executed for the WDTE register, an overflow signal is forcibly output.

3. The read value of the WDTE register is “9AH” (value that differs from written value “ACH”).

11.2.4 Operation

Watchdog timer 2 automatically starts in the reset mode following reset release.

The WDTM2 register can be written to only once following reset through byte access. To use watchdog timer 2, write the operation mode and the interval time to the WDTM2 register using 8-bit memory manipulation instructions. After this is done, the operation of watchdog timer 2 cannot be stopped.

The watchdog timer 2 program loop detection time interval can be selected by the WDCS24 to WDCS20 bits of the WDTM2 register. Writing ACH to the WDTE register clears the counter of watchdog timer 2 and starts the count operation again. After the count operation starts, write ACH to the WDTE register within the set program loop detection time interval.

If the program loop detection time is exceeded without ACH being written to the WDTE register, a reset signal (WDTRES2) or non-maskable interrupt request signal (INTWDT2) is generated depending on the set value of the WDM21 and WDM20 bits of the WDTM2 register.

To not use watchdog timer 2, write 1FH to the WDTM2 register.

For non-maskable interrupt servicing when the non-maskable interrupt request mode is set, refer to **19.10 Cautions**.

Watchdog timer 2 stops operation in the STOP mode and IDLE mode. Therefore, set the RUN1 bit 1 before entering the STOP mode or IDLE mode to clear watchdog timer 2.

Because watchdog timer 2 operates in the HALT mode, make sure that an overflow will not occur during HALT.

CHAPTER 12 REAL-TIME OUTPUT FUNCTION (RTO)

12.1 Function

The real-time output function (RTO) transfers preset data to real-time output buffer registers n (RTBLn, RTBHn), and then transfers this data with hardware to an external device via the real-time output latches, upon occurrence of a timer interrupt. The pins through which the data is output to an external device constitute a port called a real-time output port.

Because RTO can output signal without jitter, it is suitable for controlling a stepping motor.

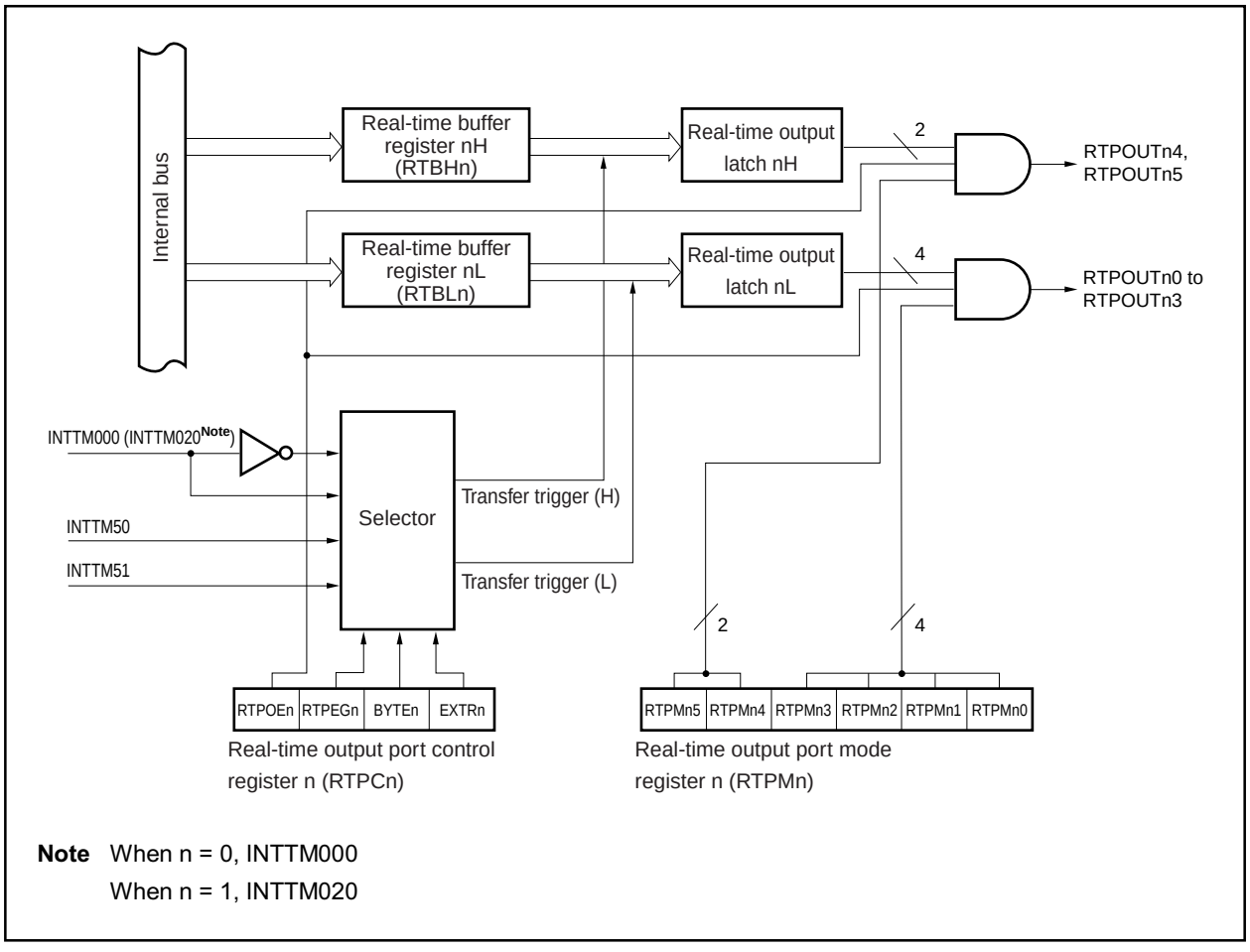
In the V850ES/KF1 and V850ES/KG1, one 6-bit real-time output port channel is provided.

In the V850ES/KJ1, two 6-bit real-time output port channels are provided.

The real-time output port can be set in the port mode or real-time output port mode in 1-bit units.

The block diagram of RTO is shown below.

Figure 12-1. Block Diagram of RTO



Note When n = 0, INTTM000
When n = 1, INTTM020

12.2 Configuration

RTO consists of the following hardware.

Table 12-1. Configuration of RTO

Item	Configuration
Registers	Real-time output buffer register n (RTBLn, RTBHn)
Control registers	Real-time output port mode register n (RTPMn) Real-time output port control register n (RTPCn)

(1) Real-time output buffer register n (RTBLn, RTBHn)

RTBLn and RTBHn are 4-bit registers that hold output data in advance.

These registers are mapped to independent addresses in the peripheral I/O register area.

They can be read/written in 8-bit or 1-bit units.

If an operation mode of 4 bits × 1 channel or 2 bits × 1 channel is specified (BYTEn = 0), data can be individually set to the RTBLn and RTBHn registers. The data of both these registers can be read at once by specifying the address of either of these registers.

If an operation mode of 6 bits × 1 channel is specified (BYTEn = 1), 8-bit data can be set to both the RTBLn and RTBHn registers by writing the data to either of these registers. Moreover, the data of both these registers can be read at once by specifying the address of either of these registers.

Table 12-2 shows the operation when the RTBLn and RTBHn registers are manipulated.

After reset : 00H R/W Address : RTBLn : FFFFF6E0H, FFFFF6F0
RTBHn : FFFFF6E2H, FFFFF6F2

	7	6	5	4	3	2	1	0
RTBLn					RTBLn3	RTBLn2	RTBLn1	RTBLn0
RTBHn	0	0	RTBHn5	RTBHn4				

Cautions 1. When writing to bits 6 and 7 of the RTBHn register, always write 0.

2. When the main clock is stopped and the CPU is operating on the subclock, do not access the RTBLn and RTBHn registers using an access method that causes a wait. For details, refer to 3.4.8 (2).

Remark n = 0, 1

n = 1 only for the V850ES/KJ1.

Table 12-2. Operation During Manipulation of Real-Time Output Buffer Registers n

Operation Mode	Register to Be Manipulated	Read		Write[Note]	
		Higher 4 bits	Lower 4 bits	Higher 4 bits	Lower 4 bits
4 bits × 1 channel, 2 bits × 1 channel	RTBLn	RTBHn	RTBLn	Invalid	RTBLn
	RTBHn	RTBHn	RTBLn	RTBHn	Invalid
6 bits × 1 channel	RTBLn	RTBHn	RTBLn	RTBHn	RTBLn
	RTBHn	RTBHn	RTBLn	RTBHn	RTBLn

Note After setting the real-time output port, set output data to the RTBLn and RTBHn registers by the time a real-time output trigger is generated.

12.3 RTO Control Registers

RTO is controlled using the following two types of registers.

- Real-time output port mode register n (RTPMn)
- Real-time output port control register n (RTPCn)

(1) Real-time output port mode register n (RTPMn)

This register selects the real-time output port mode or port mode in 1-bit units.

The RTPMn register is set by an 8-bit or 1-bit memory manipulation instruction.

After reset, RTPMn is cleared to 00H.

After reset : 00H R/W Address : FFFFF6E4H, FFFF6F4H

	7	6	5	4	3	2	1	0
RTPMn (n = 0, 1)	0	0	RTPMn5	RTPMn4	RTPMn3	RTPMn2	RTPMn1	RTPMn0

RTPMn	Control of real-time output port (n = 0 to 5)
0	Real-time output disabled
1	Real-time output enabled

Cautions 1. To reflect real-time output signals (RTPOUTn0 to RTPOUTn5) to the pins (RTPn0 to RTPn5), set them to the real-time output port with the PMC and PFC registers.

2. By enabling real-time output operation (RTPOEn = 1), the bits specified as real-time output enabled perform real-time output, and the bits specified as real-time output disabled output 0.

3. If real-time output is disabled (RTPOEn = 0), real-time output signals (RTPOUTn0 to RTPOUTn5) all output 0, regardless of the RTPMn register setting.

Remark n = 1 only in the V850ES/KJ1.

(2) Real-time output port control register n (RTPCn)

RTPCn are registers used to set the operation mode and output trigger of the real-time output port.

The relationship between the operation mode and output trigger of the real-time output port is as shown in Tables 12-3 and 12-4.

The RTPCn register is set by an 8-bit or 1-bit memory manipulation instruction.

After reset, RTPCn is cleared to 00H.

After reset : 00H R/W Address : FFFFF6E5H, FFFFF6F5H

RTPCn (n = 0, 1)

7	6	5	4	3	2	1	0
RTPOEn	RTPEGn	BYTEn	EXTRn	0	0	0	0

RTPOEn	Control of real-time output operation
0	Disables operation[Note 1]
1	Enables operation

RTPEGn	Valid edge of INTTM000 (n = 0), INTTM020 (n = 1) signal
0	Falling edge[Note 2]
1	Rising edge

BYTEn	Specification of channel configuration for real-time output
0	4 bits × 1 channel, 2 bits × 1 channel
1	6 bits × 1 channel

Notes 1. When real-time output operation is disabled (RTPOEn = 0), real-time output signals (RTPOUTn0 to RTPOUTn5) all output 0.

2. INTTM000 and INTTM020 are output for 1 clock of the count clock selected with the respective timers.

Caution Perform the settings for the RTPEGn, BYTEn, and EXTRn bits only when RTPOEn = 0.

Remark n = 1 only in the V850ES/KJ1

Table 12-3. Operation Modes and Output Triggers of Real-Time Output Port (n = 0)

BYTE0	EXTR0	Operation Mode	RTBH0 (RTP04, RTP05)	RTBL0 (RTP00 to RTP03)
0	0	4 bits × 1 channel,	INTTM51	INTTM50
	1	2 bits × 1 channel	INTTM50	INTTM000
1	0	6 bits × 1 channel	INTTM50	
	1		INTTM000	

Table 12-4. Operation Modes and Output Triggers of Real-Time Output Port (n = 1, V850ES/KJ1 only)

BYTE1	EXTR1	Operation Mode	RTBH1 (RTP14, RTP15)	RTBL1 (RTP10 to RTP13)
0	0	4 bits × 1 channel,	INTTM50	INTTM51
	1	2 bits × 1 channel	INTTM51	INTTM020
1	0	6 bits × 1 channel	INTTM51	
	1		INTTM020	

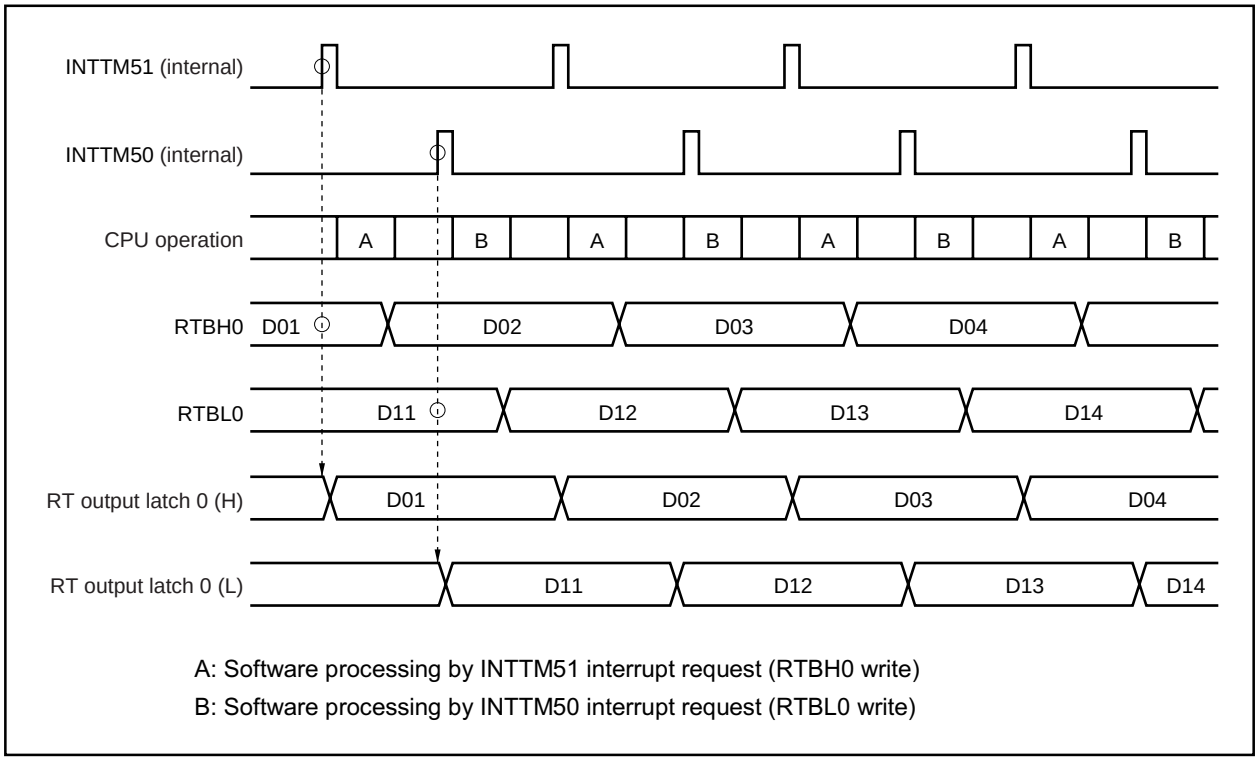
12.4 Operation

If the real-time output operation is enabled by setting bit 7 (RTPOEn) of real-time output port control register n (RTPCn) to 1, the data of real-time output buffer register n (RTBHn, RTBLn) is transferred to the real-time output latch in synchronization with the generation of the selected transfer trigger (set by EXTRn and BYTEn[Note]). Of the transferred data, only the data of the bits specified as real-time output enabled by real-time output port mode register n (RTPMn) is output from bits RTPOUTn0 to RTPOUTn5. The bits specified as real-time output disabled by the RTPMn register output 0.

If the real-time output operation is disabled by clearing RTPOEn to 0, RTPOUTn0 to RTPOUTn5 output 0 regardless of the setting of the RTPMn register.

Note EXTRn: Bit 4 of the real-time output port control register n (RTPCn)
BYTEn: Bits 5 of the real-time output port control register n (RTPCn)

Figure 12-2. Example of Operation Timing of RTO0 (When EXTR0 = 0, BYTE0 = 0)



Remark For the operation during standby, refer to **CHAPTER 21 STANDBY FUNCTION**.

12.5 Usage

(1) Disable real-time output.
Clear bit 7 (RTPOEn) of real-time output port control register n (RTPCn) to 0.

(2) Perform initialization as follows.
- Specify the real-time output port mode or port mode in 1-bit units.
  Set real-time output port mode register n (RTPMn).
- Channel configuration: Select the trigger and valid edge.
  Set bits 4 to 6 (EXTRn, BYTEn, and RTPEGn) of the RTPCn register.
- Set the initial values to real-time output buffer register n (RTBHn, RTBLn)[Note 1].

(3) Enable real-time output.
Set RTPOEn = 1.

(4) Set the next output value to the RTBHn and RTBLn registers by the time the selected transfer trigger is generated[Note 2].

(5) Set the next real-time output value to the RTBHn and RTBLn registers through interrupt servicing corresponding to the selected trigger.

Notes 1. If write to the RTBHn and RTBLn registers is performed when RTPOEn = 0, that value is transferred to real-time output latches nH and nL, respectively.

2. Even if write is performed to the RTBHn and RTBLn registers when RTPOEn = 1, data transfer to real-time output latches nH and nL is not performed.

Caution To reflect the real-time output signals (RTPOUTn0 to RTPOUTn5) to the pins, set the real-time output ports (RTPn0 to RTPn5) with the PMC and PFC registers.

12.6 Cautions

(1) Prevent the following conflicts by software.

- Conflict between real-time output disable/enable switching (RTPOEn bit) and selected real-time output trigger
- Conflict between write to the RTBHn and RTBLn registers in the real-time output enabled status and the selected real-time output trigger.

(2) Before performing initialization, disable real-time output (RTPOEn = 0).

(3) Once real-time output has been disabled (RTPOEn = 0), be sure to initialize the real-time output buffer registers (RTBHn and RTBLn) before enabling real-time output again (RTPOEn = 0 → 1).

12.7 Security Function

A circuit that sets the pin outputs to high impedance as a security function for when malfunctions of a stepping motor controlled by RTO occur is provided on chip. It forcibly resets the pins allocated to RTP00 to RTP05 via external interrupt INTP0 edge detection, and the pins allocated to RTP10 to RTP15[Note 1] via INTP1 edge detection, placing them in the high-impedance state.

The ports (P50 to 55, P60 to 65[Note 1]) placed in high impedance by INTP0[Note 2] and INTP1[Note 2] are initialized[Note 3], so settings for these ports must be performed again.

Notes 1. Only in the V850ES/KJ1

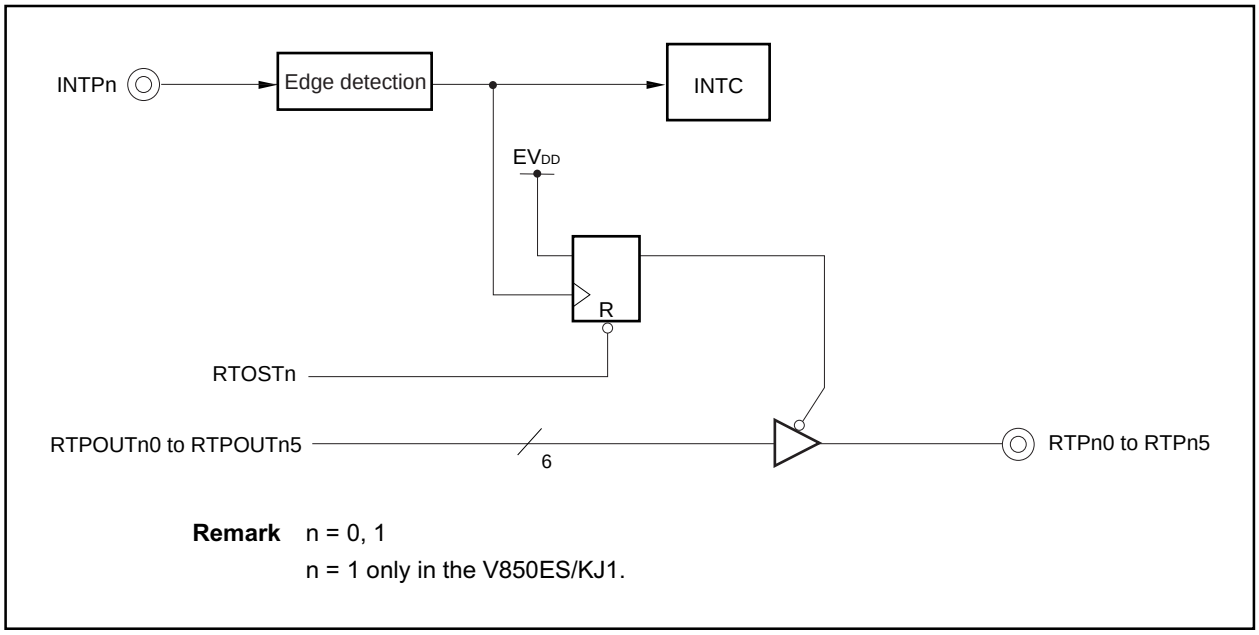
2. Regardless of the port settings, P50 to 55 and P60 to 65 are all placed in high impedance via INTPn.

3. The bits that are initialized are all the bits corresponding to P50 to 55 and P60 to 65 of the following registers.

- P5, P6L
- PM5, PM6L
- PMC5, PMC6L
- PU5, PU6L
- PFC5
- PF5

The block diagram of the security function is shown below.

Figure 12-3. Block Diagram of Security Function



Remark n = 0, 1
n = 1 only in the V850ES/KJ1.

This function is set with bits 3 and 2 (RTOST1, RTOST0) of the PLL control register (PLLCTL).

(1) PLL control register (PLLCTL)

PLLCTL is an 8-bit register that controls the PLL.

This register can be read/written in 8-bit or 1-bit units.

After reset, PLLCTL is cleared to 00H.

After reset : 01H R/W Address : FFFFF806H

	7	6	5	4	<3>	<2>	<1>	<0>
PLLCTL	0	0	0	0	RTOST1 Note 1	RTOST0	SELPLL Note 2	PLLON Note 2

RTOSTn	Control of RTPn0 to RTPn5 security function
0	INTPn is not used as trigger for security function
1	INTPn is used as trigger for security function

Notes 1. The RTOST1 bit is valid only in the V850ES/KJ1.
In the V850ES/KG1 and V850ES/KF1, this bit is fixed to 0. Changing the value of this bit does not affect the operation.

2. For details on the SELPLL bit and the PLLON bit, refer to **CHAPTER 6 CLOCK GENERATION FUNCTION**.

Cautions 1. Before outputting a value to the real-time output ports (RTPn0 to RTPn5), select INTPn interrupt edge detection and then set the RTOST0 and RTOS1 bits.

2. To set again the ports (P50 to P55, P60 to P65) as real-time output ports after placing them in high impedance via INTPn, first cancel the security function.
[Procedure to set ports again]
<1> Cancel the security function and enable port setting by setting RTOSTn = 0.
<2> Set RTOSTn = 1 (only if required)
<3> Set again as RTP pin.

3. Be sure to set bits 4 to 7 to 0.

Remark n = 0 (V850ES/KF1, V850ES/KG1)
n = 0, 1 (V850ES/KJ1)

CHAPTER 13 A/D CONVERTER

13.1 Function

The A/D converter converts analog input signals into digital values with a resolution of 10 bits. In the V850ES/KF1 and V850ES/KG1, it has an 8-channel (ANI0 to ANI7) configuration, and in the V850ES/KJ1, it has a 16-channel (ANI0 to ANI15) configuration.

The A/D converter has the following functions.

(1) 10-bit resolution A/D conversion

1 analog input channel is selected from ANI0 to ANI7 or ANI0 to ANI15, and an A/D conversion operation with resolution of 10 bits is repeatedly executed. Every time A/D conversion is completed, an interrupt request signal (INTAD) is generated.

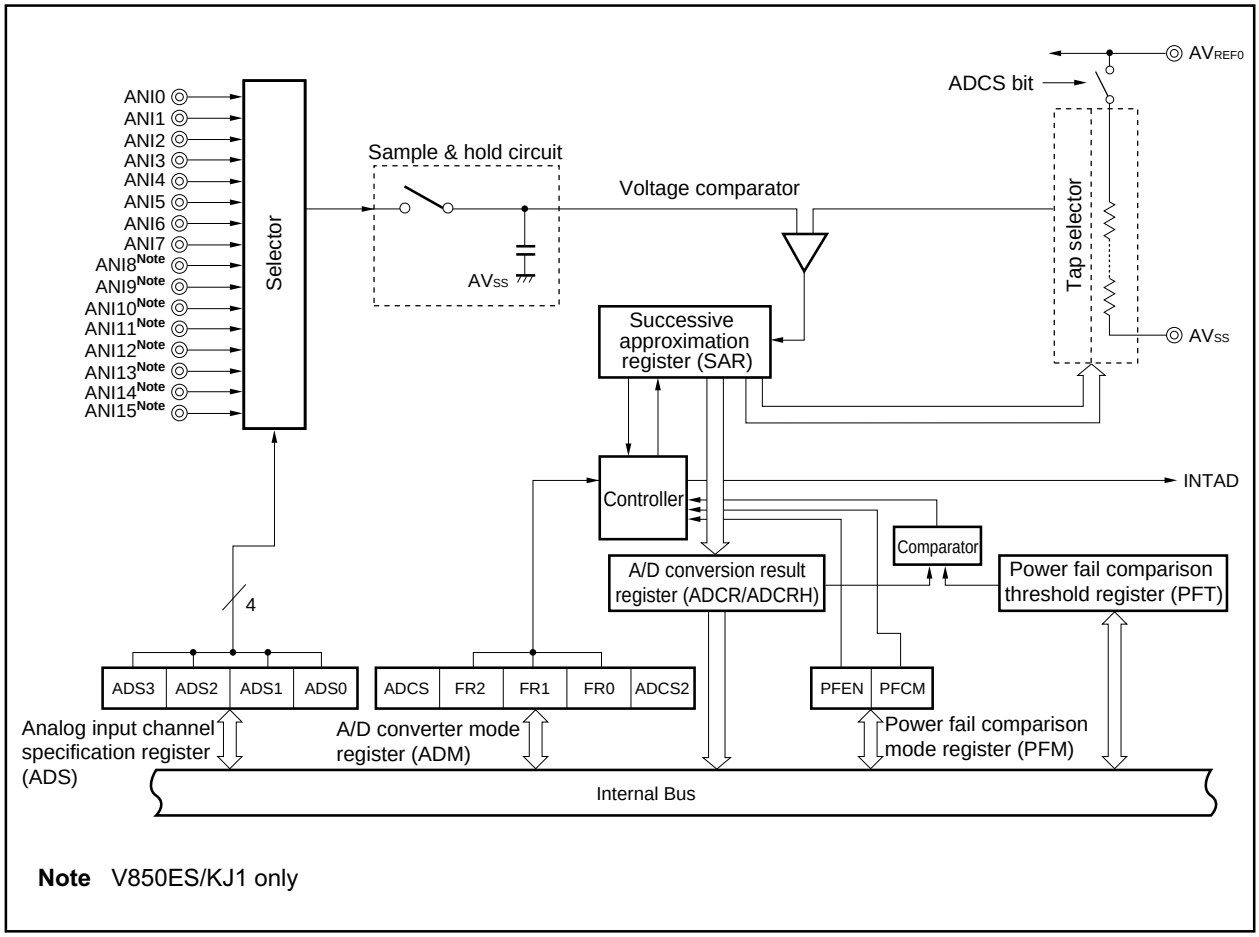
(2) Power fail detection function

This is a function to detect low voltage in a battery. The results of A/D conversion (the value in the ADCRH register) and the power fail compare threshold register (PFT) are compared, and INTAD is generated only when the comparison conditions match.

13.2 Configuration

The A/D converter consists of the following hardware.

Figure 13-1. Block Diagram of A/D Converter



Note V850ES/KJ1 only

Table 13-1. Registers of A/D Converter Used by Software

Item	Configuration
Registers	A/D conversion result register (ADCR) A/D conversion result register H (ADCRH): Only higher 8 bits can be read Power fail comparison threshold register (PFT) A/D converter mode register (ADM) Analog input channel specification register (ADS) Power fail comparison mode register (PFM)

(1) ANI0 to ANI15 pins[Note]

These are analog input pins for the 16 channels[Note] of the A/D converter. They are used to input analog signals to be converted into digital signals. Pins other than those selected as analog input by the analog input channel specification register (ADS) can be used as input ports.

Note The V850ES/KF1 and V850ES/KG1 provide only 8 channels, ANI0 to ANI7.

(2) Sample & hold circuit

The sample & hold circuit samples the analog input signals selected by the input circuit and sends the sampled data to the voltage comparator. This circuit holds the sampled analog input voltage during A/D conversion.

(3) Series resistor string

The series resistor string is connected between AV_{REF0} and AV_{SS} and generates a voltage for comparison with the analog input signal.

(4) Voltage comparator

The voltage comparator compares the value that is sampled and held with the output voltage of the series resistor string.

(5) Successive approximation register (SAR)

This register compares the sampled analog voltage value with the voltage value from the series resistor string, and converts the comparison result starting from the most significant bit (MSB).

When the least significant bit (LSB) has been converted to a digital value (end of A/D conversion), the contents of the SAR are transferred to the A/D conversion result register.

(6) A/D conversion result register (ADCR), A/D conversion result register H (ADCRH)

Each time A/D conversion ends, the conversion results are loaded from the successive approximation register and the results of A/D conversion are held in the higher 10 bits of this register (the lower 6 bits are fixed to 0).

(7) Controller

The controller compares the A/D conversion results (the value of the ADCRH register) with the value of the power fail comparison threshold register (PFT) when A/D conversion ends or the power fail detection function is used. It generates INTAD only when the comparison conditions match.

(8) AV_{REF0} pin

This is the analog power supply pin/reference voltage input pin of the A/D converter. Always use the same potential as the V_{DD} pin even when not using the A/D converter.

The signals input to the ANI0 to ANI15 pins are converted into digital signals based on the voltage applied across AV_{REF0} and AV_{SS}.

(9) AV_{SS} pin

This is the ground potential pin of the A/D converter. Always use the same potential as the V_{SS} pin even when not using the A/D converter.

(10) A/D converter mode register (ADM)

This register sets the conversion time of the analog input to be converted to a digital signal and the conversion operation start/stop.

(11) Analog input channel specification register (ADS)

This register specifies the input port for the analog voltage to be converted to a digital signal.

(12) Power fail comparison mode register (PFM)

This register sets the power fail monitoring mode.

(13) Power fail comparison threshold register (PFT)

This register sets the threshold to be compared with the A/D conversion result register (ADCR).

13.3 Registers

The A/D converter is controlled by the following registers.

- A/D converter mode register (ADM)
- Analog input channel specification register (ADS)
- A/D conversion result register, A/D conversion result register H (ADCR, ADCRH)
- Power fail comparison mode register (PFM)
- Power fail comparison threshold register (PFT)

(1) A/D converter mode register (ADM)

This register sets the conversion time of the analog input signal to be converted into a digital signal as well as conversion start and stop.

The ADM register can be read/written in 8-bit or 1-bit units.

After reset, ADM is cleared to 00H.

After reset: 00H R/W Address: FFFFF200H

	<7>	6	5	4	3	2	1	<0>
ADM	ADCS	0	FR2	FR1	FR0	0	0	ADCS2

ADCS	Control of A/D conversion operation
0	Conversion operation stopped
1	Conversion operation enabled

FR2	FR1	FR0	Selection of conversion time			
			Conversion time[Note 1]	f_{XX}		
				20 MHz	16 MHz	10 MHz
0	0	0	288/f_{XX}	14.4 μs	18.0 μs	28.8 μs
0	0	1	240/f_{XX}	Setting prohibited	15.0 μs	24.0 μs
0	1	0	192/f_{XX}	Setting prohibited	Setting prohibited	19.2 μs
0	1	1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited
1	0	0	144/f_{XX}	Setting prohibited	Setting prohibited	14.4 μs
1	0	1	120/f_{XX}	Setting prohibited	Setting prohibited	Setting prohibited
1	1	0	96/f_{XX}	Setting prohibited	Setting prohibited	Setting prohibited
1	1	1	Setting prohibited	Setting prohibited	Setting prohibited	Setting prohibited

ADCS2	Control of reference voltage generator for boosting operation[Note 2]
0	Reference voltage generator operation stopped
1	Reference voltage generator operation stopped

Notes 1. Setting the conversion time (time actually required for A/D conversion) as follows is prohibited.

$AV_{REF0} \geq 4.0$ V: Less than 14 μs

$AV_{REF0} < 4.0$ V: Less than 17 μs

2. The operation of the reference voltage generator for boosting is controlled by the ADCS2 bit and it takes 14 μs after operation is started until it is stabilized. Therefore ADCS is set to 1 (A/D conversion is started) at least 14 μs after if ADCS2 was set to 1 (reference voltage generator for boosting is on), the first conversion result is valid.

Cautions 1. Always set bits 6, 2, and 1 to 0.

2. Changing bits FR0 to FR2 while ADCS = 1 is prohibited (write access to the ADM register is enabled and rewriting of bits FR0 to FR2 is prohibited).

3. When the main clock is stopped and the CPU is operating on the subclock, do not access the ADM register using an access method that causes a wait. For details, refer to 3.4.8 (2).

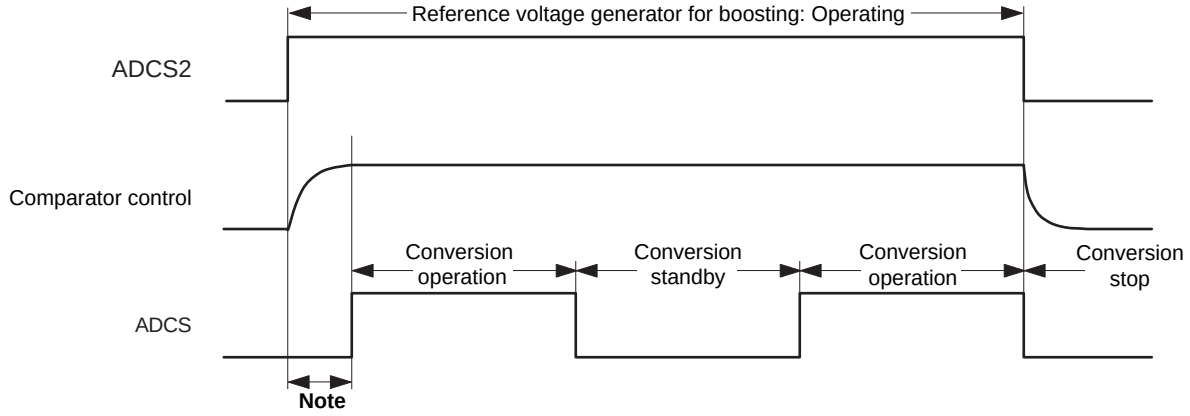
Remark f_{XX}: Main clock frequency

Table 13-2. Setting of ADCS Bit and ADCS2 Bit

ADCS	ADCS2	A/D Conversion Operation
0	0	Stopped status (DC power consumption path does not exist)
0	1	Conversion standby mode (only the reference voltage generator for boosting consumes power)
1	0	Conversion mode (reference voltage generator stops operation[Note])
1	1	Conversion mode (reference voltage generator is operating)

Note The data obtained by the first conversion must not be used.

Figure 13-2. Operation Sequence



Note 14 μs or more are required for the operation of the reference voltage generator for boosting between when the ADCS2 bit is set (1) and when the ADCS bit is set (1).

(2) Analog input channel specification register (ADS)

This register specifies the analog voltage input port for A/D conversion.

The ADS register can be read/written in 8-bit or 1-bit units.

After reset, ADS is cleared to 00H.

After reset: 00H R/W Address: FFFFF201H

	7	6	5	4	3	2	1	0
ADS	0	0	0	0	ADS3	ADS2	ADS1	ADS0

ADS3[Note 1]	ADS2	ADS1	ADS0	Specification of analog input channel
0	0	0	0	ANI0
0	0	0	1	ANI1
0	0	1	0	ANI2
0	0	1	1	ANI3
0	1	0	0	ANI4
0	1	0	1	ANI5
0	1	1	0	ANI6
0	1	1	1	ANI7
1	0	0	0	ANI8[Note 2]
1	0	0	1	ANI9[Note 2]
1	0	1	0	ANI10[Note 2]
1	0	1	1	ANI11[Note 2]
1	1	0	0	ANI12[Note 2]
1	1	0	1	ANI13[Note 2]
1	1	1	0	ANI14[Note 2]
1	1	1	1	ANI15[Note 2]

Notes 1. Because the V850ES/KF1 and V850ES/KG1 have 8 channels (ANI0 to ANI7), be sure to set the ADS3 bit to 0.

2. The ANI8 to ANI15 channels are available only in the V850ES/KJ1. In the V850ES/KF1 and V850ES/KG1, setting these channels is prohibited.

Caution When the main clock is stopped and the CPU is operating on the subclock, do not access the ADS register using an access method that causes a wait. For details, refer to 3.4.8 (2).

(3) A/D conversion result register, A/D conversion result register H (ADCR, ADCRH)

The ADCR and ADCRH registers store the A/D conversion results.

These registers are read-only in 16-bit or 8-bit units. However, specify the ADCR register for 16-bit access, and the ADCRH register for 8-bit access. In the ADCR register, the 10 bits of conversion results are read in the higher 10 bits and 0 is read in the lower 6 bits. In the ADCRH register, the higher 8 bits of the conversion results are read.

After reset, these registers are undefined.

After reset: Undefined R Address: FFFFF204H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ADCR	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	0	0	0	0	0	0

After reset: Undefined R Address: FFFFF205H

	7	6	5	4	3	2	1	0
ADCRH	AD9	AD8	AD7	AD6	AD5	AD4	AD3	AD2

Caution When the main clock is topped and the CPU is operating on the subclock, do not access the ADCR and ADCRH registers using an access method that causes a wait. For details, refer to 3.4.8 (2).

(4) Power fail comparison mode register (PFM)

This register sets the power fail monitoring mode.

PFM compares the value in the power fail comparison threshold register (PFT) with the value in A/D conversion result register H (ADCRH).

The PFM register can be read/written in 8-bit or 1-bit units.

After reset, this register is cleared to 00H.

After reset: 00H R/W Address: FFFFF202H

	<7>	6	5	4	3	2	1	0
PFM	PFEN	PFCM	0	0	0	0	0	0

PFEN	Selection of power fail comparison enable/disable
0	Power fail comparison disabled
1	Power fail comparison disabled

PFCM	Selection of power fail comparison mode
0	Interrupt request signal (INTAD) generated when ADCR ≥ PFT
1	Interrupt request signal (INTAD) generated when ADCR < PFT

Caution When the main clock is stopped and the CPU is operating on the subclock, do not access the PFM register using an access method that causes a wait. For details, refer to 3.4.8 (2).

(5) Power fail comparison threshold register (PFT)

The PFT register sets the comparison value in the power fail comparison mode.

The 8-bit data set in the PFT register is compared with the higher 8 bits (ADCRH) of the A/D conversion result register.

PFT can be read/written in 8-bit units.

After reset, PFT is cleared to 00H.

After reset: 00H R/W Address: FFFFF203H

	7	6	5	4	3	2	1	0
PFT								

Caution When the main clock is stopped and the CPU is operating on the subclock, do not access the PFT register using an access method that causes a wait. For details, refer to 3.4.8 (2).

13.4 Relationship Between Analog Input Voltage and A/D Conversion Results

The following shows the relationship between the analog input voltage input to the analog input pins (ANI0 to ANI15) and A/D conversion results (A/D conversion result register (ADCR)).

$$SAR = INT\left(\frac{V_{IN}}{AV_{REF0}} \times 1024 + 0.5\right)$$

$$ADCR^{Note} = SAR \times 64$$

Or,

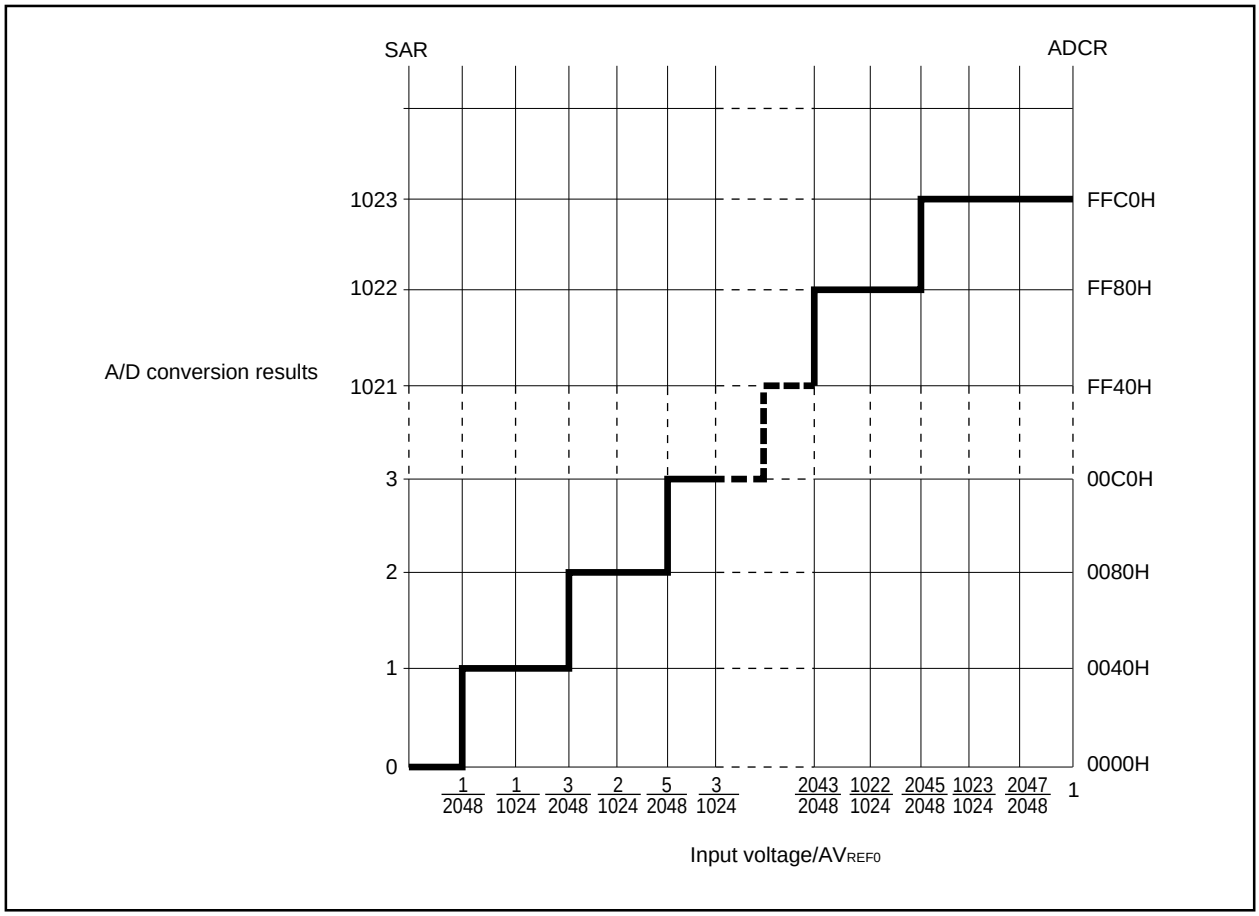
$$(SAR = 0.5) \times \frac{AV_{REF0}}{1024} < V_{IN} < (SAR + 0.5) \times \frac{AV_{REF0}}{1024}$$

INT ( ): Function that returns the integer part of the value in parenthes
V_{IN}: Analog input voltage
AV_{REF0}: Voltage of AV_{REF0} pin
ADCR: Value in the A/D conversion result register (ADCR)

Note The lower 6 bits of ADCR are fixed to 0.

The following shows the relationship between the analog input voltage and A/D conversion results.

Figure 13-3. Relationship Between Analog Input Voltage and A/D Conversion Results



13.5 Operation

★ 13.5.1 Basic operation

<1> Select the channel whose analog signal is to be converted into a digital signal using the analog input channel specification register (ADS).

<2> Set (1) the ADCS2 bit and wait 14 μs or longer.

<3> Set the ADCS bit to 1 to start conversion.
(Steps <4> to <10> are executed by hardware.)

<4> The sample & hold circuit samples the voltage input to the selected analog input channel.

<5> After sampling for a specific time, the sample & hold circuit enters the hold status and holds the input analog voltage until it has been converted into a digital signal.

<6> Set bit 9 of the successive approximation register (SAR). The tap selector sets the voltage tap of the series resistor string to (1/2) $\times$ AV_{REF0}.

<7> The voltage comparator compares the voltage difference between the voltage tap of the series resistor string and the analog input voltage. If the analog input voltage is greater than (1/2) $\times$ AV_{REF0}, the MSB of the SAR remains set. If the analog input voltage is less than (1/2) $\times$ AV_{REF0}, the MSB is reset.

<8> Next, bit 8 of the SAR is automatically set and the next comparison starts. Depending on the value of bit 9 to which the result of the preceding comparison has been set, the voltage tap of the series resistor string is selected as follows.

- Bit 9 = 1: (3/4) $\times$ AV_{REF0}
- Bit 9 = 0: (1/4) $\times$ AV_{REF0}

The analog input voltage is compared with one of these voltage taps and bit 8 of the SAR is manipulated as follows depending on the result of the comparison.

Analog input voltage $\geq$ voltage tap: Bit 8 = 1
Analog input voltage $\leq$ voltage tap: Bit 8 = 0

<9> The above steps are repeated until bit 0 of the SAR has been manipulated.

<10> When comparison of all 10 bits of the SAR has been completed, the valid digital value remains in the SAR, and the value of the SAR is transferred and latched to the A/D conversion result register (ADCR).
At the same time, an A/D conversion end interrupt request (INTAD) is generated.

<11> Repeat steps <4> to <10> until the ADCS bit is cleared to 0.
For another A/D conversion, start at <3>. However, when operating the A/D converter with the ADCS2 bit cleared to 0, start at <2>.

13.5.2 Conversion operation

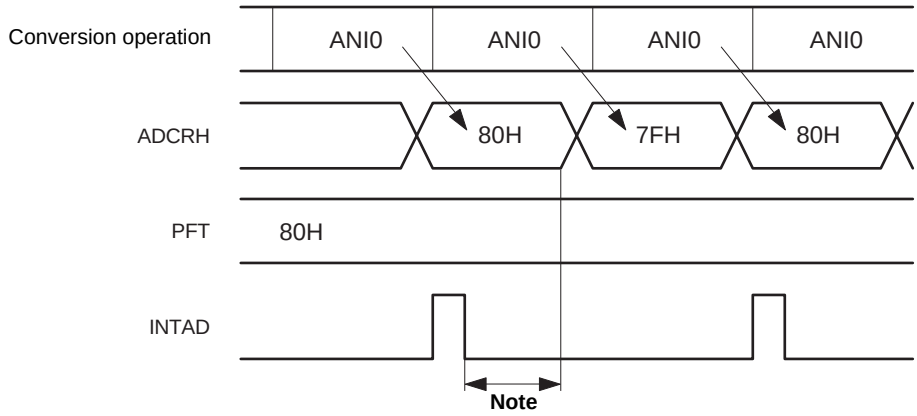
- Setting ADCS of the A/D converter mode register (ADM) to 1 starts conversion of the signal input to the channel specified by the analog input channel specification register (ADS). Upon completion of the conversion, the conversion result is stored in the ADCR register and a new conversion starts.
- If ADM, ADS, the power fail comparison threshold register (PFT), or the power fail comparison mode register (PFM) is written during conversion, conversion is interrupted and the conversion operation starts again from the beginning.
- If ADCS is set to 0 during conversion, conversion is interrupted and the conversion operation is stopped.
- For whether or not the conversion end interrupt request signal (INTAD) is generated, refer to **13.5.3**.

★ **13.5.3 Power fail monitoring function**

The conversion end interrupt request signal (INTAD) can be controlled as follows using the PFM and PFT registers.

- If PFEN = 0, INTAD is generated each time conversion ends.
- If PFEN = 1 and PFCM = 0, the conversion result and the value of the PFT register are compared when conversion ends, and INTAD is output only if ADCRH ≥ PFT.
- If PFEN and PFCM = 1, the conversion result and the value of the PFT register are compared when conversion ends and INTAD is output only if ADCRH < PFT.
- Because, when PFEN = 1, the conversion result is overwritten after INTAD has been output, unless the conversion result is read by the time the next conversion ends, in some cases it may appear as if the actual operation differs from the operation described above (refer to **Figure 13-4**).

Figure 13-4. Power Fail Monitoring Function (PFCM = 0)



Note If reading is not performed during this interval, the conversion result changes to the next conversion result.

The following describes how to set registers.

- When using the A/D converter for A/D conversion
  <1> Set (1) the ADCS2 bit of the A/D converter mode register (ADM).
  <2> Select the channel and conversion time by setting the ADS2 to ADS0 bits of the analog input channel specification register (ADS) and the FR2 to FR0 bits of the ADM register.
  <3> An interrupt request signal (INTAD) is generated.
  <4> Set (1) the ADCS bit of the ADM register.
  <5> Transfer the A/D conversion data to the A/D conversion result register (ADCR).

<Changing the channel>

  <6> Change the channel by setting the ADS2 to ADS0 bits of the ADS register.
  <7> Transfer the A/D conversion data to the A/D conversion result register (ADCR).
  <8> An interrupt request signal (INTAD) is generated.

<Ending A/D conversion>

  <9> Clear (0) the ADCS bit.
  <10> Clear (0) the ADCS2 bit.

Cautions 1. The time taken from <1> to <3> must be 14 μs or longer.
2. Steps <1> and <2> may be reversed.
3. Step <1> may be omitted. However, if omitted, do not use the first conversion result after <3>.
4. The time taken from <4> to <7> is different from the conversion time set by the FR2 to FR0 bits of the ADM register.
The time taken for <6> and <7> is the conversion time set by the FR2 to FR0 bits.

- When using the A/D converter for the power fail function
  <1> Set (1) the PFEN bit of the power fail comparison mode register (PFM).
  <2> Set the power fail comparison conditions by using the PFCM bit of the PFM register.
  <3> Set (1) the ADCS2 bit of the A/D converter mode register (ADM).
  <4> Select the channel and conversion time by setting the ADS2 to ADS0 bits of the analog input channel specification register (ADS) and the FR2 to FR0 bits of the ADM register.
  <5> Set the threshold value in the power fail comparison threshold register (PFT).
  <6> Set (1) the ADCS bit of the ADM register.
  <7> Transfer the A/D conversion data to the A/D conversion result register (ADCR).
  <8> Compare the ADCR register with the PFT register. An interrupt request signal (INTAD) is generated when the conditions match.

<Changing the channel>

  <9> Change the channel by setting the ADS2 to ADS0 bits of the ADS register.
  <10> Transfer the A/D conversion data to the A/D conversion result register (ADCR).
  <11> The ADCR register is compared with the power fail comparison threshold register (PFT). When the conditions match, an interrupt request signal (INTAD) is generated.

<Ending A/D conversion>

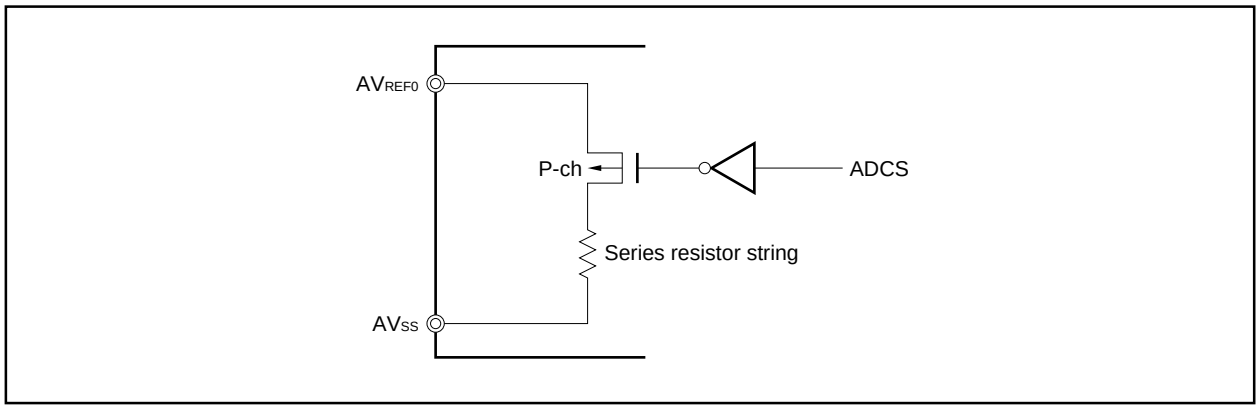
  <12> Clear (0) the ADCS bit.
  <13> Clear (0) the ADCS2 bit.

★ 13.6 Cautions on Use

(1) Power consumption in standby mode

The operation of the A/D converter stops in the standby mode. At this time, the power consumption can be reduced by stopping the conversion operation (the ADCS bit of the A/D converter mode register (ADM) = 0). Figure 13-5 shows an example of how to reduce the power consumption in the standby mode.

Figure 13-5. Example of How to Reduce Power Consumption in Standby Mode



(2) Input range of ANI0 to ANI15

Use the A/D converter with the ANI0 to ANI15 input voltages within the specified range. If a voltage of AV_{REF0} or higher or AV_{SS} or lower (even if within the absolute maximum ratings) is input to these pins, the conversion value of the channel is undefined. Also, this may affect the conversion value of other channels.

(3) Conflicting operations

(a) Conflict between writing to the A/D conversion result register (ADCR) and reading from ADM upon the end of conversion

Reading the ADM register takes precedence. After the register has been read, a new conversion result is written to the ADCR register.

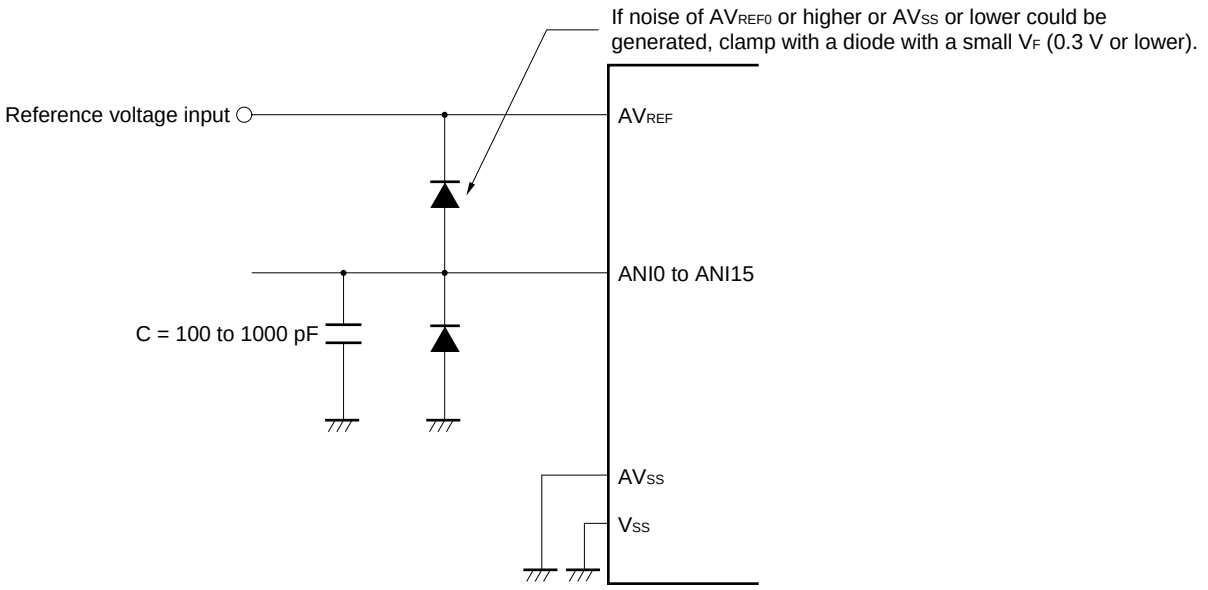
(b) Conflict between writing to ADCR and writing to the A/D converter mode register (ADM) or writing to the analog input channel specification register (ADS) upon the end of conversion

Writing to the ADM register or ADS register takes precedence. The ADCR register is not written, and nether is the conversion end interrupt signal (INTAD) generated.

(4) Measures against noise

To keep a resolution of 10 bits, be aware of noise on the AV_{REF} and ANI0 to ANI15 pins. The higher the output impedance of the analog input source, the greater the effect of noise. Therefore, it is recommended to connect external capacitors as shown in Figure 13-6 to reduce noise.

Figure 13-6. Handling of Analog Input Pins



Remark n = 0 to 15
m = 0 to 15

(5) ANI0/P70 to ANI15/P715

The analog input pins (ANI0 to ANI15) function alternately as input port pins (P70 to P715).

When performing A/D conversion by selecting any of the ANI0 to ANI15, do not execute an input instruction to port 7 during conversion. This may decrease the conversion resolution.

If digital pulses are applied to the pin adjacent to the pin subject to A/D conversion, the value of the A/D conversion may differ from the expected value because of coupling noise. Therefore, do not apply pulses to the pin adjacent to the pin subject to A/D conversion.

(6) Input impedance of AV_{REF0} pin

A series resistor string of tens of kΩ is connected between the AV_{REF0} pin and AV_{SS} pin.

Therefore, if the output impedance of the reference voltage source is high, this will result in a series connection to the series resistor string between the AV_{REF0} pin and AV_{SS} pin, resulting in a large reference voltage error.

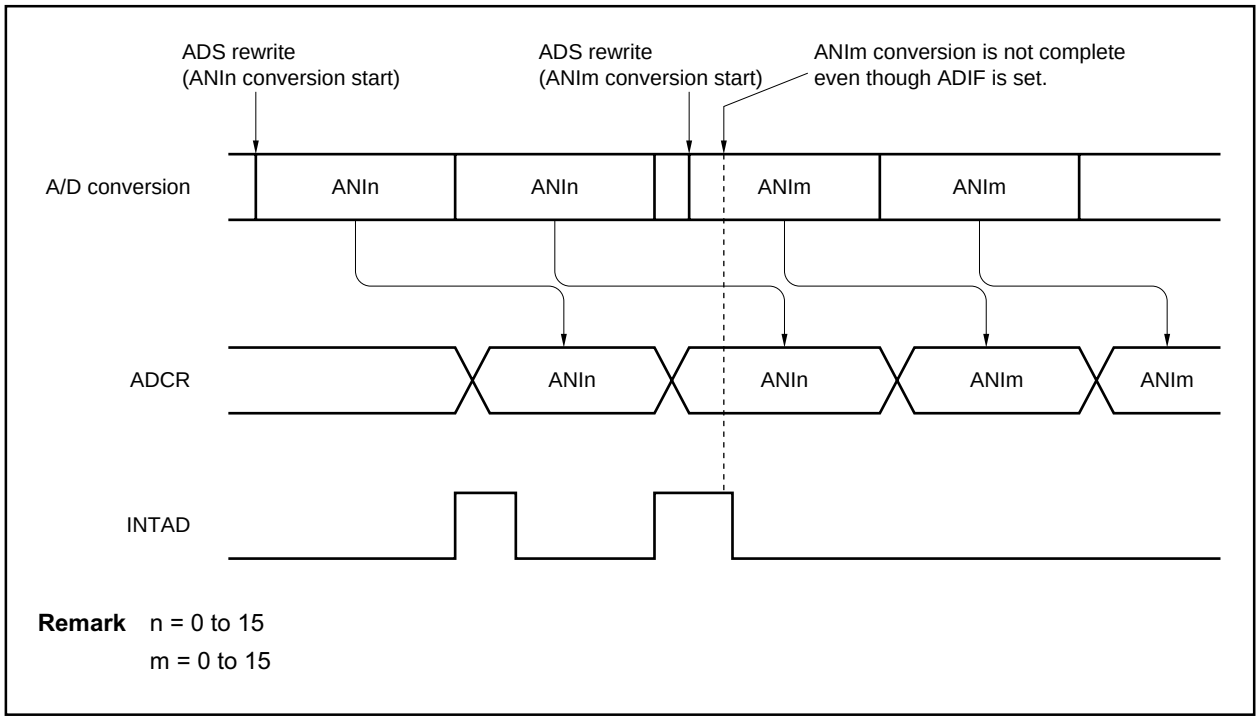
(7) Interrupt request flag (ADIC.ADIF bit)

Even when the ADS register is changed, the ADIF bit is not cleared (0).

Therefore, if the analog input pin is changed during A/D conversion, the ADIF bit may be set (1) because A/D conversion of the previous analog input pin ends immediately before the ADS register is rewritten. In a such case, note that if the ADIF bit is read immediately after the ADS register has been rewritten, the ADIF bit is set (1) even though A/D conversion of the analog input pin after the change has not been completed.

When stopping A/D conversion once and resuming it, clear the ADIF bit (0) before resuming A/D conversion.

Figure 13-7. A/D Conversion End Interrupt Request Occurrence Timing



Remark n = 0 to 15
m = 0 to 15

(8) Conversion results immediately after A/D conversion start

If the ADCS bit is set to 1 within 14 μs after the ADCS2 bit has been set to 1, or if the ADCS bit is set to 1 with the ADCS2 bit cleared to 0, the converted value immediately after the A/D conversion operation has started may not satisfy the rating. Take appropriate measures such as polling the A/D conversion end interrupt request (INTAD) and discarding the first conversion result.

(9) Reading A/D conversion result register (ADCR)

When the A/D converter mode register (ADM) or analog input channel specification register (ADS) has been written, the contents of the ADCR register may become undefined. When the conversion operation is complete, read the conversion results before writing to the ADM or ADS register. A correct conversion result may not be able to be read at a timing other than the above.

When the CPU is operating on the subclock and main clock oscillation (fx) is stopped, do not read the ADCR register.

(10) A/D converter sampling time and A/D conversion start delay time

The A/D converter sampling time differs depending on the set value of the A/D converter mode register (ADM). A delay time exists until actual sampling is started after A/D converter operation is enabled.

When using a set in which the A/D conversion time must be strictly observed, care is required for the contents shown in Figure 13-8 and Table 13-3.

Figure 13-8. Timing of A/D Converter Sampling and A/D Conversion Start Delay

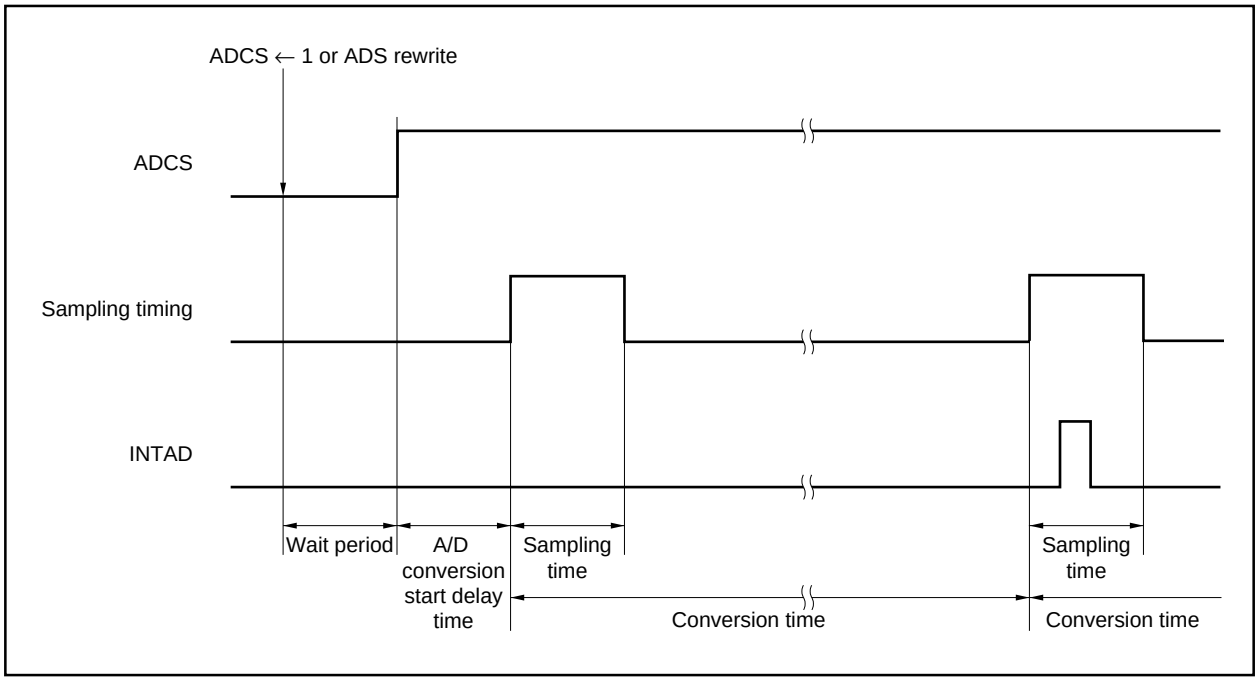


Table 13-3. A/D Converter Sampling Time and A/D Conversion Start Delay Time (ADM Set Value)

FR2	FR1	FR0	Conversion Time	Sampling Time	A/D Conversion Start Delay Time[Note]	
					MIN.	MAX.
0	0	0	288/fxx	40/fxx	32/fxx	36/fxx
0	0	1	240/fxx	32/fxx	28/fxx	32/fxx
0	1	0	192/fxx	24/fxx	24/fxx	28/fxx
1	0	0	144/fxx	20/fxx	16/fxx	18/fxx
1	0	1	120/fxx	16/fxx	14/fxx	16/fxx
1	1	0	96/fxx	12/fxx	12/fxx	14/fxx
Other than above			Setting prohibited	–	–	–

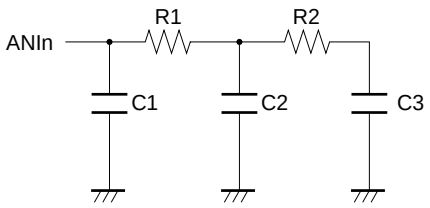
Note The A/D conversion start delay time is the time after the wait period. For the wait function, refer to **3.4.8 (2) Access to special on-chip peripheral I/O register**.

Remark fxx: Main clock frequency

(11) Internal equivalent circuit

The following shows the equivalent circuit of the analog input block.

Figure 13-9. Internal Equivalent Circuit of ANIn Pin



AV_{REF0}	R1	R2	C1	C2	C3
1.8 V	75 kΩ	30 kΩ	8 pF	4 pF	2 pF
2.7 V	12 kΩ	8 kΩ	8 pF	3 pF	2 pF
4.5 V	4 kΩ	2.7 kΩ	8 pF	1.4 pF	2 pF

Remark The above values are reference values.

13.7 How to Read A/D Converter Characteristics Table

Here, special terms unique to the A/D converter are explained.

(1) Resolution

This is the minimum analog input voltage that can be identified. That is, the percentage of the analog input voltage per bit of digital output is called 1 LSB (Least Significant Bit). The percentage of 1 LSB with respect to the full scale is expressed by %FSR (Full Scale Range). %FSR indicates the ratio of analog input voltage that can be converted as a percentage, and is always represented by the following formula regardless of the resolution.

1%FSR = (Max. value of analog input voltage that can be converted − Min. value of analog input voltage that can be converted)/100
= (AV_{REF0} – 0)/100
= AV_{REF0}/100

1 LSB is as follows when the resolution is 10 bits.

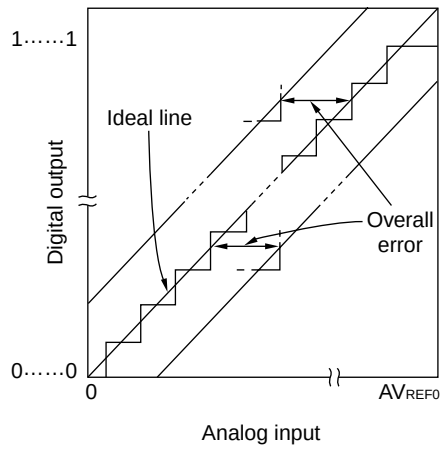
1 LSB = $1/2^{10}$ = 1/1024
= 0.098%FSR

Accuracy has no relation to resolution, but is determined by overall error.

(2) Overall error

This shows the maximum error value between the actual measured value and the theoretical value.
Zero-scale error, full-scale error, linearity error and errors that are combinations of these express the overall error.
Note that the quantization error is not included in the overall error in the characteristics table.

Figure 13-10. Overall Error

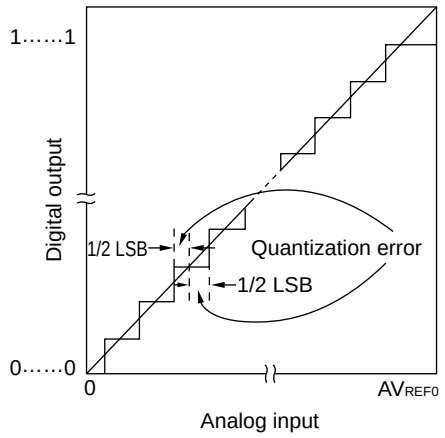


(3) Quantization error

When analog values are converted to digital values, a ±1/2 LSB error naturally occurs. In an A/D converter, an analog input voltage in a range of ±1/2 LSB is converted to the same digital code, so a quantization error cannot be avoided.

Note that the quantization error is not included in the overall error, zero-scale error, full-scale error, integral linearity error, and differential linearity error in the characteristics table.

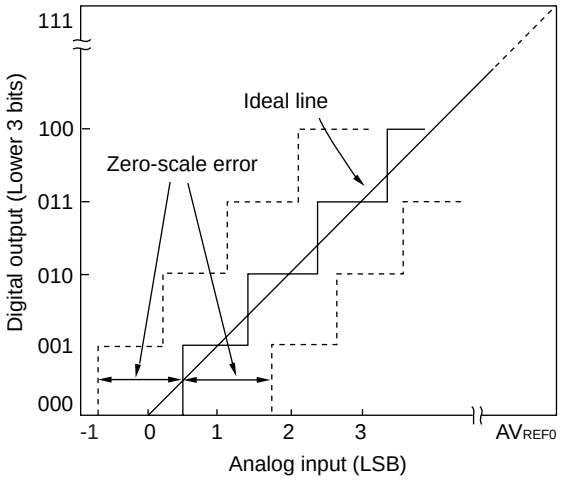
Figure 13-11. Quantization Error



(4) Zero-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (1/2 LSB) when the digital output changes from 0……000 to 0……001.

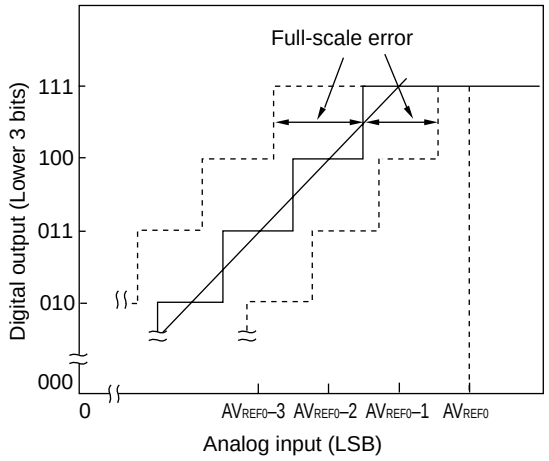
Figure 13-12. Zero-Scale Error



(5) Full-scale error

This shows the difference between the actual measurement value of the analog input voltage and the theoretical value (3/2 LSB) when the digital output changes from 1……110 to 1……111.

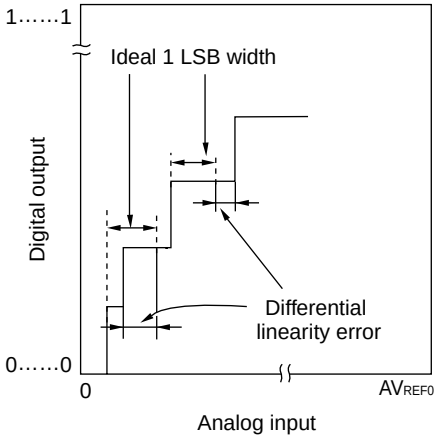
Figure 13-13. Full-Scale Error



(6) Differential linearity error

While the ideal width of code output is 1 LSB, this indicates the difference between the actual measurement value and the ideal value.

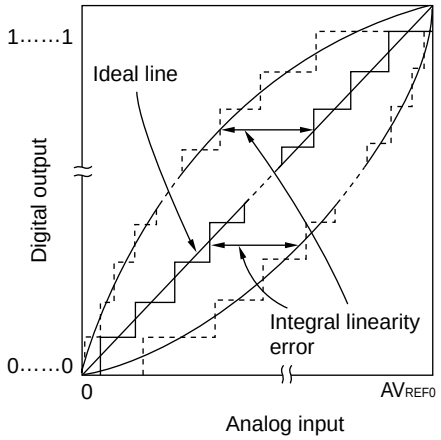
Figure 13-14. Differential Linearity Error



(7) Integral linearity error

This shows the degree to which the conversion characteristics deviate from the ideal linear relationship. It expresses the maximum value of the difference between the actual measurement value and the ideal straight line when the zero-scale error and full-scale error are 0.

Figure 13-15. Integral Linearity Error



(8) Conversion time

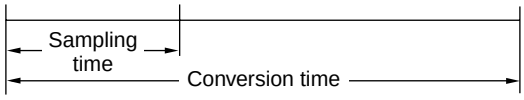
This expresses the time from when the analog input voltage was applied to the time when the digital output was obtained.

The sampling time is included in the conversion time in the characteristics table.

(9) Sampling time

This is the time the analog switch is turned on for the analog voltage to be sampled by the sample & hold circuit.

Figure 13-16. Sampling Time



CHAPTER 14 D/A CONVERTER

14.1 Functions

The V850ES/KG1 and V850ES/KJ1 incorporate two D/A converter channels (DAC0, DAC1).
The D/A converter has the following functions.

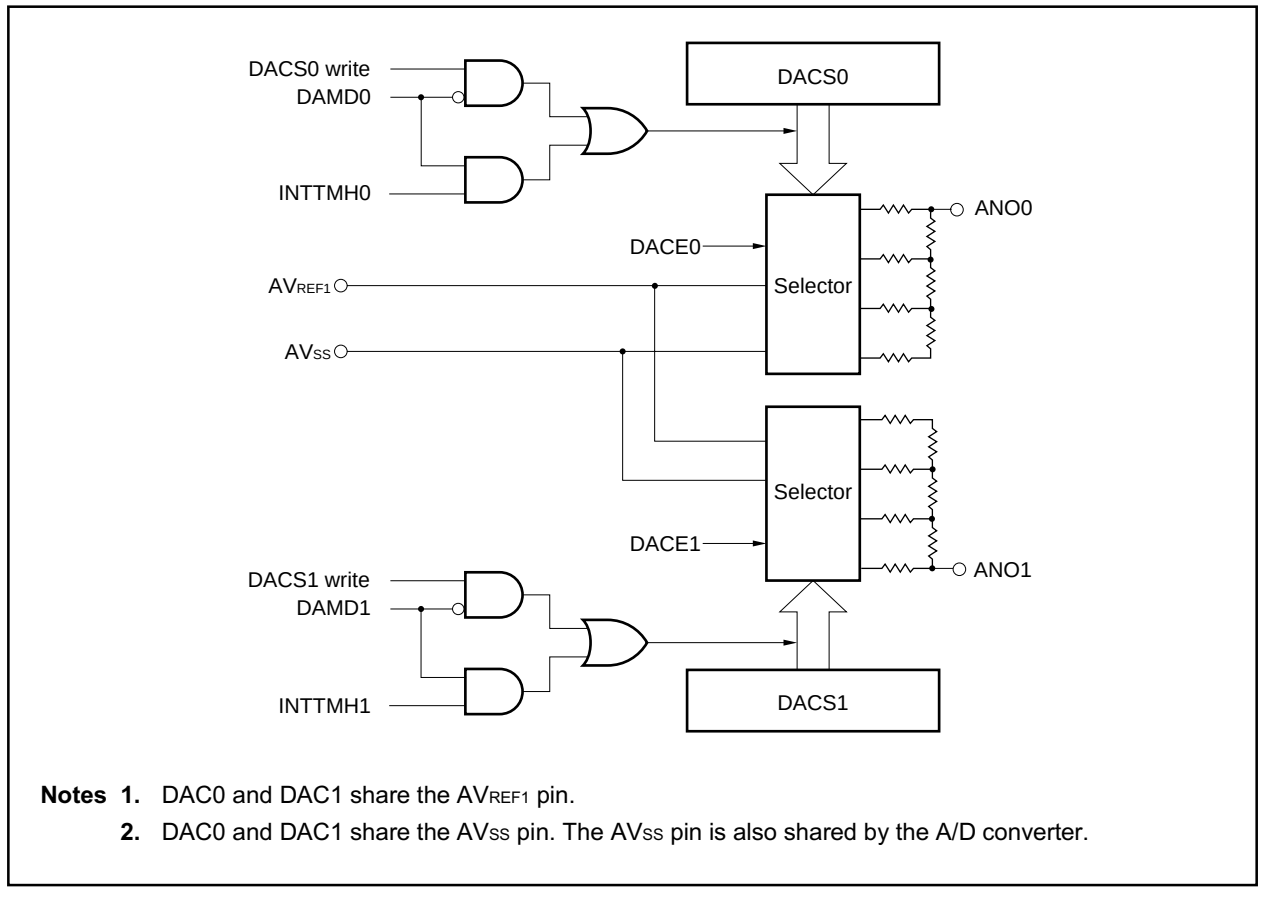
- 8-bit resolution × 2 channels
- R-2R ladder string method
- Conversion time: 20 μs (MAX.) (AV_{REF1} = 2.7 to 5.5 V)
- Analog output voltage: AV_{REF1} × m/256 (m = 0 to 255; value set to DACSn register)
- Operation modes: Normal mode, real-time output mode

Caution The V850ES/KF1 does not have a D/A converter.

Remark n = 0, 1

The D/A converter configuration is shown below.

Figure 14-1. Block Diagram of D/A Converter



Notes 1. DAC0 and DAC1 share the AV_{REF1} pin.

2. DAC0 and DAC1 share the AV_{SS} pin. The AV_{SS} pin is also shared by the A/D converter.

14.2 Configuration

The D/A converter consists of the following hardware.

Table 14-1. Configuration of D/A Converter

Item	Configuration
Control register	D/A converter mode register (DAM) D/A conversion value setting registers 0 and 1 (DACS0, DACS1)

14.3 Registers

The registers that control the D/A converter are as follows.

- D/A converter mode register (DAM)
- D/A conversion value setting registers 0 and 1 (DACS0, DACS1)

(1) D/A converter mode register (DAM)

This register controls the operation of the D/A converter.

The DAM is set by an 8-bit or 1-bit memory manipulation instruction.

After reset, DAM is cleared to 00H.

After reset: 00H R/W Address: FFFFF284H

	7	6	5	4	3	<2>	1	<0>
DAM	0	0	0	0	DAMD1	DACE1	DAMD0	DACE0

DAMDn	Selection of D/A converter operation mode (n = 0, 1)
0	Normal mode
1	Real-time output mode[Note]

DACEn	D/A converter operation enable/disable control (n = 0, 1)
0	Disable operation
1	Enable operation

Note The output trigger in the real-time output mode (DAMDn bit = 1) is as follows.

- When n = 0: INTTMH0 signal (Refer to **CHAPTER 9 8-BIT TIMERS H0 AND H1**)
- When n = 1: INTTMH1 signal (Refer to **CHAPTER 9 8-BIT TIMERS H0 AND H1**)

(2) D/A conversion value setting registers 0 and 1 (DACS0, DACS1)

These registers set the analog voltage value output to the ANO0 and ANO1 pins.

These register are set by an 8-bit memory manipulation instruction.

After reset, DACS0 and DACS1 are cleared to 00H.

After reset: 00H R/W Address: FFFFF280H

	7	6	5	4	3	2	1	0
DACS0	DA07	DA06	DA05	DA04	DA03	DA02	DA01	DA00

After reset: 00H R/W Address: FFFFF282H

	7	6	5	4	3	2	1	0
DACS1	DA17	DA16	DA15	DA14	DA13	DA12	DA11	DA10

Caution In the real-time output mode (DAMDn bit = 1), set the DACS0 and DACS1 registers before the INTTMH0/INTTMH1 signals are generated. D/A conversion starts when the INTTMH0/INTTMH1 signals are generated.

14.4 Operation

14.4.1 Operation in normal mode

D/A conversion is performed using a write operation to the D/A conversion value setting register (DACSn) as the trigger.

The setting method is described below.

<1> Set the DAMDn bit of the D/A converter mode register (DAM) to 0 (normal mode).
<2> Set the analog voltage value to be output to the ANOn pin to the DACSn register.
Steps <1> and <2> above constitute the initial settings.
<3> Set the DACEn bit of the DAM register to 1 (D/A conversion enable).
D/A conversion starts when this setting is performed.
<4> To perform subsequent D/A conversions, write to the DACSn register.
The previous D/A conversion result is held until the next D/A conversion is performed.

Remark For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

14.4.2 Operation in real-time output mode

D/A conversion is performed using the interrupt request signals (INTTMH0, INTTMH1) of 8-bit timers H0 and H1 (TMH0, TMH1) as the trigger.

The setting method is described below.

<1> Set the DAMDn bit of the DAM register to 1 (real-time output mode).
<2> Set the analog voltage value to be output to the ANOn pin to the DACSn register.
<3> Set the DACEn bit of the DAM register to 1 (D/A conversion enable).
Steps <1> to <3> above constitute the initial settings.
<4> Operate 8-bit timers H0 and H1 (TMH0, TMH1).
<5> D/A conversion starts when the INTTMH0 and INTTMH1 signals are generated.
<6> After that, the value set in DACSn is output every time the INTTMH0 are INTTMH1 signals are generated.

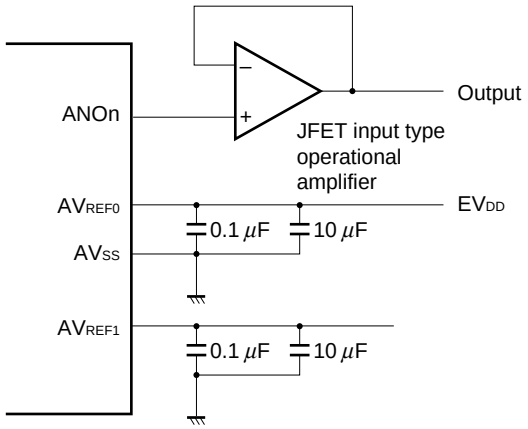
Remarks 1. The output values of the ANO0 and ANO1 pins up to <5> above are undefined.
2. For the output values of the ANIO0 and ANO1 pins in the IDLE, HALT, and STOP modes, refer to **CHAPTER 21 STANDBY FUNCTION**.

14.4.3 Cautions

Observe the following cautions when using the D/A converter of the V850ES/KG1 and V850ES/KJ1.

- When using the D/A converter, set the port pins to the input mode (PM1n bit = 1; n = 0, 1)
- When using the D/A converter, reading of the port is prohibited.
- When using the D/A converter, use both P10 and P11 as D/A outputs.
  Using one of the port 1 for D/A output and the other as a port is prohibited.
- In the real-time output mode, do not change the setting value of the DACSn register while the trigger signal is output.
- Make sure that $AV_{REF1} \leq V_{DD}$ and AV_{REF1} = 2.7 V to 5.5 V. The operation is not guaranteed if ranges other than the above are used.
- ★ Because the output impedance of the D/A converter is high, a current cannot be supplied from the ANOn pin (n = 0, 1). When connecting a resistor of 2 MΩ or lower, take appropriate measures such as inserting a JFET input type operational amplifier between the resistor and the ANOn pin.

Figure 14-2. Example of External Pin Connection



★ **Caution The figure shown here is only reference. Use it after fully evaluating.**

CHAPTER 15 ASYNCHRONOUS SERIAL INTERFACE (UART)

The number of asynchronous serial interface (UART) channels incorporated differs as follows depending on the product.

Product Name	V850ES/KF1	V850ES/KG1	V850ES/KJ1
Number of channels	2 channels (UART0, UART1)		3 channels (UART0 to UART2)

15.1 Selecting UART2 or I²C1 Mode

UART2 and I²C1 of the V850ES/KJ1 share pins, and therefore these interfaces cannot be used at the same time. Select UART2 or I²C1 in advance by using the port 8 mode control register (PMC8) and port 8 function control register (PFC8) (refer to **4.3.8 Port 8**).

Caution UART2 or I²C1 transmission/reception operations are not guaranteed if the mode is changed during transmission or reception. Be sure to disable the operation of the unit that is not used.

Figure 15-1. Selecting Mode of UART2 or I²C1

After reset: 00H R/W Address: FFFFF450H

	7	6	5	4	3	2	1	0
PMC8	0	0	0	0	0	0	PMC81	PMC80

After reset: 00H R/W Address: FFFFF470H

	7	6	5	4	3	2	1	0
PFC8	0	0	0	0	0	0	PFC81	PFC80

PFC8n	PMC8n	Operation mode
0	0	Port I/O mode
0	1	UART2 mode
1	0	Port I/O mode
1	1	I²C1 mode

Remark n = 0, 1

15.2 Features

- Maximum transfer speed: 312.5 kbps
- Full-duplex communications
  On-chip reception buffer register n (RXBn)
  On-chip transmission buffer register n (TXBn)
- Two-pin configuration[Note]
  TXDn: Transmit data output pin
  RXDn: Receive data input pin
- Reception error detection functions
  - Parity error
  - Framing error
  - Overrun error
- Interrupt sources: 3 types
  - Reception error interrupt (INTSREn): Interrupt is generated according to the logical OR of the three types of reception errors
  - Reception completion interrupt (INTSRn): Interrupt is generated when receive data is transferred from the shift register to reception buffer register n after serial transfer is completed during a reception enabled state
  - Transmission completion interrupt (INTSTn): Interrupt is generated when the serial transmission of transmit data (8 or 7 bits) from the shift register is completed
- Character length: 7 or 8 bits
- Parity functions: Odd, even, 0, or none
- Transmission stop bits: 1 or 2 bits
- On-chip dedicated baud rate generator

Note The ASCK0 pin is available only for UART0.

15.3 Configuration

Table 15-1. Configuration of UART

Item	Configuration
Registers	Receive buffer register n (RXBn) Transmit buffer register n (TXBn) Receive shift register Transmit shift register Asynchronous serial interface mode register n (ASIMM) Asynchronous serial interface status register n (ASISn) Asynchronous serial interface transmit status register n (ASIFn)
Other	Reception control parity check Addition of transmission control parity

Figure 15-2 shows the configuration of asynchronous serial interface n (UARTn).

(1) Asynchronous serial interface mode register n (ASIMn)

The ASIMn register is an 8-bit register for specifying the operation of the asynchronous serial interface.

(2) Asynchronous serial interface status register n (ASISn)

The ASISn register consists of a set of flags that indicate the error contents when a reception error occurs. The various reception error flags are set (1) when a reception error occurs and are reset (0) when the ASISn register is read.

(3) Asynchronous serial interface transmit status register n (ASIFn)

The ASIFn register is an 8-bit register that indicates the status when a transmit operation is performed.

This register consists of a transmit buffer data flag, which indicates the hold status of TXBn data, and the transmit shift register data flag, which indicates whether transmission is in progress.

(4) Reception control parity check

The receive operation is controlled according to the contents set in the ASIMn register. A check for parity errors is also performed during a receive operation, and if an error is detected, a value corresponding to the error contents is set in the ASISn register.

(5) Receive shift register

This is a shift register that converts the serial data that was input to the RXDn pin to parallel data. One byte of data is received, and if a stop bit is detected, the receive data is transferred to the receive buffer register n (RXBn).

This register cannot be directly manipulated.

(6) Receive buffer register n (RXBn)

RXBn is an 8-bit buffer register for holding receive data. When 7 characters are received, 0 is stored in the MSB.

During a reception enabled state, receive data is transferred from the receive shift register to the RXBn, synchronized with the end of the shift-in processing of one frame.

Also, the reception completion interrupt request (INTSRn) is generated by the transfer of data to the RXBn.

(7) Transmit shift register

This is a shift register that converts the parallel data that was transferred from the transmit buffer register n (TXBn) to serial data.

When one byte of data is transferred from the TXBn, the shift register data is output from the TXDn pin.

The transmission completion interrupt request (INTSTn) is generated synchronized with the completion of transmission of one frame.

This register cannot be directly manipulated.

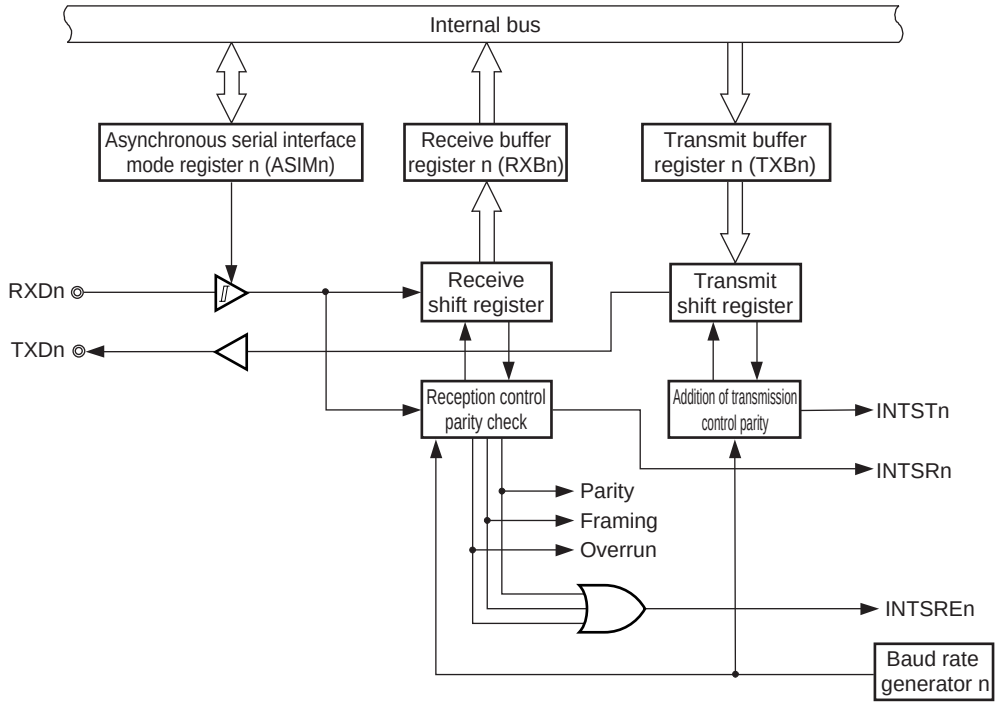
(8) Transmit buffer register n (TXBn)

TXBn is an 8-bit buffer for transmit data. A transmit operation is started by writing transmit data to TXBn.

(9) Addition of transmission control parity

A transmit operation is controlled by adding a start bit, parity bit, or stop bit to the data that is written to the TXBn register, according to the contents that were set in the ASIMn register.

Figure 15-2. Block Diagram of Asynchronous Serial Interface n



Remark For the configuration of the baud rate generator, refer to Figure 15-13.

15.4 Registers

(1) Asynchronous serial interface mode register n (ASIMn)

The ASIMn register is an 8-bit register that controls the UARTn transfer operation.

This register can be read/written in 8-bit or 1-bit units.

After reset, ASIMn is set to 01H.

Cautions 1. When using UARTn, be sure to set the external pins related to UARTn functions to the control made before setting clock select register n (CKSRn) and the baud rate generator control register n (BRGCn), and then set the UARTEn bit to 1. Then set the other bits.

★ **2. Set the UARTEn and RXEn bits to 1 while a high level is input to the RXDn pin. If these bits are set to 1 while a low level is input to the RXDn pin, reception will be started.**

(1/2)

After reset: 01H R/W Address: FFFFFA00H, FFFFFA10H, FFFFFA20H

	<7>	<6>	<5>	4	3	2	1	0
ASIMn	UARTEn	TXEn	RXEn	PSn1	PSn0	CLn	SLn	ISRMn

UARTEn	Control of operating clock
0	Stop clock supply to UARTn.
1	Supply clock to UARTn.

- If UARTEn = 0, UARTn is asynchronously reset[Note].
- If UARTEn = 0, UARTn is reset. To operate UARTn, first set UARTEn to 1.
- If the UARTEn bit is changed from 1 to 0, all the registers of UARTn are initialized. To set UARTEn to 1 again, be sure to re-set the registers of UARTn.

The output of the TXDn pin goes high when transmission is disabled, regardless of the setting of the UARTEn bit.

TXEn	Transmission enable/disable
0	Disable transmission
1	Enable transmission

- Set the TXEn bit to 1 after setting the UARTEn bit to 1 at startup. Set the UARTEn bit to 0 after setting the TXEn bit to 0 to stop.
- To initialize the transmission unit, clear (0) the TXEn bit, and after letting 2 Clock cycles (base clock) elapse, set (1) the TXEn bit again. If the TXEn bit is not set again, initialization may not be successful. (For details about the base clock, refer to **15.7.1 (1) Base clock (Clock)**.)

Note The ASISn, ASIFn, and RXBn registers are reset.

(2/2)

RXEn	Reception enable/disable
0	Disable reception[Note]
1	Enable reception

- Set the RXEn bit to 1 after setting the UARTEn bit to 1 at startup. Set the UARTEn bit to 0 after setting the RXEn bit to 0 to stop.
- To initialize the reception unit status, clear (0) the RXEn bit, and after letting 2 Clock cycles (base clock) elapse, set (1) the RXEn bit again. If the RXEn bit is not set again, initialization may not be successful. (For details about the base clock, refer to **15.7.1 (1) Base clock (Clock)**.)

PSn1	PSn0	Transmit operation	Receive operation
0	0	Don't output parity bit	Receive with no parity
0	1	Output 0 parity	Receive as 0 parity
1	0	Output odd parity	Judge as odd parity
1	1	Output even parity	Judge as even parity

- To overwrite the PSn1 and PSn0 bits, first clear (0) the TXEn and RXEn bits.
- If "0 parity" is selected for reception, no parity judgment is performed. Therefore, no error interrupt is generated because the PEn bit of the ASISn register is not set.

CLn	Specification of character length of 1 frame of transmit/receive data
0	7 bits
1	8 bits

- To overwrite the CLn bit, first clear (0) the TXEn and RXEn bits.

SLn	Specification of stop bit length of transmit data
0	1 bit
1	2 bits

- To overwrite the SLn bit, first clear (0) the TXEn bit.
- Since reception is always done with a stop bit length of 1, the SLn bit setting does not affect receive operations.

ISRMn	Enable/disable of generation of reception completion interrupt requests when an error occurs
0	Generate a reception error interrupt request (INTSREn) as an interrupt when an error occurs. In this case, no reception completion interrupt request (INTSRn) is generated.
1	Generate a reception completion interrupt request (INTSRn) as an interrupt when an error occurs. In this case, no reception error interrupt request (INTSREn) is generated.

- To overwrite the ISRMn bit, first clear (0) the RXEn bit.

Note When reception is disabled, the receive shift register does not detect a start bit. No shift-in processing or transfer processing to receive buffer register n (RXBn) is performed, and the contents of the RXBn register are retained.

When reception is enabled, the receive shift operation starts, synchronized with the detection of the start bit, and when the reception of one frame is completed, the contents of the receive shift register are transferred to the RXBn register. A reception completion interrupt (INTSRn) is also generated in synchronization with the transfer to the RXBn register.

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1)
n = 0 to 2 (V850ES/KJ1)

(2) Asynchronous serial interface status register n (ASISn)

The ASISn register, which consists of 3 error flag bits (PEn, FEn and OVEn), indicates the error status when UARTn reception is complete.

The ASISn register is cleared to 00H by a read operation. When a reception error occurs, receive buffer register n (RXBn) should be read and the error flag should be cleared after the ASISn register is read.

This register is read-only in 8-bit units.

After reset, ASISn is set to 00H.

Cautions 1. When the UARTEn bit or RXEn bit of the ASIMn register is set to 0, or when the ASISn register is read, the PEn, FEn, and OVEn bits of the ASISn register are cleared (0).

2. Operation using a bit manipulation instruction is prohibited.

3. When the main clock is stopped and the CPU is operating on the subclock, do not access the ASISn register using an access method that causes a wait.
For details, refer to 3.4.8 (2).

After reset: 00H R Address: FFFFFA03H, FFFFFA13H, FFFFFA23H

	7	6	5	4	3	2	1	0
ASISn	0	0	0	0	0	PEn	FEn	OVEn

PEn	Status flag indicating a parity error
0	When the ASIMn register's UARTEn or RXEn bit is set to 0, or after the ASISn register has been read
1	When reception was completed, the receive data parity did not match the parity bit
• The operation of the PEn bit differs according to the settings of the PSn1 and PSn0 bits of the ASIMn register.	

FEn	Status flag indicating framing error
0	When the ASIMn register's UARTEn or RXEn bit is set to 0, or after the ASISn register has been read
1	When reception was completed, no stop bit was detected
• For receive data stop bits, only the first bit is checked regardless of the stop bit length.	

OVEn	Status flag indicating an overrun error
0	When the ASIMn register's UARTEn or RXEn bit is set to 0, or after the ASISn register has been read.
1	UARTn completed the next receive operation before reading the RXBn receive data.
• When an overrun error occurs, the next receive data value is not written to the RXBn register and the data is discarded.	

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1)
n = 0 to 2 (V850ES/KJ1)

(3) Asynchronous serial interface transmit status register n (ASIFn)

The ASIFn register, which consists of 2 status flag bits, indicates the status during transmission.

By writing the next data to the TXBn register after data is transferred from the TXBn register to the transmit shift register, transmit operations can be performed continuously without suspension even during an interrupt interval. When transmission is performed continuously, data should be written after referencing the TXBFn bit of the ASIFn register to prevent writing to the TXBn register by mistake.

This register is read-only in 8-bit or 1-bit units.

After reset, ASIFn is cleared to 00H.

After reset: 00H R Address: FFFFFA05H, FFFFFA15H, FFFFFA25H

	7	6	5	4	3	2	<1>	<0>
ASIFn	0	0	0	0	0	0	TXBFn	TXSFn

TXBFn	Transmission buffer data flag
0	Data to be transferred next to TXBn register does not exist (When the ASIMn register's UARTEn or TXEn bits is 0, or when data has been transferred to the transmission shift register)
1	Data to be transferred next exists in TXBn register (Data exists in TXBn register when the TXBn register has been written to)
• When transmission is performed continuously, data should be written to the TXBn register after confirming that this flag is 0. If writing to TXBn register is performed when this flag is 1, transmit data cannot be guaranteed.	

TXSFn	Transmit shift register data flag (indicates the transmission status of UARTn)
0	Initial status or a waiting transmission (When the ASIMn register's UARTEn or TXEn bits is set to 0, or when following transmission completion, the next data transfer from the TXBn register is not performed)
1	Transmission in progress (When data has been transferred from the TXBn register)
• When the transmission unit is initialized, initialization should be executed after confirming that this flag is 0 following the occurrence of a transmission completion interrupt. If initialization is performed when this flag is 1, transmit data cannot be guaranteed.	

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1)
n = 0 to 2 (V850ES/KJ1)

(4) Receive buffer register n (RXBn)

The RXBn register is an 8-bit buffer register for storing parallel data that had been converted by the receive shift register.

When reception is enabled (RXEn bit = 1 in the ASIMn register), receive data is transferred from the receive shift register to the RXBn register, synchronized with the completion of the shift-in processing of one frame. Also, a reception completion interrupt request (INTSRn) is generated by the transfer to the RXBn register. For information about the timing for generating this interrupt request, refer to **15.6.4 Receive operation**.

If reception is disabled (RXEn bit = 0 in the ASIMn register), the contents of the RXBn register are retained, and no processing is performed for transferring data to the RXBn register even when the shift-in processing of one frame is completed. Also, no reception completion interrupt is generated.

When 7 bits is specified for the data length, bits 6 to 0 of the RXBn register are transferred for the receive data and the MSB (bit 7) is always 0. However, if an overrun error (OVEn bit = 1 in the ASISn register) occurs, the receive data at that time is not transferred to the RXBn register.

The RXBn register becomes FFH when a reset is input or UARTEn bit = 0 in the ASIMn register.

This register is read-only in 8-bit units.

After reset: FFH R Address: FFFFFA02H, FFFFFA12H, FFFFFA22H

	7	6	5	4	3	2	1	0
RXBn	RXBn7	RXBn6	RXBn5	RXBn4	RXBn3	RXBn2	RXBn1	RXBn0

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1)
n = 0 to 2 (V850ES/KJ1)

(5) Transmit buffer register n (TXBn)

The TXBn register is an 8-bit buffer register for setting transmit data.

When transmission is enabled (TXEn bit = 1 in the ASIMn register), the transmit operation is started by writing data to TXBn register.

When transmission is disabled (TXEn bit = 0 in the ASIMn register), even if data is written to TXBn register, the value is ignored.

The TXBn register data is transferred to the transmit shift register, and a transmission completion interrupt request (INTSTn) is generated, synchronized with the completion of the transmission of one frame from the transmit shift register. For information about the timing for generating this interrupt request, refer to **15.6.2 Transmit operation**.

When TXBFn bit = 1 in the ASIFn register, writing must not be performed to TXBn register.

This register can be read or written in 8-bit units.

After reset, TXBn is set to FFH.

After reset: FFH R/W Address: FFFFFA04H, FFFFFA14H, FFFFFA24H

	7	6	5	4	3	2	1	0
TXBn	TXBn7	TXBn6	TXBn5	TXBn4	TXBn3	TXBn2	TXBn1	TXBn0

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1)
n = 0 to 2 (V850ES/KJ1)

15.5 Interrupt Requests

The following three types of interrupt requests are generated from UARTn.

- Reception error interrupt (INTSREn)
- Reception completion interrupt (INTSRn)
- Transmission completion interrupt (INTSTn)

The default priorities among these three types of interrupt requests is, from high to low, reception error interrupt, reception completion interrupt, and transmission completion interrupt.

Table 15-1. Generated Interrupts and Default Priorities

Interrupt	Priority
Reception error	1
Reception completion	2
Transmission completion	3

(1) Reception error interrupt (INTSREn)

When reception is enabled, a reception error interrupt is generated according to the logical OR of the three types of reception errors explained for the ASISn register. Whether a reception error interrupt (INTSREn) or a reception completion interrupt (INTSRn) is generated when an error occurs can be specified according to the ISRMn bit of the ASIMn register.

When reception is disabled, no reception error interrupt is generated.

(2) Reception completion interrupt (INTSRn)

When reception is enabled, a reception completion interrupt is generated when data is shifted in to the receive shift register and transferred to receive buffer register n (RXBn).

A reception completion interrupt request can be generated in place of a reception error interrupt according to the ISRMn bit of the ASIMn register even when a reception error has occurred.

When reception is disabled, no reception completion interrupt is generated.

(3) Transmission completion interrupt (INTSTn)

A transmission completion interrupt is generated when one frame of transmit data containing 7-bit or 8-bit characters is shifted out from the transmit shift register.

15.6 Operation

15.6.1 Data format

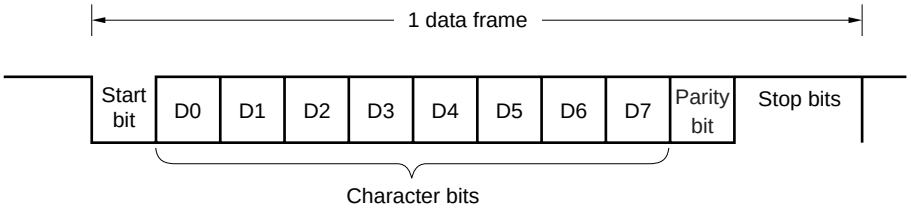
Full-duplex serial data transmission and reception can be performed.

The transmit/receive data format consists of one data frame containing a start bit, character bits, a parity bit, and stop bits as shown in Figure 15-3.

The character bit length within one data frame, the type of parity, and the stop bit length are specified according to asynchronous serial interface mode register n (ASIMn).

Also, data is transferred LSB first.

Figure 15-3. Format of Asynchronous Serial Interface Transmit/Receive Data



- Start bit ··· 1 bit
- Character bits ··· 7 bits or 8 bits
- Parity bit ··· Even parity, odd parity, 0 parity, or no parity
- Stop bits ··· 1 bit or 2 bits

15.6.2 Transmit operation

When the UARTEn bit is set to 1 in the ASIMn register, a high level is output from the TXDn pin.

Then, when the TXEn bit is set to 1 in the ASIMn register, transmission is enabled, and the transmit operation is started by writing transmit data to transmit buffer register n (TXBn).

(1) Transmission enabled state

This state is set by the TXEn bit in the ASIMn register.

- TXEn = 1: Transmission enabled state
- TXEn = 0: Transmission disabled state

Since UARTn does not have a CTS (transmission enabled signal) input pin, a port should be used to confirm whether the destination is in a reception enabled state.

(2) Starting a transmit operation

In the transmission enabled state, a transmit operation is started by writing transmit data to transmit buffer register n (TXBn). When a transmit operation is started, the data in TXBn is transferred to the transmit shift register. Then, the transmit shift register outputs data to the TXDn pin (the transmit data is transferred sequentially starting with the start bit). The start bit, parity bit, and stop bits are added automatically.

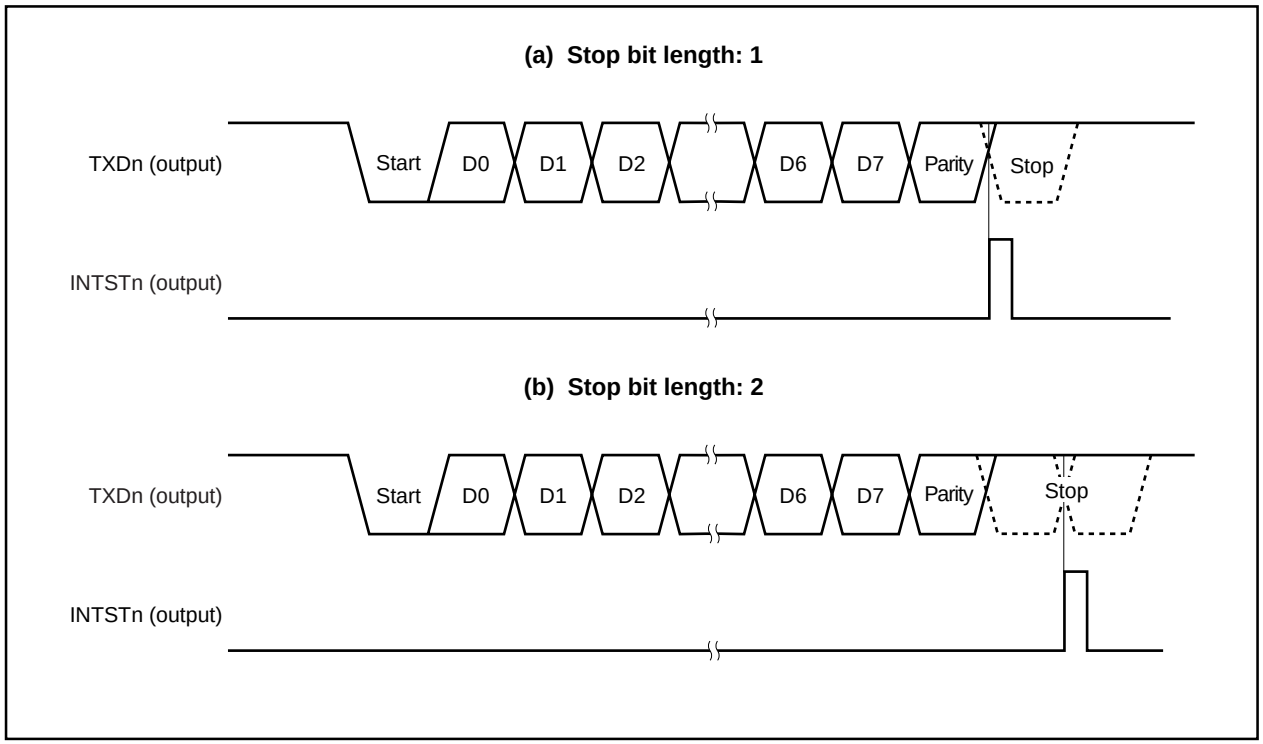
(3) Transmission interrupt

When the transmit shift register becomes empty, a transmission completion interrupt (INTSTn) is generated. The timing for generating the INTSTn interrupt differs according to the specification of the stop bit length. The INTSTn interrupt is generated at the same time that the last stop bit is output.

If the data to be transmitted next has not been written to the TXBn register, the transmit operation is suspended.

Caution Normally, when the transmit shift register becomes empty, a transmission completion interrupt (INTSTn) is generated. However, no transmission completion interrupt (INTSTn) is generated if the transmit shift register becomes empty due to reset.

Figure 15-4. Asynchronous Serial Interface Transmission Completion Interrupt Timing



15.6.3 Continuous transmission operation

UARTn can write the next transmit data to the TXBn register at the timing that the transmit shift register starts the shift operation. This enables an efficient transmission rate to be realized by continuously transmitting data even during the INTSTn interrupt service after the transmission of one data frame. In addition, reading the TXSFn bit of the ASIFn register after the occurrence of a transmission completion interrupt enables the TXBn register to be efficiently written twice (2 bytes) without waiting for the transmission of 1 data frame.

When continuous transmission is performed, data should be written after referencing the ASIFn register to confirm the transmission status and whether or not data can be written to the TXBn register.

★ **Caution The values of the TXBFn and TXSFn bits of the ASIS register change 10 → 11 → 01 in continuous transmission.**
Therefore, do not confirm the status based on the combination of the TXBFn and TXSFn bits.
Read only the TXBFn bit during continuous transmission.

TXBFn	Whether or Not Writing to TXBn Register Is Enabled
0	Writing is enabled
1	Writing is not enabled

Caution When transmission is performed continuously, write the first transmit data (first byte) to the TXBn register and confirm that the TXBFn bit is 0, and then write the next transmit data (second byte) to TXBn register. If writing to the TXBn register is performed when the TXBFn bit is 1, transmit data cannot be guaranteed.

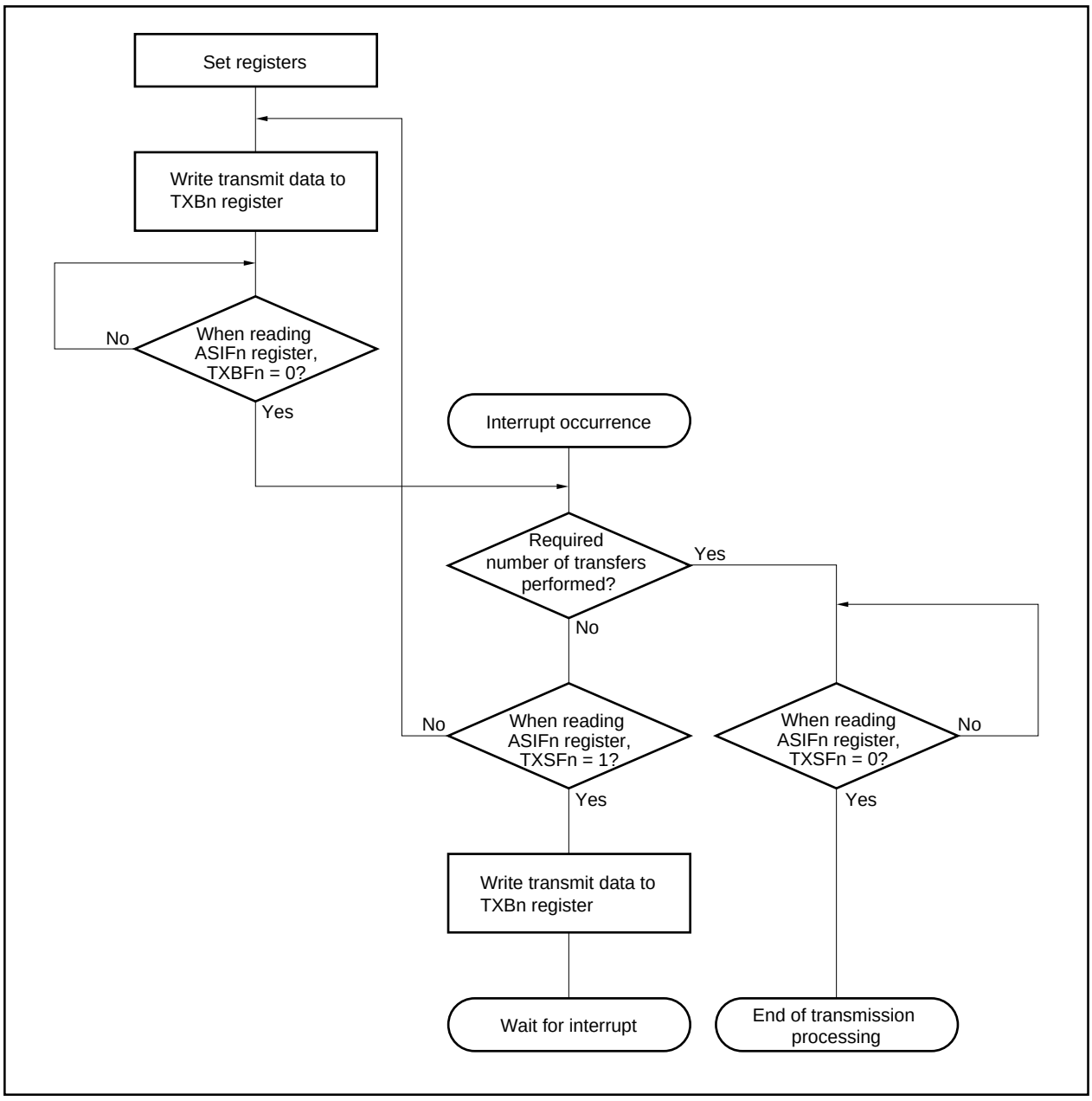
The communication status can be confirmed by referring to the TXSFn bit.

TXSFn	Transmission Status
0	Transmission is completed.
1	Under transmission.

Cautions 1. When initializing the transmission unit when continuous transmission is completed, confirm that the TXSFn bit is 0 after the occurrence of the transmission completion interrupt, and then execute initialization. If initialization is performed when the TXSFn bit is 1, transmit data cannot be guaranteed.

2. While transmission is being performed continuously, an overrun error may occur if the next transmission is completed before the INTSTn interrupt servicing following the transmission of 1 data frame is executed. An overrun error can be detected by embedding a program that can count the number of transmit data and referencing TXSFn bit.

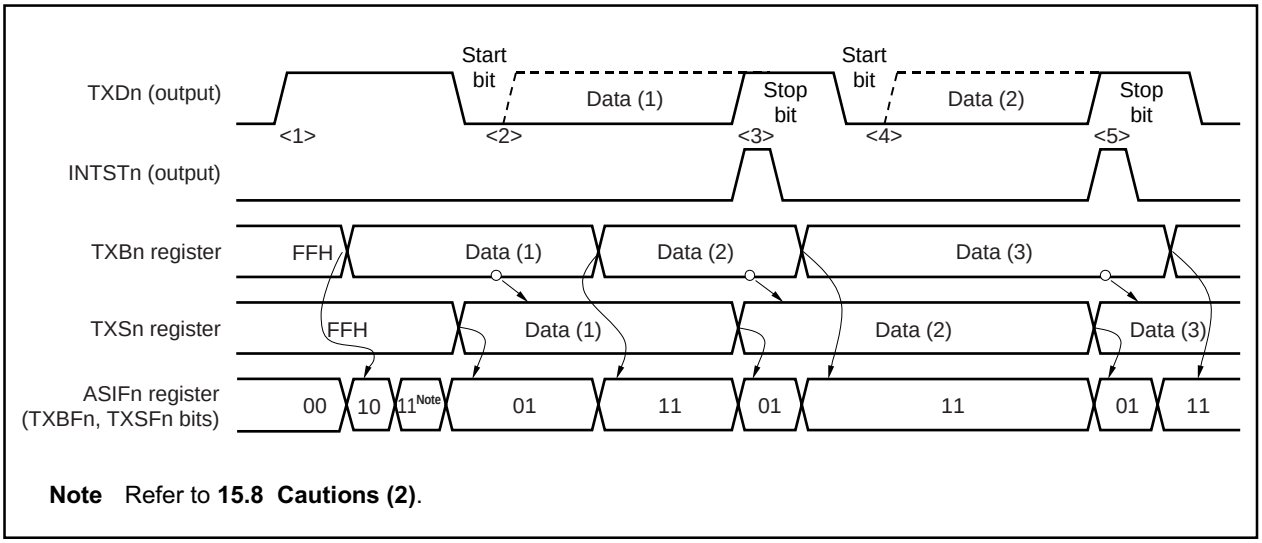
Figure 15-5. Continuous Transmission Processing Flow



(1) Starting procedure

The procedure to start continuous transmission is shown below.

Figure 15-6. Continuous Transmission Starting Procedure



Note Refer to **15.8 Cautions (2)**.

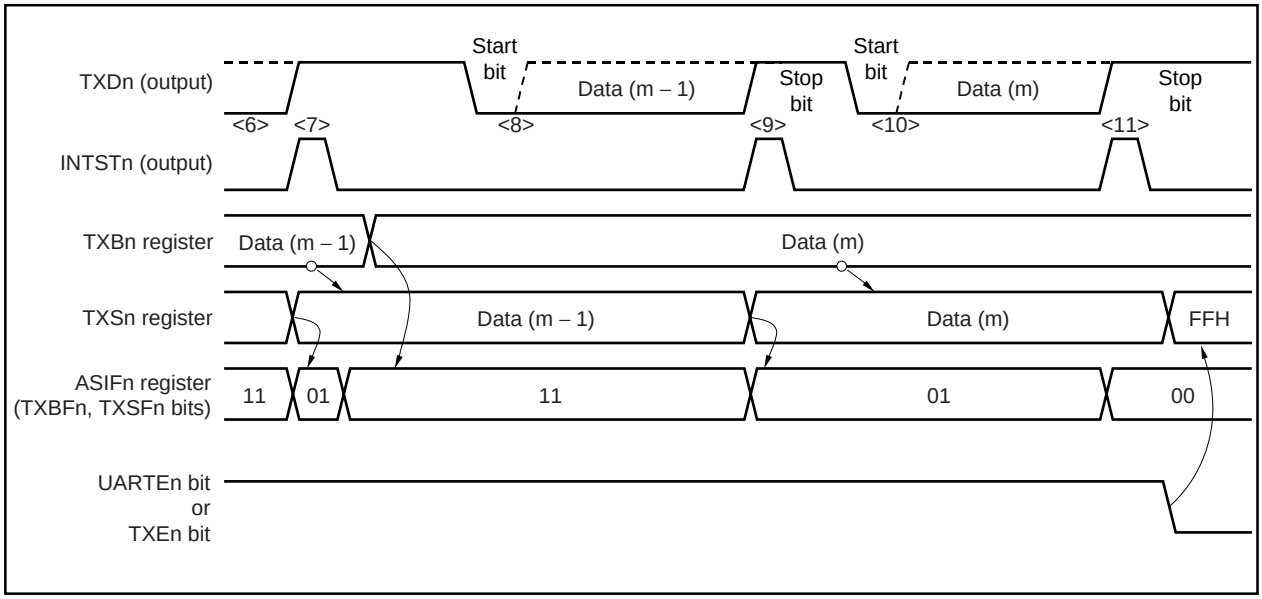
Transmission Starting Procedure	Internal Operation	ASIFn Register	
		TXBFn	TXSFn
• Set transmission mode	<1> Start transmission unit	0	0
• Write data (1)		1	0
	<2> Generate start bit	1	1Note
		0	1
	Start data (1) transmission	0	1
• Read ASIFn register (confirm that TXBFn bit = 0)		0	1
• Write data (2)		1	1
	<<Transmission in progress>>		
	<3> INTSTn interrupt occurs	0	1
• Read ASIFn register (confirm that TXBFn bit = 0)		0	1
• Write data (3)		1	1
	<4> Generate start bit		
	Start data (2) transmission		
	<<Transmission in progress>>		
	<5> INTSTn interrupt occurs	0	1
• Read ASIFn register (confirm that TXBFn bit = 0)		0	1
• Write data (4)		1	1

Note Refer to **15.8 Cautions (2)**.

(2) Ending procedure

The procedure for ending continuous transmission is shown below.

Figure 15-7. Continuous Transmission End Procedure



Transmission End Procedure	Internal Operation	ASIFn Register	
		TXBFn	TXSFn
	<6> Transmission of data (m – 2) is in progress	1	1
	<7> INTSTn interrupt occurs →	0	1
• Read ASIFn register (confirm that TXBFn bit = 0) ←		0	1
• Write data (m) →		1	1
	<8> Generate start bit Start data (m – 1) transmission <<Transmission in progress>>		
	<9> INTSTn interrupt occurs →	0	1
• Read ASIFn register (confirm that TXSFn bit = 1) ←		0	1
There is no write data			
	<10> Generate start bit Start data (m) transmission <<Transmission in progress>>		
	<11> Generate INTSTn interrupt →	0	0
• Read ASIFn register (confirm that TXSFn bit = 0) ←		0	0
• Clear (0) the UARTEn bit or TXEn bit	Initialize internal circuits		

15.6.4 Receive operation

The awaiting reception state is set by setting the UARTEn bit to 1 in the ASIMn register and then setting the RXEn bit to 1 in the ASIMn register. To start the receive operation, start sampling at the falling edge when the falling of the RXDn pin is detected. If the RXDn pin is low level at a start bit sampling point, the start bit is recognized. When the receive operation begins, serial data is stored sequentially in the receive shift register according to the baud rate that was set. A reception completion interrupt (INTSRn) is generated each time the reception of one frame of data is completed. Normally, the receive data is transferred from receive buffer register n (RXBn) to memory by this interrupt servicing.

(1) Reception enabled state

The receive operation is set to the reception enabled state by setting the RXEn bit in the ASIMn register to 1.

- RXEn bit = 1: Reception enabled state
- RXEn bit = 0: Reception disabled state

In receive disabled state, the reception hardware stands by in the initial state. At this time, the contents of receive buffer register n (RXBn) are retained, and no reception completion interrupt or reception error interrupt is generated.

(2) Starting a receive operation

A receive operation is started by the detection of a start bit.

The RXDn pin is sampled using the serial clock from baud rate generator n (BRGn).

(3) Reception completion interrupt

When RXEn = 1 in the ASIMn register and the reception of one frame of data is completed (the stop bit is detected), a reception completion interrupt (INTSRn) is generated and the receive data within the receive shift register is transferred to RXBn at the same time.

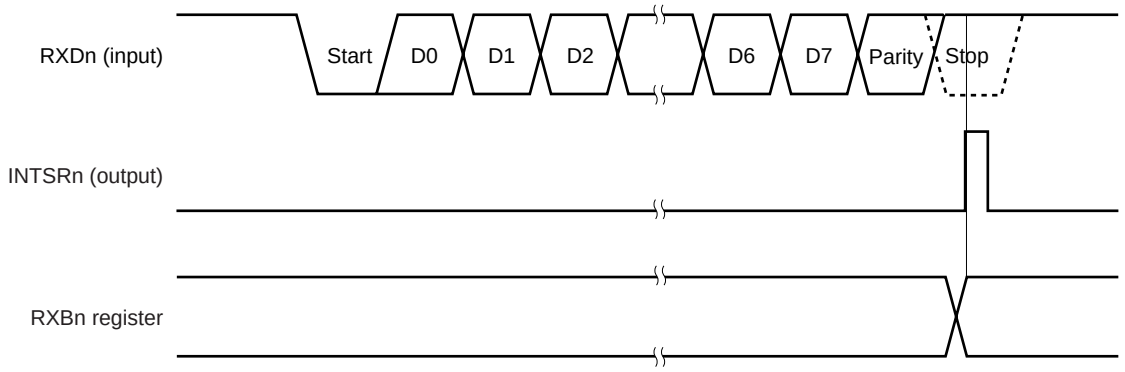
Also, if an overrun error (OVEn bit = 1 in the asynchronous serial interface status register (ASISn)) occurs, the receive data at that time is not transferred to receive buffer register n (RXBn), and either a reception completion interrupt (INTSRn) or a reception error interrupt (INTSREn) is generated according to the ISRMn bit setting in the ASIMn register.

Even if a parity error (PEn bit = 1 in the ASISn register) or framing error (FEn bit = 1 in the ASISn register) occurs during a reception operation, the receive operation continues until stop bit is received, and after reception is completed, either a reception completion interrupt (INTSRn) or a reception error interrupt (INTSREn) is generated according to the ISRMn bit setting in the ASIMn register (the receive data within the receive shift register is transferred to RXBn).

If the RXEn bit is reset (0) during a receive operation, the receive operation is immediately stopped. The contents of receive buffer register n (RXBn) and of the asynchronous serial interface status register (ASISn) at this time do not change, and no reception completion interrupt (INTSRn) or reception error interrupt (INTSREn) is generated.

No reception completion interrupt is generated when RXEn = 0 (reception is disabled).

Figure 15-8. Asynchronous Serial Interface Reception Completion Interrupt Timing



Cautions 1. Be sure to read receive buffer register n (RXBn) even when a reception error occurs. If RXBn is not read, an overrun error will occur at the next data reception and the reception error status will continue infinitely.

2. Reception is always performed assuming a stop bit length of 1.
A second stop bit is ignored.

15.6.5 Reception error

The three types of errors that can occur during a receive operation are a parity error, framing error, and overrun error. As a result of data reception, the various flags of the ASISn register are set (1), and a reception error interrupt (INTSREn) or a reception completion interrupt (INTSRn) is generated at the same time. The ISRMn bit of the ASIMn register specifies whether INTSREn or INTSRn is generated.

The type of error that occurred during reception can be detected by reading the contents of the ASISn register during the INTSREn or INTSRn interrupt servicing.

The contents of the ASISn register are reset (0) by reading the ASISn register.

Table 15-2. Reception Error Causes

Error Flag	Reception Error	Cause
PEn	Parity error	The parity specification during transmission did not match the parity of the reception data
FEn	Framing error	No stop bit was detected
OVEn	Overrun error	The reception of the next data was completed before data was read from receive buffer register n (RXBn)

(1) Separation of reception error interrupt

A reception error interrupt can be separated from the INTSRn interrupt and generated as the INTSREn interrupt by clearing the ISRMn bit of the ASIMn register to 0.

Figure 15-9. When Reception Error Interrupt Is Separated from INTSRn Interrupt (ISRMn Bit = 0)

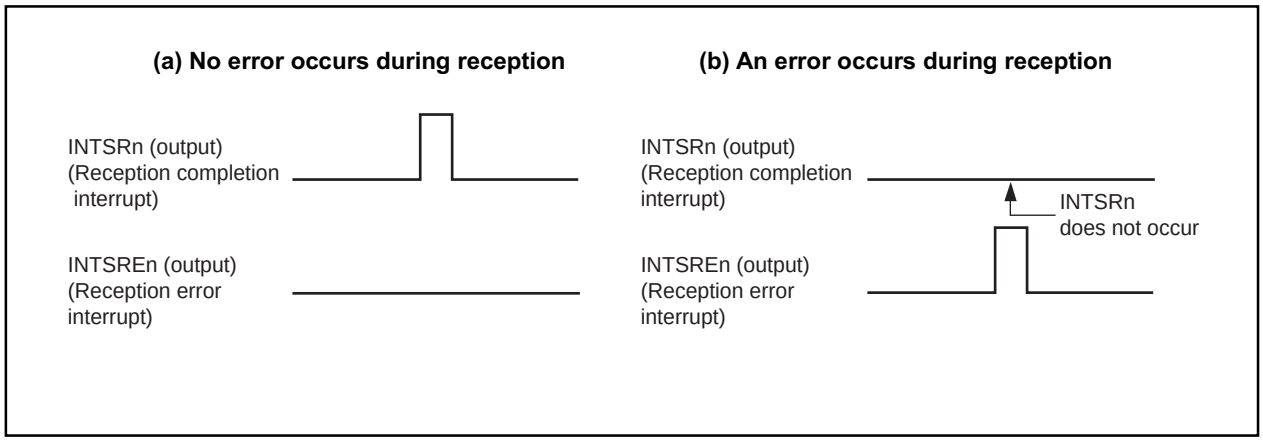
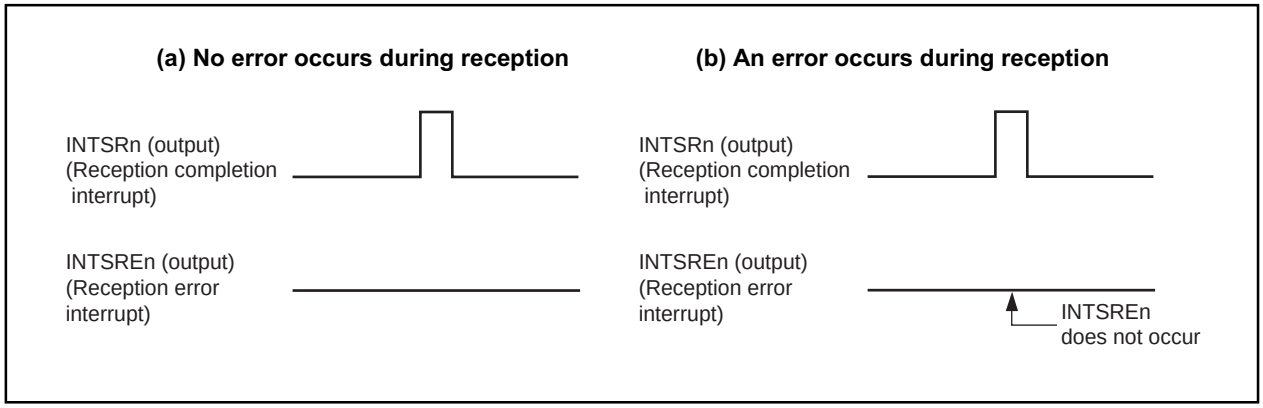


Figure 15-10. When Reception Error Interrupt Is Included in INTSRn Interrupt (ISRMn Bit = 1)



15.6.6 Parity types and corresponding operation

A parity bit is used to detect a bit error in communication data. Normally, the same type of parity bit is used on the transmission and reception sides.

(1) Even parity

(i) During transmission

The parity bit is controlled so that the number of bits with the value “1” within the transmit data including the parity bit is even. The parity bit value is as follows.

- If the number of bits with the value “1” within the transmit data is odd: 1
- If the number of bits with the value “1” within the transmit data is even: 0

(ii) During reception

The number of bits with the value “1” within the receive data including the parity bit is counted, and a parity error is generated if this number is odd.

(2) Odd parity

(i) During transmission

In contrast to even parity, the parity bit is controlled so that the number of bits with the value “1” within the transmit data including the parity bit is odd. The parity bit value is as follows.

- If the number of bits with the value “1” within the transmit data is odd: 0
- If the number of bits with the value “1” within the transmit data is even: 1

(ii) During reception

The number of bits with the value “1” within the receive data including the parity bit is counted, and a parity error is generated if this number is even.

(3) 0 parity

During transmission the parity bit is set to “0” regardless of the transmit data.

During reception, no parity bit check is performed. Therefore, no parity error is generated regardless of whether the parity bit is “0” or “1”.

(4) No parity

No parity bit is added to the transmit data.

During reception, the receive operation is performed as if there were no parity bit. Since there is no parity bit, no parity error is generated.

15.6.7 Receive data noise filter

The RXDn signal is sampled at the rising edge of the prescaler output base clock (Clock). If the same sampling value is obtained twice, the match detector output changes, and this output is sampled as input data. Therefore, data not exceeding one clock width is judged to be noise and is not delivered to the internal circuit (see **Figure 15-12**). Refer to **15.7.1 (1) Base clock (Clock)** regarding the base clock.

Also, since the circuit is configured as shown in Figure 15-11, internal processing during a receive operation is delayed by up to 2 clocks according to the external signal status.

Figure 15-11. Noise Filter Circuit

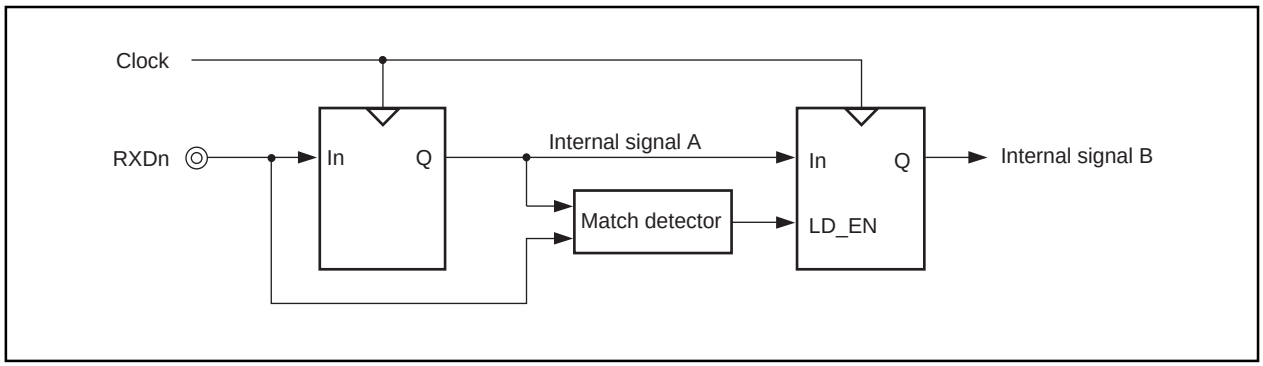
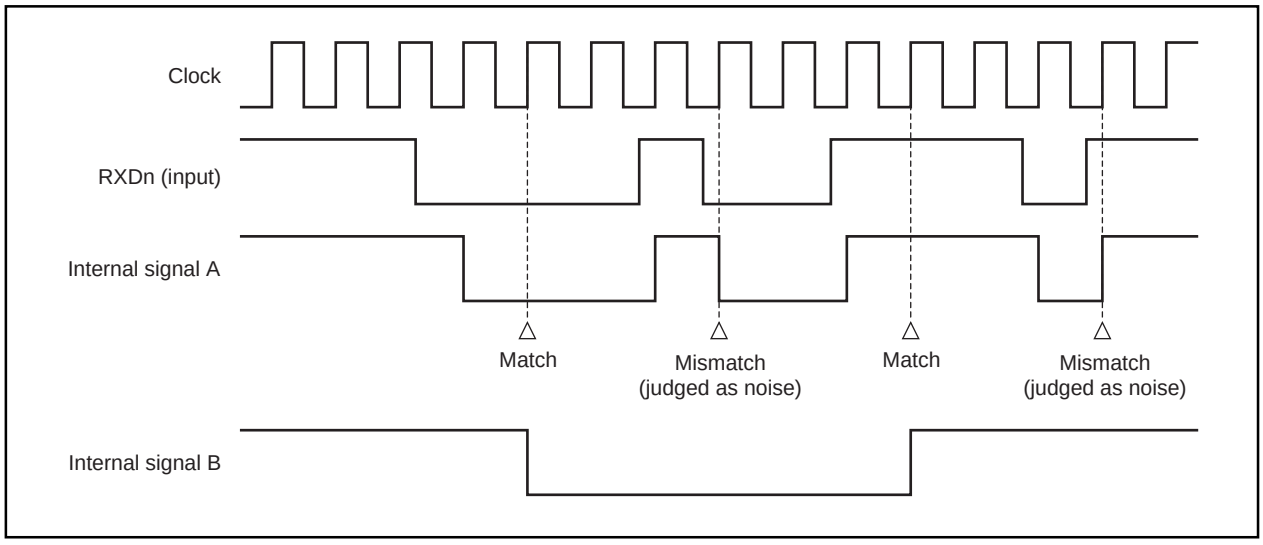


Figure 15-12. Timing of RXDn Signal Judged as Noise



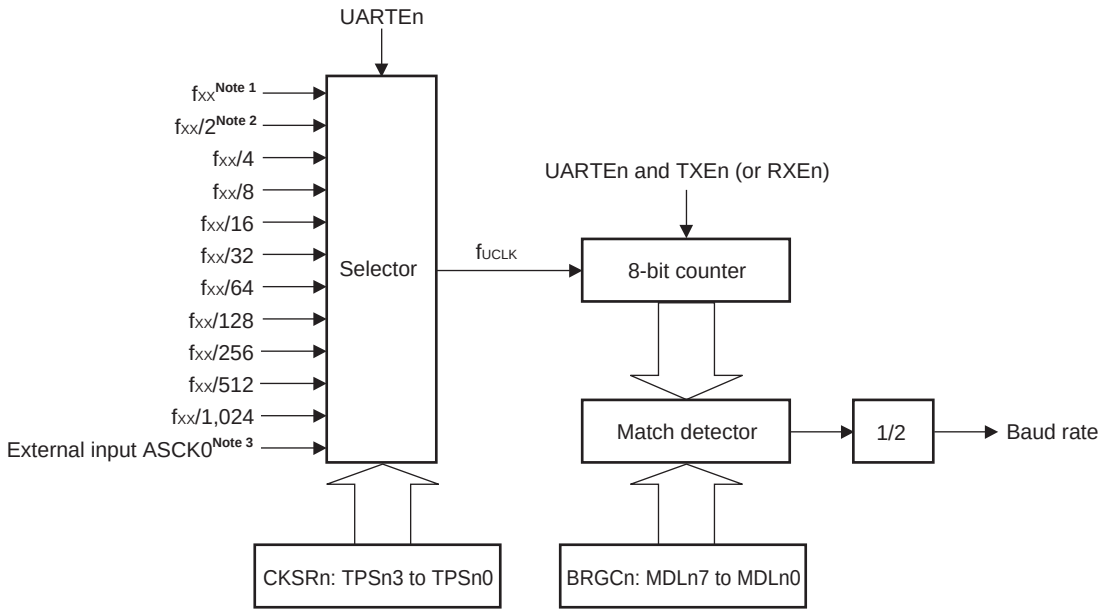
15.7 Dedicated Baud Rate Generator n (BRGn)

A dedicated baud rate generator, which consists of a source clock selector and an 8-bit programmable counter, generates serial clocks during transmission/reception by UARTn. The dedicated baud rate generator output can be selected as the serial clock for each channel.

Separate 8-bit counters exist for transmission and for reception.

15.7.1 Baud rate generator n (BRGn) configuration

Figure 15-13. Configuration of Baud Rate Generator n (BRGn)



Notes 1. V_{DD} = 4.0 to 5.5 V: Selectable when $f_{XX} \leq 12$ MHz
V_{DD} = 2.7 to 4.0 V: Selectable when $f_{XX} \leq 6$ MHz

2. V_{DD} = 2.7 to 4.0 V: Selectable when $f_{XX} \leq 12$ MHz

3. ASCK0 can be used only by UART0.

Remark f_{XX}: Main clock

(1) Base clock

When the UARTEn bit = 1 in the ASIMn register, the clock selected according to the TPSn3 to TPSn0 bits of the CKSRn register is supplied to the transmission/reception unit. This clock is called the base clock (f_{UCLK}). When UARTEn = 0, f_{UCLK} is fixed to low level.

15.7.2 Serial clock generation

A serial clock can be generated according to the settings of the CKSRn and BRGCn registers.

The base clock to the 8-bit counter is selected by the TPSn3 to TPSn0 bits of the CKSRn register.

The 8-bit counter divisor value can be set by the MDLn7 to MDLn0 bits of the BRGCn register.

(1) Clock select register n (CKSRn)

The CKSRn register is an 8-bit register for selecting the basic block using the TPSn3 to TPSn0 bits. The clock selected by the TPSn3 to TPSn0 bits becomes the base clock (f_{UCLK}) of the transmission/reception module.

This register can be read or written in 8-bit units.

After reset, CKSRn is cleared to 00H.

Caution Set the UARTEn bit of the ASIMn register to 0 before rewriting the TPSn3 to TPSn0 bits.

After reset: 00H R/W Address: FFFFFA06H, FFFFFA16H, FFFFFA26H

	7	6	5	4	3	2	1	0
CKSRn	0	0	0	0	TPSn3	TPSn2	TPSn1	TPSn0

TPSn3	TPSn2	TPSn1	TPSn0	Base clock (f_{UCLK})[Note 1]
0	0	0	0	f_{XX}
0	0	0	1	$f_{XX}/2$
0	0	1	0	$f_{XX}/4$
0	0	1	1	$f_{XX}/8$
0	1	0	0	$f_{XX}/16$
0	1	0	1	$f_{XX}/32$
0	1	1	0	$f_{XX}/64$
0	1	1	1	$f_{XX}/128$
1	0	0	0	$f_{XX}/256$
1	0	0	1	$f_{XX}/512$
1	0	1	0	$f_{XX}/1,024$
1	0	1	1	ASCK0[Note 2] (external input)
Other than above				Setting prohibited

Notes 1. Set so as to satisfy the following conditions.

V_{DD} = 4.0 to 5.5 V: $f_{UCLK} \leq 12$ MHz

V_{DD} = 2.7 to 4.0 V: $f_{UCLK} \leq 6$ MHz

2. ASCK0 input clock can be used only by UART0.

Setting of UART1 and UART2 is prohibited.

Remark n: 0 to 2

(2) Baud rate generator control register n (BRGCn)

The BRGCn register is an 8-bit register that controls the baud rate (serial transfer speed) of UARTn.

This register can be read or written in 8-bit units.

After reset, BRGCn is set to FFH.

Caution If the MDLn7 to MDLn0 bits are to be overwritten, the TXEn and RXEn bits should be set to 0 in the ASIMn register first.

After reset: FFH R/W Address: FFFFFA07H, FFFFFA17H, FFFFFA27H

	7	6	5	4	3	2	1	0
BRGCn	MDLn7	MDLn6	MDLn5	MDLn4	MDLn3	MDLn2	MDLn1	MDLn0

MDLn7	MDLn6	MDLn5	MDLn4	MDLn3	MDLn2	MDLn1	MDLn0	Setting value (k)	Serial clock
0	0	0	0	0	×	×	×	–	Setting prohibited
0	0	0	0	1	0	0	0	8	$f_{UCLK}/8$
0	0	0	0	1	0	0	1	9	$f_{UCLK}/9$
0	0	0	0	1	0	1	0	10	$f_{UCLK}/10$
⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮	⋮
1	1	1	1	1	0	1	0	250	$f_{UCLK}/250$
1	1	1	1	1	0	1	1	251	$f_{UCLK}/251$
1	1	1	1	1	1	0	0	252	$f_{UCLK}/252$
1	1	1	1	1	1	0	1	253	$f_{UCLK}/253$
1	1	1	1	1	1	1	0	254	$f_{UCLK}/254$
1	1	1	1	1	1	1	1	255	$f_{UCLK}/255$

Remarks 1. f_{UCLK}: Base clock selected by TPSn3 to TPSn0 bits of CKSRn register

2. k: Value set by MDLn7 to MDLn0 bits (k = 8, 9, 10, ..., 255)

3. The baud rate is the output clock for the 8-bit counter divided by 2

4. ×: Don't care

(3) Baud rate

The baud rate is the value obtained by the following formula.

$$\text{Baud rate} = \frac{f_{UCLK}}{2 \times k} \text{ [bps]}$$

f_{UCLK} = Frequency [Hz] of base clock selected by TPSn3 to TPSn0 bits of CKSRn register.
k = Value set by MDLn7 to MDLn0 bits of BRGCn register (k = 8, 9, 10, ..., 255)

(4) Baud rate error

The baud rate error is obtained by the following formula.

$$\text{Error (\%)} = \left(\frac{\text{Actual baud rate (baud rate with error)}}{\text{Target baud rate (normal baud rate)}} - 1 \right) \times 100 \text{ [\%]}$$

Cautions 1. Make sure that the baud rate error during transmission does not exceed the allowable error of the reception destination.

2. Make sure that the baud rate error during reception is within the allowable baud rate range during reception, which is described in (4) Allowable baud rate during reception.

Example: Base clock frequency = 10 MHz = 10,000,000 Hz
Setting of MDLn7 to MDLn0 bits in BRGCn register = 00100001B (k = 33)
Target baud rate = 153,600 bps

Baud rate = 10M/(2 × 33)
= 10,000,000/(2 × 33) = 151,515 [bps]

Error = (151,515/153,600 − 1) × 100
= −1.357 [%]

15.7.3 Baud rate setting example

Table 15-3. Baud Rate Generator Setting Data

Baud Rate (bps)	f_{XX} = 20 MHz			f_{XX} = 16 MHz			f_{XX} = 10 MHz		
	f_{UCLK}	k	ERR	f_{UCLK}	k	ERR	f_{UCLK}	k	ERR
300	f_{XX}/512	41H (65)	0.16	f_{XX}/1024	1AH (26)	0.16	f_{XX}/256	41H (65)	0.16
600	f_{XX}/256	41H (65)	0.16	f_{XX}/1024	0DH (13)	0.16	f_{XX}/128	41H (65)	0.16
1200	f_{XX}/128	41H (65)	0.16	f_{XX}/512	0DH (13)	0.16	f_{XX}/64	41H (65)	0.16
2400	f_{XX}/64	41H (65)	0.16	f_{XX}/256	0DH (13)	0.16	f_{XX}/32	41H (65)	0.16
4800	f_{XX}/32	41H (65)	0.16	f_{XX}/128	0DH (13)	0.16	f_{XX}/16	41H (65)	0.16
9600	f_{XX}/16	41H (65)	0.16	f_{XX}/64	0DH (13)	0.16	f_{XX}/8	41H (65)	0.16
10400	f_{XX}/64	0FH (15)	0.16	f_{XX}/64	0CH (12)	0.16	f_{XX}/32	0FH (15)	0.16
19200	f_{XX}/8	41H (65)	0.16	f_{XX}/32	0DH (13)	0.16	f_{XX}/4	41H (65)	0.16
24000	f_{XX}/32	0DH (13)	0.16	f_{XX}/2	A7H (167)	–0.20	f_{XX}/16	0DH (13)	0.16
31250	f_{XX}/32	0AH (10)	0.00	f_{XX}/32	08H (8)	0.00	f_{XX}/16	0AH (10)	0
33600	f_{XX}/2	95H (149)	–0.13	f_{XX}/2	77H (119)	0.04	f_{XX}	95H (149)	–0.13
38400	f_{XX}/4	41H (65)	0.16	f_{XX}/16	0DH (13)	0.16	f_{XX}/2	41H (65)	0.16
48000	f_{XX}/16	0DH (13)	0.16	f_{XX}/2	53H (83)	0.40	f_{XX}/8	0DH (13)	0.16
56000	f_{XX}/2	59H (89)	0.32	f_{XX}/2	47H (71)	0.60	f_{XX}	59H (89)	0.32
62500	f_{XX}/16	0AH (10)	0.00	f_{XX}/16	08H (8)	0.00	f_{XX}/8	0AH (10)	0.00
76800	f_{XX}/2	41H (65)	0.16	f_{XX}/8	0DH (13)	0.16	f_{XX}	41H (65)	0.16
115200	f_{XX}/2	2BH (43)	0.94	f_{XX}/2	23H (35)	–0.79	f_{XX}	2BH (43)	0.94
153600	f_{XX}/2	21H (33)	–1.36	f_{XX}/4	0DH (13)	0.16	f_{XX}	21H (33)	–1.36
312500	f_{XX}/4	08H (8)	0	f_{XX}/2	0DH (13)	–1.54	f_{XX}/2	08H (8)	0.00

Caution The maximum allowable frequency of the base clock (f_{CLK}) is 12 MHz.

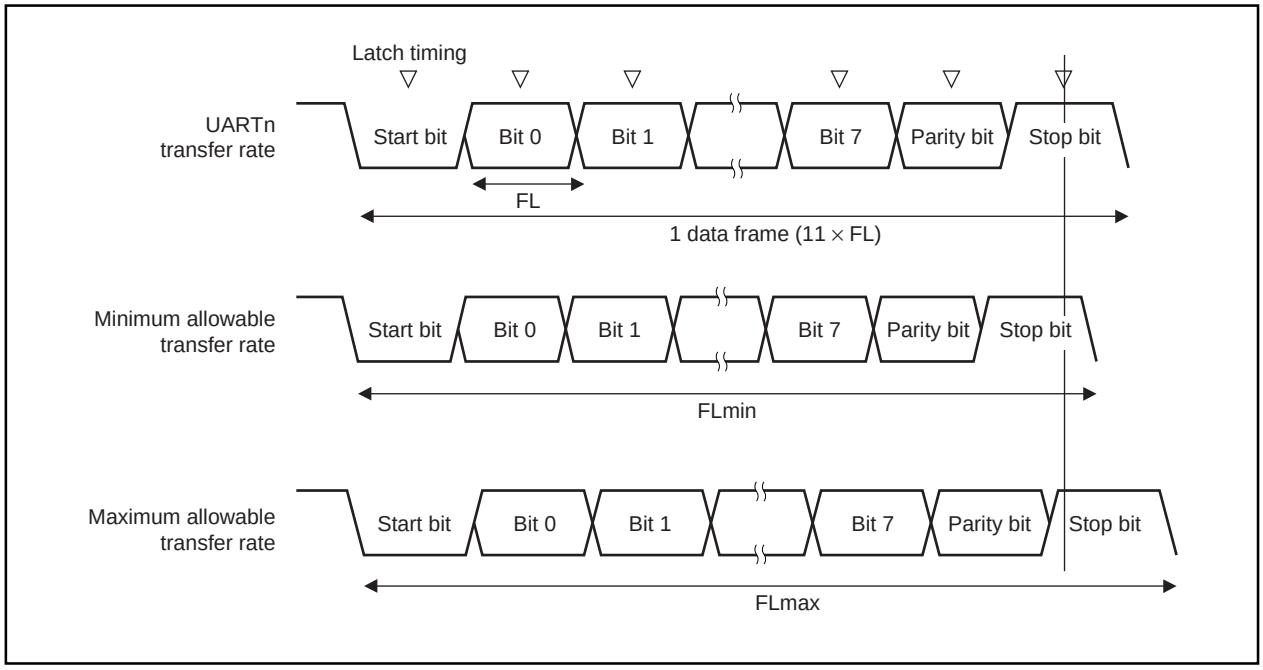
Remark f_{XX}: Main clock frequency
f_{UCLK}: Base clock frequency
k: Setting values of MDLn7 to MDLn0 bits in BRGCn register
ERR: Baud rate error [%]
n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

15.7.4 Allowable baud rate range during reception

The degree to which a discrepancy from the transmission destination's baud rate is allowed during reception is shown below.

Caution The equations described below should be used to set the baud rate error during reception so that it always is within the allowable error range.

Figure 15-14. Allowable Baud Rate Range During Reception



As shown in Figure 15-14, after the start bit is detected, the receive data latch timing is determined according to the counter that was set by the BRGCn register. If all data up to the final data (stop bit) is in time for this latch timing, the data can be received normally.
If this is applied to 11-bit reception, the following is theoretically true.

$$FL = (Brate)^{-1}$$

Brate: UARTn baud rate
k: BRGCn register setting value
FL: 1-bit data length

When the latch timing margin is 2 base clocks, the minimum allowable transfer rate (FLmin) is as follows.

$$FLmin = 11 \times FL - \frac{k-2}{2k} \times FL = \frac{21k+2}{2k} FL$$

Therefore, the transfer destination's maximum receivable baud rate (BRmax) is as follows.

$$BRmax = (FLmin/11)^{-1} = \frac{22k}{21k + 2} Brate$$

Similarly, the maximum allowable transfer rate (FLmax) can be obtained as follows.

$$\frac{10}{11} \times FLmax = 11 \times FL - \frac{k + 2}{2 \times k} \times FL = \frac{21k - 2}{2 \times k} FL$$

$$FLmax = \frac{21k - 2}{20k} FL \times 11$$

Therefore, the transfer destination's minimum receivable baud rate (BRmin) is as follows.

$$BRmin = (FLmax/11)^{-1} = \frac{20k}{21k - 2} Brate$$

The allowable baud rate error of UARTn and the transfer destination can be obtained as follows from the expressions described above for computing the minimum and maximum baud rate values.

Table 15-4. Maximum and Minimum Allowable Baud Rate Error

Division Ratio (k)	Maximum Allowable Baud Rate Error	Minimum Allowable Baud Rate Error
8	+3.53%	–3.61%
20	+4.26%	–4.31%
50	+4.56%	–4.58%
100	+4.66%	–4.67%
255	+4.72%	–4.73%

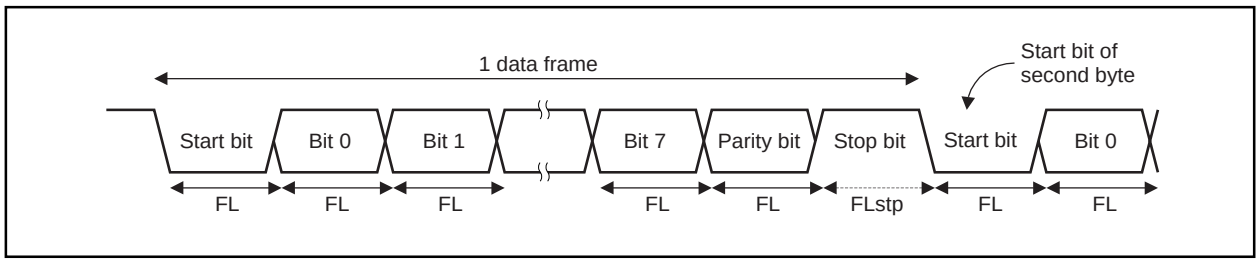
Remarks 1. The reception precision depends on the number of bits in one frame, the base clock frequency, and the division ratio (k). The higher the base clock frequency and the larger the division ratio (k), the higher the precision.

2. k: BRGCn setting value

15.7.5 Transfer rate during continuous transmission

During continuous transmission, the transfer rate from a stop bit to the next start bit is extended two clocks of the base clock longer than normal. However, on the reception side, the transfer result is not affected since the timing is initialized by the detection of the start bit.

Figure 15-15. Transfer Rate During Continuous Transmission



Representing the 1-bit data length by FL, the stop bit length by FLstp, and the base clock frequency by f_{UCLK} yields the following equation.

$$FLstp = FL + 2/f_{UCLK}$$

Therefore, the transfer rate during continuous transmission is as follows (when the stop bit length = 1).

$$\text{Transfer rate} = 11 \times FL = 2/f_{UCLK}$$

15.8 Cautions

Cautions to be observed when using UARTn are shown below.

(1) When the supply of clocks to UARTn is stopped (for example, in IDLE or STOP mode), operation stops with each register retaining the value it had immediately before the supply of clocks was stopped. The TXDn pin output also holds and outputs the value it had immediately before the supply of clocks was stopped. However, operation is not guaranteed after the supply of clocks is restarted. Therefore, after the supply of clocks is restarted, the circuits should be initialized by setting UARTEn = 0, RXEn = 0, and TXEn = 0 in the ASIMn register.

(2) UARTn has a 2-stage buffer configuration consisting of transmission buffer register n (TXBn) and the transmission shift register, and has status flags (the TXBFn and TXSFn bits of the ASIFn register) that indicate the status of each buffer. If the TXBFn and TXSFn bits are read in continuous transmission, the value changes 10 → 11 →01. Read only the TXBFn bit during continuous transmission.

CHAPTER 16 CLOCKED SERIAL INTERFACE 0 (CSI0)

The number of clocked serial interface 0 (CSI0) channels incorporated differs as follows depending on the product.

Product Name	V850ES/KF1	V850ES/KG1	V850ES/KJ1
Number of channels	2 channels (CSI00, CSI01)		3 channels (CSI00 to CSI02)

16.1 Features

- Half-duplex communications
- Master mode/slave mode selectable
- Transmission data length: 8 bits or 16 bits can be set
- MSB/LSB-first selectable for transfer data
- Eight clock signals can be selected (7 master clocks and 1 slave clock)
- 3-wire type SO0n: Serial transmit data output
  SI0n: Serial receive data input
  $\overline{\text{SCK0n}}$: Serial clock I/O
- Interrupt sources: 1 type
  - Transmission/reception completion interrupt (INTCSI0n)
- Transmission/reception mode or reception-only mode selectable
- Two transmission buffers (SOTBFn/SOTBFLn, SOTBn/SOTBLn) and two reception buffers (SIRBn/SIRBLn, SIRBEn/SIRBELn) are provided on chip
- Single transfer mode/continuous transfer mode selectable

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

16.2 Configuration

CSI0n is controlled via clocked serial interface mode register 0n (CSIM0n).

(1) Clocked serial interface mode register 0n (CSIM0n)

The CSIM0n register is an 8-bit register that specifies the operation of CSI0n.

(2) Clocked serial interface clock selection register n (CSICn)

The CSICn register is an 8-bit register that controls the CSI0n serial transfer operation.

(3) Serial I/O shift register 0n (SIO0n)

The SIO0n register is a 16-bit shift register that converts parallel data into serial data.
The SIO0n register is used for both transmission and reception.
Data is shifted in (reception) and shifted out (transmission) from the MSB or LSB side.
The actual transmission/reception operations are started up by accessing the buffer register.

(4) Serial I/O shift register 0nL (SIO0nL)

The SIO0nL register is an 8-bit shift register that converts parallel data into serial data.
The SIO0nL register is used for both transmission and reception.
Data is shifted in (reception) and shifted out (transmission) from the MSB or LSB side.
The actual transmission/reception operations are started up by access of the buffer register .

(5) Clocked serial interface receive buffer register n (SIRBn)

The SIRBn register is a 16-bit buffer register that stores receive data.

(6) Clocked serial interface receive buffer register nL (SIRBnL)

The SIRBnL register is an 8-bit buffer register that stores receive data.

(7) Clocked serial interface read-only receive buffer register n (SIRBEn)

The SIRBEn register is a 16-bit buffer register that stores receive data.
The SIRBEn register is the same as the SIRBn register. It is used to read the contents of the SIRBn register.

(8) Clocked serial interface read-only receive buffer register nL (SIRBEnL)

The SIRBEnL register is an 8-bit buffer register that stores receive data.
The SIRBEnL register is the same as the SIRBnL register. It is used to read the contents of the SIRBnL register.

(9) Clocked serial interface transmit buffer register n (SOTBn)

The SOTBn register is a 16-bit buffer register that stores transmit data.

(10) Clocked serial interface transmit buffer register nL (SOTBLnL)

The SOTBnL register is an 8-bit buffer register that stores transmit data.

(11) Clocked serial interface initial transmit buffer register n (SOTBFn)

The SOTBFn register is a 16-bit buffer register that stores the initial transmit data in the continuous transfer mode.

(12) Clocked serial interface initial transmit buffer register nL (SOTBFnL)

The SOTBFnL register is an 8-bit buffer register that stores initial transmit data in the continuous transfer mode.

(13) Selector

The selector selects the serial clock to be used.

(14) Serial clock controller

Controls the serial clock supply to the shift register. Also controls the clock output to the $\overline{\text{SCK0n}}$ pin when the internal clock is used.

(15) Serial clock counter

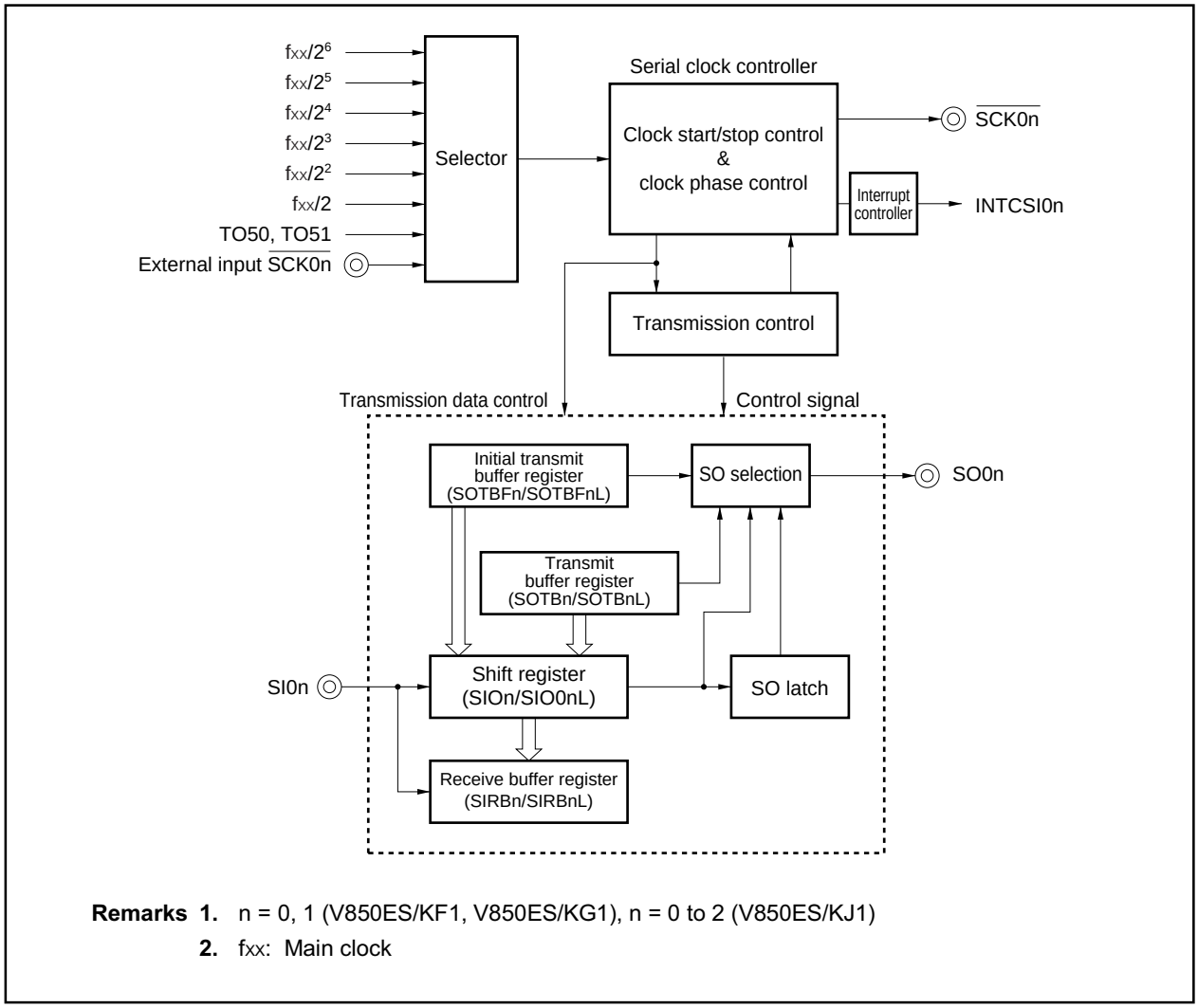
Counts the serial clock output or input during transmission/reception, and checks whether 8-bit or 16-bit data transmission/reception has been performed.

(16) Interrupt controller

Controls the interrupt request timing.

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

Figure 16-1. Block Diagram of Clocked Serial Interface



Remarks 1. n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

2. fxx: Main clock

16.3 Registers

(1) Clocked serial interface mode register 0n (CSIM0n)

The CSIM0n register controls the CSI0n operation.

These registers can be read/written in 8-bit or 1-bit units (however, bit 0 is read-only).

After reset, CSIM0n is cleared to 00H.

Caution Overwriting the TRMDn, CCLn, DIRn, CSITn, and AUTOn bits of the CSIM0n register can be done only when the CSOTn bit = 0. If these bits are overwritten at any other time, the operation cannot be guaranteed.

After reset: 00H R/W Address: FFFFFD00H, FFFFFD10H, FFFFFD20H

	<7>	<6>	5	<4>	3	2	1	<0>
CSIM0n	CSI0En	TRMDn	CCLn	DIRn	CSITn	AUTOn	0	CSOTn

CSI0En	CSI0n operation enable/disable
0	Disable CSI0n operation.
1	Enable CSI0n operation.
The internal CSI0n circuit can be reset[Note] asynchronously by setting the CSI0En bit to 0. For the $\overline{\text{SCK0n}}$ and SO0n pin output status when the CSI0En bit = 0, refer to **16.5 Output Pins**.	

TRMDn	Specification of transmission/reception mode
0	Receive-only mode
1	Transmission/reception mode
When the TRMDn bit = 0, reception is performed and the SO0n pin outputs a low level. Data reception is started by reading the SIRBn register. When the TRMDn bit = 1, transmission/reception is started by writing data to the SOTBn register.	

CCLn	Specification of data length
0	8 bits
1	16 bits

DIRn	Specification of transfer direction mode (MSB/LSB)
0	First bit of transfer data is MSB
1	First bit of transfer data is LSB

CSITn	Control of delay of interrupt request signal
0	No delay
1	Delay mode (interrupt request signal is delayed 1/2 cycle compared to the serial clock)
The delay mode (CSITn bit = 1) is valid only in the master mode (CKS0n2 to CSK0n0 bits of the CSICn register are not 111B). In the slave mode (CKS0n2 to CKS0n0 bits are 111B), do not set the delay mode.	

AUTOn	Specification of single transfer mode or continuous transfer mode
0	Single transfer mode
1	Continuous mode

CSOTn	Communication status flag
0	Communication stopped
1	Communication in progress
The CSOTn bit is cleared (0) by writing 0 to the CSI0En bit.	

Note The SIRBn, SIRBnL, SIRBE, SIRBEnL, SIOn, and SIOnL registers and the CSOTn bit of the CSIMOn register are reset.

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

(2) Clocked serial interface clock selection register n (CSICn)

The CSICn register is an 8-bit register that controls the CSI0n transfer operation.

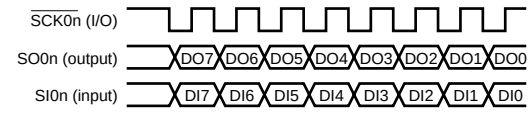
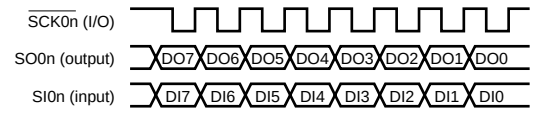
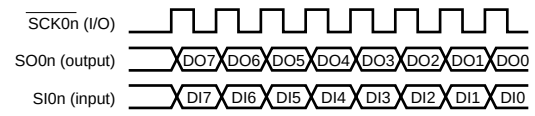
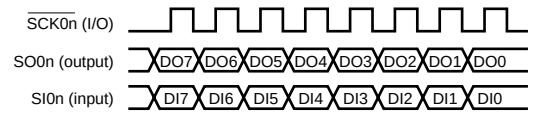
This register can be read/written in 8-bit or 1-bit units.

After reset, CSICn is cleared to 00H.

Caution The CSICn register can be overwritten only when the CSI0En bit of the CSIM0n register = 0.

After reset: 00H R/W Address: FFFFFD01H, FFFFFD11H, FFFFFD21H

	7	6	5	4	3	2	1	0
CSICn	0	0	0	CKPn	DAPn	CKS0n2	CKS0n1	CKS0n0

CKPn	DAPn	Specification of timing of transmitting/receiving data to/from $\overline{SCK0n}$
0	0	(Type 1) 
0	1	(Type 2) 
1	0	(Type 3) 
1	1	(Type 4) 

CKS0n2	CKS0n1	CKS0n0	Serial clock	Mode
0	0	0	$f_{XX}/2$ Note 1	Master mode
0	0	1	$f_{XX}/2^2$	Master mode
0	1	0	$f_{XX}/2^3$	Master mode
0	1	1	$f_{XX}/2^4$	Master mode
1	0	0	$f_{XX}/2^5$	Master mode
1	0	1	$f_{XX}/2^6$	Master mode
1	1	0	Clock generated by TO50, TO51 Note 2	Master mode
1	1	1	External clock ($\overline{SCK0n}$)	Slave mode

Notes 1. Selectable when $f_{XX} \leq 10$ MHz

2. CSI00: TO50
CSI01: TO51
CSI02: TO51

Remarks 1. f_{XX}: Main clock frequency

2. n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

(3) Clocked serial interface receive buffer registers n, nL (SIRBn, SIRBnL)

The SIRBn register is a 16-bit buffer register that stores receive data.

When the receive-only mode is set (TRMDn bit of CSIM0n register = 0), the reception operation is started by reading data from the SIRBn register.

This register is read-only in 16-bit units. When the lower 8 bits are used as the SIRBnL register, this register is read-only in 8-bit units.

In addition to reset input, this register can also be initialized by clearing (0) the CSI0En bit of the CSIM0n register.

Cautions 1. Read the SIRBn register only when a 16-bit data length has been set (CCLn bit of CSIM0n register = 1).

Read the SIRBnL register only when an 8-bit data length has been set (CCLn bit of CSIM0n register = 0).

2. When the single transfer mode has been set (AUTOn bit of CSIM0n register = 0), perform a read operation only in the idle state (CSOTn bit of CSIM0n register = 0). If the SIRBn register is read during data transfer, the data cannot be guaranteed.

(a) SIRBn register

After reset: 0000H R Address: FFFFFD02H, FFFFFD12H, FFFFFD22H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIRBn	SIRBn 15	SIRBn 14	SIRBn 13	SIRBn 12	SIRBn 11	SIRBn 10	SIRBn 9	SIRBn 8	SIRBn 7	SIRBn 6	SIRBn 5	SIRBn 4	SIRBn 3	SIRBn 2	SIRBn 1	SIRBn 0

(b) SIRBnL register

After reset: 00H R Address: FFFFFD02H, FFFFFD12H, FFFFFD22H

	7	6	5	4	3	2	1	0
SIRBnL	SIRBn7	SIRBn6	SIRBn5	SIRBn4	SIRBn3	SIRBn2	SIRBn1	SIRBn0

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

(4) Clocked serial interface read-only receive buffer registers n, nL (SIRBEn, SIRBEnL)

The SIRBEn register is a 16-bit buffer register that stores receive data.

This register is read-only in 16-bit units. However, when the lower 8 bits are used as the SIRBEnL register, the register is read-only in 8-bit units.

In addition to reset input, this register can also be initialized by clearing (0) the CSI0En bit of the CSIM0n register.

The SIRBEn register is the same as the SIRBn register. Even if the SIRBn register is read, the next operation will not start. The SIRBEn register is used to read the contents of the SIRBn register.

Cautions 1. The receive operation is not started even if data is read from the SIRBEn register.

2. The SIRBEn register can be read only if a 16-bit data length is set (CCLn bit of CSIM0n register = 1).

The SIRBEnL register can be read only if an 8-bit data length has been set (CCLn bit of CSIM0n register = 0).

(a) SIRBEn register

After reset: 0000H R Address: FFFFFD06H, FFFFFD16H, FFFFFD26H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIRBEn	SIRBEn 15	SIRBEn 14	SIRBEn 13	SIRBEn 12	SIRBEn 11	SIRBEn 10	SIRBEn 9	SIRBEn 8	SIRBEn 7	SIRBEn 6	SIRBEn 5	SIRBEn 4	SIRBEn 3	SIRBEn 2	SIRBEn 1	SIRBEn 0

(B) SIRBEnL register

After reset: 00H R Address: FFFFFD06H, FFFFFD16H, FFFFFD26H

	7	6	5	4	3	2	1	0
SIRBEnL	SIRBEn7	SIRBEn6	SIRBEn5	SIRBEn4	SIRBEn3	SIRBEn2	SIRBEn1	SIRBEn0

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

(5) Clocked serial interface transmit buffer registers n, nL (SOTBn, SOTBnL)

The SOTBn register is a 16-bit buffer register that stores transmit data.

When the transmission/reception mode is set (TRMDn bit of CSIM0n register = 1), the transmission operation is started by writing data to the SOTBn register.

This register can be read/written in 16-bit units. However, when the lower 8 bits are used as the SOTBnL register, the register is read-only in 8-bit units.

Cautions 1. Access the SOTBn register only when a 16-bit data length is set (CCLn bit of CSIM0n register = 1).

Access the SOTBnL register only when an 8-bit data length has been set (CCLn bit of CSIM0n register = 0).

2. When the single transfer mode is set (AUTOn bit of CSIM0n register = 0), perform access only in the idle state (CSOTn bit of CSIM0n register = 0). If the SOTBn register is accessed during data transfer, the data cannot be guaranteed.

(a) SOTBnL register

After reset: 0000H R/W Address: FFFFFD04H, FFFFFD14H, FFFFFD24H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOTBn	SOTBn 15	SOTBn 14	SOTBn 13	SOTBn 12	SOTBn 11	SOTBn 10	SOTBn 9	SOTBn 8	SOTBn 7	SOTBn 6	SOTBn 5	SOTBn 4	SOTBn 3	SOTBn 2	SOTBn 1	SOTBn 0

(b) SOTBnL register

After reset: 00H R/W Address: FFFFFD04H, FFFFFD14H, FFFFFD24H

	7	6	5	4	3	2	1	0
SOTBnL	SOTBn7	SOTBn6	SOTBn5	SOTBn4	SOTBn3	SOTBn2	SOTBn1	SOTBn0

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

(6) Clocked serial interface initial transmit buffer registers n, nL (SOTBFn, SOTBFnL)

The SOTBFn register is a 16-bit buffer register that stores initial transmission data in the continuous transfer mode.

The transmission operation is not started even if data is written to the SOTBFn register.

This register can be read/written in 16-bit units. However, when the lower 8 bits are used as the SOTBFnL register, the register can be read/written in 8-bit units.

Caution Access the SOTBFn register and SOTBFnL register only when a 16-bit data length has been set (CCLn bit of CSIM0n register = 1), and only when an 8-bit data length has been set (CCLn bit of CSIM0n register = 0), respectively, and only in the idle state (CSOTn bit of CSIM0n register = 0). If the SOTBFn register is accessed during data transfer, the data cannot be guaranteed.

(a) SOTBFn register

After reset: 0000H R/W Address: FFFFFD08H, FFFFFD18H, FFFFFD28H

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SOTBFn	SOTBFn 15	SOTBFn 14	SOTBFn 13	SOTBFn 12	SOTBFn 11	SOTBFn 10	SOTBFn 9	SOTBFn 8	SOTBFn 7	SOTBFn 6	SOTBFn 5	SOTBFn 4	SOTBFn 3	SOTBFn 2	SOTBFn 1	SOTBFn 0

(b) SOTBFnL register

After reset: 00H R/W Address: FFFFFD08H, FFFFFD18H, FFFFFD28H

	7	6	5	4	3	2	1	0
SOTBFnL	SOTBFn7	SOTBFn6	SOTBFn5	SOTBFn4	SOTBFn3	SOTBFn2	SOTBFn1	SOTBFn0

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

(7) Serial I/O shift registers n, nL (SIO0n, SIO0nL)

The SIO0n register is a 16-bit shift register that converts parallel data into serial data.

The transfer operation is not started even if the SIO0n register is read.

This register is read-only in 16-bit units. However, when the lower 8 bits are used as the SIO0nL register, the register is read-only in 8-bit units.

In addition to reset input, this register can also be initialized by clearing (0) the CSI0En bit of the CSIM0n register.

Caution Access the SIO0n register and SIO0nL register only when a 16-bit data length has been set (CCLn bit of CSIM0n register = 1), and only when an 8-bit data length has been set (CCLn bit of CSIM0n register = 0), respectively, and only in the idle state (CSOTn bit of CSIM0n register = 0). If the SIO0n register is accessed during data transfer, the data cannot be guaranteed.

(a) SIO0n register

After reset: 0000H R Address: FFFFFD0AH, FFFFFD1AH, FFFFFD2AH

	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SIO0n	SIOn15	SIOn14	SIOn13	SIOn12	SIOn11	SIOn10	SIOn9	SIOn8	SIOn7	SIOn6	SIOn5	SIOn4	SIOn3	SIOn2	SIOn1	SIOn0

(b) SIO0nL register

After reset: 00H R Address: FFFFFD0AH, FFFFFD1AH, FFFFFD2AH

	7	6	5	4	3	2	1	0
SIO0nL	SIOn7	SIOn6	SIOn5	SIOn4	SIOn3	SIOn2	SIOn1	SIOn0

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

Table 16-1. Use of Each Buffer Register ★

Register Name	R/W		Single Transfer		Continuous Transfer[Note 1]	
			Transmission/Reception Mode	Receive-Only Mode	Transmission/Reception Mode	Receive-Only Mode
SIRBn (SirBnL)	Read	Function	Storing received data[Note 2]	• Reading starts reception • Storing received data	Storing up to the (N - 1)th received data (other than the last)[Note 2]	• Reading starts reception • Storing up to the (N - 2)th data (other than the last two)
		Use method	When transmission and reception are complete, read the received data from this register.	• First, read dummy data and start transfer. • To perform reception of the next data after reception is complete, read the received data from this register.	When reception is complete, read the received data from this register. Repeat this operation until the (N - 1)th data has been received.	When reception is complete, read the received data from this register. Repeat this operation until the (N - 2)th data has been received. (Supplement) Do not read the (N - 1)th data from this register. If read, a reception operation starts and continuous transfer cannot be completed.
SIRBEn (SIRBEnL)	Read	Function	–	Storing the data received last[Note 2]	–	Storing the (N - 1)th received data[Note 2]
		Use method	Not used.	If reception of the next data will not be performed after reception is complete, read the received data from this register.	Not used	Read the (N - 1)th received data from this register when the (N - 1)th or Nth (last) data has been received.
SIO0n (SIO0nL)	Read	Function	–	–	Storing the Nth (last) received data[Note 2]	Storing the Nth (last) received data[Note 2]
		Use method	Not used.	Not used	When the Nth (last) transmission/reception is complete, read the Nth (last) data.	When the Nth (last) data has been received, read the Nth (last) data.
SOTBn (SOTBnL)	Write	Function	• Starting transmission/reception when written • Storing the data to be transmitted	–	• Starting transmission/reception when written • Storing the data to be transmitted second and subsequently	–
		Use method	• First, write a dummy data (FFH) to start transmission/reception. • When transmission/reception is complete, write the data to be transmitted next.	Not used	When transmission/reception is complete, write the data to be transmitted next to this register to start the next transmission/reception.	Not used
SOTBFn (SOTBFnL)	Write	Function	–	–	Storing the data to be transmitted first[Note 2]	–
		Use method	Not used	Not used	Before starting transmission/reception (writing to SOTBn), write the data to be transmitted first.	Not used

Notes 1. It is assumed that the number of data to be transmitted is N.

2. Neither reading nor writing will start communication.

Remark In the 16-bit mode, the registers not enclosed in parentheses are used; in the 8-bit mode, the registers in parentheses are used.

16.4 Operation

16.4.1 Transmission/reception completion interrupt request signal (INTCSI0n)

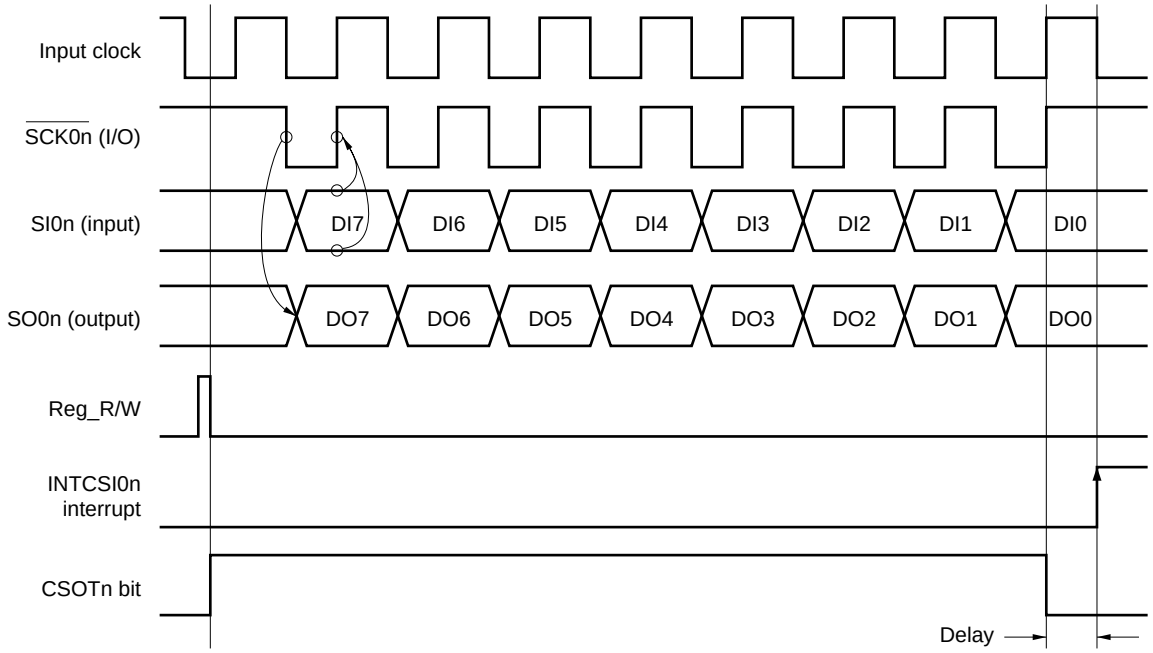
INTCSI0n is set (1) upon completion of data transmission/reception.

Writing to the CSIM0n register also clears (0) INTCSI0n.

Caution The delay mode (CSITn bit = 1) is valid only in the master mode (bits CKS0n2 to CKS0n0 of the CSICn register are not 111B). The delay mode cannot be set when the slave mode is set (bits CKS0n2 to CKS0n0 = 111B).

Figure 16-2. Timing Chart of Interrupt Request Signal Output in Delay Mode (1/2)

(a) Transmit/receive type 1

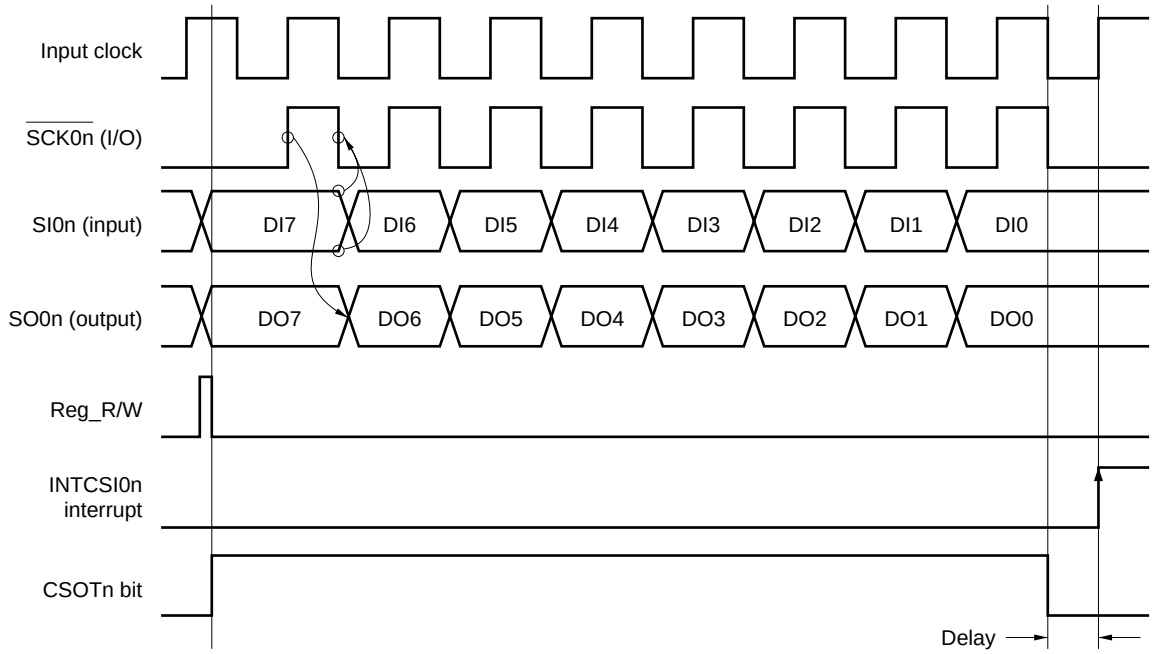


Remarks 1. n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

2. Reg_R/W: Internal signal. This signal indicates that a clocked serial interface receive buffer register n and nL (SIRBn/SIRBnL) read or clocked serial interface transmit buffer register n and nL (SOTBn/SOTBnL) write was performed.

Figure 16-2. Timing Chart of Interrupt Request Signal Output in Delay Mode (2/2)

(b) Transmit/receive type 4



Remarks 1. n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

2. Reg_R/W: Internal signal. This signal indicates that a clocked serial interface receive buffer register n and nL (SIRBn/SIRBnL) read or clocked serial interface transmit buffer register n and nL (SOTBn/SOTBnL) write was performed.

16.4.2 Single transfer mode

(1) Usage

In the receive-only mode (TRMDn bit of CSIM0n register = 0), communication is started by reading clocked serial interface receive buffer registers n and nL (SIRBn/SIRBnL).

In the transmission/reception mode n and nL (TRMDn bit of CSIM0n register = 1), communication is started by writing to clocked serial interface transmit buffer registers n and nL (SOTBn/SOTBnL).

In the slave mode, the operation must be enabled beforehand (CSI0En bit of CSIM0n register = 1).

When communication is started, the value of the CSOTn bit of the CSIM0n register becomes 1 (transmission execution status).

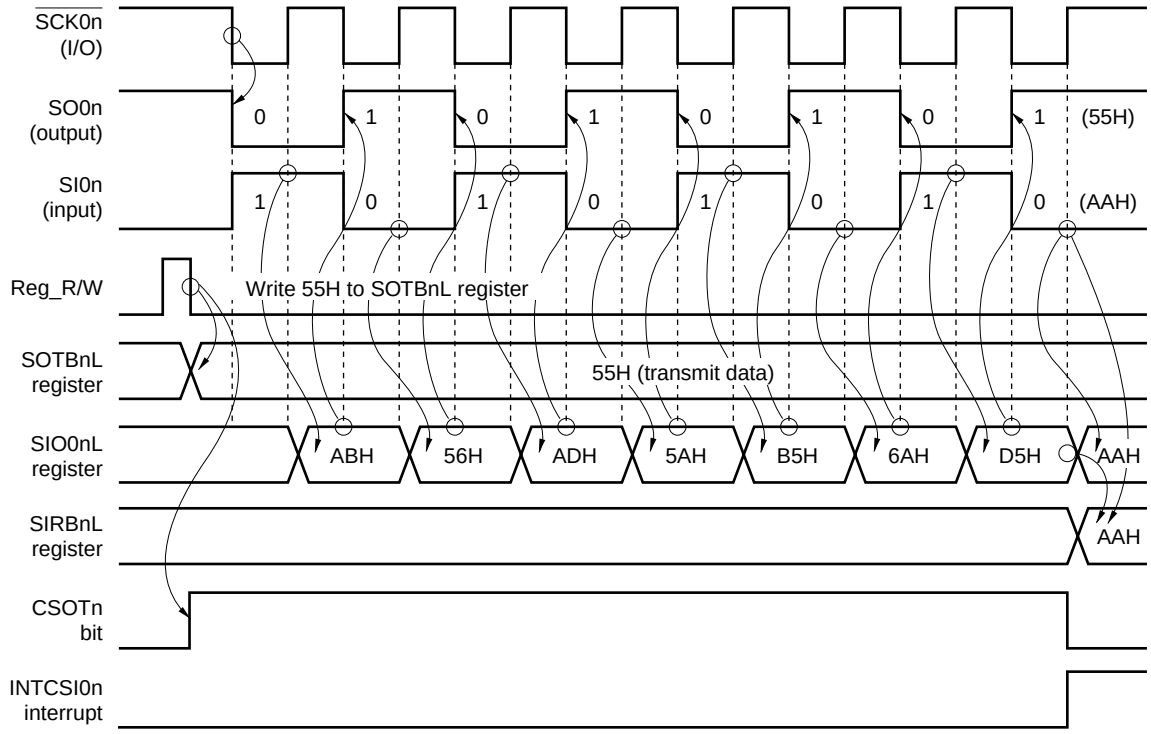
Upon communication completion, the transmission/reception completion interrupt (INTCSI0n) is set (1), and the CSOTn bit is cleared (0). The next data communication request is then waited for.

Caution When the CSOTn bit of the CSIM0n register = 1, do not manipulate the CSI0n register.

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

Figure 16-3. Timing Chart in Single Transfer Mode (1/2)

(a) In transmission/reception mode, data length: 8 bits, transfer direction: MSB first, no interrupt delay, single transfer mode, when AAH is received and 55H is transmitted, transmit/receive type 1



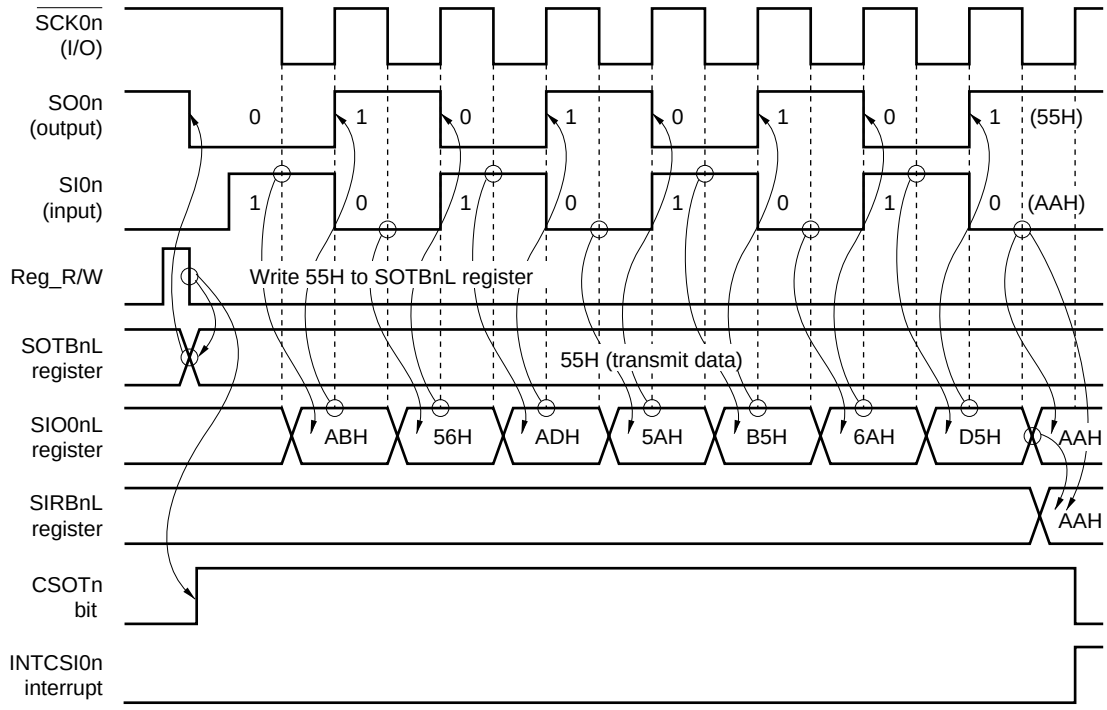
Remarks 1. n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

2. Reg_R/W: Internal signal. This signal indicates that a clocked serial interface receive buffer register n and nL (SIRBn/SIRBnL) read or clocked serial interface transmit buffer register n and nL (SOTBn/SOTBnL) write was performed.

3. For the transmit/receive types, refer to **16.3 (2) Clocked serial interface clock selection register n (CSICn)**.

Figure 16-3. Timing Chart in Single Transfer Mode (2/2)

(b) In transmission/reception mode, data length: 8 bits, transfer direction: MSB first, no interrupt delay, single transfer mode, when AAH is received and 55H is transmitted, transmit/receive type 2



Remarks 1. n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

2. Reg_R/W: Internal signal. This signal indicates that a clocked serial interface receive buffer register n and nL (SIRBn/SIRBnL) read or clocked serial interface transmit buffer register n and nL (SOTBn/SOTBnL) write was performed.

3. For the transmit/receive types, refer to **16.3 (2) Clocked serial interface clock selection register n (CSICn)**.

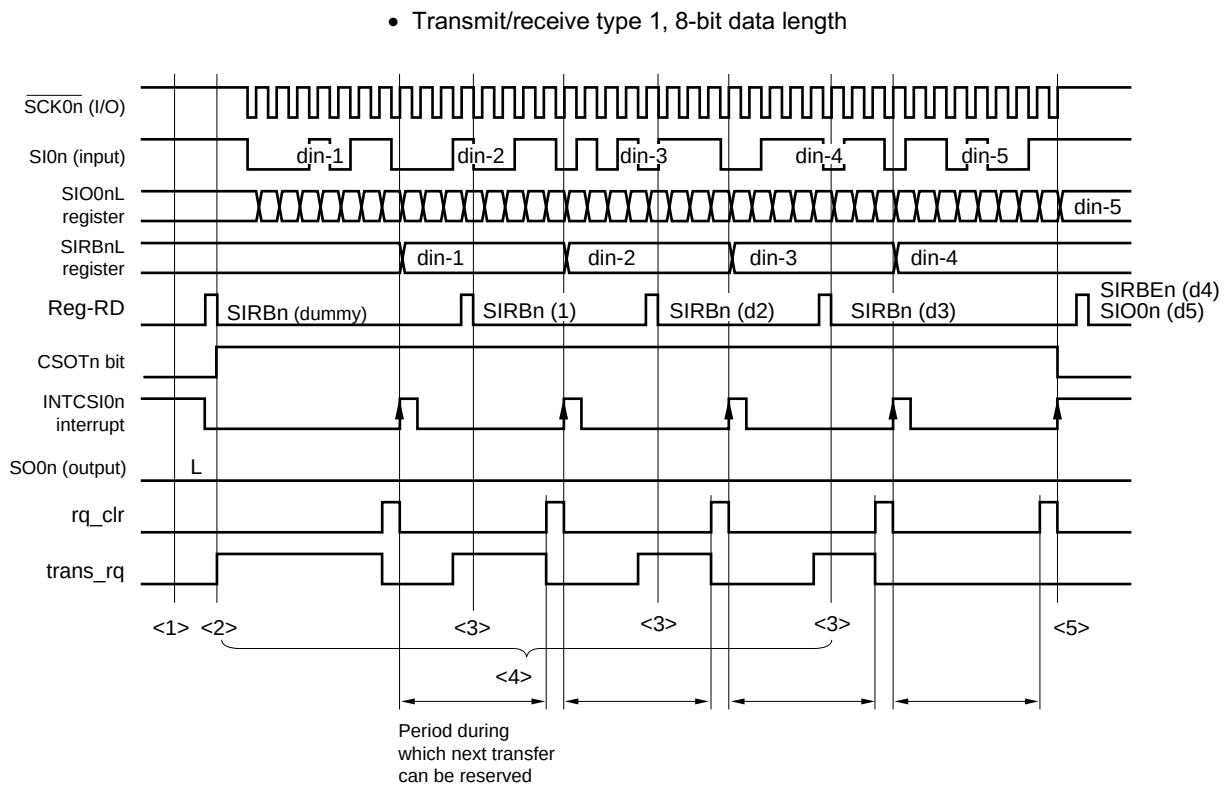
16.4.3 Continuous transfer mode

(1) Usage (receive-only: 8-bit data length)

<1> Set the continuous transfer mode (AUTOn bit of CSIM0n register = 1) and the receive-only mode (TRMDn bit of CSIM0n register = 0).
<2> Read the SIRBnL register (start transfer with dummy read).
<3> When the transmission/reception completion interrupt request (INTCSI0n) has been set (1), read the SIRBnL register[Note] (reserve next transfer).
<4> Repeat step <3> (N – 2) times. (N: Number of transfer data)
Ignore the interrupt triggered by reception of the (N – 1)th data (at this time, the SIRBEnL register can be read).
<5> Following output of the last transmission/reception completion interrupt request (INTCSI0n), read the SIRBEnL register and the SIO0nL register[Note].

Note When transferring N number of data, receive data is loaded by reading the SIRBnL register from the first data to the (N – 2)th data. The (N – 1)th data is loaded by reading the SIRBEnL register, and the Nth (last) data is loaded by reading the SIO0nL register.

Figure 16-4. Continuous Transfer (Receive-Only) Timing Chart



Remarks 1. n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

2. Reg_RD: Internal signal. This signal indicates that clocked serial interface receive buffer register nL (SIRBnL) has been read.

rq_clr: Internal signal. Transfer request clear signal.

trans_rq: Internal signal. Transfer request signal.

In the case of the continuous transfer mode, two transfer requests are set at the start of the first transfer. Following the transmission/reception completion interrupt request (INTCSI0n), transfer is continued if the SIRBnL register can be read within the next transfer reservation period. If the SIRBnL register cannot be read, transfer ends and the SIRBnL register does not receive the new value of the SIO0nL register.

The last data can be obtained by reading the SIO0nL register following completion of the transfer.

(2) Usage (transmission/reception: 8-bit data length)

<1> Set the continuous transfer mode (AUTOn bit of CSIM0n register = 1) and the transmission/reception mode (TRMDn bit of CSIM0n register = 1)

<2> Write the first data to the SOTBFnL register.

<3> Write the 2nd data to the SOTBnL register (start transfer).

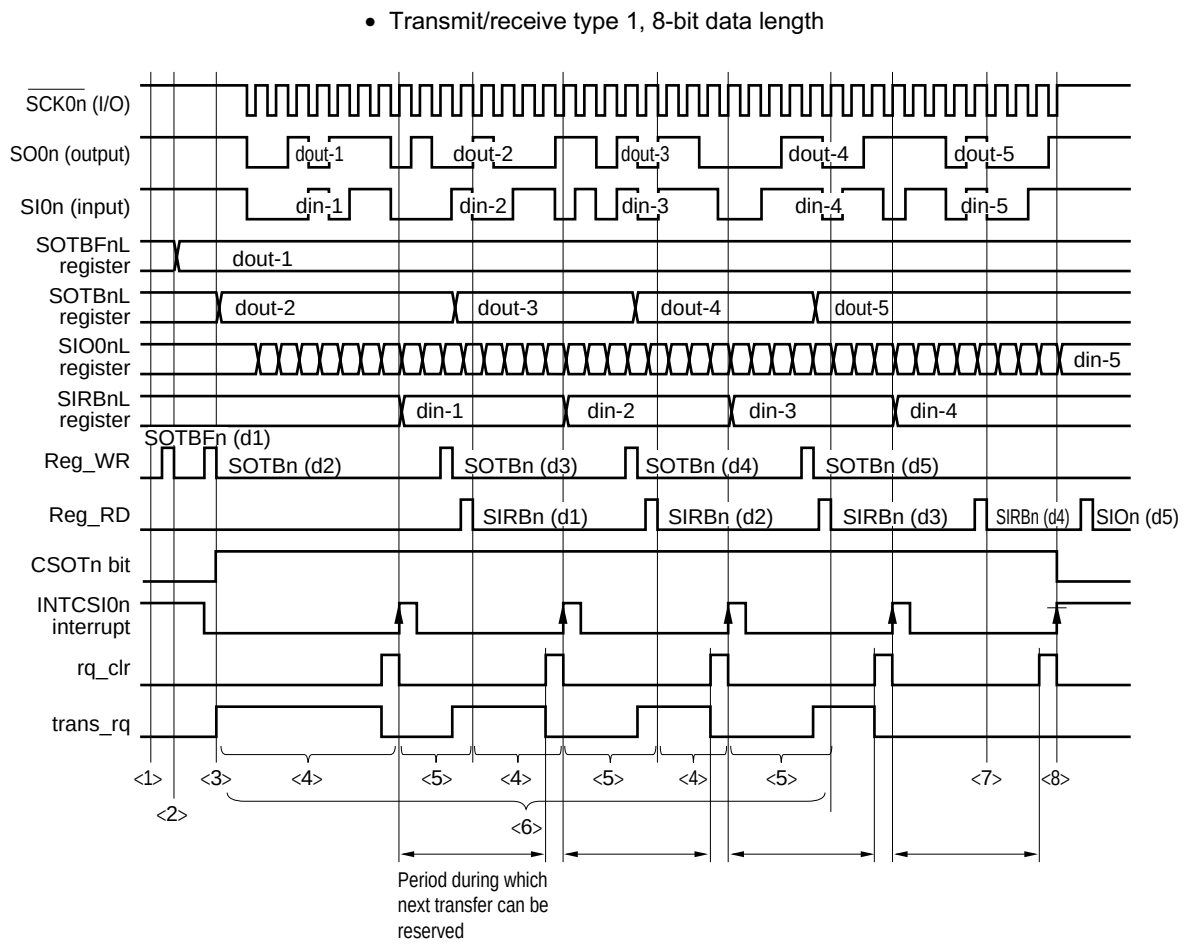
<4> When the transmission/reception completion interrupt request (INTCOSI0n) has been set (1), write the next data to the SOTBnL register (reserve next transfer). Read the SIRBnL register to load the receive data.

<5> Repeat step <4> as long as data to be sent remains.

<6> Wait for the INTCSI0n interrupt. When the interrupt request signal is set (1), read the SIRBnL register to load the (N – 1)th receive data (N: Number of transfer data).

<7> Following the last transmission/reception completion interrupt request (INTCSI0n), read the SIO0nL register to load the Nth (last) receive data.

Figure 16-5. Continuous Transfer (Transmission/Reception) Timing Chart



Remarks 1. n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

2. Reg_WR: Internal signal. This signal indicates that clocked serial interface transmit buffer register nL (SOTBnL) has been written.

Reg_RD: Internal signal. This signal indicates that clocked serial interface receive buffer register nL (SIRBnL) has been read.

rq_clr: Internal signal. Transfer request clear signal.

trans_rq: Internal signal. Transfer request signal.

In the case of the continuous transfer mode, two transfer requests are set at the start of the first transfer. Following the transmission/reception completion interrupt request (INTCSI0n), transfer is continued if the SOTBnL register can be written within the next transfer reservation period. If the SOTBnL register cannot be written, transfer ends and the SIRBnL register does not receive the new value of the SIO0nL register.

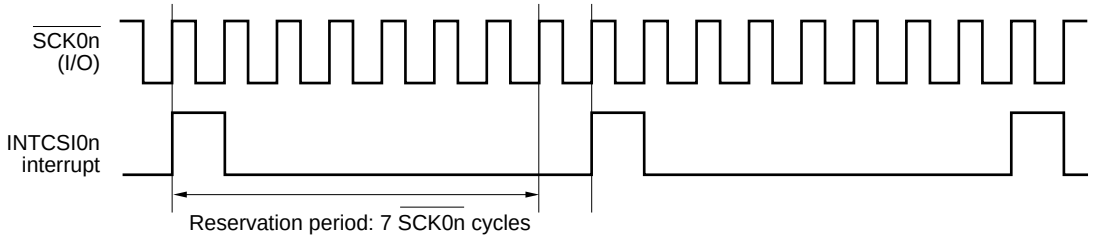
The last receive data can be obtained by reading the SIO0nL register following completion of the transfer.

(3) Next transfer reservation period

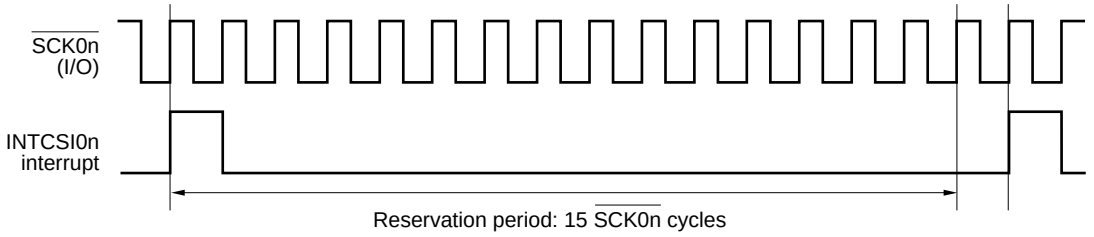
In the continuous transfer mode, the next transfer must be prepared with the period shown in Figure 16-6.

Figure 16-6. Timing Chart of Next Transfer Reservation Period (1/2)

(a) When data length: 8 bits, transmit/receive type 1



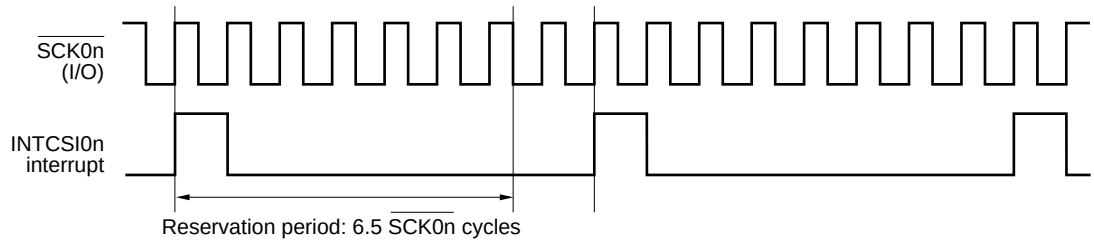
(b) When data length: 16 bits, transmit/receive type 1



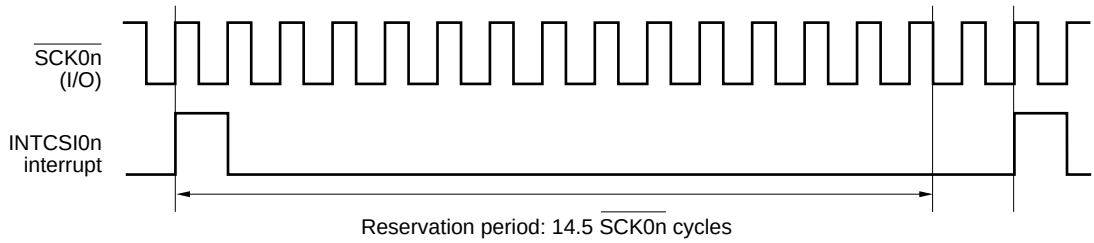
Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

Figure 16-6. Timing Chart of Next Transfer Reservation Period (2/2)

(c) When data length: 8 bits, transmit/receive type 2



(d) When data length: 16 bits, transmit/receive type 2



Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

(4) Cautions

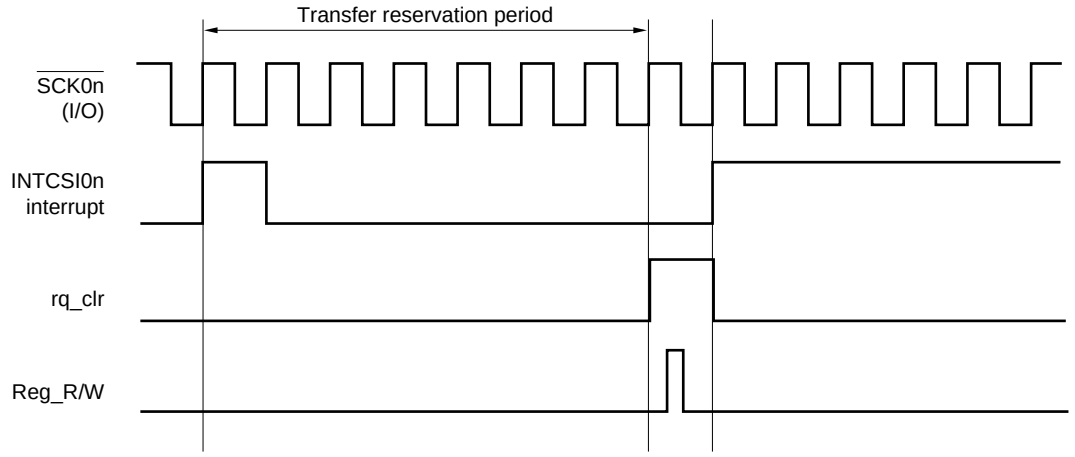
To continue continuous transfers, it is necessary to either read the SIRBn register or write to the SOTBn register during the transfer reservation period.

If access is performed to the SIRBn register or the SOTBn register when the transfer reservation period is over, the following occurs.

(i) In case of conflict between transfer request clear and register access

Since request cancellation has higher priority, the next transfer request is ignored. Therefore, transfer is interrupted, and normal data transfer cannot be performed.

Figure 16-7. Transfer Request Clear and Register Access Conflict



Remarks 1. n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

2. rq_clr: Internal signal. Transfer request clear signal.

Reg_R/W: Internal signal. This signal indicates that a clocked serial interface receive buffer register n and nL (SIRBn/SIRBnL) read or clocked serial interface transmit buffer register n and nL (SOTBn/SOTBnL) write was performed.

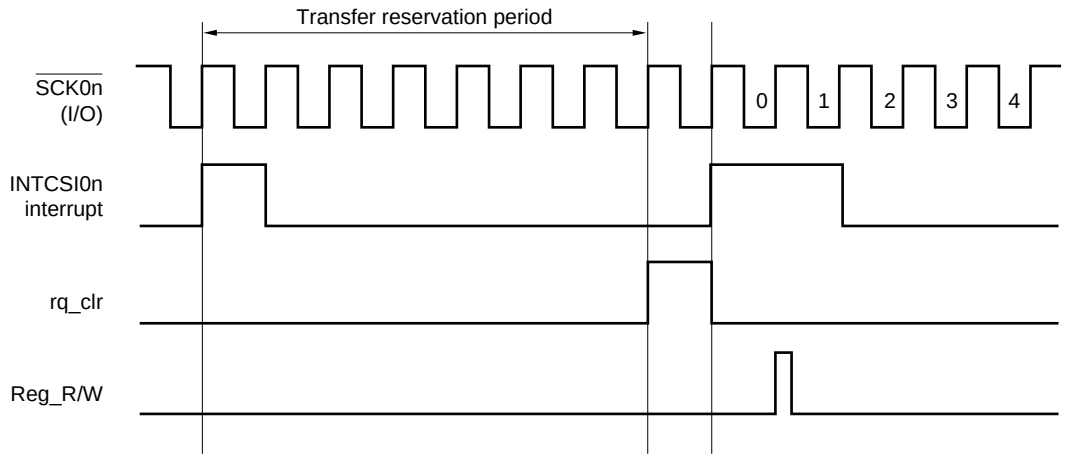
(ii) In case of conflict between interrupt request and register access

Since continuous transfer has stopped once, executed as a new continuous transfer.

In the slave mode, a bit phase error transfer error results (refer to **Figure 16-8**).

In the transmission/reception mode, the value of the SOTBFn register is retransmitted, and illegal data is sent.

Figure 16-8. Interrupt Request and Register Access Conflict



Remarks 1. n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

2. rq_clr: Internal signal. Transfer request clear signal.

Reg_R/W: Internal signal. This signal indicates that a clocked serial interface receive buffer register n and nL (SIRBn/SIRBnL) read or clocked serial interface transmit buffer register n and nL (SOTBn/SOTBnL) write was performed.

16.5 Output Pins

The following describes the output pins. For the setting of each pin, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

(1) $\overline{\text{SCK0n}}$ pin

When the CSI0n operation is disabled (CSI0En bit of CSIM0n register = 0), the $\overline{\text{SCK0n}}$ pin output status is as follows.

Table 16-2. $\overline{\text{SCK0n}}$ Pin Output Status

CKPn	CKS0n2	CKS0n1	CKS0n0	$\overline{\text{SCK0n}}$ Pin Output
0	Don't care	Don't care	Don't care	Fixed to high level
1	1	1	1	Fixed to high level
	Other than above			Fixed to low level

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

(2) SO0n pin

When the CSI0n operation is disabled (CSI0En bit of CSIM0n register = 0), the SO0n pin output status is as follows.

Table 16-3. SO0n Pin Output Status

TRMDn	DAPn	AUTOn	CCLn	DIRn	SO0n Pin Output
0	Don't care	Don't care	Don't care	Don't care	Fixed to low level
1	0	Don't care	Don't care	Don't care	SO latch value (low level)
	1	0	0	0	SOTBn7 bit value
				1	SOTBn0 bit value
			1	0	SOTBn15 bit value
				1	SOTBn0 bit value
		1	0	0	SOTBFn7 bit value
				1	SOTBFn0 bit value
			1	0	SOTBFn15 bit value
				1	SOTBFn0 bit value

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

CHAPTER 17 CLOCKED SERIAL INTERFACE A (CSIA) WITH AUTOMATIC TRANSMIT/RECEIVE FUNCTION

The number of CSIA channels incorporated differs as follows depending on the product.

Product Name	V850ES/KF1	V850ES/KG1	V850ES/KJ1
Number of channels	1 channel (CSIA0)	2 channels (CSIA0, CSIA1)	

17.1 Functions

CSIAn has the following two modes.

- 3-wire serial I/O mode
- 3-wire serial I/O mode with automatic transmit/receive function

(1) 3-wire serial I/O mode

This mode is used to transfer 8-bit data using three lines: a serial clock pin ($\overline{\text{SCKAn}}$) and two serial data pins (SIAn and SOAn).

In addition, whether 8-bit data is transferred MSB or LSB first can be specified, so this interface can be connected to any device.

(2) 3-wire serial I/O mode with automatic transmit/receive function

This mode is used to transfer 8-bit data using three lines: a serial clock pin ($\overline{\text{SCKAn}}$) and two serial data pins (SIAn and SOAn).

In addition, whether 8-bit data is transferred MSB or LSB first can be specified, so this interface can be connected to any device.

Data can be transferred to/from a display driver etc. without using software since a 32-byte transfer buffer RAM is incorporated.

- Master mode/slave mode selectable
- Transfer data length: 8 bits
- MSB/LSB-first selectable for transfer data
- Automatic transmit/receive function:
  Number of transfer bytes can be specified between 1 and 32
  Transfer interval can be specified (0 to 63 clocks)
  Single transfer/repeat transfer selectable
- On-chip dedicated baud rate generator (6/8/16/32 divisions)
- 3-wire SOAn: Serial data output
  SIAn: Serial data input
  $\overline{\text{SCKAn}}$: Serial clock I/O
- Transmission/reception completion interrupt: INTCSIAn
- Internal 32-byte buffer RAM

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

17.2 Configuration

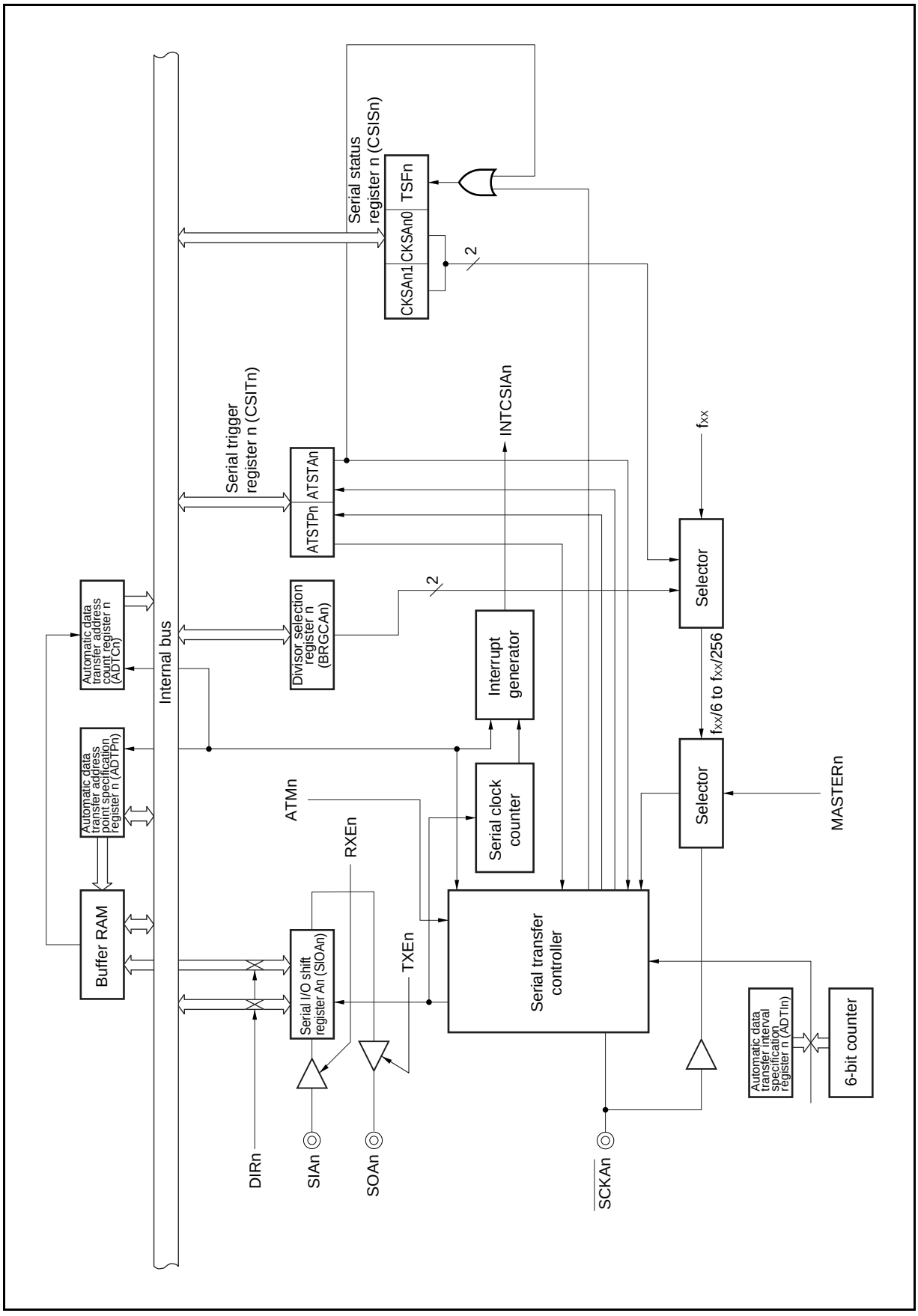
CSIAn consists of the following hardware.

Table 17-1. Configuration of CSIAn

Item	Configuration
Register	Serial I/O shift register An (SIOAn) Automatic data transfer address count register n (ADTCn) CSIAn buffer RAM (CSIAnBm, CSIAnBmL, CSIAnBmH) (m = 0 to F)
Control registers	Serial operation mode specification register n (CSIMAn) Serial status register n (CSISn) Serial trigger register n (CSITn) Divisor selection register n (BRGCAn) Automatic data transfer address point specification register n (ADTPn) Automatic data transfer interval specification register n (ADTIn)

Remark For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

Figure 17-1. Block Diagram of CSIAn



(1) Serial I/O shift register An (SIOAn)

This is an 8-bit register used to store transmit/receive data in 1-byte transfer mode (ATEn bit of serial operation mode specification register n (CSIMAn) = 0). Writing transmit data to SIOAn starts the transfer. In addition, after a transfer completion interrupt request signal (INTCSIAn) is output TSFn bit of serial status register n (CSISn) = 0), data can be received by reading data from SIOAn.

This register can be written or read by an 8-bit memory manipulation instruction. However, writing to the SIOAn register is prohibited when TSFn bit of serial status register n (CSISn) = 1

After reset, this register is cleared to 00H.

Cautions 1. A transfer operation is started by writing to SIOAn register. Consequently, when transmission is disabled (TXEn bit of CSIMAn register = 0), write dummy data to the SIOAn register to start the transfer operation, and then perform a receive operation.

2. Do not write data to SIOAn while the automatic transmit/receive function is operating.

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

(2) Automatic data transfer address count register n (ADTCn)

This is a register used to indicate buffer RAM addresses during automatic transfer. When automatic transfer is stopped, the data position when transfer stopped can be ascertained by reading ADTCn register value.

This register can be set by an 8-bit memory manipulation instruction.

After reset, this register is cleared to 00H. However, reading from ADTCn register is prohibited when TSFn bit of serial status register n (CSISn) = 1.

After reset: 00H R Address: FFFFFD47H, FFFFD57H

	7	6	5	4	3	2	1	0
ADTCn	ADTCn7	ADTCn6	ADTCn5	ADTCn4	ADTCn3	ADTCn2	ADTCn1	ADTCn0

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

17.3 Registers

Serial interface CSIAn is controlled by the following six registers.

- Serial operation mode specification register n (CSIMAn)
- Serial status register n (CSISn)
- Serial trigger register n (CSITn)
- Divisor selection register n (BRGCAn)
- Automatic data transfer address point specification register n (ADTPn)
- Automatic data transfer interval specification register n (ADTIn)

(1) Serial operation mode specification register n (CSIMAn)

This is an 8-bit register used to control the serial transfer operation.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

After reset, sets this register is cleared to 00H.

After reset: 00H R/W Address: FFFFFD40H, FFFFD50H

	<7>	6	5	4	3	2	1	0
CSIMAn	CSIAEn	ATEn	ATMn	MASTERn	TXEn	RXEn	DIRn	0

CSIAEn	CSIAn operation enable/disable control
0	Disable CSIAn operation (SOAn: Low level, $\overline{\text{SCKAn}}$: High level)
1	Enable CSIAn operation

- When CSIAEn = 0, the CSIAn unit is reset[Note] asynchronously.
- When CSIAEn = 0, the CSIAn unit is reset, so to operate CSIAn, first set CSIAEn = 1.
- If the CSIAEn bit is changed from 1 to 0, all the registers and bits shown in Note below are initialized. To set CSIAEn to 1 again, first re-set the registers of the CSIAn unit.
- If the CSIAEn bit is changed from 1 to 0, the buffer RAM value is not held. Also, when the CSIAEn bit is 0, the buffer RAM cannot be accessed.

ATEn	Automatic transfer operation enable/disable control
0	1-byte transfer mode
1	Automatic transfer mode

ATMn	Specification of automatic transfer mode
0	Single transfer mode (stops at address specified with ADTPn register)
1	Repeat transfer mode (Following transfer completion, the ADTCn register is cleared to 00H and transmission starts again.)

MASTERn	Specification of CSIAn master/slave mode
0	Slave mode (synchronized with $\overline{\text{SCKAn}}$ input clock)
1	Master mode (synchronized with internal clock)

TXEn	Transmission enable/disable control
0	Disable transmission (SOAn: Low level)
1	Enable transmission

RXEn	Reception enable/disable control
0	Disable reception
1	Enable reception

DIRn	Specification of transfer data direction
0	MSB first
1	LSB first

Note The ADTCn, CSITn, and SIOAn registers and the TSFn bit of the CSIS register are reset.

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

(2) Serial status register n (CSISn)

This is an 8-bit register used to select the serial clock and to indicate the transfer operation of CSIAn.

This register can be set by a 1-bit or 8-bit memory manipulation instruction.

After reset, this register is cleared to 00H. However, rewriting the CSISn register is prohibited when the TSFn bit is 1.

After reset: 00H R/W Address: FFFFFD41H, FFFFD51H

	7	6	5	4	3	2	1	0
CSISn	CKSAn1	CKSAn0	0	0	0	0	0	TSFn

CKSAn1	CKSAn0	Serial clock (f_{SCKA}) selection[Note]			
			20 MHz	16 MHz	10 MHz
0	0	f_{XX}	Setting prohibited	Setting prohibited	100 ns
0	1	$f_{XX}/2$	100 ns	125 ns	200 ns
1	0	$f_{XX}/4$	200 ns	250 ns	400 ns
1	1	$f_{XX}/8$	400 ns	500 ns	800 ns
Rewriting CSISn is prohibited when the CSIAEn bit of the CSIMAn register is 1.					

TSFn	Transfer status
0	CSIAEn bit of CSIMAn register = 0 At reset input At completion of specified transfer When transfer has been suspended by setting ATSTPn bit of CSITn register to 1
1	From transfer start to completion of specified transfer

Note Set f_{SCKA} so as to satisfy the following conditions.

V_{DD} = 4.0 to 5.5 V: $f_{SCKA} \leq$ 10 MHz

V_{DD} = 2.7 to 4.0: $f_{SCKA} \leq$ 5 MHz

Cautions 1. The TSFn bit is read-only.

2. When the TSFn bit = 1, rewriting the CSIMAn, CSISn, BRGCAn, ADTPn, ADTIn, SIOAn registers is prohibited. However, the transfer buffer RAM can be rewritten.

3. When writing to bits 1 to 5, always write 0.

Remark n = 0 (V850ES/KF1)

n = 0, 1 (V850ES/KG1, V850ES/KJ1)

(3) Serial trigger register n (CSITn)

This is an 8-bit register used to control execution/stop of automatic data transfer.

The CSITn register between the buffer RAM and shift register can be set by an 8-bit or 1-bit memory manipulation instruction.

After reset, this register is cleared to 00H. However, manipulate only when the ATEn bit of serial operation mode specification register n (CSIMAn) is 1 (manipulation prohibited when ATEn bit = 0).

After reset: 00H R/W Address: FFFFFD42H, FFFFD52H

	7	6	5	4	3	2	<1>	<0>
CSITn	0	0	0	0	0	0	ATSTPn	ATSTAn

ATSTPn	Automatic data transfer suspension
0	–
1	Stop automatic data transfer

Even when ATSTPn = 1 is set, transfer does not stop until 1 byte has been transferred. 1 is held until immediately before the INTCSIAn interrupt signal is generated, and ATSTPn is automatically cleared to 0 after that.
After automatic transfer has been suspended, the data address at the point of suspension is stored in automatic data transfer address count register n (ADTCn).
A function to resume automatic data transfer is not provided, so if transfer has been interrupted by setting the ATSTPn bit to 1, set each register again, and set the ATSTAn bit to start automatic data transfer.

ATSTAn	Automatic data transfer start
0	–
1	Start automatic data transfer

Even when ATSTAn = 1, automatic data transfer does not start until 1 byte has been transferred.
1 is held until immediately before the INTCSIAn interrupt signal is generated, and ATSTAn is automatically cleared to 0 after that.

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

(4) Divisor selection register n (BRGCAn)

This is an 8-bit register used to control the serial transfer speed (divisor of CSIA clock).

This register can be set by an 8-bit memory manipulation instruction. However, when the TSFn bit of serial status register n (CSISn) is 1, rewriting the BRGCAn register is prohibited.

After reset, this register is set to 03H.

After reset: 03H R/W Address: FFFFFD43H, FFFFD53H

	7	6	5	4	3	2	1	0
BRGCAn	0	0	0	0	0	0	BRGCn1	BRGCn0

BRGCn1	BRGCn0	Selection of CSIAn serial clock (f_{SCKA} division ratio)
0	0	6 (f_{SCKA}/6)
0	1	8 (f_{SCKA}/8)
1	0	16 (f_{SCKA}/16)
1	1	32 (f_{SCKA}/32)

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

(5) Automatic data transfer address point specification register n (ADTPn)

This is an 8-bit register used to specify the buffer RAM address that ends transfer during automatic data transfer the ATEn bit of serial operation mode specification register n (CSIMAn) = 1).

This register can be set by an 8-bit memory manipulation instruction. However, when the TSFn bit of serial status register n (CSISn) is 1, rewriting the ADTPn register is prohibited.

In the V850ES/KF1, V850ES/KG1, and V850ES/KJ1, 00H to 1FH can be specified because 32 bytes of buffer RAM are incorporated.

Example When the ADTP register is set to 07H
8 bytes of FFFFFFE00H to FFFFFFE07H are transferred.

In repeat transfer mode (ATMn bit of CSIMAn register = 1), transfer is performed repeatedly up to the address value specified by ADTPn.

Example When 07H is set in ADTP0 (repeat transfer mode)
Transfer is repeated as FFFFFFE00H to FFFFFFE07H, … .

After reset: 00H R/W Address: FFFFFD44H, FFFFD54H

	7	6	5	4	3	2	1	0
ADTPn	0	0	0	ADTPn4	ADTPn3	ADTPn2	ADTPn1	ADTPn0

Caution Be sure to set bits 5 to 7 to 0.

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

The relationship between buffer RAM address values and the ADTPn register setting values is shown below.

Table 17-2. Relationship Between Buffer RAM Address Values and ADTP0 Register Setting Values

Buffer RAM Address Value	ADTP0 Register Setting Value	Buffer RAM Address Value	ADTP0 Register Setting Value
FFFFFE00H	00H	FFFFFE10H	10H
FFFFFE01H	01H	FFFFFE11H	11H
FFFFFE02H	02H	FFFFFE12H	12H
FFFFFE03H	03H	FFFFFE13H	13H
FFFFFE04H	04H	FFFFFE14H	14H
FFFFFE05H	05H	FFFFFE15H	15H
FFFFFE06H	06H	FFFFFE16H	16H
FFFFFE07H	07H	FFFFFE17H	17H
FFFFFE08H	08H	FFFFFE18H	18H
FFFFFE09H	09H	FFFFFE19H	19H
FFFFFE0AH	0AH	FFFFFE1AH	1AH
FFFFFE0BH	0BH	FFFFFE1BH	1BH
FFFFFE0CH	0CH	FFFFFE1CH	1CH
FFFFFE0DH	0DH	FFFFFE1DH	1DH
FFFFFE0EH	0EH	FFFFFE1EH	1EH
FFFFFE0FH	0FH	FFFFFE1FH	1FH

Table 17-3. Relationship Between Buffer RAM Address Values and ADTP1 Register Setting Values

Buffer RAM Address Value	ADTP1 Register Setting Value	Buffer RAM Address Value	ADTP1 Register Setting Value
FFFFFE20H	00H	FFFFFE30H	10H
FFFFFE21H	01H	FFFFFE31H	11H
FFFFFE22H	02H	FFFFFE32H	12H
FFFFFE23H	03H	FFFFFE33H	13H
FFFFFE24H	04H	FFFFFE34H	14H
FFFFFE25H	05H	FFFFFE35H	15H
FFFFFE26H	06H	FFFFFE36H	16H
FFFFFE27H	07H	FFFFFE37H	17H
FFFFFE28H	08H	FFFFFE38H	18H
FFFFFE29H	09H	FFFFFE39H	19H
FFFFFE2AH	0AH	FFFFFE3AH	1AH
FFFFFE2BH	0BH	FFFFFE3BH	1BH
FFFFFE2CH	0CH	FFFFFE3CH	1CH
FFFFFE2DH	0DH	FFFFFE3DH	1DH
FFFFFE2EH	0EH	FFFFFE3EH	1EH
FFFFFE2FH	0FH	FFFFFE3FH	1FH

(6) Automatic data transfer interval specification register n (ADTIn)

This is an 8-bit register used to specify the interval period between 1-byte transfers during automatic data transfer (ATEn bit of serial operation mode specification register n (CSIMAn) = 1).

Set this register when in master mode (MASTERn bit of CSIMAn register = 1) (setting is unnecessary in slave mode). Setting in 1-byte transfer mode (ATEn bit of CSIMAn = 0) is also valid. When the interval time specified by the ADTIn register after the end of 1-byte transfer has elapsed, an interrupt request signal (INTCSIAn) is output. The number of clocks for the interval can be set to between 0 and 63 clocks.

The specified interval time is the transfer clock (specified by divisor selection register n (BRGCAn)) multiplied by an integer value.

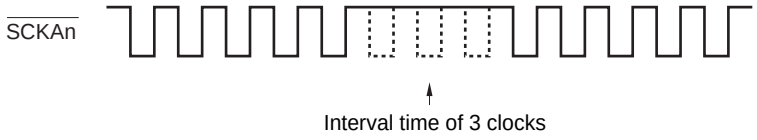
After reset: 00H R/W Address: FFFFFD45H, FFFFD55H

	7	6	5	4	3	2	1	0
ADTIn	0	0	ADTIn5	ADTIn4	ADTIn3	ADTIn2	ADTIn1	ADTIn0

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

This register can be set by an 8-bit memory manipulation instruction. However, when the TSFn bit of serial status register n (CSISn) is 1, rewriting the ADTIn register is prohibited.

Example When ADTIn register = 03H



(7) CSIAn buffer RAM (CSIAnBm)

This area holds transmit/receive data (up to 32 bytes) in automatic transfer mode in 1-bit units.

The CSIAnBm register can be read/written in 16-bit units only. However, when the higher 8 bits and the lower 8 bits of the CSIAnBm register are used as the CSIAnBmH register and CSIAnBmL register, respectively, these registers can be read/written in 8-bit units.

After automatic transfer is started, only data equal to one byte more than the number of bytes stored in the ADTPn register is transmitted/received in sequence from the CSIAmB0L register.

Caution When the main clock stops and the CPU operates on the subclock, do not access the ASISn register.
For details, refer to 3.4.8 (2).

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)
m = 0 to F

Table 17-4. CSIA0 Buffer RAM

Address	Symbol	R/W	Manipulatable Bits		After Reset
			8	16	
FFFFFE00H	CSIA0B0	R/W		√	Undefined
FFFFFE00H	CSIA0B0L	R/W	√		Undefined
FFFFFE01H	CSIA0B0H	R/W	√		Undefined
FFFFFE02H	CSIA0B1	R/W		√	Undefined
FFFFFE02H	CSIA0B1L	R/W	√		Undefined
FFFFFE03H	CSIA0B1H	R/W	√		Undefined
FFFFFE04H	CSIA0B2	R/W		√	Undefined
FFFFFE04H	CSIA0B2L	R/W	√		Undefined
FFFFFE05H	CSIA0B2H	R/W	√		Undefined
FFFFFE06H	CSIA0B3	R/W		√	Undefined
FFFFFE06H	CSIA0B3L	R/W	√		Undefined
FFFFFE07H	CSIA0B3H	R/W	√		Undefined
FFFFFE08H	CSIA0B4	R/W		√	Undefined
FFFFFE08H	CSIA0B4L	R/W	√		Undefined
FFFFFE09H	CSIA0B4H	R/W	√		Undefined
FFFFFE0AH	CSIA0B5	R/W		√	Undefined
FFFFFE0AH	CSIA0B5L	R/W	√		Undefined
FFFFFE0BH	CSIA0B5H	R/W	√		Undefined
FFFFFE0CH	CSIA0B6	R/W		√	Undefined
FFFFFE0CH	CSIA0B6L	R/W	√		Undefined
FFFFFE0DH	CSIA0B6H	R/W	√		Undefined
FFFFFE0EH	CSIA0B7	R/W		√	Undefined
FFFFFE0EH	CSIA0B7L	R/W	√		Undefined
FFFFFE0FH	CSIA0B7H	R/W	√		Undefined
FFFFFE10H	CSIA0B8	R/W		√	Undefined
FFFFFE10H	CSIA0B8L	R/W	√		Undefined
FFFFFE11H	CSIA0B8H	R/W	√		Undefined
FFFFFE12H	CSIA0B9	R/W		√	Undefined
FFFFFE12H	CSIA0B9L	R/W	√		Undefined
FFFFFE13H	CSIA0B9H	R/W	√		Undefined
FFFFFE14H	CSIA0BA	R/W		√	Undefined
FFFFFE14H	CSIA0BAL	R/W	√		Undefined
FFFFFE15H	CSIA0BAH	R/W	√		Undefined
FFFFFE16H	CSIA0BB	R/W		√	Undefined
FFFFFE16H	CSIA0BBL	R/W	√		Undefined
FFFFFE17H	CSIA0BBH	R/W	√		Undefined
FFFFFE18H	CSIA0BC	R/W		√	Undefined
FFFFFE18H	CSIA0BCL	R/W	√		Undefined
FFFFFE19H	CSIA0BCH	R/W	√		Undefined
FFFFFE1AH	CSIA0BD	R/W		√	Undefined
FFFFFE1AH	CSIA0BDL	R/W	√		Undefined
FFFFFE1BH	CSIA0BDH	R/W	√		Undefined
FFFFFE1CH	CSIA0BE	R/W		√	Undefined
FFFFFE1CH	CSIA0BEL	R/W	√		Undefined
FFFFFE1DH	CSIA0BEH	R/W	√		Undefined
FFFFFE1EH	CSIA0BF	R/W		√	Undefined
FFFFFE1EH	CSIA0BFL	R/W	√		Undefined
FFFFFE1FH	CSIA0BFH	R/W	√		Undefined

Table 17-5. CSIA1 Buffer RAM

Address	Symbol	R/W	Manipulatable Bits		After Reset
			8	16	
FFFFFE20H	CSIA1B0	R/W		√	Undefined
FFFFFE20H	CSIA1B0L	R/W	√		Undefined
FFFFFE21H	CSIA1B0H	R/W	√		Undefined
FFFFFE22H	CSIA1B1	R/W		√	Undefined
FFFFFE22H	CSIA1B1L	R/W	√		Undefined
FFFFFE23H	CSIA1B1H	R/W	√		Undefined
FFFFFE24H	CSIA1B2	R/W		√	Undefined
FFFFFE24H	CSIA1B2L	R/W	√		Undefined
FFFFFE25H	CSIA1B2H	R/W	√		Undefined
FFFFFE26H	CSIA1B3	R/W		√	Undefined
FFFFFE26H	CSIA1B3L	R/W	√		Undefined
FFFFFE27H	CSIA1B3H	R/W	√		Undefined
FFFFFE28H	CSIA1B4	R/W		√	Undefined
FFFFFE28H	CSIA1B4L	R/W	√		Undefined
FFFFFE29H	CSIA1B4H	R/W	√		Undefined
FFFFFE2AH	CSIA1B5	R/W		√	Undefined
FFFFFE2AH	CSIA1B5L	R/W	√		Undefined
FFFFFE2BH	CSIA1B5H	R/W	√		Undefined
FFFFFE2CH	CSIA1B6	R/W		√	Undefined
FFFFFE2CH	CSIA1B6L	R/W	√		Undefined
FFFFFE2DH	CSIA1B6H	R/W	√		Undefined
FFFFFE2EH	CSIA1B7	R/W		√	Undefined
FFFFFE2EH	CSIA1B7L	R/W	√		Undefined
FFFFFE2FH	CSIA1B7H	R/W	√		Undefined
FFFFFE30H	CSIA1B8	R/W		√	Undefined
FFFFFE30H	CSIA1B8L	R/W	√		Undefined
FFFFFE31H	CSIA1B8H	R/W	√		Undefined
FFFFFE32H	CSIA1B9	R/W		√	Undefined
FFFFFE32H	CSIA1B9L	R/W	√		Undefined
FFFFFE33H	CSIA1B9H	R/W	√		Undefined
FFFFFE34H	CSIA1BA	R/W		√	Undefined
FFFFFE34H	CSIA1BAL	R/W	√		Undefined
FFFFFE35H	CSIA1BAH	R/W	√		Undefined
FFFFFE36H	CSIA1BB	R/W		√	Undefined
FFFFFE36H	CSIA1BBL	R/W	√		Undefined
FFFFFE37H	CSIA1BBH	R/W	√		Undefined
FFFFFE38H	CSIA1BC	R/W		√	Undefined
FFFFFE38H	CSIA1BCL	R/W	√		Undefined
FFFFFE39H	CSIA1BCH	R/W	√		Undefined
FFFFFE3AH	CSIA1BD	R/W		√	Undefined
FFFFFE3AH	CSIA1BDL	R/W	√		Undefined
FFFFFE3BH	CSIA1BDH	R/W	√		Undefined
FFFFFE3CH	CSIA1BE	R/W		√	Undefined
FFFFFE3CH	CSIA1BEL	R/W	√		Undefined
FFFFFE3DH	CSIA1BEH	R/W	√		Undefined
FFFFFE3EH	CSIA1BF	R/W		√	Undefined
FFFFFE3EH	CSIA1BFL	R/W	√		Undefined
FFFFFE3F	CSIA1BFH	R/W	√		Undefined

Remark V850ES/KG1, V850ES/KJ1 only

17.4 Operation

CSIAn can be used in the following two modes.

- 3-wire serial I/O mode
- 3-wire serial I/O mode with automatic transmit/receive function

17.4.1 3-wire serial I/O mode

The one-byte data transmission/reception is executed in the mode in which the ATEn bit of serial operation mode specification register n (CSIMAn) is set to 0.

In this mode, communication is executed by using three lines: serial clock ($\overline{\text{SCKAn}}$), serial data output (SOAn), and serial data input (SIAn) pins.

The 3-wire serial I/O mode is controlled by the following three registers.

- Serial operation mode specification register n (CSIMAn)
- Serial status register n (CSISn)
- Divisor selection register n (BRGCAn)

Remark For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

(1) 1-byte transmission/reception communication operation

(a) 1-byte transmission/reception

When the CSIAEn bit and ATEn bit of serial operation mode specification register n (CSIMAn) = 1, 0, respectively, if transfer data is written to serial I/O shift register An (SIOAn), the data is output via the SOA0 pin in synchronization with the $\overline{\text{SCKAn}}$ pin falling edge, and then input via the SIAn pin in synchronization with the falling edge of the $\overline{\text{SCKAn}}$ pin, and stored in the SIOAn register in synchronization with the rising edge 1 clock later.

Data transmission and data reception can be performed simultaneously.

If only reception is to be performed, transfer can only be started by writing a dummy value to the SIOAn register.

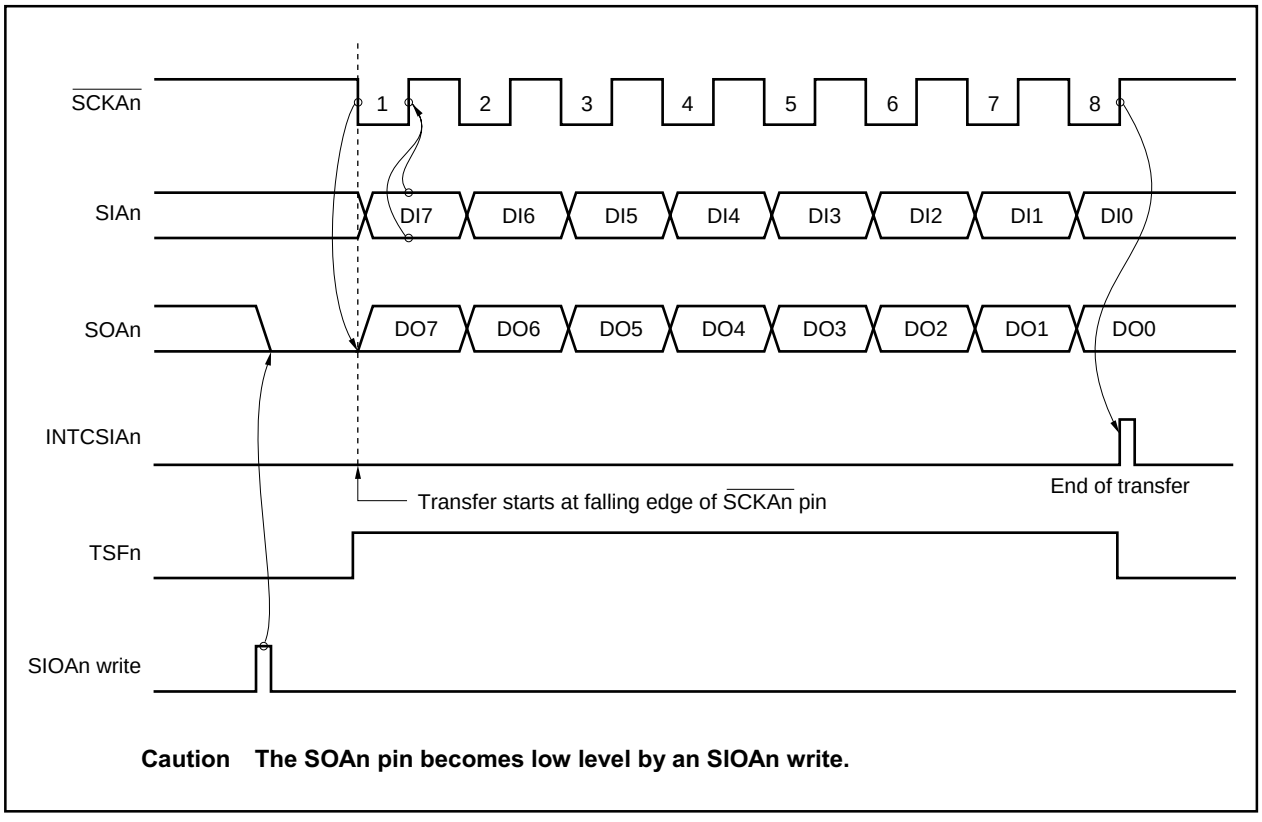
When transfer of 1 byte is complete, an interrupt request signal (INTCSIAn) is generated.

In 1-byte transmission/reception, the setting of the ATMn bit of CSIMAn is invalid.

Be sure to read data after confirming that the TSFn bit of serial status register n (CSISn) = 0.

Caution Determine the setting procedure of alternate-function pins considering the relationship with the communication partner.

Figure 17-2. 3-Wire Serial I/O Mode Timing

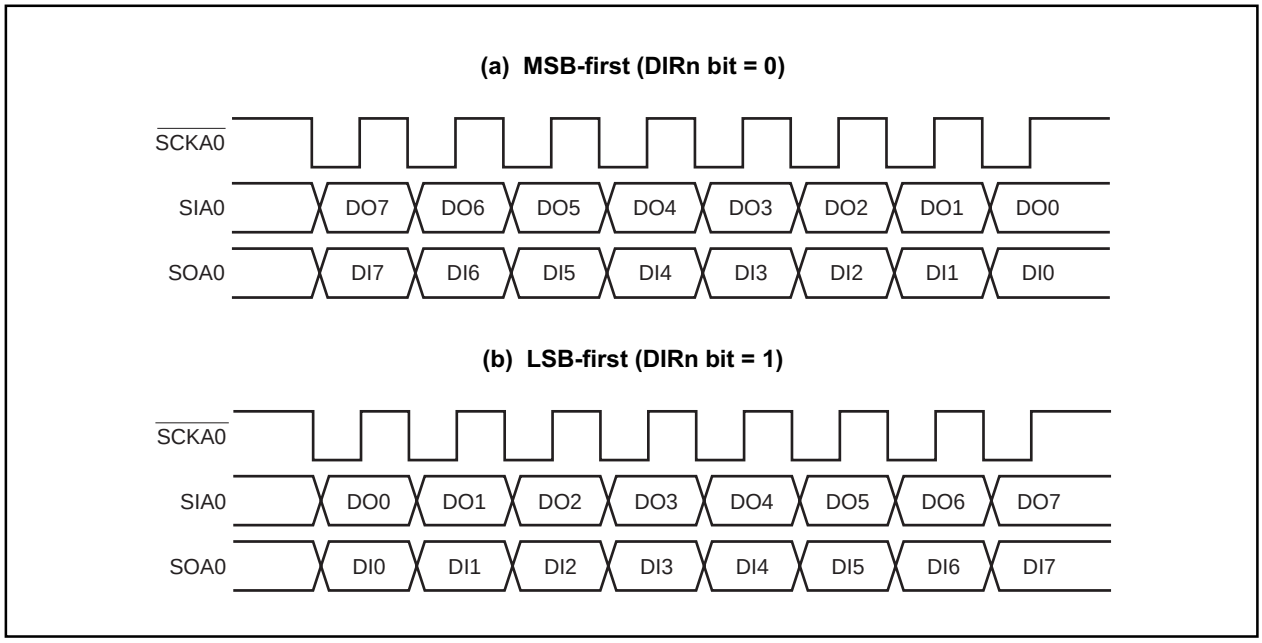


Caution The SOAn pin becomes low level by an SIOAn write.

(b) Data format

In the data format, data is changed in synchronization with the $\overline{\text{SCKAn}}$ pin falling edge as shown below. The data length is fixed to 8 bits and the data transfer direction can be switched by the specification of the DIRn bit of serial operation mode specification register n (CSIMAn).

Figure 17-3. Format of Transmit/Receive Data



(c) Switching MSB/LSB as start bit

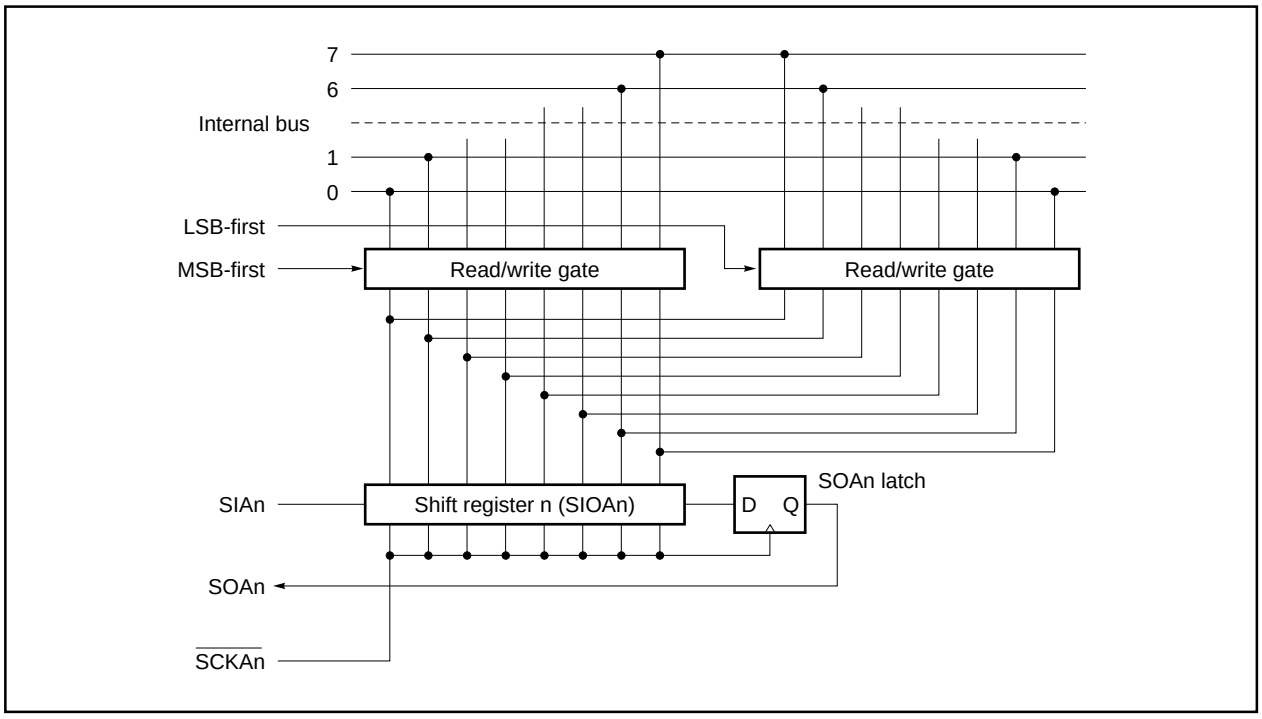
Figure 17-4 shows the configuration of serial I/O shift register n (SIOAn) and the internal bus. As shown in the figure, MSB/LSB can be read/written in reverse form.

Switching MSB/LSB as the start bit can be specified using the DIRn bit of serial operation mode specification register n (CSIMAn).

Start bit switching is realized by switching the bit order for data written to SIOAn. The SIOAn shift order remains unchanged.

Thus, switching between MSB-first and LSB-first must be performed before writing data to the shift register.

Figure 17-4. Transfer Bit Order Switching Circuit



(d) Transfer start

Serial transfer is started by setting transfer data to serial I/O shift register n (SIOAn) when the following two conditions are satisfied.

- Serial interface CSIAn operation control bit (CSIAEn) = 1
- Other than during serial communication

Caution If CSIAEn is set to 1 after data is written to SIOAn, communication does not start.

Upon termination of 8-bit communication, serial communication automatically stops and the interrupt request signal (INTCSIAn) is generated.

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

17.4.2 3-wire serial I/O mode with automatic transmit/receive function

Up to 32 bytes of data can be transmitted/received without using software in the mode in which the ATEn bit of serial operation mode specification register n (CSIMAn) is set to 1. After communication is started, only data of the set number of bytes stored in RAM in advance can be transmitted, and only data of the set number of bytes can be received and stored in RAM.

The 3-wire serial I/O mode with automatic transmit/receive function is controlled by the following registers.

- Serial operation mode specification register n (CSIMAn)
- Serial status register n (CSISn)
- Serial trigger register n (CSITn)
- Divisor selection register n (BRGCAn)
- Automatic data transfer address point specification register n (ADTPn)
- Automatic data transfer interval specification register n (ADTIn)

Remark For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

(1) Automatic transmit/receive data setting

(a) Transmit data setting

<1> Write transmit data from the least significant address FFFFFE00H/FFFFFE20H of buffer RAM (up to FFFFFE1FH/FFFFFE3FH at maximum). The transmit data should be in the order from lower address to higher address.

<2> Set the automatic data transfer address point specification register n (ADTPn) to the value obtained by subtracting 1 from the number of transmit data bytes.

(b) Automatic transmission/reception mode setting

<1> Set the CSIAEn bit and ATEn bit of serial operating mode specification register n (CSIMAn) to 1.
<2> Set the RXEn bit and TXEn bit of the CSIMAn register to 1.
<3> Set a data transfer interval in automatic data transfer interval specification register n (ADTIn).
<4> Set the ATSTAn bit of serial trigger register n (CSITn) to 1.

The following operations are automatically carried out when (a) and (b) are carried out.

- After the buffer RAM data indicated by automatic data transfer address count register n (ADTCn) is transferred to the SIOAn register, transmission is carried out (start of automatic transmission/reception).
- The received data is written to the buffer RAM address indicated by the ADTCn register.
- ADTCn register is incremented and the next data transmission/reception is carried out. Data transmission/reception continues until the ADTCn register incremental output matches the set value of automatic data transfer address point specification register n (ADTPn) (end of automatic transmission/reception). However, if the ATMn bit of CSIMAn is set to 1 (continuous transfer mode), the ADTCn register is cleared after a match between the ADTPn and ADTCn registers, and then repeated transmission/reception is started.
- When automatic transmission/reception is terminated, the TSFn bit is cleared to 0.

Caution Determine the setting procedure of alternate-function pins considering the relationship with the communication partner.

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

(2) Automatic transmission/reception communication operation

(a) Automatic transmission/reception mode

Automatic transmission/reception can be performed using buffer RAM.
The data stored in the buffer RAM is output from the SOAn pin via the SIOAn register in synchronization with the $\overline{\text{SCKAn}}$ pin falling edge by performing (a) and (b) in **(1) Automatic transmit/receive data setting**.
The data is then input from the SIAn pin via the SIOAn register in synchronization with the serial clock falling edge of the SCKAn pin and the receive data is stored in the buffer RAM in synchronization with the rising edge 1 clock later.
Data transfer ends if the TSFn bit of serial status register n (CSISn) is set to 1 when any of the following conditions is met.

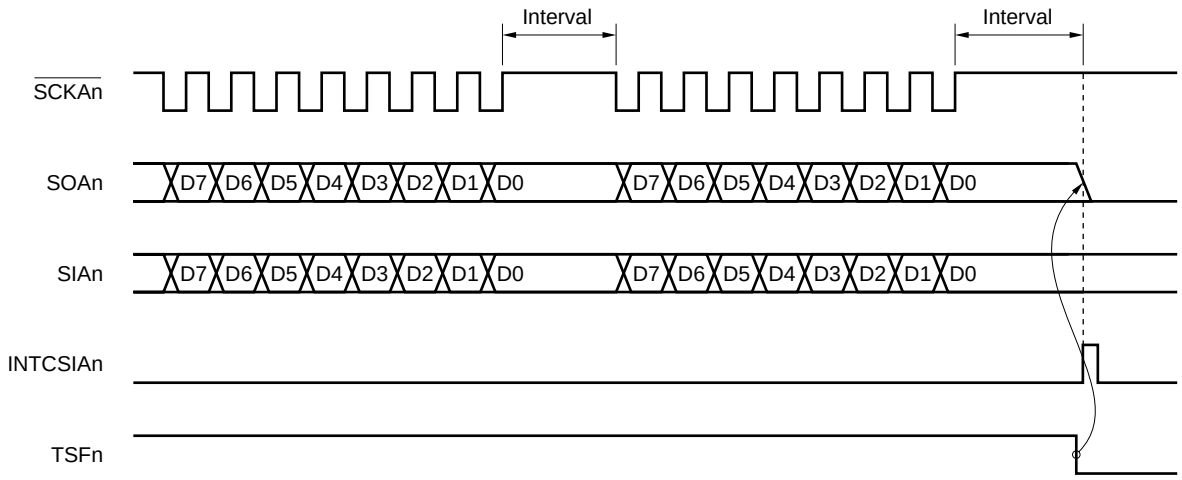
- Reset by setting the CSIAEn bit of the CSIMAn register to 0
- Transfer of 1 byte is complete by setting the ATSTPn bit of the CSITn register to 1
- Transfer of the range specified by the ADTPn register is complete

At this time, an interrupt request signal (INTCSIAn) is generated except when the CSIAEn bit = 0.

If a transfer is terminated in the middle, transfer starting from the remaining data is not possible. Read automatic data transfer address count register n (ADTCn) to confirm how much of the data has already been transferred, set the transfer data again, and perform (a) and (b) in (1) Automatic transmit/receive data setting.

Figure 17-5 shows the operation timing in automatic transmission/reception mode and Figure 17-6 shows the operation flowchart. Figure 17-7 shows the operation of internal buffer RAM when 6 bytes of data are transmitted/received.

Figure 17-5. Automatic Transmission/Reception Mode Operation Timings



Cautions 1. Because, in the automatic transmission/reception mode, the automatic transmit/receive function reads/writes data from/to the internal buffer RAM after 1-byte transmission/reception, an interval is inserted until the next transmission/reception. As the buffer RAM read/write is performed at the same time as CPU processing, the interval is dependent upon the value of automatic data transfer interval specification register n (ADTIn).

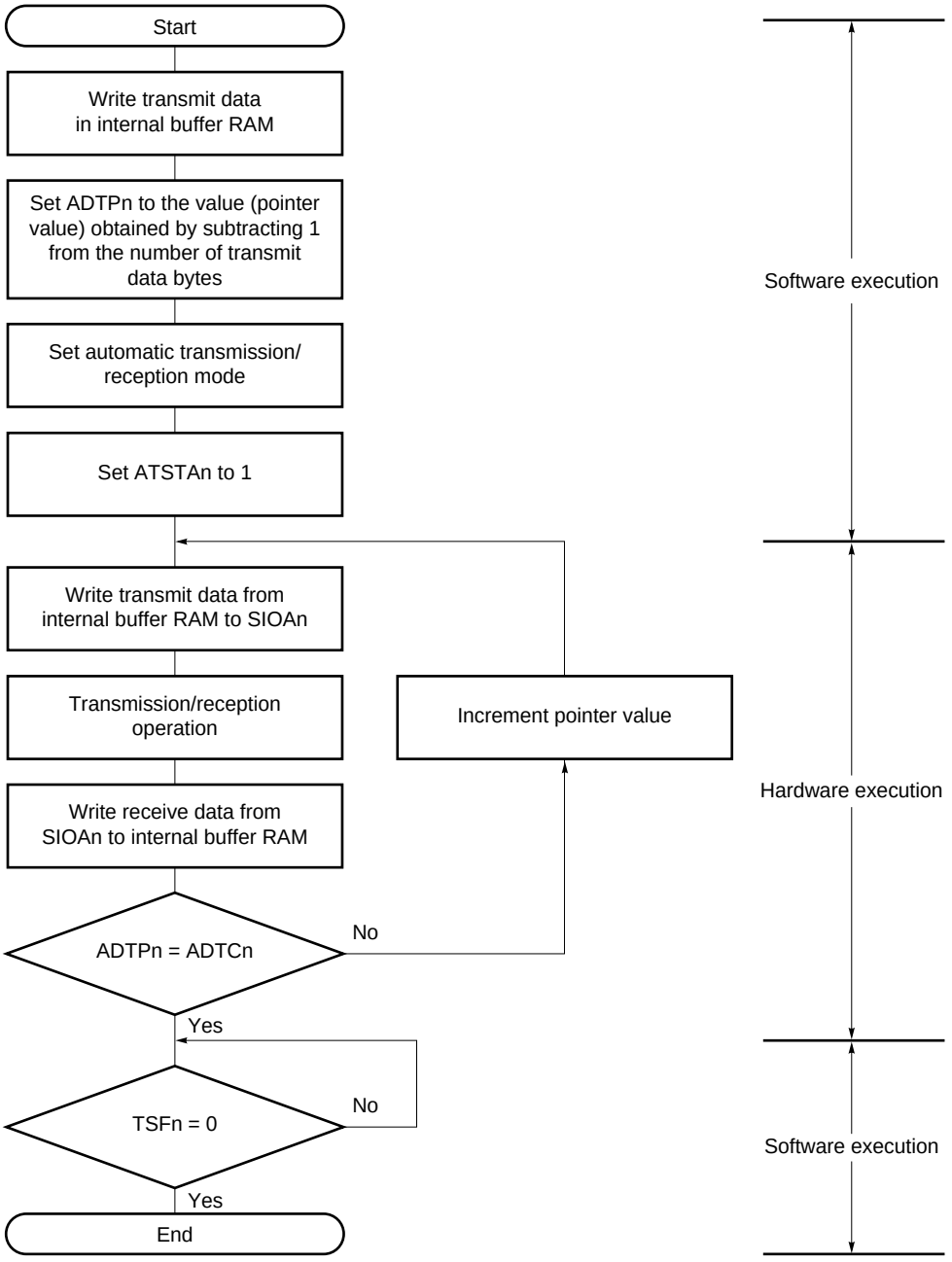
2. When the TSFn bit is cleared, the SOAn pin becomes low level.

3. If CPU access to the buffer RAM conflicts with CSIA read/write during the interval time, the interval time becomes longer.

Remarks 1. CSIAFn: Interrupt request flag
TSFn: Bit n of serial status register n (CSISn)

2. n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

Figure 17-6. Automatic Transmission/Reception Mode Flowchart



ADTPn: Automatic data transfer address point specification register n
ADTIn: Automatic data transfer interval specification register n
ATSTAn: Bit 0 of serial trigger register n (CSITn)
SIOAn: Serial I/O shift register n
ADTCn: Automatic data transfer address count register n
TSFn: Bit 0 of serial status register n (CSISn)

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

In 6-byte transmission/reception (ATMn bit = 0, RXEn bit = 1, TXEn bit = 1 in the CSIMAn register) in automatic transmission/reception mode, internal buffer RAM operates as follows.

(i) When transmission/reception operation is started (see Figure 17-7 (a).)

When the ATSTAn bit of serial trigger register n (CSITn) is set to 1, transmit data 1 (T1) is transferred from the internal buffer RAM to SIOAn. When transmission of the first byte is completed, receive data 1 (R1) is transferred from SIOAn to the buffer RAM, and automatic data transfer address count register n (ADTCn) is incremented. Then transmit data 2 (T2) is transferred from the internal buffer RAM to SIOAn.

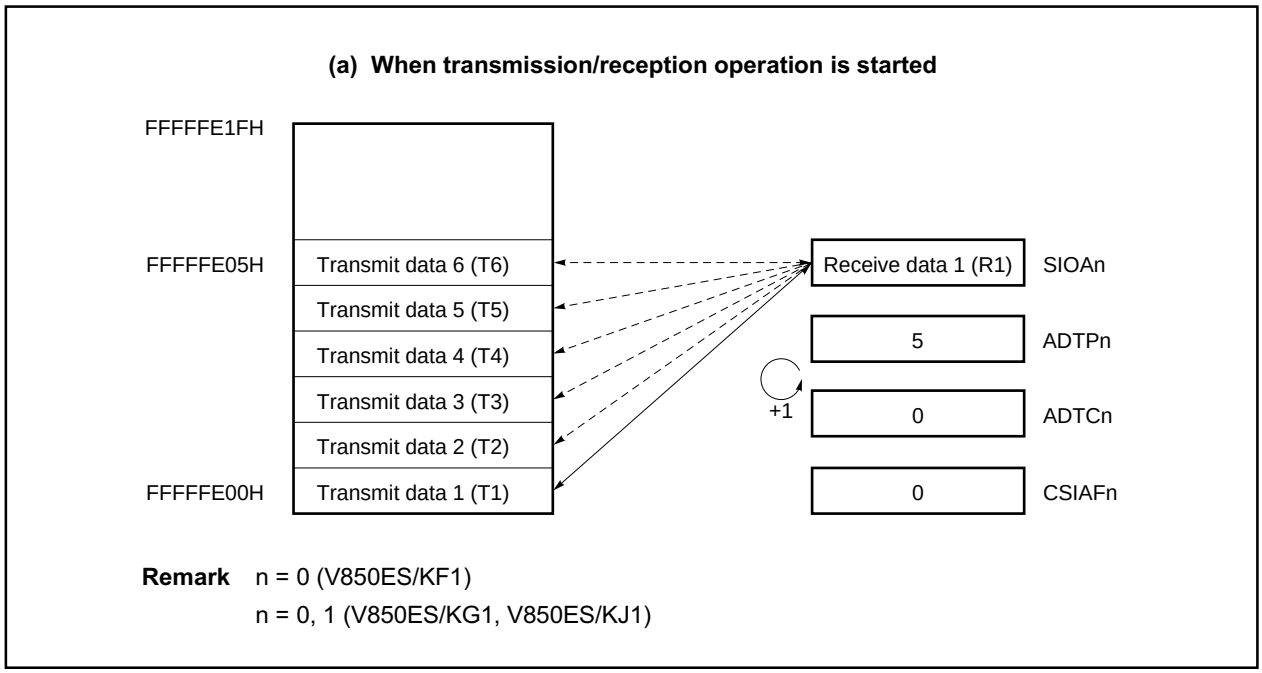
(ii) 4th byte transmission/reception point (see Figure 17-7 (b).)

Transmission/reception of the third byte is completed, and transmit data 4 (T4) is transferred from the internal buffer RAM to the SIOAn register. When transmission of the fourth byte is completed, the receive data 4 (R4) is transferred from the SIOAn register to the internal buffer RAM, and the ADTCn register is incremented.

(iii) Completion of transmission/reception (see Figure 17-7 (c).)

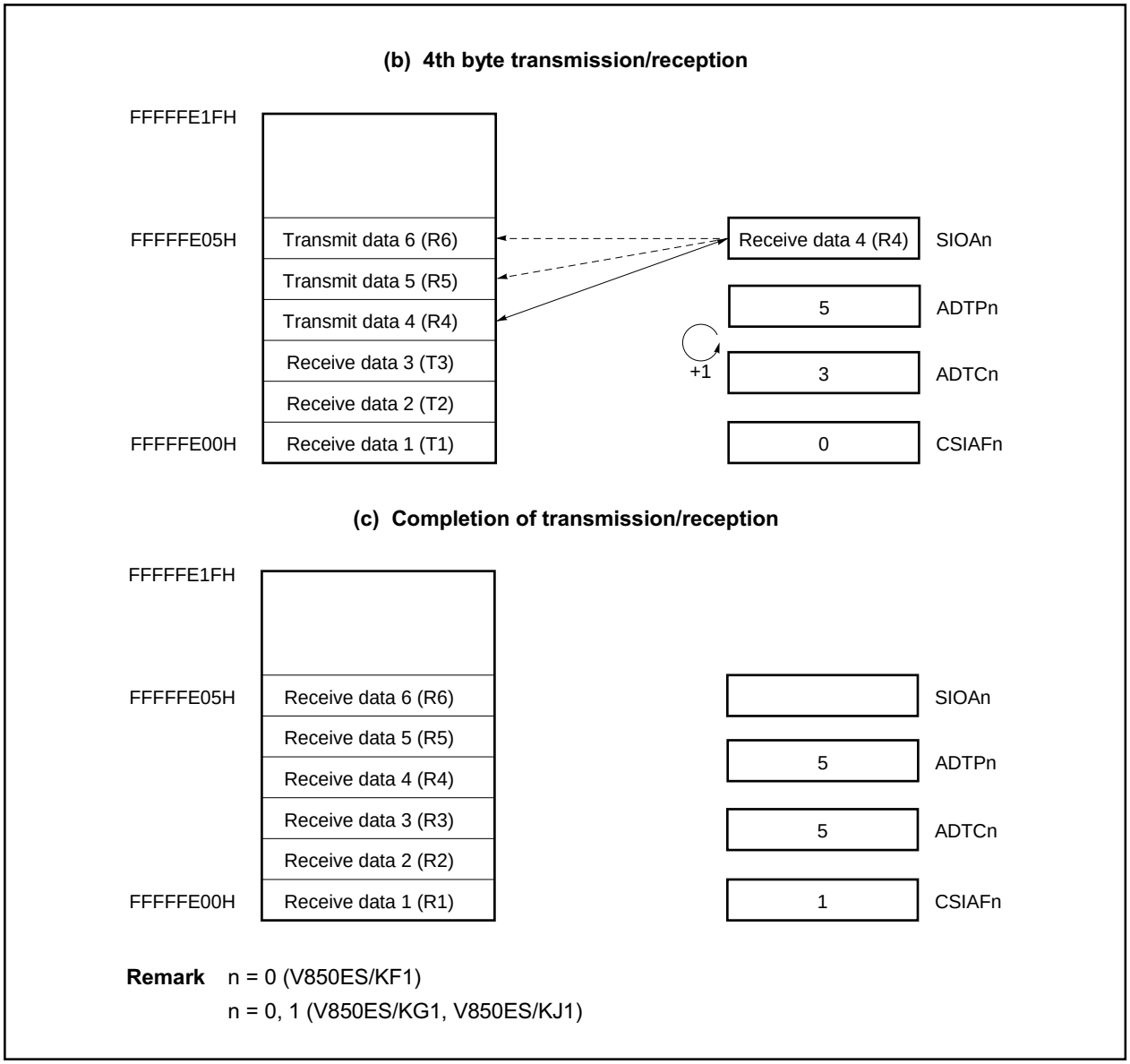
When transmission of the sixth byte is completed, receive data 6 (R6) is transferred from SIOAn register to the internal buffer RAM, and the interrupt request flag (CSIAFn) is set (INTCSIAn generation).

Figure 17-7. Internal Buffer RAM Operation in 6-Byte Transmission/Reception (in Automatic Transmission/Reception Mode) (1/2)



Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

Figure 17-7. Internal Buffer RAM Operation in 6-Byte Transmission/Reception (in Automatic Transmission/Reception Mode) (2/2)



Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

(b) Automatic transmission mode

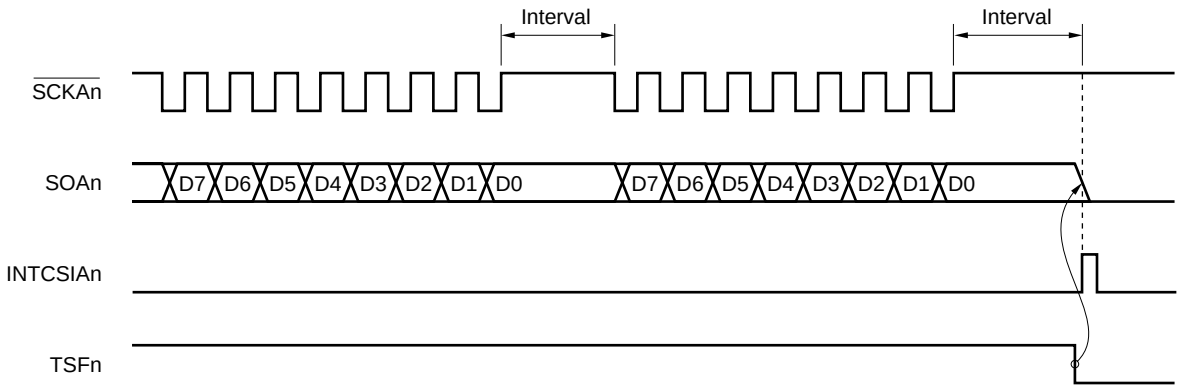
In this mode, the specified number of 8-bit unit data are transmitted.

Serial transfer is started when the ATSTAn bit of serial trigger register n (CSITn) is set to 1 while the CSIAEn, ATEn, and TXEAn bits of serial operating mode specification register n (CSIMAn) are set to 1.

When the final byte has been transmitted, an interrupt request flag (CSIAFn) is set.

Figure 17-8 shows the automatic transmission mode operation timing, and Figure 17-9 shows the operation flowchart. Figure 17-10 shows the operation of the internal buffer RAM when 6 bytes of data are transmitted or received.

Figure 17-8. Automatic Transmission Mode Operation Timing



Cautions 1. Because, in the automatic transmission mode, the automatic transmit/receive function reads data from the internal buffer RAM after 1-byte transmission, an interval is inserted until the next transmission. As the buffer RAM read is performed at the same time as CPU processing, the interval is dependent upon the value of automatic data transfer interval specification register n (ADTIn) (see (6) Automatic transmit/receive interval time).

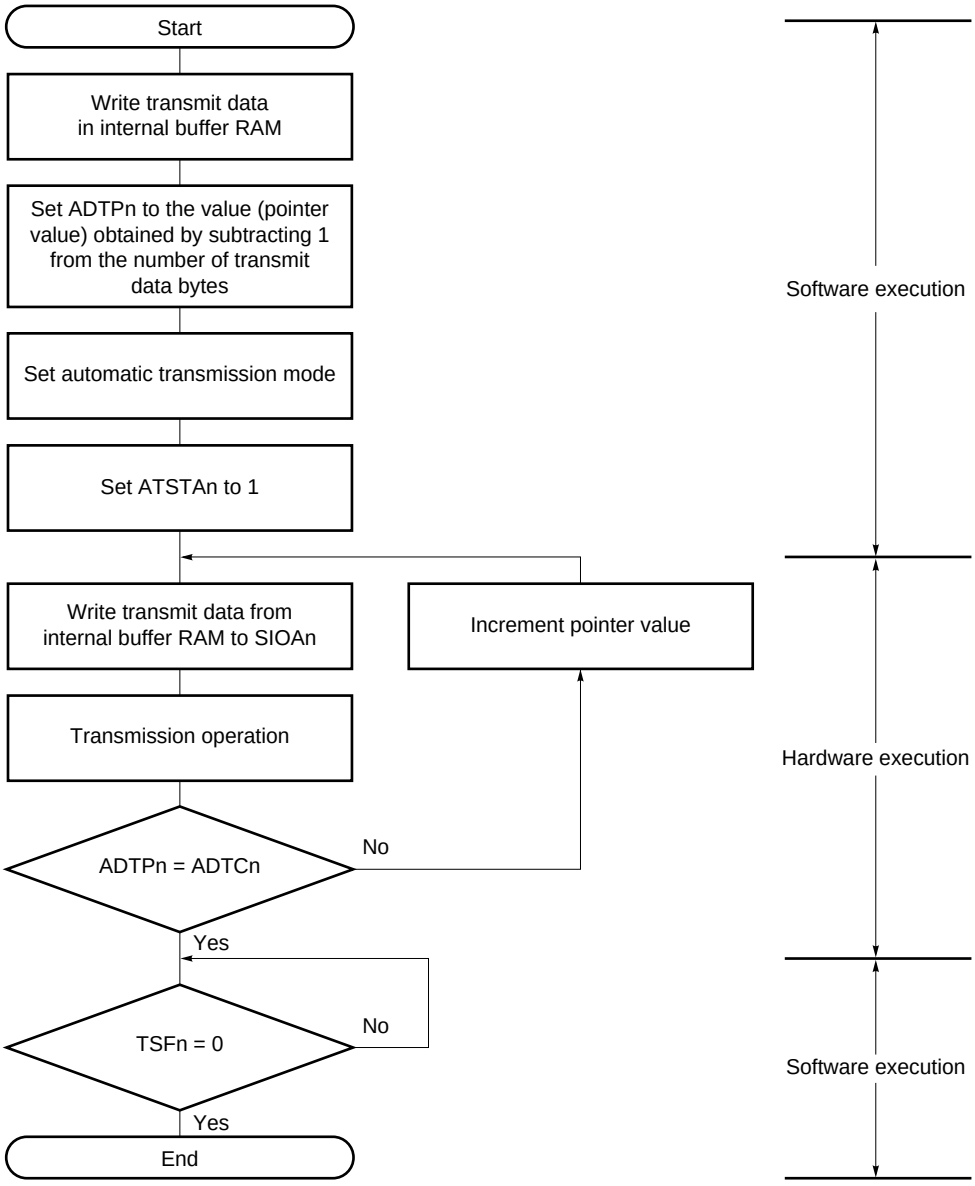
2. When the TSFn bit is cleared, the SOAn pin becomes low level.

3. If CPU access to the buffer RAM conflicts with CSIA read/write during the interval time, the interval time becomes longer.

Remarks 1. CSIAFn: Interrupt request flag
TSFn: Bit 0 of serial status register n (CSISn)

2. n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

Figure 17-9. Automatic Transmission Mode Flowchart



ADTPn: Automatic data transfer address point specification register n
ADTIn: Automatic data transfer interval specification register n
ATSTAn: Bit 0 of serial trigger register n (CSITn)
SIOAn: Serial I/O shift register n
ADTCn: Automatic data transfer address count register n
TSFn: Bit 0 of serial status register n (CSISn)

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

In 6-byte transmission (ATMn = 0, RXEn bit = 0, TXEn bit = 1, ATE0 bit = 1) in automatic transmission mode, internal buffer RAM operates as follows.

(i) When transmission is started (see Figure 17-10 (a).)

When the ATSTAn bit of serial trigger register n (CSITn) is set to 1, transmit data 1 (T1) is transferred from the internal buffer RAM to SIOAn. When transmission of the first byte is completed, automatic data transfer address count register n (ADTCn) is incremented. Then transmit data 2 (T2) is transferred from the internal buffer RAM to the SIOAn register.

(ii) 4th byte transmission point (see Figure 17-10 (b).)

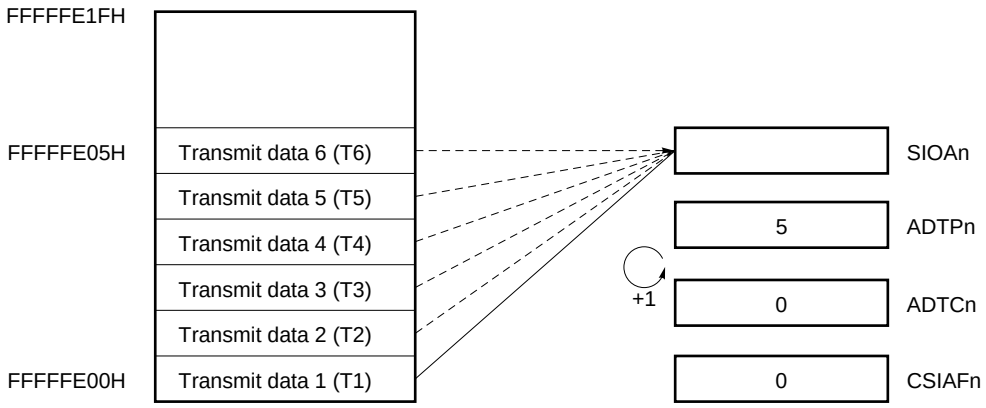
Transmission of the third byte is completed, and transmit data 4 (T4) is transferred from the internal buffer RAM to the SIOAn register. When transmission of the fourth byte is completed, the ADTCn register is incremented.

(iii) Completion of transmission (see Figure 17-10 (c).)

When transmission of the sixth byte is completed, the interrupt request flag (CSIAFn) is set (INTCSIAn signal generation), and the TFSn flag is cleared.

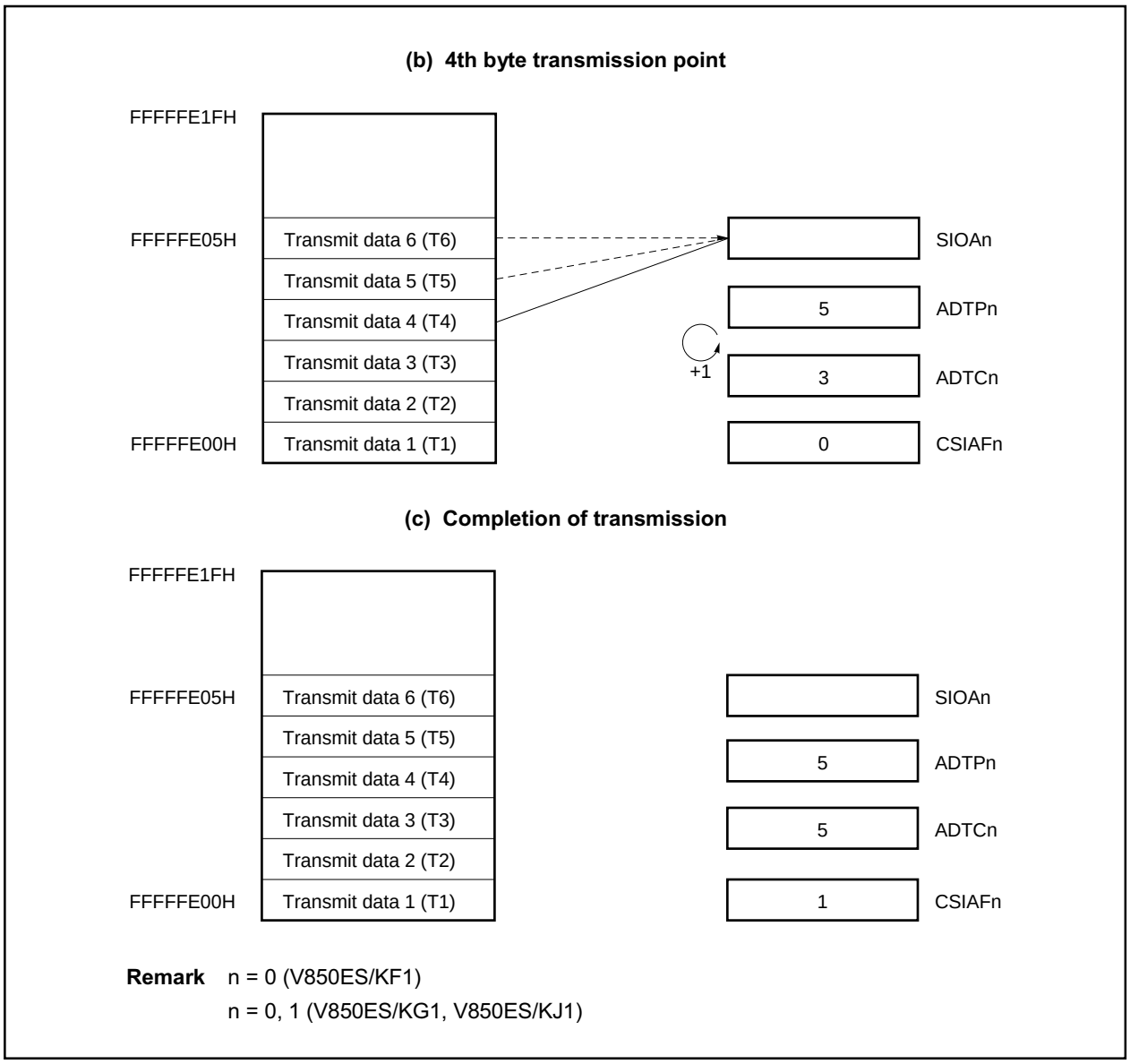
Figure 17-10. Internal Buffer RAM Operation in 6-Byte Transmission (in Automatic Transmission Mode) (1/2)

(a) When transmission is started



Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

Figure 17-10. Internal Buffer RAM Operation in 6-Byte Transmission (in Automatic Transmission Mode) (2/2)



Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

(c) Repeat transmission mode

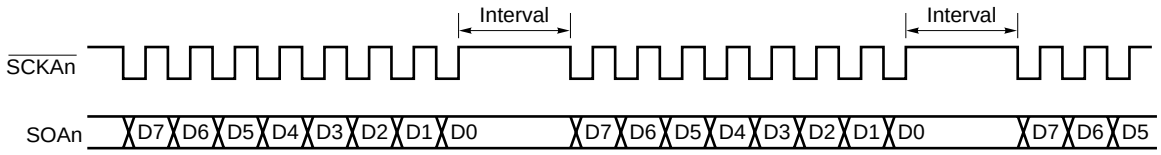
In this mode, data stored in the internal buffer RAM is transmitted repeatedly.

Serial transfer is started when the ATSTAn bit of serial trigger register n (CSITn) is set to 1 while the CSIAEn, ATEn, ATMn, and TXEn bits of serial operating mode specification register n (CSIMAn) are set to 1.

Unlike the basic transmission mode, after the final byte (data in address FA1FH) has been transmitted, the interrupt request signal (INTCSIAn) is not generated, the automatic data transfer address count register n (ADTCn) is reset to 0, and the internal buffer RAM contents are transmitted again.

The repeat transmission mode operation timing is shown in Figure 17-11, and the operation flowchart in Figure 17-12. Figure 17-13 shows the operation of the internal buffer RAM when 6 bytes of data are transmitted in the repeat transmission mode.

Figure 17-11. Repeat Transmission Mode Operation Timing



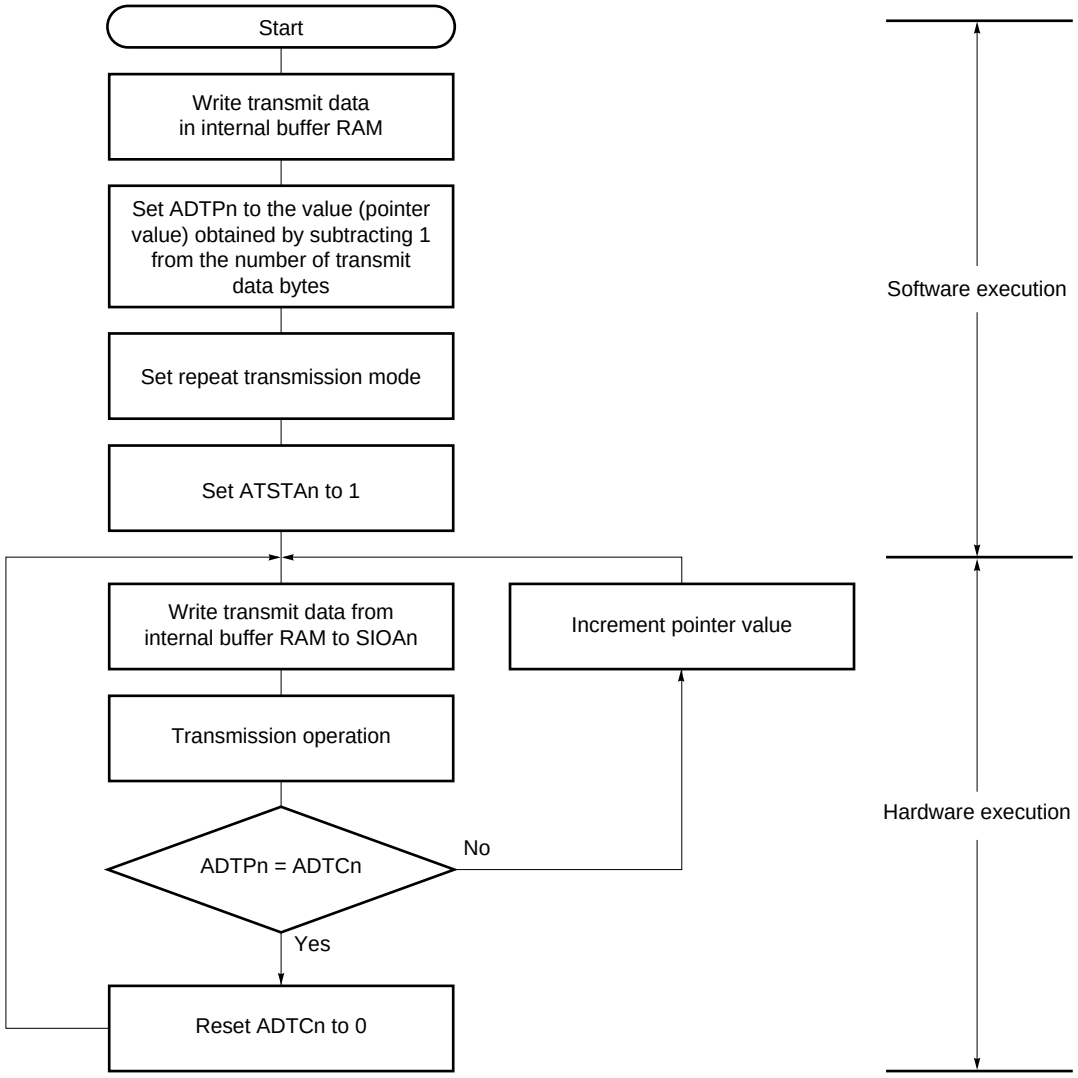
Caution Because, in the repeat transmission mode, a read is performed on the buffer RAM after the transmission of one byte, the interval is included in the period up to the next transmission. As the buffer RAM read is performed at the same time as CPU processing, the interval is dependent upon automatic data transfer interval specification register n (ADTIn).

If CPU access to the buffer RAM conflicts with CSIA read/write during the interval time, the interval time becomes longer.

Remark n = 0 (V850ES/KF1)

n = 0, 1 (V850ES/KG1, V850ES/KJ1)

Figure 17-12. Repeat Transmission Mode Flowchart



ADTPn: Automatic data transfer address point specification register n
ADTIn: Automatic data transfer interval specification register n
ATSTAn: Bit 0 of serial trigger register n (CSITn)
SIOAn: Serial I/O shift register n
ADTCn: Automatic data transfer address count register n

Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

In 6-byte transmission (ATMn bit = 1, RXEAn bit = 0, TXEAn bit = 1, ATEn bit = 1) in repeat transmission mode, internal buffer RAM operates as follows.

(i) When transmission is started (see Figure 17-13 (a).)

When the ATSTAn bit of serial trigger register n (CSITn) is set to 1, transmit data 1 (T1) is transferred from the internal buffer RAM to the SIOAn register. When transmission of the first byte is completed, automatic data transfer address count register n (ADTCn) is incremented. Then transmit data 2 (T2) is transferred from the internal buffer RAM to the SIOAn register.

(ii) Upon completion of transmission of 6 bytes (see Figure 17-13 (b).)

When transmission of the sixth byte is completed, the interrupt request signal (INTCSIAn) is not generated.

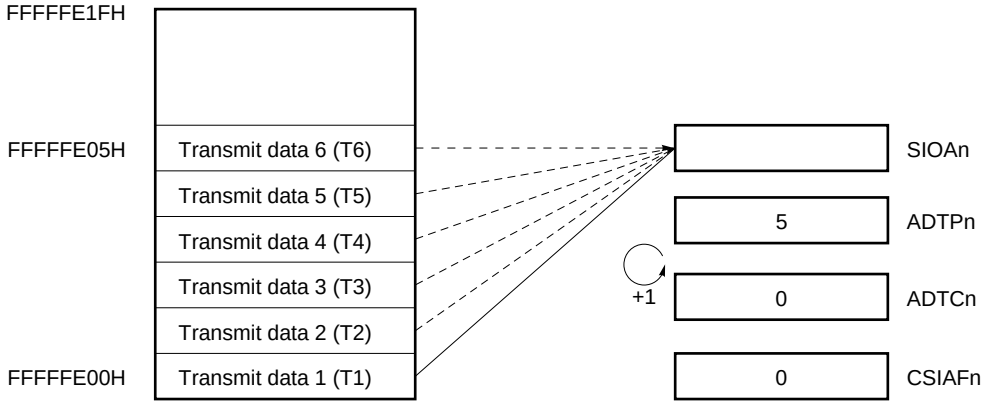
The ADTCn register is reset to 0.

(iii) 7th byte transmission point (see Figure 17-13 (c).)

Transmit data 1 (T1) is transferred from the internal buffer RAM to SIOAn register again. When transmission of the first byte is completed, the ADTCn register is incremented. Then transmit data 2 (T2) is transferred from the internal buffer RAM to the SIOAn register.

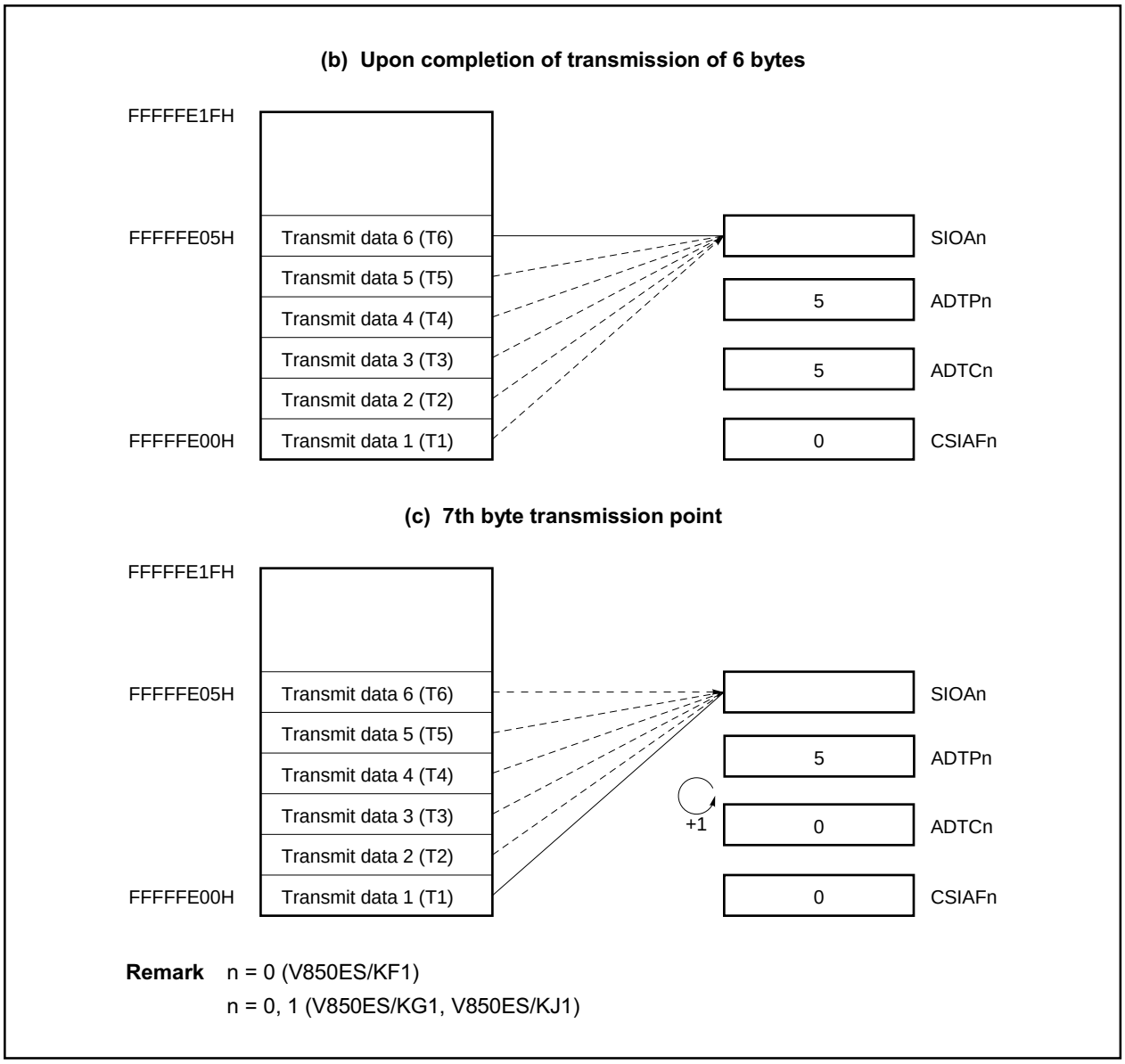
Figure 17-13. Internal Buffer RAM Operation in 6-Byte Transmission (in Repeat Transmission Mode) (1/2)

(a) When transmission is started



Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

Figure 17-13. Internal Buffer RAM Operation in 6-Byte Transmission (in Repeat Transmission Mode) (2/2)

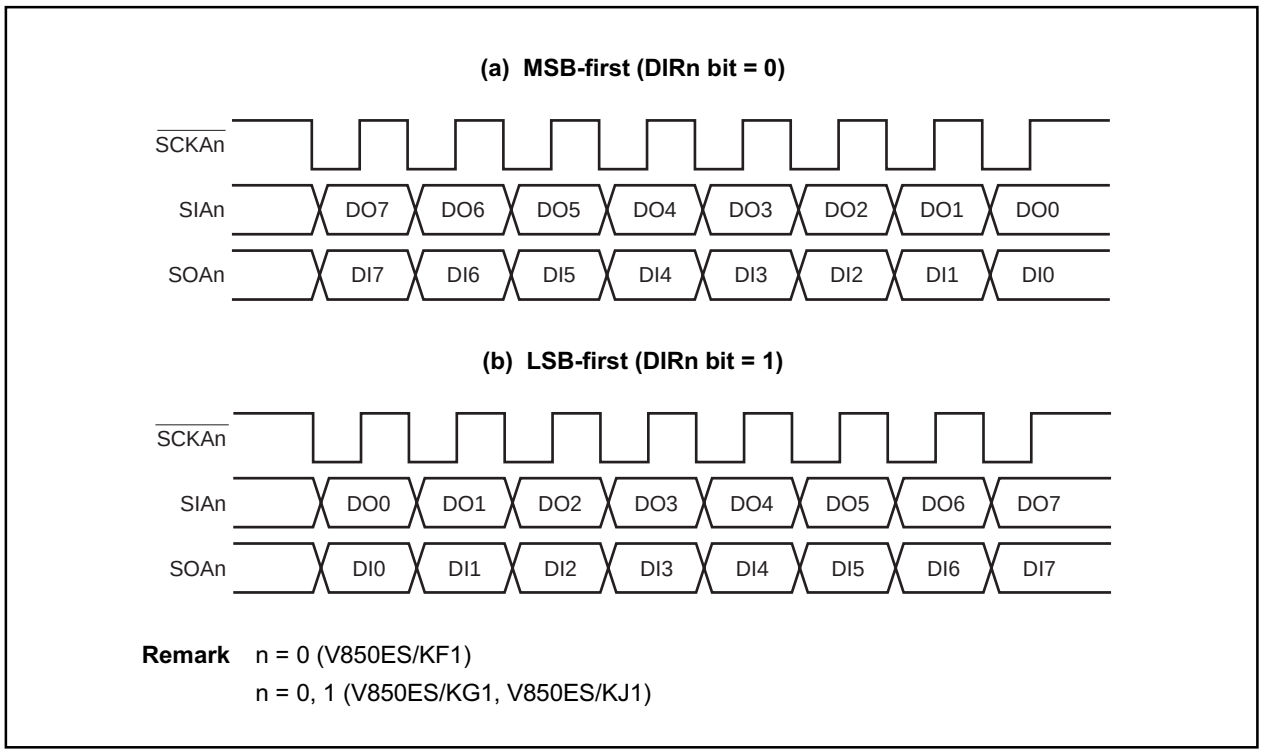


Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

(d) Data format

In the data format, data is changed in synchronization with the $\overline{\text{SCKAn}}$ pin falling edge as shown below. The data length is fixed to 8 bits and the data transfer direction can be switched by the specification of the DIRn bit of serial operation mode specification register n (CSIMAn).

Figure 17-14. Format of CSIAn Transmit/Receive Data



Remark n = 0 (V850ES/KF1)
n = 0, 1 (V850ES/KG1, V850ES/KJ1)

(e) Automatic transmission/reception suspension and restart

Automatic transmission/reception can be temporarily suspended by setting the ATSTPn bit of serial trigger register n (CSITn) to 1.

During 8-bit data transfer, the transmission/reception is not suspended. It is suspended upon completion of 8-bit data transfer.

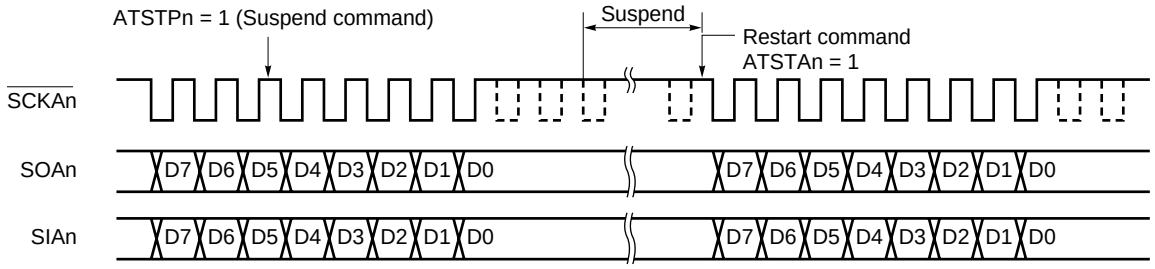
When suspended, the TSFn bit of serial status register n (CSISn) is set to 0 after transfer of the 8th bit.

To restart automatic transmission/reception, set the ATSTAn bit of the CSITn register to 1. The remaining data can be transmitted in this way.

Cautions 1. If the IDLE instruction is executed during automatic transmission/reception, transfer is suspended and the IDLE mode is set if during 8-bit data transfer. When the IDLE mode is cleared, automatic transmission/reception is restarted from the suspended point.

2. When suspending automatic transmission/reception, do not change the operating mode to 3-wire serial I/O mode while the TSFn bit = 1.

Figure 17-15. Automatic Transmission/Reception Suspension and Restart



ATSTPn: Bit 1 of serial trigger register n (CSITn)

ATSTAn: Bit 0 of CSITn

Remark n = 0 (V850ES/KF1)

n = 0, 1 (V850ES/KG1, V850ES/KJ1)

CHAPTER 18 I²C BUS

To use the I²C bus function, set the P38/SDA0, P39/SCL0, P80/SDA1, and P81/SCL1 pins to N-ch open drain output as the alternate function.

The number of I²C bus channels incorporated differs as follows depending on the product.

Product Name	V850ES/KF1	V850ES/KG1	V850ES/KJ1
Number of channels	1 channel (I²C0)		2 channels (I²C0, I²C1)

The products with an on-chip I²C bus are shown below.

- V850/KF1: μPD703208Y, 703209Y, 703210Y, 70F3210Y
- V850/KG1: μPD703212Y, 703213Y, 703214Y, 70F3214Y
- V850/KJ1: μPD703216Y, 703217Y, 70F3217Y

18.1 Selecting UART2 or I²C1 Mode

UART2 and I²C1 of the V850ES/KJ1 share pins, and therefore these interfaces cannot be used at the same time. Select UART2 or I²C1 in advance by using the port 8 mode control register (PMC8) and port 8 function control register (PFC8) (refer to **4.3.8 Port 8**).

Caution UART2 or I²C1 transmission/reception operations are not guaranteed if the mode is changed during transmission or reception. Be sure to disable the operation of the unit that is not used.

Figure 18-1. Selecting Mode of UART2 or I²C1

After reset: 00H R/W Address: FFFFF450H

	7	6	5	4	3	2	1	0
PMC8	0	0	0	0	0	0	PMC81	PMC80

After reset: 00H R/W Address: FFFFF470H

	7	6	5	4	3	2	1	0
PFC8	0	0	0	0	0	0	PFC81	PFC80

PFC8n	PMC8n	Operation mode
0	0	Port I/O mode
0	1	UART2 mode
1	0	Port I/O mode
1	1	I²C1 mode

Remark n = 0, 1

18.2 Features

The I²C0 and I²C1 have the following two modes.

- Operation stop mode
- I²C (Inter IC) bus mode (multimaster supported)

(1) Operation stop mode

This mode is used when serial transfers are not performed. It can therefore be used to reduce power consumption.

(2) I²C bus mode (multimaster support)

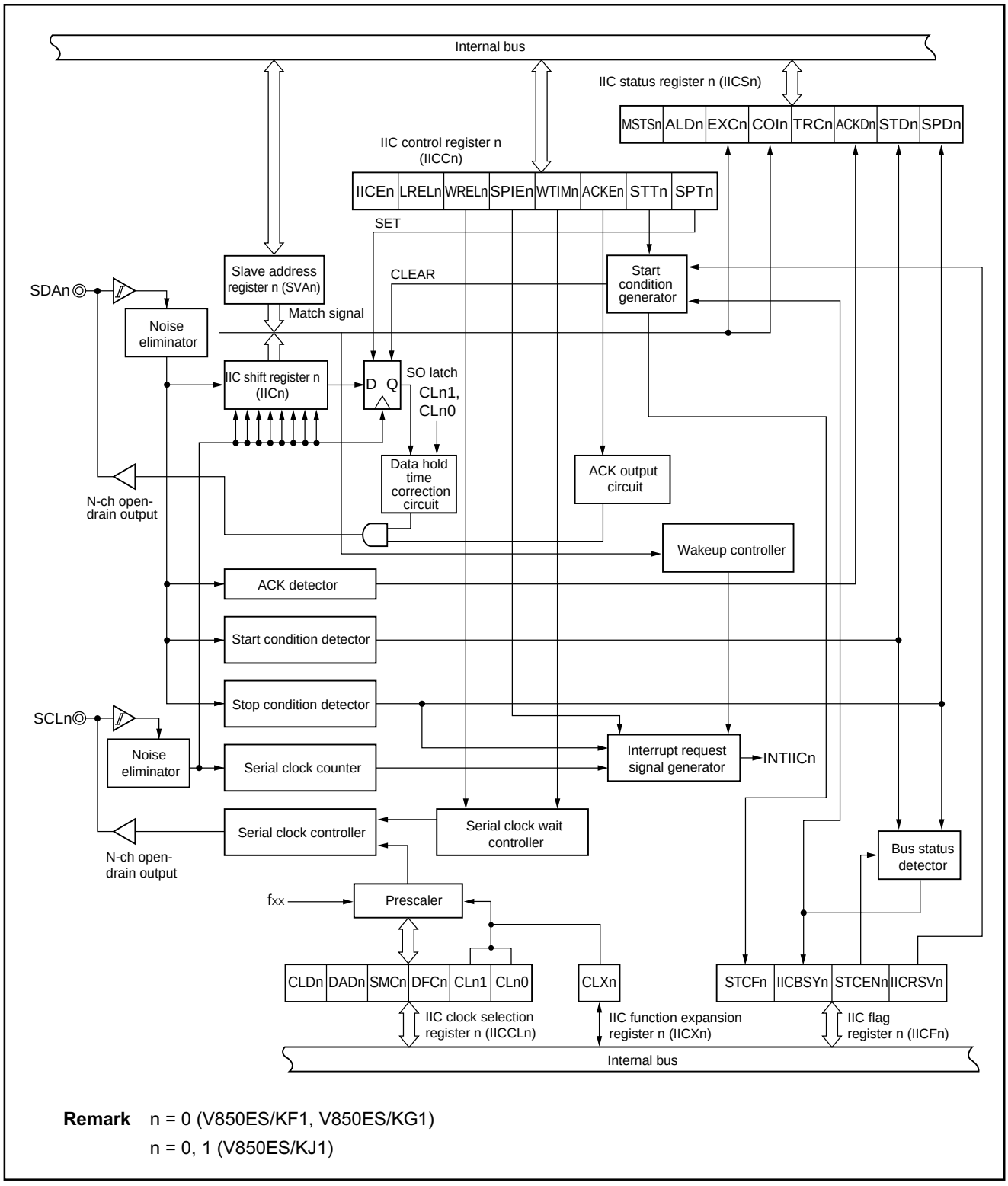
This mode is used for 8-bit data transfers with several devices via two lines: a serial clock (SCLn) line and a serial data bus (SDAn) line.

This mode complies with the I²C bus format and the master device can output “start condition”, “data”, and “stop condition” data to the slave device, via the serial data bus. The slave device automatically detects these received data by hardware. This function can simplify the part of application program that controls the I²C bus.

Since the SCLn and SDAn pins are used for N-ch open drain outputs, I²Cn requires pull-up resistors for the serial clock line and the serial data bus line.

Remark n = 0 (V850ES/KF1, V850ES/KG1)
n = 0, 1 (V850ES/KJ1)

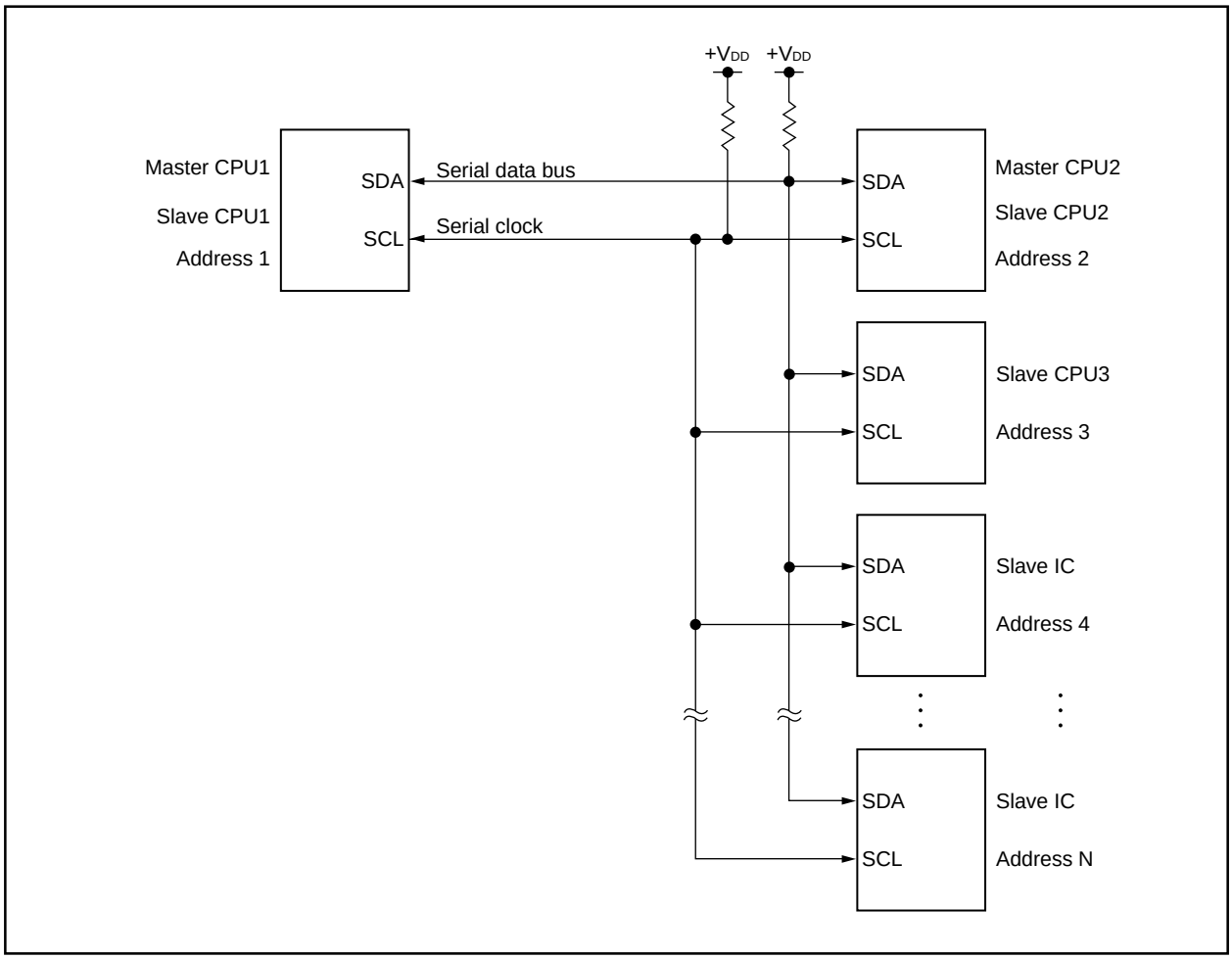
Figure 18-2. Block Diagram of I²Cn



Remark n = 0 (V850ES/KF1, V850ES/KG1)
n = 0, 1 (V850ES/KJ1)

A serial bus configuration example is shown below.

Figure 18-3. Serial Bus Configuration Example Using I²C Bus



18.3 Configuration

I²Cn includes the following hardware.

Table 18-1. Configuration of I²Cn

Item	Configuration
Registers	IIC shift registers 0 and 1 (IIC0, IIC1) Slave address registers 0 and 1 (SVA0, SVA1)
Control registers	IIC control registers 0 and 1 (IICC0, IICC1) IIC status registers 0 and 1 (IICS0, IICS1) IIC flag registers 0, 1 (IICCF0, IICCF1) IIC clock selection registers 0 and 1 (IICCL0, IICCL1) IIC function expansion registers 0 and 1 (IICX0, IICX1)

Remark n = 0 (V850ES/KF1, V850ES/KG1)
n = 0, 1 (V850ES/KJ1)

(1) IIC shift registers 0 and 1 (IIC0, IIC1)

IICn is used to convert 8-bit serial data to 8-bit parallel data and to convert 8-bit parallel data to 8-bit serial data.
IICn can be used for both transmission and reception.
Write and read operations to IICn are used to control the actual transmit and receive operations.
IICn can be read/written by an 8-bit memory manipulation instruction.
After reset, IIC0 and IIC1 are cleared to 00H.

(2) Slave address registers 0 and 1 (SVA0, SVA1)

SVAn sets local addresses when in slave mode.
SVAn can be read/written by an 8-bit memory manipulation instruction.
After reset, SVA0 and SVA1 are cleared to 00H.

(3) SO latch

The SO latch is used to retain the SDAn pin's output level.

(4) Wakeup controller

This circuit generates an interrupt request when the address received by this register matches the address value set to slave address register n (SVAn) or when an extension code is received.

(5) Prescaler

This selects the sampling clock to be used.

(6) Serial clock counter

This counter counts the serial clocks that are output and the serial clocks that are input during transmit/receive operations and is used to verify that 8-bit data was sent or received.

(7) Interrupt request signal generator

This circuit controls the generation of interrupt request signals (INTIICn).

An I^2C interrupt is generated following either of two triggers.

- Rising of the eighth or ninth clock of the serial clock (set by WTIMn bit[Note])
- Interrupt request generated when a stop condition is detected (set by SPIEn bit[Note])

Note WTIMn bit: Bit 3 of IIC control register n (IICCn)
SPIEn bit: Bit 4 of IIC control register n (IICCn)

(8) Serial clock controller

In master mode, this circuit generates the clock output via the SCLn pin from a sampling clock.

(9) Serial clock wait controller

This circuit controls the wait timing.

(10) ACK output circuit, stop condition detector, start condition detector, and ACK detector

These circuits are used to output and detect various control signals.

(11) Data hold time correction circuit

This circuit generates the hold time for data corresponding to the falling edge of the serial clock.

(12) Start condition generator

This circuit generates a start condition when the STTn bit is set.

However, in the communication reservation disabled status (IICRSVn = 1), when the bus is not released (IICBSYn = 1), start condition requests are ignored and the STCFn flag is set.

(13) Bus status detector

This circuit detects whether or not the bus is released by detecting start conditions and stop conditions.

However, as the bus status cannot be detected immediately following operation, the initial status is set by the STCENn bit.

18.4 Control Registers

I²C0 and I²C1 are controlled by the following registers.

- IIC control registers 0, 1 (IICC0, IICC1)
- IIC status registers 0, 1 (IICS0, IICS1)
- IIC flag registers 0, 1 (IICF0, IICF1)
- IIC clock selection registers 0, 1 (IICCL0, IICCL1)
- IIC function expansion registers 0, 1 (IICX0, IICX1)

The following registers are also used.

- IIC shift registers 0, 1 (IIC0, IIC1)
- Slave address registers 0, 1 (SVA0, SVA1)

Remark For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

(1) IIC control registers 0, 1 (IICC0, IICC1)

IICCn is used to enable/stop I²Cn operations, set wait timing, and set other I²C operations.

IICCn can be set by an 8-bit or 1-bit memory manipulation instruction (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

After reset, IICCn is cleared to 00H.

(1/4)

After reset: 00H R/W Address: FFFFFD82H, FFFFFD92H

	<7>	<6>	5	4	3	2	1	0
IICCn	IICEn	LRELn	WRELn	SPIEn	WTIMn	ACKEn	STTn	SPTn

(n = 0, 1)

IICEn	I²Cn operation enable/disable specification
0	Stop operation. Preset IIC status register n (IICSn)[Note 1]. Stop internal operation.
1	Enable operation.

Condition for clearing (IICEn = 0)	Condition for setting (IICEn = 1)
• Cleared by instruction • Reset	• Set by instruction

LRELn	Exit from communications
0	Normal operation
1	This exits from the current communications operation and sets standby mode. This setting is automatically cleared after being executed. Its uses include cases in which a locally irrelevant extension code has been received. The SCLn and SDAn lines are set to high impedance. The following flags are cleared. • STDn • ACKDn • TRCn • COIn • EXCn • MSTSn • STTn • SPTn
The standby mode following exit from communications remains in effect until the following communications entry conditions are met. • After a stop condition is detected, restart is in master mode. • An address match or extension code reception occurs after the start condition.	
Condition for clearing (LRELn = 0)[Note 2]	Condition for setting (LRELn = 1)
• Automatically cleared after execution • Reset	• Set by instruction

Notes 1. The IICS register, and the IICFn.STCFn, IICFn.IICBSYn, IICCLn.CLDn, and IICCLn.DADn bits are reset.

2. This flag's signal is invalid when IICEn = 0.

Remark STDn: Bit 1 of IIC status register n (IICSn)
ACKDn: Bit 2 of IIC status register n (IICSn)
TRCn: Bit 3 of IIC status register n (IICSn)
COIn: Bit 4 of IIC status register n (IICSn)
EXCn: Bit 5 of IIC status register n (IICSn)
MSTSn: Bit 7 of IIC status register n (IICSn)

(2/4)

WRELn	Wait cancellation control
0	Do not cancel wait
1	Cancel wait. This setting is automatically cleared after wait is canceled.

Condition for clearing (WRELn = 0)[Note]	Condition for setting (WRELn = 1)
• Automatically cleared after execution • Reset	• Set by instruction

SPIEn	Enable/disable generation of interrupt request when stop condition is detected
0	Disable
1	Enable

Condition for clearing (SPIEn = 0)[Note]	Condition for setting (SPIEn = 1)
• Cleared by instruction • Reset	• Set by instruction

WTIMn	Control of wait and interrupt request generation
0	Interrupt request is generated at the eighth clock's falling edge. Master mode: After output of eight clocks, clock output is set to low level and wait is set. Slave mode: After input of eight clocks, the clock is set to low level and wait is set for master device.
1	Interrupt request is generated at the ninth clock's falling edge. Master mode: After output of nine clocks, clock output is set to low level and wait is set. Slave mode: After input of nine clocks, the clock is set to low level and wait is set for master device.

An interrupt is generated at the falling of the 9th clock during address transfer independently of the setting of this bit. The setting of this bit is valid when the address transfer is completed.. When in master mode, a wait is inserted at the falling edge of the ninth clock during address transfers. For a slave device that has received a local address, a wait is inserted at the falling edge of the ninth clock after an $\overline{\text{ACK}}$ signal is issued. However, when the slave device has received an extension code, a wait is inserted at the falling edge of the eighth clock.

Condition for clearing (WTIMn = 0)[Note]	Condition for setting (WTIMn = 1)
• Cleared by instruction • Reset	• Set by instruction

Note This flag's signal is invalid when IICEn = 0.

(3/4)

ACKEn	Acknowledgment control
0	Disable acknowledgment.
1	Enable acknowledgment. During the ninth clock period, the SDAn line is set to low level. However, $\overline{ACK}$ is invalid during address transfers and other than in expansion mode.

Condition for clearing (ACKEn = 0)[Note]	Condition for setting (ACKEn = 1)
• Cleared by instruction • Reset	• Set by instruction

STTn	Start condition trigger
0	Do not generate a start condition.
1	When bus is released (in STOP mode): Generate a start condition (for starting as master). The SDAn line is changed from high level to low level and then the start condition is generated. Next, after the rated amount of time has elapsed, SCLn is changed to low level. When a third party is communicating • When communication reservation function is enabled (IICRSVn = 0) Functions as the start condition reservation flag. When set, automatically generates a start condition after the bus is released. • When communication reservation function is disabled (IICRSVn = 1) The STCFn flag is set. No start condition is generated. In the wait state (when master device): Generates a restart condition after releasing the wait.
Cautions concerning set timing For master reception: Cannot be set during transfer. Can be set only when ACKEn has been set to 0 and slave has been notified of final reception. For master transmission: A start condition cannot be generated normally during the ACKn period. Set during the wait period. • Cannot be set at the same time as SPTn	

Condition for clearing (STTn = 0)[Note]	Condition for setting (STTn = 1)
• Cleared by loss in arbitration • Cleared after start condition is generated by master device • When LRELn = 1 (exit from communications) • When IICEn = 0 (operation stop) • Cleared when RESET is input	• Set by instruction

Note This flag's signal is invalid when IICEn = 0.

Remarks 1. Bit 1 (STTn) is 0 if it is read after data setting.

2. IICRSVn: Bit 0 of IIC flag register n (IICFn)

STCFn: IICRSVn: Bit 7 of IIC flag register n (IICFn)

(4/4)

SPTn	Stop condition trigger
0	Stop condition is not generated.
1	Stop condition is generated (termination of master device's transfer). After the SDAn line goes to low level, either set the SCLn line to high level or wait until it goes to high level. Next, after the rated amount of time has elapsed, the SDAn line is changed from low level to high level and a stop condition is generated.

Cautions concerning setting timing

For master reception: Cannot be set during transfer.
Can be set only when ACKEn has been set to 0 and during the wait period after slave has been notified of final reception.

For master transmission: A stop condition cannot be generated normally during the ACKn period. Set during the wait period.

- Cannot be set at the same time as STTn.
- SPTn can be set only when in master mode[Note 1]
- When WTIMn has been set to 0, if SPTn is set during the wait period that follows output of eight clocks, note that a stop condition will be generated during the high-level period of the ninth clock.
  When a ninth clock must be output, WTIMn should be changed from 0 to 1 during the wait period following output of eight clocks, and SPTn should be set during the wait period that follows output of the ninth clock.

Condition for clearing (SPTn = 0)[Note 2]	Condition for setting (SPTn = 1)
• Cleared by instruction • Cleared by loss in arbitration • Automatically cleared after stop condition is detected • When LRELn = 1 (exit from communications) • When IICEn = 0 (operation stop) • Cleared when $\overline{\text{RESET}}$ is input	• Set by instruction

Notes 1. Set SPTn only in master mode. However, SPTn must be set and a stop condition generated before the first stop condition is detected following the switch to operation enable status. For details, see **18.5 Cautions**.

2. When IICEn is cleared to 0, the signal of this flag is invalid.

Caution When bit 3 (TRCn) of IIC status register n (IICSn) is set to 1, WRELn is set during the ninth clock and wait is canceled, after which TRCn is cleared and the SDAn line is set to high impedance.

Remark Bit 0 (SPTn) is 0 if it is read after data setting.

(2) IIC status registers 0, 1 (IICS0, IICS1)

IICSn indicates the status of the I²Cn bus.

IICSn can be set by an 8-bit or 1-bit memory manipulation instruction. IICSn is a read-only register (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

After reset, IICSn is cleared to 00H.

Caution When the main clock is stopped and the CPU is operating on the subclock, do not access the IICSn register using an access method that causes a wait.
For details, refer to 3.4.8 (2).

(1/3)

After reset: 00H R Address: FFFFFD86H, FFFFFD96H

	7	6	5	4	3	2	1	0
IICSn	MSTSn	ALDn	EXCn	COIn	TRCn	ACKDn	STDn	SPDn

(n = 0, 1)

MSTSn	Master device status
0	Slave device status or communication standby status
1	Master device communication status

Condition for clearing (MSTSn = 0)	Condition for setting (MSTSn = 1)
• When a stop condition is detected • When ALDn = 1 (arbitration loss) • Cleared by LRELn = 1 (exit from communications) • When IICEn changes from 1 to 0 (operation stop) • Reset	• When a start condition is generated

ALDn	Detection of arbitration loss
0	This status means either that there was no arbitration or that the arbitration result was a “win”.
1	This status indicates the arbitration result was a “loss”. MSTSn is cleared.

Condition for clearing (ALDn = 0)	Condition for setting (ALDn = 1)
• Automatically cleared after IICSn is read[Note] • When IICEn changes from 1 to 0 (operation stop) • Reset	• When the arbitration result is a “loss”.

Note This register is also cleared when a bit manipulation instruction is executed for bits other than IICSn.

Remark LRELn: Bit 6 of IIC control register n (IICCn)
IICEn: Bit 7 of IIC control register n (IICCn)

(2/3)

EXCn	Detection of extension code reception
0	Extension code was not received.
1	Extension code was received.

Condition for clearing (EXCn = 0)	Condition for setting (EXCn = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LRELn = 1 (exit from communications) • When IICEn changes from 1 to 0 (operation stop) • Reset	• When the higher four bits of the received address data is either “0000” or “1111” (set at the rising edge of the eighth clock).

COIn	Detection of matching addresses
0	Addresses do not match.
1	Addresses match.

Condition for clearing (COIn = 0)	Condition for setting (COIn = 1)
• When a start condition is detected • When a stop condition is detected • Cleared by LRELn = 1 • When IICEn changes from 1 to 0 • Reset	• When the received address matches the local address (slave address register n (SVAn)) (set at the rising edge of the eighth clock).

TRCn	Detection of transmit/receive status
0	Receive status (other than transmit status). The SDAn line is set for high impedance.
1	Transmit status. The value in the SO latch is enabled for output to the SDAn line (valid starting at the falling edge of the first byte’s ninth clock).

Condition for clearing (TRCn = 0)	Condition for setting (TRCn = 1)
• When a stop condition is detected • Cleared by LRELn = 1 (exit from communications) • When IICEn changes from 1 to 0 (operation stop) • Cleared by WRELn = 1[Note] (wait release) • When ALDn changes from 0 to 1 (arbitration loss) • Reset Master • When “1” is output to the first byte’s LSB (transfer direction specification bit) Slave • When a start condition is detected When not used for communication	Master • When a start condition is generated Slave • When “1” is input in the first byte’s LSB (transfer direction specification bit)

Note TRCn is cleared and SDAn line become high impedance when bit 5 (WRELn) of IIC control register n (IICCn) is set and wait state is released at ninth clock with bit 3 (TRCn) of IIC status register n (IICSn) = 1.

Remark WRELn: Bit 5 of IIC control register n (IICCn)
LRELn: Bit 6 of IIC control register n (IICCn)
IICEn: Bit 7 of IIC control register n (IICCn)

(3/3)

ACKDn	Detection of ACK
0	ACK was not detected.
1	ACK was detected.

Condition for clearing (ACKDn = 0)	Condition for setting (ACKDn = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock • Cleared by LRELn = 1 (exit from communications) • When IICEn changes from 1 to 0 (operation stop) • Reset	• After the SDAn line is set to low level at the rising edge of the SCLn's ninth clock

STDn	Detection of start condition
0	Start condition was not detected.
1	Start condition was detected. This indicates that the address transfer period is in effect

Condition for clearing (STDn = 0)	Condition for setting (STDn = 1)
• When a stop condition is detected • At the rising edge of the next byte's first clock following address transfer • Cleared by LRELn = 1 (exit from communications) • When IICEn changes from 1 to 0 (operation stop) • Reset	When a start condition is detected

SPDn	Detection of stop condition
0	Stop condition was not detected.
1	Stop condition was detected. The master device's communication is terminated and the bus is released.

Condition for clearing (SPDn = 0)	Condition for setting (SPDn = 1)
• At the rising edge of the address transfer byte's first clock following setting of this bit and detection of a start condition • When IICEn changes from 1 to 0 (operation stop) • Reset	When a stop condition is detected

Remark LRELn: Bit 6 of IIC control register n (IICCn)
IICEn: Bit 7 of IIC control register n (IICCn)

(3) IIC flag registers 0, 1 (IICF0, IICF1)

IICF0 and IICF1 are registers that set the operation mode of I²Cn and indicate the status of the I²C bus.

These registers can be read/written in 8-bit or 1-bit units. However, the STCFn and IICBSYn bits are read-only.

The IICRSVn bit can be used to enable/disable the communication reservation function (refer to **18.14 Communication Reservation**).

The STCENn bit can be used to set the initial value of the IICBSYn bit (refer to **18.15 Cautions**).

The IICRSVn and STCENn bits can be written only when the operation of I2Cn is disabled (the IICEn bit of the IICCn register is 0). When operation is enabled, the IICFn register can be read (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

After reset, these registers are cleared to 00H.

After reset: 00H R/W[Note] Address: FFFFFD8AH, FFFFFD9AH

	7	6	5	4	3	2	1	0
IICFn	STCFn	IICBSYn	0	0	0	0	STCENn	IICRSVn

(n = 0, 1)

STCFn	STTn clear flag
0	Generate start condition
1	Start condition generation unsuccessful: clear STTn flag

Condition for clearing (STCFn = 0)	Condition for setting (STCFn = 1)
• Clearing by setting STTn = 1 • Reset	• Generating start condition unsuccessful and STTn flag cleared when communication reservation is disabled (IICRSVn = 1).

IICBSYn	I²Cn bus status flag
0	Bus release status
1	Bus communication status

Condition for clearing (IICBSYn = 0)	Setting conditions (IICBSYn = 1)
• Detection of stop condition • Reset	• Detection of start condition • Setting of IICEn when STCENn = 0

Note Bits 6 and 7 are read-only bits.

Remark STTn: Bit 1 of IIC control register n (IICCn)
IICEn: Bit 7 of IIC control register n (IICCn)

(2/2)

STCENn	Initial start enable trigger
0	After operation is enabled (IICEn = 1), enable generation of a start condition upon detection of a stop condition.
1	After operation is enabled (IICEn = 1), enable generation of a start condition without detecting a stop condition.

Condition for clearing (STCEn = 0)	Condition for setting (STCEn = 1)
• Detection of start condition • Reset	• Setting by instruction

Cautions 1. Write to the STCENn bit only when the operation is stopped (IICEn = 0).

2. As the bus release status (IICBSY = 0) is recognized regardless of the actual bus status when STCENn = 1, when generating the first start condition (STTn = 1), it is necessary to verify that no third party communications are in progress in order to prevent such communications from being destroyed.

Remark STTn: Bit 1 of IIC control register n (IICCn)
IICEn: Bit 7 of IIC control register n (IICCn)

IICRSVn	Communication reservation function disable bit
0	Enable communication reservation
1	Disable communication reservation

Condition for clearing (IICRSVn = 0)	Condition for setting (IICRSVn = 1)
• Clearing by instruction • Reset	• Setting by instruction

Caution Write to the IICRSVn bit only when the operation is stopped (IICEn = 0).

(4) IIC clock selection registers 0, 1 (IICCL0, IICCL1)

IICCLn is used to set the transfer clock for the I²C bus.

IICCLn can be set by an 8-bit or 1-bit memory manipulation instruction. Bits SMCn, CLn1 and CLn0 are set in combination with CLXn bit of IIC function expansion register n (IICXn) (see **18.4 (6) I²Cn transfer clock setting method**) (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

After reset, IICCLn is cleared to 00H.

After reset: 00H R/W[Note] Address: FFFFFD84H, FFFFFD94H

	7	6	5	4	3	2	1	0
IICCLn	0	0	CLDn	DADn	SMCn	DFCn	CLn1	CLn0

(n = 0, 1)

CLDn	Detection of SCLn line level (valid only when IICEn = 1)
0	SCLn line was detected at low level.
1	SCLn line was detected at high level.

Condition for clearing (CLDn = 0)	Condition for setting (CLDn = 1)
• When the SCLn line is at low level • When IICEn = 0 (operation stop) • Reset	• When the SCLn line is at high level

DADn	Detection of SDAn line level (valid only when IICEn = 1)
0	SDAn line was detected at low level.
1	SDAn line was detected at high level.

Condition for clearing (DADn = 0)	Condition for setting (DADn = 1)
• When the SDAn line is at low level • When IICEn = 0 (operation stop) • Reset	• When the SDAn line is at high level

SMCn	Operation mode switching
0	Operates in standard mode.
1	Operates in high-speed mode.

DFCn	Digital filter operation control
0	Digital filter off.
1	Digital filter on.
Digital filter can be used only in high-speed mode. In high-speed mode, the transfer clock does not vary regardless of DFCn switching (on/off). The digital filter is used for noise elimination in high-speed mode.	

Note Bits 4 and 5 are read only bits.

Remark IICEn: Bit 7 of IIC control register n (IICCn)

(5) IIC function expansion registers 0, 1 (IICX0, IICX1)

These registers set the function expansion of I²Cn (valid only in high-speed mode).

IICXn is set with a 1-bit or 8-bit memory manipulation instruction. Set the CLXn bit in combination with the SMCn, CLn1, and CLn0 bits of IIC clock selection register n (IICCLn) (see **18.4 (6) I²Cn transfer clock setting method**) (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

After reset, these registers are cleared to 00H.

After reset: 00H R/W Address: FFFFFD85H, FFFFFD95H

	7	6	5	4	3	2	1	0
IICXn	0	0	0	0	0	0	0	CLXn

(n = 0, 1)

(6) I²Cn transfer clock setting method

The I²Cn transfer clock frequency (f_{SCL}) is calculated using the following expression (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

$$f_{SCL} = 1/(m \times T + t_R + t_F)$$

m = 12, 24, 48, 54, 86, 88, 172, 198 (see **Table 18-2 Selection Clock Setting**.)

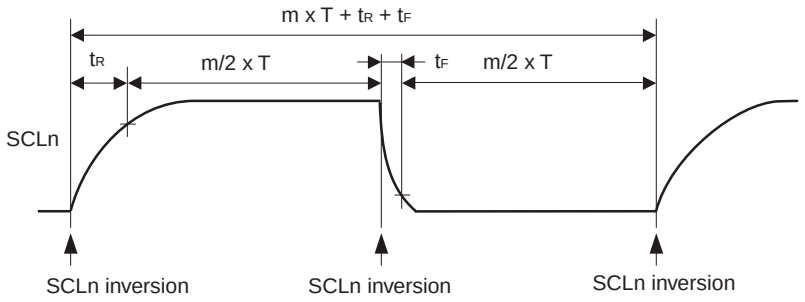
T: $1/f_{XX}$

t_R: SCLn rise time

t_F: SCLn fall time

For example, the I²Cn transfer clock frequency (f_{SCL}) when f_{XX} = 20 MHz, m = 198, t_R = 200 ns, and t_F = 50 ns is calculated using following expression.

$$f_{SCL} = 1/(198 \times 50 \text{ ns} + 200 \text{ ns} + 50 \text{ ns}) \cong 98.5 \text{ kHz}$$



The selection clock is set using a combination of the SMCn, CLn1, and CLn0 bits of IIC clock selection register n (IICCLn) and the CLXn bit of IIC function expansion register n (IICXn).

Table 18-2. Selection Clock Setting

IICXn	IICCLn			Selection Clock	Transfer clock (fxx/m)	Settable Internal System Clock Frequency (fxx) Range	Operation Mode
Bit 0	Bit 3	Bit 1	Bit 0				
CLXn	SMCn	CLn1	CLn0				
0	0	0	0	fxx/2	fxx/88	4.0 MHz to 8.38 MHz	Normal mode (SMCn = 0)
0	0	0	1	fxx/2	fxx/172	8.38 MHz to 16.76 MHz	
0	0	1	0	fxx	fxx/86	4.19 MHz to 8.38 MHz	
0	0	1	1	fxx/3	fxx/198	16.0 MHz to 19.8 MHz	
0	1	0	x	fxx/2	fxx/48	8 MHz to 16.76 MHz	High-speed mode (SMCn = 1)
0	1	1	0	fxx	fxx/24	4 MHz to 8.38 MHz	
0	1	1	1	fxx/3	fxx/54	16 MHz to 20 MHz	
1	0	x	x	Setting prohibited			
1	1	0	x	fxx/2	fxx/24	8.00 MHz to 8.38 MHz	High-speed mode (SMCn = 1)
1	1	1	0	fxx	fxx/12	4.00 MHz to 4.19 MHz	
1	1	1	1	Setting prohibited			

Remarks 1. n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

2. x: Don't care

(7) IIC shift registers 0, 1 (IIC0, IIC1)

IICn is used for serial transmission/reception (shift operations) that is synchronized with the serial clock. It can be read from or written to in 8-bit units, but data should not be written to IICn during a data transfer.

When the IICn register is written during wait, the wait is cancelled and data transfer is started (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

After reset: 00H R/W Address: FFFFFD80H, FFFFFD90H

	7	6	5	4	3	2	1	<0>
IICn								

(n = 0, 1)

(8) Slave address registers 0, 1 (SVA0, SVA1)

SVAn holds the I²C bus's slave addresses.

It can be read from or written to in 8-bit units, but bit 0 should be fixed as 0.

After reset: 00H R/W Address: FFFFFD83H, FFFFFD93H

	7	6	5	4	3	2	1	0
SVAn								0

(n = 0, 1)

18.5 Functions

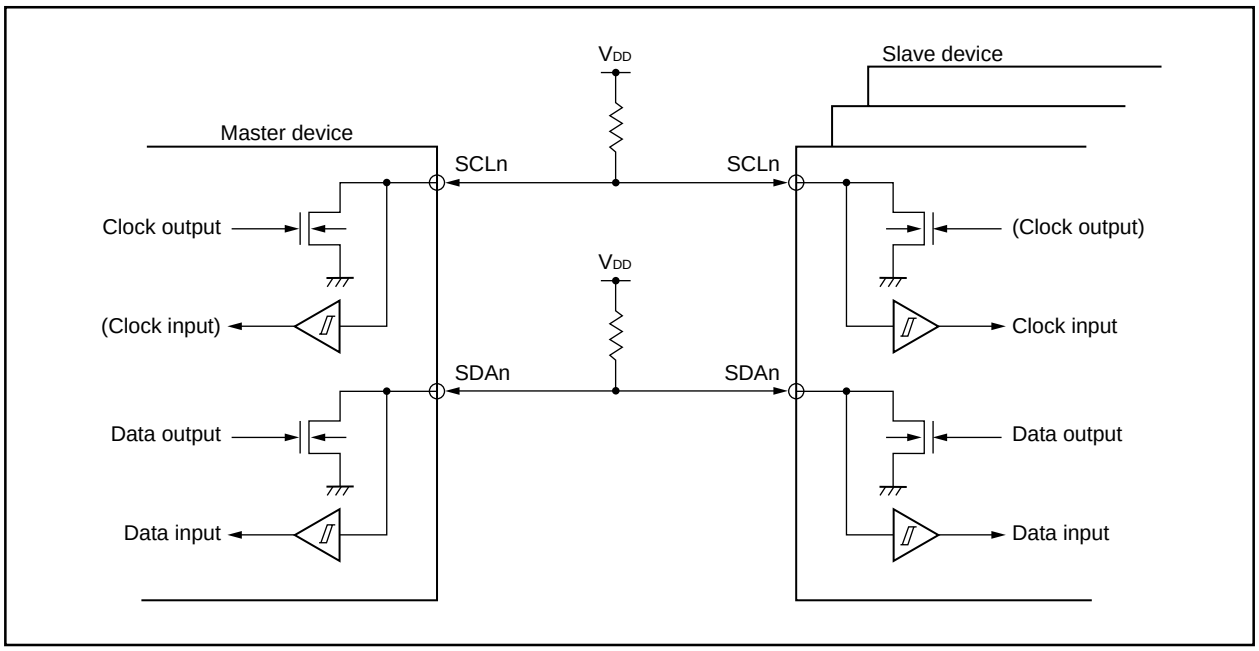
18.5.1 Pin configuration

The serial clock pin (SCLn) and serial data bus pin (SDAn) are configured as follows (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

SCLn .....This pin is used for serial clock input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.
SDAn .....This pin is used for serial data input and output.
This pin is an N-ch open-drain output for both master and slave devices. Input is Schmitt input.

Since outputs from the serial clock line and the serial data bus line are N-ch open-drain outputs, an external pull-up resistor is required.

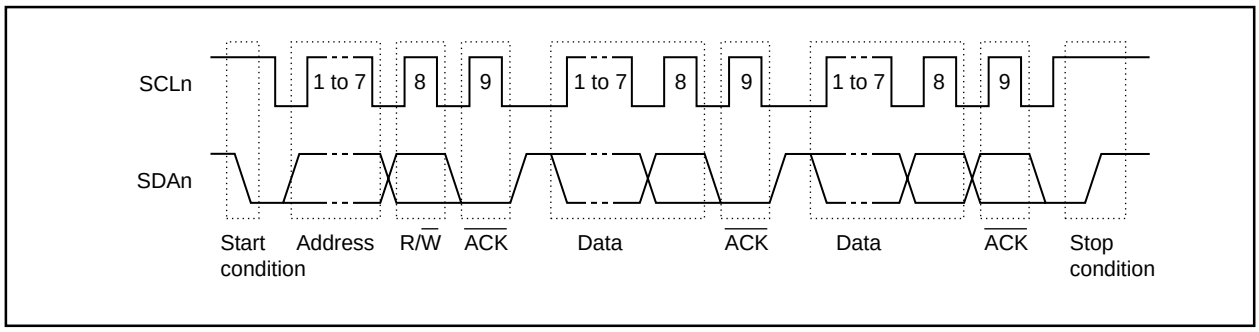
Figure 18-4. Pin Configuration Diagram



18.6 I²C Bus Definitions and Control Methods

The following section describes the I²C bus's serial data communication format and the signals used by the I²C bus. The transfer timing for the "start condition", "data", and "stop condition" output via the I²C bus's serial data bus is shown below.

Figure 18-5. I²C Bus's Serial Data Transfer Timing



The master device outputs the start condition, slave address, and stop condition.

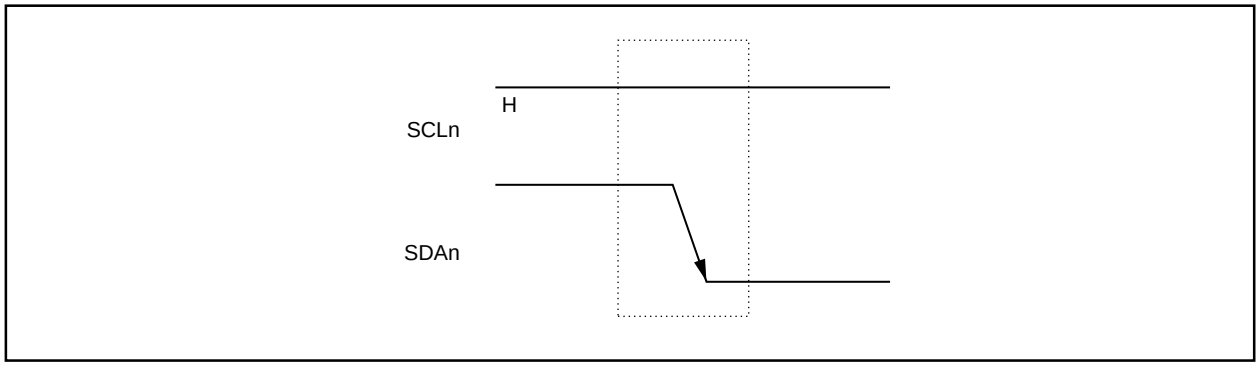
The acknowledge signal ($\overline{ACK}$) can be output by either the master or slave device (normally, it is output by the device that receives 8-bit data).

The serial clock (SCLn) is continuously output by the master device. However, in the slave device, the SCLn's low-level period can be extended and a wait can be inserted (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

18.6.1 Start condition

A start condition is met when the SCLn pin is at high level and the SDAn pin changes from high level to low level. The start conditions for the SCLn pin and SDAn pin are signals that the master device outputs to the slave device when starting a serial transfer. Start conditions can be detected when the device is used as a slave (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

Figure 18-6. Start Conditions



A start condition is output when bit 1 (STTn) of IIC control register n (IICCn) is set to 1 after a stop condition has been detected (SPDn: Bit 0 = 1 in the IIC status register n (IICSn)). When a start condition is detected, bit 1 of IICSn (STDn) is set to 1.

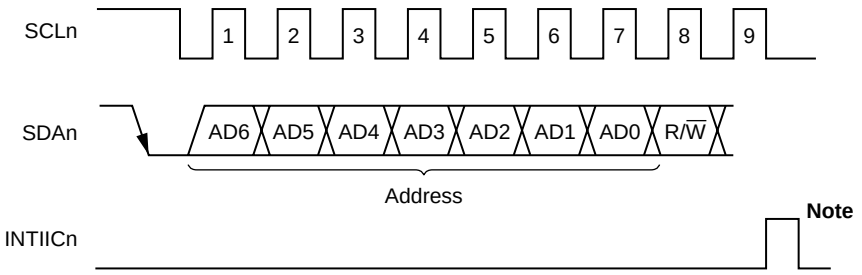
18.6.2 Addresses

The 7 bits of data that follow the start condition are defined as an address.

An address is a 7-bit data segment that is output in order to select one of the slave devices that are connected to the master device via bus lines. Therefore, each slave device connected via the bus lines must have a unique address.

The slave devices include hardware that detects the start condition and checks whether or not the 7-bit address data matches the data values stored in slave address register n (SVAn). If the address data matches the SVAn values, the slave device is selected and communicates with the master device until the master device transmits a start condition or stop condition (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

Figure 18-7. Address



Note The interrupt request signal (INTIICn) is generated if a local address or extension code is received during slave device operation.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

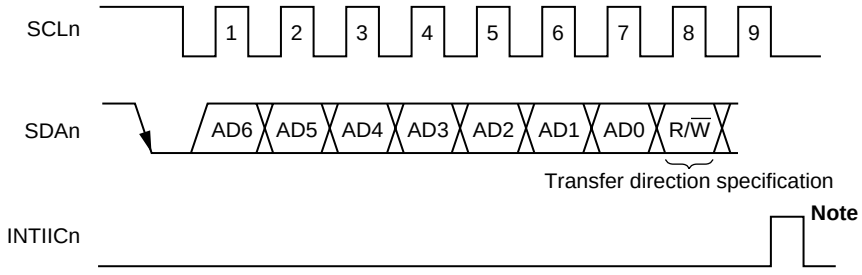
The slave address and the eighth bit, which specifies the transfer direction as described in **(3) Transfer direction specification** below, are together written to the IIC shift register (IICn) and are then output. Received addresses are written to IICn.

The slave address is assigned to the higher 7 bits of IICn.

18.6.3 Transfer direction specification

In addition to the 7-bit address data, the master device sends 1 bit that specifies the transfer direction. When this transfer direction specification bit has a value of 0, it indicates that the master device is transmitting data to a slave device. When the transfer direction specification bit has a value of 1, it indicates that the master device is receiving data from a slave device.

Figure 18-8. Transfer Direction Specification



Note The interrupt request signal (INTIICn) is generated if a local address or extension code is received during slave device operation.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

18.6.4 Acknowledge signal ($\overline{ACK}$)

The acknowledge signal ($\overline{ACK}$) is used by the transmitting and receiving devices to confirm serial data reception.

The receiving device returns one $\overline{ACK}$ signal for each 8 bits of data it receives. The transmitting device normally receives an $\overline{ACK}$ signal after transmitting 8 bits of data. However, when the master device is the receiving device, it does not output an $\overline{ACK}$ signal after receiving the final data to be transmitted. The transmitting device detects whether or not an $\overline{ACK}$ signal is returned after it transmits 8 bits of data. When an $\overline{ACK}$ signal is returned, the reception is judged as normal and processing continues. If the slave device does not return an $\overline{ACK}$ signal, the master device outputs either a stop condition or a restart condition and then stops the current transmission. Failure to return an $\overline{ACK}$ signal may be caused by the following two factors.

(a) Reception was not performed normally.

(b) The final data was received.

When the receiving device sets the SDAn line to low level during the ninth clock, the $\overline{ACK}$ signal becomes active (normal receive response).

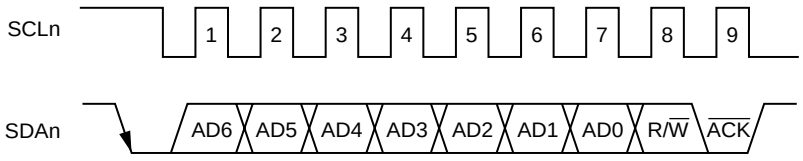
When bit 2 (ACKEn) of IIC control register n (IICCn) is set to 1, automatic $\overline{ACK}$ signal generation is enabled (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

Transmission of the eighth bit following the 7 address data bits causes bit 3 (TRCn) of IIC status register n (IICSn) to be set. When this TRCn bit's value is 0, it indicates receive mode. Therefore, ACKEn should be set to 1 (n = 0, 1).

When the slave device is receiving (when TRCn = 0), if the slave device does not need to receive any more data after receiving several bytes, setting ACKEn to 0 will prevent the master device from starting transmission of the subsequent data.

Similarly, when the master device is receiving (when TRCn = 0) and the subsequent data is not needed and when either a restart condition or a stop condition should therefore be output, setting ACKEn to 0 will prevent the $\overline{ACK}$ signal from being returned. This prevents the MSB data from being output via the SDAn line (i.e., stops transmission) during transmission from the slave device.

Figure 18-9. $\overline{ACK}$ Signal



Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

When the local address is received, an $\overline{ACK}$ signal is automatically output in synchronization with the falling edge of the SCLn's eighth clock regardless of the ACKEn value. No $\overline{ACK}$ signal is output if the received address is not a local address (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

The $\overline{ACK}$ signal output method during data reception is based on the wait timing setting, as described below.

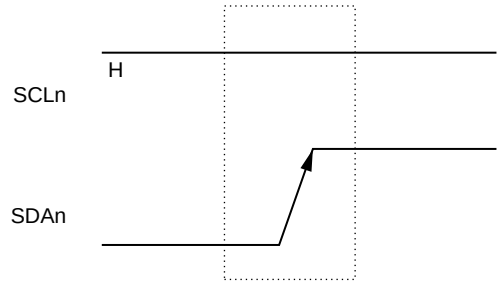
- When 8-clock wait is selected: (WTIMn = 0) — $\overline{ACK}$ signal is output at the falling edge of the SCLn's eighth clock if ACKEn is set to 1 before wait cancellation.
- When 9-clock wait is selected: (WTIMn = 1) — $\overline{ACK}$ signal is automatically output at the falling edge of the SCLn's eighth clock if ACKEn has already been set to 1.

18.6.5 Stop condition

When the SCLn pin is at high level, changing the SDAn pin from low level to high level generates a stop condition (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

A stop condition is a signal that the master device outputs to the slave device when serial transfer has been completed. Stop conditions can be detected when the device is used as a slave.

Figure 18-10. Stop Condition



Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

A stop condition is generated when bit 0 (SPTn) of IIC control register n (IICCn) is set to 1. When the stop condition is detected, bit 0 (SPDn) of IIC status register n (IICSn) is set to 1 and INTIICn is generated when bit 4 (SPIEn) of IICCn is set to 1.

18.6.6 Wait signal ($\overline{\text{WAIT}}$)

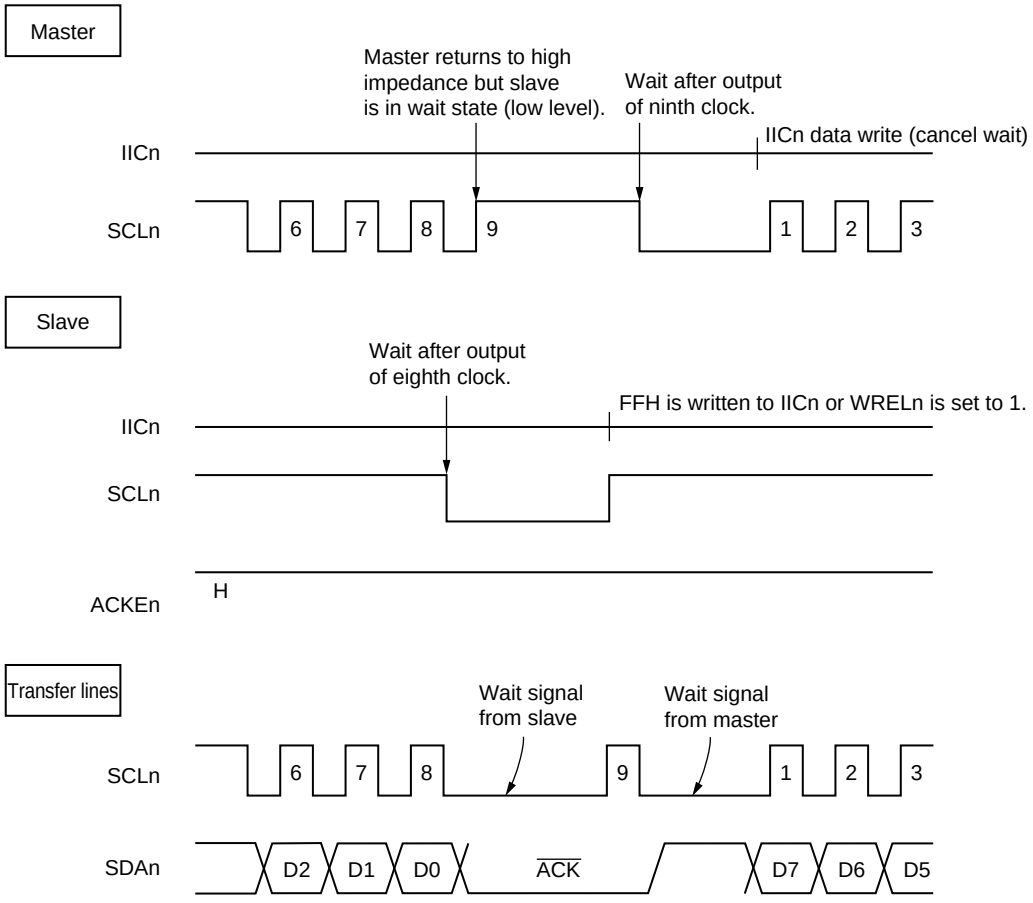
The wait signal ($\overline{\text{WAIT}}$) is used to notify the communication partner that a device (master or slave) is preparing to transmit or receive data (i.e., is in a wait state).

Setting the SCLn pin to low level notifies the communication partner of the wait status. When wait status has been canceled for both the master and slave devices, the next data transfer can begin (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

Figure 18-11. Wait Signal (1/2)

(a) When master device has a nine-clock wait and slave device has an eight-clock wait

(master: transmission, slave: reception, and ACKEn = 1)

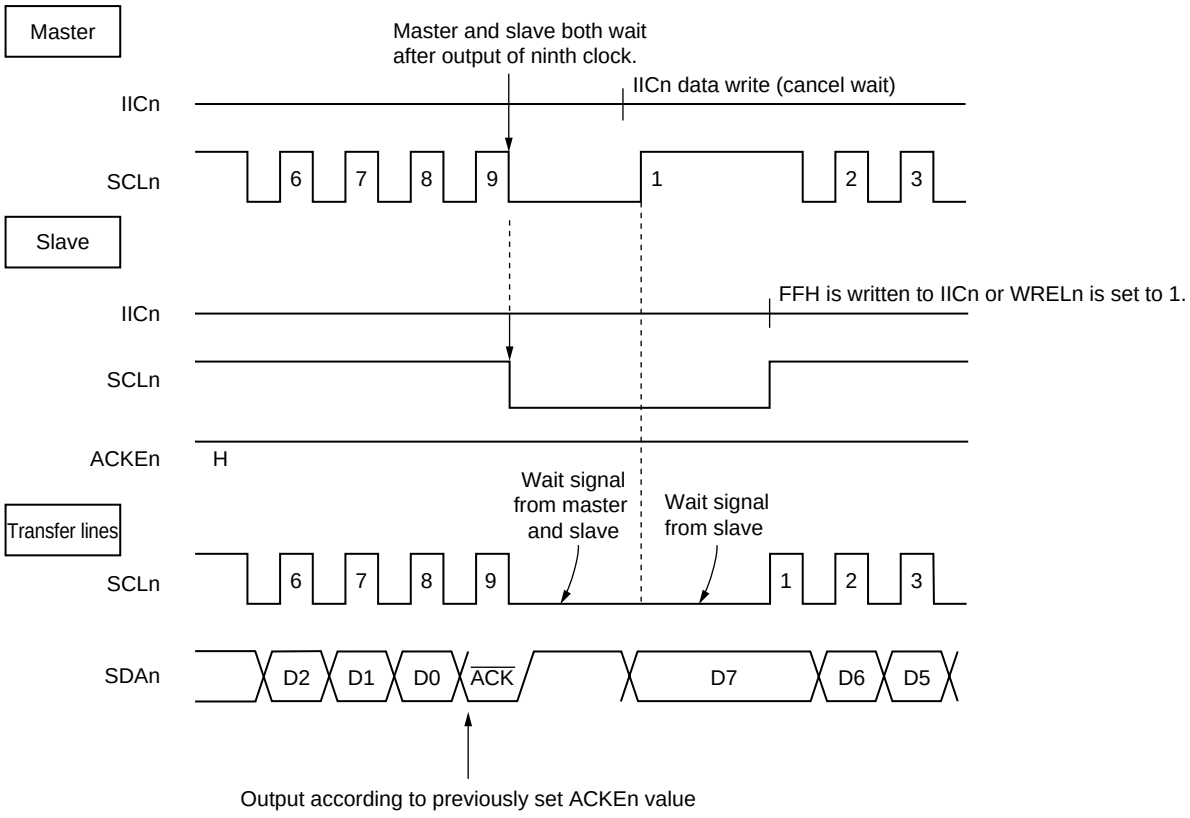


Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

Figure 18-11. Wait Signal (2/2)

(b) When master and slave devices both have a nine-clock wait

(master: transmission, slave: reception, and ACKEn = 1)



Remarks 1. ACKEn: Bit 2 of IIC control register n (IICCn)
WRELn: Bit 5 of IIC control register n (IICCn)

2. n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

A wait may be automatically generated depending on the setting for bit 3 (WTIMn) of IIC control register n (IICCn).

Normally, when bit 5 (WRELn) of IICCn is set to 1 or when FFH is written to IIC shift register n (IICn), the wait status is canceled and the transmitting side writes data to IICn to cancel the wait status.

The master device can also cancel the wait status via either of the following methods.

- By setting bit 1 (STTn) of IICCn to 1
- By setting bit 0 (SPTn) of IICCn to 1

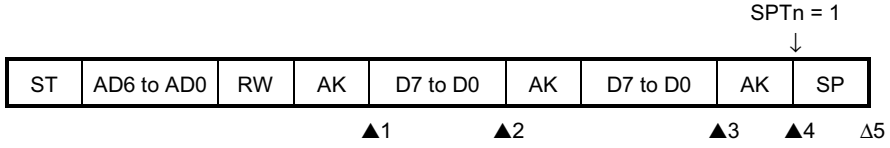
18.7 I²C Interrupt Requests (INTIICn)

The following shows the value of IIC status register n (IICSn) at the INTIICn interrupt request generation timing and at the INTIICn interrupt timing (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

18.7.1 Master device operation

(1) Start ~ Address ~ Data ~ Data ~ Stop (normal transmission/reception)

<1> When WTIMn = 0



▲1: IICSn = 10XXX110B

▲2: IICSn = 10XXX000B

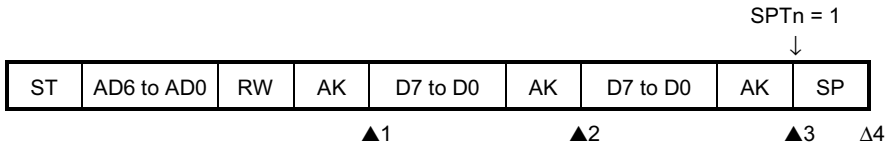
▲3: IICSn = 10XXX000B (WTIMn = 0)

▲4: IICSn = 10XXXX00B

∆ 5: IICSn = 00000001B

Remark ▲: Always generated
∆: Generated only when SPIEn = 1
X: Don't care
n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1



▲1: IICSn = 10XXX110B

▲2: IICSn = 10XXX100B

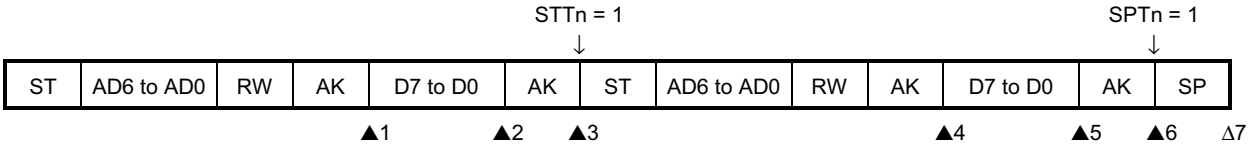
▲3: IICSn = 10XXXX00B

∆ 4: IICSn = 00000001B

Remark ▲: Always generated
∆: Generated only when SPIEn = 1
X: Don't care
n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(2) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop (restart)

<1> When WTIMn = 0



▲1: IICSn = 10XXX110B

▲2: IICSn = 10XXX000B (WTIMn = 1)

▲3: IICSn = 10XXXX00B (WTIMn = 0)

▲4: IICSn = 10XXX110B (WTIMn = 0)

▲5: IICSn = 10XXX000B (WTIMn = 1)

▲6: IICSn = 10XXXX00B

Δ 7: IICSn = 00000001B

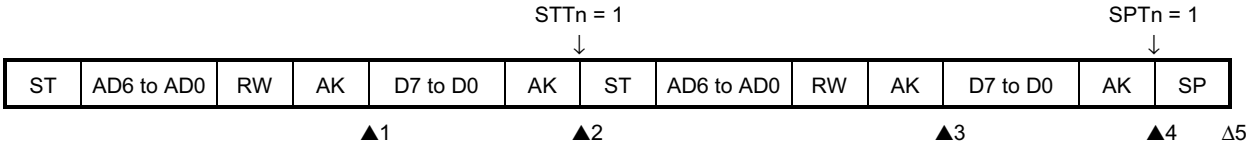
Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1



▲1: IICSn = 10XXX110B

▲2: IICSn = 10XXXX00B

▲3: IICSn = 10XXX110B

▲4: IICSn = 10XXXX00B

Δ 5: IICSn = 00000001B

Remark ▲: Always generated

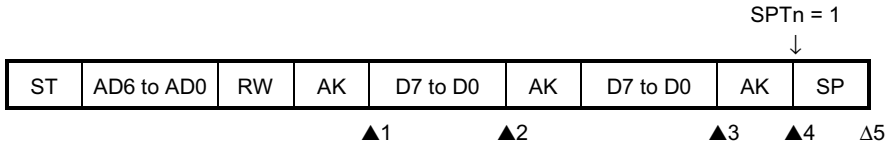
Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(3) Start ~ Code ~ Data ~ Data ~ Stop (extension code transmission)

<1> When WTIMn = 0



▲1: IICSn = 1010X110B

▲2: IICSn = 1010X000B

▲3: IICSn = 1010X000B (WTIMn = 1)

▲4: IICSn = 1010XX00B

Δ 5: IICSn = 00000001B

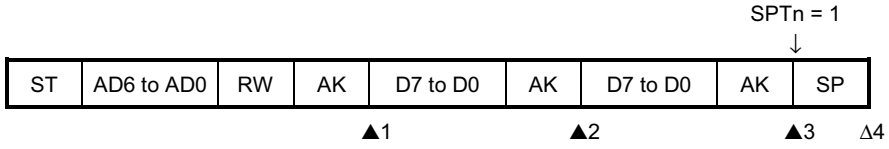
Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1



▲1: IICSn = 1010X110B

▲2: IICSn = 1010X100B

▲3: IICSn = 1010XX00B

Δ 4: IICSn = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

18.7.2 Slave device operation (when receiving slave address data (match with SVAn))

(1) Start ~ Address ~ Data ~ Data ~ Stop

<1> When WTIMn = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP
				▲1	▲2		▲3	Δ4

▲1: IICSn = 0001X110B

▲2: IICSn = 0001X000B

▲3: IICSn = 0001X000B

Δ 4: IICSn = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP
				▲1	▲2		▲3	Δ4

▲1: IICSn = 0001X110B

▲2: IICSn = 0001X100B

▲3: IICSn = 0001XX00B

Δ 4: IICSn = 00000001B

Remark ▲: Always generated

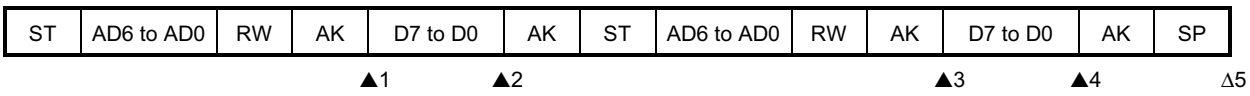
Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(2) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIMn = 0 (after restart, match with SVAn)



▲1: IICSn = 0001X110B

▲2: IICSn = 0001X000B

▲3: IICSn = 0001X110B

▲4: IICSn = 0001X000B

∆ 5: IICSn = 00000001B

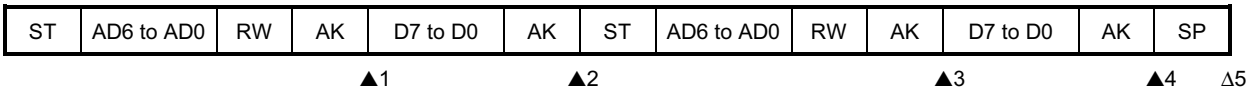
Remark ▲: Always generated

∆: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1 (after restart, match with SVAn)



▲1: IICSn = 0001X110B

▲2: IICSn = 0001XX00B

▲3: IICSn = 0001X110B

▲4: IICSn = 0001XX00B

∆ 5: IICSn = 00000001B

Remark ▲: Always generated

∆: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(3) Start ~ Address ~ Data ~ Start ~ Code ~ Data ~ Stop

<1> When WTIMn = 0 (after restart, extension code reception)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP
				▲1	▲2				▲3		▲4	Δ5

▲1: IICSn = 0001X110B

▲2: IICSn = 0001X000B

▲3: IICSn = 0010X010B

▲4: IICSn = 0010X000B

Δ 5: IICSn = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1 (after restart, extension code reception)

ST	AD6 to AD0	RW	AK	D7 to D0	AK	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP
				▲1		▲2			▲3	▲4		▲5 Δ6

▲1: IICSn = 0001X110B

▲2: IICSn = 0001XX00B

▲3: IICSn = 0010X010B

▲4: IICSn = 0010X110B

▲5: IICSn = 0010XX00B

Δ 6: IICSn = 00000001B

Remark ▲: Always generated

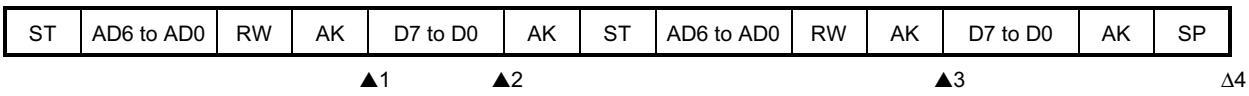
Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(4) Start ~ Address ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIMn = 0 (after restart, mismatch with address (= not extension code))



▲1: IICSn = 0001X110B

▲2: IICSn = 0001X000B

▲3: IICSn = 00000X10B

∆ 4: IICSn = 00000001B

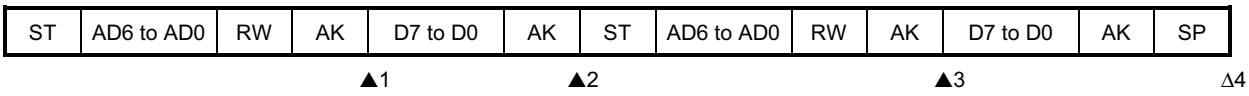
Remark ▲: Always generated

∆: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1 (after restart, mismatch with address (= not extension code))



▲1: IICSn = 0001X110B

▲2: IICSn = 0001XX00B

▲3: IICSn = 00000X10B

∆ 4: IICSn = 00000001B

Remark ▲: Always generated

∆: Generated only when SPIEn = 1

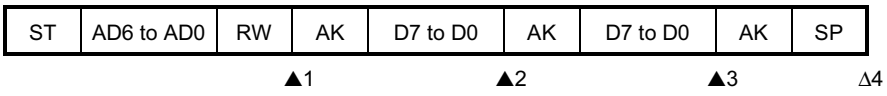
X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

18.7.3 Slave device operation (when receiving extension code)

(1) Start ~ Code ~ Data ~ Data ~ Stop

<1> When WTIMn = 0



▲1: IICSn = 0010X010B

▲2: IICSn = 0010X000B

▲3: IICSn = 0010X000B

Δ 4: IICSn = 00000001B

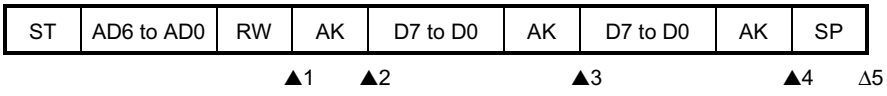
Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1



▲1: IICSn = 0010X010B

▲2: IICSn = 0010X110B

▲3: IICSn = 0010X100B

▲4: IICSn = 0010XX00B

Δ 5: IICSn = 00000001B

Remark ▲: Always generated

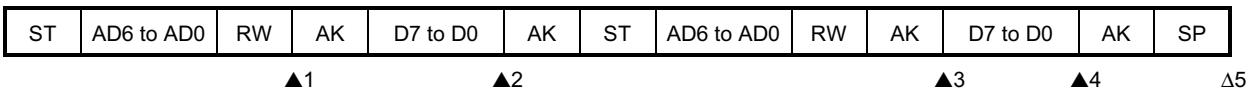
Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(2) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIMn = 0 (after restart, match with SVAn)



▲1: IICSn = 0010X010B

▲2: IICSn = 0010X000B

▲3: IICSn = 0001X110B

▲4: IICSn = 0001X000B

∆ 5: IICSn = 00000001B

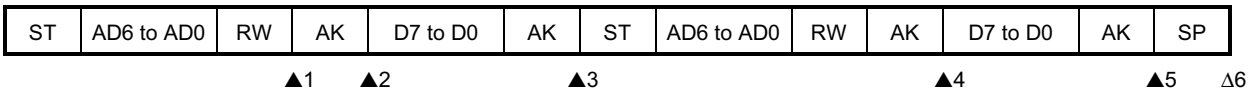
Remark ▲: Always generated

∆: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1 (after restart, match with SVAn)



▲1: IICSn = 0010X010B

▲2: IICSn = 0010X110B

▲3: IICSn = 0010XX00B

▲4: IICSn = 0001X110B

▲5: IICSn = 0001XX00B

∆ 6: IICSn = 00000001B

Remark ▲: Always generated

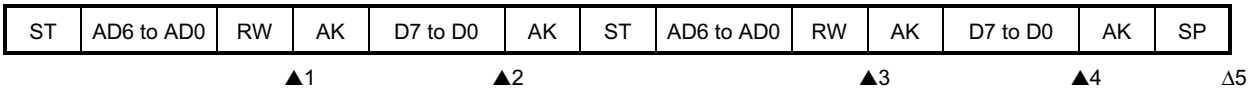
∆: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(3) Start ~ Code ~ Data ~ Start ~ Code ~ Data ~ Stop

<1> When WTIMn = 0 (after restart, extension code reception)



▲1: IICSn = 0010X010B

▲2: IICSn = 0010X000B

▲3: IICSn = 0010X010B

▲4: IICSn = 0010X000B

Δ 5: IICSn = 00000001B

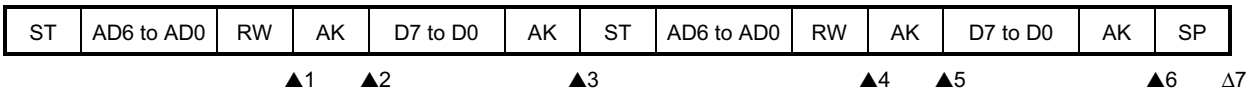
Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1 (after restart, extension code reception)



▲1: IICSn = 0010X010B

▲2: IICSn = 0010X110B

▲3: IICSn = 0010XX00B

▲4: IICSn = 0010X010B

▲5: IICSn = 0010X110B

▲6: IICSn = 0010XX00B

Δ 7: IICSn = 00000001B

Remark ▲: Always generated

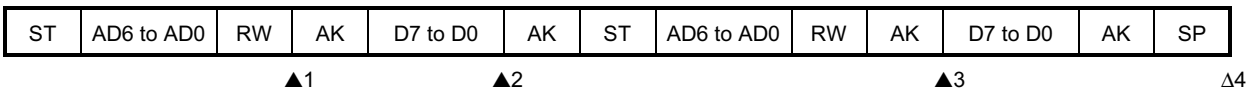
Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(4) Start ~ Code ~ Data ~ Start ~ Address ~ Data ~ Stop

<1> When WTIMn = 0 (after restart, mismatch with address (= not extension code))



▲1: IICSn = 0010X010B

▲2: IICSn = 0010X000B

▲3: IICSn = 00000X10B

Δ 4: IICSn = 00000001B

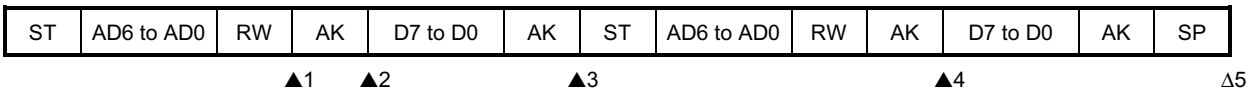
Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1 (after restart, mismatch with address (= not extension code))



▲1: IICSn = 0010X010B

▲2: IICSn = 0010X110B

▲3: IICSn = 0010XX00B

▲4: IICSn = 00000X10B

Δ 5: IICSn = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

18.7.4 Operation without communication

(1) Start ~ Code ~ Data ~ Data ~ Stop

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

Δ1

Δ 1: IICSn = 00000001B

Remark Δ: Generated only when SPIEn = 1
n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

18.7.5 Arbitration loss operation (operation as slave after arbitration loss)

(1) When arbitration loss occurs during transmission of slave address data

<1> When WTIMn = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

▲1 ▲2 ▲3 Δ4

▲1: IICSn = 0101X110B (Example: when ALDn is read during interrupt servicing)

▲2: IICSn = 0001X000B

▲3: IICSn = 0001X000B

Δ 4: IICSn = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn = 1
X: Don't care
n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

▲1 ▲2 ▲3 Δ4

▲1: IICSn = 0101X110B (Example: when ALDn is read during interrupt servicing)

▲2: IICSn = 0001X100B

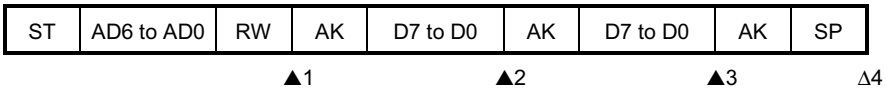
▲3: IICSn = 0001XX00B

Δ 4: IICSn = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn = 1
X: Don't care
n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(2) When arbitration loss occurs during transmission of extension code

<1> When WTIMn = 0



▲1: IICSn = 0110X010B (Example: when ALDn is read during interrupt servicing)

▲2: IICSn = 0010X000B

▲3: IICSn = 0010X000B

Δ 4: IICSn = 00000001B

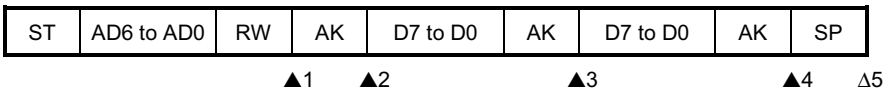
Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1



▲1: IICSn = 0110X010B (Example: when ALDn is read during interrupt servicing)

▲2: IICSn = 0010X110B

▲3: IICSn = 0010X100B

▲4: IICSn = 0010XX00B

Δ 5: IICSn = 00000001B

Remark ▲: Always generated

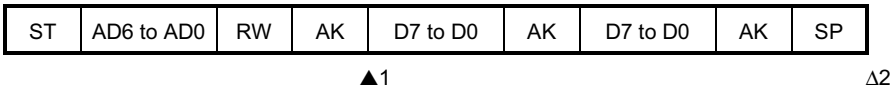
Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

18.7.6 Operation when arbitration loss occurs (no communication after arbitration loss)

(1) When arbitration loss occurs during transmission of slave address data



▲1: IICSn = 01000110B (Example: when ALDn is read during interrupt servicing)

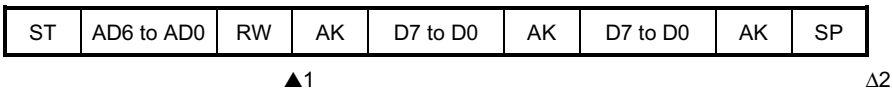
Δ 2: IICSn = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(2) When arbitration loss occurs during transmission of extension code



▲1: IICSn = 0110X010B (Example: when ALDn is read during interrupt servicing)

IICCn's LRELn is set to 1 by software

Δ 2: IICSn = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(3) When arbitration loss occurs during data transfer

<1> When WTIMn = 0

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

▲1 ▲2 Δ3

▲1: IICSn = 10001110B

▲2: IICSn = 01000000B (Example: when ALDn is read during interrupt servicing)

Δ 3: IICSn = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> When WTIMn = 1

ST	AD6 to AD0	RW	AK	D7 to D0	AK	D7 to D0	AK	SP

▲1 ▲2 Δ3

▲1: IICSn = 10001110B

▲2: IICSn = 01000100B (Example: when ALDn is read during interrupt servicing)

Δ 3: IICSn = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(4) When loss occurs due to restart condition during data transfer

<1> Not extension code (Example: mismatches with SVAn)

ST	AD6 to AD0	RW	AK	D7 to Dn	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP

▲1 ▲2 Δ3

▲1: IICSn = 1000X110B

▲2: IICSn = 01000110B (Example: when ALDn is read during interrupt servicing)

Δ 3: IICSn = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn = 1
X: Don't care
Dn = D6 to D0
n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

<2> Extension code

ST	AD6 to AD0	RW	AK	D7 to Dn	ST	AD6 to AD0	RW	AK	D7 to D0	AK	SP

▲1 ▲2 Δ3

▲1: IICSn = 1000X110B

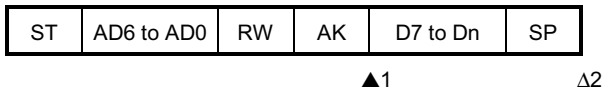
▲2: IICSn = 0110X010B (Example: when ALDn is read during interrupt servicing)

IICCn's LRELn is set to 1 by software

Δ 3: IICSn = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn = 1
X: Don't care
Dn = D6 to D0
n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(5) When loss occurs due to stop condition during data transfer



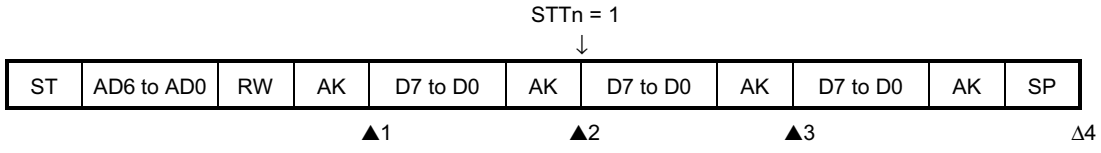
▲1: IICSn = 1000X110B

Δ 2: IICSn = 01000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn = 1
X: Don't care
Dn = D6 to D0
n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(6) When arbitration loss occurs due to low-level data when attempting to generate a restart condition

When WTIMn = 1



▲1: IICSn = 1000X110B

▲2: IICSn = 1000XX00B

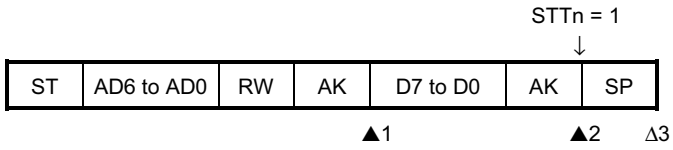
▲3: IICSn = 01000100B (Example: when ALDn is read during interrupt servicing)

Δ 4: IICSn = 00000001B

Remark ▲: Always generated
Δ: Generated only when SPIEn = 1
X: Don't care
n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(7) When arbitration loss occurs due to a stop condition when attempting to generate a restart condition

When WTIMn = 1



▲1: IICSn = 1000X110B

▲2: IICSn = 1000XX00B

Δ 3: IICSn = 01000001B

Remark ▲: Always generated

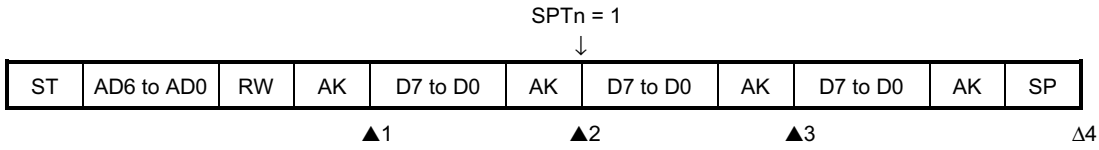
Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(8) When arbitration loss occurs due to low-level data when attempting to generate a stop condition

When WTIMn = 1



▲1: IICSn = 1000X110B

▲2: IICSn = 1000XX00B

▲3: IICSn = 01000000B (Example: when ALDn is read during interrupt servicing)

Δ 4: IICSn = 00000001B

Remark ▲: Always generated

Δ: Generated only when SPIEn = 1

X: Don't care

n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

18.8 Interrupt Request (INTIICn) Generation Timing and Wait Control

The setting of bit 3 (WTIMn) in IIC control register n (IICCn) determines the timing by which INTIICn is generated and the corresponding wait control, as shown below.

Table 18-3. INTIICn Generation Timing and Wait Control

WTIMn	During Slave Device Operation			During Master Device Operation		
	Address	Data Reception	Data Transmission	Address	Data Reception	Data Transmission
0	9 Notes 1, 2	8 Note 2	8 Note 2	9	8	8
1	9 Notes 1, 2	9 Note 2	9 Note 2	9	9	9

Notes 1. The slave device's INTIICn signal and wait period occurs at the falling edge of the ninth clock only when there is a match with the address set to slave address register n (SVAn).
At this point, $\overline{ACK}$ is output regardless of the value set to IICCn's bit 2 (ACKEn). For a slave device that has received an extension code, INTIICn occurs at the falling edge of the eighth clock.
When the address does not match after restart, IITIICn is generated at the falling of the 9th clock, but no wait occurs.

2. If the received address does not match the contents of slave address register n (SVAn) and extension codes have not been received, neither INTIICn nor a wait occurs.

Remarks 1. The numbers in the table indicate the number of the serial clock's clock signals. Interrupt requests and wait control are both synchronized with the falling edge of these clock signals.

2. n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(1) During address transmission/reception

- Slave device operation: Interrupt and wait timing are determined depending on the conditions in Notes 1 and 2 above regardless of the WTIMn bit.
- Master device operation: Interrupt and wait timing occur at the falling edge of the ninth clock regardless of the WTIMn bit.

(2) During data reception

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIMn bit.

(3) During data transmission

- Master/slave device operation: Interrupt and wait timing are determined according to the WTIMn bit.

(4) Wait cancellation method

The four wait cancellation methods are as follows.

- By setting bit 5 (WRELn) of IIC control register n (IICCn) to 1
- By writing to IIC shift register n (IICn)
- By start condition setting (bit 1 (STTn) of IIC control register n (IICCn) = 1)
- By step condition setting (bit 0 (SPTn) of IIC control register n (IICCn) = 1)

Caution Master only

When an 8-clock wait has been selected (WTIMn = 0), the output level of $\overline{ACK}$ must be determined prior to wait cancellation.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

(5) Stop condition detection

INTIICn is generated when a stop condition is detected.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

18.9 Address Match Detection Method

When in I^2C bus mode, the master device can select a particular slave device by transmitting the corresponding slave address.

Address match detection is performed automatically by hardware. An interrupt request (INTIICn) occurs when a local address has been set to slave address register n (SVAn) and when the address set to SVAn matches the slave address sent by the master device, or when an extension code has been received (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

18.10 Error Detection

In I^2C bus mode, the status of the serial data bus (SDAn) during data transmission is captured by IIC shift register n (IICn) of the transmitting device, so the IICn data prior to transmission can be compared with the transmitted IICn data to enable detection of transmission errors. A transmission error is judged as having occurred when the compared data values do not match (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

18.11 Extension Code

(1) When the higher 4 bits of the receive address are either 0000 or 1111, the extension code flag (EXCn) is set for extension code reception and an interrupt request (INTIICn) is issued at the falling edge of the eighth clock.
The local address stored in slave address register n (SVAn) is not affected.

(2) If 11110xx0 is set to SVAn by a 10-bit address transfer and 11110xx0 is transferred from the master device, the results are as follows. Note that INTIICn occurs at the falling edge of the eighth clock.

- Higher 4 bits of data match: EXCn = 1**Note**
- 7 bits of data match: COIn = 1**Note**

Note EXCn: Bit 5 of IIC status register n (IICSn)
COIn: Bit 4 of IIC status register n (IICSn)

(3) Since the processing after the interrupt request occurs differs according to the data that follows the extension code, such processing is performed by software.
For example, when operation as a slave is not desired after the extension code is received, set bit 6 (LRELn) of IIC control register n (IICCn) to 1 and the CPU will enter the next communication wait state.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

Table 18-4. Extension Code Bit Definitions

Slave Address	R/W Bit	Description
0000 000	0	General call address
0000 000	1	Start byte
0000 001	X	CBUS address
0000 010	X	Address that is reserved for different bus format
1111 0xx	X	10-bit slave address specification

18.12 Arbitration

When several master devices simultaneously output a start condition (when STTn is set to 1 before STDn is set to 1[Note]), communication among the master devices is performed as the number of clocks is adjusted until the data differs. This kind of operation is called arbitration (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

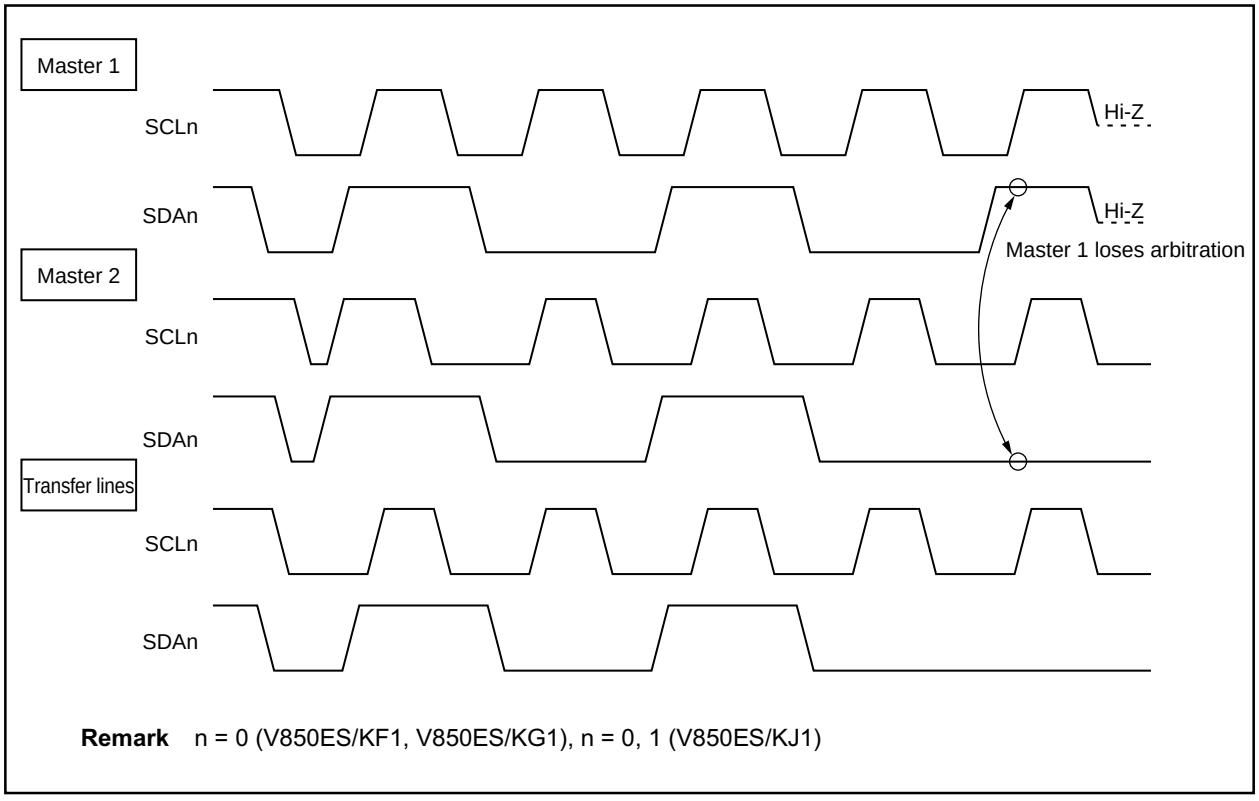
When one of the master devices loses in arbitration, an arbitration loss flag (ALDn) in IIC status register n (IICSn) is set (1) via the timing by which the arbitration loss occurred, and the SCLn and SDAn lines are both set for high impedance, which releases the bus.

The arbitration loss is detected based on the timing of the next interrupt request (the eighth or ninth clock, when a stop condition is detected, etc.) and the ALDn = 1 setting that has been made by software.

For details of interrupt request timing, see **18.7 I²C Interrupt Requests (INTIICn)**.

Note STDn: Bit 1 of IIC status register n (IICSn)
STTn: Bit 1 of IIC control register n (IICCn)

Figure 18-12. Arbitration Timing Example



Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

Table 18-5. Status During Arbitration and Interrupt Request Generation Timing

Status During Arbitration	Interrupt Request Generation Timing
During address transmission	At falling edge of eighth or ninth clock following byte transfer Note 1
Read/write data after address transmission	
During extension code transmission	
Read/write data after extension code transmission	
During data transmission	
During $\overline{ACK}$ signal transfer period after data reception	
When restart condition is detected during data transfer	
When stop condition is detected during data transfer	When stop condition is output (when SPIEn = 1) Note 2
When data is at low level while attempting to output a restart condition	At falling edge of eighth or ninth clock following byte transfer Note 1
When stop condition is detected while attempting to output a restart condition	When stop condition is output (when SPIEn = 1) Note 2
When data is at low level while attempting to output a stop condition	At falling edge of eighth or ninth clock following byte transfer Note 1
When SCLn is at low level while attempting to output a restart condition	

Notes 1. When WTIMn (bit 3 of the IIC control register n (IICCn)) = 1, an interrupt request occurs at the falling edge of the ninth clock. When WTIMn = 0 and the extension code's slave address is received, an interrupt request occurs at the falling edge of the eighth clock.

2. When there is a possibility that arbitration will occur, set SPIEn = 1 for master device operation.

Remarks 1. SPIEn: Bit 4 of IIC control register n (IICCn)

2. n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

18.13 Wakeup Function

The I²C bus slave function is a function that generates an interrupt request (INTIICn) when a local address or extension code has been received.

This function makes processing more efficient by preventing unnecessary interrupt requests from occurring when addresses do not match.

When a start condition is detected, wakeup standby mode is set. This wakeup standby mode is in effect while addresses are transmitted due to the possibility that an arbitration loss may change the master device (which has output a start condition) to a slave device.

However, when a stop condition is detected, bit 4 (SPIEn) of IIC control register n (IICCn) is set regardless of the wake up function, and this determines whether interrupt requests are enabled or disabled (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

18.14 Communication Reservation

18.14.1 When communication reservation function is enabled (IICRSVn bit of IICFn register = 0)

To start master device communications when not currently using a bus, a communication reservation can be made to enable transmission of a start condition when the bus is released. There are two modes under which the bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{\text{ACK}}$ is not returned and the bus was released when bit 6 (LRELn) of IIC control register n (IICCn) was set to “1”).

If bit 1 (STTn) of IICCn is set (1) while the bus is not used, a start condition is automatically generated and wait status is set after the bus is released (after a stop condition is detected).

When the bus release is detected (when a stop condition is detected), writing to IIC shift register n (IICn) causes the master’s address transfer to start. At this point, IICCn’s bit 4 (SPIEn) should be set (1).

When STTn has been set (1), the operation mode (as start condition or as communication reservation) is determined according to the bus status.

If the bus has been released.....a start condition is generated
If the bus has not been released (standby mode).....communication reservation

To detect which operation mode has been determined for STTn, set STTn (1), wait for the wait period, then check the MSTSn (bit 7 of IIC status register n (IICSn)).

Wait periods, which should be set via software, are listed in Table 18-6. These wait periods can be set via the settings for bits 3, 1, and 0 (SMCn, CLn1, and CLn0) in IIC clock selection register n (IICCLn).

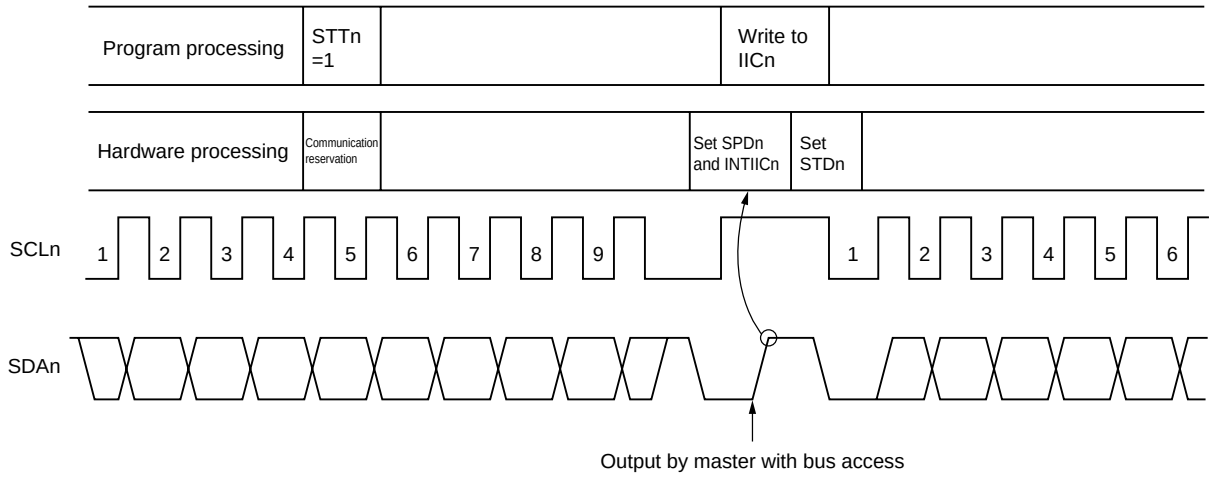
Table 18-6. Wait Periods

SMCn	CLn1	CLn0	Wait Period
0	0	0	26 clocks
0	0	1	46 clocks
0	1	0	92 clocks
0	1	1	37 clocks
1	0	0	16 clocks
1	0	1	
1	1	0	32 clocks
1	1	1	13 clocks

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

The communication reservation timing is shown below.

Figure 18-13. Communication Reservation Timing

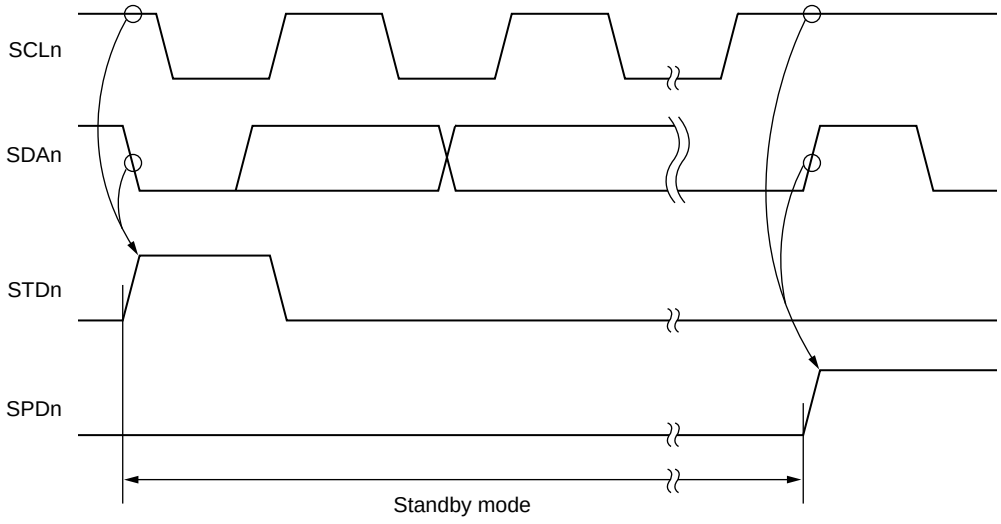


IICn: IIC shift register n
STTn: Bit 1 of IIC control register n (IICCn)
STDn: Bit 1 of IIC status register n (IICSn)
SPDn: Bit 0 of IIC status register n (IICSn)

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

Communication reservations are accepted via the following timing. After bit 1 (STDn) of IIC status register n (IICSn) is set to 1, a communication reservation can be made by setting bit 1 (STTn) of IIC control register n (IICCn) to 1 before a stop condition is detected (n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)).

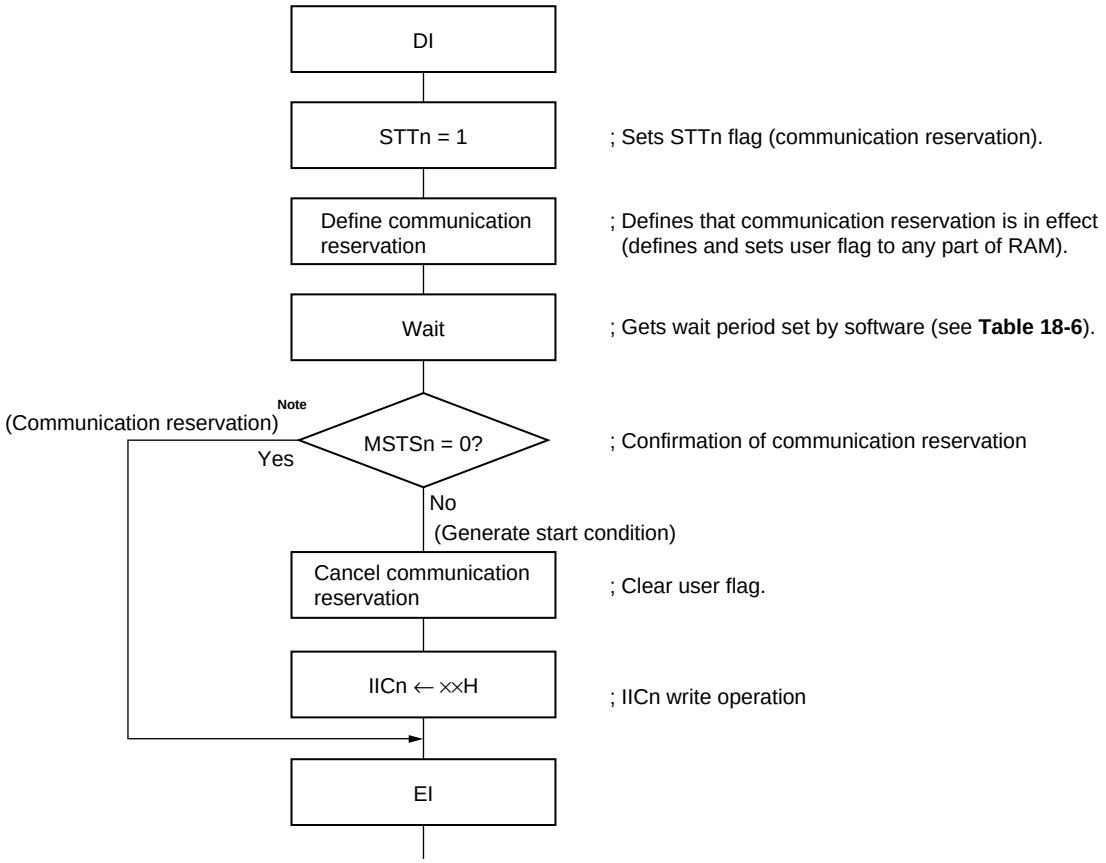
Figure 18-14. Timing for Accepting Communication Reservations



Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

The communication reservation flowchart is illustrated below.

Figure 18-15. Communication Reservation Flowchart



Note The communication reservation operation executes a write to IIC shift register n (IICn) when a stop condition interrupt request occurs.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

★ **18.14.2 When communication reservation function is disabled (IICRSVn bit of IICFn register = 1)**

When the STTn bit of the IICCn register is set when the bus is not used in a communication during bus communication, this request is rejected and a start condition is not generated. The following two statuses are included in the status where bus is not used.

- When arbitration results in neither master nor slave operation
- When an extension code is received and slave operation is disabled ($\overline{ACK}$ signal is not returned and the bus was released when the LRELn bit of the IICCn register was set to 1)

To confirm whether the start condition was generated or request was rejected, check the STCFn flag of the IICFn register. The time shown in Table 18-7 is required until the STCFn flag is set after setting the STTn bit = 1. Therefore, secure the time by software.

Table 18-7. Wait Periods

CLn1	CLn0	Wait Period
0	0	6 clocks
0	1	6 clocks
1	0	3 clocks
1	1	9 clocks

Remarks 1. ×: don't care

2. n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

18.15 Cautions

(1) When STCENn bit of IICFn register = 0

Immediately after I²Cn operation is enabled, the bus communication status (IICBSYn bit of IICFn register = 1) is recognized regardless of the actual bus status. To execute master communication in the status where a stop condition has not been detected, generate a stop condition and then release the bus before starting the master communication.

Use the following sequence for generating a stop condition.

<1> Set the IICCLn register.
<2> Set the IICEn bit of the IICCn register.
<3> Set the SPTn bit of the IICCn register.

(2) When STCENn bit of IICFn register = 1

Immediately after I²Cn operation is enabled, the bus released status (IICBSYn bit = 0) is recognized regardless of the actual bus status. To issue the first start condition (STTn bit of IICCn register = 1), it is necessary to confirm that the bus has been released, so as to not disturb other communications.

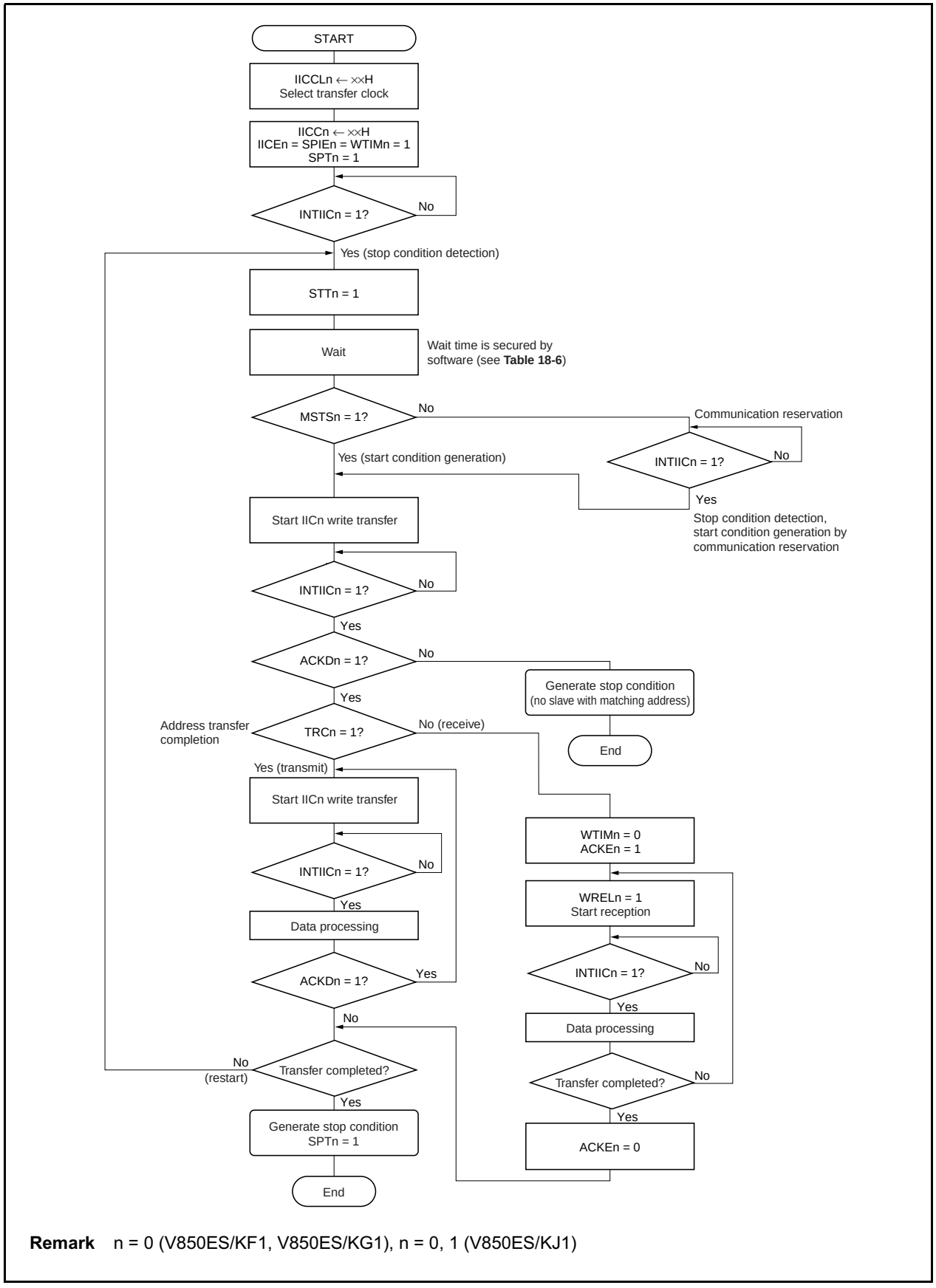
Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

★ 18.16 Communication Operations

18.16.1 Master operation 1

The following shows the flowchart for master communication when the communication reservation function is enabled (IICRSVn bit of IICFn register = 0) and the master operation is started after a stop condition is detected (STCENn bit of IICFn register = 0).

Figure 18-16. Master Operation Flowchart (1)

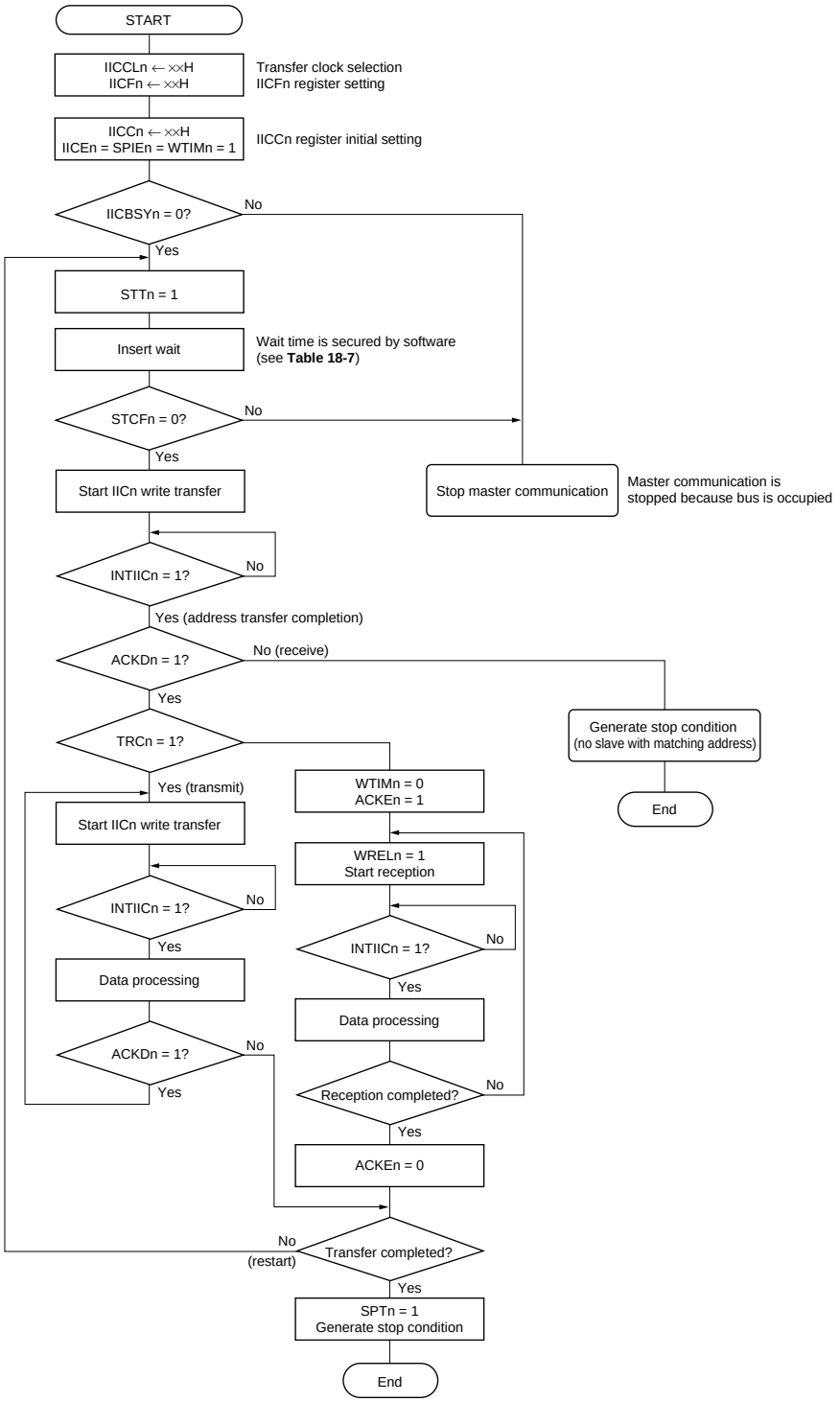


Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

★ 18.16.2 Master operation 2

The following shows the flowchart for master communication when the communication reservation function is disabled (IICRSVn bit = 1) and the master operation is started without detecting a stop condition (STCENn bit = 1).

Figure 18-17. Master Operation Flowchart (2)



Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

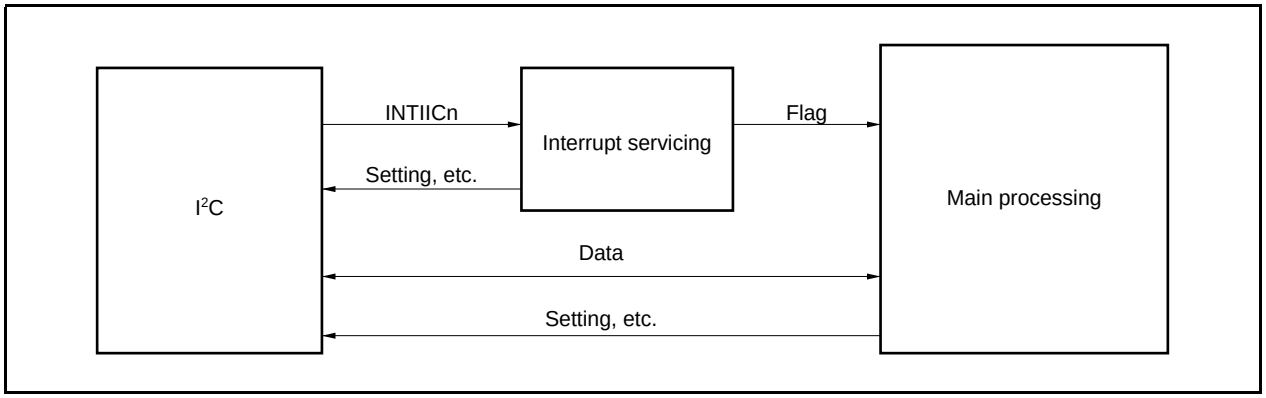
★ **18.16.3 Slave operation**

The following shows the processing procedure of the slave operation.

Basically, the operation of the slave device is event-driven. Therefore, processing by an INTIICn interrupt (processing requiring a significant change of the operation status, such as stop condition detection during communication) is necessary.

The following description assumes that data communication does not support extension codes. Also, it is assumed that the INTIICn interrupt servicing performs only status change processing and that the actual data communication is performed during the main processing.

Figure 18-18. Software Outline During Slave Operation



Therefore, the following three flags are prepared so that the data transfer processing can be performed by transmitting these flags to the main processing instead of INTIICn.

(1) Communication mode flag

This flag indicates the following communication statuses.

Clear mode: Data communication not in progress

Communication mode: Data communication in progress (valid address detection stop condition detection, acknowledgment from master not detected, address mismatch)

(2) Ready flag

This flag indicates that data communication is enabled. This is the same status as an INTIICn interrupt during normal data transfer. This flag is set in the interrupt processing block and cleared in the main processing block. The ready flag for the first data for transmission is not set in the interrupt processing block, so the first data is transmitted without clearance processing (the address match is regarded as a request for the next data).

(3) Communication direction flag

This flag indicates the direction of communication and is the same as the value of TRCn.

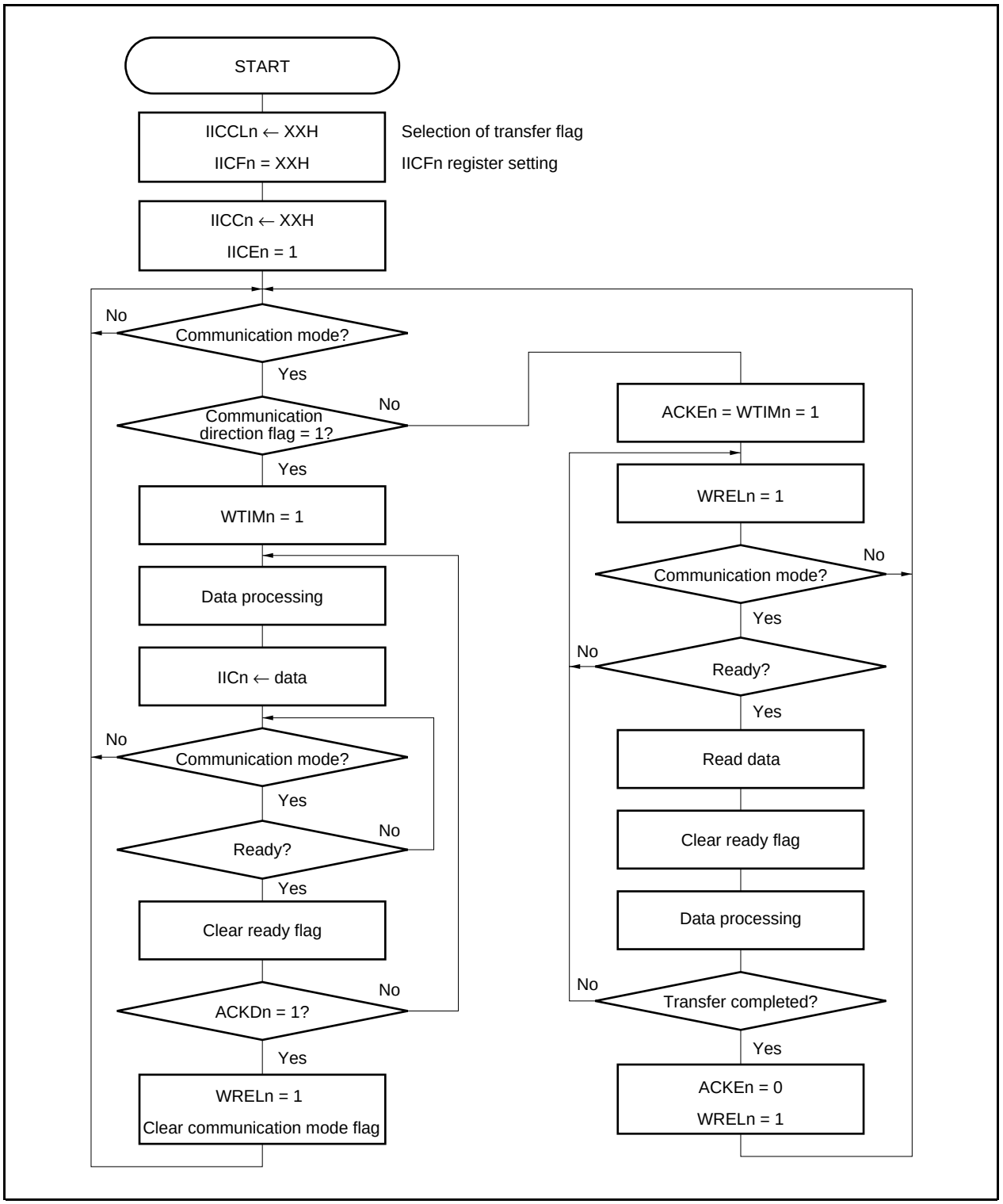
The following shows the operation of the main processing block during slave operation.

Start I²Cn and wait for the communication enabled status. When communication is enabled, perform transfer using the communication mode flag and ready flag (the processing of the stop condition and start condition is performed by interrupts, conditions are confirmed by flags).

For transmission, repeat the transmission operation until the master device stops returning acknowledgment. When the master device stops returning acknowledgment, transfer is complete.

For reception, receive the required number of data and do not return acknowledgment for the next data immediately after transfer is complete. After that, the master device generates the stop condition or restart condition. This causes exit from communications.

Figure 18-19. Slave Operation Flowchart (1)



The following shows an example of the processing of the slave device by an INTIICn interrupt (it is assumed that no extension codes are used here). During an INTIICn interrupt, the status is confirmed and the following steps are executed.

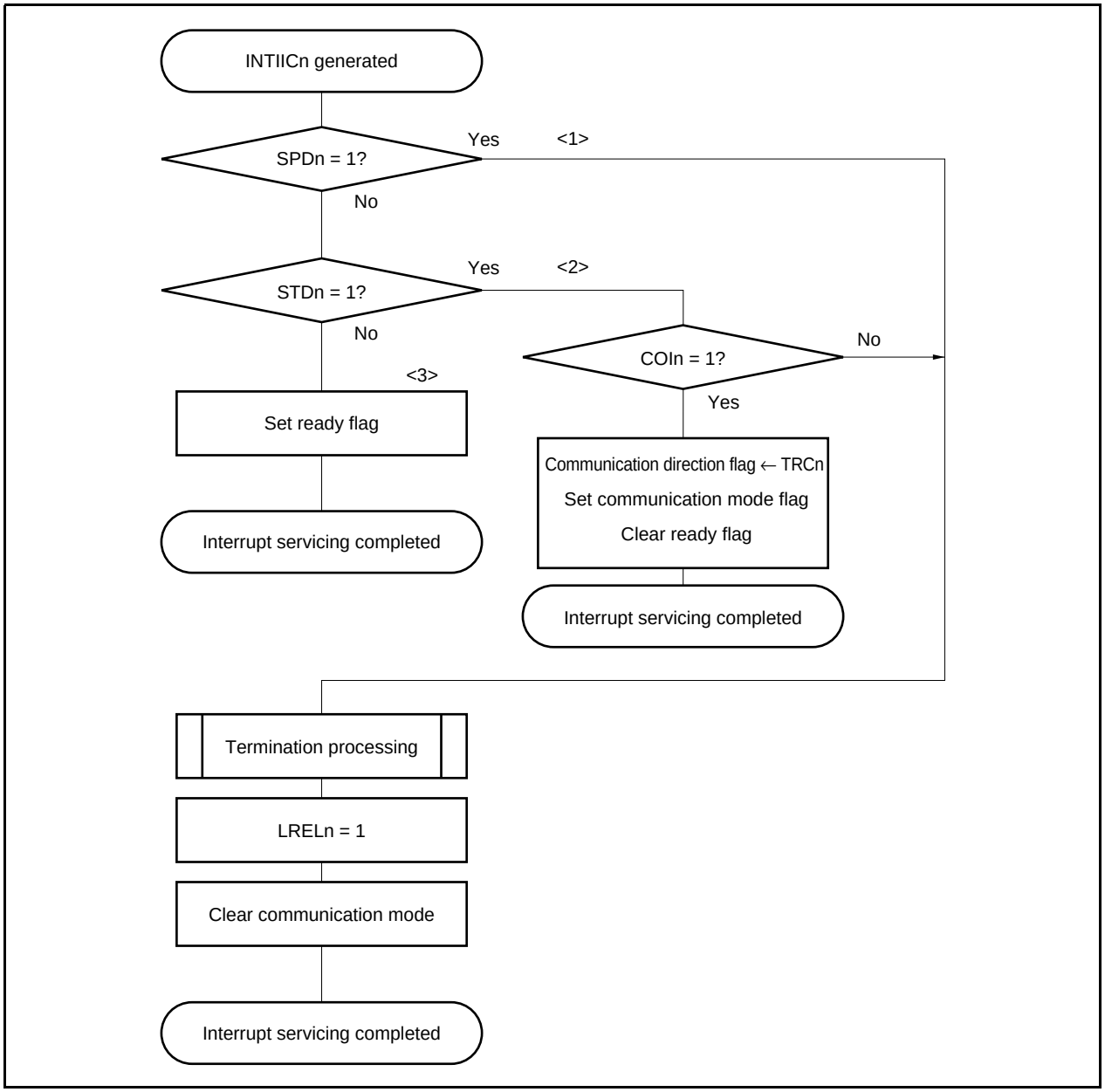
<1> When a stop condition is detected, communication is terminated.

<2> When a start condition is detected, the address is confirmed. If the address does not match, communication is terminated. If the address matches, the communication mode is set and wait is released, and operation returns from the interrupt (the ready flag is cleared).

<3> For data transmission/reception, when the ready flag is set, operation returns from the interrupt while the IIC0 bus remains in the wait status.

Remark <1> to <3> in the above correspond to <1> to <3> in Figure 18-20 Slave Operation Flowchart (2).

Figure 18-20. Slave Operation Flowchart (2)



18.17 Timing of Data Communication

When using I²C bus mode, the master device outputs an address via the serial bus to select one of several slave devices as its communication partner.

After outputting the slave address, the master device transmits the TRCn bit (bit 3 of IIC status register n (IICSn)) that specifies the data transfer direction and then starts serial communication with the slave device.

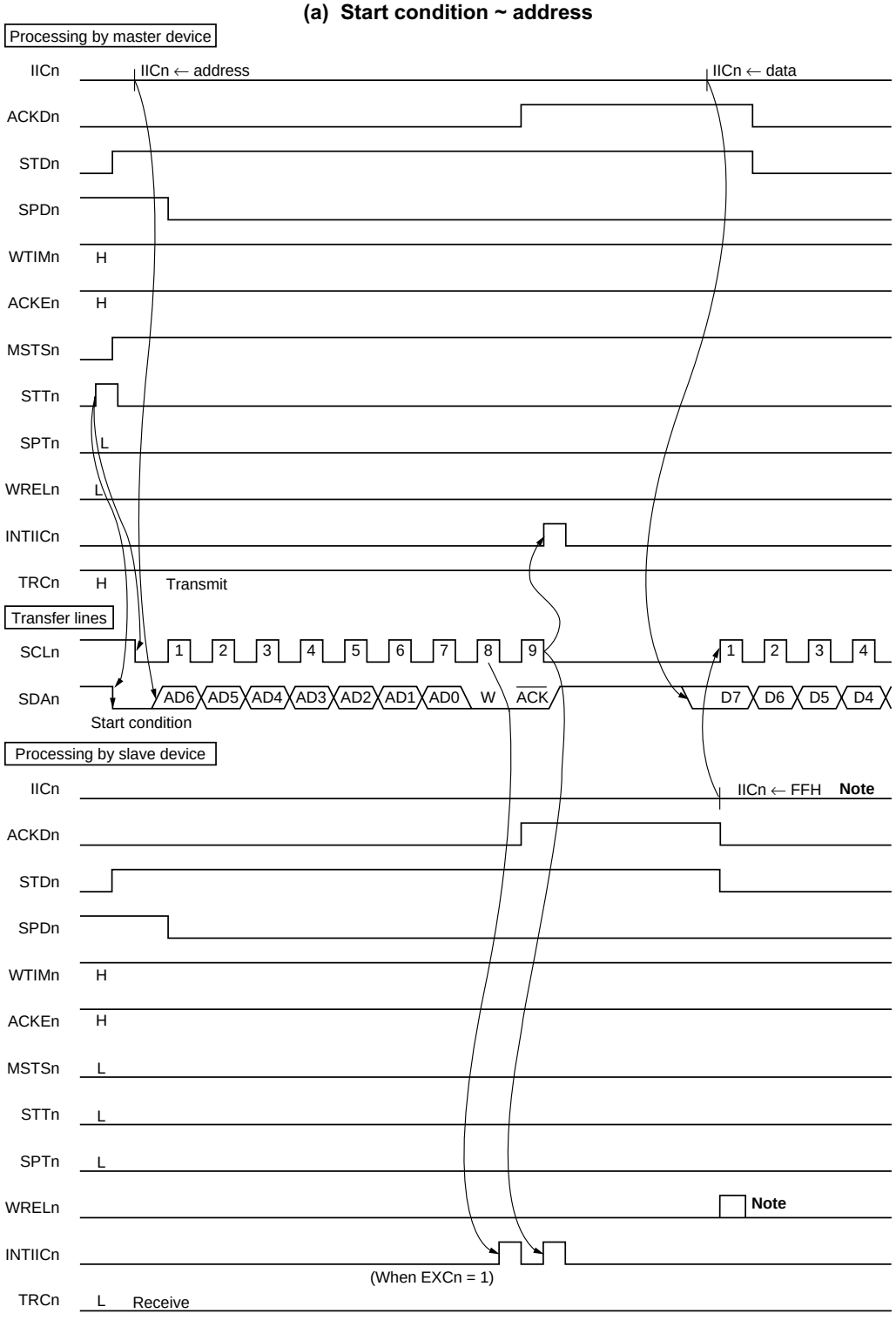
IIC shift register n (IICn)'s shift operation is synchronized with the falling edge of the serial clock (SCLn). The transmit data is transferred to the SO latch and is output (MSB first) via the SDAn pin.

Data input via the SDAn pin is captured by IICn at the rising edge of SCLn.

The data communication timing is shown below.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

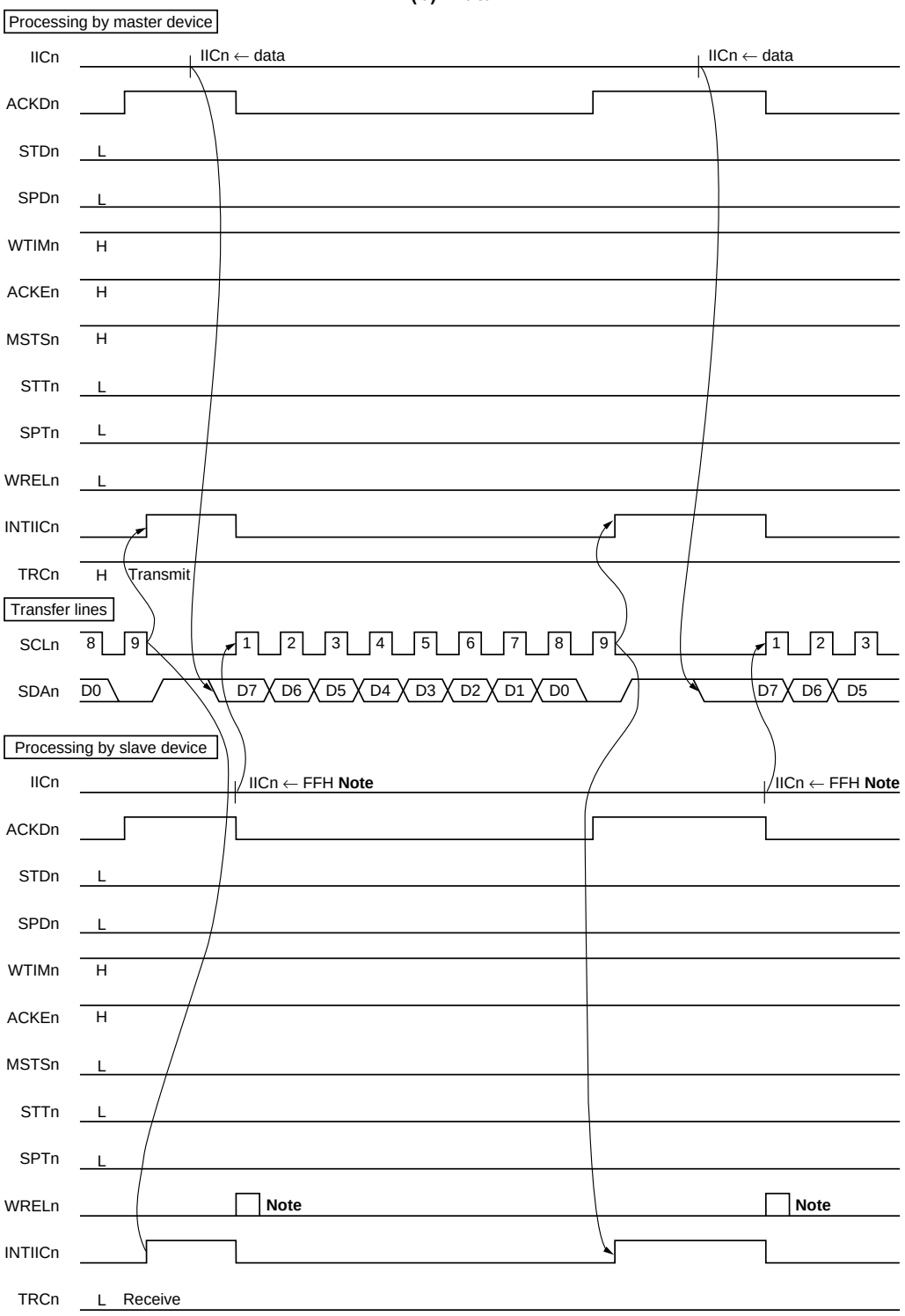
Figure 18-21. Example of Master to Slave Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)



Note To cancel slave wait, write FFH to IICn or set WRELn.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

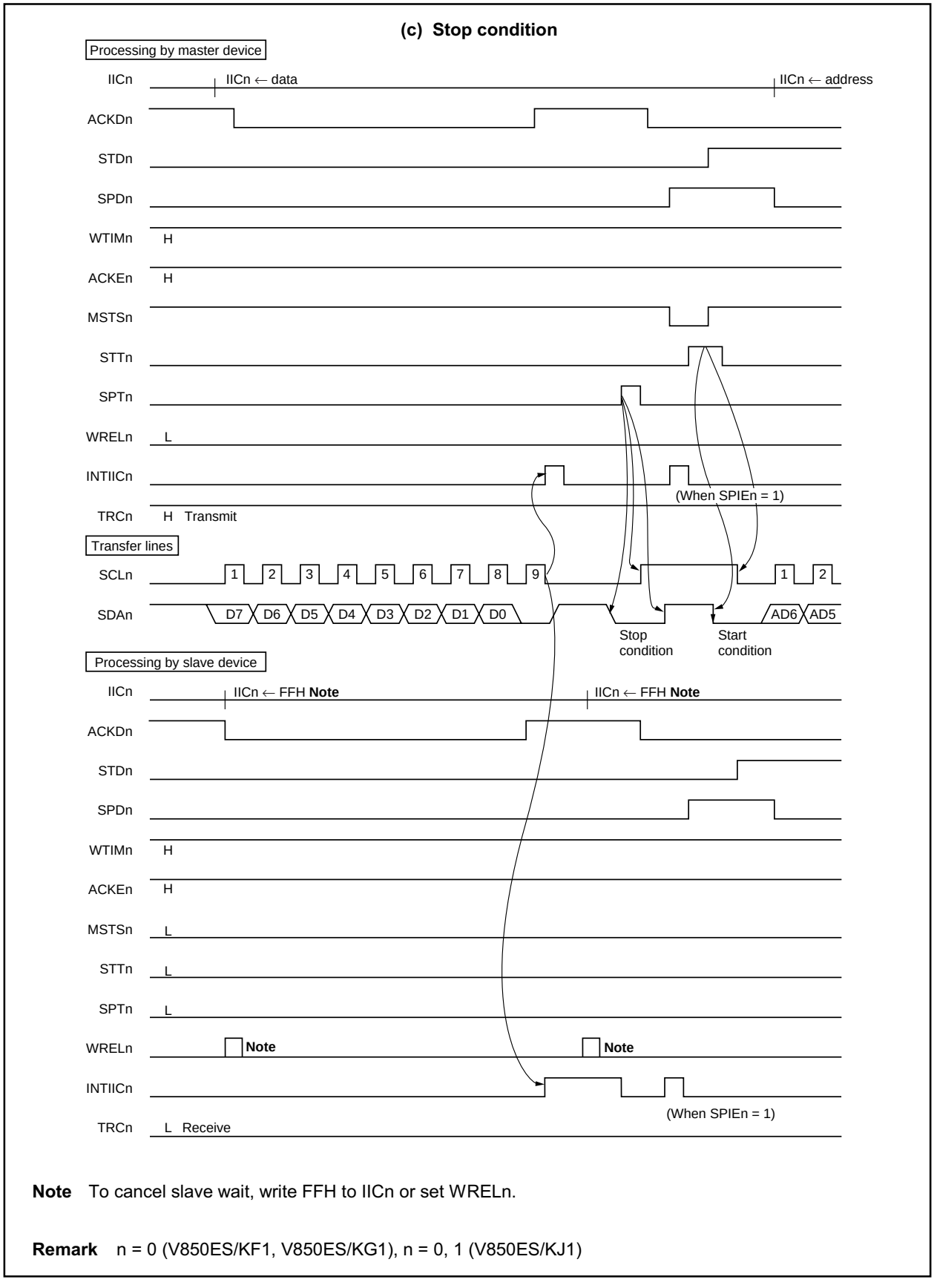
Figure 18-21. Example of Master to Slave Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (2/3)



Note To cancel slave wait, write FFH to IICn or set WRELn.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

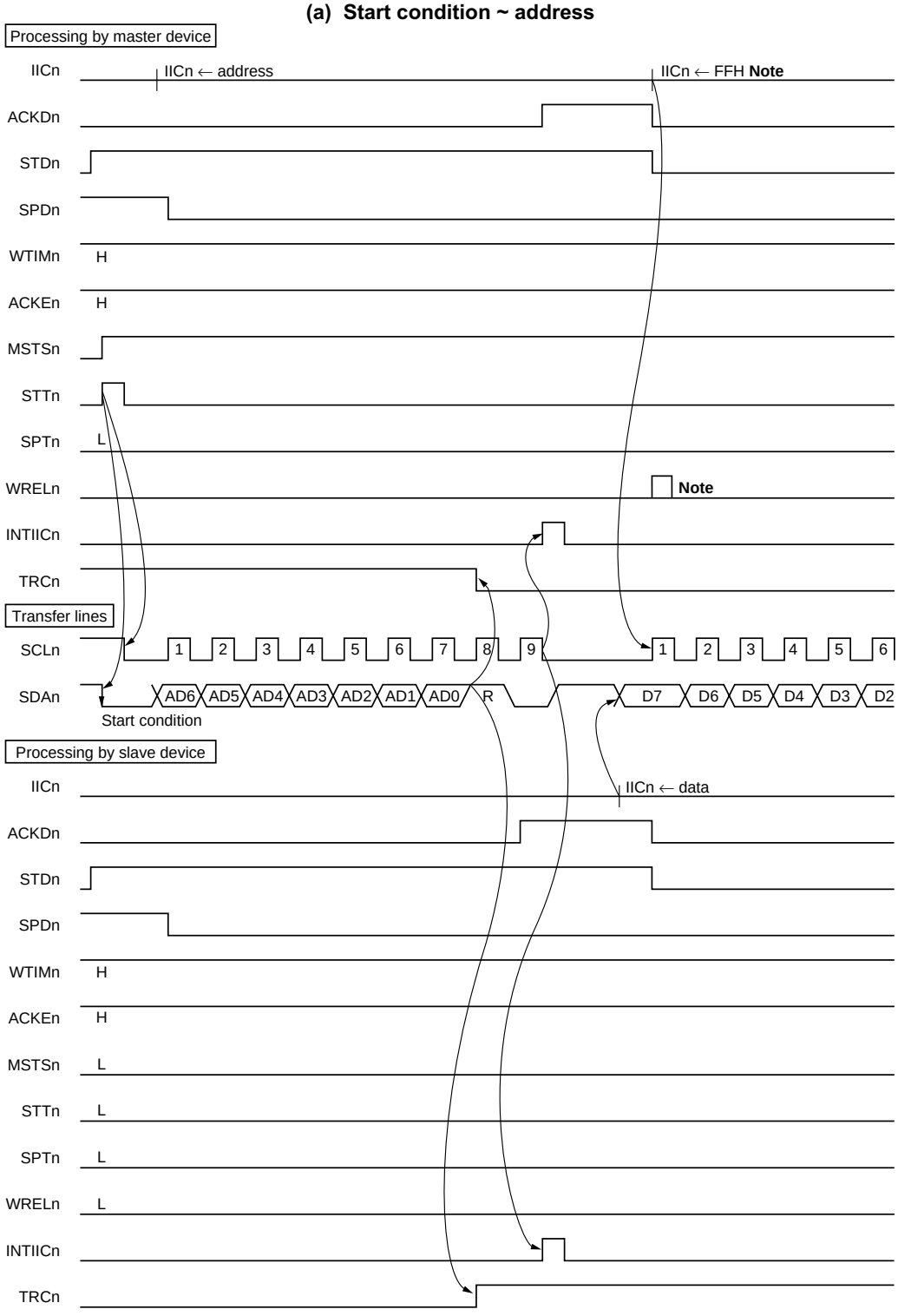
Figure 18-21. Example of Master to Slave Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (3/3)



Note To cancel slave wait, write FFH to IICn or set WRELn.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

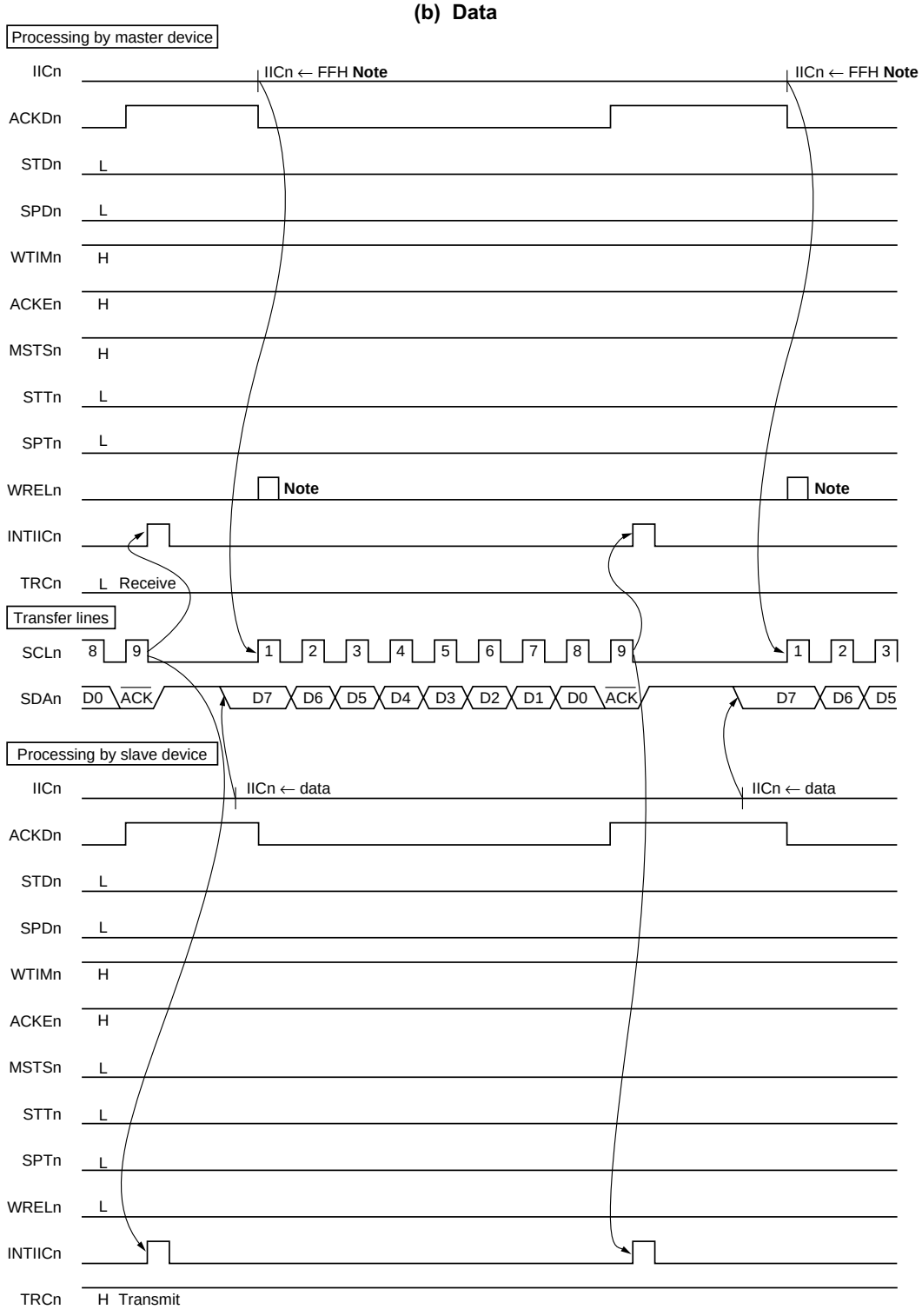
Figure 18-22. Example of Slave to Master Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (1/3)



Note To cancel master wait, write FFH to IICn or set WRELn.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

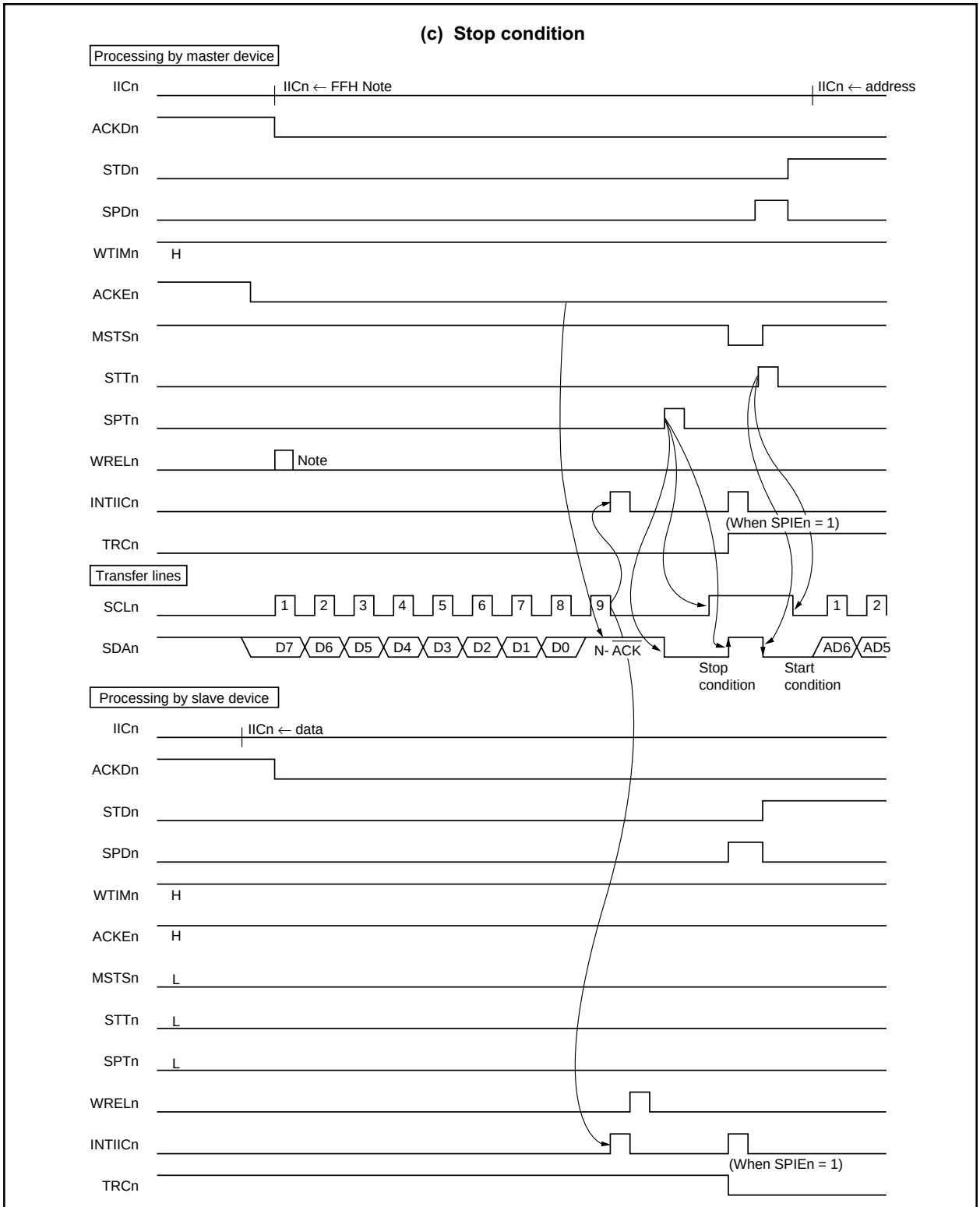
Figure 18-22. Example of Slave to Master Communication (When 9-Clock Wait Is Selected for Both Master and Slave) (2/3)



Note To cancel master wait, write FFH to IICn or set WRELn.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

Figure 18-22. Example of Slave to Master Communication
(When 9-Clock Wait Is Selected for Both Master and Slave) (3/3)



Note To cancel master wait, write FFH to IICn or set WRELn.

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

CHAPTER 19 INTERRUPT/EXCEPTION PROCESSING FUNCTION

19.1 Overview

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 are provided with a dedicated interrupt controller (INTC) for interrupt servicing and realize an interrupt function that can service interrupt requests from a total of 33 to 48 sources.

An interrupt is an event that occurs independently of program execution, and an exception is an event whose occurrence is dependent on program execution.

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 can process interrupt requests from the on-chip peripheral hardware and external sources. Moreover, exception processing can be started by the TRAP instruction (software exception) or by generation of an exception event (fetching of an illegal op code) (exception trap).

19.1.1 Features

Interrupt Source				V850ES/KF1	V850ES/KG1	V850ES/KJ1
Interrupt function	Non-maskable interrupt	External		1 channel (NMI pin)		
		Internal		2 channels (WDT1, WDT2)		
	Maskable interrupt	External		7 channels (all edge detection interrupts)		
		Internal	WDT1	1 channel	1 channel	1 channel
			TM0	4 channels	8 channels	12 channels
			TMH	2 channels	2 channels	2 channels
			TM5	2 channels	2 channels	2 channels
			WT	2 channels	2 channels	2 channels
			BRG	1 channel	1 channel	1 channel
			UART	6 channels	6 channels	9 channels
			CSI0	2 channels	2 channels	3 channels
			CSIA	1 channel	2 channels	2 channels
			IIC	1 channel	1 channel	2 channels
			KR	1 channel	1 channel	1 channel
			AD	1 channel	1 channel	1 channel
			Total	24 channels	29 channels	38 channels
Exception function	Software exception			16 channels (TRAP00H to TRAP0FH)		
				16 channels (TRAP10H to TRAP1FH)		
	Exception trap			2 channels (ILGOP/DBG0)		

Tables 19-1 to 19-3 list the interrupt/exception sources.

Table 19-1. Interrupt Source List (V850ES/KF1) (1/2)

Type	Classification	Default Priority	Name	Trigger	Interrupt Source	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Reset	Interrupt	–	RESET	$\overline{\text{RESET}}$ pin input	Pin	0000H	00000000H	Undefined	–
				Internal reset input from WDT1, WDT2	WDT1, WDT2				
Non-maskable	Interrupt	–	NMI	NMI pin valid edge input	Pin	0010H	00000010H	**Note 1**	–
		–	INTWDT1	WDT1 overflow (when non-maskable interrupt selected)	WDT1	0020H	00000020H	**Note 1**	–
		–	INTWDT2	WDT2 overflow (when non-maskable interrupt selected)	WDT2	0030H	00000030H	nextPC	–
Software exception	Exception	–	TRAP0n Note 2	TRAP instruction	–	004nH Note 2	00000040H	nextPC	–
		–	TRAP1n Note 2	TRAP instruction	–	005nH Note 2	00000050H	nextPC	–
Exception trap	Exception	–	ILGOP/ DBG0	Illegal op code/DBTRAP instruction	–	0060H	00000060H	nextPC	–
Maskable	Interrupt	0	INTWDTM1	WDT1 overflow (when interval timer selected)	WDT1	0080H	00000080H	nextPC	WDT1IC
		1	INTP0	INTP0 pin valid edge input	Pin	0090H	00000090H	nextPC	PIC0
		2	INTP1	INTP1 pin valid edge input	Pin	00A0H	000000A0H	nextPC	PIC1
		3	INTP2	INTP2 pin valid edge input	Pin	00B0H	000000B0H	nextPC	PIC2
		4	INTP3	INTP3 pin valid edge input	Pin	00C0H	000000C0H	nextPC	PIC3
		5	INTP4	INTP4 pin valid edge input	Pin	00D0H	000000D0H	nextPC	PIC4
		6	INTP5	INTP5 pin valid edge input	Pin	00E0H	000000E0H	nextPC	PIC5
		7	INTP6	INTP6 pin valid edge input	Pin	00F0H	000000F0H	nextPC	PIC6
		8	INTTM000	TM00 and CR000 match	TM00	0100H	00000100H	nextPC	TM0IC00
		9	INTTM001	TM00 and CR001 match	TM00	0110H	00000110H	nextPC	TM0IC01
		10	INTTM010	TM01 and CR010 match	TM01	0120H	00000120H	nextPC	TM0IC10
		11	INTTM011	TM01 and CR011 match	TM01	0130H	00000130H	nextPC	TM0IC11
		12	INTTM50	TM50 and CR50 match	TM50	0140H	00000140H	nextPC	TM5IC0
		13	INTTM51	TM51 and CR51 match	TM51	0150H	00000150H	nextPC	TM5IC1
		14	INTCSI00	CSI00 transfer completion	CSI00	0160H	00000160H	nextPC	CSI0IC0
		15	INTCSI01	CSI01 transfer completion	CSI01	0170H	00000170H	nextPC	CSI0IC1
		16	INTSRE0	UART0 reception error occurrence	UART0	0180H	00000180H	nextPC	SREIC0
		17	INTSR0	UART0 reception completion	UART0	0190H	00000190H	nextPC	SRIC0

Notes 1. For restoration via the RETI instruction in the case of INTWDT1 and INTWDT2, refer to **19.10 Cautions**.

2. n = 0 to FH

Table 19-1. Interrupt Source List (V850ES/KF1) (2/2)

Type	Classification	Default Priority	Name	Trigger	Interrupt Source	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Maskable	Interrupt	18	INTST0	UART0 transmission completion	UART0	01A0H	000001AH	nextPC	STIC0
		19	INTSRE1	UART1 reception error occurrence	UART1	01B0H	000001B0H	nextPC	SREIC1
		20	INTSR1	UART1 reception completion	UART1	01C0H	000001C0H	nextPC	SRIC1
		21	INTST1	UART1 transmission completion	UART1	01D0H	000001D0H	nextPC	STIC1
		22	INTTMH0	TMH0 and CMP00/CMP01 match	TMH0	01E0H	000001E0H	nextPC	TMHIC0
		23	INTTMH1	TMH1 and CMP10/CMP11 match	TMH1	01F0H	000001F0H	nextPC	TMHIC1
		24	INTCSIA0	CSIA0 transfer completion	CSIA0	0200H	00000200H	nextPC	CSIAIC0
		25	INTIIC0[Note]	I^2C0 transfer completion	I^2C0	0210H	00000210H	nextPC	IICIC0
		26	INTAD	A/D conversion completion	A/D	0220H	00000220H	nextPC	ADIC
		27	INTKR	Key return interrupt	KR	0230H	00000230H	nextPC	KRIC
		28	INTWTI	Watch timer interval	WT	0240H	00000240H	nextPC	WTIIC
		29	INTWT	Watch timer reference time	WT	0250H	00000250H	nextPC	WTIC
		30	INTBRG	8-bit counter of prescaler 3 and PRSCM match	Prescaler 3	0260H	00000260H	nextPC	BRGIC

Note Only in the μPD703208Y, 703209Y, 703210Y, and 70F3210Y

Remarks 1. Default priority: The priority order when two or more maskable interrupt requests with the same priority level are generated at the same time. The highest priority is 0.

The priority of non-maskable interrupt request is as follows.

INTWDT2 > INTWDT1 > NMI

Restored PC: The value of the program counter (PC) saved to EIPC, FEPC, or DBPC when interrupt/exception processing is started. The restored PC when a non-maskable or maskable interrupt is acknowledged while either of the following instructions is being executed does not become nextPC (when an interrupt is acknowledged during the execution of an instruction, the execution of that instruction is stopped and is resumed following completion of interrupt servicing).

- Load instructions (SLD.B, SLD.BU, SLD.H, SLD.HU, SLD.W)
- Divide instructions (DIV, DIVH, DIVU, DIVHU)
- PREPARE, DISPOSE instructions (only when an interrupt occurs before stack pointer update)

nextPC: The PC value at which processing is started following interrupt/exception processing.

2. The execution address of the illegal op code when an illegal op code exception occurs is calculated with (Restored PC – 4).

Table 19-2. Interrupt Source List (V850ES/KG1) (1/2)

Type	Classification	Default Priority	Name	Trigger	Interrupt Source	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Reset	Interrupt	–	RESET	$\overline{\text{RESET}}$ pin input	Pin	0000H	00000000H	Undefined	–
				Internal reset input from WDT1, WDT2	WDT1, WDT2				
Non-maskable	Interrupt	–	NMI	NMI pin valid edge input	Pin	0010H	00000010H	nextPC	–
		–	INTWDT1	WDT1 overflow (when non-maskable interrupt selected)	WDT1	0020H	00000020H	**Note 1**	–
		–	INTWDT2	WDT2 overflow (when non-maskable interrupt selected)	WDT2	0030H	00000020H	**Note 1**	–
Software exception	Exception	–	TRAP0n[Note 2]	TRAP instruction	–	004nH[Note 2]	00000040H	nextPC	–
		–	TRAP1n[Note 2]	TRAP instruction	–	005nH[Note 2]	00000050H	nextPC	–
Exception trap	Exception	–	ILGOP/ DBG0	Illegal op code/DBTRAP instruction	–	0060H	00000060H	nextPC	–
Maskable	Interrupt	0	INTWDTM1	WDT1 overflow (when interval timer selected)	WDT1	0080H	00000080H	nextPC	WDT1IC
		1	INTP0	INTP0 pin valid edge input	Pin	0090H	00000090H	nextPC	PIC0
		2	INTP1	INTP1 pin valid edge input	Pin	00A0H	000000A0H	nextPC	PIC1
		3	INTP2	INTP2 pin valid edge input	Pin	00B0H	000000B0H	nextPC	PIC2
		4	INTP3	INTP3 pin valid edge input	Pin	00C0H	000000C0H	nextPC	PIC3
		5	INTP4	INTP4 pin valid edge input	Pin	00D0H	000000D0H	nextPC	PIC4
		6	INTP5	INTP5 pin valid edge input	Pin	00E0H	000000E0H	nextPC	PIC5
		7	INTP6	INTP6 pin valid edge input	Pin	00F0H	000000F0H	nextPC	PIC6
		8	INTTM000	TM00 and CR000 match	TM00	0100H	00000100H	nextPC	TM0IC00
		9	INTTM001	TM00 and CR001 match	TM00	0110H	00000110H	nextPC	TM0IC01
		10	INTTM010	TM01 and CR010 match	TM01	0120H	00000120H	nextPC	TM0IC10
		11	INTTM011	TM01 and CR011 match	TM01	0130H	00000130H	nextPC	TM0IC11
		12	INTTM50	TM50 and CR50 match	TM50	0140H	00000140H	nextPC	TM5IC0
		13	INTTM51	TM51 and CR51 match	TM51	0150H	00000150H	nextPC	TM5IC1
		14	INTCSI00	CSI00 transfer completion	CSI00	0160H	00000160H	nextPC	CSI0IC0
		15	INTCSI01	CSI01 transfer completion	CSI01	0170H	00000170H	nextPC	CSI0IC1
		16	INTSRE0	UART0 reception error occurrence	UART0	0180H	00000180H	nextPC	SREIC0
		17	INTSR0	UART0 reception completion	UART0	0190H	00000190H	nextPC	SRIC0

Notes 1. For restoration via the RETI instruction in the case of INTWDT1 and INTWDT2, refer to **19.10 Cautions**.

2. n = 0 to FH

Table 19-2. Interrupt Source List (V850ES/KG1) (2/2)

Type	Classification	Default Priority	Name	Trigger	Interrupt Source	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Maskable	Interrupt	18	INTST0	UART0 transmission completion	UART0	01A0H	000001AH	nextPC	STIC0
		19	INTSRE1	UART1 reception error occurrence	UART1	01B0H	000001B0H	nextPC	SREIC1
		20	INTSR1	UART1 reception completion	UART1	01C0H	000001C0H	nextPC	SRIC1
		21	INTST1	UART1 transmission completion	UART1	01D0H	000001D0H	nextPC	STIC1
		22	INTTMH0	TMH0 and CMP00/CMP01 match	TMH0	01E0H	000001E0H	nextPC	TMHIC0
		23	INTTMH1	TMH1 and CMP10/CMP11 match	TMH1	01F0H	000001F0H	nextPC	TMHIC1
		24	INTCSIA0	CSIA0 transfer completion	CSIA0	0200H	00000200H	nextPC	CSIAIC0
		25	INTIIC0[Note 1]	I^2C0 transfer completion	I^2C0	0210H	00000210H	nextPC	IICIC0
		26	INTAD	A/D conversion completion	A/D	0220H	00000220H	nextPC	ADIC
		27	INTKR	Key return interrupt	KR	0230H	00000230H	nextPC	KRIC
		28	INTWTI	Watch timer interval	WT	0240H	00000240H	nextPC	WTIIC
		29	INTWT	Watch timer reference time	WT	0250H	00000250H	nextPC	WTIC
		30	INTBRG	8-bit counter of prescaler 3 and PRSCM match	Prescaler 3	0260H	00000260H	nextPC	BRGIC
		31	INTTM020	TM02 and CR020 match	TM02	0270H	00000270H	nextPC	TM0IC20
		32	INTTM021	TM02 and CR021 match	TM02	0280H	00000280H	nextPC	TM0IC21
		33	INTTM030	TM03 and CR030 match	TM03	0290H	00000290H	nextPC	TM0IC30
		34	INTTM031	TM03 and CR031 match	TM03	02A0H	000002A0H	nextPC	TM0IC31
		35	INTCSIA1	CSIA1 transfer completion	CSIA1	02B0H	000002B0H	nextPC	CSIAIC1

Note Only for the μPD703212Y, 703213Y, 703214Y, and 70F3214Y

Remarks 1. Default priority: The priority order when two or more maskable interrupt requests with the same priority level are generated at the same time. The highest priority is 0.

The priority of non-maskable interrupt request is as follows.

INTWDT2 > INTWDT1 > NMI

Restored PC: The value of the program counter (PC) saved to EIPC, FEPC, or DBPC when interrupt/exception processing is started. The restored PC when a non-maskable or maskable interrupt is acknowledged while either of the following instructions is being executed does not become nextPC (when an interrupt is acknowledged during the execution of an instruction, the execution of that instruction is stopped and is resumed following completion of interrupt servicing).

- Load instructions (SLD.B, SLD.BU, SLD.H, SLD.HU, SLD.W)
- Divide instructions (DIV, DIVH, DIVU, DIVHU)
- PREPARE, DISPOSE instructions (only when an interrupt occurs before stack pointer update)

nextPC: The PC value at which processing is started following interrupt/exception processing.

2. The execution address of the illegal op code when an illegal op code exception occurs is calculated with (Restored PC – 4).

Table 19-3. Interrupt Source List (V850ES/KJ1) (1/2)

Type	Classification	Default Priority	Name	Trigger	Interrupt Source	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Reset	Interrupt	–	RESET	$\overline{\text{RESET}}$ pin input	Pin	0000H	00000000H	Undefined	–
				Internal reset input from WDT1, WDT2	WDT1 WDT2				
Non-maskable	Interrupt	–	NMI	NMI pin valid edge input	Pin	0010H	00000010H	nextPC	–
		–	INTWDT1	WDT1 overflow (when non-maskable interrupt selected)	WDT1	0020H	00000020H	**Note 1**	–
		–	INTWDT2	WDT2 overflow (when non-maskable interrupt selected)	WDT2	0030H	00000020H	**Note 1**	–
Software exception	Exception	–	TRAP0n[Note 2]	TRAP instruction	–	004nH[Note 2]	00000040H	nextPC	–
		–	TRAP1n[Note 2]	TRAP instruction	–	005nH[Note 2]	00000050H	nextPC	–
Exception trap	Exception	–	ILGOP/ DBG0	Illegal op code/DBTRAP instruction	–	0060H	00000060H	nextPC	–
Maskable	Interrupt	0	INTWDTM1	WDT1 overflow (when interval timer selected)	WDT1	0080H	00000080H	nextPC	WDT1IC
		1	INTP0	INTP0 pin valid edge input	Pin	0090H	00000090H	nextPC	PIC0
		2	INTP1	INTP1 pin valid edge input	Pin	00A0H	000000A0H	nextPC	PIC1
		3	INTP2	INTP2 pin valid edge input	Pin	00B0H	000000B0H	nextPC	PIC2
		4	INTP3	INTP3 pin valid edge input	Pin	00C0H	000000C0H	nextPC	PIC3
		5	INTP4	INTP4 pin valid edge input	Pin	00D0H	000000D0H	nextPC	PIC4
		6	INTP5	INTP5 pin valid edge input	Pin	00E0H	000000E0H	nextPC	PIC5
		7	INTP6	INTP6 pin valid edge input	Pin	00F0H	000000F0H	nextPC	PIC6
		8	INTTM000	TM00 and CR000 match	TM00	0100H	00000100H	nextPC	TM0IC00
		9	INTTM001	TM00 and CR001 match	TM00	0110H	00000110H	nextPC	TM0IC01
		10	INTTM010	TM01 and CR010 match	TM01	0120H	00000120H	nextPC	TM0IC10
		11	INTTM011	TM01 and CR011 match	TM01	0130H	00000130H	nextPC	TM0IC11
		12	INTTM50	TM50 and CR50 match	TM50	0140H	00000140H	nextPC	TM5IC0
		13	INTTM51	TM51 and CR51 match	TM51	0150H	00000150H	nextPC	TM5IC1
		14	INTCSI00	CSI00 transfer completion	CSI00	0160H	00000160H	nextPC	CSI0IC0
		15	INTCSI01	CSI01 transfer completion	CSI01	0170H	00000170H	nextPC	CSI0IC1
		16	INTSRE0	UART0 reception error occurrence	UART0	0180H	00000180H	nextPC	SREIC0
		17	INTSR0	UART0 reception completion	UART0	0190H	00000190H	nextPC	SRIC0
		18	INTST0	UART0 transmission completion	UART0	01A0H	000001AH	nextPC	STIC0
		19	INTSRE1	UART1 reception error occurrence	UART1	01B0H	000001B0H	nextPC	SREIC1
		20	INTSR1	UART1 reception completion	UART1	01C0H	000001C0H	nextPC	SRIC1
		21	INTST1	UART1 transmission completion	UART1	01D0H	000001D0H	nextPC	STIC1

Notes 1. For restoration via the RETI instruction in the case of INTWDT1 and INTWDT2, refer to **19.10 Cautions**.

2. n = 0 to FH

Table 19-3. Interrupt Source List (V850ES/KJ1) (2/2)

Type	Classification	Default Priority	Name	Trigger	Interrupt Source	Exception Code	Handler Address	Restored PC	Interrupt Control Register
Maskable	Interrupt	22	INTTMH0	TMH0 and CMP00/CMP01 match	TMH0	01E0H	000001E0H	nextPC	TMHIC0
		23	INTTMH1	TMH1 and CMP10/CMP11 match	TMH1	01F0H	000001F0H	nextPC	TMHIC1
		24	INTCSIA0	CSIA0 transfer completion	CSIA0	0200H	00000200H	nextPC	CSIAIC0
		25	INTIIC0[Note]	I^2C0 transfer completion	I^2C0	0210H	00000210H	nextPC	IICIC0
		26	INTAD	A/D conversion completion	A/D	0220H	00000220H	nextPC	ADIC
		27	INTKR	Key return interrupt	KR	0230H	00000230H	nextPC	KRIC
		28	INTWTI	Watch timer interval	WT	0240H	00000240H	nextPC	WTIIC
		29	INTWT	Watch timer reference time	WT	0250H	00000250H	nextPC	WTIC
		30	INTBRG	8-bit counter of prescaler 3 and PRSCM match	Prescaler 3	0260H	00000260H	nextPC	BRGIC
		31	INTTM020	TM02 and CR020 match	TM02	0270H	00000270H	nextPC	TM0IC20
		32	INTTM021	TM02 and CR021 match	TM02	0280H	00000280H	nextPC	TM0IC21
		33	INTTM030	TM03 and CR030 match	TM03	0290H	00000290H	nextPC	TM0IC30
		34	INTTM031	TM03 and CR031 match	TM03	02A0H	000002A0H	nextPC	TM0IC31
		35	INTCSIA1	CSIA1 transfer completion	CSIA1	02B0H	000002B0H	nextPC	CSIAIC1
		36	INTTM040	TM04 and CR040 match	TM04	02C0H	000002C0H	nextPC	TM0IC40
		37	INTTM041	TM04 and CR041 match	TM04	02D0H	000002D0H	nextPC	TM0IC41
		38	INTTM050	TM05 and CR050 match	TM05	02E0H	000002E0H	nextPC	TM0IC50
		39	INTTM051	TM05 and CR051 match	TM05	02F0H	000002F0H	nextPC	TM0IC51
		40	INTCSI02	CSI02 transfer completion	CSI02	0300H	00000300H	nextPC	CSI0IC2
		41	INTSRE2	UART2 reception error occurrence	UART2	0310H	00000310H	nextPC	SREIC2
		42	INTSR2	UART2 reception completion	UART2	0320H	00000320H	nextPC	SRIC2
		43	INTST2	UART2 transmission completion	UART2	0330H	00000330H	nextPC	STIC2
		44	INTIIC1[Note]	I^2C1 transfer completion	I^2C1	0340H	00000340H	nextPC	IICIC1

Note Only for the μPD703216Y, 703217Y, and 70F3217Y

Remarks 1. Default priority: The priority order when two or more maskable interrupt requests with the same priority level are generated at the same time. The highest priority is 0.

The priority of non-maskable interrupt request is as follows.

INTWDT2 > INTWDT1 > NMI

Restored PC: The value of the program counter (PC) saved to EIPC, FEPC, or DBPC when interrupt/exception processing is started. The restored PC when a non-maskable or maskable interrupt is acknowledged while either of the following instructions is being executed does not become nextPC (when an interrupt is acknowledged during the execution of an instruction, the execution of that instruction is stopped and is resumed following completion of interrupt servicing).

- Load instructions (SLD.B, SLD.BU, SLD.H, SLD.HU, SLD.W)
- Divide instructions (DIV, DIVH, DIVU, DIVHU)
- PREPARE, DISPOSE instructions (only when an interrupt occurs before stack pointer update)

nextPC: The PC value at which processing is started following interrupt/exception processing.

2. The execution address of the illegal op code when an illegal op code exception occurs is calculated with (Restored PC – 4).

19.2 Non-Maskable Interrupts

Non-maskable interrupt requests are acknowledged unconditionally, even when interrupts are disabled (DI state). Non-maskable interrupts (NMI) are not subject to priority control and take precedence over all other interrupt requests.

The following three types of non-maskable interrupt requests are available in the V850ES/KF1, V850ES/KG1, and V850ES/KJ1.

- NMI pin input (NMI)
- Non-maskable interrupt request due to overflow of watchdog timer 1 (INTWDT1)
- Non-maskable interrupt request due to overflow of watchdog timer 2 (INTWDT2)

There are four choices for the valid edge of an NMI pin, namely: rising edge, falling edge, both edges, and no edge detection.

The non-maskable interrupt due to overflow of watchdog timer 1 (INTWDT1) functions by setting the WDTM14 and WDTM13 bits of watchdog timer mode register 1 (WDTM1) to 10.

The non-maskable interrupt due to overflow of watchdog timer 2 (INTWDT2) functions by setting the WDM21 and WDM20 bits of watchdog timer mode register 2 (WDTM2) to 01.

When two or more non-maskable interrupts occur simultaneously, they are processed in a sequence determined by the following priority order (the interrupt requests with low priority level are ignored).

INTWDT2 > INTWDT1 > NMI

If during NMI processing, an NMI, INTWDT1, or INTWDT2 request newly occurs, processing is performed as follows.

(1) If an NMI request newly occurs during NMI processing

The new NMI request is held pending regardless of the value of the NP bit of the program status word (PSW) of the CPU. The NMI request held pending is acknowledged upon completion of processing of the NMI currently being executed (following RETI instruction execution).

(2) If an INTWDT1 request newly occurs during NMI processing

If the NP bit of PSW remains set (to 1) during NMI processing, the new INTWDT1 request is held pending. The INTWDT1 request held pending is acknowledged upon completion of processing of the NMI currently being executed (following RETI instruction execution).

If the NP bit of PSW is cleared (to 0) during NMI processing, a newly generated INTWDT1 request is executed (NMI processing is interrupted).

(3) If an INTWDT2 request newly occurs during NMI processing

A newly generated INTWDT2 request is executed regardless of the value of the NP bit of PSW (NMI processing is interrupted).

Caution For non-maskable interrupt servicing from non-maskable interrupt requests (INTWDT1, INTWDT2), refer to 19.10 Cautions.

Figure 19-1. Acknowledging Non-Maskable Interrupt Requests (1/2)

(a) If two or more NMI requests are simultaneously generated

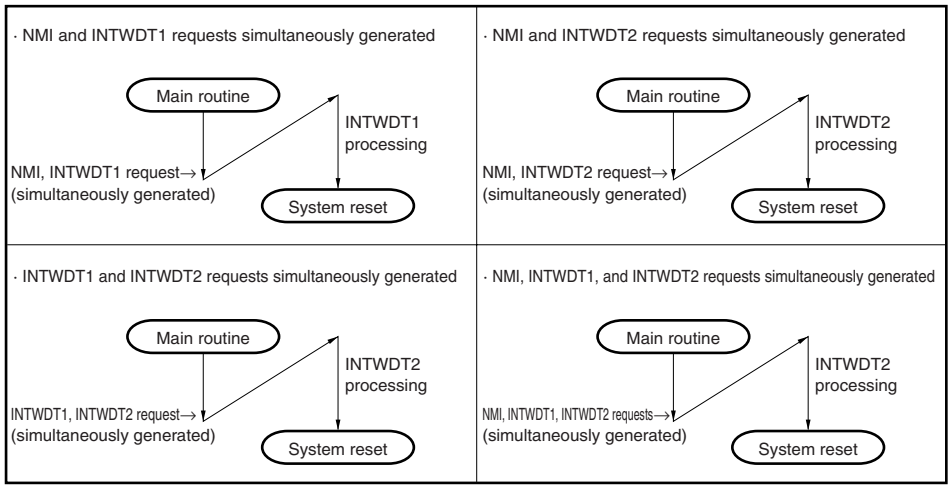
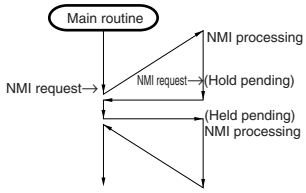
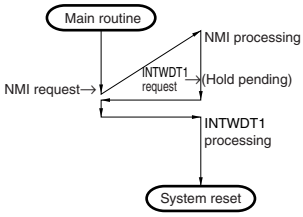
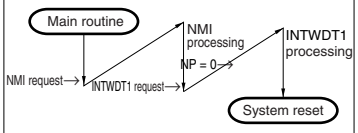
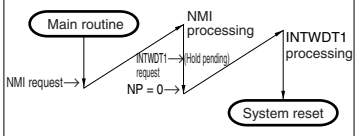
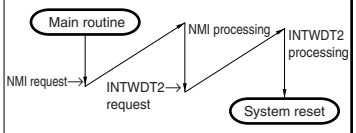
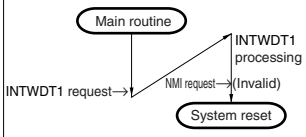
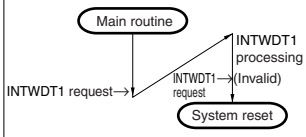
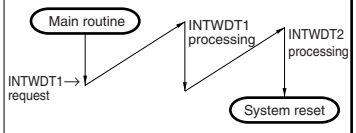
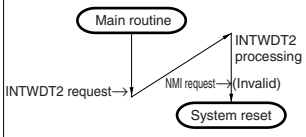
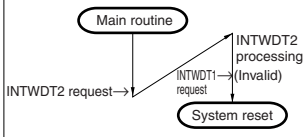
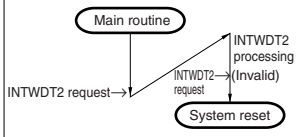


Figure 19-1. Acknowledging Non-Maskable Interrupt Requests (2/2)

(b) If a new NMI request is generated during a non-maskable interrupt servicing

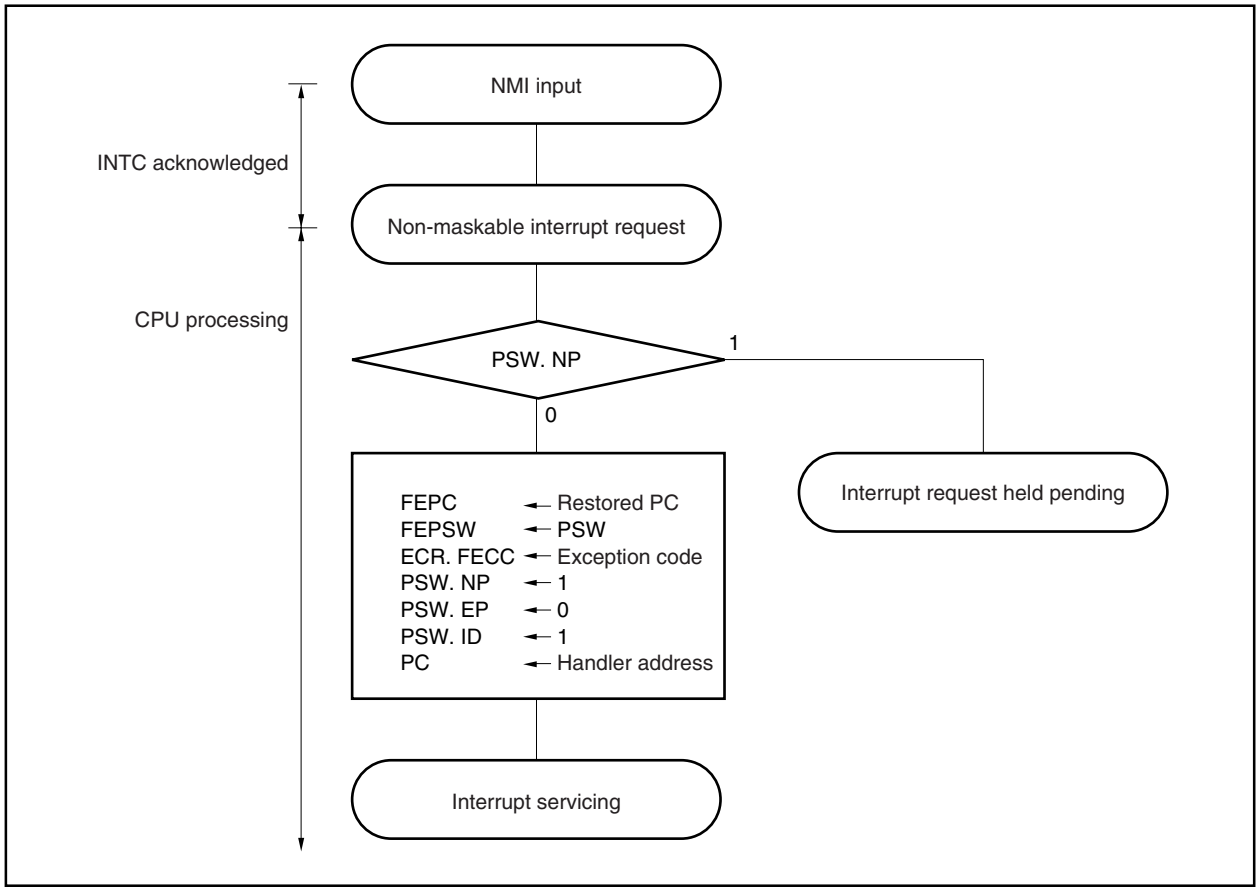
Non-maskable interrupt currently being serviced	Non-maskable interrupt request newly generated during non-maskable interrupt servicing		
	NMI	INTWDT1	INTWDT2
NMI	· Generation of NMI request during NMI processing 	· Generation of INTWDT1 request during NMI processing (NP = 1 state prior to INTWDT1 request is maintained)  · Generation of INTWDT1 request during NMI processing (Set NP = 0 before INTWDT1 request)  · Generation of INTWDT1 request during NMI processing (Set NP = 0 after INTWDT1 request) 	· Generation of INTWDT2 request during NMI processing 
INTWDT1	· Generation of NMI request during INTWDT1 processing 	· Generation of INTWDT1 request during INTWDT1 processing 	· Generation of INTWDT2 request during INTWDT1 processing 
INTWDT2	· Generation of NMI request during INTWDT2 processing 	· Generation of INTWDT1 request during INTWDT2 processing 	· Generation of INTWDT2 request during INTWDT2 processing 

19.2.1 Operation

Upon generation of a non-maskable interrupt request, the CPU performs the following processing and transfers control to a handler routine.

<1> Saves the restored PC to FEPC.
<2> Saves the current PSW to FEPSW.
<3> Writes the exception code 0010H to the higher halfword (FECC) of ECR.
<4> Sets the NP and ID bits of the PSW and clears the EP bit.
<5> Loads the handler address of the non-maskable interrupt to the PC and transfers control.

Figure 19-2. Non-Maskable Interrupt Servicing



19.2.2 Restore

Execution is restored from non-maskable interrupt servicing by the RETI instruction.

(1) In case of NMI

Restore from NMI processing is done with the RETI instruction.

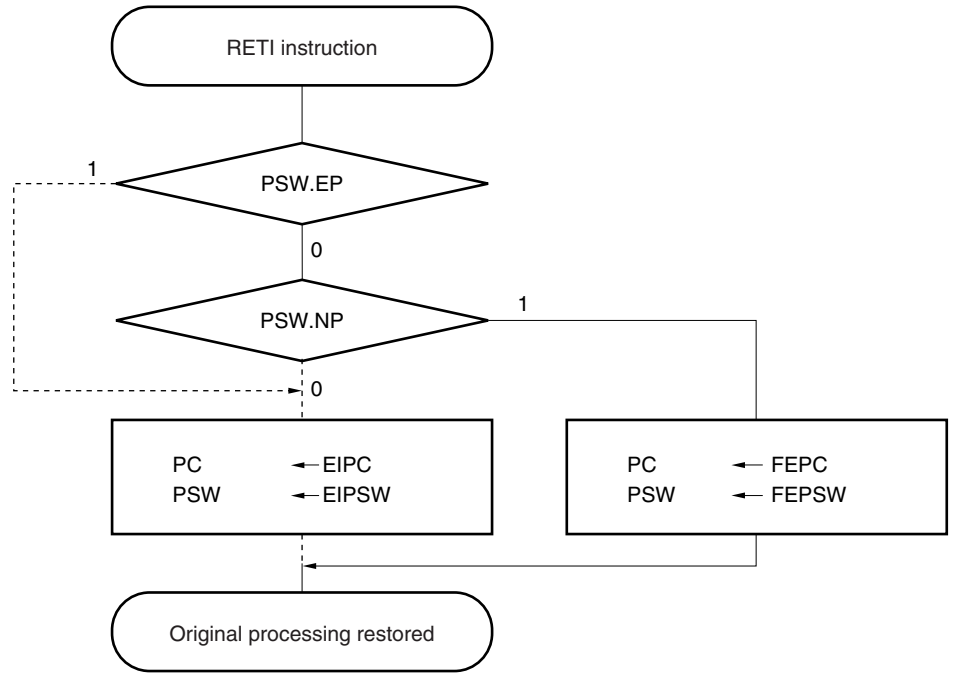
When the RETI instruction is executed, the CPU performs the following processing and transfers control to the address of the restored PC.

(i) Loads the values of the restored PC and PSW from FEPC and FEPSW, respectively, because the EP bit and NP bit of the PSW are 0 and 1, respectively.

(ii) Transfers control back to the loaded address of the restored PC and PSW.

Figure 19-3 shows the processing flow of the RETI instruction.

Figure 19-3. RETI Instruction Processing



Caution When the PSW.EP bit and PSW.NP bit are changed by the LDSR instruction during non-maskable interrupt servicing, in order to restore the PC and PSW correctly during restoring by the RETI instruction, it is necessary to set PSW.EP back to 0 and PSW.NP back to 1 using the LDSR instruction immediately before the RETI instruction.

Remark The solid line shows the CPU processing flow.

(2) In case of INTWDT1, INTWDT2

Refer to **19.10 Cautions**.

19.2.3 NP flag

The NP flag is a status flag that indicates that non-maskable interrupt servicing is in progress. This flag is set when a non-maskable interrupt request has been acknowledged, and masks all non-maskable requests to prevent multiple interrupts.

After reset : 00000020H

	31	8	7	6	5	4	3	2	1	0
PSW	0		NP	EP	ID	SAT	CY	OV	S	Z

NP	NMI servicing status
0	No non-maskable interrupt servicing
1	Non-maskable interrupt serving in progress

19.3 Maskable Interrupts

Maskable interrupt requests can be masked by interrupt control registers. The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 have 33 to 48 maskable interrupt sources (refer to **19.1.1 Features**).

If two or more maskable interrupt requests are generated at the same time, they are acknowledged according to the default priority. In addition to the default priority, eight levels of interrupt priorities can be specified by using the interrupt control registers, allowing programmable priority control.

When an interrupt request has been acknowledged, the interrupt disabled (DI) status is set and the acknowledgment of other maskable interrupts is disabled.

When the EI instruction is executed in an interrupt servicing routine, the interrupt enabled (EI) status is set, which enables acknowledgment of interrupts having a priority higher than that of the interrupt request currently in progress. Note that only interrupts with a higher priority have this capability; interrupts with the same priority level cannot be nested.

To use multiple interrupts, it is necessary to save EIPC and EIPSW to memory or a register before executing the EI instruction, and restore EIPC and EIPSW to the original values by executing the DI instruction before the RETI instruction.

When the WDTM14 bit of watchdog timer mode register 1 (WDTM1) is set to 0, the watchdog timer overflow interrupt functions as a maskable interrupt (INTWDTM1).

19.3.1 Operation

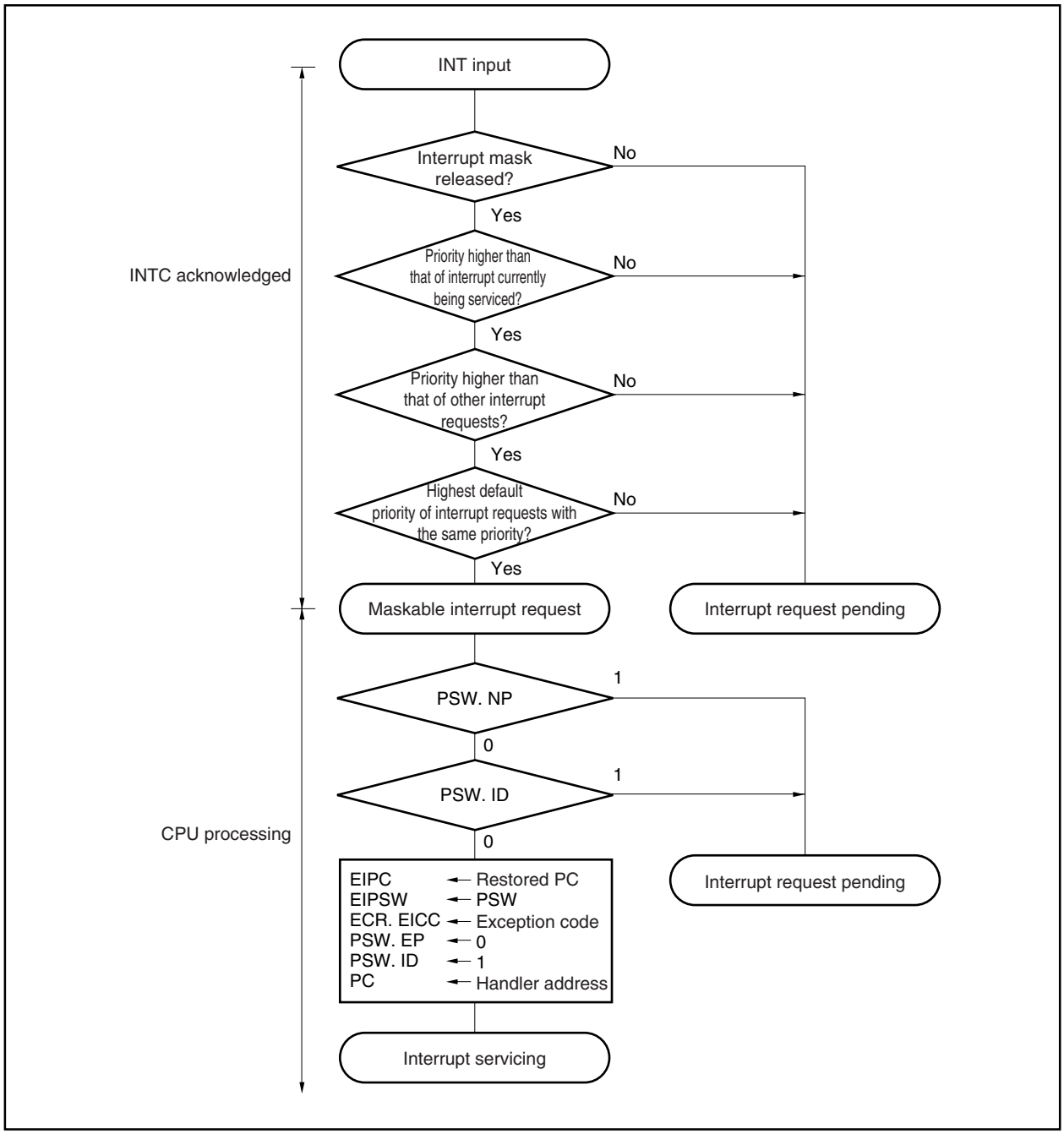
If a maskable interrupt request is generated, the CPU performs the following processing and transfers control to a handler routine.

<1> Saves the restored PC to EIPC.
<2> Saves the current PSW to EIPSW.
<3> Writes an exception code to the lower halfword of ECR (EICC).
<4> Sets the ID bit of the PSW and clears the EP bit.
<5> Loads the corresponding handler address to the PC and transfers control.

The maskable interrupt request masked by INTC and the maskable interrupt request that occurs while another interrupt is being serviced (when PSW.NP = 1 or PSW.ID = 1) are held pending internally. When the interrupts are unmasked, or when PSW.NP = 0 and PSW.ID = 0 by using the RETI and LDSR instructions, a new maskable interrupt servicing is started in accordance with the priority of the pending maskable interrupt request.

Figure 19-4 shows the servicing flow for maskable interrupts.

Figure 19-4. Maskable Interrupt Servicing



19.3.2 Restore

Execution is restored from maskable interrupt servicing by the RETI instruction.

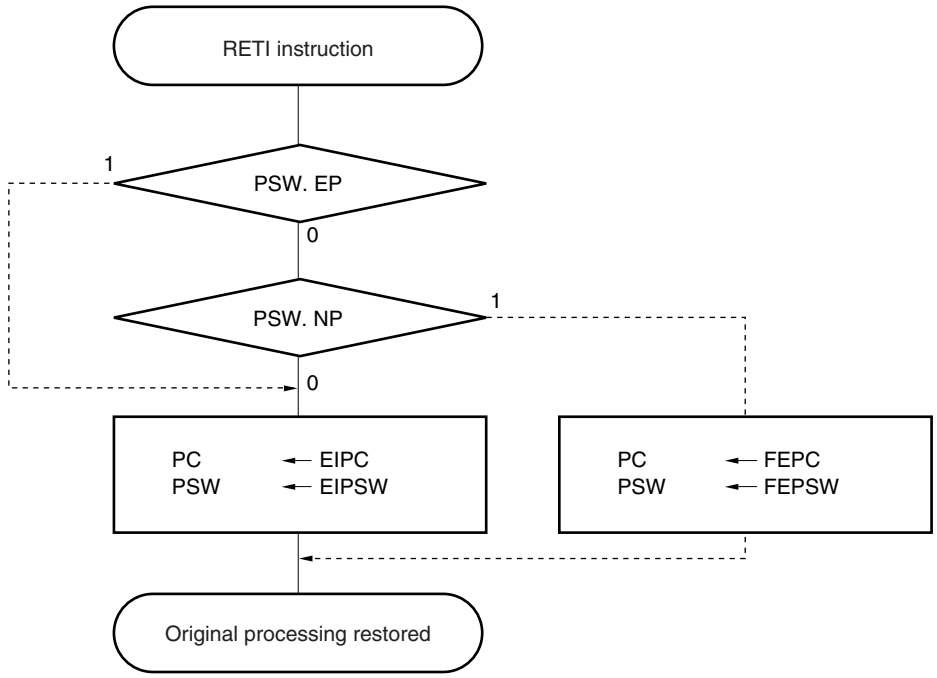
Operation of RETI instruction

When the RETI instruction is executed, the CPU performs the following processing and transfers control to the address of the restored PC.

(1) Loads the values of the restored PC and PSW from EIPC and EIPSW because the EP bit and NP bit of the PSW are both 0.
(2) Transfers control to the loaded address of the restored PC and PSW.

Figure 19-5 shows the processing flow of the RETI instruction.

Figure 19-5. RETI Instruction Processing



Caution When the PSW.EP bit and PSW.NP bit are changed by the LDSR instruction during maskable interrupt servicing, in order to restore the PC and PSW correctly during restoring by the RETI instruction, it is necessary to set PSW.EP back to 0 and PSW.NP back to 0 using the LDSR instruction immediately before the RETI instruction.

Remark The solid line shows the CPU processing flow.

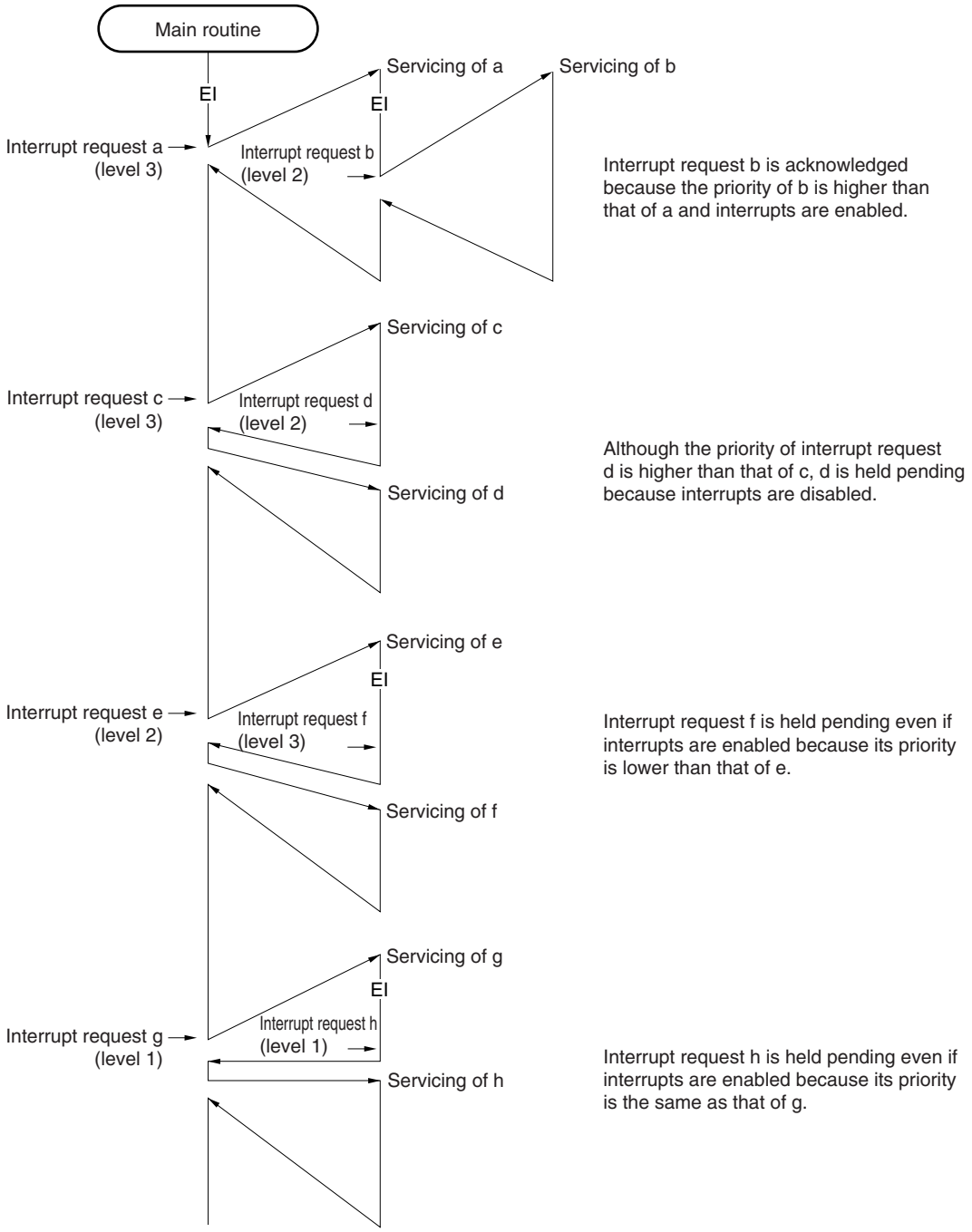
19.3.3 Priorities of maskable interrupts

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 provide a multiple interrupt servicing in which an interrupt can be acknowledged while another interrupt is being serviced. Multiple interrupts can be controlled by priority levels.

There are two types of priority level control: control based on the default priority levels, and control based on the programmable priority levels specified by the interrupt priority level specification bit (xxPRn). When two or more interrupts having the same priority level specified by xxPRn are generated at the same time, interrupts are serviced in order depending on the priority level allocated to each interrupt request (default priority level) beforehand. For more information, refer to **Tables 19-1**, **19-2**, and **19-3 Interrupt Sources**. Programmable priority control divides interrupt requests into eight levels by setting the priority level specification flag.

Note that when an interrupt request is acknowledged, the ID flag of the PSW is automatically set (1). Therefore, when multiple interrupts are to be used, clear (0) the ID flag beforehand (for example, by placing the EI instruction into the interrupt service program) to enable interrupts.

Figure 19-6. Example of Interrupt Nesting (1/2)

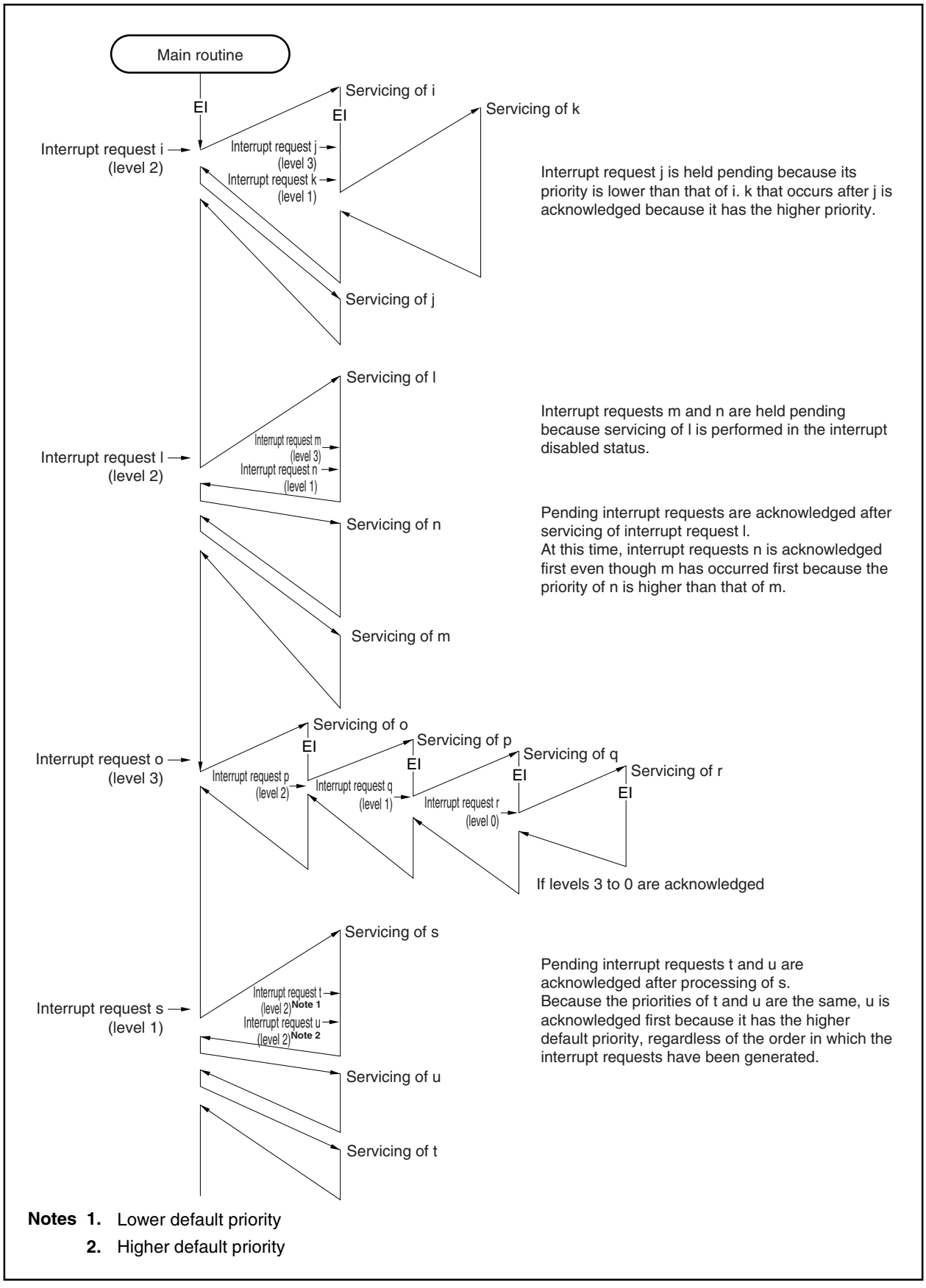


Caution The values of EIPC and EIPSW must be saved before executing multiple interrupts.

Remarks 1. a to u in the figure are the names of interrupt requests shown for the sake of explanation.

2. The default priority in the figure indicates the relative priority between two interrupt requests.

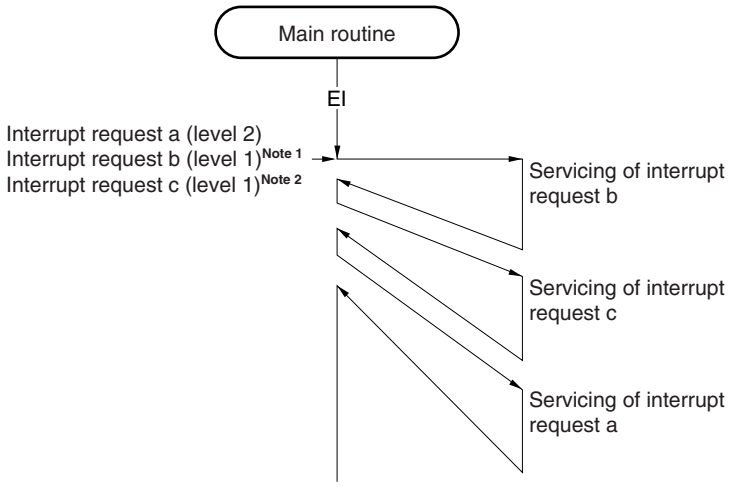
Figure 19-6. Example of Interrupt Nesting (2/2)



Notes 1. Lower default priority

2. Higher default priority

Figure 19-7. Example of Servicing Simultaneously Generated Interrupt Requests



·Interrupt requests b and c are acknowledged first according to their priorities.
·Because the priorities of b and c are the same, b is acknowledged first because it has the higher default priority.

Notes 1. Higher default priority
2. Lower default priority

19.3.4 Interrupt control register (xxICn)

An interrupt control register is assigned to each maskable interrupt and sets the control conditions for each maskable interrupt request.

The interrupt control registers can be read/written in 8-bit or 1-bit units.

Caution Be sure to read the xxIFn bit of the xxICn register while interrupts are disabled (DI). If the xxIFn bit is read while interrupts are enabled (EI), an incorrect value may be read if there is a conflict between acknowledgment of the interrupt and reading of the bit.

After reset: 47H R/W Address: FFFFF110H to FFFFF168H

	<7>	<6>	5	4	3	2	1	0
xxICn	xxIFn	xxMKn	0	0	0	xxPRn2	xxPRn1	xxPRn0

xxIFn	Interrupt request flag[Note]
0	Interrupt request not generated
1	Interrupt request generated

xxMKn	Interrupt mask flag
0	Enables interrupt servicing
1	Disables interrupt servicing (pending)

xxPRn2	xxPRn1	xxPRn0	Interrupt priority specification bit
0	0	0	Specifies level 0 (highest)
0	0	1	Specifies level 1
0	1	0	Specifies level 2
0	1	1	Specifies level 3
1	0	0	Specifies level 4
1	0	1	Specifies level 5
1	1	0	Specifies level 6
1	1	1	Specifies level 7 (lowest)

Note Automatically reset by hardware when interrupt request is acknowledged.

Remark xx: Identifying name of each peripheral unit (CSI0, TM5, TM0, P, WDT, BRG, WT, WTI, KR, AD, IIC, CSIA, TMH, ST, SR, SRE)
n: Peripheral unit number (See **Tables 19-4** to **19-6**.)

Following tables list the addresses and bits of the interrupt control registers.

Table 19-4. Interrupt Control Registers (xxICn) (V850ES/KF1)

Address	Register	Bits							
		<7>	<6>	5	4	3	2	1	0
FFFFF110H	WDT1IC	WDT1IF	WDT1MK	0	0	0	WDT1PR2	WDT1PR1	WDT1PR0
FFFFF112H	PIC0	PIF0	PMK0	0	0	0	PPR02	PPR01	PPR00
FFFFF114H	PIC1	PIF1	PMK1	0	0	0	PPR12	PPR11	PPR10
FFFFF116H	PIC2	PIF2	PMK2	0	0	0	PPR22	PPR21	PPR20
FFFFF118H	PIC3	PIF3	PMK3	0	0	0	PPR32	PPR31	PPR30
FFFFF11AH	PIC4	PIF4	PMK4	0	0	0	PPR42	PPR41	PPR40
FFFFF11CH	PIC5	PIF5	PMK5	0	0	0	PPR52	PPR51	PPR50
FFFFF11EH	PIC6	PIF6	PMK6	0	0	0	PPR62	PPR61	PPR60
FFFFF120H	TM0IC00	TM0IF00	TM0MK00	0	0	0	TM0PR002	TM0PR001	TM0PR000
FFFFF122H	TM0IC01	TM0IF01	TM0MK01	0	0	0	TM0PR012	TM0PR011	TM0PR010
FFFFF124H	TM0IC10	TM0IF10	TM0MK10	0	0	0	TM0PR102	TM0PR101	TM0PR100
FFFFF126H	TM0IC11	TM0IF11	TM0MK11	0	0	0	TM0PR112	TM0PR111	TM0PR110
FFFFF128H	TM5IC0	TM5IF0	TM5MK0	0	0	0	TM5PR02	TM5PR01	TM5PR00
FFFFF12AH	TM5IC1	TM5IF1	TM5MK1	0	0	0	TM5PR12	TM5PR11	TM5PR10
FFFFF12CH	CSI0IC0	CSI0IF0	CSI0MK0	0	0	0	CSI0PR02	CSI0PR01	CSI0PR00
FFFFF12EH	CSI0IC1	CSI0IF1	CSI0MK1	0	0	0	CSI0PR12	CSI0PR11	CSI0PR10
FFFFF130H	SREIC0	SREIF0	SREMK0	0	0	0	SREPR02	SREPR01	SREPR00
FFFFF132H	SRIC0	SRIF0	SRMK0	0	0	0	SRPR02	SRPR01	SRPR00
FFFFF134H	STIC0	STIF0	STMK0	0	0	0	STPR02	STPR01	STPR00
FFFFF136H	SREIC1	SREIF1	SREMK1	0	0	0	SREPR12	SREPR11	SREPR10
FFFFF138H	SRIC1	SRIF1	SRMK1	0	0	0	SRPR12	SRPR11	SRPR10
FFFFF13AH	STIC1	STIF1	STMK1	0	0	0	STPR12	STPR11	STPR10
FFFFF13CH	TMHIC0	TMHIF0	TMHMK0	0	0	0	TMHPR02	TMHPR01	TMHPR00
FFFFF13EH	TMHIC1	TMHIF1	TMHMK1	0	0	0	TMHPR12	TMHPR11	TMHPR10
FFFFF140H	CSIAIC0	CSIAIF0	CSIAMK0	0	0	0	CSIAPR02	CSIAPR01	CSIAPR00
FFFFF142H	IICIC0[Note]	IICIF0	IICMK0	0	0	0	IICPR02	IICPR01	IICPR00
FFFFF144H	ADIC	ADIF	ADMK	0	0	0	ADPR2	ADPR1	ADPR0
FFFFF146H	KRIC	KRIF	KRMK	0	0	0	KRPR2	KRPR1	KRPR0
FFFFF148H	WTIIC	WTIIF	WTIMK	0	0	0	WTIPR2	WTIPR1	WTIPR0
FFFFF14AH	WTIC	WTIF	WTMK	0	0	0	WTPR2	WTPR1	WTPR0
FFFFF14CH	BRGIC	BRGIF	BRGMK	0	0	0	BRGPR2	BRGPR1	BRGPR0

Note Only for the μPD703208Y, 703209Y, 703210Y, and 70F3210Y

Table 19-5. Interrupt Control Registers (xxICn) (V850ES/KG1)

Address	Register	Bits							
		<7>	<6>	5	4	3	2	1	0
FFFFF110H	WDT1IC	WDT1IF	WDT1MK	0	0	0	WDT1PR2	WDT1PR1	WDT1PR0
FFFFF112H	PIC0	PIF0	PMK0	0	0	0	PPR02	PPR01	PPR00
FFFFF114H	PIC1	PIF1	PMK1	0	0	0	PPR12	PPR11	PPR10
FFFFF116H	PIC2	PIF2	PMK2	0	0	0	PPR22	PPR21	PPR20
FFFFF118H	PIC3	PIF3	PMK3	0	0	0	PPR32	PPR31	PPR30
FFFFF11AH	PIC4	PIF4	PMK4	0	0	0	PPR42	PPR41	PPR40
FFFFF11CH	PIC5	PIF5	PMK5	0	0	0	PPR52	PPR51	PPR50
FFFFF11EH	PIC6	PIF6	PMK6	0	0	0	PPR62	PPR61	PPR60
FFFFF120H	TM0IC00	TM0IF00	TM0MK00	0	0	0	TM0PR002	TM0PR001	TM0PR000
FFFFF122H	TM0IC01	TM0IF01	TM0MK01	0	0	0	TM0PR012	TM0PR011	TM0PR010
FFFFF124H	TM0IC10	TM0IF10	TM0MK10	0	0	0	TM0PR102	TM0PR101	TM0PR100
FFFFF126H	TM0IC11	TM0IF11	TM0MK11	0	0	0	TM0PR112	TM0PR111	TM0PR110
FFFFF128H	TM5IC0	TM5IF0	TM5MK0	0	0	0	TM5PR02	TM5PR01	TM5PR00
FFFFF12AH	TM5IC1	TM5IF1	TM5MK1	0	0	0	TM5PR12	TM5PR11	TM5PR10
FFFFF12CH	CSI0IC0	CSI0IF0	CSI0MK0	0	0	0	CSI0PR02	CSI0PR01	CSI0PR00
FFFFF12EH	CSI0IC1	CSI0IF1	CSI0MK1	0	0	0	CSI0PR12	CSI0PR11	CSI0PR10
FFFFF130H	SREIC0	SREIF0	SREMK0	0	0	0	SREPR02	SREPR01	SREPR00
FFFFF132H	SRIC0	SRIF0	SRMK0	0	0	0	SRPR02	SRPR01	SRPR00
FFFFF134H	STIC0	STIF0	STMK0	0	0	0	STPR02	STPR01	STPR00
FFFFF136H	SREIC1	SREIF1	SREMK1	0	0	0	SREPR12	SREPR11	SREPR10
FFFFF138H	SRIC1	SRIF1	SRMK1	0	0	0	SRPR12	SRPR11	SRPR10
FFFFF13AH	STIC1	STIF1	STMK1	0	0	0	STPR12	STPR11	STPR10
FFFFF13CH	TMHIC0	TMHIF0	TMHMK0	0	0	0	TMHPR02	TMHPR01	TMHPR00
FFFFF13EH	TMHIC1	TMHIF1	TMHMK1	0	0	0	TMHPR12	TMHPR11	TMHPR10
FFFFF140H	CSIAIC0	CSIAIF0	CSIAMK0	0	0	0	CSIAPR02	CSIAPR01	CSIAPR00
FFFFF142H	IICIC0[Note]	IICIF0	IICMK0	0	0	0	IICPR02	IICPR01	IICPR00
FFFFF144H	ADIC	ADIF	ADMK	0	0	0	ADPR2	ADPR1	ADPR0
FFFFF146H	KRIC	KRIF	KRMK	0	0	0	KRPR2	KRPR1	KRPR0
FFFFF148H	WTIIC	WTIIF	WTIMK	0	0	0	WTIPR2	WTIPR1	WTIPR0
FFFFF14AH	WTIC	WTF	WTMK	0	0	0	WTPR2	WTPR1	WTPR0
FFFFF14CH	BRGIC	BRGIF	BRGMK	0	0	0	BRGPR2	BRGPR1	BRGPR0
FFFFF14EH	TM0IC20	TM0IF20	TM0MK20	0	0	0	TM0PR202	TM0PR201	TM0PR200
FFFFF150H	TM0IC21	TM0IF21	TM0MK21	0	0	0	TM0PR212	TM0PR211	TM0PR210
FFFFF152H	TM0IC30	TM0IF30	TM0MK30	0	0	0	TM0PR302	TM0PR301	TM0PR300
FFFFF154H	TM0IC31	TM0IF31	TM0MK31	0	0	0	TM0PR312	TM0PR311	TM0PR310
FFFFF156H	CSIAIC1	CSIAIF1	CSIAMK1	0	0	0	CSIAPR12	CSIAPR11	CSIAPR10

Note Only for the μPD703212Y, 703213Y, 703214Y, and 70F3214Y

Table 19-6. Interrupt Control Registers (xxICn) (V850ES/KJ1) (1/2)

Address	Register	Bits							
		<7>	<6>	5	4	3	2	1	0
FFFFF110H	WDT1IC	WDT1IF	WDT1MK	0	0	0	WDT1PR2	WDT1PR1	WDT1PR0
FFFFF112H	PIC0	PIF0	PMK0	0	0	0	PPR02	PPR01	PPR00
FFFFF114H	PIC1	PIF1	PMK1	0	0	0	PPR12	PPR11	PPR10
FFFFF116H	PIC2	PIF2	PMK2	0	0	0	PPR22	PPR21	PPR20
FFFFF118H	PIC3	PIF3	PMK3	0	0	0	PPR32	PPR31	PPR30
FFFFF11AH	PIC4	PIF4	PMK4	0	0	0	PPR42	PPR41	PPR40
FFFFF11CH	PIC5	PIF5	PMK5	0	0	0	PPR52	PPR51	PPR50
FFFFF11EH	PIC6	PIF6	PMK6	0	0	0	PPR62	PPR61	PPR60
FFFFF120H	TM0IC00	TM0IF00	TM0MK00	0	0	0	TM0PR002	TM0PR001	TM0PR000
FFFFF122H	TM0IC01	TM0IF01	TM0MK01	0	0	0	TM0PR012	TM0PR011	TM0PR010
FFFFF124H	TM0IC10	TM0IF10	TM0MK10	0	0	0	TM0PR102	TM0PR101	TM0PR100
FFFFF126H	TM0IC11	TM0IF11	TM0MK11	0	0	0	TM0PR112	TM0PR111	TM0PR110
FFFFF128H	TM5IC0	TM5IF0	TM5MK0	0	0	0	TM5PR02	TM5PR01	TM5PR00
FFFFF12AH	TM5IC1	TM5IF1	TM5MK1	0	0	0	TM5PR12	TM5PR11	TM5PR10
FFFFF12CH	CSI0IC0	CSI0IF0	CSI0MK0	0	0	0	CSI0PR02	CSI0PR01	CSI0PR00
FFFFF12EH	CSI0IC1	CSI0IF1	CSI0MK1	0	0	0	CSI0PR12	CSI0PR11	CSI0PR10
FFFFF130H	SREIC0	SREIF0	SREMK0	0	0	0	SREPR02	SREPR01	SREPR00
FFFFF132H	SRIC0	SRIF0	SRMK0	0	0	0	SRPR02	SRPR01	SRPR00
FFFFF134H	STIC0	STIF0	STMK0	0	0	0	STPR02	STPR01	STPR00
FFFFF136H	SREIC1	SREIF1	SREMK1	0	0	0	SREPR12	SREPR11	SREPR10
FFFFF138H	SRIC1	SRIF1	SRMK1	0	0	0	SRPR12	SRPR11	SRPR10
FFFFF13AH	STIC1	STIF1	STMK1	0	0	0	STPR12	STPR11	STPR10
FFFFF13CH	TMHIC0	TMHIF0	TMHMK0	0	0	0	TMHPR02	TMHPR01	TMHPR00
FFFFF13EH	TMHIC1	TMHIF1	TMHMK1	0	0	0	TMHPR12	TMHPR11	TMHPR10
FFFFF140H	CSIAIC0	CSIAIF0	CSIAMK0	0	0	0	CSIAPR02	CSIAPR01	CSIAPR00
FFFFF142H	IICIC0[Note]	IICIF0	IICMK0	0	0	0	IICPR02	IICPR01	IICPR00
FFFFF144H	ADIC	ADIF	ADMK	0	0	0	ADPR2	ADPR1	ADPR0
FFFFF146H	KRIC	KRIF	KRMK	0	0	0	KRPR2	KRPR1	KRPR0
FFFFF148H	WTIIC	WTIIF	WTIMK	0	0	0	WTIPR2	WTIPR1	WTIPR0
FFFFF14AH	WTIC	WTIF	WTMK	0	0	0	WTPR2	WTPR1	WTPR0
FFFFF14CH	BRGIC	BRGIF	BRGMK	0	0	0	BRGPR2	BRGPR1	BRGPR0
FFFFF14EH	TM0IC20	TM0IF20	TM0MK20	0	0	0	TM0PR202	TM0PR201	TM0PR200
FFFFF150H	TM0IC21	TM0IF21	TM0MK21	0	0	0	TM0PR212	TM0PR211	TM0PR210
FFFFF152H	TM0IC30	TM0IF30	TM0MK30	0	0	0	TM0PR302	TM0PR301	TM0PR300
FFFFF154H	TM0IC31	TM0IF31	TM0MK31	0	0	0	TM0PR312	TM0PR311	TM0PR310
FFFFF156H	CSIAIC1	CSIAIF1	CSIAMK1	0	0	0	CSIAPR12	CSIAPR11	CSIAPR10
FFFFF158H	TM0IC40	TM0IF40	TM0MK40	0	0	0	TM0PR402	TM0PR401	TM0PR400
FFFFF15AH	TM0IC41	TM0IF41	TM0MK41	0	0	0	TM0PR412	TM0PR411	TM0PR410
FFFFF15CH	TM0IC50	TM0IF50	TM0MK50	0	0	0	TM0PR502	TM0PR501	TM0PR500
FFFFF15EH	TM0IC51	TM0IF51	TM0MK51	0	0	0	TM0PR512	TM0PR511	TM0PR510
FFFFF160H	CSI0IC2	CSI0IF2	CSI0MK2	0	0	0	CSI0PR22	CSI0PR21	CSI0PR20

Note Only for the μPD703216Y, 703217Y, and 70F3217Y

Table 19-6. Interrupt Control Registers (xxICn) (V850ES/KJ1) (2/2)

Address	Register	Bits							
		<7>	<6>	5	4	3	2	1	0
FFFFF162H	SREIC2	SREIF2	SREMK2	0	0	0	SREPR22	SREPR21	SREPR20
FFFFF164H	SRIC2	SRIF2	SRMK2	0	0	0	SRPR22	SRPR21	SRPR20
FFFFF166H	STIC2	STIF2	STMK2	0	0	0	STPR22	STPR21	STPR20
FFFFF168H	IICIC1[Note]	IICIF1	IICMK1	0	0	0	IICPR12	IICPR11	IICPR10

Note Only for the μPD703216Y, 703217Y, and 70F3217Y

19.3.5 Interrupt mask registers 0 to 2 (IMR0 to IMR2)

These registers set the interrupt mask status for maskable interrupts. Bits xxMKn of the IMR0 to IMR2 register and bits xxMKn of the xxICn register are respectively linked.

The IMRm register can be read/written in 16-bit units (m = 0 to 2).

When the higher 8 bits of the IMRm register are treated as the IMRmH register and the lower 8 bits of the IMRm register as the IMRmL register, they can be read/written in 8-bit or 1-bit units (m = 0 to 2).

Caution In the device file, the xxMKn bit of the xxICn register is defined as a reserved word. Therefore, if bit manipulation is performed using the name xxMKn, the xxICn register, not the IMRm register, is rewritten (as a result, the IMRm register is also rewritten).

(i) V850ES/KF1

After reset: FFFFH R/W Address: FFFFF100H (IMR0, IMR0L), FFFFF101H (IMR0H)

	15	14	13	12	11	10	9	8
IMR0 (IMR0H[Note])	CSI0MK1	CSI0MK0	TM5MK1	TM5MK0	TM0MK11	TM0MK10	TM0MK01	TM0MK00
	7	6	5	4	3	2	1	0
(IMR0L)	PMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	WDT1MK

After reset: FFFFH R/W Address: FFFFF102H (IMR1, IMR1L), FFFFF103H (IMR1H)

	15	14	13	12	11	10	9	8
IMR1 (IMR1H[Note])	1	BRGMK	WTMK	WTIMK	KRMK	ADMK	IICMK0	CSIAMK0
	7	6	5	4	3	2	1	0
(IMR1L)	TMHMK1	TMHMK0	STMK1	SRMK1	SREMK1	STMK0	SRMK0	SREMK0

xxMKn	Interrupt mask flag setting
0	Enables interrupt servicing
1	Disables interrupt servicing

Note When reading from or writing to bits 8 to 15 of the IMR0 and IMR1 registers in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the IMR0H and IMR1H registers.

Caution Set bit 15 of the IMR1 register to 1. The operation is not guaranteed if the value is changed.

Remark xx: Identifying name of each peripheral unit (CSI0, TM5, TM0, P, WDT, BRG, WT, WTI, KR, AD, IIC, CSIA, TMH, ST, SR, SRE)
n: Peripheral unit number (See **Tables 19-4** to **19-6**.)

(ii) V850ES/KG1

After reset: FFFFH R/W Address: FFFFF100H (IMR0, IMR0L), FFFFF101H (IMR0H)

	15	14	13	12	11	10	9	8
IMR0 (IMR0H[Note])	CSI0MK1	CSI0MK0	TM5MK1	TM5MK0	TM0MK11	TM0MK10	TM0MK01	TM0MK00
	7	6	5	4	3	2	1	0
(IMR0L)	PMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	WDT1MK

After reset: FFFFH R/W Address: FFFFF102H (IMR1, IMR1L), FFFFF103H (IMR1H)

	15	14	13	12	11	10	9	8
IMR1 (IMR1H[Note])	TM0MK20	BRGMK	WTMK	WTIMK	KRMK	ADMK	IICMK0	CSIAMK0
	7	6	5	4	3	2	1	0
(IMR1L)	TMHMK1	TMHMK0	STMK1	SRMK1	SREMK1	STMK0	SRMK0	SREMK0

After reset: FFFFH R/W Address: FFFFF104H (IMR2, IMR2L), FFFFF105H (IMR2H)

	15	14	13	12	11	10	9	8
IMR2 (IMR2H[Note])	1	1	1	1	1	1	1	1
	7	6	5	4	3	2	1	0
(IMR2L)	1	1	1	1	CSIAMK1	TM0MK31	TM0MK30	TM0MK21

xxMKn	Interrupt mask flag setting
0	Enables interrupt servicing
1	Disables interrupt servicing

Note When reading from or writing to bits 8 to 15 of the IMR0 to IMR2 registers in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the IMR0H to IMR2H registers.

Caution Set bits 15 to 4 of the IMR2 register to 1. The operation is not guaranteed if their value is changed.

Remark xx: Identifying name of each peripheral unit (CSI0, TM5, TM0, P, WDT, BRG, WT, WTI, KR, AD, IIC, CSIA, TMH, ST, SR, SRE)
n: Peripheral unit number (See **Tables 19-4** to **19-6**.)

(iii) V850ES/KJ1

After reset: FFFFH R/W Address: FFFFF100H (IMR0, IMR0L), FFFFF101H (IMR0H)

	15	14	13	12	11	10	9	8
IMR0 (IMR0H[Note])	CSI0MK1	CSI0MK0	TM5MK1	TM5MK0	TM0MK11	TM0MK10	TM0MK01	TM0MK00
	7	6	5	4	3	2	1	0
(IMR0L)	PMK6	PMK5	PMK4	PMK3	PMK2	PMK1	PMK0	WDT1MK

After reset: FFFFH R/W Address: FFFFF102H (IMR1, IMR1L), FFFFF103H (IMR1H)

	15	14	13	12	11	10	9	8
IMR1 (IMR1H[Note])	TM0MK20	BRGMK	WTMK	WTIMK	KRMK	ADMK	IICMK0	CSIAMK0
	7	6	5	4	3	2	1	0
(IMR1L)	TMHMK1	TMHMK0	STMK1	SRMK1	SREMK1	STMK0	SRMK0	SREMK0

After reset: FFFFH R/W Address: FFFFF104H (IMR2, IMR2L), FFFFF105H (IMR2H)

	15	14	13	12	11	10	9	8
IMR2 (IMR2H[Note])	1	1	1	IICMK1	STMK2	SRMK2	SREMK2	CSI0MK2
	7	6	5	4	3	2	1	0
(IMR2L)	TM0MK51	TM0MK50	TM0MK41	TM0MK40	CSIAMK1	TM0MK31	TM0MK30	TM0MK21

xxMKn	Interrupt mask flag setting
0	Enables interrupt servicing
1	Disables interrupt servicing

Note When reading from or writing to bits 8 to 15 of the IMR0 to IMR2 registers in 8-bit or 1-bit units, specify these bits as bits 0 to 7 of the IMR0H to IMR2H registers.

Caution Set bits 15 to 13 of the IMR2 register to 1. The operation is not guaranteed if their value is changed.

Remark xx: Identifying name of each peripheral unit (CSI0, TM5, TM0, P, WDT, BRG, WT, WTI, KR, AD, IIC, CSIA, TMH, ST, SR, SRE)
n: Peripheral unit number (See **Tables 19-4** to **19-6**.)

19.3.6 In-service priority register (ISPR)

This register holds the priority level of the maskable interrupt currently being acknowledged. When the interrupt request is acknowledged, the bit of this register corresponding to the priority level of that interrupt is set (1) and remains set while the interrupt is being serviced.

When the RETI instruction is executed, the bit among those that are set (1) in the ISPR register that corresponds to the interrupt request having the highest priority is automatically reset (0) by hardware. However, it is not reset (0) when execution is returned from non-maskable interrupt servicing or exception processing.

This register can only be read, in 8-bit or 1-bit units.

After reset, ISPR is cleared to 00H.

Caution If an interrupt is acknowledged while the ISPR register is being read in the interrupt enabled (EI) status, the value of the ISPR register after the bits of the register have been set to 1 by acknowledging the interrupt may be read. To accurately read the value of the ISPR register before an interrupt is acknowledged, read the register while interrupts are disabled (DI status).

After reset: 00H R Address: FFFFF1FAH

	<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
ISPR	ISPR7	ISPR6	ISPR5	ISPR4	ISPR3	ISPR2	ISPR1	ISPR0

ISPRn	Priority of interrupt currently being acknowledged
0	Interrupt request with priority n is not acknowledged
1	Interrupt request with priority n is being acknowledged

Remark n = 0 to 7 (priority level)

19.3.7 Maskable interrupt status flag

The interrupt disable flag (ID) is allocated to the PSW and controls the maskable interrupt's operating state, and stores control information regarding enabling/disabling reception of interrupt requests.

After reset, this flag is set to 00000020H.

After reset: 00000020H

	31	8	7	6	5	4	3	2	1	0
PSW	0		NP	EP	**ID**	SAT	CY	OV	S	Z

ID	Maskable interrupt servicing specification[Note]
0	Maskable interrupt acknowledgment enabled
1	Maskable interrupt acknowledgment disabled

Note Interrupt disable flag (ID) function

ID is set (1) by the DI instruction and reset (0) by the EI instruction. Its value is also modified by the RETI instruction or LDSR instruction when referencing the PSW.

Non-maskable interrupts and exceptions are acknowledged regardless of this flag. When a maskable interrupt is acknowledged, the ID flag is automatically set (1) by hardware.

An interrupt request generated during the acknowledgment disabled period (ID = 1) can be acknowledged when the xxIFn bit of xxICn is set (1), and the ID flag is reset (0).

19.3.8 Watchdog timer mode register 1 (WDTM1)

This register is a special register that can be written to only in a special sequence. To generate a maskable interrupt (INTWDT1), set the WDTM14 bit to 0.

This register can be read/written in 8-bit or 1-bit units (for details, refer to **CHAPTER 11 WATCHDOG TIMER FUNCTIONS**).

After reset: 00H R/W Address: FFFFF6C2H

	<7>	6	5	4	3	2	1	0
WDTM1	RUN1	0	0	WDTM14	WDTM13	0	0	0

RUN1	Watchdog timer operation mode selection[Note 1]
0	Stop count operation
1	Clear counter and start count operation

WDTM14	WDTM13	Watchdog timer operation mode selection[Note 2]
0	0	Interval timer mode
0	1	(Generate maskable interrupt INTWDTM1 when overflow occurs)
1	0	Watchdog timer mode 1[Note 3]
		(Generate non-maskable interrupt INTWDT1 when overflow occurs)
1	1	Watchdog timer mode 2
		(Start WDTRES2 reset operation when overflow occurs)

Notes 1. Once the RUN1 bit has been set (1), it cannot be cleared (0) by software. Therefore, once counting starts, it cannot be stopped except through $\overline{\text{RESET}}$ input.

2. Once the WDTM14 and WDTM13 bits have been set (1), they cannot be cleared (0) by software. $\overline{\text{RESET}}$ input is the only way to clear these bits.

3. For non-maskable interrupt servicing due to a non-maskable interrupt request (INTWDT1), refer to **19.10 Cautions**.

19.4 External Interrupt Request Input Pins (NMI, INTP0 to INTP6)

19.4.1 Noise elimination

(1) Noise elimination for NMI pin

The NMI pin includes a noise eliminator that operates using analog delay. Therefore, a signal input to the NMI pin is not detected as an edge unless it maintains its input level for a certain period. The edge is detected only after a certain period has elapsed.

The NMI pin is used for releasing the STOP mode. In the STOP mode, noise elimination using the system clock is not performed because the internal system clock is stopped.

(2) Noise elimination for INTP0 to INTP6 pins

The INTP0 to INTP6 pins include a noise eliminator that operates using analog delay. Therefore, a signal input to each pin is not detected as an edge unless it maintains its input level for a certain period. The edge is detected only after a certain period has elapsed.

19.4.2 Edge detection

The valid edges of the NMI and INTP0 to INTP6 pins can be selected from the following four types for each pin.

- Falling edge
- Rising edge
- Both edges
- No edge detection

After reset, the edge detection for the NMI pin is set to “no edge detection”. Therefore, interrupt requests cannot be acknowledged (the NMI pin functions as a normal port) unless a valid edge is specified by the INTF0 and INTR0 registers.

When using P02 as an output port, set the NMI pin valid edge to “no edge detection”.

(1) External interrupt rising edge specification register 0 (INTR0), external interrupt falling edge specification register 0 (INTF0)

This is an 8-bit register that specifies detection of the rising and falling edges of the NMI and INTP0 to INTP3 pins.

This register can be read/written in 8-bit or 1-bit units.

Caution When switching to the port function from the external interrupt function (alternate function), edge detection may be performed. Therefore, set the port mode after setting INTF0n = INTR0n = 0.

After reset: 00H R/W Address: INTR0 FFFFFC20H, INTF0 FFFFFC00H

	7	6	5	4	3	2	1	0
INTR0	0	INTR06	INTR05	INTR04	INTR03	INTR02	0	0
		INTP3	INTP2	INTP1	INTP0	NMI		
INTF0	0	INTF06	INTF05	INTF04	INTF03	INTF02	0	0
		INTP3	INTP2	INTP1	INTP0	NMI		

Remark For specification of the valid edge, refer to **Table 19-7**.

Table 19-7. INTP0 to INTP3 Pins Valid Edge Specification

INTF0n	INTR0n	Valid edge specification (n = 2 to 6)
0	0	No edge detection
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

Remark n = 2: Control of NMI pin

n = 3 to 6: Control of INTP0 to INTP3 pins

(2) External interrupt rising edge specification register 9H (INTR9H), external interrupt falling edge specification register 9H (INTF9H)

This is an 8-bit register that specifies detection of the rising edge of the INTP4 to INTP6 pins.

This register can be read/written in 8-bit or 1-bit units.

Caution When switching to the port function from the external interrupt function (alternate function), edge detection may be performed. Therefore, set the port mode after setting INTF9n = INTR9n = 0.

After reset: 00H R/W Address: INTR9H FFFFFC33H, INTF9H FFFFFC13H

	7	6	5	4	3	2	1	0
INTR9H	INTR915	INTR914	INTR913	0	0	0	0	0
	INTP6	INTP5	INTP4					
	7	6	5	4	3	2	1	0
INTF9H	INTF915	INTF914	INTF913	0	0	0	0	0
	INTP6	INTP5	INTP4					

Remark For specification of the valid edge, refer to **Table 19-8**.

Table 19-8. INTP4 to INTP6 Pins Valid Edge Specification

INTF9n	INTR9n	Valid edge specification (n = 13 to 15)
0	0	No edge detection
0	1	Rising edge
1	0	Falling edge
1	1	Both edges

Remark n = 13 to 15: Control of INTP4 to INTP6 pins

19.5 Software Exceptions

A software exception is generated when the CPU executes the TRAP instruction. Software exceptions can always be acknowledged.

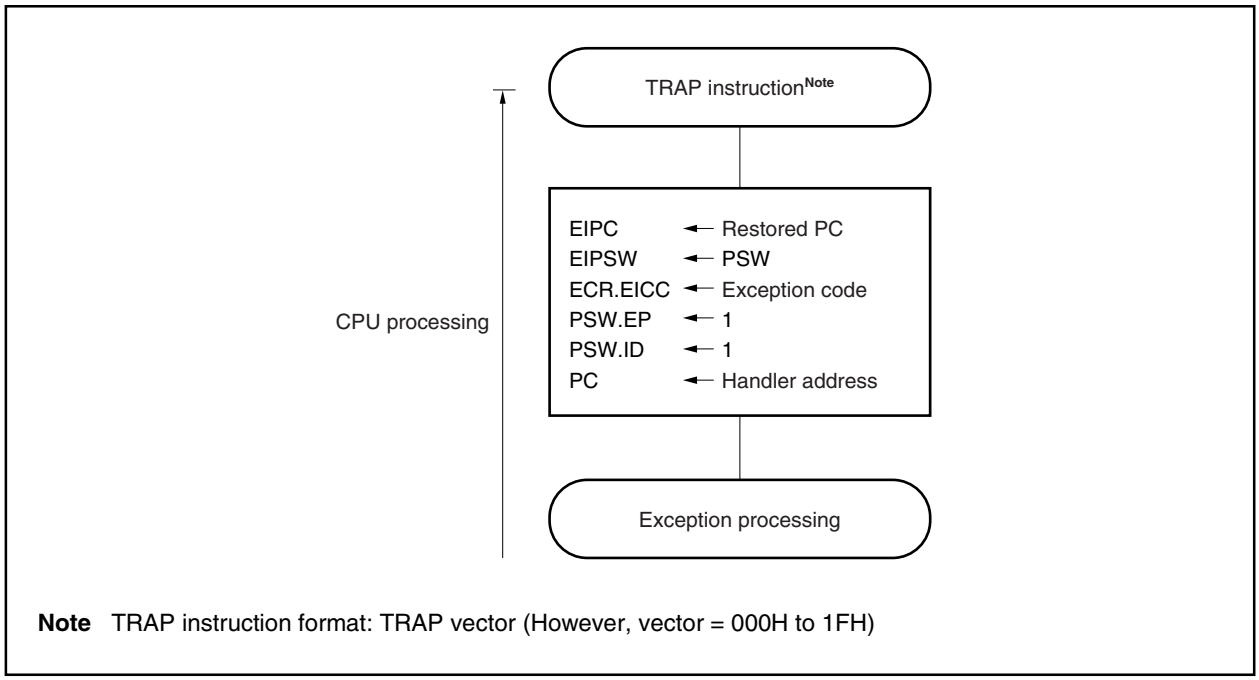
19.5.1 Operation

If a software exception occurs, the CPU performs the following processing and transfers control to a handler routine.

<1> Saves the restored PC to EIPC.
<2> Saves the current PSW to EIPSW.
<3> Writes an exception code to the lower 16 bits (EICC) of ECR (interrupt source).
<4> Sets the EP and ID bits of the PSW.
<5> Loads the handler address (00000040H or 00000050H) for the software exception routine to the PC and transfers control.

Figure 19-8 shows the software exception processing flow.

Figure 19-8. Software Exception Processing



Note TRAP instruction format: TRAP vector (However, vector = 000H to 1FH)

The handler address is determined by the operand (vector) of the TRAP instruction. If the vector is 000H to 1FH, the handler address is 00000040H, and if the vector is 10 to 1FH, the handler address is 00000050H.

19.5.2 Restore

Execution is restored from software exception processing by the RETI instruction.

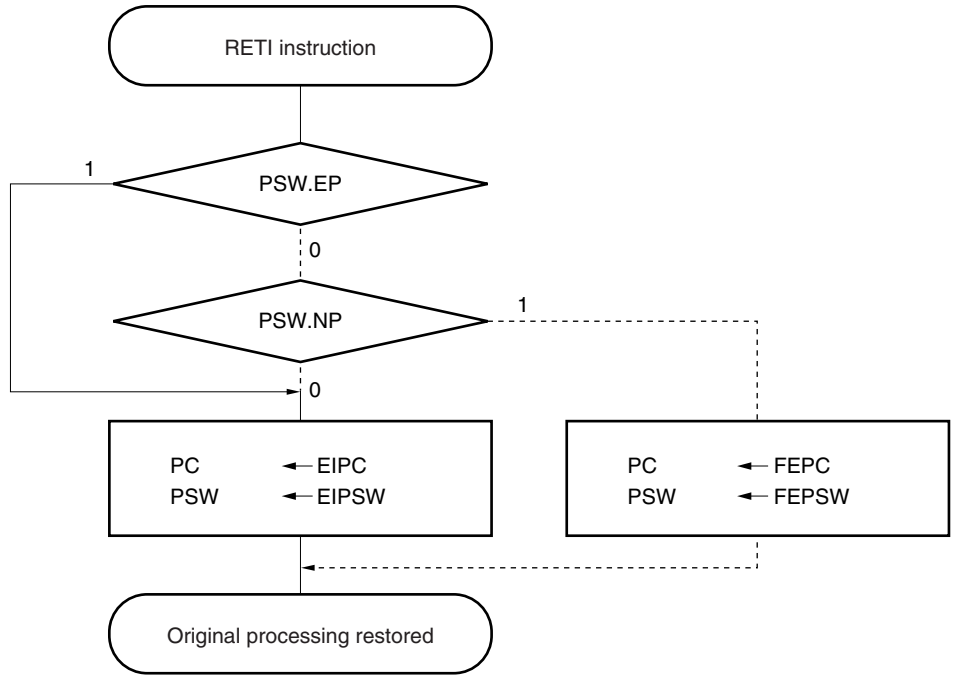
When the RETI instruction is executed, the CPU performs the following processing and transfers control to the address of the restored PC.

<1> Loads the restored PC and PSW from EIPC and EIPSW because the EP bit of the PSW is 1.

<2> Transfers control to the address of the restored PC and PSW.

Figure 19-9 shows the processing flow of the RETI instruction.

Figure 19-9. RETI Instruction Processing



Caution When the PSW.EP bit and PSW.NP bit are changed by the LDSR instruction during software exception processing, in order to restore the PC and PSW correctly during restoring by the RETI instruction, it is necessary to set PSW.EP back to 1 using the LDSR instruction immediately before the RETI instruction.

Remark The solid line shows the CPU processing flow.

19.5.3 Exception status flag (EP)

The EP flag, which is bit 6 of the PSW, is a status flag that indicates that exception processing is in progress. It is set when an exception occurs.

After reset: 00000020H

	31	8	7	6	5	4	3	2	1	0
PSW	0		NP	**EP**	ID	SAT	CY	OV	S	Z

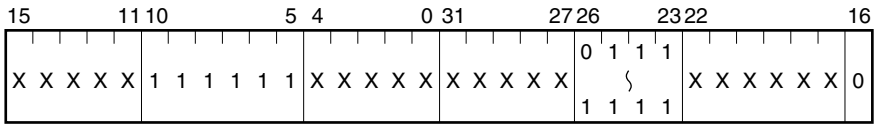
EP	Exception processing status
0	Exception processing not in progress
1	Exception processing in progress

19.6 Exception Trap

The exception trap is an interrupt that is requested when the illegal execution of an instruction takes place. In the V850ES/KF1, V850ES/KG1, and V850ES/KJ1, an illegal op code trap (ILGOP: illegal OP code trap) is considered as an exception trap.

19.6.1 Illegal op code

An illegal op code is defined as an instruction with instruction op code (bits 10 to 5) = 111111B, sub-op code (bits 26 to 23) = 0111B to 1111B, and sub-op code (bit 16) = 0B. When such an instruction is executed, an exception trap is generated.



X: Don't care

Caution It is recommended not to use illegal op code because instructions may newly be assigned in the future.

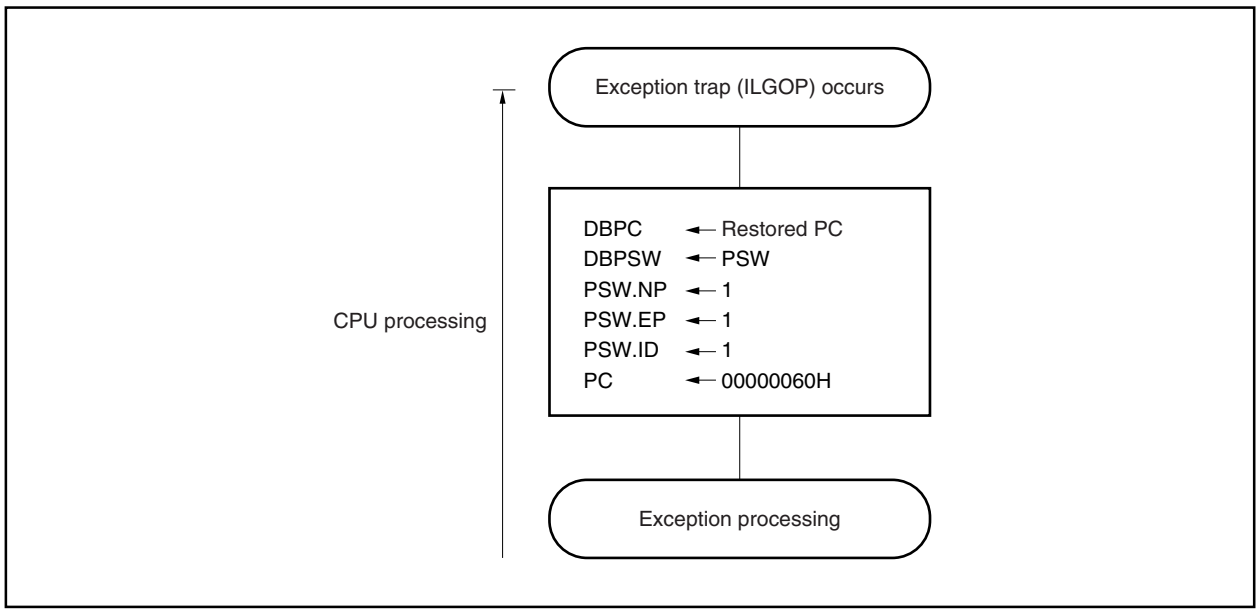
(1) Operation

Upon generation of an exception trap, the CPU performs the following processing and transfers control to a handler routine.

<1> Saves the restored PC to DBPC.
<2> Saves the current PSW to DBPSW.
<3> Sets the NP, EP, and ID bits of the PSW.
<4> Loads the handler address (00000060H) for the exception trap routine to the PC and transfers control.

Figure 19-10 shows the exception trap processing flow.

Figure 19-10. Exception Trap Processing



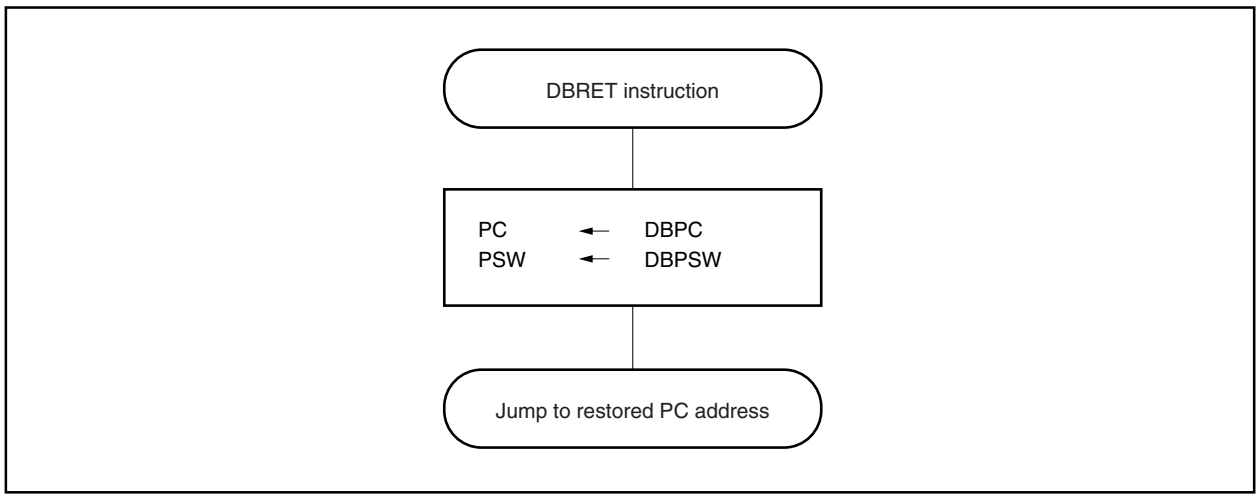
(2) Restore

Execution is restored from exception trap processing by the DBRET instruction. When the DBRET instruction is executed, the CPU performs the following processing and transfers control to the address of the restored PC.

<1> Loads the restored PC and PSW from DBPC and DBPSW.
<2> Transfers control to the loaded address of the restored PC and PSW.

Figure 19-11 shows the processing flow for restore from exception trap processing.

Figure 19-11. Processing Flow for Restore from Exception Trap



19.6.2 Debug trap

A debug trap is an exception that occurs upon execution of the DBTRAP instruction and that can be acknowledged at all times.

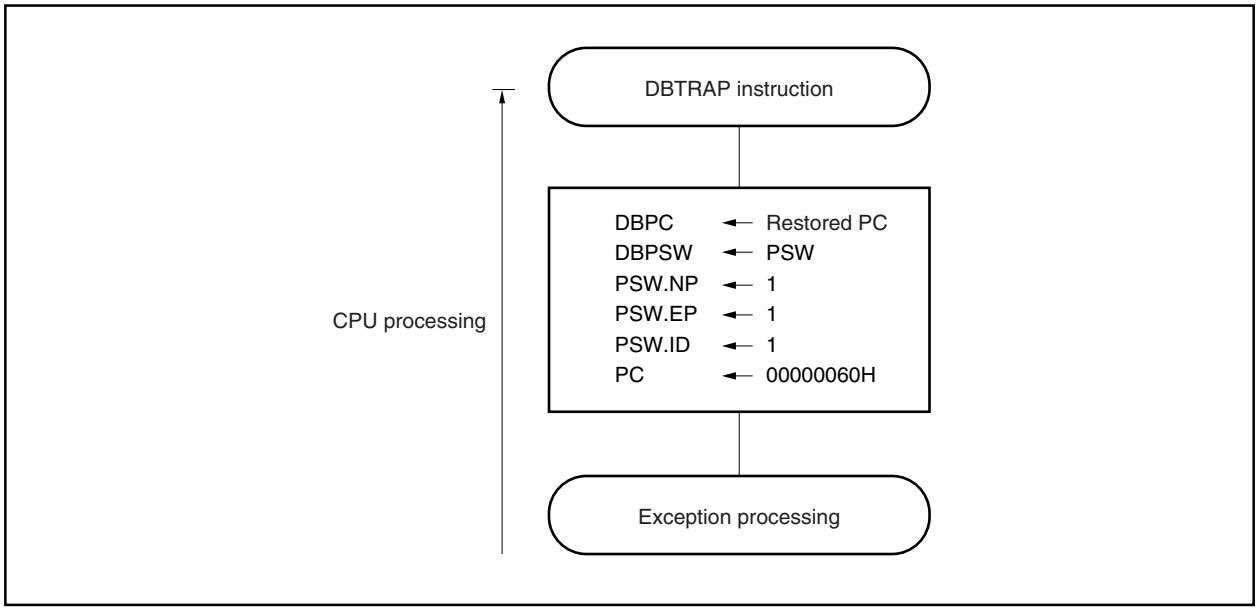
When a debug trap occurs, the CPU performs the following processing.

(1) Operation

<1> Saves the restored PC to DBPC.
<2> Saves the current PSW to DBPSW.
<3> Sets the NP, EP, and ID bits of the PSW.
<4> Sets the handler address (00000060H) for the debug trap routine to the PC and transfers control.

Figure 19-12 shows the debug trap processing flow.

Figure 19-12. Debug Trap Processing



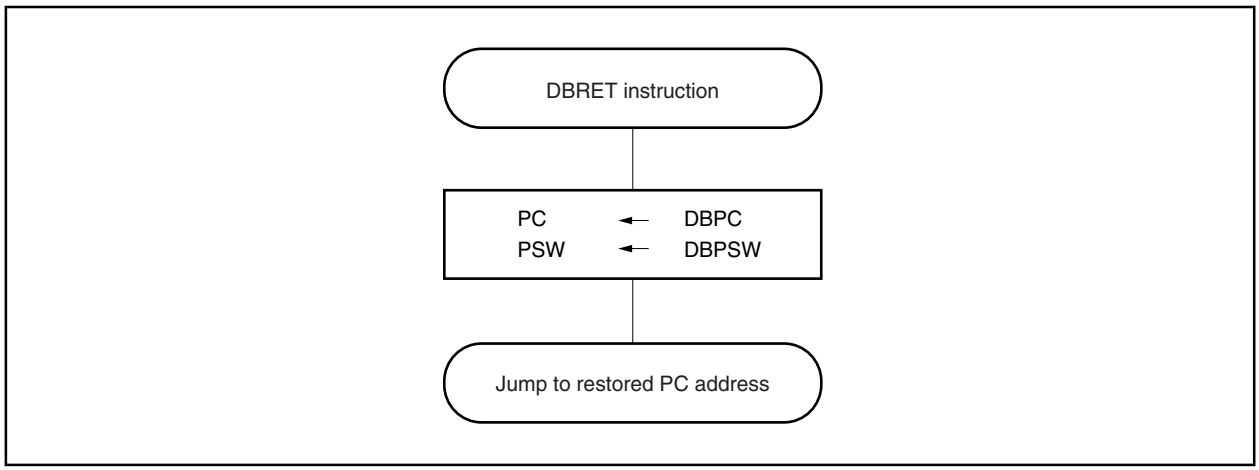
(2) Restore

Execution is restored from debug trap processing by the DBRET instruction. When the DBRET instruction is executed, the CPU performs the following processing and transfers control to the address of the restored PC.

<1> Loads the restored PC and PSW from DBPC and DBPSW.
<2> Transfers control to the loaded address of the restored PC and PSW.

Figure 19-13 shows the processing flow for restore from debug trap processing.

Figure 19-13. Processing Flow for Restore from Debug Trap



19.7 Multiple Interrupt Servicing Control

Multiple interrupt servicing control is a function that stops an interrupt service routine currently in progress if a higher priority interrupt request is generated, and processes the acknowledgment operation of the higher priority interrupt.

If an interrupt with a lower or equal priority is generated and a service routine is currently in progress, the later interrupt will be held pending.

Multiple interrupt servicing control is performed when interrupts are enabled (ID = 0). Even in an interrupt servicing routine, multiple interrupt control must be performed while interrupts are enabled (ID = 0). If a maskable interrupt or software exception is generated in a maskable interrupt or software exception service program, EIPC and EIPSW must be saved.

The following example illustrates the procedure.

(1) To acknowledge maskable interrupt requests in service program

Service program for maskable interrupt or exception

```
    …
    …
• EIPC saved to memory or register
• EIPSW saved to memory or register
• EI instruction (enables interrupt acknowledgment)
    …
    …                                  ←Acknowledges maskable interrupt
    …
    …
• DI instruction (disables interrupt acknowledgment)
• Saved value restored to EIPSW
• Saved value restored to EIPC
• RETI instruction
```

(2) To generate exception in service program

Service program for maskable interrupt or exception

…
…
- EIPC saved to memory or register
- EIPSW saved to memory or register

…
- TRAP instruction

…
- Saved value restored to EIPSW
- Saved value restored to EIPC
- RETI instruction

←Acknowledges exceptions such as TRAP instruction.

Priorities 0 to 7 (0 is the highest) can be set for each maskable interrupt request in multiple interrupt servicing control by software. To set a priority level, write values to the xxPRn0 to xxPRn2 bits of the interrupt request control register (xxICn) corresponding to each maskable interrupt request. After reset, interrupt requests are masked by the xxMKn bit, and the priority is set to level 7 by the xxPRn0 to xxPRn2 bits.

Priorities of maskable interrupts are as follows.

(High) Level 0 > Level 1 > Level 2 > Level 3 > Level 4 > Level 5 > Level 6 > Level 7 (Low)

Interrupt servicing that has been suspended as a result of multiple interrupt servicing control is resumed after the interrupt servicing of the higher priority has been completed and the RETI instruction has been executed.
A pending interrupt request is acknowledged after the current interrupt servicing has been completed and the RETI instruction has been executed.

Caution In a non-maskable interrupt servicing routine (in the time until the RETI instruction is executed), maskable interrupts are not acknowledged and held pending.

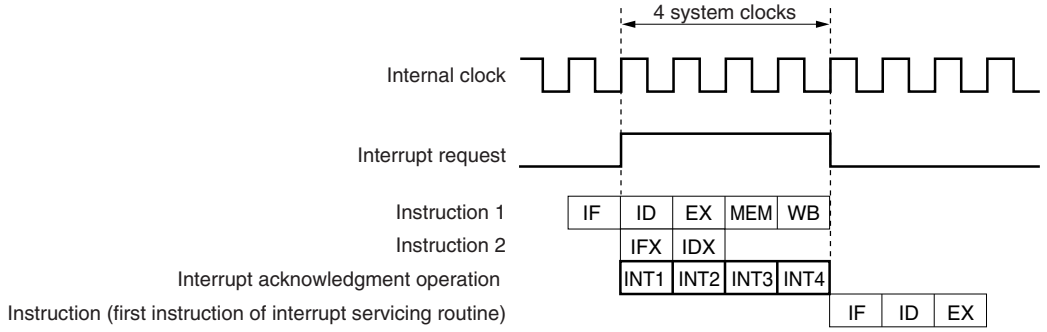
19.8 Interrupt Response Time

Except in the following cases, the CPU interrupt response time is a minimum of 4 clocks. If inputting consecutive interrupt requests, at least 4 clocks must be placed between each interrupt.

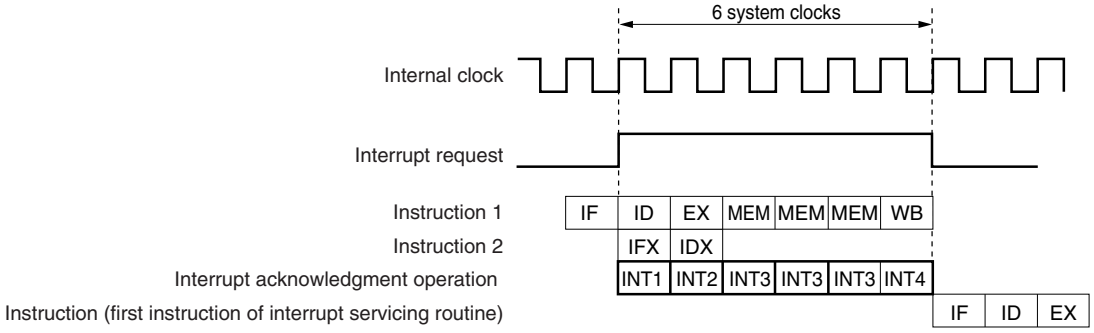
- IDLE/STOP mode
- External bus access
- Consecutive interrupt request non-sample instruction
- Access to interrupt control register
- Access to peripheral I/O register

Figure 19-14. Pipeline Operation During Interrupt Request Acknowledgment (Outline)

(1) Minimum interrupt response time



(2) Maximum interrupt response time



INT1 to INT4: Interrupt acknowledgment processing
IFX: Invalid instruction fetch
IDX: Invalid instruction decode

Interrupt response time (internal system clock)			Condition
	Internal interrupt	External interrupt	
Min.	4	4 + analog delay	The following cases are excluded. • IDLE/STOP mode • External bus access • Consecutive interrupt request non-sample instruction • Access to interrupt control register • Access to peripheral I/O register
Max.	6	6 + analog delay	

19.9 Periods in Which Interrupts Are Not Acknowledged by CPU

Interrupts are acknowledged by the CPU while an instruction is being executed. However, no interrupt is acknowledged between an interrupt request non-sample instruction and the next instruction.

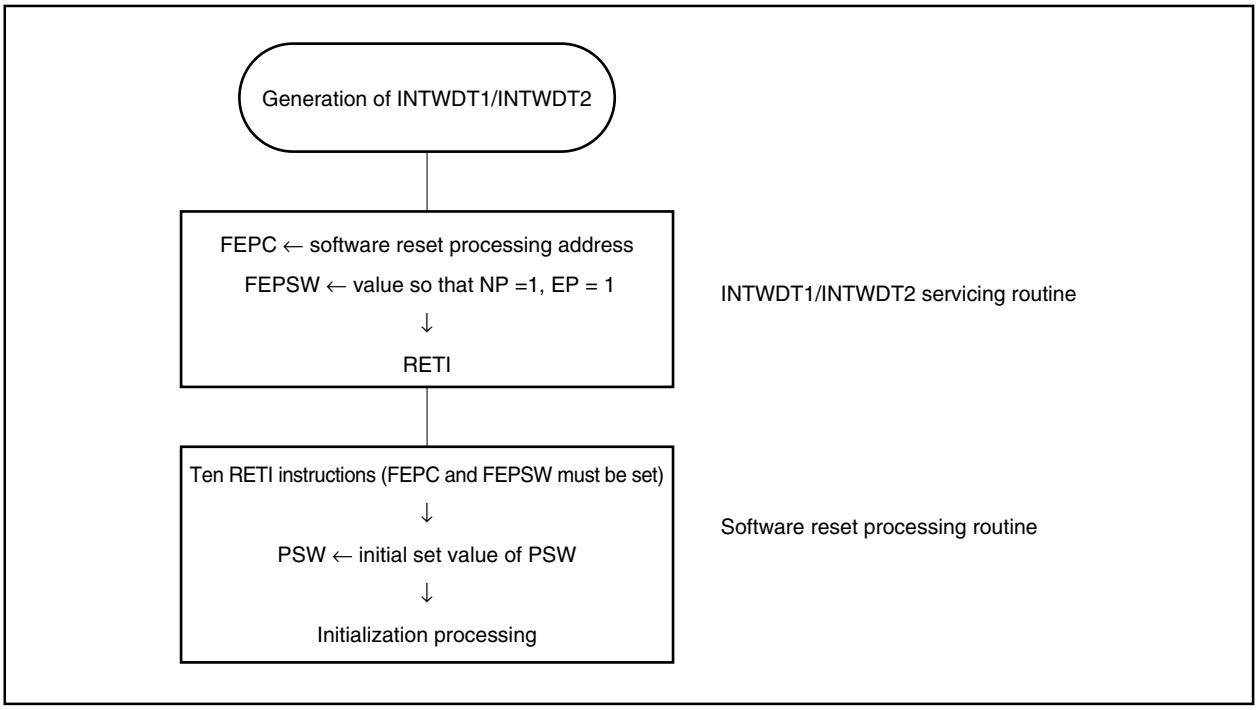
The following instructions are interrupt request non-sample instructions.

- EI instruction
- DI instruction
- LDSR reg2, 0x5 instructions (vs. PSW)
- Store instruction for command register (PRCMD)
- Store instruction and bit manipulation instruction for the following registers
  - Interrupt-related registers:
    Interrupt control register (xxICn), interrupt mask registers 0 to 2 (IMR0 to IMR2)

★ 19.10 Cautions

Design the system so that restoring by the RETI instruction is as follows after a maskable interrupt triggered by a non-maskable interrupt request (INTWDT1/INTWDT2) is serviced.

Figure 19-15. Restoring by RETI



CHAPTER 20 KEY INTERRUPT FUNCTION

20.1 Function

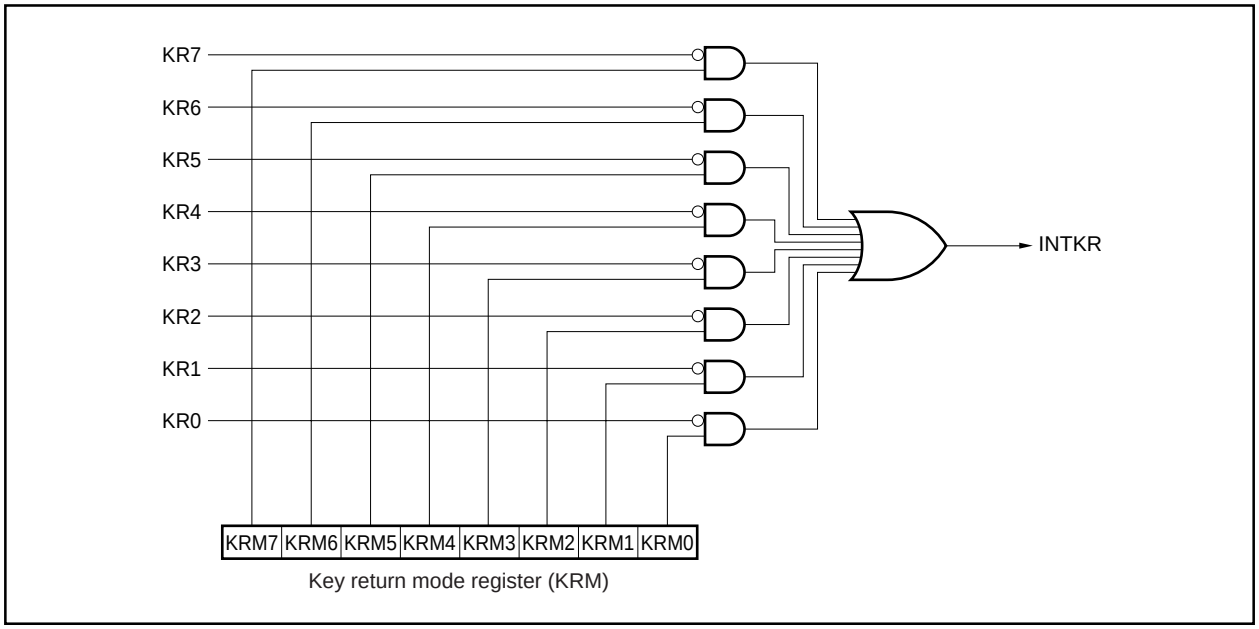
A key interrupt (INTKR) can be generated by inputting a falling edge to the eight key input pins (KR0 to KR7) by setting the key return mode register (KRM).

Caution If any of KR0 to KR7 is at low level, an interrupt is not generated even if a falling edge is input to another pin.

Table 20-1. Assignment of Key Return Detection Pins

Flag	Pin Description
KRM0	Controls KR0 signal in 1-bit units
KRM1	Controls KR1 signal in 1-bit units
KRM2	Controls KR2 signal in 1-bit units
KRM3	Controls KR3 signal in 1-bit units
KRM4	Controls KR4 signal in 1-bit units
KRM5	Controls KR5 signal in 1-bit units
KRM6	Controls KR6 signal in 1-bit units
KRM7	Controls KR7 signal in 1-bit units

Figure 20-1. Key Return Block Diagram



20.2 Key Interrupt Control Register

(1) Key return mode register (KRM)

The KRM register controls the KRM0 to KRM7 bits using the KR0 to KR7 signals.

This register can be read/written in 8-bit or 1-bit units.

After reset, KRM is cleared to 00H.

After reset: 00H R/W Address: FFFFF300H

	7	6	5	4	3	2	1	0
KRM	KRM7	KRM6	KRM5	KRM4	KRM3	KRM2	KRM1	KRM0

KRMn	Key return mode control
0	Does not detect key return signal
1	Detects key return signal

Caution If the key return mode register (KRM) is changed, an interrupt request flag may be set. To prevent this, change the KRM register after disabling interrupts, and then enable interrupts after clearing the interrupt request flag.

Remark For the alternate-function pin settings, refer to **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**.

CHAPTER 21 STANDBY FUNCTION

21.1 Overview

The power consumption of the system can be effectively reduced by using the standby modes in combination and selecting the appropriate mode for the application.

The available standby modes are listed in Table 21-1.

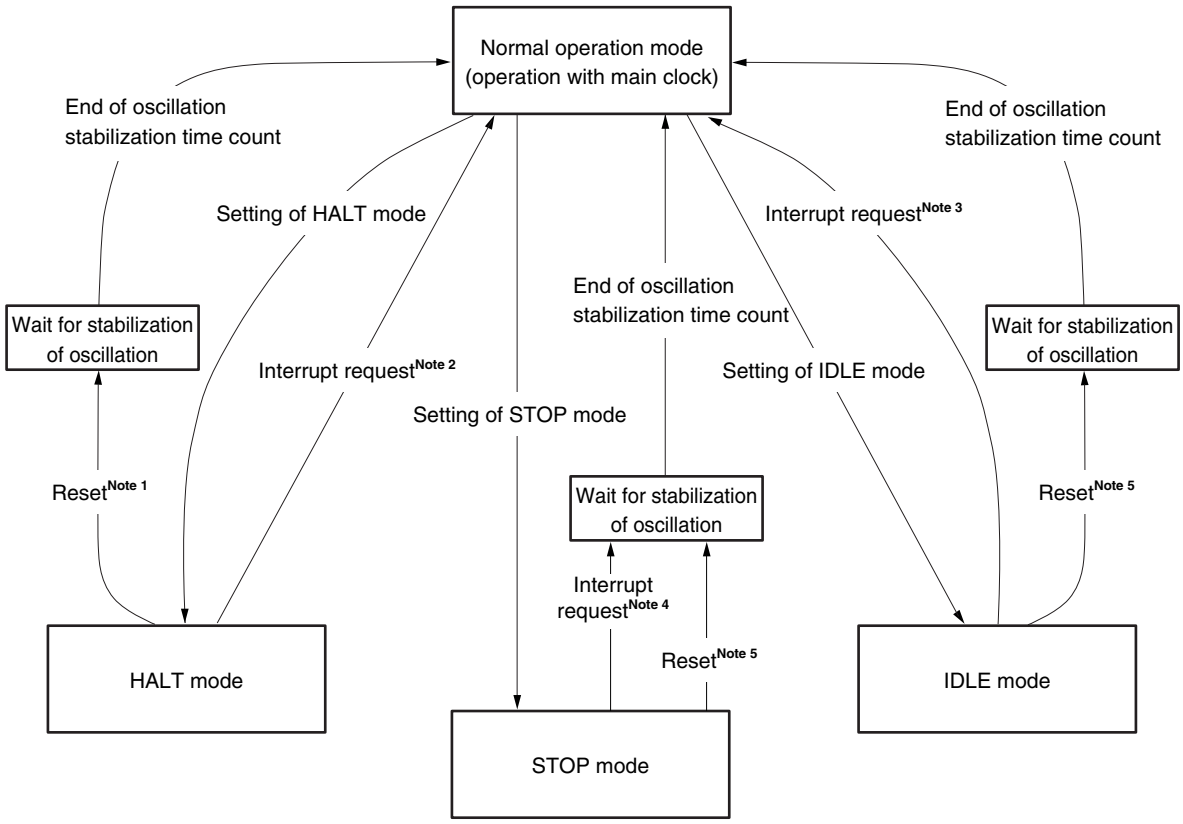
Table 21-1. Standby Modes

Mode	Functional Outline
HALT mode	Mode to stop only the operating clock of the CPU
IDLE mode	Mode to stop all the operations of the internal circuits except the oscillator[Note 1]
STOP mode	Mode to stop all the operations of the internal circuits except the subclock oscillator[Note 2]
Subclock operation mode	Mode to use the subclock as the internal system clock
Sub-IDLE mode	Mode to stop all the operations of the internal circuits, except the oscillator, in the subclock operation mode

★ **Notes 1.** The PLL does not stop. To realize low power consumption, stop the PLL and then shift to the IDLE mode.

★ **2.** Change to the clock-through mode, stop the PLL, then shift to the STOP mode. For details, refer to **CHAPTER 6 CLOCK GENERATION FUNCTION**.

Figure 21-1. Status Transition (1/2)



Notes 1. Reset input by $\overline{\text{RESET}}$ input, watchdog timer 1 overflow, or watchdog timer 2 overflow.

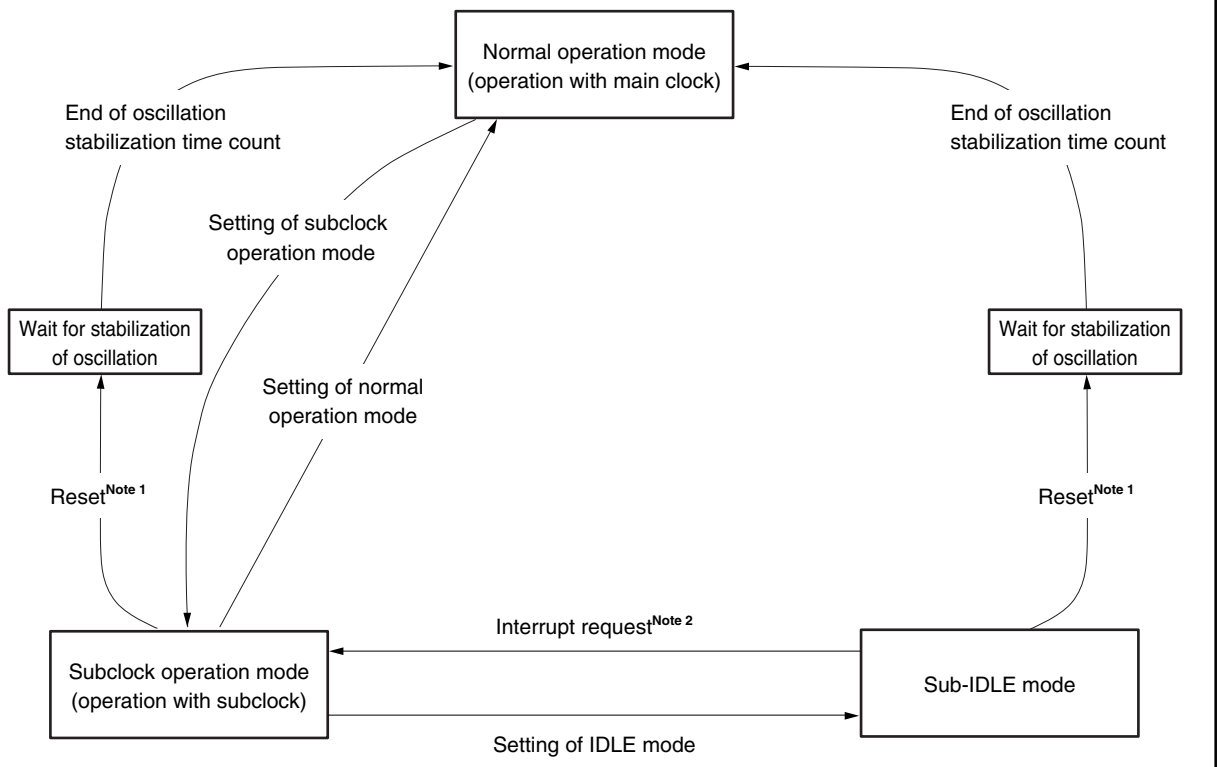
2. Non-maskable interrupt request or unmasked maskable interrupt request.

3. Non-maskable interrupt request (NMI pin input), unmasked external interrupt request (INTP0 to INTP6 pin input), or unmasked internal interrupt request from peripheral functions operable in IDLE mode.

4. Non-maskable interrupt request (NMI pin input), unmasked external interrupt request (INTP0 to INTP6 pin input), or unmasked internal interrupt request from peripheral functions operable in STOP mode.

5. Reset input by $\overline{\text{RESET}}$ input or watchdog timer 2 (when the CPU is operating on the subclock) overflow.

Figure 21-1. Status Transition (2/2)



Notes 1. Reset input by $\overline{\text{RESET}}$ input or watchdog timer 2 overflow.

2. Non-maskable interrupt request (NMI pin input), unmasked external interrupt request (INTP0 to INTP6 pin input), or unmasked internal interrupt request from peripheral functions operable in sub-IDLE mode.

21.2 Registers

(1) Power save control register (PSC)

This is an 8-bit register that controls the standby function. The STP bit of this register is used to specify the standby mode. The PSC register is a special register (refer to **3.4.7 Special registers**). Data can be written to this register only in a specific sequence so that its contents are not rewritten by mistake due to a program hang-up.

This register can be read or written in 8-bit or 1-bit units.

After reset: 00H R/W Address: FFFFF1FEH

	<7>	6	<5>	<4>	3	2	<1>	0
PSC	NMI2M	0	NMI0M	INTM	0	0	STP	0

NMI2M	Control of non-maskable interrupt request (INTWDT2) from watchdog timer 2[Note 1]
0	INTWDT2 request enabled
1	INTWDT2 request disabled

NMI0M	Control of non-maskable interrupt request from NMI pin[Note 1]
0	NMI request enabled
1	NMI request disabled

INTM	Control of all non-maskable interrupt requests (INTxx[Note 2])[Note 1]
0	INTxxx request enabled
1	INTxxx request disabled

STP	Standby mode setting
0	Normal mode
1	Standby mode[Note 3]

Notes 1. Setting these bits is valid only in the IDLE/STOP mode.

2. For details, refer to **Tables 19-1** to **19-3 Interrupt Sources**.

3. Set the STOP or IDLE mode using the PSM bit of the PSMR register.

Caution If the NMI2M, NMI0M, and INTM bits, and the STP bit are set to 1 at the same time, the setting of NMI2M, NMI0M, and INTM bits becomes invalid. If there is an unmasked interrupt request being held pending when the STOP mode is set, set the bit corresponding to the interrupt (NMI2M, NMI0M, or INTM) to 1, and then set the STP bit to 1.

(2) Power save mode register (PSMR)

This is an 8-bit register that controls the operation status in the power save mode and the clock operation.

This register can be read or written in 8-bit or 1-bit units.

After reset, this register is cleared to 00H.

After reset: 00H R/W After reset: FFFFF820H

	7	6	5	4	3	2	1	<0>
PSMR	0	0	0	0	0	0	0	PSM

PSM	Specification of operation in software standby mode
0	IDLE mode
1	STOP mode

Cautions 1. Be sure to clear bits 1 to 7 of the PSMR register to 0.

2. The PSM bit is valid only when the STP bit of the PSC register is 1.

(3) Oscillation stabilization time selection register (OSTS)

The wait time until the oscillation stabilizes after the STOP mode is released is controlled by the oscillation stabilization time register (OSTS).

The OSTS register is set by an 8-bit memory manipulation instruction.

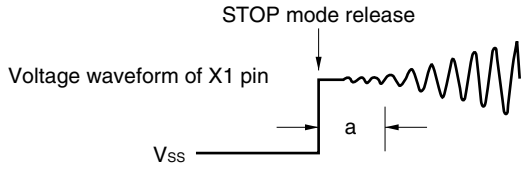
After reset, OSTS is cleared to 01H.

After reset: 01H R/W Address: FFFFF6C0H

	7	6	5	4	3	2	1	0
OSTS	0	0	0	0	0	OSTS2	OSTS1	OSTS0

OSTS2	OSTS1	OSTS0	Selection of oscillation stabilization time			
				fx		
				4 MHz	5 MHz	10 MHz
0	0	0	$2^{13}/f_x$	2.048 ms	1.638 ms	0.819 ms
0	0	1	$2^{15}/f_x$	8.192 ms	6.554 ms	3.277 ms
0	1	0	$2^{16}/f_x$	16.38 ms	13.11 ms	6.554 ms
0	1	1	$2^{17}/f_x$	32.77 ms	26.21 ms	13.11 ms
1	0	0	$2^{18}/f_x$	65.54 ms	52.43 ms	26.21 ms
1	0	1	$2^{19}/f_x$	131.1 ms	104.9 ms	52.43 ms
1	1	0	$2^{20}/f_x$	262.1 ms	209.7 ms	104.9 ms
1	1	1	$2^{21}/f_x$	524.3 ms	419.4 ms	209.7 ms

Cautions 1. The wait time following release of the STOP mode does not include the time until the clock oscillation starts ("a" in the figure below) following release of the STOP mode, regardless of whether the STOP mode is released through $\overline{\text{RESET}}$ input or the occurrence of an interrupt request signal.



2. Be sure to set bits 3 to 7 to 0.

3. The oscillation stabilization time following reset release is $2^{15}/f_x$ (because the initial value of the OSTS register = 01H).

4. The oscillation stabilization time is also inserted during external clock input.

Remark fx = Oscillation frequency

21.3 HALT Mode

21.3.1 Setting and operation status

The HALT mode is set when a dedicated instruction (HALT) is executed in the normal operation mode.

In the HALT mode, the clock oscillator continues operating. Only clock supply to the CPU is stopped; clock supply to the other on-chip peripheral functions continues.

As a result, program execution is stopped, and the internal RAM retains the contents before the HALT mode was set. The on-chip peripheral functions that are independent of instruction processing by the CPU continue operating.

Table 21-3 shows the operation status in the HALT mode.

The average power consumption of the system can be reduced by using the HALT mode in combination with the normal operation mode for intermittent operation.

Cautions 1. Insert five or more NOP instructions after the HALT instruction.

2. If the HALT instruction is executed with an interrupt request signal held pending, the system shift to the HALT mode, but the HALT mode is immediately released by the pending interrupt request.

21.3.2 Releasing HALT mode

The HALT mode is released by a non-maskable interrupt request, an unmasked maskable interrupt request, and $\overline{\text{RESET}}$ pin input.

After the HALT mode has been released, the normal operation mode is restored.

(1) Releasing HALT mode by non-maskable interrupt request or unmasked maskable interrupt request

The HALT mode is released by a non-maskable interrupt request or an unmasked maskable interrupt request, regardless of the priority of the interrupt request. If the HALT mode is set in an interrupt servicing routine, however, an interrupt request that is issued later is serviced as follows.

(a) If an interrupt request with a priority lower than that of the interrupt request currently being serviced is issued, only the HALT mode is released, and that interrupt request is not acknowledged. The interrupt request itself is retained.

(b) If an interrupt request with a priority higher than that of the interrupt request currently being serviced is issued (including a non-maskable interrupt request), the HALT mode is released and that interrupt request is acknowledged.

Table 21-2. Operation After Releasing HALT Mode by Interrupt Request

Release Source	Interrupt Enabled (EI) Status	Interrupt Disabled (DI) Status
Non-maskable interrupt request	Execution branches to the handler address	
Maskable interrupt request	Execution branches to the handler address or the next instruction is executed	The next instruction is executed

(2) Releasing HALT mode by $\overline{\text{RESET}}$ pin input

The same operation as the normal reset operation is performed.

Table 21-3. Operation Status in HALT Mode

Setting of HALT Mode / Item		When CPU Is Operating with Main Clock	
		When Subclock Is Not Used	When Subclock Is Used
CPU		Stops operation	
ROM correction		Stops operation	
Main clock oscillator		Oscillation enabled	
Subclock oscillator		–	Oscillation enabled
Interrupt controller		Operable	
16-bit timers (TM00 to TM05)		Operable	
8-bit timers (TM50, TM51)		Operable	
Timer H (TMH0, TMH1)		Operable	
Watch timer		Operable when main clock output is selected as count clock	Operable
Watchdog timer 1		Operable	
Watchdog timer 2		Operable when main clock is selected as count clock	Operable
Serial interface	CSI00 to CSI02	Operable	
	CSIA0 to CSIA1	Operable	
	I^2C0[Note], I^2C1[Note]	Operable	
	UART0 to UART2	Operable	
Key interrupt function		Operable	
A/D converter		Operable	
D/A converter		Operable only when real-time output mode is selected	
Real-time output		Operable	
Port function		Retains status before HALT mode was set.	
External bus interface		Refer to **CHAPTER 5 BUS CONTROL FUNCTION**.	
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the HALT mode was set.	

Note Only products with I^2C

21.4 IDLE Mode

21.4.1 Setting and operation status

The IDLE mode is set by clearing the PSM bit of the power save mode register (PSMR) to 0 and setting the STP bit of the power save control register (PSC) to 1 in the normal operation mode.

In the IDLE mode, the clock oscillator continues operation but clock supply to the CPU and other on-chip peripheral functions stops.

As a result, program execution stops and the contents of the internal RAM before the IDLE mode was set are retained. The CPU and other on-chip peripheral functions stop operating. However, the on-chip peripheral functions that can operate with the subclock or an external clock continue operating.

Table 21-5 shows the operation status in the IDLE mode.

The IDLE mode can reduce the power consumption more than the HALT mode because it stops the operation of the on-chip peripheral functions. The main clock oscillator does not stop, so the normal operation mode can be restored without waiting for the oscillation stabilization time after the IDLE mode has been released, in the same manner as when the HALT mode is released.

Caution Insert five or more NOP instructions after the instruction that stores data in the PSC register to set the IDLE mode.

21.4.2 Releasing IDLE mode

The IDLE mode is released by a non-maskable interrupt request (NMI pin input), unmasked external interrupt request (INTP0 to INTP6 pin input), unmasked internal interrupt request from the peripheral functions operable in the IDLE mode, or $\overline{\text{RESET}}$ input.

After the IDLE mode has been released, the normal operation mode is restored.

(1) Releasing IDLE mode by non-maskable interrupt request or unmasked maskable interrupt request

The IDLE mode is released by a non-maskable interrupt request or an unmasked maskable interrupt request, regardless of the priority of the interrupt request. If the IDLE mode is set in an interrupt servicing routine, however, an interrupt request that is issued later is processed as follows.

(a) If an interrupt request with a priority lower than that of the interrupt request currently being serviced is issued, only the IDLE mode is released, and that interrupt request is not acknowledged. The interrupt request itself is retained.

(b) If an interrupt request with a priority higher than that of the interrupt request currently being serviced is issued (including a non-maskable interrupt request), the IDLE mode is released and that interrupt request is acknowledged.

Table 21-4. Operation After Releasing IDLE Mode by Interrupt Request

Release Source	Interrupt Enabled (EI) Status	Interrupt Disabled (DI) Status
Non-maskable interrupt request	Execution branches to the handler address	
Maskable interrupt request	Execution branches to the handler address or the next instruction is executed	The next instruction is executed

(2) Releasing IDLE mode by $\overline{\text{RESET}}$ pin input

The same operation as the normal reset operation is performed.

Table 21-5. Operation Status in IDLE Mode

Setting of IDLE Mode / Item		When CPU Is Operating with Main Clock	
		When Subclock Is Not Used	When Subclock Is Used
CPU		Stops operation	
ROM correction		Stops operation	
Main clock oscillator		Oscillation enabled	
Subclock oscillator		–	Oscillation enabled
Interrupt controller		Stops operation	
16-bit timers (TM00 to TM05)		TM00, TM02 to TM05: Stop operation TM01: Operable when INTWT is selected as count clock and f_{BRG} is selected as count clock of WT	TM00, TM02 to TM05: Stop operation TM01: Operable when INTWT is selected as count clock
8-bit timers (TM50, TM51)		• Operable when TI5m is selected as count clock • Operable when INTTM010 is selected as count clock and TM01 is enabled in IDLE mode	
Timer H (TMH0)		Stops operation	
Timer H (TMH1)		Stops operation	Operable when f_{XT} is selected as count clock
Watch timer		Operable when main clock output is selected as count clock	Operable
Watchdog timer 1		Stops operation	
Watchdog timer 2		Stops operation	Operable when f_{XT} is selected as count clock
Serial interface	CSI00 to CSI02	Operable when $\overline{\text{SCK0n}}$ input clock is selected as operation clock	
	CSIA0, CSIA1	Stops operation	
	I^2C0[Note 1], I^2C1[Note 1]	Stops operation	
	UART0	Operable when ASCK0 is selected as count clock	
	UART0, UART2	Stops operation	
Key interrupt function		Operable	
A/D converter		Stops operation	
D/A converter		Stops operation (retains output)[Note 2]	ch0: Stops operation (retains output)[Note 2] ch1: (For other conditions than following, refer to Note.) Operable only when real-time output mode is selected and subclock (f_{XT}) is selected as count clock of TMH1
Real-time output		Operable only when INTTM5m is selected as real-time output trigger and TM5m is enabled in IDLE mode	
Port function		Retains status before IDLE mode was set.	
External bus interface		Refer to **CHAPTER 5 BUS CONTROL FUNCTION**.	
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the IDLE mode was set.	

Notes 1. Only products with I^2C

2. If the IDLE mode is set immediately after D/A conversion has started (during conversion), the D/A converter continues operating until D/A conversion is complete and retains the output at the end of D/A conversion.

Remark m = 0 or 1
n = 0 to 2

21.5 STOP Mode

21.5.1 Setting and operation status

The STOP mode is set when the PSM bit of the power save mode register (PSMR) is set to 1 and the STP bit of the power save control register (PSC) is set to 1 in the normal operation mode.

In the STOP mode, the subclock oscillator continues operating but the main clock oscillator stops. Clock supply to the CPU and the on-chip peripheral functions is stopped.

As a result, program execution is stopped, and the contents of the internal RAM before the STOP mode was set are retained. The on-chip peripheral functions that operate with the clock oscillated by the subclock oscillator or an external clock continue operating.

Table 21-7 shows the operation status in the STOP mode.

Because the STOP stops operation of the main clock oscillator, it reduces the power consumption to a level lower than the IDLE mode. If the subclock oscillator and external clock are not used, the power consumption can be minimized with only leakage current flowing.

Caution Insert five or more NOP instructions after the instruction that stores data in the PSC register to set the STOP mode.

21.5.2 Releasing STOP mode

The STOP mode is released by a non-maskable interrupt request (NMI pin input), unmasked external interrupt request (INTP0 to INTP6 pin input), unmasked internal interrupt request from the peripheral functions operable in the STOP mode, or $\overline{\text{RESET}}$ pin input.

After the STOP mode has been released, the normal operation mode is restored after the oscillation stabilization time has been secured.

(1) Releasing STOP mode by non-maskable interrupt request or unmasked maskable interrupt request

The STOP mode is released by a non-maskable interrupt request or an unmasked maskable interrupt request, regardless of the priority of the interrupt request. If the software STOP mode is set in an interrupt servicing routine, however, an interrupt request that is issued later is serviced as follows.

(a) If an interrupt request with a priority lower than that of the interrupt request currently being serviced is issued, only the STOP mode is released, and that interrupt request is not acknowledged. The interrupt request itself is retained.

(b) If an interrupt request with a priority higher than that of the interrupt request currently being serviced is issued (including a non-maskable interrupt request), the STOP mode is released and that interrupt request is acknowledged.

Table 21-6. Operation After Releasing STOP Mode by Interrupt Request

Release Source	Interrupt Enabled (EI) Status	Interrupt Disabled (DI) Status
Non-maskable interrupt request	Execution branches to the handler address	
Maskable interrupt request	Execution branches to the handler address or the next instruction is executed	The next instruction is executed

(2) Releasing STOP mode by $\overline{\text{RESET}}$ pin input

The same operation as the normal reset operation is performed.

Table 21-7. Operation Status in STOP Mode

Item \ Setting of STOP Mode		When CPU Is Operating with Main Clock	
		When Subclock Is Not Used	When Subclock Is Used
CPU		Stops operation	
ROM correction		Stops operation	
Main clock oscillator		Oscillation stops	
Subclock oscillator		–	Oscillation enabled
Interrupt controller		Stops operation	
16-bit timers (TM00 to TM05)		Stop operation	TM00, TM02 to TM05: Stop operation TM01: Operable when INTWT is selected as count clock and subclock (f_{XT}) is selected as count clock of WT
8-bit timers (TM50, TM51)		Operable when TI5m is selected as count clock	Operable when TI5m is selected as count clock or when INTTM010 is selected as count clock and TM01 is enabled in STOP mode
Timer H (TMH0)		Stops operation	
Timer H (TMH1)		Stops operation	Operable when f_{XT} is selected as count clock
Watch timer		Stops operation	Operable when f_{XT} is selected as count clock
Watchdog timer 1		Stops operation	
Watchdog timer 2		Stops operation	Operable when f_{XT} is selected as count clock
Serial interface	CSI00 to CSI02	Operable when $\overline{\text{SCK0n}}$ input clock is selected as operation clock	
	CSIA0, CSIA1	Stops operation	
	I^2C0[Note 1], I^2C1[Note 1]	Stops operation	
	UART0	Operable when ASCK0 is selected as count clock	
	UART1, UART2	Stops operation	
Key interrupt function		Operable	
A/D converter		Stops operation	
D/A converter		Stops operation (retains output)[Note 2]	ch0: Stops operation (retains output)[Note 2] ch1: (For conditions other than the following, refer to Note.) Operable only when real-time output mode is selected and subclock (f_{XT}) is selected as count clock of TMH1
Real-time output		Operable when INTTM5m is selected as real-time output trigger and TM5 is enabled in STOP mode	
Port function		Retains status before STOP mode was set.	
External bus interface		Refer to **CHAPTER 5 BUS CONTROL FUNCTION**.	
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the STOP mode was set.	

Notes 1. Only products with I^2C

2. If the STOP mode is set immediately after D/A conversion has started (during conversion), the D/A converter continues operating until D/A conversion is complete, and retains the output at the end of D/A conversion.

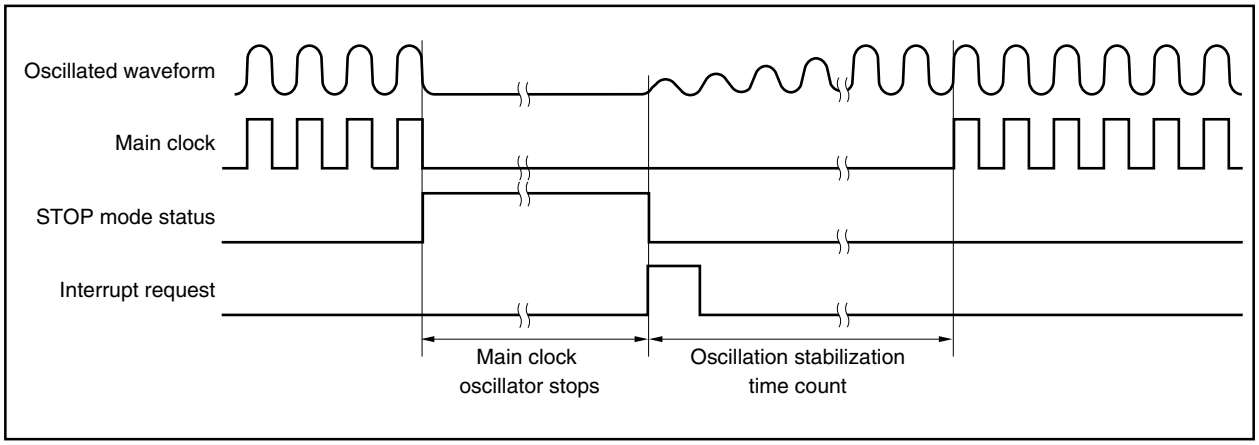
Remark m = 0 or 1
n = 0 to 2

21.6 Securing Oscillation Stabilization Time

When the STOP mode is released, only the oscillation stabilization time set by the oscillation stabilization time selection register (OSTS) elapses. If the software STOP mode has been released by $\overline{\text{RESET}}$ pin input, however, the reset value of the OSTS register, $2^{15}/f_X$ (8.192 ms at f_X = 4 kHz) elapses.

Figure 21-2 shows the operation performed when the STOP mode is released by an interrupt request.

Figure 21-2. Oscillation Stabilization Time



Caution For details of the OSTS register, refer to 21.2 (4) Oscillation stabilization time selection register (OSTS).

21.7 Subclock Operation Mode

21.7.1 Setting and operation status

The subclock operation mode is set when the CK3 bit of the processor clock control register (PCC) is set to 1 in the normal operation mode.

When the subclock operation mode is set, the internal system clock is changed from the main clock to the subclock.

When the MCK bit of the PCC register is set to 1, the operation of the main clock oscillator is stopped. As a result, the system operates only with the subclock.

Table 21-8 shows the operation status in power operation mode.

In the subclock operation mode, the power consumption can be reduced to a level lower than in the normal operation mode because the subclock is used as the internal system clock. In addition, the power consumption can be further reduced to the level of the STOP mode by stopping the operation of the main system clock oscillator.

Cautions 1. When manipulating the CK3 bit of the PCC register, do not change the set values of the CK2 to CK0 bits (using a bit manipulation instruction to manipulate the bit is recommended). For details, refer to 6.3 (1) Processor clock control register (PCC).

2. If the following conditions are not satisfied, change the CK2 to CK0 bits so that the conditions are satisfied and set the subclock operation mode.

Main clock (f_{XX}) > Subclock (f_{XT}: 32.768 kHz) × 4

21.7.2 Releasing subclock operation mode

The subclock operation mode is released when the CK3 bit of the PCC register is cleared to 0 or by $\overline{\text{RESET}}$ pin input. If the main clock is stopped (MCK bit of PCC register = 1), set the MCK bit of the PCC register to 1, secure the oscillation stabilization time of the main clock by software, and clear the CK3 bit of the PCC register to 0.

The normal operation mode is restored when the subclock operation mode is released.

Caution When manipulating the CK3 bit of the PCC register, do not change the set values of the CK2 to CK0 bits (using a bit manipulation instruction to manipulate the bit is recommended). For details, refer to 6.3 (1) Processor clock control register (PCC).

Table 21-8. Operation Status in Subclock Operation Mode

Item \ Setting of Subclock Operation Mode		Operation Status	
		When Main Clock Is Oscillating	When Main Clock Is Stopped
CPU		Operable	
ROM correction		Operable	
Subclock oscillator		Oscillation enabled	
Interrupt controller		Operable	
16-bit timers (TM00 to TM05)		Operable	TM00, TM02 to TM05: Stop operation TM01: Operable only under the following conditions • INTWT is selected as count clock and subclock (f_{XT}) is selected as count clock of WT
8-bit timers (TM50, TM51)		Operable	• Operable when TI5m is selected as count clock • Operable when INTTM010 is selected as count clock, INTWT is selected as count clock of TM01, and subclock (f_{XT}) is selected as count clock of WT
Timer H (TMH0)		Operable	Stops operation
Timer H (TMH1)		Operable	Operable when f_{XT} is selected as count clock
Watch timer		Operable	Operable when f_{XT} is selected as count clock
Watchdog timer 1		Operable	Stops operation
Watchdog timer 2		Operable	Operable when f_{XT} is selected as count clock
Serial interface	CSI00 to CSI02	Operable	Operable when $\overline{SCK0n}$ input clock is selected as operation clock
	CSIA0, CSIA1	Operable	Stops operation
	I^2C0[Note], I^2C1[Note]	Operable	Stops operation
	UART0	Operable	Operable when ASCK0 is selected as count clock
	UART1, UART2	Operable	Stops operation
Key interrupt function		Operable	
A/D converter		Operable	Stops operation
D/A converter		Operable	ch0: Operable only when normal mode is selected ch1: Operable under the following conditions • When normal mode is selected • When real-time output mode is selected and subclock (f_{XT}) is selected as count clock of TMH1
Real-time output		Operable	• INTTM5m is selected as real-time output trigger and TI5m is selected as count clock of TM5m • Operable when INTTM010 is selected, INTWT is selected as count clock of T01, and subclock (f_{XT}) is selected as count clock of WT
Port function		Settable	
External bus interface		Operable	
Internal data		Settable	

Note Only products with I^2C

Remark m = 0 or 1
n = 0 to 2

21.8 Sub-IDLE Mode

21.8.1 Setting and operation status

The sub-IDLE mode is set when the PSM bit of the power save mode register (PSMR) is cleared to 0 and the STP bit of the power save control register (PSC) is set to 1 in the subclock operation mode.

In this mode, the clock oscillator continues operation but clock supply to the CPU and the other on-chip peripheral functions is stopped.

As a result, program execution is stopped and the contents of the internal RAM before the sub-IDLE mode was set are retained. The CPU and the other on-chip peripheral functions are stopped. However, the on-chip peripheral functions that can operate with the subclock or an external clock continue operating.

Table 21-10 shows the operation status in the sub-IDLE mode.

Because the sub-IDLE mode stops operation of the CPU and other on-chip peripheral functions, it can reduce the power consumption more than the subclock operation mode. If the sub-IDLE mode is set after the main clock has been stopped, the power consumption can be reduced to a level as low as that in the STOP mode.

21.8.2 Releasing sub-IDLE mode

The sub-IDLE mode is released by a non-maskable interrupt request (NMI pin input), unmasked external interrupt request (INTP0 to INTP6 pin input), unmasked internal interrupt request from the peripheral functions operable in the sub-IDLE mode, or $\overline{\text{RESET}}$ pin input.

When the sub-IDLE mode is released by an interrupt request, the subclock operation mode is set. If it is released by $\overline{\text{RESET}}$ pin input, the normal operation mode is restored.

(1) Releasing sub-IDLE mode by non-maskable interrupt request or unmasked maskable interrupt request

The sub-IDLE mode is released by a non-maskable interrupt request or an unmasked maskable interrupt request, regardless of the priority of the interrupt request. If the sub-IDLE mode is set in an interrupt servicing routine, however, an interrupt request that is issued later is serviced as follows.

(a) If an interrupt request with a priority lower than that of the interrupt request currently being serviced is issued, only the sub-IDLE mode is released, and that interrupt request is not acknowledged. The interrupt request itself is retained.

(b) If an interrupt request with a priority higher than that of the interrupt request currently being serviced is issued (including a non-maskable interrupt request), the sub-IDLE mode is released and that interrupt request is acknowledged.

Table 21-9. Operation After Releasing Sub-IDLE Mode by Interrupt Request

Release Source	Interrupt Enabled (EI) Status	Interrupt Disabled (DI) Status
Non-maskable interrupt request	Execution branches to the handler address	
Maskable interrupt request	Execution branches to the handler address or the next instruction is executed	The next instruction is executed

(2) Releasing sub-IDLE mode by $\overline{\text{RESET}}$ pin input

The same operation as the normal reset operation is performed.

Table 21-10. Operation Status in Sub-IDLE Mode

Item \ Setting of Sub-IDLE Mode		Operation Status	
		When Main Clock Is Oscillating	When Main Clock Is Stopped
CPU		Stops operation	
ROM correction		Stops operation	
Subclock oscillator		Oscillation enabled	
Interrupt controller		Stops operation	
16-bit timers (TM00 to TM05)		TM00, TM02 to TM05: Stop operation TM01: Operable when INTWT is selected as count clock	TM00, TM02 to TM05: Stop operation TM01: Operable when INTWT is selected as count clock and subclock (f_{XT}) is selected as count clock of WT
8-bit timers (TM50, TM51)		• Operable when TI5m is selected as count clock • Operable when INTTM010 is selected as count clock and INTWT is selected as count clock of TM01	• Operable when TI5m is selected as count clock • Operable when INTTM010 is selected as count clock, INTWT is selected as count clock of TM01, and subclock (f_{XT}) is selected as count clock of WT
Timer H (TMH0)		Stops operation	
Timer H (TMH1)		Operable when f_{XT} is selected as count clock	
Watch timer		Stops operation	Operable when f_{XT} is selected as count clock
Watchdog timer 1		Operable	Stops operation
Watchdog timer 2		Operable when f_{XT} is selected as count clock	
Serial interface	CSI00 to CSI02	Stops operation	Operable when $\overline{SCK0n}$ input clock is selected as operation clock
	CSIA0, CSIA1	Stops operation	
	I^2C0[Note], I^2C1[Note]	Stops operation	
	UART0	Operable when ASCK0 is selected as count clock	
	UART1, UART2	Stops operation	
Key interrupt function		Operable	
A/D converter		Stops operation	
D/A converter		ch0: Stops operation (retains output)[Note 2] ch1: (For other than the following conditions, refer to Note.) Operable when real-time output mode is selected and subclock (f_{XT}) is selected as count clock of TMH1.	
Real-time output		• Operable when ITNTM5m is selected as real-time output trigger and TI5m is selected as count clock of TM5m • Operable when INTTM010 is selected, and INTWT is selected as count clock of TM01	• Operable when INTTM5m is selected as real-time output trigger and TI5m is selected as count clock of TM5 • Operable when INTTM010 is selected, INTWT is selected as count clock of TM01, and subclock (f_{XT}) is selected as count clock of WT
Port function		Retains status before sub-IDLE mode was set.	
External bus interface		Refer to **CHAPTER 5 BUS CONTROL FUNCTION**.	
Internal data		The CPU registers, statuses, data, and all other internal data such as the contents of the internal RAM are retained as they were before the sub-IDLE mode was set.	

Notes 1. Only products with I^2C

2. If the sub-IDLE mode is set immediately after D/A conversion has started (during conversion), the D/A converter continues operating until D/A conversion is complete and retains the output at the end of D/A conversion.

Remark m = 0 or 1
n = 0 to 2

CHAPTER 22 RESET FUNCTION

22.1 Overview

The following reset functions are available.

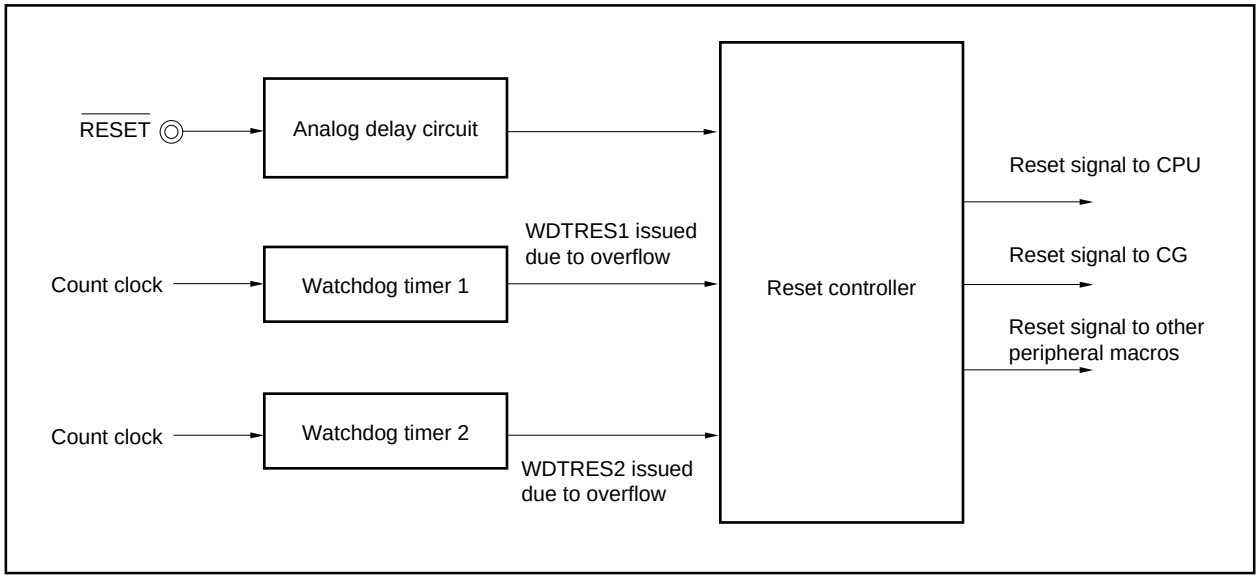
- Reset function by $\overline{\text{RESET}}$ pin input
- Reset function by overflow of watchdog timer 1 (WDTRES1)
- Reset function by overflow of watchdog timer 2 (WDTRES2)

If the $\overline{\text{RESET}}$ pin goes high, the reset status is released, and the CPU starts executing the program. Initialize the contents of each register in the program as necessary.

The $\overline{\text{RESET}}$ pin has a noise eliminator that operates by analog delay to prevent malfunction caused by noise.

22.2 Configuration

Figure 22-1. Reset Block Diagram



22.3 Operation

The system is reset, initializing each hardware unit, when a low level is input to the $\overline{\text{RESET}}$ pin or if watchdog timer 1 or watchdog timer 2 overflows (WDTRES1 or WDTRES2).

While a low level is being input to the $\overline{\text{RESET}}$ pin, the main clock oscillator stops. Therefore, the overall power consumption of the system can be reduced.

If the $\overline{\text{RESET}}$ pin goes high or if WDTRES1 or WDTRES2 is received, the reset status is released.

If the reset status is released by $\overline{\text{RESET}}$ pin input or WDTRES2, the oscillation stabilization time elapses (reset value of OSTS register: 2^{15}/fxx) and then the CPU starts program execution.

If the reset status is released by WDTRES1, the oscillation stabilization time is not inserted because the main system clock oscillator does not stop.

Table 22-1. Hardware Status on $\overline{\text{RESET}}$ Pin Input or Occurrence of WDTRES2

Item	During Reset	After Reset
Main clock oscillator (f_X)	Oscillation stops (f_X = 0 level).	Oscillation starts
Subclock oscillator (f_{XT})	Oscillation can continue without effect from reset[Note 1].	
Peripheral clock (f_{XX} to f_{XX}/1024), internal system clock (f_{CLK}), CPU clock (f_{CPU})	Operation stops	Operation starts. However, operation stops during oscillation stabilization time count.
Watchdog timer 1 clock (f_{XW})	Operation stops	Operation starts[Note 2]
Internal RAM	Undefined if power-on reset occurs or writing data to RAM and reset conflict (data loss); otherwise, retains values immediately before reset input.	
I/O lines (ports)	High impedance	
On-chip peripheral I/O registers	Initialized to specified status	
Other on-chip peripheral functions	Operation stops	Operation can be started

Notes 1. The on-chip feedback resistor is “connected” by default (refer to **6.3 (1) Processor clock control register (PCC)**).

2. The clock is in the initialized status (interval timer mode).

Table 22-2. Hardware Status on Occurrence of WDTRES1

Item	During Reset	After Reset
Main clock oscillator (f_X)	Oscillation continues[Note]	
Subclock oscillator (f_{XT})	Oscillation can continue without effect from reset[Note].	
Peripheral clock (f_{XX} to f_{XX}/1024), internal system clock (f_{CLK}), CPU clock (f_{CPU})	Operation stops	Operation starts
Watchdog timer 1 clock (f_{XW})	Operation continues	
Internal RAM	Undefined if writing data to RAM and reset conflict (data loss); otherwise, retains values immediately before reset input.	
I/O lines (ports)	High impedance	
On-chip peripheral I/O registers	Initialized to specified status	
Other on-chip peripheral functions	Operation stops	Operation can be started

Note The on-chip feedback resistor is "connected" by default (refer to **6.3 (1) Processor clock control register (PCC)**).

Figure 22-2. Hardware Status on $\overline{\text{RESET}}$ Input

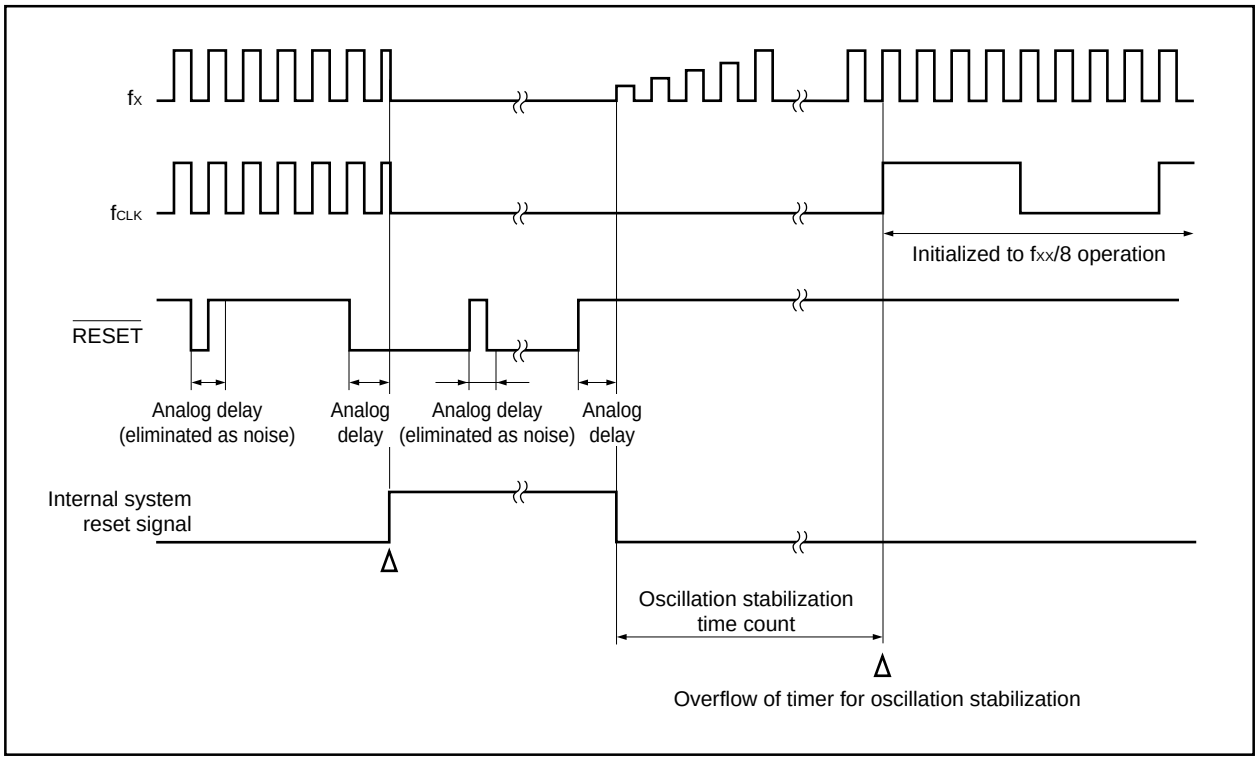
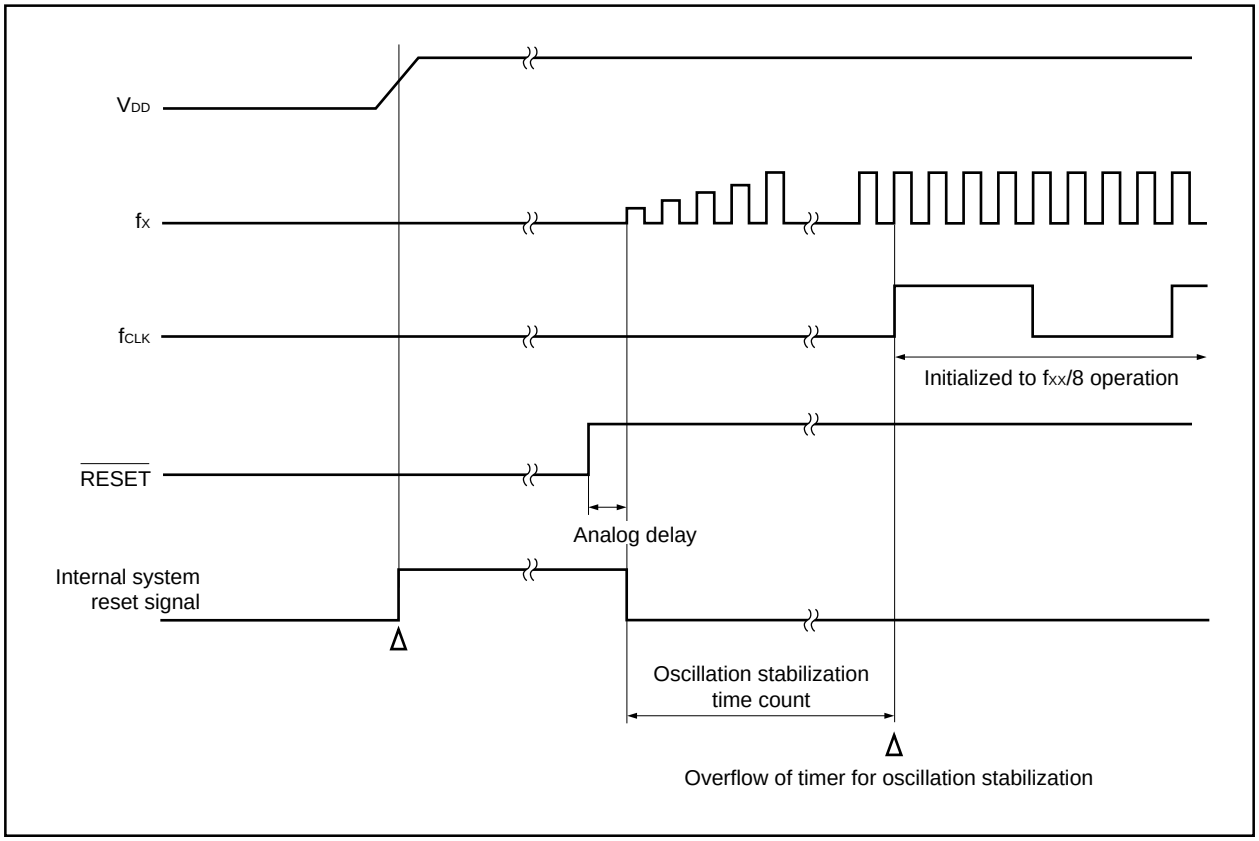


Figure 22-3. Operation on Power Application



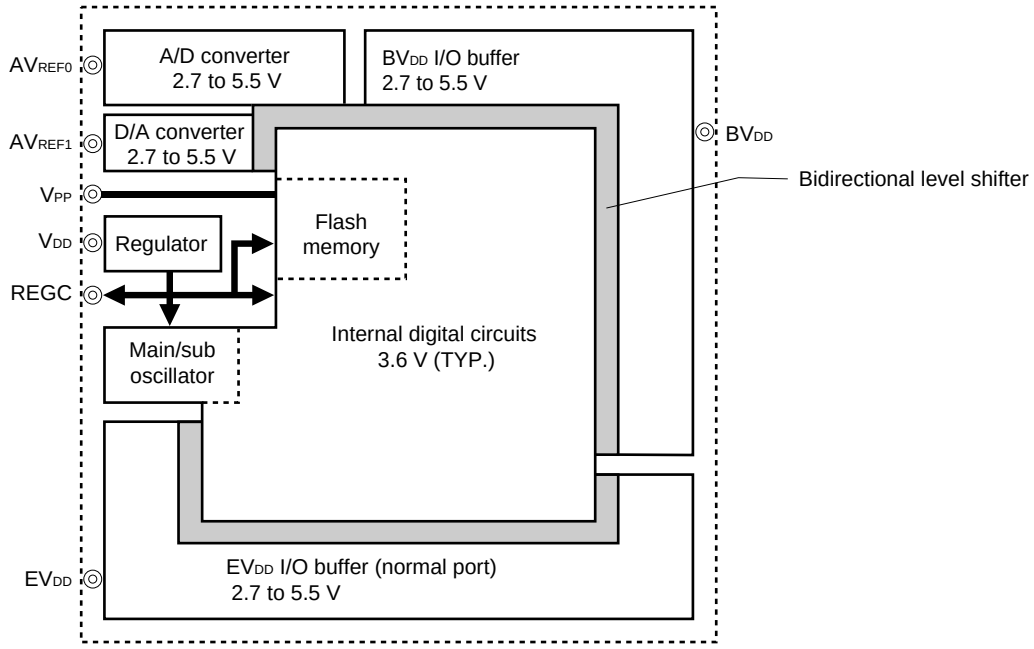
CHAPTER 23 REGULATOR

23.1 Overview

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 include a regulator to reduce the power consumption and noise.

This regulator supplies a stepped-down V_{DD} power supply voltage to the oscillator block and internal logic circuits (except the A/D converter, D/A converter, and output buffer). The regulator output voltage is set to 3.6 V (TYP.).

★ **Figure 23-1. Regulator**



Caution Use the regulator with a setting of $V_{DD} = EV_{DD} = AV_{REF0} = AV_{REF1} \geq BV_{DD}$.

23.2 Operation

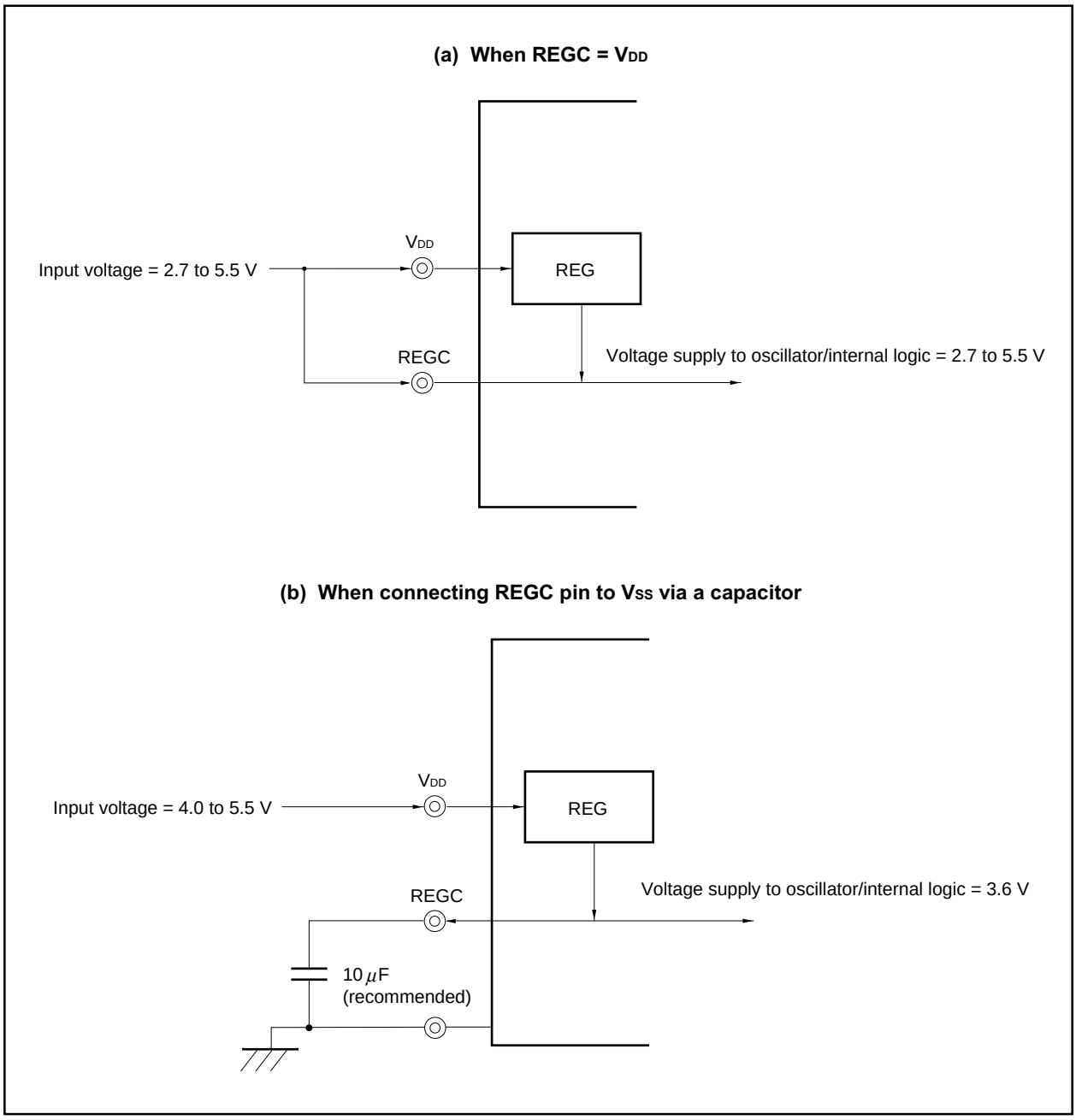
The regulator stops operating in the following modes (but only when REGC = V_{DD}).

- During $\overline{\text{RESET}}$ input
- In STOP mode
- In sub-IDLE mode

Be sure to connect a capacitor (10 μF) to the REGC pin to stabilize the regulator output.

A diagram of the regulator pin connections is shown below.

Figure 23-2. REGC Pin Connection



CHAPTER 24 ROM CORRECTION FUNCTION

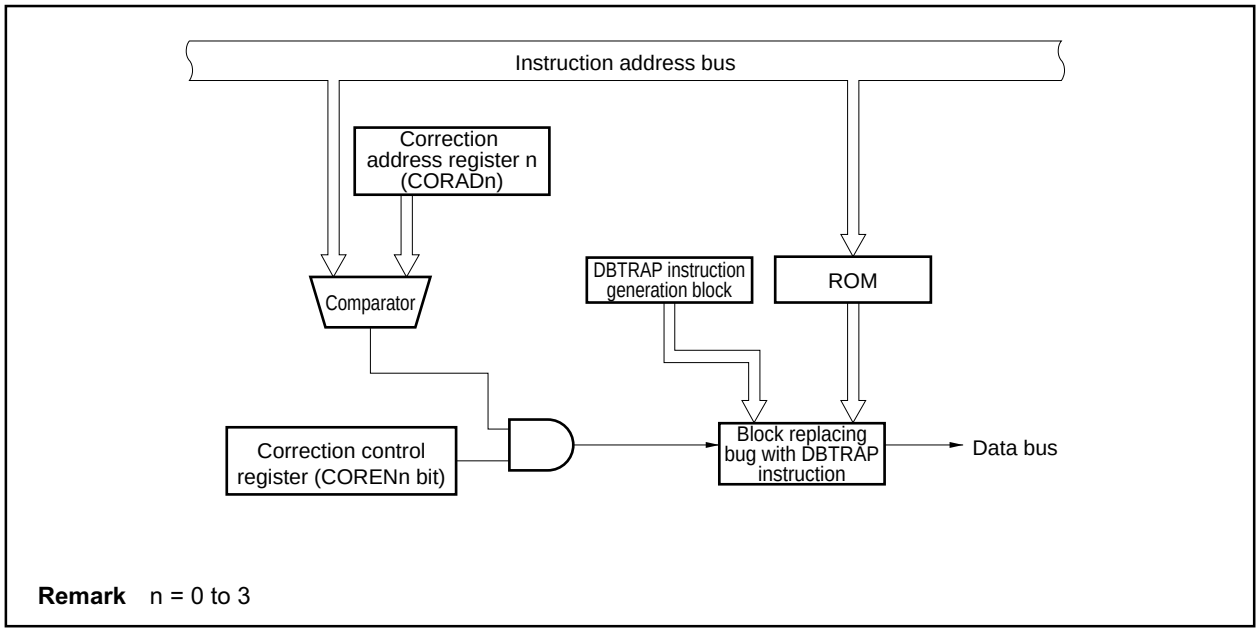
24.1 Overview

The ROM correction function is used to replace part of the program in the mask ROM with the program of an external memory or the internal RAM.

By using this function, program bugs found in the mask ROM can be corrected.

Up to four address can be specified for correction.

Figure 24-1. Block Diagram of ROM Correction



Remark n = 0 to 3

24.2 Control Registers

24.2.1 Correction address registers 0 to 3 (CORAD0 to CORAD3)

These registers are used to set the first address of the program to be corrected.

The program can be corrected at up to four places because four correction address register n (CORADn) are provided (n = 0 to 3).

The CORADn register can only be read or written in 32-bit units.

If the higher 16 bits of the CORADn register are used as the CORADnH register, and the lower 16 bits as the CORADnL register, these registers can be read or written in 16-bit units.

Because the ROM capacity differs depending on the product, set correction addresses in the following ranges.

μPD703208, 703208Y, 7030212, 703212Y (64 KB): 0000000H to 000FFFEH
μPD703209, 703209Y, 703213, 703213Y, 703216, 703216Y (96 KB): 0000000H to 0017FFEH
μPD703210, 703210Y, 703214, 703214Y, 703217, 703217Y (128 KB): 0000000H to 001FFFEH

Fix bits 0 and 17 to 31 to 0.

After reset: 00000000H R/W Address: Refer to Table 24-1.

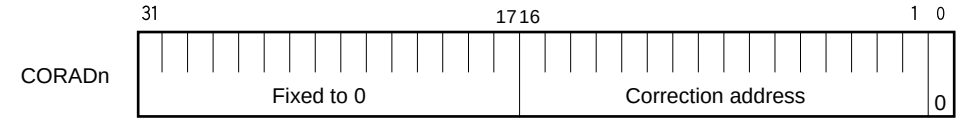


Table 24-1. Address of CORADn

FFFFF840H		CORAD0	FFFFF848H		CORAD2
	FFFFF840H	CORAD0L		FFFFF848H	CORAD2L
	FFFFF842H	CORAD0H		FFFFF84AH	CORAD2H
FFFFF844H		CORAD1	FFFFF84CH		CORAD3
	FFFFF844H	CORAD1L		FFFFF84CH	CORAD3L
	FFFFF846H	CORAD1H		FFFFF84EH	CORAD3H

24.2.2 Correction control register (CORCN)

This register disables or enables the correction operation at the address specified by correction address register n (CORADn) (n = 0 to 3).

Each channel can be enabled or disabled by this register.

This register is set by using an 8-bit or 1-bit memory manipulation instruction.

After reset: 00H R/W Address: FFFFF880H

	7	6	5	4	3	2	1	0
CORCN	0	0	0	0	COREN3	COREN2	COREN1	COREN0

CORENn	Correction operation enable/disable
0	Disabled
1	Enabled

Remark n = 0 to 3

Table 24-2. Correspondence Between CORCN Register Bits and CORADn Registers

CORCN Register Bit	Corresponding CORADn Register
COREN3	CORAD3
COREN2	CORAD2
COREN1	CORAD1
COREN0	CORAD0

24.3 ROM Correction Operation and Program Flow

<1> If the address to be corrected and the fetch address of the internal ROM match, the fetch code is replaced by the DBTRAP instruction.

<2> When the DBTRAP instruction is executed, execution branches to address 00000060H.

<3> Software processing after branching causes the result of ROM correction to be judged (the fetch address and ROM correction operation are confirmed) and execution to branch to the correction software.

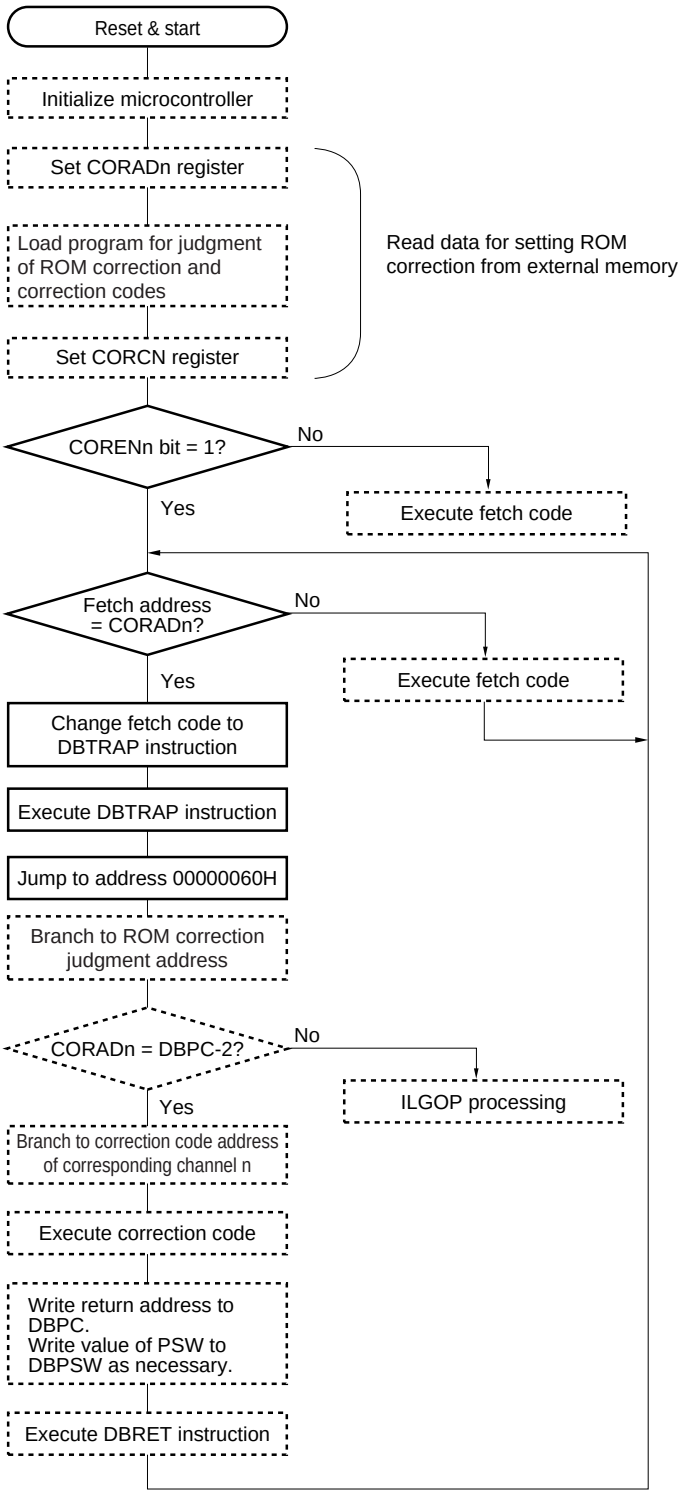
<4> After the correction software has been executed, the return address is set, and return processing is started by the DBRET instruction.

Cautions 1. The software that performs <3> and <4> must be executed in the internal ROM/RAM.

2. When setting an address to be corrected to the CORADn register, clear the higher bits to 0 in accordance with the capacity of the internal ROM.

3. The ROM correction function cannot be used to correct the data of the internal ROM. It can only be used to correct instruction codes. If ROM correction is used to correct data, that data is replaced with the DBTRAP instruction code.

★ **Figure 24-2. ROM Correction Operation and Program Flow**



Remarks 1. ⬚ : Processing by user program (software)

▭ : Processing by ROM correction (hardware)

2. n = 0 to 3

CHAPTER 25 FLASH MEMORY

The following products are the on-chip flash memory versions of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1.

(1) V850ES/KF1
μPD70F3210, 70F3210Y: Products with 128 KB flash memory

(2) V850ES/KG1
μPD70F3214, 70F3214Y: Products with 128 KB flash memory

(3) V850ES/KJ1
μPD70F3217, 70F3217Y: Products with 128 KB flash memory

When an instruction is fetched from this flash memory, 4 bytes can be accessed with 1 clock, in the same manner as the mask ROM versions.

Data can be written to the flash memory with the flash memory mounted on the target system (on-board). Connect a dedicated flash programmer to the target system to write the flash memory.

The following are the assumed environments and applications of flash memory.

- Changing software after soldering the V850ES/KF1, V850ES/KG1, or V850ES/KJ1 onto the target system
- Producing many variations of a product in small quantities by changing the software
- Adjusting data when mass production is started

Caution There are differences in noise immunity and noise radiation between the flash memory and mask ROM versions. When pre-producing and application set with the flash memory version and then mass-producing it with the mask ROM version, be sure to conduct sufficient evaluation for the commercial samples (not engineering samples) of the mask ROM version.

25.1 Features

- 4 byte/1 clock access (during instruction fetch access)
- Erasing all areas at once
- Communication with dedicated flash programmer via serial interface
- Erase/write voltage: V_{PP} = 10 V
- On-board programming

25.2 Writing with Flash Programmer

Data can be written to the flash memory on-board or off-board, by using a dedicated flash programmer.

(1) On-board programming

The contents of the flash memory can be rewritten after the V850ES/KF1, V850ES/KG1, or V850ES/KJ1 has been mounted on the target system. The connectors that connect the dedicated flash programmer must be mounted on the target system.

(2) Off-board programming

Data can be written to the flash memory with a dedicated program adapter (FA series) before the V850ES/KF1, V850ES/KG1, or V850ES/KJ1 is mounted on the target system.

Remark The FA series is a product of Naito Densei Machida Mfg. Co., Ltd.

Table 25-1. Wiring Between μPD70F3210 and 70F3210Y (V850ES/KF1), and PG-FP4

Pin Configuration of Flash Programmer (PG-FP4)			Pin Name on FA Board	With CSI00-HS		With CSI00		With UART0	
Signal Name	I/O	Pin Function		Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SI/RxD	Input	Receive signal	SI	P41/SO00	20	P41/SO00	20	P30/TXD0	22
SO/TxD	Output	Transmit signal	SO	P40/SI00	19	P40/SI00	19	P31/RXD0	23
SCK	Output	Transfer clock	SCK	P42/$\overline{SCK00}$	21	P42/$\overline{SCK00}$	21	Not needed	Not needed
CLK	Output	Clock to V850ES/KF1	X1	X1	12	X1	12	X1	12
			X2	X2[Note]	13	X2[Note]	13	X2[Note]	13
/RESET	Output	Reset signal	/RESET	$\overline{RESET}$	14	$\overline{RESET}$	14	$\overline{RESET}$	14
VPP	Output	Write voltage	VPP	V_{PP}	8	V_{PP}	8	V_{PP}	8
HS	Input	Handshake signal for CSI0 + HS communication	RESERVE /HS	PCS1/$\overline{CS1}$	48	Not needed	Not needed	Not needed	Not needed
VDD	I/O	V_{DD} voltage generation/ voltage monitor	VDD	V_{DD}	9	V_{DD}	9	V_{DD}	9
				EV_{DD}	31	EV_{DD}	31	EV_{DD}	31
				AV_{REF0}	1	AV_{REF0}	1	AV_{REF0}	1
GND	–	Ground	GND	V_{SS}	11	V_{SS}	11	V_{SS}	11
				AV_{SS}	2	AV_{SS}	2	AV_{SS}	2
				EV_{SS}	30	EV_{SS}	30	EV_{SS}	30

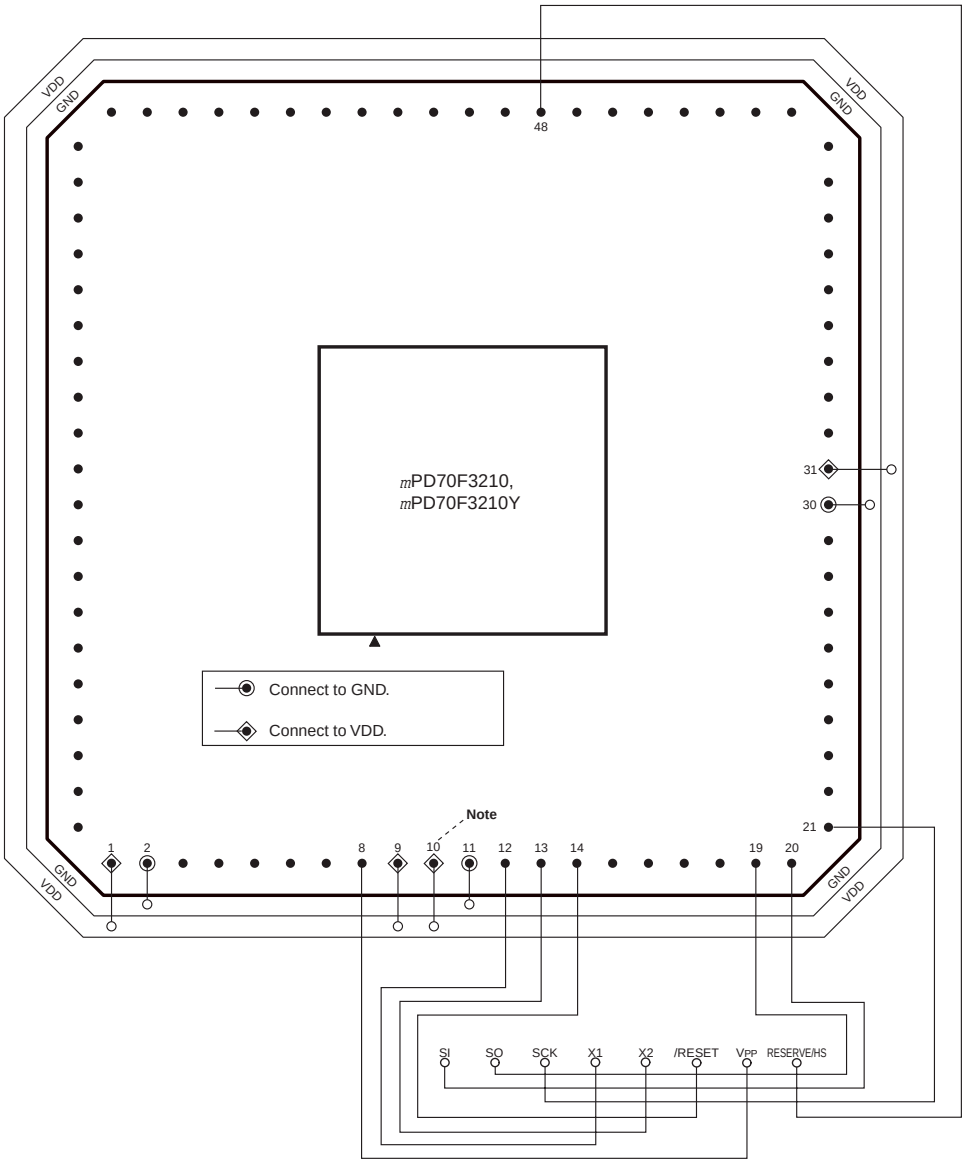
Note When using the clock out of the flash programmer, connect CLK of the programmer to X1, and connect its inverse signal to X2.

Cautions 1. Be sure to connect the REGC pin in either of the following ways.

- **Connect to GND via a 10 μF capacitor**
- **Directly connect to V_{DD}**

2. When connecting the REGC pin to GND via a 10 μF capacitor, the clock cannot be supplied from the CLK pin of the flash programmer.
Supply the clock by creating an oscillator on the board.

Figure 25-1. Wiring Example of V850ES/KF1 Flash Writing Adapter (FA-80GC-8BT, FA-80GK-9EU)



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Note Be sure to connect the REGC pin in either of the following ways.

- Connect to GND via a 10 μF capacitor.
- Directly connect to V_{DD}.

When connecting the REGC pin to GND via a 10 μF capacitor, the clock cannot be supplied from the CLK pin of the flash programmer.

Supply the clock by preparing an oscillator on the board.

Remarks 1. Handle the pins not described above in accordance with the specified handling of unused pins (refer to **2.4 Pin I/O Circuits and Recommended Connection of Unused Pins).**

When connecting to V_{DD} via a resistor, use of a resistor of 1 kΩ to 10 kΩ is recommended.

2. This adapter is for 80-pin plastic QFP and 80-pin plastic TQFP (fine pitch) packages.

3. This diagram shows the wiring when using a handshake-supporting CSI.

Table 25-2. Wiring Between μPD70F3214 and 70F3214Y (V850ES/KG1), and PG-FP4

Pin Configuration of Flash Programmer (PG-FP4)			Pin Name on FA Board	With CSI00-HS		With CSI00		With UART0	
Signal Name	I/O	Pin Function		Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SI/RxD	Input	Receive signal	SI	P41/SO00	23	P41/SO00	23	P30/TXD0	25
SO/TxD	Output	Transmit signal	SO	P40/SI00	22	P40/SI00	22	P31/RXD0	26
SCK	Output	Transfer clock	SCK	P42/$\overline{SCK00}$	24	P42/$\overline{SCK00}$	24	Not needed	Not needed
CLK	Output	Clock to V850ES/KG1	X1	X1	12	X1	12	X1	12
			X2	X2[Note]	13	X2[Note]	13	X2[Note]	13
/RESET	Output	Reset signal	/RESET	$\overline{RESET}$	14	$\overline{RESET}$	14	$\overline{RESET}$	14
VPP	Output	Write voltage	VPP	V_{PP}	8	V_{PP}	8	V_{PP}	8
HS	Input	Handshake signal for CSI0 + HS communication	RESERVE /HS	PCS1/$\overline{CS1}$	60	Not needed	Not needed	Not needed	Not needed
VDD	I/O	V_{DD} voltage generation/voltage monitor	VDD	V_{DD}	9	V_{DD}	9	V_{DD}	9
				BV_{DD}	70	BV_{DD}	70	BV_{DD}	70
				EV_{DD}	34	EV_{DD}	34	EV_{DD}	34
				AV_{REF0}	1	AV_{REF0}	1	AV_{REF0}	1
				AV_{REF1}	5	AV_{REF1}	5	AV_{REF1}	5
GND	–	Ground	GND	V_{SS}	11	V_{SS}	11	V_{SS}	11
				AV_{SS}	2	AV_{SS}	2	AV_{SS}	2
				BV_{SS}	69	BV_{SS}	69	BV_{SS}	69
				EV_{SS}	33	EV_{SS}	33	EV_{SS}	33

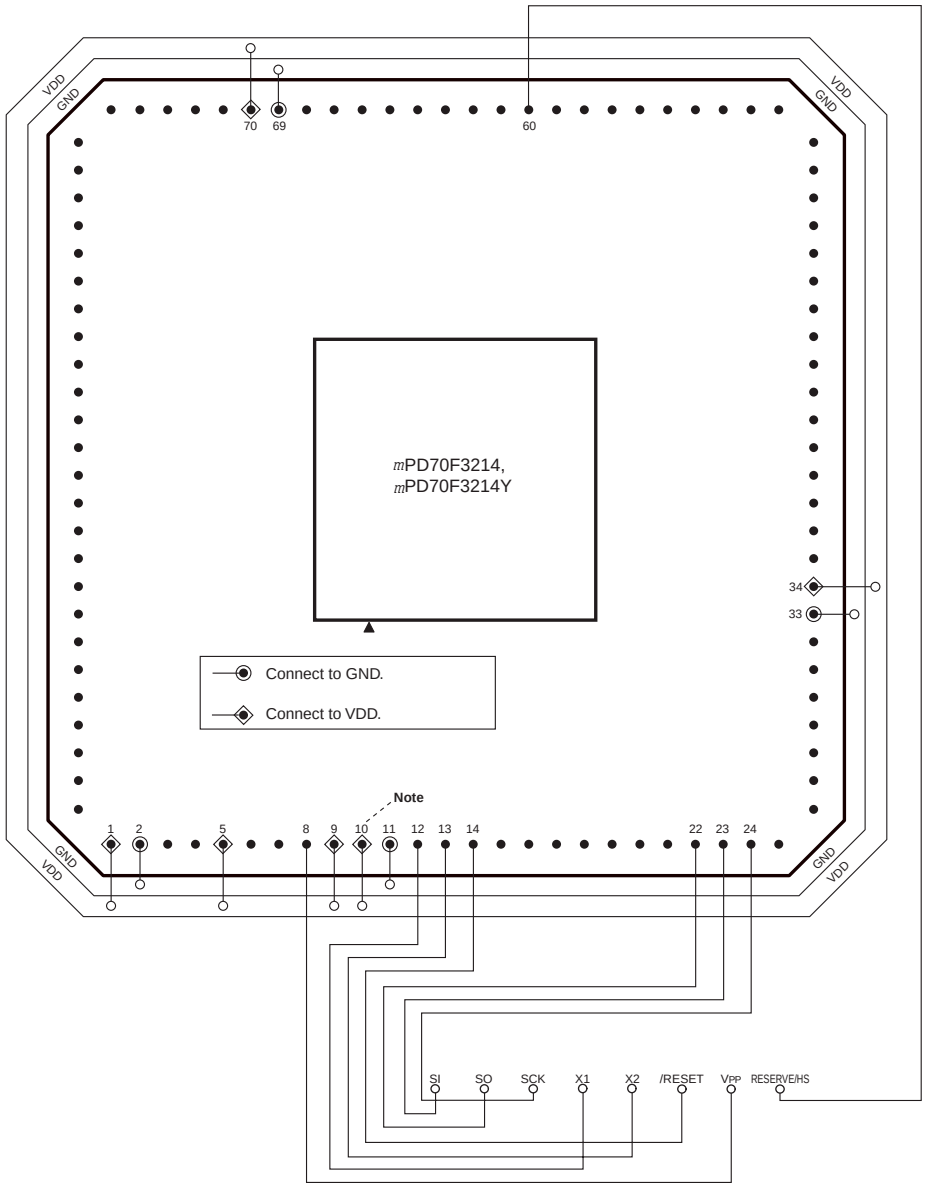
Note When using the clock out of the flash programmer, connect CLK of the programmer to X1, and connect its inverse signal to X2.

Cautions 1. Be sure to connect the REGC pin in either of the following ways.

- **Connect to GND via a 10 μF capacitor**
- **Directly connect to V_{DD}**

2. When connecting the REGC pin to GND via a 10 μF capacitor, the clock cannot be supplied from the CLK pin of the flash programmer.
Supply the clock by creating an oscillator on the board.

Figure 25-2. Wiring Example of V850ES/KG1 Flash Writing Adapter (FA-100GC-8EU)



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Note Be sure to connect the REGC pin in either of the following ways.

- Connect to GND via a 10 μF capacitor.
- Directly connect to V_{DD}.

When connecting the REGC pin to GND via a 10 μF capacitor, the clock cannot be supplied from the CLK pin of the flash programmer.

Supply the clock by preparing an oscillator on the board.

Remarks 1. Handle the pins not described above in accordance with the specified handling of unused pins (refer to **2.4 Pin I/O Circuits and Recommended Connection of Unused Pins).**

When connecting to V_{DD} via a resistor, use of a resistor of 1 kΩ to 10 kΩ is recommended.

2. This adapter is for a 100-pin plastic LQFP (fine pitch) package.

3. This diagram shows the wiring when using a handshake-supporting CSI.

Table 25-3. Wiring Between μPD70F3217 and 70F3217Y (V850ES/KJ1), and PG-FP4

Pin Configuration of Flash Programmer (PG-FP4)			Pin Name on FA Board	With CIS00-HS		With CSI00		With UART0	
Signal Name	I/O	Pin Function		Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.
SI/RxD	Input	Receive signal	SI	P41/SO00	23	P41/SO00	23	P30/TXD0	25
SO/TxD	Output	Transmit signal	SO	P40/SI00	22	P40/SI00	22	P31/RXD0	26
SCK	Output	Transfer clock	SCK	P42/$\overline{SCK00}$	24	P42/$\overline{SCK00}$	24	Not needed	Not needed
CLK	Output	Clock to V850ES/KJ1	X1	X1	12	X1	12	X1	12
			X2	X2[Note]	13	X2[Note]	13	X2[Note]	13
/RESET	Output	Reset signal	/RESET	$\overline{RESET}$	14	$\overline{RESET}$	14	$\overline{RESET}$	14
VPP	Output	Write voltage	VPP	V_{PP}	8	V_{PP}	8	V_{PP}	8
HS	Input	Handshake signal for CSI0 + HS communication	RESERVE /HS	PCS1/$\overline{CS1}$	82	Not needed	Not needed	Not needed	Not needed
VDD	I/O	V_{DD} voltage generation/voltage monitor	VDD	V_{DD}	9	V_{DD}	9	V_{DD}	9
				BV_{DD}	104	BV_{DD}	70	BV_{DD}	70
				EV_{DD}	34	EV_{DD}	34	EV_{DD}	34
				AV_{REF0}	1	AV_{REF0}	1	AV_{REF0}	1
				AV_{REF1}	5	AV_{REF1}	5	AV_{REF1}	5
GND	–	Ground	GND	V_{SS}	11	V_{SS}	11	V_{SS}	11
				AV_{SS}	2	AV_{SS}	2	AV_{SS}	2
				BV_{SS}	103	BV_{SS}	69	BV_{SS}	69
				EV_{SS}	33	EV_{SS}	33	EV_{SS}	33

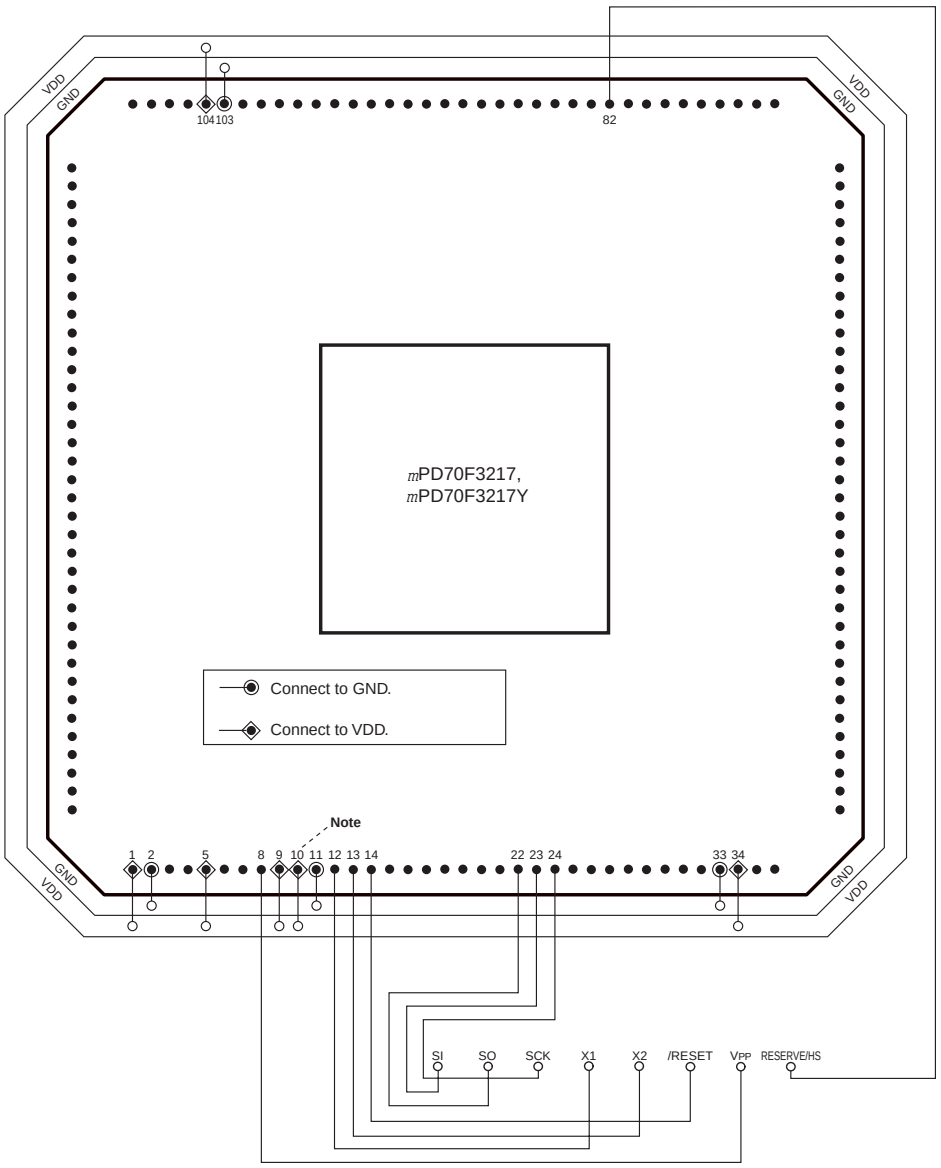
Note When using the clock out of the flash programmer, connect CLK of the programmer to X1, and connect its inverse signal to X2.

Cautions 1. Be sure to connect the REGC pin in either of the following ways.

- **Connect to GND via a 10 μF capacitor**
- **Directly connect to V_{DD}**

2. When connecting the REGC pin to GND via a 10 μF capacitor, the clock cannot be supplied from the CLK pin of the flash programmer.
Supply the clock by creating an oscillator on the board.

Figure 25-3. Wiring Example of V850ES/KJ1 Flash Writing Adapter (FA-144GJ-UEN)



Note Be sure to connect the REGC pin in either of the following ways.

- Connect to GND via a 10 μF capacitor.
- Directly connect to V_{DD}.

When connecting the REGC pin to GND via a 10 μF capacitor, the clock cannot be supplied from the CLK pin of the flash programmer.

Supply the clock by preparing an oscillator on the board.

Remarks 1. Handle the pins not described above in accordance with the specified handling of unused pins (refer to **2.4 Pin I/O Circuits and Recommended Connection of Unused Pins).**

When connecting to V_{DD} via a resistor, use of a resistor of 1 kΩ to 10 kΩ is recommended.

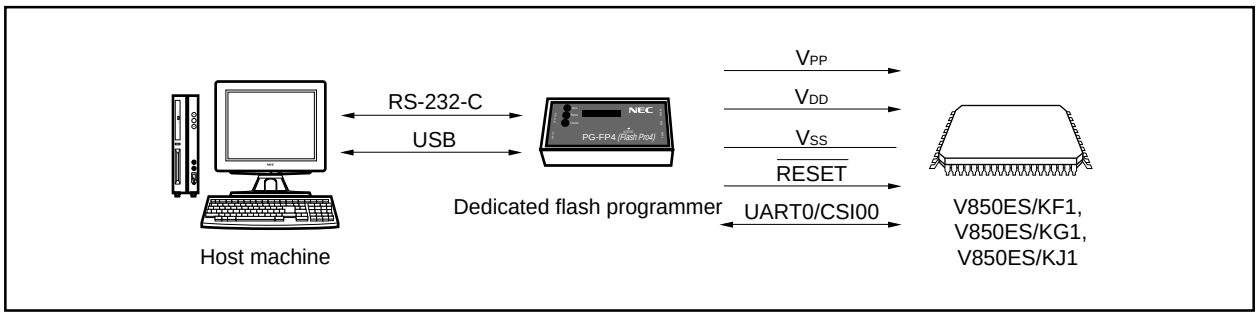
2. This adapter is for a 144-pin plastic LQFP (fine pitch) package.

3. This diagram shows the wiring when using a handshake-supporting CSI.

25.3 Programming Environment

The environment required for writing a program to the flash memory of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 is illustrated below.

Figure 25-4. Environment for Writing Program to Flash Memory



A host machine that controls the dedicated flash programmer is necessary.

To interface between the flash programmer and the V850ES/KF1, V850ES/KG1, and V850ES/KJ1, UART0 or CSI00 is used for manipulation such as writing and erasing. To write the flash memory off-board, a dedicated program adapter (FA series) is necessary.

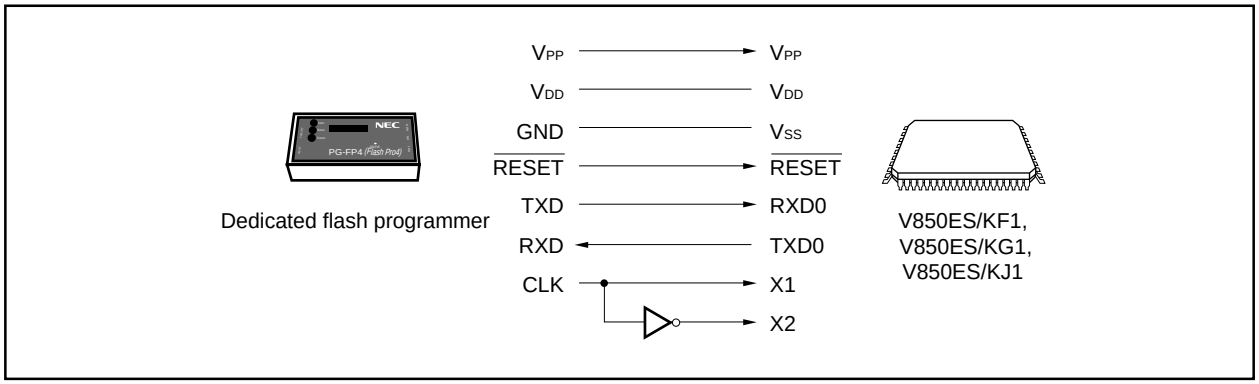
25.4 Communication Mode

Communication between the dedicated flash programmer and the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 is established by serial communication via UART0 or CSI00 of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1.

(1) UART0

Transfer rate: 9600 to 153600 bps (LSB first)

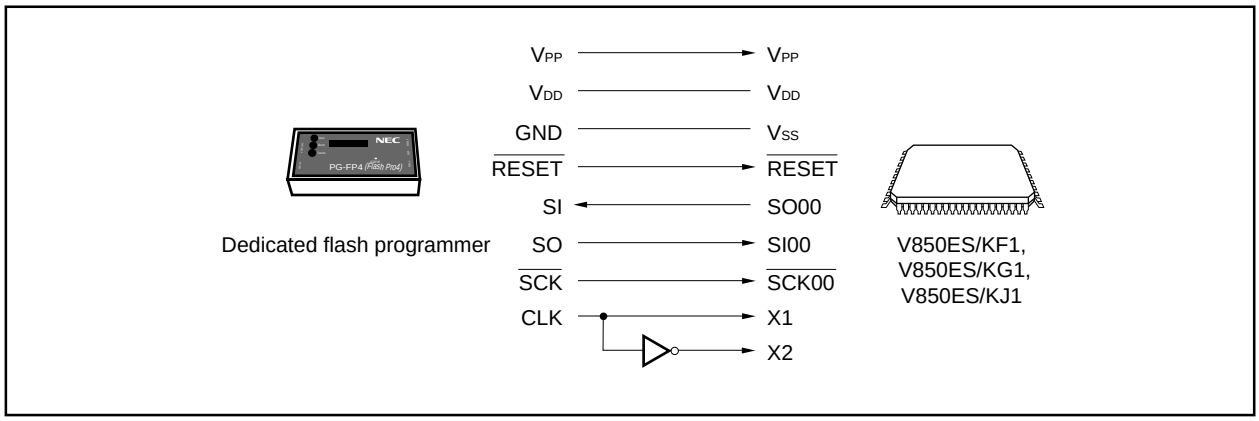
Figure 25-5. Communication with Dedicated Flash Programmer (UART0)



(2) CSI00

Transfer rate: 2.4 kHz to 2.5 MHz (MSB first)

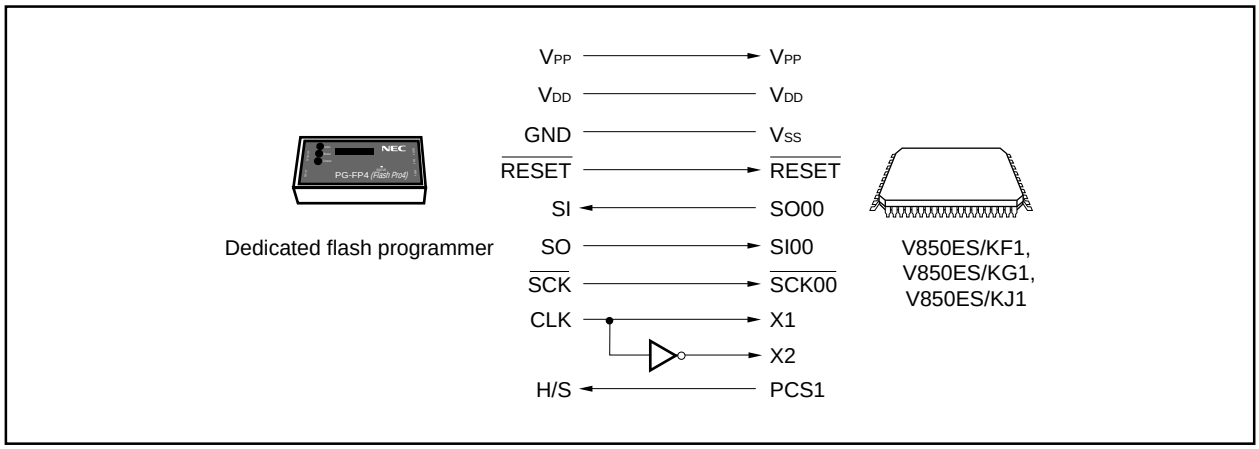
Figure 25-6. Communication with Dedicated Flash Programmer (CSI00)



(3) CSI communication mode supporting handshake

Transfer rate: 2.4 kHz to 2.5 MHz (MSB first)

Figure 25-7. Communication with Flash Programmer (CSI00+H/S)



If the PG-FP4 is used as the flash programmer, the PG-PF4 generates the following signal for the V850ES/KF1, V850ES/KG1, and V850ES/KJ1. For details, refer to the **PG-FP4 User's Manual (U15260E)**.

Table 25-4. Signals Generated by Dedicated Flash Programmer (PG-FP4)

PG-FP4			V850ES/KF1, V850ES/KG1, V850ES/KJ1	Connection	
Signal Name	I/O	Pin Function	Pin Name	CSI00	UART0
VPP	Output	Write voltage	V_{PP}	◎	◎
VDD[Note 1]	I/O	V_{DD} voltage generation	V_{DD}	◎	◎
GND	–	Ground	V_{SS}	◎	◎
CLK	Output	Clock output to V850ES/KF1, V850ES/KG1, or V850ES/KJ1	X1, X2[Note 2]	○	○
$\overline{\text{RESET}}$	Output	Reset signal	$\overline{\text{RESET}}$	◎	◎
SI/RxD	Input	Receive signal	SO00/TXD0	◎	◎
SO/TxD	Output	Transmit signal	SI00/RXD0	◎	◎
SCK	Output	Transfer clock	$\overline{\text{SCK00}}$	◎	×
H/S	Input	Handshake signal of CSI00+HS communication	PCS1	△	×

Notes 1. The PG-FP3 has a V_{DD} voltage monitoring function.

2. For off-board writing only: connect the clock output of the flash programmer to X1 and its inverse signal to X2.

Remark ◎: Be sure to connect the pin.
○: The pin does not have to be connected if the signal is generated on the target board.
×: The pin does not have to be connected.
△: In handshake mode

25.5 Pin Processing

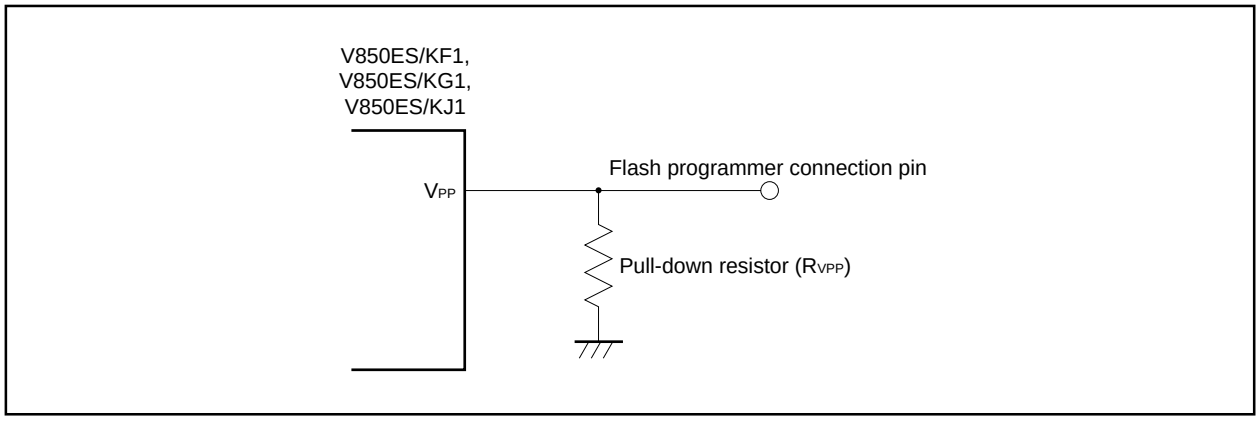
To write the flash memory on-board, connectors that connect the flash programmer must be provided on the target system. First provide a function that selects the normal operation mode or flash memory programming mode on the board.

When the flash memory programming mode is set, all the pins not used for programming the flash memory are in the same status as immediately after reset. Therefore, if the external device does not recognize the state immediately after reset, the pins must be processed as described below.

25.5.1 V_{PP} pin

In the normal operation mode, connect the V_{PP} pin to V_{SS}. In the flash memory programming mode, a write voltage of 10 V is supplied to the V_{PP} pin. An example of connection of the V_{PP} pin is illustrated below.

Figure 25-8. Example of Connection of V_{PP} Pin



25.5.2 Serial interface pins

The pins used by each serial interface are listed below.

Table 25-5. Pins Used by Each Serial Interface

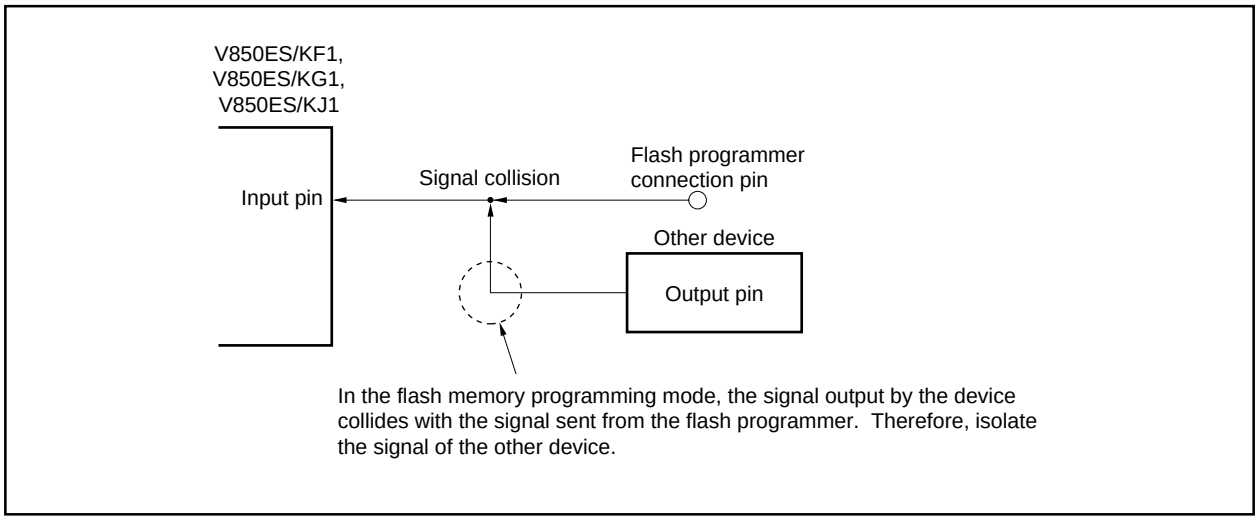
Serial Interface	Pins Used
CSI00	SO00, SI00, $\overline{\text{SCK00}}$
CSI00 + HS	SO00, SI00, $\overline{\text{SCK00}}$, PCS1
UART0	TXD0, RXD0

To connect the dedicated flash programmer to the pins of a serial interface that is connected to another device on the board, care must be exercised so that signals do not collide or that the other device does not malfunction.

(1) Signal collision

If the flash programmer (output) is connected to a pin (input) of a serial interface connected to another device (output), signal collision takes place. To avoid this collision, either isolate the connection with the other device, or make the other device go into an output high-impedance state.

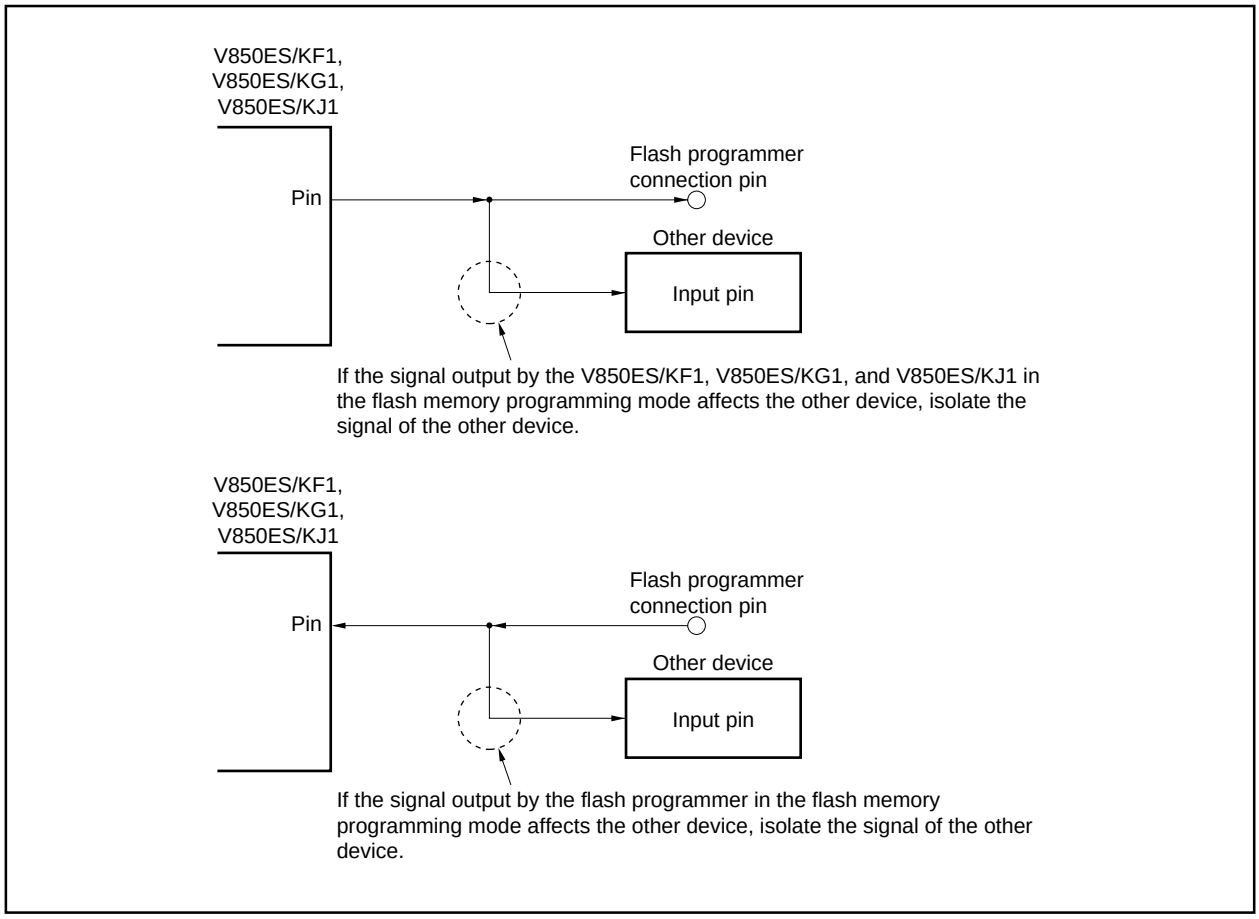
Figure 25-9. Signal Collision (Input Pin of Serial Interface)



(2) Malfunction of other device

If the dedicated flash programmer (output or input) is connected to a pin (input or output) of a serial interface connected to another device (input), a signal may be output to the other device, causing the device to malfunction. To avoid this malfunction, isolate the connection with the other device.

Figure 25-10. Malfunction of Other Device

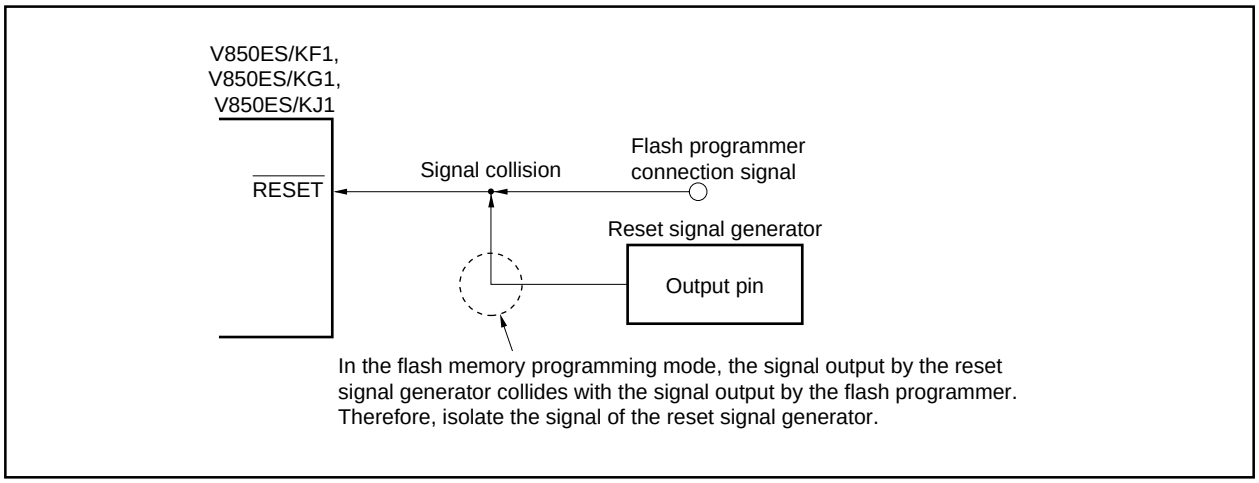


25.5.3 $\overline{\text{RESET}}$ pin

If the reset signal of the flash programmer is connected to the $\overline{\text{RESET}}$ pin that is connected to the reset signal generator on the board, signal collision takes place. To prevent this collision, isolate the connection with the reset signal generator.

If the reset signal is input from the user system while the flash memory programming mode is set, the flash memory will not be correctly programmed. Do not input any signal other than the reset signal of the flash programmer.

Figure 25-11. Signal Collision ($\overline{\text{RESET}}$ Pin)



25.5.4 Port pins

When the system shifts to the flash memory programming mode, all the pins that are not used for flash memory programming are in the same status as that immediately after reset. If the external device connected to each port does not recognize the status of the port immediately after reset, pins require appropriate processing, such as connecting to V_{DD} via a resistor or connecting to V_{SS} via a resistor.

25.5.5 Other signal pins

Connect the X1, X2, XT1, XT2, and REGC pins in the same status as in the normal operation mode.

To input the operating clock from the programmer, however, connect the clock out of the programmer to X1, and its inverse signal to X2.

25.5.6 Power supply

Supply the same power as in the normal operation mode for the power supply (V_{DD}, V_{SS}, AV_{REF0}, AV_{REF1}, AV_{SS}, BV_{DD}, BV_{SS}, EV_{DD}, and EV_{SS}).

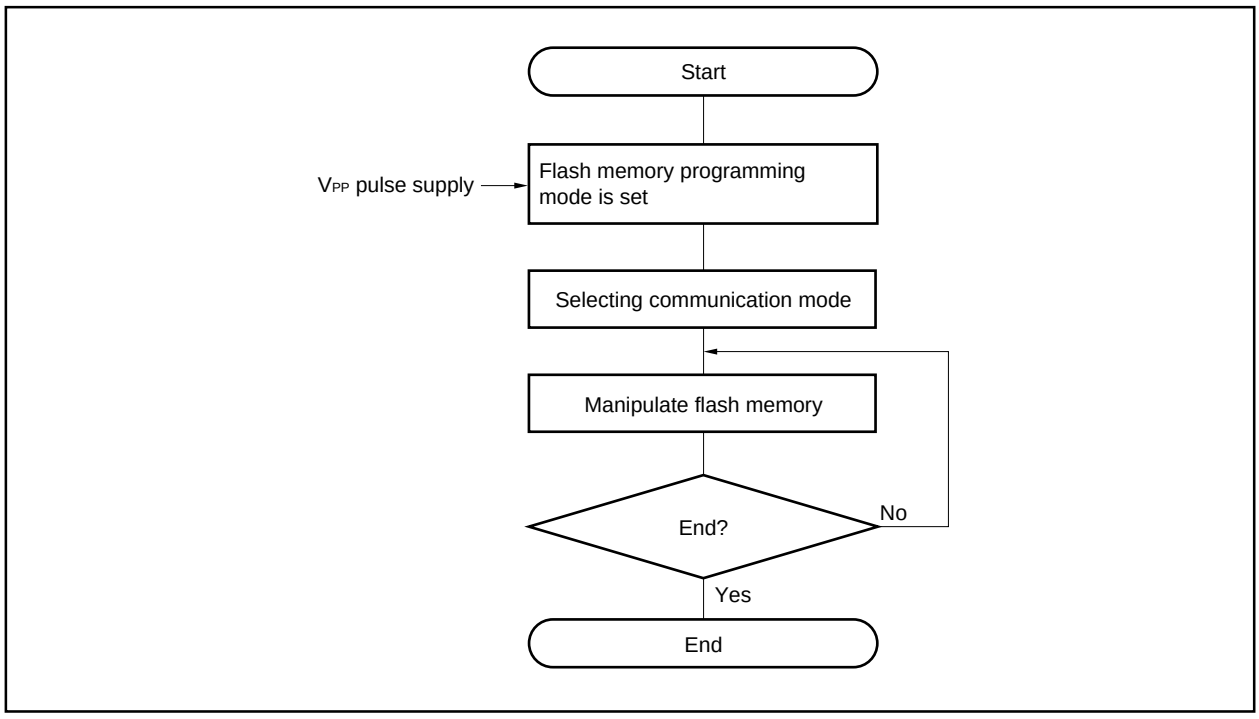
Caution VDD of the flash programmer (PG-FP3) has a power monitor function. Be sure to connect V_{DD} and V_{SS} to VDD and GND of the flash programmer.

25.6 Programming Method

25.6.1 Controlling flash memory

The following figure illustrates the procedure to manipulate the flash memory.

Figure 25-12. Flash Memory Manipulation Procedure

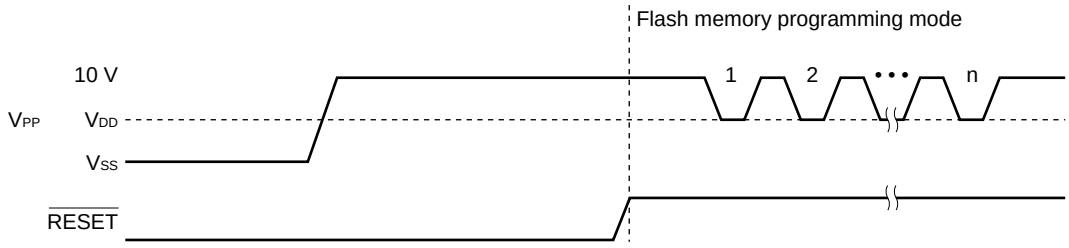


25.6.2 Flash memory programming mode

To rewrite the contents of the flash memory by using the dedicated flash programmer, set the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 in the flash memory programming mode. To set the mode, set the V_{PP} pin and clear the reset signal.

Change the mode by using a jumper when writing the flash memory on-board.

Figure 25-13. Flash Memory Programming Mode



V_{PP}	Operation mode
V_{SS}	Normal operation mode
10 V	Flash memory programming mode

25.6.3 Selecting communication mode

In the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 a communication mode is selected by inputting pulses (up to 8 pulses) to the V_{PP} pin after the flash memory programming mode is entered. These V_{PP} pulses are generated by the flash programmer.

The following table shows the relationship between the number of pulses and communication modes.

Table 25-6. Communication Modes

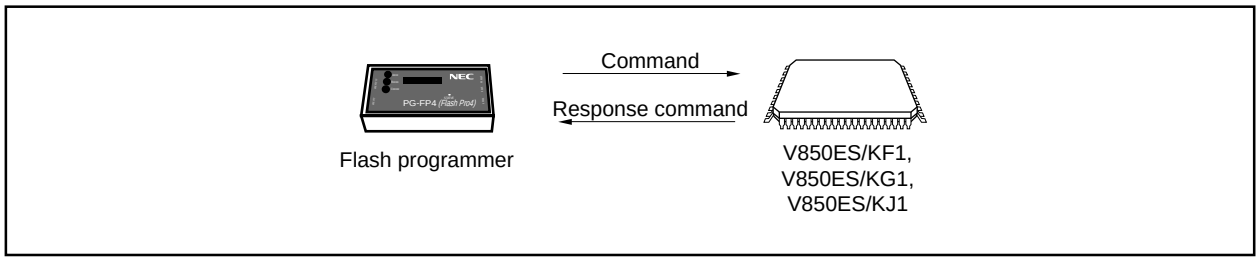
V_{PP} Pulse	Communication Mode	Remark
0	CSI00	V850ES/KF1, V850ES/KG1, and V850ES/KJ1 operate as slave with MSB first.
3	CSI00 + HS	V850ES/KF1, V850ES/KG1, and V850ES/KJ1 operate as slave with MSB first.
8	UART0	Communication rate: 9600 bps (after reset), LSB first
Other	RFU	Setting prohibited

Caution When UART0 is selected, the receive clock is calculated based on the reset command sent from the dedicated flash programmer after the V_{PP} pulse has been received.

25.6.4 Communication commands

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 communicate with the flash programmer by using commands. The signals sent from the flash programmer to the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 are called commands, and the commands sent from the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 to the flash programmer are called response commands.

Figure 25-14. Communication Commands



The flash memory control commands of the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 are listed in the table below. All these commands are issued from the programmer and the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 perform processing corresponding to the respective commands.

Table 25-7. Flash Memory Control Commands

Classification	Command Name	Function
Verify	Batch verify command	Compares the contents of the entire memory with the input data.
Erase	Batch erase command	Erases the contents of the entire memory.
Blank check	Batch blank check command	Checks the erasure status of the entire memory.
Data write	High-speed write command	Writes data by specifying the write address and number of bytes to be written, and executes a verify check.
	Successive write command	Writes data from the address following that of the high-speed write command executed immediately before, and executes a verify check.
System setting, control	Status read command	Obtains the operation status
	Oscillation frequency setting command	Sets the oscillation frequency
	Erase time setting command	Sets the erase time for batch erase
	Write time setting command	Sets the write time for writing data
	Baud rate setting command	Sets the baud rate when UART is used
	Silicon signature command	Reads the silicon signature information
	Reset command	Escapes from each status

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 return a response command for the command issued by the dedicated flash programmer. The response commands sent from the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 are listed below.

Table 25-8. Response Commands

Command Name	Function
ACK (acknowledge)	Acknowledges command/data.
NAK (not acknowledge)	Acknowledges illegal command/data.

CHAPTER 26 ELECTRICAL SPECIFICATIONS (STANDARD PRODUCTS, SPECIAL GRADE (A) PRODUCTS)

Standard products are as follows:

V850ES/KF1:	V850ES/KG1:	V850ES/KJ1:
μPD703208	μPD703212	μPD703216
μPD703208Y	μPD703212Y	μPD703216Y
μPD703209	μPD703213	μPD703217
μPD703209Y	μPD703213Y	μPD703217Y
μPD703210	μPD703214	μPD70F3217
μPD703210Y	μPD703214Y	μPD70F3217Y
μPD70F3210	μPD70F3214	
μPD70F3210Y	μPD70F3214Y	

Special grade (A) products are as follows.

V850ES/KF1:	V850ES/KG1:	V850ES/KJ1:
μPD703208(A)	μPD703212(A)	μPD703216(A)
μPD703208Y(A)	μPD703212Y(A)	μPD703216Y(A)
μPD703209(A)	μPD703213(A)	μPD703217(A)
μPD703209Y(A)	μPD703213Y(A)	μPD703217Y(A)
μPD703210(A)	μPD703214(A)	μPD70F3217(A)
μPD703210Y(A)	μPD703214Y(A)	μPD70F3217Y(A)
μPD70F3210(A)	μPD70F3214(A)	
μPD70F3210Y(A)	μPD70F3214Y(A)	

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	V_{PP}	Flash memory version, **Note 1**	−0.3 to +10.5	V
	BV_{DD}	$BV_{DD} \leq V_{DD}$	−0.3 to V_{DD} + 0.3 **Note 2**	V
	EV_{DD}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	AV_{REF0}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	AV_{REF1}	$AV_{REF1} \leq V_{DD}$ (D/A output mode) $AV_{REF1} = AV_{REF0} = V_{DD}$ (port mode)	−0.3 to V_{DD} + 0.3 **Note 2**	V
	V_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.3 to +0.3	V
	AV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.3 to +0.3	V
	BV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.3 to +0.3	V
	EV_{SS}	$V_{SS} = EV_{SS} = BV_{SS} = AV_{SS}$	−0.3 to +0.3	V
Input voltage	V_{I1}	P00 to P06, P30 to P35, P38, P39, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915, $\overline{\text{RESET}}$	−0.3 to EV_{DD} + 0.3 **Note 2**	V
	V_{I2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7	−0.3 to BV_{DD} + 0.3 **Note 2**	V
	V_{I3}	P10, P11	−0.3 to AV_{REF1} + 0.3 **Note 2**	V
	V_{I4}	P36, P37, P614, P615	−0.3 to +13 **Note 3**	V
★	V_{I5}	X1, X2, XT1, XT2	−0.3 to V_{DD} + 0.3 **Note 2**	V
Analog input voltage	V_{IAN}	P70 to P715	−0.3 to AV_{REF0} + 0.3 **Note 2**	V

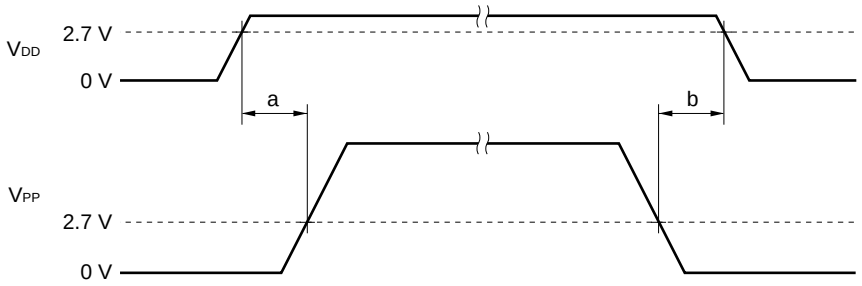
Notes 1. Make sure that the following conditions of the V_{PP} voltage application timing are satisfied when the flash memory is written.

- **When supply voltage rises**

  V_{PP} must exceed V_{DD} 15 μs or more after V_{DD} has reached the lower-limit value (2.7 V) of the operating voltage range (see a in the figure below).

- **When supply voltage drops**

  V_{DD} must be lowered 10 μs or more after V_{PP} falls below the lower-limit value (2.7 V) of the operating voltage range of V_{DD} (see b in the figure below).



2. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

3. When pull-up is not specified by a mask option. The same as V_{I1} when pull-up is specified.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I_{OL} Note	P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915, PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7	Per pin	20	mA
		P36 to P39, P614, P615		30	mA
		P00 to P06, P30 to P39, P40 to P42	Total of all pins: 70 mA	35	mA
		P50 to P55, P60 to P615, P80, P81, P90 to P915		35	
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7	Total of all pins: 70 mA	35	mA
		PDL0 to PDL15, PDH0 to PDH7		35	mA
Output current, high	I_{OH} Note	Per pin		−10	mA
		P00 to P06, P30 to P35, P40 to P42	Total of all pins: −60 mA	−30	
		P50 to P55, P60 to P613, P80, P81, P90 to P915		−30	mA
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7	Total of all pins: −60 mA	−30	mA
★		PDL0 to PDL15, PDH0 to PDH7		−30	mA
		P10, P11	Per pin	−10	
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}	Mask ROM version		−65 to +150	°C
		Flash memory version		−40 to +125	°C

Note In the V850ES/KF1, the specifications of the total of all pins for I_{OL} and I_{OH} are as follows since BV_{DD} system pins do not exist.

I_{OL}	Total of pins: 70 mA	P00 to P06, P30 to P35, P38, P39, P40 to P42	35	mA
		P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL15	35	mA
I_{OH}	Total of pins: −60 mA	P00 to P06, P30 to P35, P40 to P42	−30	mA
		P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL15	−30	mA

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

3. The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

In the V850ES/KF1, the specification of V_{I2} is the same as that of the V_{I1} since the BV_{DD} pin does not exist.

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

Capacitance (T_A = 25°C, V_{DD} = EV_{DD} = AV_{REF0} = BV_{DD} = AV_{REF1} = V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_X = 1 MHz Unmeasured pins returned to 0 V	P70 to P715			15	pF
I/O capacitance	C_{IO}		**Note**			15	pF
			P36 to P39, P614, P615			20	pF

Note P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915, PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

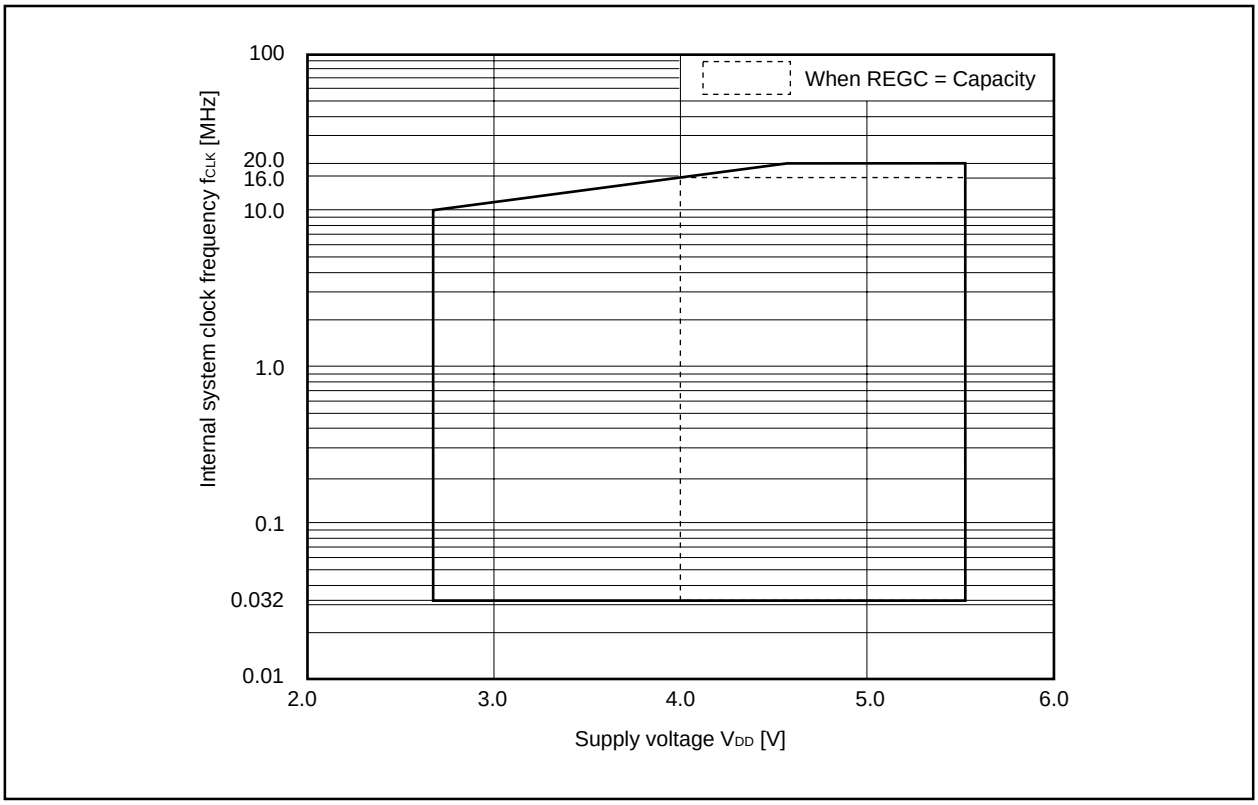
P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

Operating Conditions

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
★ Internal system clock frequency	f_{CLK}	REGC = V_{DD} = 5 V ±10% In PLL mode (OSC = 2 to 5 MHz)	0.25		20	MHz
★		REGC = Capacity, V_{DD} = 4.0 to 5.5 V In PLL mode (OSC = 2 to 4 MHz)	0.25		16	MHz
★		REGC = V_{DD} = 2.7 to 5.5 V	0.0625		10	MHz
		REGC = V_{DD} = 2.7 to 5.5 V, operating with subclock		32.768		kHz

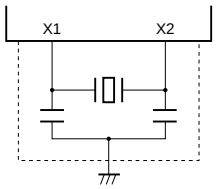
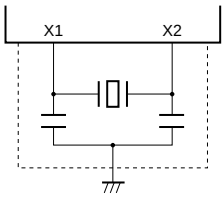
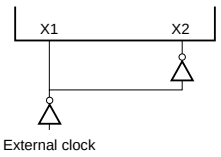
Internal System Clock Frequency vs. Supply Voltage



PLL Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_x		2		5	MHz
Output frequency	f_{xx}		8		20	MHz
Lock time	t_{PLL}	After V_{DD} reaches MIN.:2.7 V			200	μs

Main Clock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		2		10	MHz
		Oscillation stabilization timeNote 2	After reset is released		$2^{15}/f_X$		s
			After STOP mode is released		**Note 3**		s
Crystal resonator		Oscillation frequency (f_X)Note 1		2		10	MHz
		Oscillation stabilization timeNote 2	After reset is released		$2^{15}/f_X$		s
			After STOP mode is released		**Note 3**		s
External clock		X1, X2 input frequency (f_X)	REGC = V_{DD} Duty = 50% ±5%	2		10	MHz

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize the resonator after reset or STOP mode is released.

3. The value differs depending on the OSTS register settings.

Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

(i) Murata Manufacturing Co., Ltd.: Ceramic resonator (T_A = –40 to +85°C)

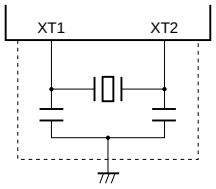
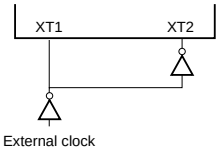
Manufacturer	Product Name	Type	Oscillation Frequency f_{XX} (MHz)	Recommended Circuit Constant			Recommended Voltage Range	
				C1 (pF)	C2 (pF)	Rd (kΩ)	MIN. (V)	MAX. (V)
Murata Mfg. Co., Ltd.	CSTCC2M00G56-R0	SMD	2.000	47	47	0	2.7	5.5
	CSTCC3M00G56-R0	SMD	3.000	47	47	0	2.7	5.5
	CSTCR4M00G55-R0	SMD	4.000	39	39	0	2.7	5.5
	CSTLS4M00G56-B0			47	47	0	2.7	5.5
	CSTCR5M00G55-R0	SMD	5.000	39	39	0	2.7	5.5
	CSTLS5M00G56-B0			47	47	0	2.7	5.5
	CSTCE10M0G52-R0	SMD	10.000	10	10	0	2.7	5.5
	CSTLS10M0G53-B0			15	15	0	2.7	5.5
	CSTCC2M00G56A-R0	SMD	2.000	47	47	0	2.7	5.5
	CSTCC3M00G56A-R0	SMD	3.000	47	47	0	2.7	5.5
	CSTCR4M00G55A-R0	SMD	4.000	39	39	0	2.7	5.5
	CSTCR5M00G55A-R0	SMD	5.000	39	39	0	2.7	5.5
	CSTCE10M0G52A-R0	SMD	10.000	10	10	0	2.7	5.5

Caution This oscillator constant is a reference value based on evaluation under a specific environment by the resonator manufacturer.

If optimization of oscillator characteristics is necessary in the actual application, apply to the resonator manufacturer for evaluation on the implementation circuit.

The oscillation voltage and oscillation frequency indicate only oscillator characteristics. Use the V850ES/KF1, V850ES/KG1, and V850ES/KJ1 so that the internal operating conditions are within the specifications of the DC and AC characteristics.

Subclock Oscillator Characteristics (T_A = –40 to +85°C, V_{DD} = 2.7 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2			10		s
External clock		XT1 input frequency (f_{XT})Note 1 Duty = 50% ±5%	REGC = V_{DD}	32		35	kHz

Notes 1. Indicates only oscillator characteristics.

2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 2.7 V) to when the crystal resonator stabilizes.

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (1/5)

Parameter	Symbol	Conditions		MAX.	Unit
★ Output current, high	I_{OH1}	Per pin for P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915		–5.0	mA
		Total of P00 to P06, P30 to P35, P40 to P42	EV_{DD} = 4.0 to 5.5 V	–30	mA
			EV_{DD} = 2.7 to 5.5 V	–15	mA
		Total of P50 to P55, P60 to P613, P80, P81, P90 to P915	EV_{DD} = 4.0 to 5.5 V	–30	mA
			EV_{DD} = 2.7 to 5.5 V	–15	mA
	I_{OH2}	Per pin for PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7, PDH0 to PDH7, PDL0 to PDL15		–5.0	mA
★		Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7	BV_{DD} = 4.0 to 5.5 V	–30	mA
★			BV_{DD} = 2.7 to 5.5 V	–15	mA
★		Total of PDL0 to PDL15, PDH0 to PDH7	BV_{DD} = 4.0 to 5.5 V	–30	mA
★			BV_{DD} = 2.7 to 5.5 V	–15	mA
★ Output current, low	I_{OL1}	Per pin for P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915		10	mA
		Per pin for P36 to P39	EV_{DD} = 4.0 to 5.5 V	15	mA
			EV_{DD} = 2.7 to 5.5 V	8	mA
		Per pin for P614, P615	EV_{DD} = 4.0 to 5.5 V	10	mA
			EV_{DD} = 2.7 to 5.5 V	5	mA
		Total of P00 to P06, P30 to P37, P40 to P42		30	mA
		Total of P38, P39, P50 to P55, P60 to P615, P80, P81, P90 to P915		30	mA
	I_{OL2}	Per pin for PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7, PDH0 to PDH7, PDL0 to PDL15		10	mA
		Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7		30	mA
		Total of PDL0 to PDL15, PDH0 to PDH7		30	mA

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (2/5)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	**Note 1**	$0.7EV_{DD}$		EV_{DD}	V
	V_{IH2}	**Note 2**	$0.8EV_{DD}$		EV_{DD}	V
	V_{IH3}	**Note 3**	$0.7BV_{DD}$		BV_{DD}	V
	V_{IH4}	P70 to P715	$0.7AV_{REF0}$		AV_{REF0}	V
	V_{IH5}	P10, P11[Note 4]	$0.7AV_{REF1}$		AV_{REF1}	V
	V_{IH6}	P36, P37, P614, P615	$0.7EV_{DD}$		12[Note 5]	V
	V_{IH7}	X1, X2, XT1, XT2	EV_{DD} – 0.5		EV_{DD}	V
Input voltage, low	V_{IL1}	**Note 1**	EV_{SS}		$0.3EV_{DD}$	V
	V_{IL2}	**Note 2**	EV_{SS}		$0.2EV_{DD}$	V
	V_{IL3}	**Note 3**	BV_{SS}		$0.3BV_{DD}$	V
	V_{IL4}	P70 to P715	AV_{SS}		$0.3AV_{REF0}$	V
	V_{IL5}	P10, P11[Note 4]	AV_{SS}		$0.3AV_{REF1}$	V
	V_{IL6}	P36, P37, P614, P615	EV_{SS}		$0.3EV_{DD}$	V
	V_{IL7}	X1, X2, XT1, XT2	EV_{SS}		0.4	V

Notes 1. P00, P01, P30, P41, P60 to P65, P67, P611, P98, P911 and their alternate-function pins.

2. $\overline{\text{RESET}}$, P02 to P06, P31 to P35, P38, P39, P40, P42, P50 to P55, P66, P68 to P610, P612, P613, P80, P81, P90 to P97, P99, P910, P912 to P915 and their alternate-function pins.

3. PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7 and their alternate-function pins.

4. When used as port pins, set AV_{REF1} = AV_{REF0} = V_{DD}.

5. When pull-up is not specified by a mask option. EV_{DD} when pull-up is specified.

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (3/5)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	**Note 1**	I_{OH} = –2.0 mA, EV_{DD} = 4.0 to 5.5 V	EV_{DD} – 1.0		EV_{DD}	V
		Note 2	I_{OH} = –0.1 mA, EV_{DD} = 2.7 to 5.5 V	EV_{DD} – 0.5		EV_{DD}	V
	V_{OH2}	**Note 3**	I_{OH} = –2.0 mA, EV_{DD} = 4.0 to 5.5 V	BV_{DD} – 1.0		BV_{DD}	V
		Note 4	I_{OH} = –0.1 mA, EV_{DD} = 2.7 to 5.5 V	BV_{DD} – 0.5		BV_{DD}	V
★	V_{OH3}	P10, P11[Note 5]	I_{OH} = –2.0 mA	AV_{REF1} – 1.0		AV_{REF1}	V
★			I_{OH} = –0.1 mA	AV_{REF1} – 0.5		AV_{REF1}	V
Output voltage, low	V_{OL1}	**Note 6**	I_{OL} = 2.0 mA[Note 7]	0		0.8	V
	V_{OL2}	**Note 8**	I_{OL} = 2.0 mA[Note 7]	0		0.8	V
	V_{OL3}	P10, P11[Note 5]	I_{OL} = 2 mA	0		0.8	V
	V_{OL4}	P36 to P39	I_{OL} = 15 mA, EV_{DD} = 4.0 to 5.5 V	0		2.0	V
			I_{OL} = 8 mA, EV_{DD} = 3.0 to 5.5 V	0		1.0	V
			I_{OL} = 5 mA, EV_{DD} = 2.7 to 5.5 V	0		1.0	V
	V_{OL5}	P614, P615	I_{OL} = 10 mA, EV_{DD} = 4.0 to 5.5 V	0		2.0	V
			I_{OL} = 5 mA, EV_{DD} = 2.7 to 5.5 V	0		1.0	V

Notes 1. Total of P00 to P06, P30 to P35, P40 to P42 and their alternate-function pins: I_{OH} = –30 mA, total of P50 to P55, P60 to P613, P80, P81, P90 to P915 and their alternate-function pins: I_{OH} = –30 mA.

2. Total of P00 to P06, P30 to P35, P40 to P42 and their alternate-function pins: I_{OH} = –15 mA, total of P50 to P55, P60 to P613, P80, P81, P90 to P915 and their alternate-function pins: I_{OH} = –15 mA.

3. Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7: I_{OH} = –30 mA, total of PDH0 to PDH7, PDL0 to PDL15 and their alternate-function pins: I_{OH} = –30 mA.

4. Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7: I_{OH} = –15 mA, total of PDH0 to PDH7, PDL0 to PDL15 and their alternate-function pins: I_{OH} = –15 mA.

5. When used as port pins, set AV_{REF1} = AV_{REF0} = V_{DD}.

6. Total of P00 to P06, P30 to P37, P40 to P42 and their alternate-function pins: I_{OL} = 30 mA, total of P38 to P39, P50 to P55, P60 to P615, P80, P81, P90 to P915 and their alternate-function pins: I_{OL} = 30 mA.

7. Refer to I_{OL1} for I_{OL} of P36 to P39, P614, and P615.

8. Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7 and their alternate-function pins:I_{OL} = 30 mA, total of PDH0 to PDH7, PDL0 to PDL15 and their alternate-function pins: I_{OL} = 30 mA.

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (4/5)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH}	V_{IN} = V_{DD}				3.0	μA
Input leakage current, low	I_{LIL}	V_{IN} = 0 V				–3.0	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}				3.0	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–3.0	μA
Supply current[Note] (flash memory version)	I_{DD1}	Normal operation	f_{XX} = 20 MHz (OSC = 5 MHz) (in PLL mode) REGC = V_{DD} = 5 V ±10%		43	60	mA
			f_{XX} = 16 MHz (OSC = 4 MHz) (in PLL mode) REGC = Capacity V_{DD} = 5 V ±10%		27	40	mA
			f_{XX} = 10 MHz (OSC = 10 MHz) REGC = V_{DD} = 3 V ±10%		14	29	mA
	I_{DD2}	HALT mode	f_{XX} = 20 MHz (OSC = 5 MHz) (in PLL mode) REGC = V_{DD} = 5 V ±10%		18	28	mA
			f_{XX} = 16 MHz (OSC = 4 MHz) (in PLL mode) REGC = Capacity V_{DD} = 5 V ±10%		11	20	mA
			f_{XX} = 10 MHz (OSC = 10 MHz) REGC = V_{DD} = 3 V ±10%		6	11	mA
	I_{DD3}	IDLE mode	OSC = 5 MHz (when PLL mode off) REGC = V_{DD} = 5 V ±10%		1200	2000	μA
			OSC = 4 MHz (when PLL mode off) REGC = Capacity V_{DD} = 5 V ±10%		900	1600	μA
			OSC = 10 MHz (when PLL mode off) REGC = V_{DD} = 3 V ±10%		900	1600	μA
	I_{DD4}	Subclock operating mode	f_{XT} = 32.768 kHz		190	320	μA
	I_{DD5}	Subclock IDLE mode	f_{XT} = 32.768 kHz		15	60	μA
	I_{DD6}	STOP mode			0.1	30	μA
Pull-up resistor	R_L	V_{IN} = 0 V		10	30	100	kΩ

Note Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped). AV_{REF0} is not included.

DC Characteristics

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (5/5)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Supply current[Note 1] (mask ROM version)	I_{DD1}	Normal operation	f_{XX} = 20 MHz (OSC = 5 MHz) (in PLL mode) REGC = V_{DD} = 5 V ±10%		30	45	mA
			f_{XX} = 16 MHz (OSC = 4 MHz) (in PLL mode) REGC = Capacity V_{DD} = 5 V ±10%		18	30	mA
			f_{XX} = 10 MHz (OSC = 10 MHz) REGC = V_{DD} = 3 V ±10%		9	18	mA
	I_{DD2}	HALT mode	f_{XX} = 20 MHz (OSC = 5 MHz) (in PLL mode) REGC = V_{DD} = 5 V ±10%		17	25	mA
			f_{XX} = 16 MHz (OSC = 4 MHz) (in PLL mode) REGC = Capacity V_{DD} = 5 V ±10%		10	18	mA
			f_{XX} = 10 MHz (OSC = 10 MHz) REGC = V_{DD} = 3 V ±10%		5	10	mA
	I_{DD3}	IDLE mode	OSC = 5 MHz (when PLL mode off) REGC = V_{DD} = 5 V ±10%[Note 2]		900	1400	μA
			OSC = 4 MHz (when PLL mode off) REGC = Capacity V_{DD} = 5 V ±10%		600	1000	μA
			OSC = 10 MHz (when PLL mode off) REGC = V_{DD} = 3 V ±10%		600	1000	μA
	I_{DD4}	Subclock operating mode	f_{XT} = 32.768 kHz		70	160	μA
	I_{DD5}	Subclock IDLEmode	f_{XT} = 32.768 kHz		15	60	μA
	I_{DD6}	STOP mode			0.1	30	μA
Pull-up resistance	R_L	V_{IN} = 0 V		10	30	100	kΩ

Notes 1. Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped). AV_{REF0} is not included.

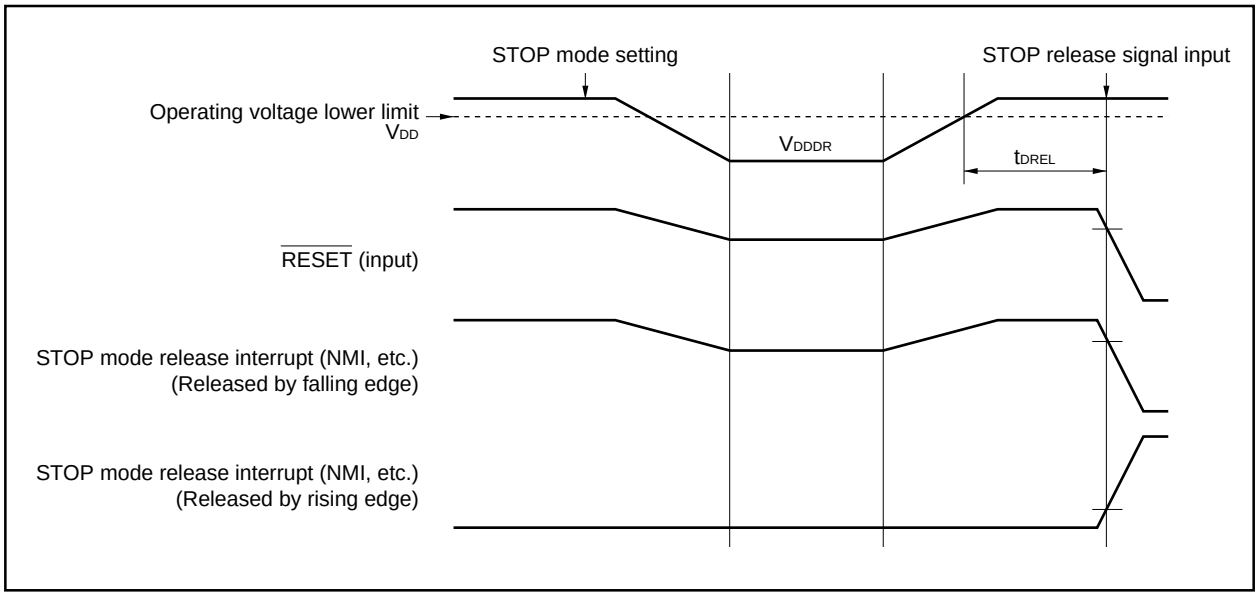
★ **2.** When the capacitance of the capacitor in the oscillator is 15 pF.

Data Retention Characteristics

STOP Mode (T_A = –40 to +85°C)

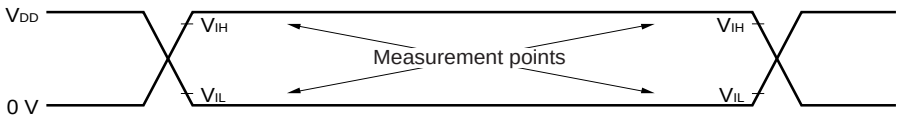
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	2.0		5.5	V
STOP release signal input time	t_{DREL}		0			μs

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

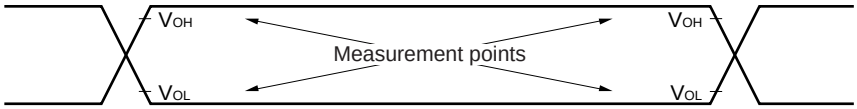


AC Characteristics

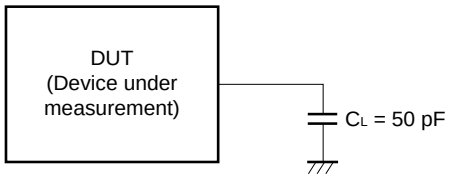
AC Test Input Measurement Points (V_{DD}, AV_{DD}, EV_{DD}, BV_{DD})



AC Test Output Measurement Points



Load Conditions



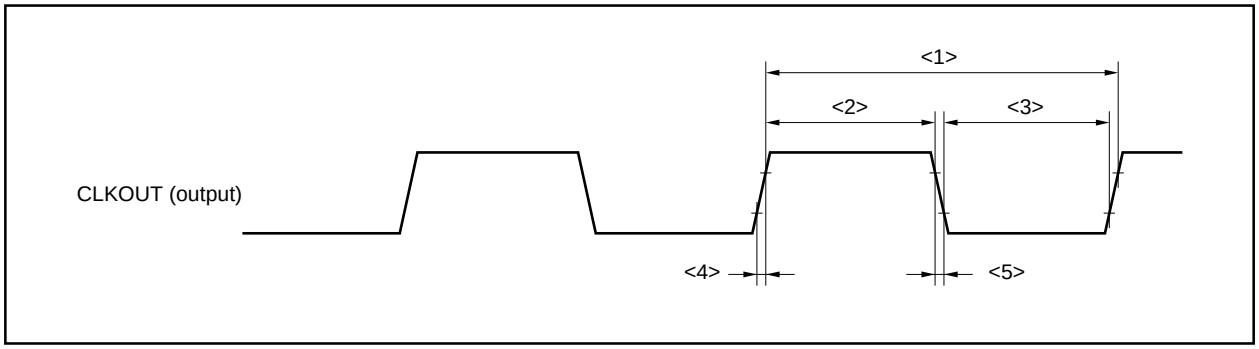
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

CLKOUT Output Timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output cycle	t_{CYK}	<1>		50 ns	30.6 μs	
High-level width	t_{WKH}	<2>	V_{DD} = 4.0 to 5.5 V	t_{CYK}/2 – 17		ns
			V_{DD} = 2.7 to 5.5 V	t_{CYK}/2 – 26		ns
Low-level width	t_{WKL}	<3>	V_{DD} = 4.0 to 5.5 V	t_{CYK}/2 – 17		ns
			V_{DD} = 2.7 to 5.5 V	t_{CYK}/2 – 26		ns
Rise time	t_{KR}	<4>	V_{DD} = 4.0 to 5.5 V		17	ns
			V_{DD} = 2.7 to 5.5 V		26	ns
Fall time	t_{KF}	<5>	V_{DD} = 4.0 to 5.5 V		17	ns
			V_{DD} = 2.7 to 5.5 V		26	ns

Clock Timing



Bus Timing

(1) In multiplex bus mode

(a) CLKOUT asynchronous: In multiplex bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}	<11>		0.5T – 23		ns
Address hold time (from ASTB↓)	t_{HSTA}	<12>		0.5T – 15		ns
Delay time from $\overline{RD}$↓ to address float	t_{FRDA}	<13>			16	ns
Data input setup time from address	t_{SAID}	<14>			(2 + n)T – 40	ns
Data input setup time from $\overline{RD}$↓	t_{SRID}	<15>			(1 + n)T – 25	ns
Delay time from ASTB↓ to $\overline{RD}$, $\overline{WRm}$↓	$t_{DSTRDWR}$	<16>		0.5T – 20		ns
Data input hold time (from $\overline{RD}$↑)	t_{HRDID}	<17>		0		ns
Address output time from $\overline{RD}$↑	t_{DRDA}	<18>		(1 + i)T – 16		ns
Delay time from $\overline{RD}$, $\overline{WRm}$↑ to ASTB↑	$t_{DRDWRST}$	<19>		0.5T – 10		ns
Delay time from $\overline{RD}$↑ to ASTB↓	t_{DRDST}	<20>		(1.5 + i)T – 10		ns
$\overline{RD}$, $\overline{WRm}$ low-level width	t_{WRDWRL}	<21>		(1 + n)T – 10		ns
ASTB high-level width	t_{WSTH}	<22>		T – 25		ns
Data output time from $\overline{WRm}$↓	t_{DWROD}	<23>			20	ns
Data output setup time (to $\overline{WRm}$↑)	t_{SODWR}	<24>		(1 + n)T – 25		ns
Data output hold time (from $\overline{WRm}$↑)	t_{HWROD}	<25>		T – 15		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<26>	n ≥ 1		1.5T – 45	ns
	t_{SAWT2}	<27>			(1.5 + n)T – 45	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<28>	n ≥ 1	(0.5 + n)T		ns
	t_{HAWT2}	<29>		(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	t_{SSTWT1}	<30>	n ≥ 1		T – 32	ns
	t_{SSTWT2}	<31>			(1 + n)T – 32	ns
$\overline{WAIT}$ hold time (from ASTB↓)	t_{HSTWT1}	<32>	n ≥ 1	nT		ns
	t_{HSTWT2}	<33>		(1 + n)T		ns
$\overline{HLDRQ}$ high-level width	t_{WHQH}	<34>		T + 10		ns
$\overline{HLDAK}$ low-level width	t_{WHAL}	<35>		T – 15		ns
Delay time from $\overline{HLDAK}$↑ to bus output	t_{DHAC}	<36>		–40		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	t_{DHQHA1}	<37>			(2n + 7.5)T + 40	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	t_{DHQHA2}	<38>		0.5T	1.5T + 40	ns

Remarks 1. T = 1/f_{CPU} (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. m = 0, 1

4. i: Number of idle states inserted after a read cycle (0 or 1).

5. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to ASTB↓)	t_{SAST}	<11>		0.5T – 42		ns
Address hold time (from ASTB↓)	t_{HSTA}	<12>		0.5T – 30		ns
Delay time from $\overline{RD}$↓ to address float	t_{FRDA}	<13>			32	ns
Data input setup time from address	t_{SAID}	<14>			(2 + n)T – 72	ns
Data input setup time from $\overline{RD}$↓	t_{SRID}	<15>			(1 + n)T – 40	ns
Delay time from ASTB↓ to $\overline{RD}$, $\overline{WRm}$↓	$t_{DSTRDWR}$	<16>		0.5T – 35		ns
Data input hold time (from $\overline{RD}$↑)	t_{HRDID}	<17>		0		ns
Address output time from $\overline{RD}$↑	t_{DRDA}	<18>		(1 + i)T – 32		ns
Delay time from $\overline{RD}$, $\overline{WRm}$↑ to ASTB↑	$t_{DRDWRST}$	<19>		0.5T – 20		ns
Delay time from $\overline{RD}$↑ to ASTB↓	t_{DRDST}	<20>		(1.5 + i)T – 20		ns
$\overline{RD}$, $\overline{WRm}$ low-level width	t_{WRDWRL}	<21>		(1 + n)T – 20		ns
ASTB high-level width	t_{WSTH}	<22>		T–50		ns
Data output time from $\overline{WRm}$↓	t_{DWROD}	<23>			35	ns
Data output setup time (to $\overline{WRm}$↑)	t_{SODWR}	<24>		(1 + n)T – 40		ns
Data output hold time (from $\overline{WRm}$↑)	t_{HWROD}	<25>		T – 30		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<26>	n ≥ 1		1.5T – 80	ns
	t_{SAWT2}	<27>			(1.5 + n)T – 80	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<28>	n ≥ 1	(0.5 + n)T		ns
	t_{HAWT2}	<29>		(1.5 + n)T		ns
$\overline{WAIT}$ setup time (to ASTB↓)	t_{SSTWT1}	<30>	n ≥ 1		T – 60	ns
	t_{SSTWT2}	<31>			(1 + n)T – 60	ns
$\overline{WAIT}$ hold time (from ASTB↓)	t_{HSTWT1}	<32>	n ≥ 1	nT		ns
	t_{HSTWT2}	<33>		(1 + n)T		ns
$\overline{HLDRQ}$ high-level width	t_{WHQH}	<34>		T + 10		ns
$\overline{HLDAK}$ low-level width	t_{WHAL}	<35>		T – 15		ns
Delay time from $\overline{HLDAK}$↑ to bus output	t_{DHAC}	<36>		–80		ns
Delay time from $\overline{HLDRQ}$↓ to $\overline{HLDAK}$↓	t_{DHQHA1}	<37>			(2n + 7.5)T + 70	ns
Delay time from $\overline{HLDRQ}$↑ to $\overline{HLDAK}$↑	t_{DHQHA2}	<38>		0.5T	1.5T + 70	ns

Caution Set the following in accordance with the usage conditions of the CPU operation clock frequency (n = 0 to 3).

- 70 ns < $1/f_{CPU}$ < 84 ns
  Set an address setup wait (ASWn bit = 1).
- 62.5 ns < $1/f_{CPU}$ < 70 ns
  Set an address setup wait (ASWn bit = 1) and address hold wait (AHWn bit = 1).

Remarks 1. T = $1/f_{CPU}$ (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. m = 0, 1

4. i: Number of idle states inserted after a read cycle (0 or 1).

5. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(b) CLKOUT synchronous: In multiplex bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	t_{DKA}	<39>		0	19	ns
Delay time from CLKOUT↑ to address float	t_{FKA}	<40>		0	14	ns
Delay time from CLKOUT↓ to ASTB	t_{DKST}	<41>		0	23	ns
Delay time from CLKOUT↑ to $\overline{RD}$, $\overline{WRm}$	t_{DKRDWR}	<42>		–22	0	ns
Data input setup time (to CLKOUT↑)	t_{SIDK}	<43>		15		ns
Data input hold time (from CLKOUT↑)	t_{HKID}	<44>		0		ns
Data output delay time from CLKOUT↑	t_{DKOD}	<45>			19	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	t_{SWTK}	<46>		15		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	t_{HKWT}	<47>		0		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	t_{SHQK}	<48>		15		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	t_{HKHQ}	<49>		0		ns
Delay time from CLKOUT↑ to bus float	t_{DKF}	<50>			20	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	t_{DKHA}	<51>			20	ns

Remarks 1. m = 0, 1

2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

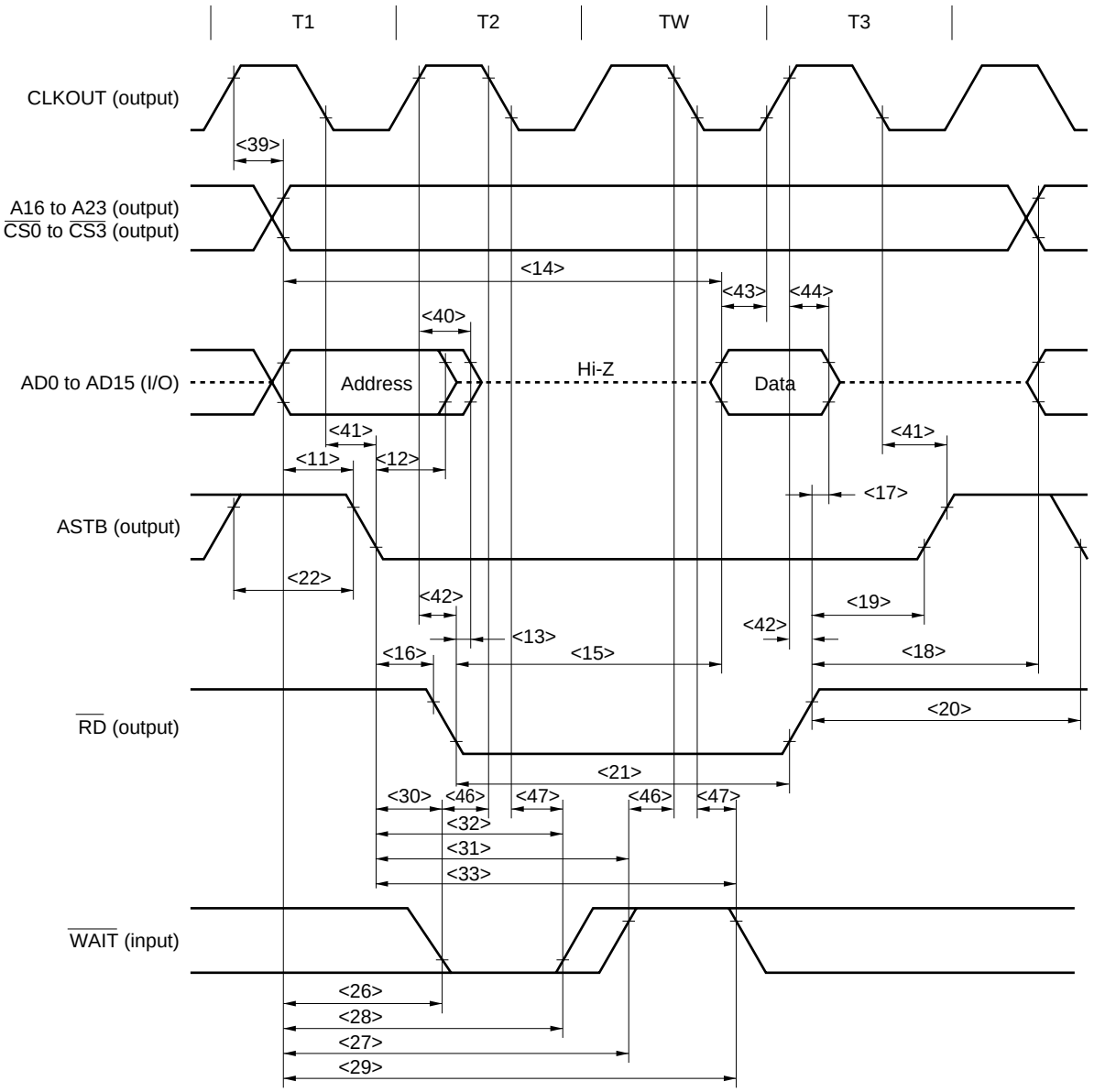
(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address	t_{DKA}	<39>		0	19	ns
Delay time from CLKOUT↑ to address float	t_{FKA}	<40>		0	18	ns
Delay time from CLKOUT↓ to ASTB	t_{DKST}	<41>		0	55	ns
Delay time from CLKOUT↑ to $\overline{RD}$, $\overline{WRm}$	t_{DKRDWR}	<42>		–22	0	ns
Data input setup time (to CLKOUT↑)	t_{SIDK}	<43>		30		ns
Data input hold time (from CLKOUT↑)	t_{HKID}	<44>		0		ns
Data output delay time from CLKOUT↑	t_{DKOD}	<45>			19	ns
$\overline{WAIT}$ setup time (to CLKOUT↓)	t_{SWTK}	<46>		25		ns
$\overline{WAIT}$ hold time (from CLKOUT↓)	t_{HKWT}	<47>		0		ns
$\overline{HLDRQ}$ setup time (to CLKOUT↓)	t_{SHQK}	<48>		25		ns
$\overline{HLDRQ}$ hold time (from CLKOUT↓)	t_{HKHQ}	<49>		0		ns
Delay time from CLKOUT↑ to bus float	t_{DKF}	<50>			40	ns
Delay time from CLKOUT↑ to $\overline{HLDAK}$	t_{DKHA}	<51>			40	ns

Remarks 1. m = 0, 1

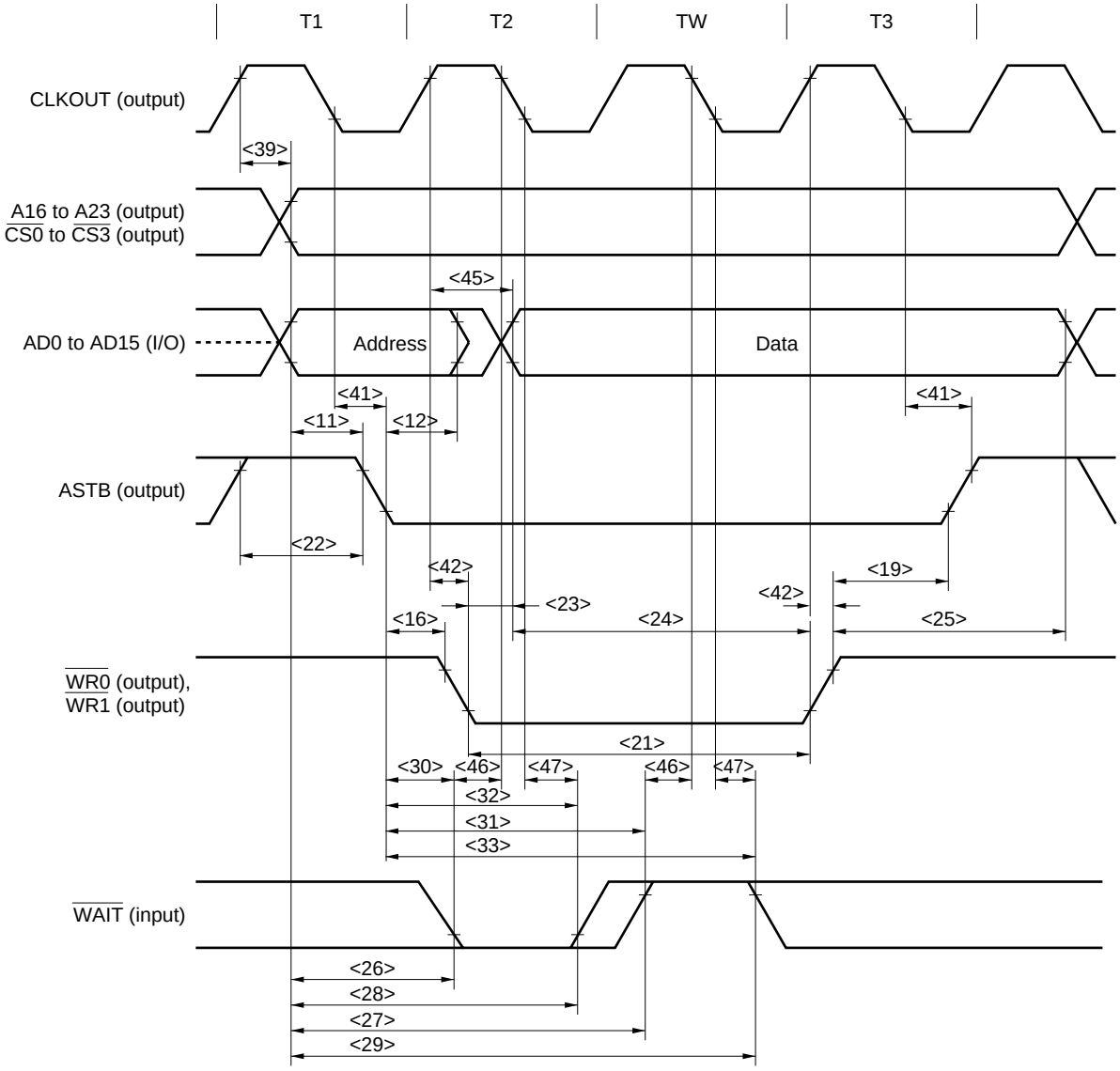
2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

Read Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait): In Multiplex Bus Mode



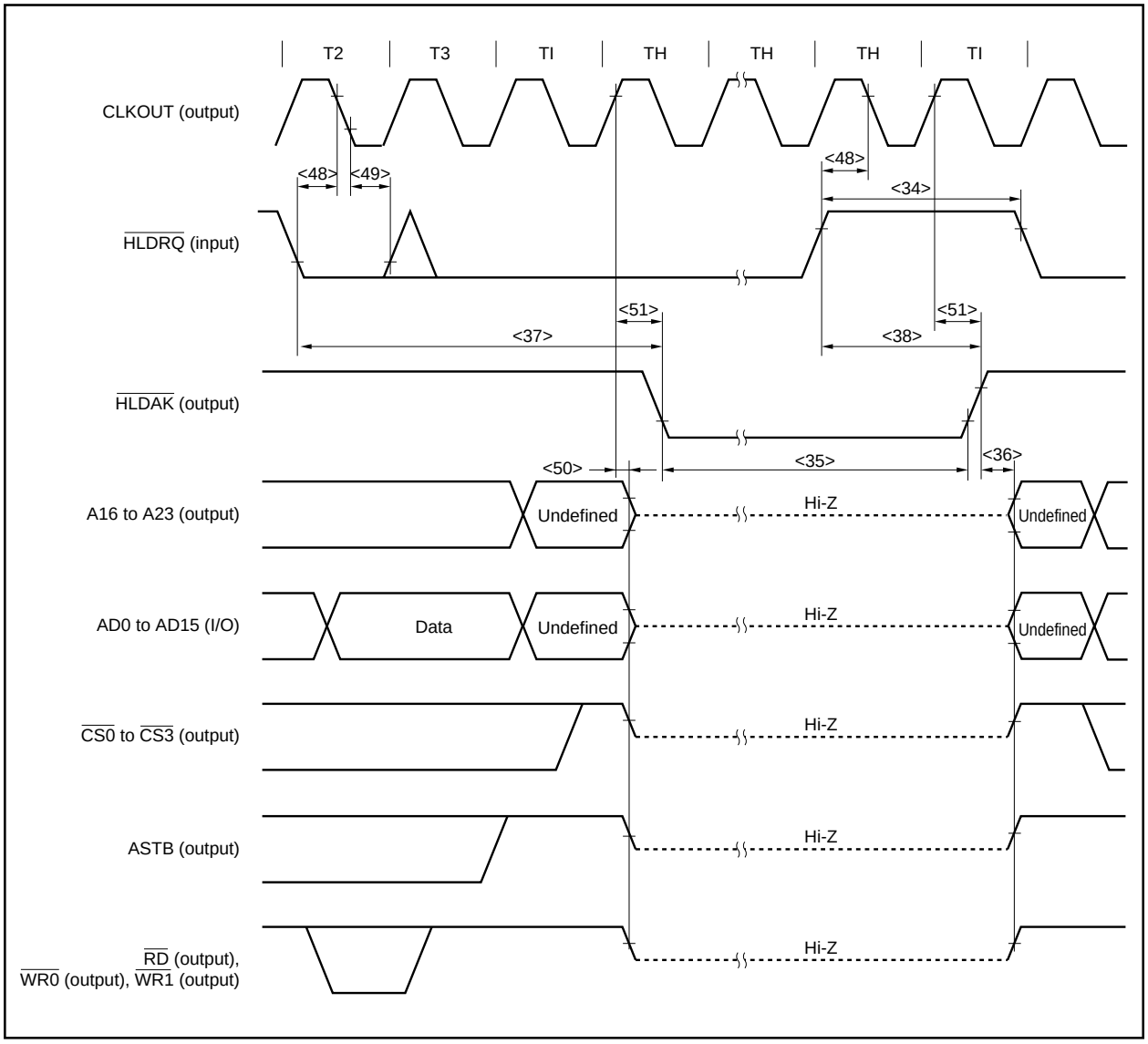
Remark WR0 and WR1 are high level.

Write Cycle (CLKOUT Synchronous/Asynchronous, 1 Wait): In Multiplex Bus Mode



Remarks RD is high level.

★ **Bus Hold: In Multiplex Bus Mode**



(2) In separate bus mode

(a) Read cycle (CLKOUT asynchronous): In separate bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{RD}$↓)	t_{SARD}	<52>		0.5T – 50		ns
Address hold time (from $\overline{RD}$↑)	t_{HARD}	<53>		–13		ns
$\overline{RD}$ low-level width	t_{WRDL}	<54>		(1.5 + n)T – 15		ns
Data setup time (to $\overline{RD}$↑)	t_{SISD}	<55>		30		ns
Data hold time (from $\overline{RD}$↑)	t_{HISD}	<56>		0		ns
Data setup time (to address)	t_{SAID}	<57>			(2 + n)T – 65	ns
$\overline{WAIT}$ setup time (to $\overline{RD}$↓)	t_{SRDWT1}	<58>			0.5T – 32	ns
	t_{SRDWT2}	<59>			(0.5 + n)T – 32	ns
$\overline{WAIT}$ hold time (from $\overline{RD}$↓)	t_{HRDWT1}	<60>		0.5T		ns
	t_{HRDWT2}	<61>		(0.5 + n)T		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<62>			T – 65	ns
	t_{SAWT2}	<63>			(1 + n)T – 65	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<64>		T		ns
	t_{HAWT2}	<65>		(1 + n)T		ns

Cautions 1. The separate bus mode is not supported in the V850ES/KF1.

2. Set the following in accordance with the usage conditions of the CPU operation clock frequency (n = 0 to 3).

- $1/f_{CPU}$ < 100 ns

  Set an address setup wait (ASWn bit = 1).

Remarks 1. T = $1/f_{CPU}$ (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{RD}$↓)	t_{SARD}	<52>		0.5T – 100		ns
Address hold time (from $\overline{RD}$↑)	t_{HARD}	<53>		–26		ns
$\overline{RD}$ low-level width	t_{WRDL}	<54>		(1.5 + n)T – 30		ns
Data setup time (to $\overline{RD}$↑)	t_{SISD}	<55>		60		ns
Data hold time (from $\overline{RD}$↑)	t_{HISD}	<56>		0		ns
Data setup time (to address)	t_{SAID}	<57>			(2 + n)T – 120	ns
$\overline{WAIT}$ setup time (to $\overline{RD}$↓)	t_{SRDWT1}	<58>			0.5T – 50	ns
	t_{SRDWT2}	<59>			(0.5 + n)T – 50	ns
$\overline{WAIT}$ hold time (from $\overline{RD}$↓)	t_{HRDWT1}	<60>		0.5T		ns
	t_{HRDWT2}	<61>		(0.5 + n)T		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<62>			T – 130	ns
	t_{SAWT2}	<63>			(1 + n)T – 130	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<64>		T		ns
	t_{HAWT2}	<65>		(1 + n)T		ns

Cautions 1. The separate bus mode is not supported in the V850ES/KF1.

2. Set the following in accordance with the usage conditions of the CPU operation clock frequency (n = 0 to 3).

- $1/f_{CPU}$ < 200 ns

  Set an address setup wait (ASWn bit = 1).

Remarks 1. T = $1/f_{CPU}$ (f_{CPU}: CPU operating clock frequency)

2. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

3. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(b) Read cycle (CLKOUT synchronous): In separate bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address, CS	t_{DKSA}	<66>		0	35	ns
Data input setup time (to CLKOUT↑)	t_{SISDK}	<67>		15		ns
Data input hold time (from CLKOUT↑)	t_{HKISD}	<68>		0		ns
Delay time from CLKOUT↓↑ to $\overline{RD}$	t_{DKSR}	<69>		0	6	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	t_{SWTK}	<70>		20		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	t_{HKWT}	<71>		0		ns

Caution The separate bus mode is not supported in the V850ES/KF1.

Remark The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address, CS	t_{DKSA}	<66>		0	65	ns
Data input setup time (to CLKOUT↑)	t_{SISDK}	<67>		30		ns
Data input hold time (from CLKOUT↑)	t_{HKISD}	<68>		0		ns
Delay time from CLKOUT↓↑ to $\overline{RD}$	t_{DKSR}	<69>		0	10	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	t_{SWTK}	<70>		40		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	t_{HKWT}	<71>		0		ns

Caution The separate bus mode is not supported in the V850ES/KF1.

Remark The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(c) Write cycle (CLKOUT asynchronous): In separate bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{WRm}$↓)	t_{SAW}	<72>		T – 60		ns
Address hold time (from $\overline{WRm}$↑)	t_{HAW}	<73>		0.5T – 10		ns
$\overline{WRm}$ low-level width	t_{WWRL}	<74>		(0.5 + n)T – 10		ns
Data output time from $\overline{WRm}$↓	t_{DOSDW}	<75>		–5		ns
Data setup time (to $\overline{WRm}$↑)	t_{SOSDW}	<76>		(0.5 + n)T – 20		ns
Data hold time (from $\overline{WRm}$↑)	t_{HOSDW}	<77>		0.5T – 20		ns
Data setup time (to address)	t_{SAOD}	<78>		T – 30		ns
$\overline{WAIT}$ setup time (to $\overline{WRm}$↓)	t_{SWRWT1}	<79>		30		ns
	t_{SWRWT2}	<80>		nT – 30		ns
$\overline{WAIT}$ hold time (from $\overline{WRm}$↓)	t_{HWRWT1}	<81>		0		ns
	t_{HWRWT2}	<82>		nT		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<83>			T – 45	ns
	t_{SAWT2}	<84>			(1 + n)T – 45	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<85>		T		ns
	t_{HAWT2}	<86>		(1 + n)T		ns

Cautions 1. The separate bus mode is not supported in the V850ES/KF1.

2. Set the following in accordance with the usage conditions of the CPU operation clock frequency (n = 0 to 3).

- $1/f_{CPU}$ < 60 ns

  Set an address setup wait (ASWn bit = 1).

Remarks 1. m = 0, 1

2. T = $1/f_{CPU}$ (f_{CPU}: CPU operating clock frequency)

3. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

4. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Address setup time (to $\overline{WRm}$↓)	t_{SAW}	<72>		T – 100		ns
Address hold time (from $\overline{WRm}$↑)	t_{HAW}	<73>		0.5T – 10		ns
$\overline{WRm}$ low-level width	t_{WWRL}	<74>		(0.5 + n)T – 10		ns
Data output time from $\overline{WRm}$↓	t_{DOSDW}	<75>		–5		ns
Data setup time (to $\overline{WRm}$↑)	t_{SOSDW}	<76>		(0.5 + n)T – 35		ns
Data hold time (from $\overline{WRm}$↑)	t_{HOSDW}	<77>		0.5T – 35		ns
Data setup time (to address)	t_{SAOD}	<78>		T – 55		ns
$\overline{WAIT}$ setup time (to $\overline{WRm}$↓)	t_{SWRWT1}	<79>		50		ns
	t_{SWRWT2}	<80>		nT – 50		ns
$\overline{WAIT}$ hold time (from $\overline{WRm}$↓)	t_{HWRWT1}	<81>		0		ns
	t_{HWRWT2}	<82>		nT		ns
$\overline{WAIT}$ setup time (to address)	t_{SAWT1}	<83>			T – 100	ns
	t_{SAWT2}	<84>			(1 + n)T – 100	ns
$\overline{WAIT}$ hold time (from address)	t_{HAWT1}	<85>		T		ns
	t_{HAWT2}	<86>		(1 + n)T		ns

Cautions 1. The separate bus mode is not supported in the V850ES/KF1.

2. Set the following in accordance with the usage conditions of the CPU operation clock frequency (n = 0 to 3).

- $1/f_{CPU}$ < 100 ns

  Set an address setup wait (ASWn bit = 1).

Remarks 1. m = 0, 1

2. T = $1/f_{CPU}$ (f_{CPU}: CPU operating clock frequency)

3. n: Number of wait clocks inserted in the bus cycle.
The sampling timing changes when a programmable wait is inserted.

4. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(d) Write cycle (CLKOUT synchronous): In separate bus mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 4.0 to 5.5 V, 4.0 V ≤ BV_{DD} ≤ V_{DD}, 4.0 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (1/2)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address, CS	t_{DKSA}	<87>		0	35	ns
Data output delay time from CLKOUT↑	t_{DKSD}	<88>		0	10	ns
Delay time from CLKOUT↑↓ to $\overline{WRm}$	t_{DKSW}	<89>		0	10	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	t_{SWTK}	<90>		20		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	t_{HKWT}	<91>		0		ns

Caution The separate bus mode is not supported in the V850ES/KF1.

Remarks 1. m = 0, 1

2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF) (2/2)

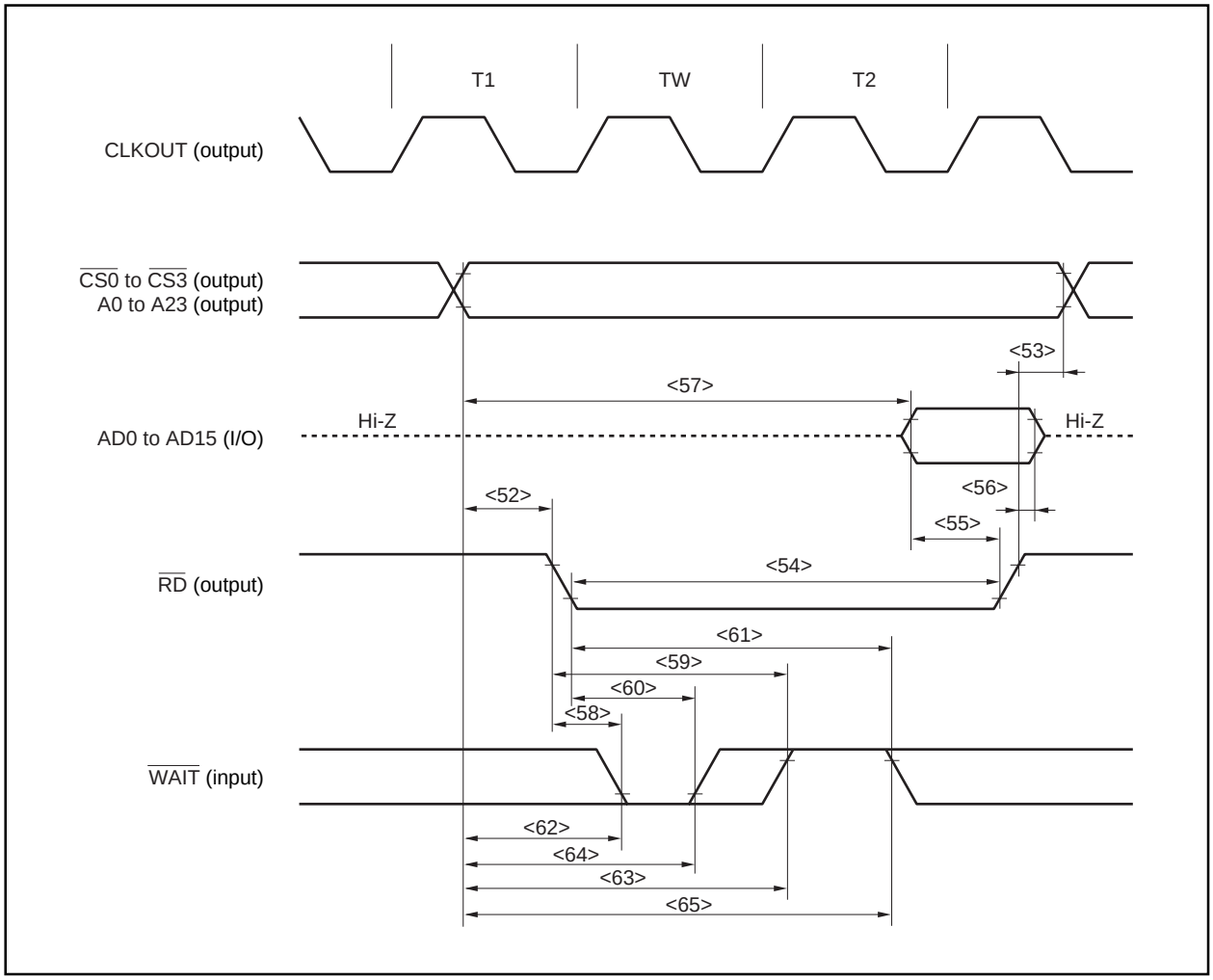
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Delay time from CLKOUT↑ to address, CS	t_{DKSA}	<87>		0	65	ns
Data output delay time from CLKOUT↑	t_{DKSD}	<88>		0	15	ns
Delay time from CLKOUT↑↓ to $\overline{WRm}$	t_{DKSW}	<89>		0	15	ns
$\overline{WAIT}$ setup time (to CLKOUT↑)	t_{SWTK}	<90>		40		ns
$\overline{WAIT}$ hold time (from CLKOUT↑)	t_{HKWT}	<91>		0		ns

Caution The separate bus mode is not supported in the V850ES/KF1.

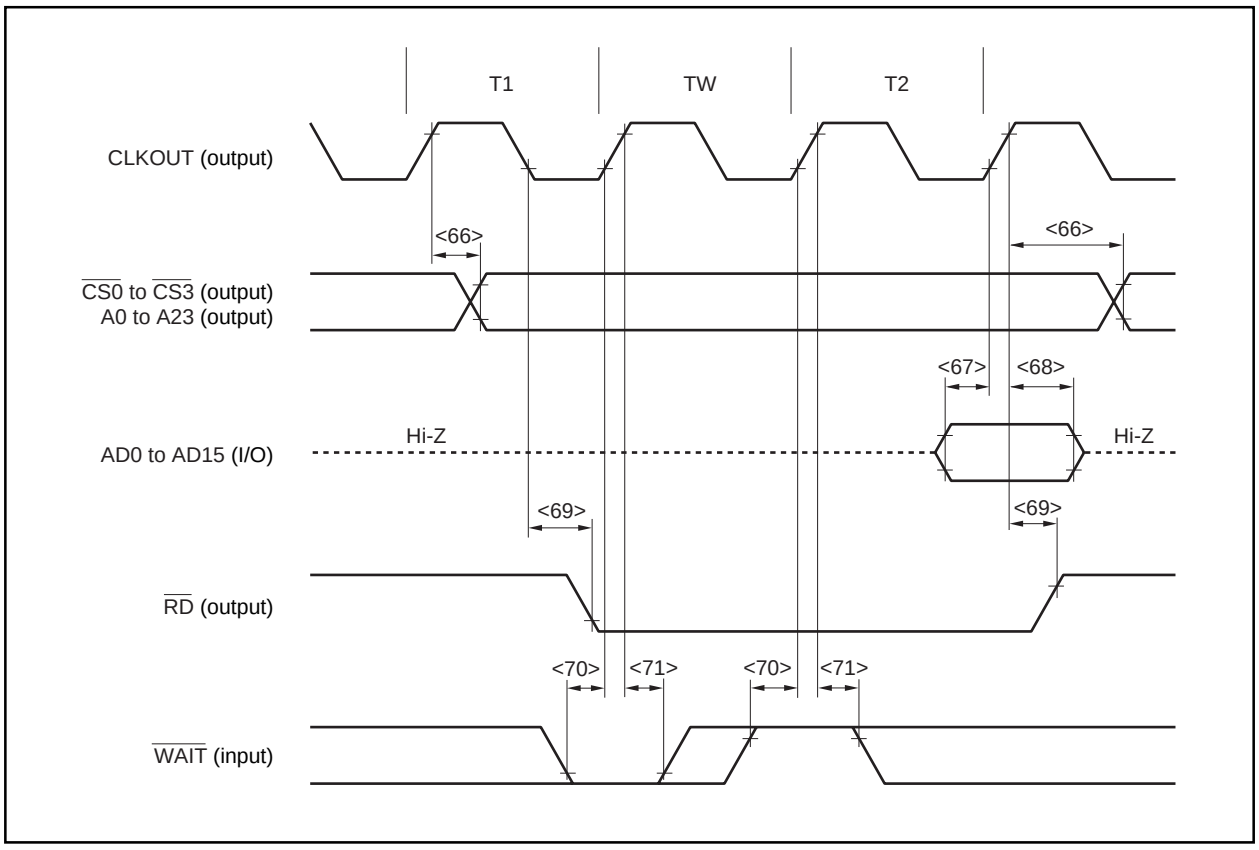
Remarks 1. m = 0, 1

2. The values in the above specifications are values for when clocks with a 1:1 duty ratio are input from X1.

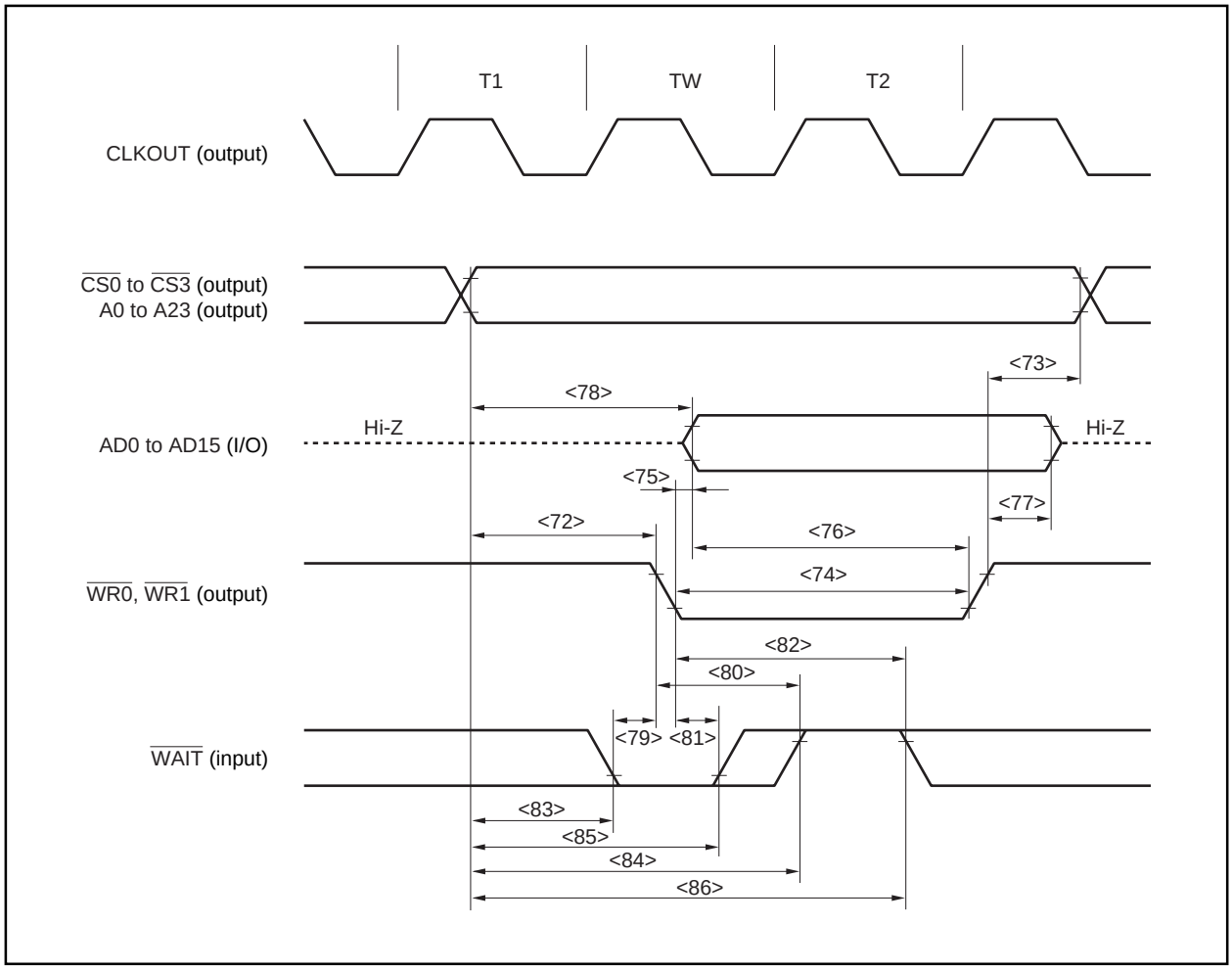
Read Cycle (CLKOUT Asynchronous, 1 Wait): In Separate Bus Mode



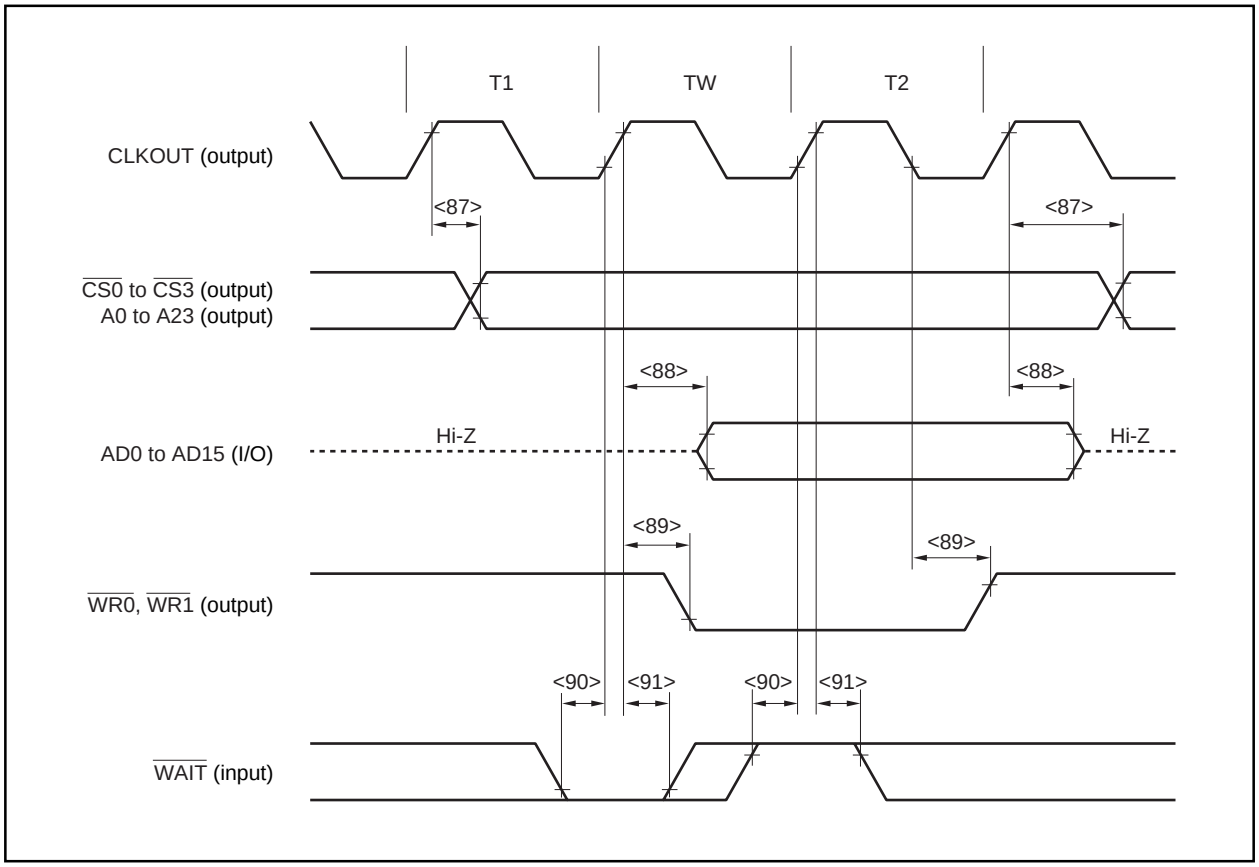
Read Cycle (CLKOUT Synchronous, 1 Wait): In Separate Bus Mode



Write Cycle (CLKOUT Asynchronous, 1 Wait): In Separate Bus Mode



Write Cycle (CLKOUT Synchronous, 1 Wait): In Separate Bus Mode



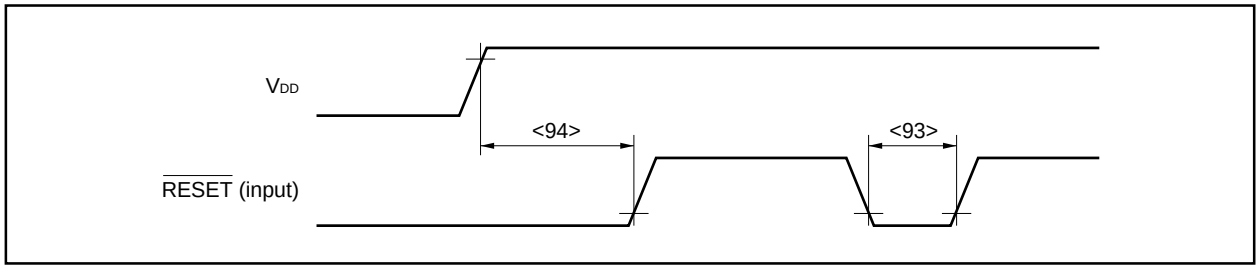
Basic Operation

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

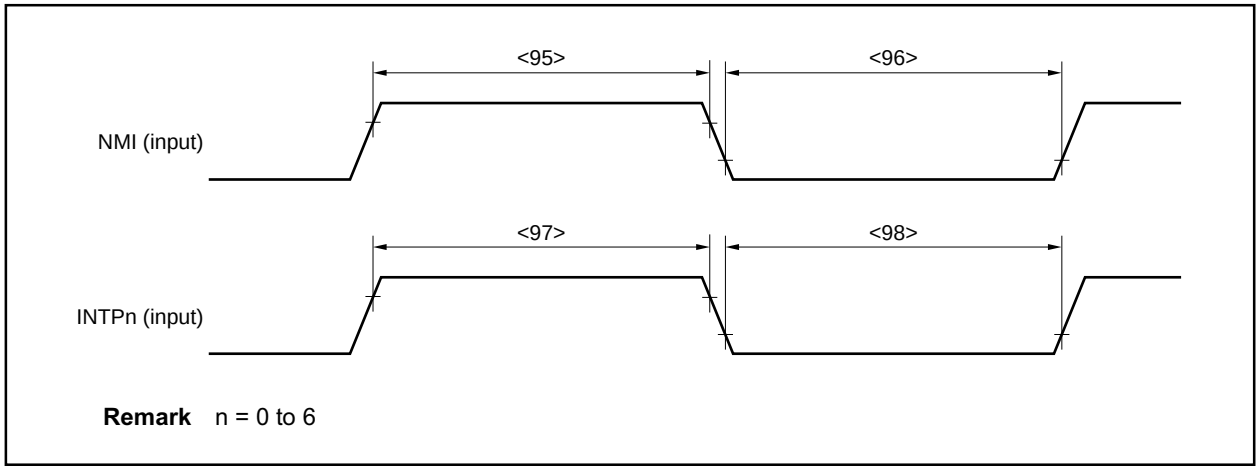
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	t_{WRSL1}	<93>	Reset in power-on status	2		ns
	t_{WRSL2}	<94>	Power-on-reset when REGC = V_{DD}	2		μs
			Power-on-reset when REGC = Capacity	10		μs
NMI high-level width	t_{WNIH}	<95>	Analog noise elimination	1		μs
NMI low-level width	t_{WNIL}	<96>	Analog noise elimination	1		μs
★ INTPn high-level width	t_{WITH}	<97>	n = 0 to 6 (analog noise elimination)	600		ns
★ INTPn low-level width	t_{WITL}	<98>	n = 0 to 6 (analog noise elimination)	600		ns

Remark T = 1/f_{XX}

Reset



Interrupt



Remark n = 0 to 6

Timer Timing

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TI0n high-level width	t_{TI0H}	REGC = V_{DD} = 5 V ±10%	2/fsam + 0.1[Note]		ns
					ns
TI0n low-level width	t_{TI0L}	REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	2/fsam + 0.2[Note]		ns
					ns
TI50 high-level width	t_{TI5H}	REGC = V_{DD} = 5 V ±10%	50		ns
TI51 low-level width	t_{TI5L}	REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	100		ns

Note f_{sam} = Timer count clock
However, f_{sam} = f_{XX}/4 when the TI0n valid edge is selected as the timer count clock.

Remark V850ES/KF1: n = 00, 01, 10, 11
V850ES/KG1: n = 00, 01, 10, 11, 20, 21, 30, 31
V850ES/KJ1: n = 00, 01, 10, 11, 20, 21, 30, 31, 40, 41, 50, 51

★ **UART Timing**

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transmit rate				312.5	kbps
ASCK0 cycle time		REGC = V_{DD} = 5 V ±10%		12	MHz
		REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V		6	MHz

CSI0 Timing

(1) Master mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{KCY1}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	200		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	400		ns
$\overline{SCK0n}$ high-/low-level width	t_{KH1}, t_{KL1}	<100>		t_{KCY1}/2 – 30		ns
SI0n setup time (to $\overline{SCK0n}$↑)	t_{SIK1}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	50		ns
SI0n hold time (from $\overline{SCK0n}$↑)	t_{KSI1}	<102>	REGC = V_{DD} = 5 V ±10%	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	50		ns
Delay time from $\overline{SCK0n}$↓ to SO0n output	t_{KSO1}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		30	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V		60	ns

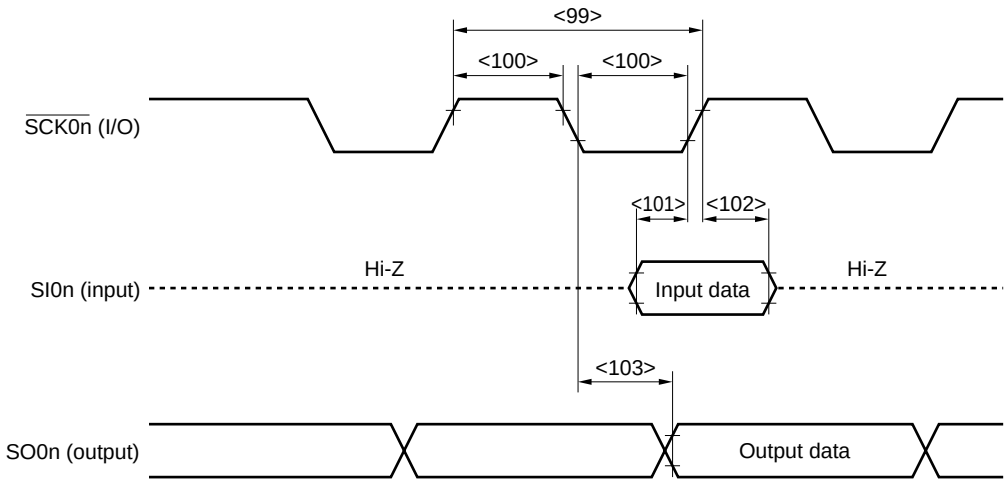
Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

(2) Slave mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{KCY2}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	200		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	400		ns
$\overline{SCK0n}$ high-/low-level width	t_{KH2}, t_{KL2}	<100>	REGC = V_{DD} = 4.0 to 5.5 V	45		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	90		ns
SI0n setup time (to $\overline{SCK0n}$↑)	t_{SIK2}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	60		ns
SI0n hold time (from $\overline{SCK0n}$↑)	t_{KSI2}	<102>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	60		ns
Delay time from $\overline{SCK0n}$↓ to SO0n output	t_{KSO2}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		50	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V		100	ns

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)



Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

CSIA Timing

(1) Master mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKAn}$ cycle time	t_{KCY3}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	500		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	1000		ns
$\overline{SCKAn}$ high-/low-level width	t_{KH3}, t_{KL3}	<100>		$t_{KCY3}/2 - 30$		ns
SIAn setup time (to $\overline{SCKAn}$↑)	t_{SIK3}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	60		ns
SIAn hold time (from $\overline{SCKAn}$↑)	t_{KSI3}	<102>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	60		ns
Delay time from $\overline{SCKAn}$↓ to SOAn output	t_{KSO3}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		30	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V		60	ns

Remark n = 0 (V850ES/KF1), n = 0, 1 (V850ES/KG1, V850ES/KJ1)

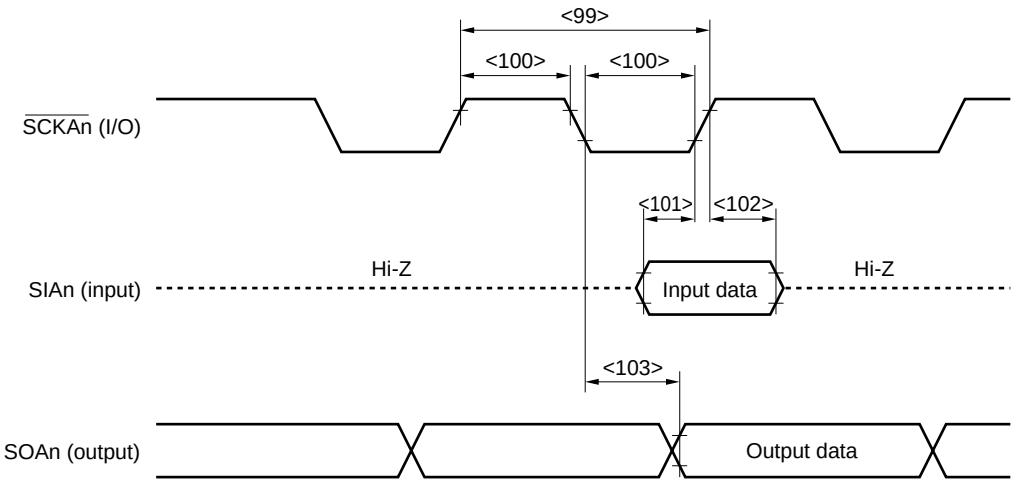
(2) Slave mode

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKAn}$ cycle time	t_{KCY4}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	840		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	1700		ns
$\overline{SCKAn}$ high-/low-level width	t_{KH4}, t_{KL4}	<100>		$t_{KCY4}/2 - 30$		ns
SIAn setup time (to $\overline{SCKAn}$↑)	t_{SIK4}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	50		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	100		ns
SIAn hold time (from $\overline{SCKAn}$↑)	t_{KSI4}	<102>	REGC = V_{DD} = 4.0 to 5.5 V	50		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V	100		ns
Delay time from $\overline{SCKAn}$↓ to SOAn output	t_{KSO4}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		$t_{CY} \times 2 + 30$ Note	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 2.7 to 5.5 V		$t_{CY} \times 2 + 60$ Note	ns

Note t_{CY}: Internal clock output cycle
f_{XX} (CKSAn1 = 0, CKSAn0 = 0), $f_{XX}/2$ (CKSAn1 = 0, CKSAn0 = 1)
$f_{XX}/2^2$ (CKSAn1 = 1, CKSAn0 = 0), $f_{XX}/2^3$ (CKSAn1 = 1, CKSAn0 = 1)

Remark n = 0 (V850ES/KF1), n = 0, 1 (V850ES/KG1, V850ES/KJ1)



Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

I^2C Bus Mode (Y Products (Products with On-Chip I^2C) Only)

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter		Symbol		Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLn clock frequency		f_{CLK}		0	100	0	400	kHz
Bus free time (Between start and stop conditions)		t_{BUF}	<104>	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	<105>	4.0	–	0.6	–	μs
SCLn clock low-level width		t_{LOW}	<106>	4.7	–	1.3	–	μs
SCLn clock high-level width		t_{HIGH}	<107>	4.0	–	0.6	–	μs
Setup time for start/restart conditions		$t_{SU:STA}$	<108>	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	<109>	5.0	–	–	–	μs
	I^2C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	<110>	250	–	100[Note 4]	–	ns
SDAn and SCLn signal rise time		t_R	<111>	–	1000	20 + 0.1Cb[Note 5]	300	ns
SDAn and SCLn signal fall time		t_F	<112>	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	<113>	4.0	–	0.6	–	μs
Pulse width of spike suppressed by input filter		t_{SP}	<114>	–	–	0	50	ns
Capacitance load of each bus line		Cb		–	400	–	400	pF

Notes 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time internally for the SDAn signal (at $V_{IHmin.}$ of SCLn signal) in order to occupy the undefined area at the falling edge of SCLn.

3. If the system does not extend the SCLn signal low hold time (t_{LOW}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

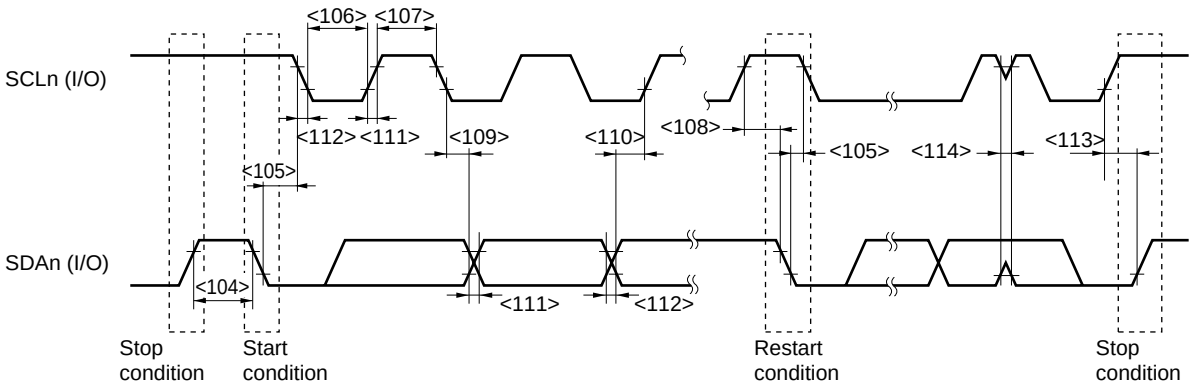
4. The high-speed mode I^2C bus can be used in the normal-mode I^2C bus system. In this case, set the high-speed mode I^2C bus so that it meets the following conditions.

- If the system does not extend the SCLn signal's low state hold time:
  $t_{SU:DAT} \geq 250$ ns
- If the system extends the SCLn signal's low state hold time:
  Transmit the following data bit to the SDAn line prior to the SCLn line release ($t_{Rmax.}$ + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns: Normal mode I^2C bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

I^2C Bus Mode (Y Products (Products with On-Chip I^2C) Only)



Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

A/D Converter

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note 1]		4.0 ≤ AV_{REF0} ≤ 5.5 V		±0.2	±0.4	%FSR
		2.7 ≤ AV_{REF0} ≤ 4.0 V		±0.3	±0.6	%FSR
Conversion time	t_{CONV}	4.0 ≤ AV_{REF0} ≤ 5.5 V	14		100	μs
		2.7 ≤ AV_{REF0} ≤ 4.0 V	17		100	μs
Zero-scale error[Note 1]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±0.4	%FSR
		2.7 ≤ AV_{REF0} ≤ 4.0 V			±0.6	%FSR
Full-scale error[Note 1]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±0.4	%FSR
		2.7 ≤ AV_{REF0} ≤ 4.0 V			±0.6	%FSR
Non-linearity error[Note 2]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±2.5	LSB
		2.7 ≤ AV_{REF0} ≤ 4.0 V			±4.5	LSB
Differential linearity error[Note 2]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±1.5	LSB
		2.7 ≤ AV_{REF0} ≤ 4.0 V			±2.0	LSB
Analog input voltage	V_{IAN}		0		AV_{REF0}	V
AV_{REF0} current	IA_{REF0}	When using A/D converter		1.0	2.0	mA
		When not using A/D converter		1.0	10	μA

Notes 1. Excluding quantization error (±0.05%FSR).

2. Excluding quantization error (±0.5LSB).

Remark LSB: Least Significant Bit
FSR: Full Scale Range

D/A Converter (V850ES/KG1, V850ES/KJ1 only)

(T_A = –40 to +85°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Overall error[Notes 1, 2]		Load condition = 2 MΩ				1.2	%FSR
		Load condition = 4 MΩ				0.8	%FSR
		Load condition = 10 MΩ				0.6	%FSR
Settling time[Notes 1, 2]		C = 30 pF	V_{DD} = 4.5 to 5.5 V			10	μs
			V_{DD} = 2.7 to 4.5 V			15	μs
Output resistance[Note 3]	R_O	Output data 55H			8		kΩ
AV_{REF1} current[Note 4]	IAV_{REF1}	During D/A conversion			1.5	3.0	mA
		When D/A conversion stopped			1.0	10	μA

Notes 1. Excluding quantization error (±0.2%FSR).

2. R is the D/A converter output pin load resistance, and C is the D/A converter output pin load capacitance.

3. Value of 1 channel of D/A converter

4. Value of 2 channels of D/A converter

Flash Memory Programming Characteristics

(T_A = +10 to +40°C, V_{DD} = EV_{DD} = AV_{REF0} = 2.7 to 5.5 V, 2.7 V ≤ BV_{DD} ≤ V_{DD}, 2.7 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

(1) Basic characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Programming operation frequency			2		10	MHz
V_{PP} supply voltage	V_{PP2}	During flash memory programming	9.7	10.0	10.3	V
V_{DD} supply current	I_{DD}	When V_{PP} = V_{PP2}, f_{XX} = 10 MHz, V_{DD} = 5.5 V			60	mA
V_{PP} supply current	I_{PP}	When V_{PP} = V_{PP2}			100	mA
Step erase time	t_{ER}	**Note 1**	0.196	0.2	0.204	s
Overall erase time	t_{ERA}	When step erase time = 0.2 s, **Note 2**			20	s/area
Writeback time	t_{WB}	**Note 3**	4.9	5.0	5.1	ms
Number of writebacks	C_{WB}	When writeback time = 1 ms, **Note 4**			100	Times
Number of erases/writebacks	C_{ERWB}				16	Times
Step write time	t_{WR}	**Note 5**	49	50	51	μs
Overall write time per word	t_{WRW}	When step write time = 50 μs (1 word = 4 byte), **Note 6**	49		510	μs/word
Number of rewrites per area	C_{ERWR}	1 erase + 1 write after erase = 1 rewrite, **Note 7**	20			Count/area

Notes 1. The recommended setting value of the step erase time is 0.2 s.

2. The prewrite time prior to erasure and the erase verify time (writeback time) are not included.

3. The recommended setting value of the writeback time is 5.0 ms.

4. Writeback is executed once by the issuance of the writeback command. Therefore, the retry count must be the maximum value minus the number of commands issued.

5. The recommended setting value of the step writing time is 50 μs.

6. 100 μs is added to the actual writing time per word. The internal verify time during and after the writing is not included.

7. When writing initially to shipped products, it is counted as one rewrite for both “erase to write” and “write only”.

Example (P: Write, E: Erase)

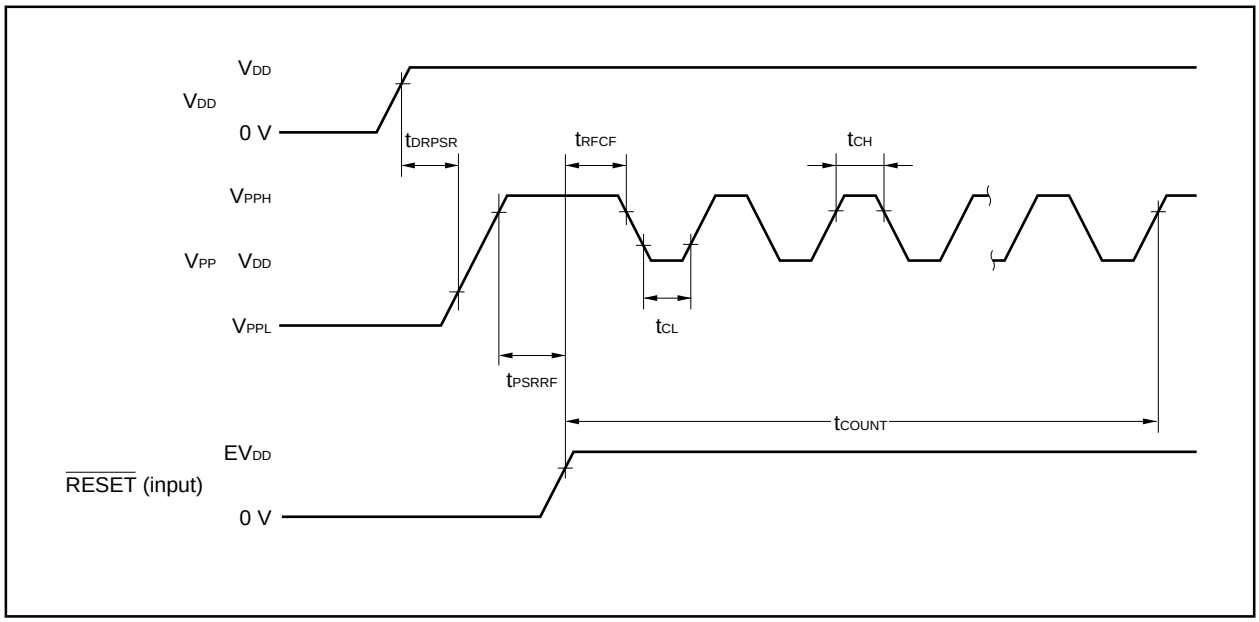
Shipped product ⟶P→E→P→E→P: 3 rewrites

Shipped product → E→P→E→P→E→P: 3 rewrites

(2) Serial write operation characteristics

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Setup time from $V_{DD}\uparrow$ to $V_{PP}\uparrow$	t_{DPRSR}		15			μs
Setup time from $V_{PP}\uparrow$ to RESET↑	t_{PSRRF}		10			μs
Count start time from RESET↑ to V_{PPH}	t_{RFOF}		2			μs
Count complete time	t_{COUNT}				20	ms
V_{PP} counter high-/low-level width	t_{CH}/t_{CL}		8			μs
V_{PP} pulse low-level input voltage	V_{PPL}		$0.8V_{DD}$		$1.2V_{DD}$	V
V_{PP} pulse high-level input voltage	V_{PPH}		9.7	10.0	10.3	V

Flash Write Mode Setting Timing



★ CHAPTER 27 ELECTRICAL SPECIFICATIONS (SPECIAL GRADE (A1) PRODUCTS)

Special grade (A1) products are as follows.

V850ES/KF1:
- μPD703208(A1)
- μPD703208Y(A1)
- μPD703209(A1)
- μPD703209Y(A1)
- μPD703210(A1)
- μPD703210Y(A1)

V850ES/KG1:
- μPD703212(A1)
- μPD703212Y(A1)
- μPD703213(A1)
- μPD703213Y(A1)
- μPD703214(A1)
- μPD703214Y(A1)

V850ES/KJ1:
- μPD703216(A1)
- μPD703216Y(A1)
- μPD703217(A1)
- μPD703217Y(A1)

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	BV_{DD}	$BV_{DD} \leq V_{DD}$	−0.3 to V_{DD} + 0.3 Note 1	V
	EV_{DD}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	AV_{REF0}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	AV_{REF1}	$AV_{REF1} \leq V_{DD}$ (D/A output mode) $AV_{REF1} = AV_{REF0} = V_{DD}$ (port mode)	−0.3 to V_{DD} + 0.3 Note 1	V
Input voltage	V_{I1}	P00 to P06, P30 to P35, P38, P39, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915, $\overline{\text{RESET}}$	−0.3 to EV_{DD} + 0.3 Note 1	V
	V_{I2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7	−0.3 to BV_{DD} + 0.3 Note 1	V
	V_{I3}	P10, P11	−0.3 to AV_{REF1} + 0.3 Note 1	V
	V_{I4}	P36, P37, P614, P615	−0.3 to +13 Note 2	V
	V_{I5}	X1, X2, XT1, XT2	−0.3 to V_{DD} + 0.3 Note 1	V
Analog input voltage	V_{IAN}	P70 to P715	−0.3 to AV_{REF0} + 0.3 Note 1	V

Notes 1. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

2. When pull-up is not specified by a mask option. The same as V_{I1} when pull-up is specified.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I_{OL} Note	P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915, PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7	Per pin	16	mA
		P36 to P39, P614, P615		24	mA
		P00 to P06, P30 to P39, P40 to P42	Total of all pins: 56 mA	28	mA
		P50 to P55, P60 to P615, P80, P81, P90 to P915		28	
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7	Total of all pins: 56 mA	28	mA
		PDL0 to PDL15, PDH0 to PDH7		28	mA
Output current, high	I_{OH} Note	Per pin		−8	mA
		P00 to P06, P30 to P35, P40 to P42	Total of all pins: −48 mA	−24	
		P50 to P55, P60 to P613, P80, P81, P90 to P915		−24	mA
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7	Total of all pins: −48 mA	−24	mA
		PDL0 to PDL15, PDH0 to PDH7		−24	mA
		P10, P11	Per pin	−8	
Operating ambient temperature	T_A			−40 to +110	°C
Storage temperature	T_{stg}			−65 to +150	°C

Note In the V850ES/KF1, the specifications of the total of all pins for I_{OL} and I_{OH} are as follows since BV_{DD} system pins do not exist.

I_{OL}	Total of pins: 56 mA	P00 to P06, P30 to P35, P38, P39, P40 to P42	28	mA
		P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL15	28	mA
I_{OH}	Total of pins: −48 mA	P00 to P06, P30 to P35, P40 to P42	−24	mA
		P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL15	−24	mA

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

3. The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

In the V850ES/KF1, the specification of V_{I2} is the same as that of the V_{I1} since the BV_{DD} pin does not exist.

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

Capacitance (T_A = 25°C, V_{DD} = EV_{DD} = AV_{REF0} = BV_{DD} = AV_{REF1} = V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_X = 1 MHz Unmeasured pins returned to 0 V	P70 to P715			15	pF
I/O capacitance	C_{IO}		**Note**			15	pF
			P36 to P39, P614, P615			20	pF

Note P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915, PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

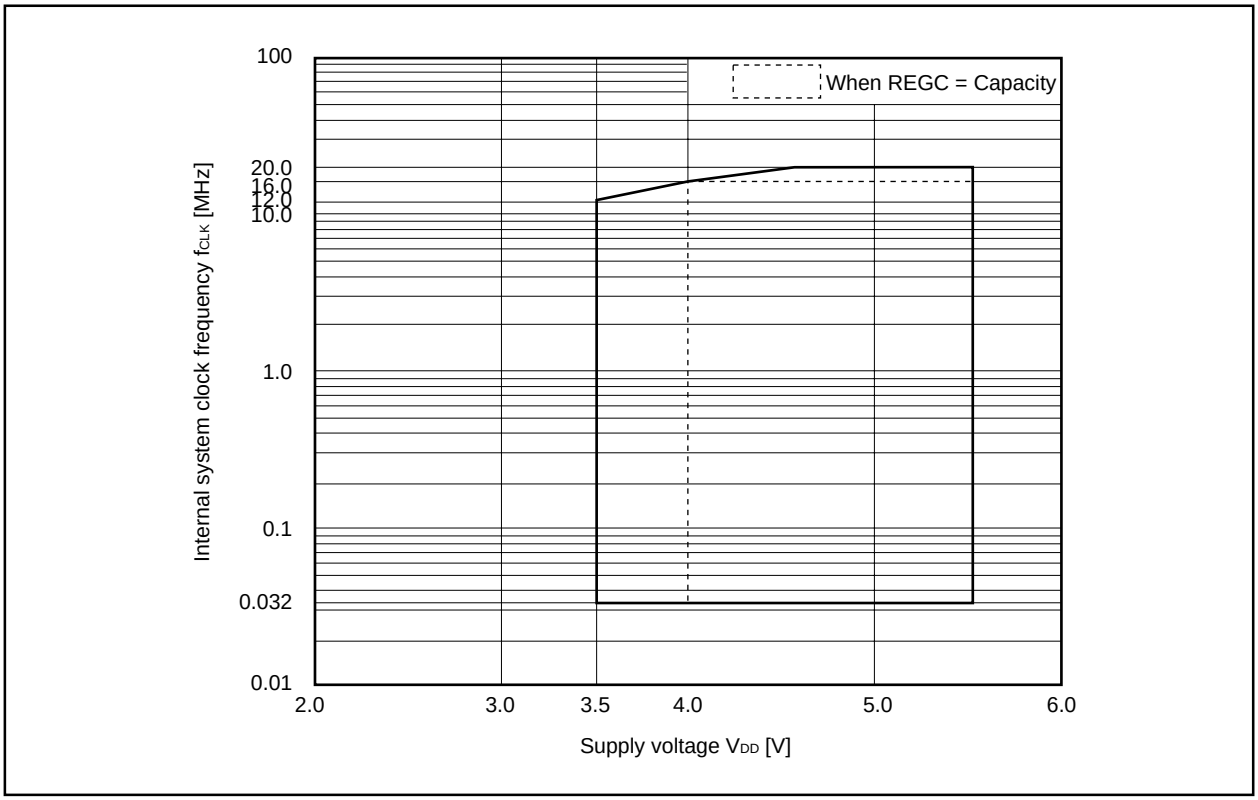
P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

Operating Conditions

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	REGC = V_{DD} = 5 V ±10% In PLL mode (OSC = 2 to 5 MHz)	0.25		20	MHz
		REGC = Capacity, V_{DD} = 4.0 to 5.5 V In PLL mode (OSC = 2 to 4 MHz)	0.25		16	MHz
		REGC = V_{DD} 3.5 to 5.5 V In PLL mode (OSC = 2 to 3 MHz)	0.25		12	MHz
		REGC = V_{DD} = 3.5 to 5.5 V	0.0625		10	MHz
		REGC = V_{DD} = 3.5 to 5.5 V, operating with subclock		32.768		kHz

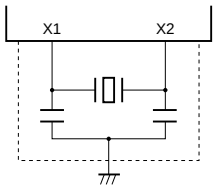
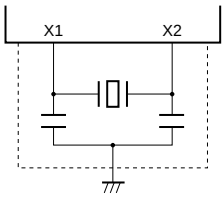
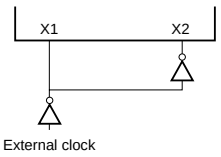
Internal System Clock Frequency vs. Supply Voltage



PLL Characteristics (T_A = –40 to +110°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_x		2		5	MHz
Output frequency	f_{xx}		8		20	MHz
Lock time	t_{PLL}	After V_{DD} reaches MIN.: 3.5 V			200	μs

Main Clock Oscillator Characteristics (T_A = –40 to +110°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		2		10	MHz
		Oscillation stabilization timeNote 2	After reset is released		$2^{15}/f_X$		s
			After STOP mode is released		**Note 3**		s
Crystal resonator		Oscillation frequency (f_X)Note 1		2		10	MHz
		Oscillation stabilization timeNote 2	After reset is released		$2^{15}/f_X$		s
			After STOP mode is released		**Note 3**		s
External clock		X1, X2 input frequency (f_X)	REGC = V_{DD} Duty = 50% ±5%	2		10	MHz

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize the resonator after reset or STOP mode is released.

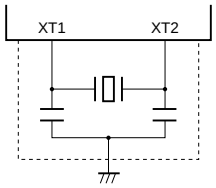
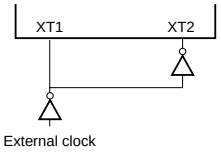
3. The value differs depending on the OSTS register settings.

Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

Subclock Oscillator Characteristics (T_A = –40 to +110°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2			10		s
External clock		XT1 input frequency (f_{XT})Note 1 Duty = 50% ±5%	REGC = V_{DD}	32		35	kHz

Notes 1. Indicates only oscillator characteristics.

2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.5 V) to when the crystal resonator stabilizes.

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

DC Characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (1/4)

Parameter	Symbol	Conditions		MAX.	Unit
Output current, high	I_{OH1}	Per pin for P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915		–4.0	mA
		Total of P00 to P06, P30 to P35, P40 to P42	EV_{DD} = 4.0 to 5.5 V	–24	mA
			EV_{DD} = 3.5 to 5.5 V	–12	mA
		Total of P50 to P55, P60 to P613, P80, P81, P90 to P915	EV_{DD} = 4.0 to 5.5 V	–24	mA
			EV_{DD} = 3.5 to 5.5 V	–12	mA
	I_{OH2}	Per pin for PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7, PDH0 to PDH7, PDL0 to PDL15		–4.0	mA
		Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7	EV_{DD} = 4.0 to 5.5 V	–24	mA
			EV_{DD} = 2.7 to 5.5 V	–12	mA
		Total of PDL0 to PDL15, PDH0 to PDH7	EV_{DD} = 4.0 to 5.5 V	–24	mA
			EV_{DD} = 2.7 to 5.5 V	–12	mA
Output current, low	I_{OL1}	Per pin for P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915		8	mA
		Per pin for P36 to P39	EV_{DD} = 4.0 to 5.5 V	12	mA
			EV_{DD} = 3.5 to 5.5 V	6.4	mA
		Per pin for P614, P615	EV_{DD} = 4.0 to 5.5 V	8	mA
			EV_{DD} = 3.5 to 5.5 V	4	mA
		Total of P00 to P06, P30 to P37, P40 to P42		24	mA
		Total of P38, P39, P50 to P55, P60 to P615, P80, P81, P90 to P915		24	mA
	I_{OL2}	Per pin for PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7, PDH0 to PDH7, PDL0 to PDL15		8	mA
		Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7		24	mA
		Total of PDL0 to PDL15, PDH0 to PDH7		24	mA

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

DC Characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (2/4)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	**Note 1**	0.7EV_{DD}		EV_{DD}	V
	V_{IH2}	**Note 2**	0.8EV_{DD}		EV_{DD}	V
	V_{IH3}	**Note 3**	0.7BV_{DD}		BV_{DD}	V
	V_{IH4}	P70 to P715	0.7AV_{REF0}		AV_{REF0}	V
	V_{IH5}	P10, P11 Note 4	0.7AV_{REF1}		AV_{REF1}	V
	V_{IH6}	P36, P37, P614, P615	0.7EV_{DD}		12 Note 5	V
	V_{IH7}	X1, X2, XT1, XT2	EV_{DD} – 0.5		EV_{DD}	V
Input voltage, low	V_{IL1}	**Note 1**	EV_{SS}		0.3EV_{DD}	V
	V_{IL2}	**Note 2**	EV_{SS}		0.2EV_{DD}	V
	V_{IL3}	**Note 3**	BV_{SS}		0.3BV_{DD}	V
	V_{IL4}	P70 to P715	AV_{SS}		0.3AV_{REF0}	V
	V_{IL5}	P10, P11 Note 4	AV_{SS}		0.3AV_{REF1}	V
	V_{IL6}	P36, P37, P614, P615	EV_{SS}		0.3EV_{DD}	V
	V_{IL7}	X1, X2, XT1, XT2	EV_{SS}		0.4	V

Notes 1. P00, P01, P30, P41, P60 to P65, P67, P611, P98, P911 and their alternate-function pins.

2. $\overline{\text{RESET}}$, P02 to P06, P31 to P35, P38, P39, P40, P42, P50 to P55, P66, P68 to P610, P612, P613, P80, P81, P90 to P97, P99, P910, P912 to P915 and their alternate-function pins.

3. PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7 and their alternate-function pins.

4. When used as port pins, set AV_{REF1} = AV_{REF0} = V_{DD}.

5. When pull-up is not specified by a mask option. EV_{DD} when pull-up is specified.

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

DC Characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (3/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	**Note 1**	I_{OH} = –1.6 mA, EV_{DD} = 4.0 to 5.5 V	EV_{DD} – 1.0		EV_{DD}	V
		Note 2	I_{OH} = –0.88 mA, EV_{DD} = 3.5 to 5.5 V	EV_{DD} – 0.5		EV_{DD}	V
	V_{OH2}	**Note 3**	I_{OH} = –1.6 mA, EV_{DD} = 4.0 to 5.5 V	BV_{DD} – 1.0		BV_{DD}	V
		Note 4	I_{OH} = –0.88 mA, EV_{DD} = 3.5 to 5.5 V	BV_{DD} – 0.5		BV_{DD}	V
	V_{OH3}	P10, P11[Note 5]	I_{OH} = –1.6 mA	AV_{REF1} – 1.0		AV_{REF1}	V
			I_{OH} = –0.88 mA	AV_{REF1} – 0.5		AV_{REF1}	V
Output voltage, low	V_{OL1}	**Note 6**	I_{OL} = 1.6 mA[Note 7]	0		0.8	V
	V_{OL2}	**Note 8**	I_{OL} = 1.6 mA[Note 7]	0		0.8	V
	V_{OL3}	P10, P11[Note 5]	I_{OL} = 1.6 mA	0		0.8	V
	V_{OL4}	P36 to P39	I_{OL} = 12 mA, EV_{DD} = 4.0 to 5.5 V	0		2.0	V
			I_{OL} = 6.4 mA, EV_{DD} = 3.5 to 5.5 V	0		1.0	V
	V_{OL5}	P614, P615	I_{OL} = 8 mA, EV_{DD} = 4.0 to 5.5 V	0		2.0	V
			I_{OL} = 4 mA, EV_{DD} = 3.8 to 5.5 V	0		1.0	V

Notes 1. Total of P00 to P06, P30 to P35, P40 to P42 and their alternate-function pins: I_{OH} = –24 mA, total of P50 to P55, P60 to P613, P80, P81, P90 to P915 and their alternate-function pins: I_{OH} = –24 mA.

2. Total of P00 to P06, P30 to P35, P40 to P42 and their alternate-function pins: I_{OH} = –12 mA, total of P50 to P55, P60 to P613, P80, P81, P90 to P915 and their alternate-function pins: I_{OH} = –12 mA.

3. Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7: I_{OH} = –24 mA, total of PDH0 to PDH7, PDL0 to PDL15 and their alternate-function pins: I_{OH} = –24 mA.

4. Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7: I_{OH} = –12 mA, total of PDH0 to PDH7, PDL0 to PDL15 and their alternate-function pins: I_{OH} = –12 mA.

5. When used as port pins, set AV_{REF1} = AV_{REF0} = V_{DD}.

6. Total of P00 to P06, P30 to P37, P40 to P42 and their alternate-function pins: I_{OL} = 24 mA, total of P38 to P39, P50 to P55, P60 to P615, P80, P81, P90 to P915 and their alternate-function pins: I_{OL} = 24 mA.

7. Refer to I_{OL1} for I_{OL} of P36 to P39, P614, and P615.

8. Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7 and their alternate-function pins:I_{OL} = 24 mA, total of PDH0 to PDH7, PDL0 to PDL15 and their alternate-function pins: I_{OL} = 24 mA.

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

DC Characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (4/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH}	V_{IN} = V_{DD}				10.0	μA
Input leakage current, low	I_{LIL}	V_{IN} = 0 V				–10.0	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}				10.0	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–10.0	μA
Supply current[Note]	I_{DD1}	Normal operation All peripheral functions operating	f_{XX} = 20 MHz (OSC = 5 MHz) (in PLL mode) REGC = V_{DD} = 5 V ±10%		30	47	mA
			f_{XX} = 16 MHz (OSC = 4 MHz) (in PLL mode) REGC = Capacity V_{DD} = 5 V ±10%		18	32	mA
	I_{DD2}	HALT mode All peripheral functions operating	f_{XX} = 20 MHz (OSC = 5 MHz) (in PLL mode) REGC = V_{DD} = 5 V ±10%		17	27	mA
			f_{XX} = 16 MHz (OSC = 4 MHz) (in PLL mode) REGC = Capacity V_{DD} = 5 V ±10%		10	20	mA
	I_{DD3}	IDLE mode Watch timer operating	OSC = 5 MHz (when PLL mode off) REGC = V_{DD} = 5 V ±10%		900	3300	μA
			OSC = 4 MHz (when PLL mode off) REGC = Capacity V_{DD} = 5 V ±10%		600	2300	μA
	I_{DD4}	Subclock operating mode	f_{XT} = 32.768 kHz Main clock oscillator stopped		70	1460	μA
	I_{DD5}	Subclock IDLE mode	f_{XT} = 32.768 kHz Main clock oscillator stopped, watch timer operating		15	1360	μA
	I_{DD6}	STOP mode	Subclock oscillator stopped (XT1 = V_{SS})		0.1	1330	μA
Pull-up resistor	R_L	V_{IN} = 0 V		10	30	120	kΩ

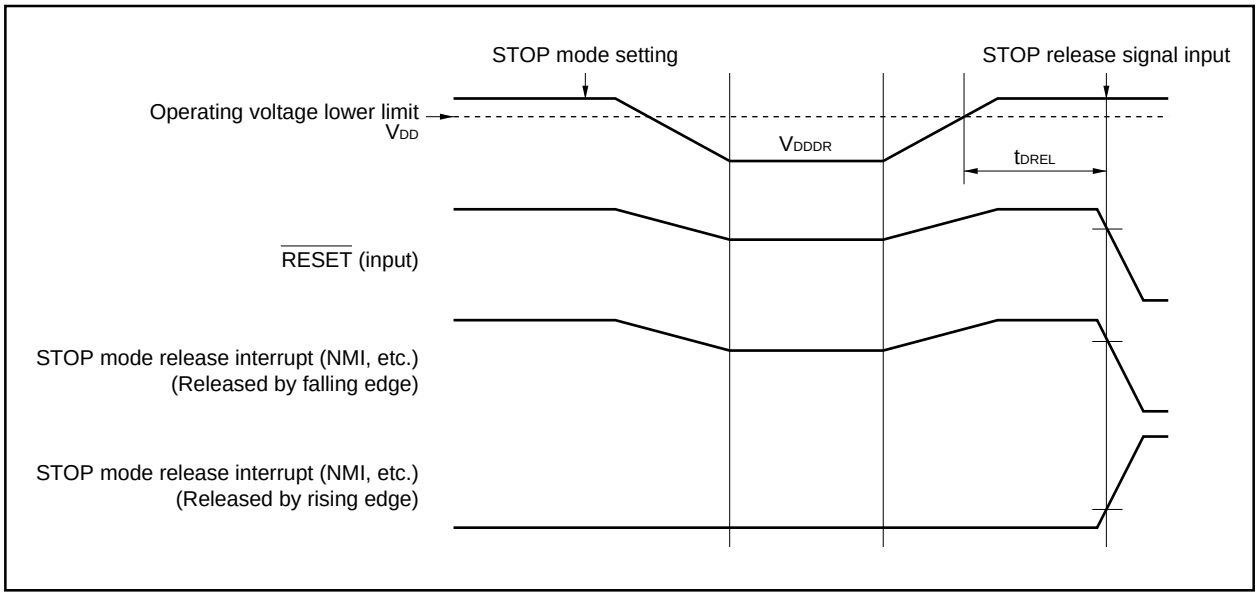
Note Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped). AV_{REF0} is not included.

Data Retention Characteristics

STOP Mode (T_A = –40 to +110°C)

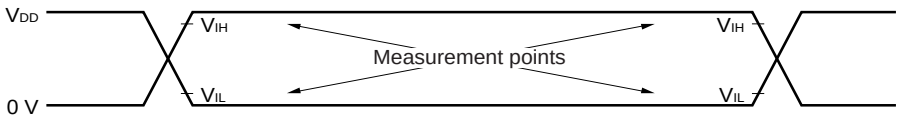
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	2.0		5.5	V
STOP release signal input time	t_{DREL}		0			μs

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

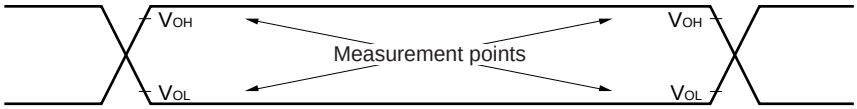


AC Characteristics

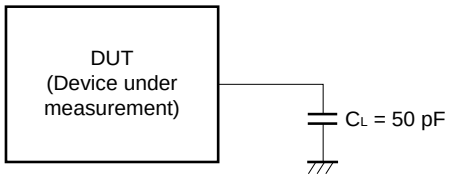
AC Test Input Measurement Points (V_{DD}, AV_{DD}, EV_{DD}, BV_{DD})



AC Test Output Measurement Points



Load Conditions



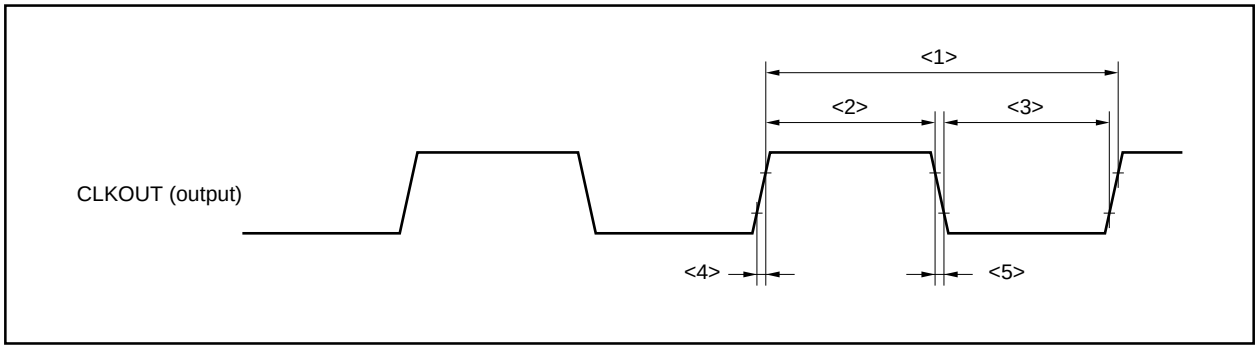
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

CLKOUT Output Timing

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output cycle	t_{CYK}	<1>		50 ns	30.6 μs	
High-level width	t_{WKH}	<2>	V_{DD} = 4.0 to 5.5 V	t_{CYK}/2 – 18		ns
			V_{DD} = 3.5 to 5.5 V	t_{CYK}/2 – 26		ns
Low-level width	t_{WKL}	<3>	V_{DD} = 4.0 to 5.5 V	t_{CYK}/2 – 18		ns
			V_{DD} = 3.5 to 5.5 V	t_{CYK}/2 – 26		ns
Rise time	t_{KR}	<4>	V_{DD} = 4.0 to 5.5 V		18	ns
			V_{DD} = 3.5 to 5.5 V		26	ns
Fall time	t_{KF}	<5>	V_{DD} = 4.0 to 5.5 V		18	ns
			V_{DD} = 3.5 to 5.5 V		26	ns

Clock Timing



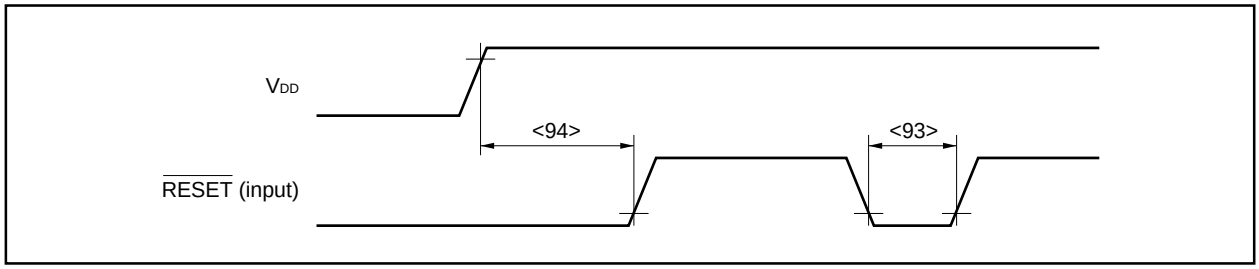
Basic Operation

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

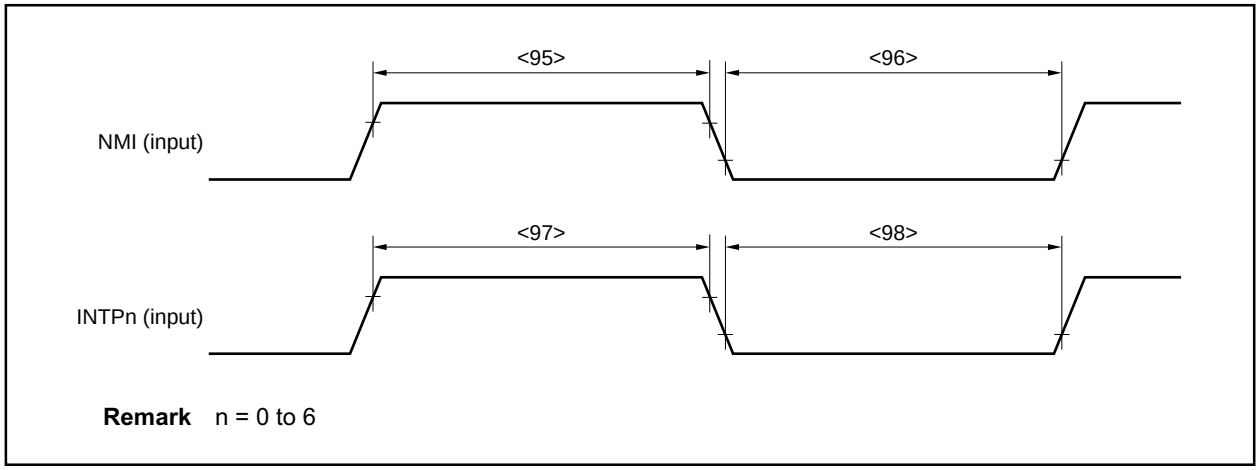
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	t_{WRSL1}	<93>	Reset in power-on status	2		ns
	t_{WRSL2}	<94>	Power-on-reset when REGC = V_{DD}	2		μs
			Power-on-reset when REGC = Capacity	10		μs
NMI high-level width	t_{WNIH}	<95>	Analog noise elimination	1		μs
NMI low-level width	t_{WNIL}	<96>	Analog noise elimination	1		μs
INTPn high-level width	t_{WITH}	<97>	n = 0 to 6 (analog noise elimination)	0.6		μs
INTPn low-level width	t_{WITL}	<98>	n = 0 to 6 (analog noise elimination)	0.6		μs

Remark T = 1/f_{XX}

Reset



Interrupt



Remark n = 0 to 6

Timer Timing

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TI0n high-level width	t_{TI0H}	REGC = V_{DD} = 5 V ±10%	2/fsam + 0.1[Note]		ns
					ns
TI0n low-level width	t_{TI0L}	REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	2/fsam + 0.2[Note]		ns
					ns
TI50 high-level width	t_{TI5H}	REGC = V_{DD} = 5 V ±10%	50		ns
TI51 low-level width	t_{TI5L}	REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	100		ns

Note f_{sam} = Timer count clock

However, f_{sam} = f_{XX}/4 when the TI0n valid edge is selected as the timer count clock.

Remark V850ES/KF1: n = 00, 01, 10, 11

V850ES/KG1: n = 00, 01, 10, 11, 20, 21, 30, 31

V850ES/KJ1: n = 00, 01, 10, 11, 20, 21, 30, 31, 40, 41, 50, 51

UART Timing

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transmit rate				312.5	kbps
ASCK0 frequency[Note]		REGC = V_{DD} = 5 V ±10%		12	MHz
		REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V		6	MHz

Note The ASCK0 pin is only provided in the V850ES/KJ1.

CSI0 Timing

(1) Master mode

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{KCY1}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	200		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	400		ns
$\overline{SCK0n}$ high-/low-level width	t_{KH1}, t_{KL1}	<100>		t_{KCY1}/2 – 30		ns
SI0n setup time (to $\overline{SCK0n}$↑)	t_{SIK1}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	33		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	58		ns
SI0n hold time (from $\overline{SCK0n}$↑)	t_{KSI1}	<102>	REGC = V_{DD} = 5 V ±10%	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	50		ns
Delay time from $\overline{SCK0n}$↓ to SO0n output	t_{KSO1}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		30	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V		60	ns

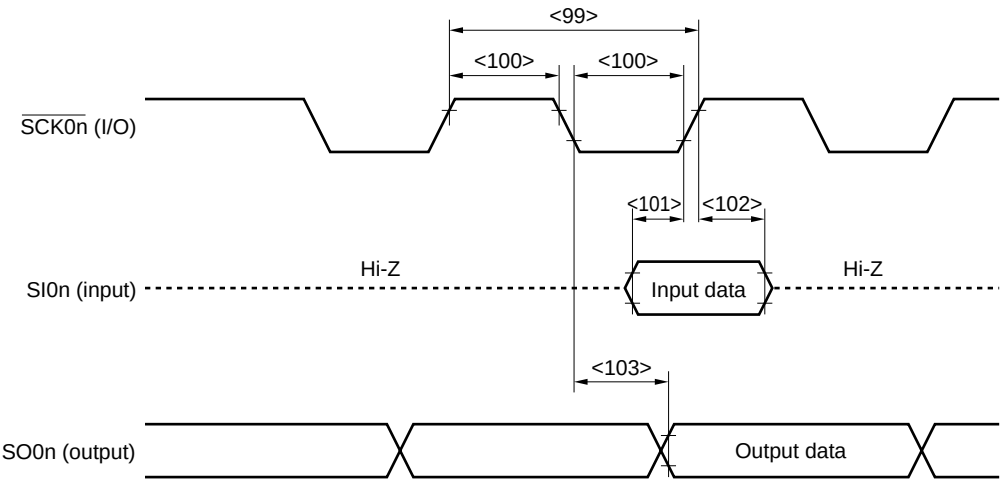
Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

(2) Slave mode

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{KCY2}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	200		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	400		ns
$\overline{SCK0n}$ high-/low-level width	t_{KH2}, t_{KL2}	<100>	REGC = V_{DD} = 4.0 to 5.5 V	45		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	90		ns
SI0n setup time (to $\overline{SCK0n}$↑)	t_{SIK2}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	60		ns
SI0n hold time (from $\overline{SCK0n}$↑)	t_{KSI2}	<102>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	60		ns
Delay time from $\overline{SCK0n}$↓ to SO0n output	t_{KSO2}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		50	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V		100	ns

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)



Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

CSIA Timing

(1) Master mode

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKAn}$ cycle time	t_{KCY3}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	500		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	1000		ns
$\overline{SCKAn}$ high-/low-level width	t_{KH3}, t_{KL3}	<100>		$t_{KCY3}/2$ – 30		ns
SIAn setup time (to $\overline{SCKAn}$↑)	t_{SIK3}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	39		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	68		ns
SIAn hold time (from $\overline{SCKAn}$↑)	t_{KSI3}	<102>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	60		ns
Delay time from $\overline{SCKAn}$↓ to SOAn output	t_{KSO3}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		30	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V		60	ns

Remark n = 0 (V850ES/KF1), n = 0, 1 (V850ES/KG1, V850ES/KJ1)

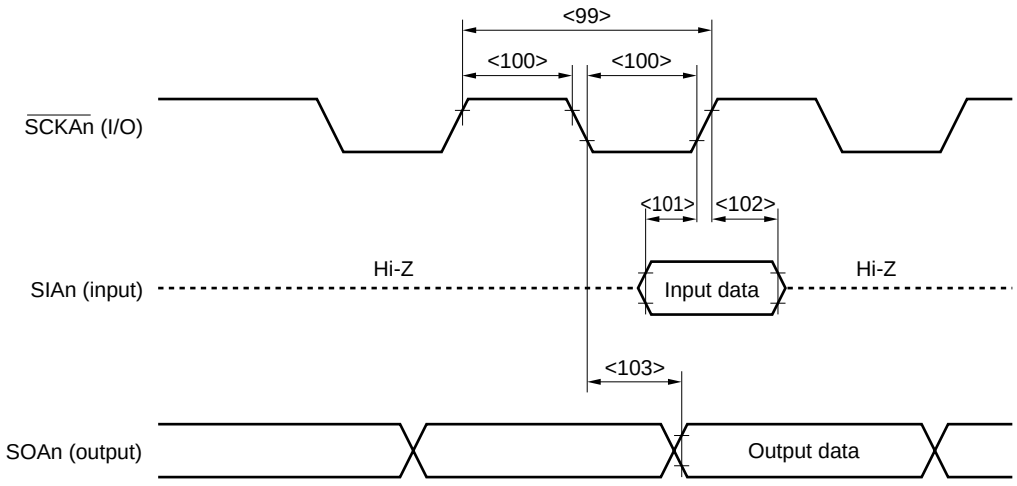
(2) Slave mode

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKAn}$ cycle time	t_{KCY4}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	840		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	1700		ns
$\overline{SCKAn}$ high-/low-level width	t_{KH4}, t_{KL4}	<100>		$t_{KCY4}/2$ – 30		ns
SIAn setup time (to $\overline{SCKAn}$↑)	t_{SIK4}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	50		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	100		ns
SIAn hold time (from $\overline{SCKAn}$↑)	t_{KSI4}	<102>	REGC = V_{DD} = 4.0 to 5.5 V	50		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	100		ns
Delay time from $\overline{SCKAn}$↓ to SOAn output	t_{KSO4}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		$t_{CY} \times 2 + 30$ Note	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V		$t_{CY} \times 2 + 60$ Note	ns

Note t_{CY}: Internal clock output cycle
f_{XX} (CKSAn1 = 0, CKSAn0 = 0), $f_{XX}/2$ (CKSAn1 = 0, CKSAn0 = 1)
$f_{XX}/2^2$ (CKSAn1 = 1, CKSAn0 = 0), $f_{XX}/2^3$ (CKSAn1 = 1, CKSAn0 = 1)

Remark n = 0 (V850ES/KF1), n = 0, 1 (V850ES/KG1, V850ES/KJ1)



Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

I^2C Bus Mode (Y Products (Products with On-Chip I^2C) Only)

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter		Symbol		Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLn clock frequency		f_{CLK}		0	100	0	400	kHz
Bus free time (Between start and stop conditions)		t_{BUF}	<104>	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	<105>	4.0	–	0.6	–	μs
SCLn clock low-level width		t_{LOW}	<106>	4.7	–	1.3	–	μs
SCLn clock high-level width		t_{HIGH}	<107>	4.0	–	0.6	–	μs
Setup time for start/restart conditions		$t_{SU:STA}$	<108>	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	<109>	5.0	–	–	–	μs
	I^2C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	<110>	250	–	100[Note 4]	–	ns
SDAn and SCLn signal rise time		t_R	<111>	–	1000	20 + 0.1Cb[Note 5]	300	ns
SDAn and SCLn signal fall time		t_F	<112>	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	<113>	4.0	–	0.6	–	μs
Pulse width of spike suppressed by input filter		t_{SP}	<114>	–	–	0	50	ns
Capacitance load of each bus line		Cb		–	400	–	400	pF

Notes 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time internally for the SDAn signal (at $V_{IHmin.}$ of SCLn signal) in order to occupy the undefined area at the falling edge of SCLn.

3. If the system does not extend the SCLn signal low hold time (t_{LOW}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

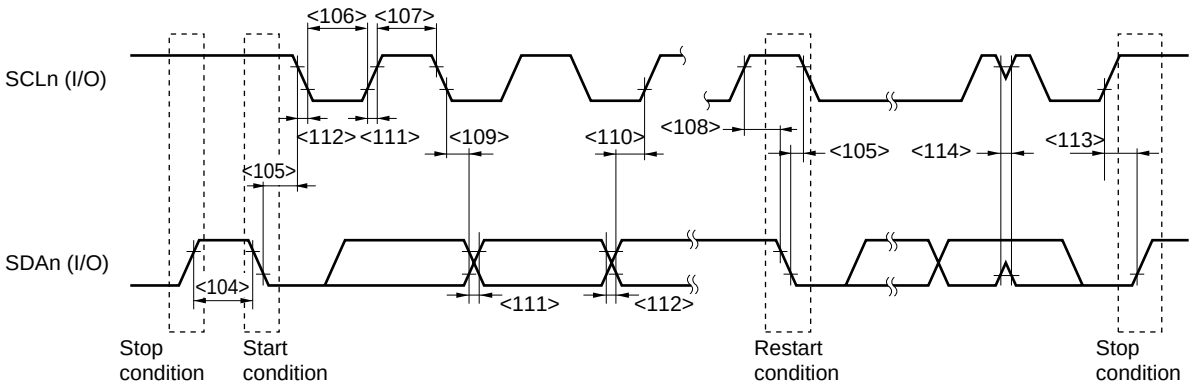
4. The high-speed mode I^2C bus can be used in the normal-mode I^2C bus system. In this case, set the high-speed mode I^2C bus so that it meets the following conditions.

- If the system does not extend the SCLn signal's low state hold time:
  $t_{SU:DAT} \geq 250$ ns
- If the system extends the SCLn signal's low state hold time:
  Transmit the following data bit to the SDAn line prior to the SCLn line release ($t_{Rmax.}$ + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns: Normal mode I^2C bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

I^2C Bus Mode (Y Products (Products with On-Chip I^2C) Only)



Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

A/D Converter

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note 1]		4.0 ≤ AV_{REF0} ≤ 5.5 V		±0.2	±0.6	%FSR
		3.5 ≤ AV_{REF0} ≤ 4.0 V		±0.3	±0.8	%FSR
Conversion time	t_{CONV}	4.0 ≤ AV_{REF0} ≤ 5.5 V	14		60	μs
		3.5 ≤ AV_{REF0} ≤ 4.0 V	17		60	μs
Zero-scale error[Note 1]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±0.6	%FSR
		3.5 ≤ AV_{REF0} ≤ 4.0 V			±0.8	%FSR
Full-scale error[Note 1]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±0.6	%FSR
		3.5 ≤ AV_{REF0} ≤ 4.0 V			±0.8	%FSR
Non-linearity error[Note 2]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±4.5	LSB
		3.5 ≤ AV_{REF0} ≤ 4.0 V			±6.5	LSB
Differential linearity error[Note 2]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±2.0	LSB
		3.5 ≤ AV_{REF0} ≤ 4.0 V			±2.5	LSB
Analog input voltage	V_{IAN}		0		AV_{REF0}	V
AV_{REF0} current	IA_{REF0}	When using A/D converter		1.0	2.0	mA
		When not using A/D converter		1.0	10	μA

Notes 1. Excluding quantization error (±0.05%FSR).

2. Excluding quantization error (±0.5LSB).

Remark LSB: Least Significant Bit
FSR: Full Scale Range

D/A Converter (V850ES/KG1, V850ES/KJ1 only)

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Overall error[Notes 1, 2]		Load condition = 2 MΩ				1.2	%FSR
		Load condition = 4 MΩ				0.8	%FSR
		Load condition = 10 MΩ				0.6	%FSR
Settling time[Notes 1, 2]		C = 30 pF	V_{DD} = 4.5 to 5.5 V			10	μs
			V_{DD} = 3.5 to 4.5 V			15	μs
Output resistance[Note 3]	R_O	Output data 55H			8		kΩ
AV_{REF1} current[Note 4]	IAV_{REF1}	During D/A conversion			1.5	3.0	mA
		When D/A conversion stopped			1.0	10	μA

Notes 1. Excluding quantization error (±0.2%FSR).

2. R is the D/A converter output pin load resistance, and C is the D/A converter output pin load capacitance.

3. Value of 1 channel of D/A converter

4. Value of 2 channels of D/A converter

★ CHAPTER 28 ELECTRICAL SPECIFICATIONS (SPECIAL GRADE (A2) PRODUCTS)

Special grade (A2) products are as follows.

V850ES/KF1:
- μPD703208(A2)
- μPD703208Y(A2)
- μPD703209(A2)
- μPD703209Y(A2)
- μPD703210(A2)
- μPD703210Y(A2)

V850ES/KG1:
- μPD703212(A2)
- μPD703212Y(A2)
- μPD703213(A2)
- μPD703213Y(A2)
- μPD703214(A2)
- μPD703214Y(A2)

V850ES/KJ1:
- μPD703216(A2)
- μPD703216Y(A2)
- μPD703217(A2)
- μPD703217Y(A2)

Absolute Maximum Ratings (T_A = 25°C) (1/2)

Parameter	Symbol	Conditions	Ratings	Unit
Supply voltage	V_{DD}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	V_{PP}	Flash memory version, **Note 1**	−0.3 to +10.5	V
	BV_{DD}	$BV_{DD} \leq V_{DD}$	−0.3 to V_{DD} + 0.3 **Note 1**	V
	EV_{DD}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	AV_{REF0}	$V_{DD} = EV_{DD} = AV_{REF0}$	−0.3 to +6.5	V
	AV_{REF1}	$AV_{REF1} \leq V_{DD}$ (D/A output mode) $AV_{REF1} = AV_{REF0} = V_{DD}$ (port mode)	−0.3 to V_{DD} + 0.3 **Note 1**	V
Input voltage	V_{I1}	P00 to P06, P30 to P35, P38, P39, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915, $\overline{\text{RESET}}$	−0.3 to EV_{DD} + 0.3 **Note 1**	V
	V_{I2}	PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7	−0.3 to BV_{DD} + 0.3 **Note 1**	V
	V_{I3}	P10, P11	−0.3 to AV_{REF1} + 0.3 **Note 1**	V
	V_{I4}	P36, P37, P614, P615	−0.3 to +13 **Note 2**	V
	V_{I5}	X1, X2, XT1, XT2	−0.3 to V_{DD} + 0.3 **Note 1**	V
Analog input voltage	V_{IAN}	P70 to P715	−0.3 to AV_{REF0} + 0.3 **Note 1**	V

Notes 1. Be sure not to exceed the absolute maximum ratings (MAX. value) of each supply voltage.

2. When pull-up is not specified by a mask option. The same as V_{I1} when pull-up is specified.

Absolute Maximum Ratings (T_A = 25°C) (2/2)

Parameter	Symbol	Conditions		Ratings	Unit
Output current, low	I_{OL} Note	P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915, PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7	Per pin	14	mA
		P36 to P39, P614, P615		21	mA
		P00 to P06, P30 to P39, P40 to P42	Total of all pins: 49 mA	24.5	mA
		P50 to P55, P60 to P615, P80, P81, P90 to P915		24.5	
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7	Total of all pins: 49 mA	24.5	mA
		PDL0 to PDL15, PDH0 to PDH7		24.5	mA
Output current, high	I_{OH} Note	Per pin		–7	mA
		P00 to P06, P30 to P35, P40 to P42	Total of all pins: –42 mA	–21	
		P50 to P55, P60 to P613, P80, P81, P90 to P915		–21	mA
		PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7	Total of all pins: –42 mA	–21	mA
		PDL0 to PDL15, PDH0 to PDH7		–21	mA
		P10, P11	Per pin	–7	
Operating ambient temperature	T_A			–40 to +125	°C
Storage temperature	T_{stg}			–65 to +150	°C

Note In the V850ES/KF1, the specifications of the total of all pins for I_{OL} and I_{OH} are as follows since BV_{DD} system pins do not exist.

I_{OL}	Total of pins: 49 mA	P00 to P06, P30 to P35, P38, P39, P40 to P42	24.5	mA
		P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL15	24.5	mA
I_{OH}	Total of pins: –42 mA	P00 to P06, P30 to P35, P40 to P42	–21	mA
		P50 to P55, P90, P91, P96 to P99, P913 to P915, PCM0 to PCM3, PCS0, PCS1, PCT0, PCT1, PCT4, PCT6, PDL0 to PDL15	–21	mA

Cautions 1. Do not directly connect the output (or I/O) pins of IC products to each other, or to V_{DD}, V_{CC}, and GND. Open-drain pins or open-collector pins, however, can be directly connected to each other. Direct connection of the output pins between an IC product and an external circuit is possible, if the output pins can be set to the high-impedance state and the output timing of the external circuit is designed to avoid output conflict.

2. Product quality may suffer if the absolute maximum rating is exceeded even momentarily for any parameter. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded. The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

3. The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

In the V850ES/KF1, the specification of V_{I2} is the same as that of the V_{I1} since the BV_{DD} pin does not exist.

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

Capacitance (T_A = 25°C, V_{DD} = EV_{DD} = AV_{REF0} = BV_{DD} = AV_{REF1} = V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f_X = 1 MHz Unmeasured pins returned to 0 V	P70 to P715			15	pF
I/O capacitance	C_{IO}		**Note**			15	pF
			P36 to P39, P614, P615			20	pF

Note P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915, PCD0 to PCD3, PCM0 to PCM5, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

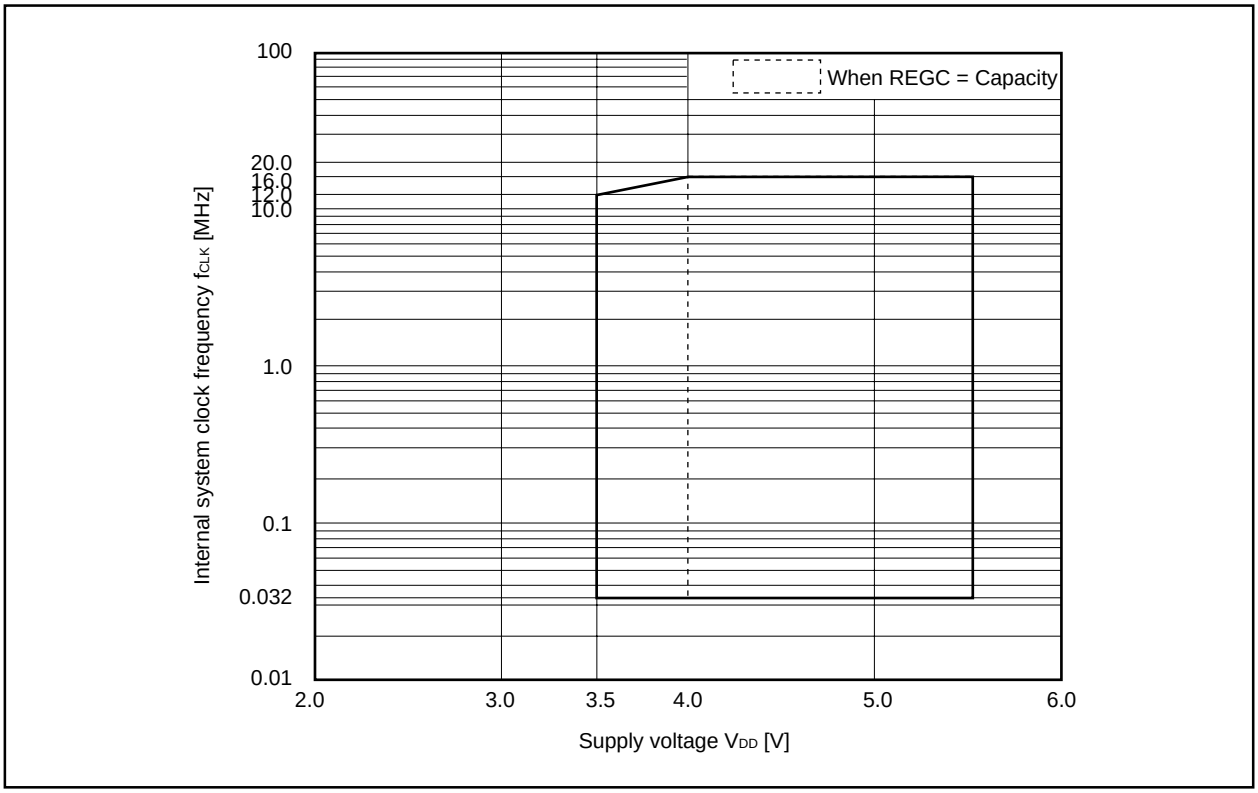
P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

Operating Conditions

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Internal system clock frequency	f_{CLK}	REGC = V_{DD} = 5 V ±10% In PLL mode (OSC = 2 to 4 MHz)	0.25		16	MHz
		REGC = Capacity, V_{DD} = 4.0 to 5.5 V In PLL mode (OSC = 2 to 4 MHz)	0.25		16	MHz
		REGC = V_{DD} = 3.5 to 5.5 V In PLL mode (OSC = 2 to 3 MHz)	0.25		12	MHz
		REGC = V_{DD} = 3.5 to 5.5 V	0.0625		10	MHz
		REGC = V_{DD} = 3.5 to 5.5 V, operating with subclock		32.768		kHz

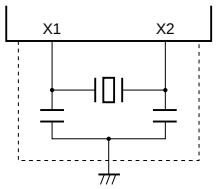
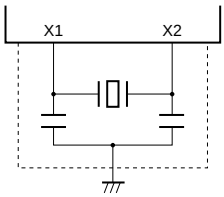
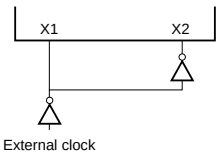
Internal System Clock Frequency vs. Supply Voltage



PLL Characteristics (T_A = –40 to +125°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input frequency	f_x		2		4	MHz
Output frequency	f_{xx}		8		16	MHz
Lock time	t_{PLL}	After V_{DD} reaches MIN.: 3.5 V			200	μs

Main Clock Oscillator Characteristics (T_A = –40 to +125°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Ceramic resonator		Oscillation frequency (f_X)Note 1		2		10	MHz
		Oscillation stabilization timeNote 2	After reset is released		$2^{15}/f_X$		s
			After STOP mode is released		**Note 3**		s
Crystal resonator		Oscillation frequency (f_X)Note 1		2		10	MHz
		Oscillation stabilization timeNote 2	After reset is released		$2^{15}/f_X$		s
			After STOP mode is released		**Note 3**		s
External clock		X1, X2 input frequency (f_X)	REGC = V_{DD} Duty = 50% ±5%	2		10	MHz

Notes 1. Indicates only oscillator characteristics.

2. Time required to stabilize the resonator after reset or STOP mode is released.

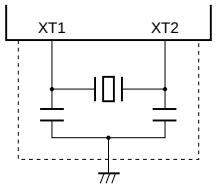
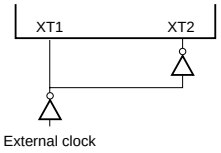
3. The value differs depending on the OSTS register settings.

Cautions 1. When using the main clock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. When the main clock is stopped and the device is operating on the subclock, wait until the oscillation stabilization time has been secured by the program before switching back to the main clock.

Subclock Oscillator Characteristics (T_A = –40 to +125°C, V_{DD} = 3.5 to 5.5 V, V_{SS} = 0 V)

Resonator	Recommended Circuit	Parameter	Conditions	MIN.	TYP.	MAX.	Unit
Crystal resonator		Oscillation frequency (f_{XT})Note 1		32	32.768	35	kHz
		Oscillation stabilization timeNote 2			10		s
External clock		XT1 input frequency (f_{XT})Note 1 Duty = 50% ±5%	REGC = V_{DD}	32		35	kHz

Notes 1. Indicates only oscillator characteristics.

2. Time required from when V_{DD} reaches oscillation voltage range (MIN.: 3.5 V) to when the crystal resonator stabilizes.

Cautions 1. When using the subclock oscillator, wire as follows in the area enclosed by the broken lines in the above figures to avoid an adverse effect from wiring capacitance.

- **Keep the wiring length as short as possible.**
- **Do not cross the wiring with the other signal lines.**
- **Do not route the wiring near a signal line through which a high fluctuating current flows.**
- **Always make the ground point of the oscillator capacitor the same potential as V_{SS}.**
- **Do not ground the capacitor to a ground pattern through which a high current flows.**
- **Do not fetch signals from the oscillator.**

2. The subclock oscillator is designed as a low-amplitude circuit for reducing current consumption, and is more prone to malfunction due to noise than the main clock oscillator. Particular care is therefore required with the wiring method when the subclock is used.

DC Characteristics

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (1/4)

Parameter	Symbol	Conditions		MAX.	Unit
Output current, high	I_{OH1}	Per pin for P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915		–3.5	mA
		Total of P00 to P06, P30 to P35, P40 to P42	EV_{DD} = 4.0 to 5.5 V	–21	mA
			EV_{DD} = 2.7 to 5.5 V	–10.5	mA
		Total of P50 to P55, P60 to P613, P80, P81, P90 to P915	EV_{DD} = 4.0 to 5.5 V	–21	mA
			EV_{DD} = 2.7 to 5.5 V	–10.5	mA
	I_{OH2}	Per pin for PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7, PDH0 to PDH7, PDL0 to PDL15		–3.5	mA
		Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7	EV_{DD} = 4.0 to 5.5 V	–21	mA
			EV_{DD} = 2.7 to 5.5 V	–10.5	mA
		Total of PDL0 to PDL15, PDH0 to PDH7	EV_{DD} = 4.0 to 5.5 V	–21	mA
			EV_{DD} = 2.7 to 5.5 V	–10.5	mA
Output current, low	I_{OL1}	Per pin for P00 to P06, P10, P11, P30 to P35, P40 to P42, P50 to P55, P60 to P613, P80, P81, P90 to P915		7	mA
		Per pin for P36 to P39	EV_{DD} = 4.0 to 5.5 V	10.5	mA
			EV_{DD} = 3.5 to 5.5 V	5.6	mA
		Per pin for P614, P615	EV_{DD} = 4.0 to 5.5 V	7	mA
			EV_{DD} = 3.5 to 5.5 V	3.5	mA
		Total of P00 to P06, P30 to P37, P40 to P42		21	mA
		Total of P38, P39, P50 to P55, P60 to P615, P80, P81, P90 to P915		21	mA
	I_{OL2}	Per pin for PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7, PDH0 to PDH7, PDL0 to PDL15		7	mA
		Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7		21	mA
		Total of PDL0 to PDL15, PDH0 to PDH7		21	mA

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

DC Characteristics

(T_A = –40 to +110°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (2/4)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Input voltage, high	V_{IH1}	**Note 1**	0.7EV_{DD}		EV_{DD}	V
	V_{IH2}	**Note 2**	0.8EV_{DD}		EV_{DD}	V
	V_{IH3}	**Note 3**	0.7BV_{DD}		BV_{DD}	V
	V_{IH4}	P70 to P715	0.7AV_{REF0}		AV_{REF0}	V
	V_{IH5}	P10, P11[Note 4]	0.7AV_{REF1}		AV_{REF1}	V
	V_{IH6}	P36, P37, P614, P615	0.7EV_{DD}		12[Note 5]	V
	V_{IH7}	X1, X2, XT1, XT2	EV_{DD} – 0.5		EV_{DD}	V
Input voltage, low	V_{IL1}	**Note 1**	EV_{SS}		0.3EV_{DD}	V
	V_{IL2}	**Note 2**	EV_{SS}		0.2EV_{DD}	V
	V_{IL3}	**Note 3**	BV_{SS}		0.3BV_{DD}	V
	V_{IL4}	P70 to P715	AV_{SS}		0.3AV_{REF0}	V
	V_{IL5}	P10, P11[Note 4]	AV_{SS}		0.3AV_{REF1}	V
	V_{IL6}	P36, P37, P614, P615	EV_{SS}		0.3EV_{DD}	V
	V_{IL7}	X1, X2, XT1, XT2	EV_{SS}		0.4	V

Notes 1. P00, P01, P30, P41, P60 to P65, P67, P611, P98, P911 and their alternate-function pins.

2. $\overline{\text{RESET}}$, P02 to P06, P31 to P35, P38, P39, P40, P42, P50 to P55, P66, P68 to P610, P612, P613, P80, P81, P90 to P97, P99, P910, P912 to P915 and their alternate-function pins.

3. PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7, PDL0 to PDL15, PDH0 to PDH7 and their alternate-function pins.

4. When used as port pins, set AV_{REF1} = AV_{REF0} = V_{DD}.

5. When pull-up is not specified by a mask option. EV_{DD} when pull-up is specified.

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

DC Characteristics

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (3/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Output voltage, high	V_{OH1}	**Note 1**	I_{OH} = –1.4 mA, EV_{DD} = 4.0 to 5.5 V	EV_{DD} – 1.0		EV_{DD}	V
		Note 2	I_{OH} = –0.07 mA, EV_{DD} = 3.5 to 5.5 V	EV_{DD} – 0.5		EV_{DD}	V
	V_{OH2}	**Note 3**	I_{OH} = –1.4 mA, EV_{DD} = 4.0 to 5.5 V	BV_{DD} – 1.0		BV_{DD}	V
		Note 4	I_{OH} = –0.07 mA, EV_{DD} = 3.5 to 5.5 V	BV_{DD} – 0.5		BV_{DD}	V
	V_{OH3}	P10, P11[Note 5]	I_{OH} = –1.4 mA	AV_{REF1} – 1.0		AV_{REF1}	V
			I_{OH} = –0.07 mA	AV_{REF1} – 0.5		AV_{REF1}	V
Output voltage, low	V_{OL1}	**Note 6**	I_{OL} = 1.4 mA[Note 7]	0		0.8	V
	V_{OL2}	**Note 8**	I_{OL} = 1.4 mA[Note 7]	0		0.8	V
	V_{OL3}	P10, P11[Note 5]	I_{OL} = 1.4 mA	0		0.8	V
	V_{OL4}	P36 to P39	I_{OL} = 10.5 mA, EV_{DD} = 4.0 to 5.5 V	0		2.0	V
			I_{OL} = 5.6 mA, EV_{DD} = 3.5 to 5.5 V	0		1.0	V
	V_{OL5}	P614, P615	I_{OL} = 7 mA, EV_{DD} = 4.0 to 5.5 V	0		2.0	V
			I_{OL} = 3.5 mA, EV_{DD} = 3.5 to 5.5 V	0		1.0	V

Notes 1. Total of P00 to P06, P30 to P35, P40 to P42 and their alternate-function pins: I_{OH} = –21 mA, total of P50 to P55, P60 to P613, P80, P81, P90 to P915 and their alternate-function pins: I_{OH} = –21 mA.

2. Total of P00 to P06, P30 to P35, P40 to P42 and their alternate-function pins: I_{OH} = –10.5 mA, total of P50 to P55, P60 to P613, P80, P81, P90 to P915 and their alternate-function pins: I_{OH} = –10.5 mA.

3. Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7: I_{OH} = –21 mA, total of PDH0 to PDH7, PDL0 to PDL15 and their alternate-function pins: I_{OH} = –21 mA.

4. Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7: I_{OH} = –10.5 mA, total of PDH0 to PDH7, PDL0 to PDL15 and their alternate-function pins: I_{OH} = –10.5 mA.

5. When used as port pins, set AV_{REF1} = AV_{REF0} = V_{DD}.

6. Total of P00 to P06, P30 to P37, P40 to P42 and their alternate-function pins: I_{OL} = 21 mA, total of P38 to P39, P50 to P55, P60 to P615, P80, P81, P90 to P915 and their alternate-function pins: I_{OL} = 21 mA.

7. Refer to I_{OL1} for I_{OL} of P36 to P39, P614, and P615.

8. Total of PCD0 to PCD3, PCM0 to PCM3, PCS0 to PCS7, PCT0 to PCT7 and their alternate-function pins:I_{OL} = 21 mA, total of PDH0 to PDH7, PDL0 to PDL15 and their alternate-function pins: I_{OL} = 21 mA.

Caution The following pins are not provided in the V850ES/KF1.

P10, P11, P36, P37, P60 to P615, P78 to P715, P80, P81, P92 to P95, P910 to P912, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH0 to PDH7, AV_{REF1}, BV_{DD}, BV_{SS}

The following pins are not provided in the V850ES/KG1.

P60 to P615, P78 to P715, P80, P81, PCD0 to PCD3, PCM4, PCM5, PCS2 to PCS7, PCT2, PCT3, PCT5, PCT7, PDH6, PDH7

DC Characteristics

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V) (4/4)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Input leakage current, high	I_{LIH}	V_{IN} = V_{DD}				10.0	μA
Input leakage current, low	I_{LIL}	V_{IN} = 0 V				–10.0	μA
Output leakage current, high	I_{LOH}	V_O = V_{DD}				10.0	μA
Output leakage current, low	I_{LOL}	V_O = 0 V				–10.0	μA
Supply current[Note]	I_{DD1}	Normal operation All peripheral functions operating	f_{XX} = 20 MHz (OSC = 4 MHz) (in PLL mode) REGC = V_{DD} = 5 V ±10%		30	43	mA
			f_{XX} = 16 MHz (OSC = 4 MHz) (in PLL mode) REGC = Capacity V_{DD} = 5 V ±10%		18	33	mA
	I_{DD2}	HALT mode All peripheral functions operating	f_{XX} = 20 MHz (OSC = 4 MHz) (in PLL mode) REGC = V_{DD} = 5 V ±10%		17	26	mA
			f_{XX} = 16 MHz (OSC = 4 MHz) (in PLL mode) REGC = Capacity V_{DD} = 5 V ±10%		10	21	mA
	I_{DD3}	IDLE mode Watch timer operating	OSC = 4 MHz (when PLL mode off) REGC = V_{DD} = 5 V ±10%		900	3700	μA
			OSC = 4 MHz (when PLL mode off) REGC = Capacity V_{DD} = 5 V ±10%		600	2900	μA
	I_{DD4}	Subclock operating mode	f_{XT} = 32.768 kHz Main clock oscillator stopped		70	2060	μA
	I_{DD5}	Subclock IDLE mode	f_{XT} = 32.768 kHz Main clock oscillator stopped, watch timer operating		15	1900	μA
	I_{DD6}	STOP mode	Subclock oscillator stopped (XT1 = V_{SS})		0.1	1930	μA
Pull-up resistor	R_L	V_{IN} = 0 V		10	30	120	kΩ

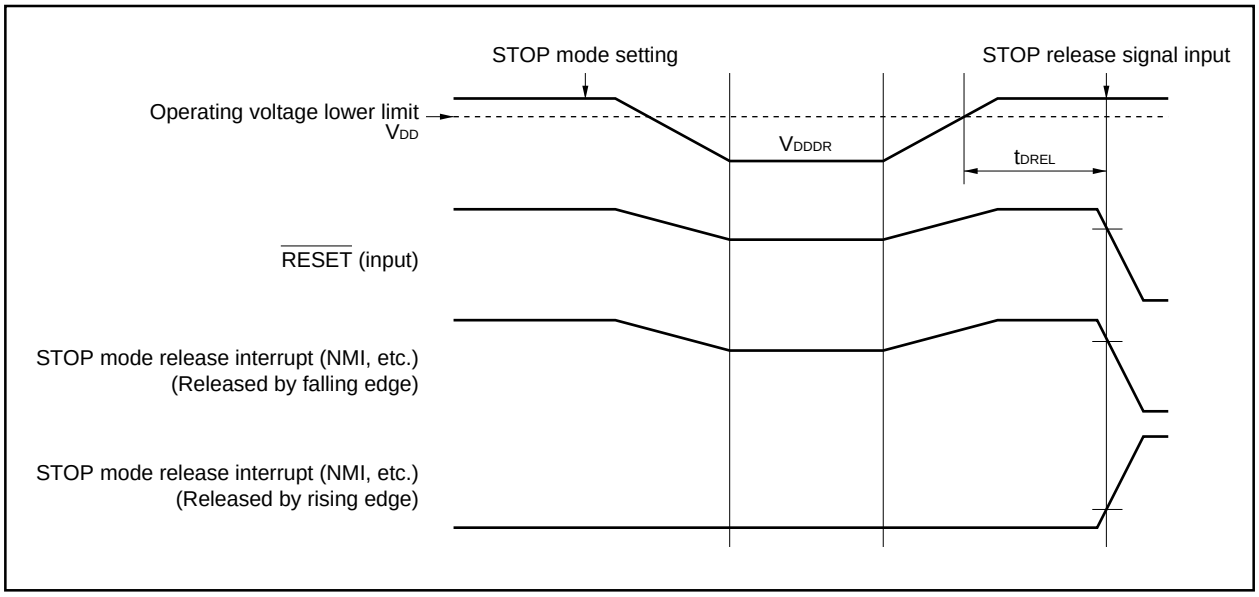
Note Total current of V_{DD}, EV_{DD}, and BV_{DD} (all ports stopped). AV_{REF0} is not included.

Data Retention Characteristics

STOP Mode (T_A = –40 to +125°C)

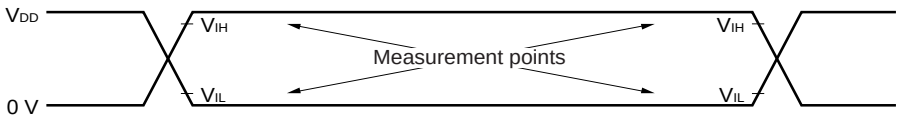
Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Data retention voltage	V_{DDDR}	STOP mode	2.0		5.5	V
STOP release signal input time	t_{DREL}		0			μs

Caution Shifting to STOP mode and restoring from STOP mode must be performed within the rated operating range.

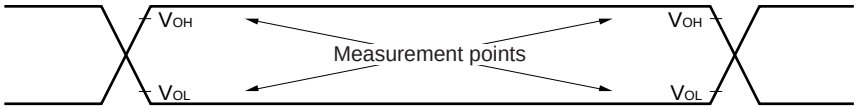


AC Characteristics

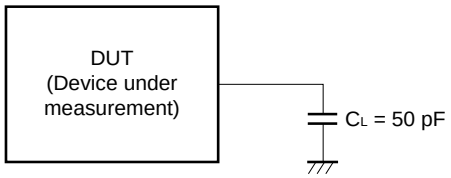
AC Test Input Measurement Points (V_{DD}, AV_{DD}, EV_{DD}, BV_{DD})



AC Test Output Measurement Points



Load Conditions



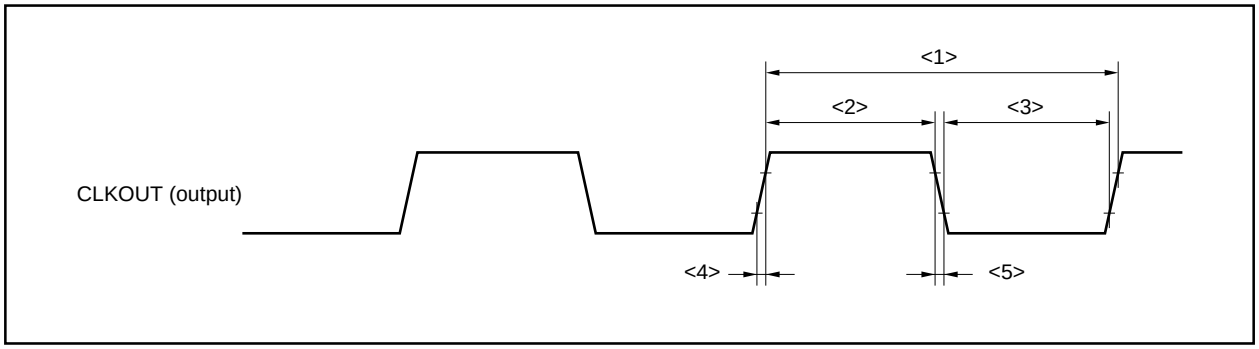
Caution If the load capacitance exceeds 50 pF due to the circuit configuration, bring the load capacitance of the device to 50 pF or less by inserting a buffer or by some other means.

CLKOUT Output Timing

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
Output cycle	t_{CYK}	<1>		62.5 ns	30.6 μs	
High-level width	t_{WKH}	<2>	V_{DD} = 4.0 to 5.5 V	t_{CYK}/2 – 18		ns
			V_{DD} = 3.5 to 5.5 V	t_{CYK}/2 – 26		ns
Low-level width	t_{WKL}	<3>	V_{DD} = 4.0 to 5.5 V	t_{CYK}/2 – 18		ns
			V_{DD} = 3.5 to 5.5 V	t_{CYK}/2 – 26		ns
Rise time	t_{KR}	<4>	V_{DD} = 4.0 to 5.5 V		18	ns
			V_{DD} = 3.5 to 5.5 V		26	ns
Fall time	t_{KF}	<5>	V_{DD} = 4.0 to 5.5 V		18	ns
			V_{DD} = 3.5 to 5.5 V		26	ns

Clock Timing



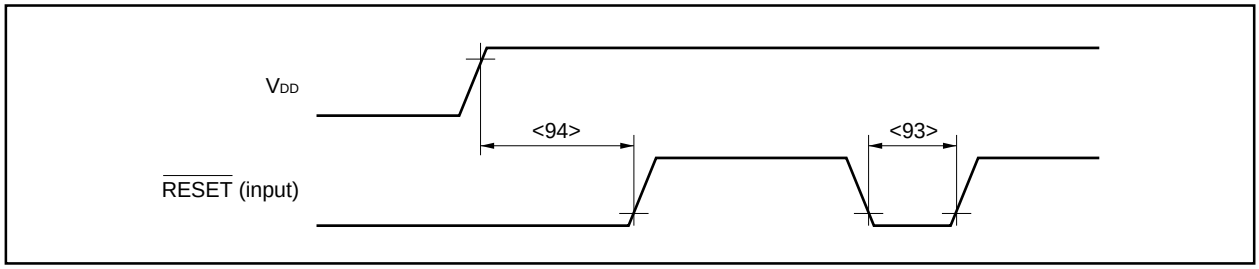
Basic Operation

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

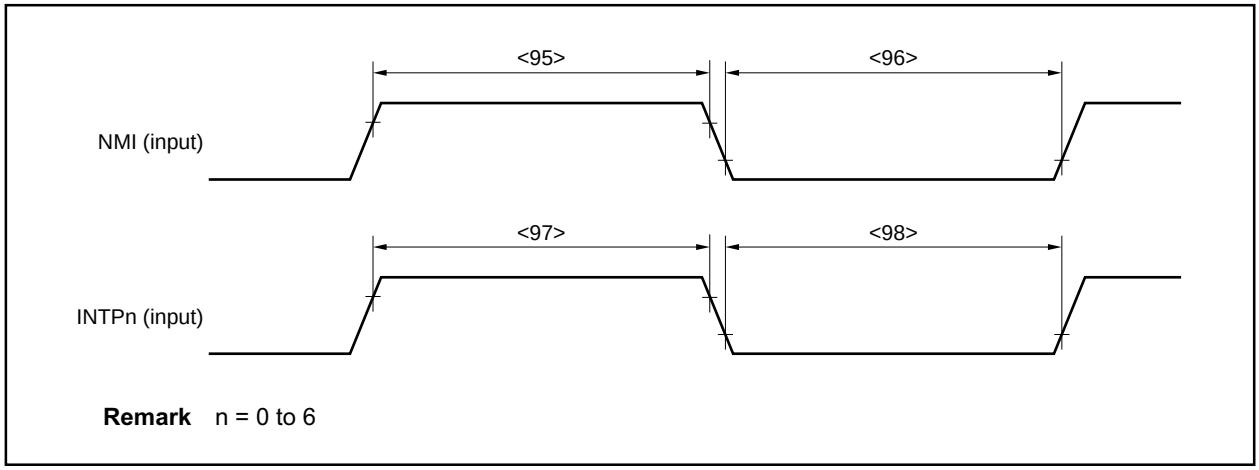
Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{\text{RESET}}$ low-level width	t_{WRSL1}	<93>	Reset in power-on status	2		ns
	t_{WRSL2}	<94>	Power-on-reset when REGC = V_{DD}	2		μs
			Power-on-reset when REGC = Capacity	10		μs
NMI high-level width	t_{WNIH}	<95>	Analog noise elimination	1		μs
NMI low-level width	t_{WNIL}	<96>	Analog noise elimination	1		μs
INTPn high-level width	t_{WITH}	<97>	n = 0 to 6 (analog noise elimination)	0.6		μs
INTPn low-level width	t_{WITL}	<98>	n = 0 to 6 (analog noise elimination)	0.6		μs

Remark T = 1/f_{XX}

Reset



Interrupt



Remark n = 0 to 6

Timer Timing

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
TI0n high-level width	t_{TI0H}	REGC = V_{DD} = 5 V ±10%	2/fsam + 0.1[Note]		ns
					ns
TI0n low-level width	t_{TI0L}	REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	2/fsam + 0.2[Note]		ns
					ns
TI50 high-level width	t_{TI5H}	REGC = V_{DD} = 5 V ±10%	50		ns
TI51 low-level width	t_{TI5L}	REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	100		ns

Note f_{sam} = Timer count clock
However, f_{sam} = f_{XX}/4 when the TI0n valid edge is selected as the timer count clock.

Remark V850ES/KF1: n = 00, 01, 10, 11
V850ES/KG1: n = 00, 01, 10, 11, 20, 21, 30, 31
V850ES/KJ1: n = 00, 01, 10, 11, 20, 21, 30, 31, 40, 41, 50, 51

UART Timing

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Transmit rate				312.5	kbps
ASCK0 frequency[Note]		REGC = V_{DD} = 5 V ±10%		12	MHz
		REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V		6	MHz

Note The ASCK0 pin is only provided in the V850ES/KJ1.

CSI0 Timing

(1) Master mode

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{KCY1}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	200		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	400		ns
$\overline{SCK0n}$ high-/low-level width	t_{KH1}, t_{KL1}	<100>		t_{KCY1}/2 – 30		ns
SI0n setup time (to $\overline{SCK0n}$↑)	t_{SIK1}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	33		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	58		ns
SI0n hold time (from $\overline{SCK0n}$↑)	t_{KSI1}	<102>	REGC = V_{DD} = 5 V ±10%	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	50		ns
Delay time from $\overline{SCK0n}$↓ to SO0n output	t_{KSO1}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		30	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V		60	ns

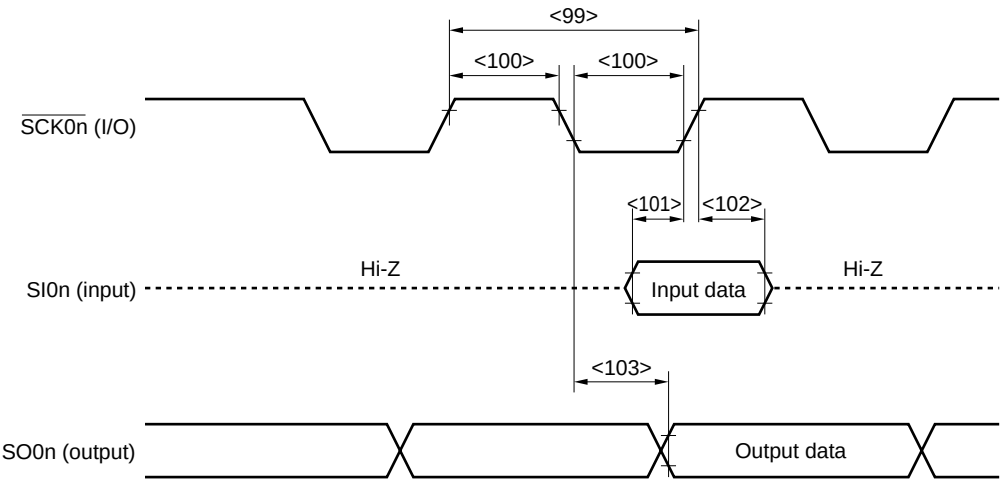
Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

(2) Slave mode

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCK0n}$ cycle time	t_{KCY2}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	200		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	400		ns
$\overline{SCK0n}$ high-/low-level width	t_{KH2}, t_{KL2}	<100>	REGC = V_{DD} = 4.0 to 5.5 V	45		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	90		ns
SI0n setup time (to $\overline{SCK0n}$↑)	t_{SIK2}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	60		ns
SI0n hold time (from $\overline{SCK0n}$↑)	t_{KSI2}	<102>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	60		ns
Delay time from $\overline{SCK0n}$↓ to SO0n output	t_{KSO2}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		50	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V		100	ns

Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)



Remark n = 0, 1 (V850ES/KF1, V850ES/KG1), n = 0 to 2 (V850ES/KJ1)

CSIA Timing

(1) Master mode

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKAn}$ cycle time	t_{KCY3}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	500		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	1000		ns
$\overline{SCKAn}$ high-/low-level width	t_{KH3}, t_{KL3}	<100>		$t_{KCY3}/2$ – 30		ns
SIAn setup time (to $\overline{SCKAn}$↑)	t_{SIK3}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	39		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	68		ns
SIAn hold time (from $\overline{SCKAn}$↑)	t_{KSI3}	<102>	REGC = V_{DD} = 4.0 to 5.5 V	30		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	60		ns
Delay time from $\overline{SCKAn}$↓ to SOAn output	t_{KSO3}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		30	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V		60	ns

Remark n = 0 (V850ES/KF1), n = 0, 1 (V850ES/KG1, V850ES/KJ1)

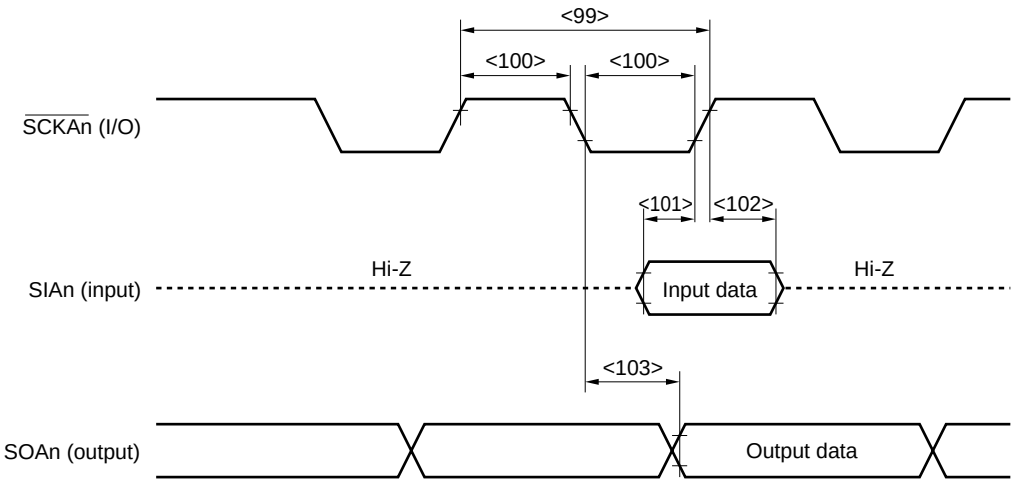
(2) Slave mode

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter	Symbol		Conditions	MIN.	MAX.	Unit
$\overline{SCKAn}$ cycle time	t_{KCY4}	<99>	REGC = V_{DD} = 4.0 to 5.5 V	840		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	1700		ns
$\overline{SCKAn}$ high-/low-level width	t_{KH4}, t_{KL4}	<100>		$t_{KCY4}/2$ – 30		ns
SIAn setup time (to $\overline{SCKAn}$↑)	t_{SIK4}	<101>	REGC = V_{DD} = 4.0 to 5.5 V	50		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	100		ns
SIAn hold time (from $\overline{SCKAn}$↑)	t_{KSI4}	<102>	REGC = V_{DD} = 4.0 to 5.5 V	50		ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V	100		ns
Delay time from $\overline{SCKAn}$↓ to SOAn output	t_{KSO4}	<103>	REGC = V_{DD} = 4.0 to 5.5 V		$t_{CY} \times 2 + 30$ Note	ns
			REGC = Capacity, V_{DD} = 4.0 to 5.5 V, REGC = V_{DD} = 3.5 to 5.5 V		$t_{CY} \times 2 + 60$ Note	ns

Note t_{CY}: Internal clock output cycle
f_{XX} (CKSAn1 = 0, CKSAn0 = 0), $f_{XX}/2$ (CKSAn1 = 0, CKSAn0 = 1)
$f_{XX}/2^2$ (CKSAn1 = 1, CKSAn0 = 0), $f_{XX}/2^3$ (CKSAn1 = 1, CKSAn0 = 1)

Remark n = 0 (V850ES/KF1), n = 0, 1 (V850ES/KG1, V850ES/KJ1)



Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

I^2C Bus Mode (Y Products (Products with On-Chip I^2C) Only)

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V, C_L = 50 pF)

Parameter		Symbol		Normal Mode		High-Speed Mode		Unit
				MIN.	MAX.	MIN.	MAX.	
SCLn clock frequency		f_{CLK}		0	100	0	400	kHz
Bus free time (Between start and stop conditions)		t_{BUF}	<104>	4.7	–	1.3	–	μs
Hold time[Note 1]		$t_{HD:STA}$	<105>	4.0	–	0.6	–	μs
SCLn clock low-level width		t_{LOW}	<106>	4.7	–	1.3	–	μs
SCLn clock high-level width		t_{HIGH}	<107>	4.0	–	0.6	–	μs
Setup time for start/restart conditions		$t_{SU:STA}$	<108>	4.7	–	0.6	–	μs
Data hold time	CBUS compatible master	$t_{HD:DAT}$	<109>	5.0	–	–	–	μs
	I^2C mode			0[Note 2]	–	0[Note 2]	0.9[Note 3]	μs
Data setup time		$t_{SU:DAT}$	<110>	250	–	100[Note 4]	–	ns
SDAn and SCLn signal rise time		t_R	<111>	–	1000	20 + 0.1Cb[Note 5]	300	ns
SDAn and SCLn signal fall time		t_F	<112>	–	300	20 + 0.1Cb[Note 5]	300	ns
Stop condition setup time		$t_{SU:STO}$	<113>	4.0	–	0.6	–	μs
Pulse width of spike suppressed by input filter		t_{SP}	<114>	–	–	0	50	ns
Capacitance load of each bus line		Cb		–	400	–	400	pF

Notes 1. At the start condition, the first clock pulse is generated after the hold time.

2. The system requires a minimum of 300 ns hold time internally for the SDAn signal (at $V_{IHmin.}$ of SCLn signal) in order to occupy the undefined area at the falling edge of SCLn.

3. If the system does not extend the SCLn signal low hold time (t_{LOW}), only the maximum data hold time ($t_{HD:DAT}$) needs to be satisfied.

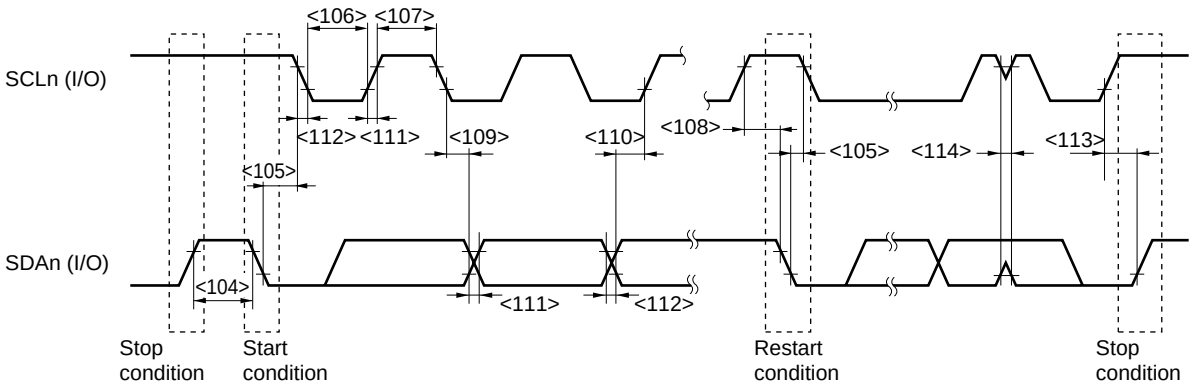
4. The high-speed mode I^2C bus can be used in the normal-mode I^2C bus system. In this case, set the high-speed mode I^2C bus so that it meets the following conditions.

- If the system does not extend the SCLn signal's low state hold time:
  $t_{SU:DAT} \geq 250$ ns
- If the system extends the SCLn signal's low state hold time:
  Transmit the following data bit to the SDAn line prior to the SCLn line release ($t_{Rmax.}$ + $t_{SU:DAT}$ = 1000 + 250 = 1250 ns: Normal mode I^2C bus specification).

5. Cb: Total capacitance of one bus line (unit: pF)

Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

I^2C Bus Mode (Y Products (Products with On-Chip I^2C) Only)



Remark n = 0 (V850ES/KF1, V850ES/KG1), n = 0, 1 (V850ES/KJ1)

A/D Converter

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Resolution			10	10	10	bit
Overall error[Note 1]		4.0 ≤ AV_{REF0} ≤ 5.5 V		±0.2	±0.7	%FSR
		3.5 ≤ AV_{REF0} ≤ 4.0 V		±0.3	±0.9	%FSR
Conversion time	t_{CONV}	4.0 ≤ AV_{REF0} ≤ 5.5 V	14		60	μs
		3.5 ≤ AV_{REF0} ≤ 4.0 V	17		60	μs
Zero-scale error[Note 1]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±0.7	%FSR
		3.5 ≤ AV_{REF0} ≤ 4.0 V			±0.9	%FSR
Full-scale error[Note 1]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±0.7	%FSR
		3.5 ≤ AV_{REF0} ≤ 4.0 V			±0.9	%FSR
Non-linearity error[Note 2]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±5.5	LSB
		3.5 ≤ AV_{REF0} ≤ 4.0 V			±7.5	LSB
Differential linearity error[Note 2]		4.0 ≤ AV_{REF0} ≤ 5.5 V			±2.5	LSB
		3.5 ≤ AV_{REF0} ≤ 4.0 V			±3.0	LSB
Analog input voltage	V_{IAN}		0		AV_{REF0}	V
AV_{REF0} current	IA_{REF0}	When using A/D converter		1.0	2.0	mA
		When not using A/D converter		1.0	10	μA

Notes 1. Excluding quantization error (±0.05%FSR).

2. Excluding quantization error (±0.5LSB).

Remark LSB: Least Significant Bit
FSR: Full Scale Range

D/A Converter (V850ES/KG1, V850ES/KJ1 only)

(T_A = –40 to +125°C, V_{DD} = EV_{DD} = AV_{REF0} = 3.5 to 5.5 V, 3.5 V ≤ BV_{DD} ≤ V_{DD}, 3.5 V ≤ AV_{REF1} ≤ V_{DD}, V_{SS} = EV_{SS} = BV_{SS} = AV_{SS} = 0 V)

Parameter	Symbol	Conditions		MIN.	TYP.	MAX.	Unit
Resolution						8	bit
Overall error[Notes 1, 2]		Load condition = 2 MΩ				1.2	%FSR
		Load condition = 4 MΩ				0.8	%FSR
		Load condition = 10 MΩ				0.6	%FSR
Settling time[Notes 1, 2]		C = 30 pF	V_{DD} = 4.5 to 5.5 V			10	μs
			V_{DD} = 2.7 to 4.5 V			15	μs
Output resistance[Note 3]	R_O	Output data 55H			8		kΩ
AV_{REF1} current[Note 4]	IAV_{REF1}	During D/A conversion			1.5	3.0	mA
		When D/A conversion stopped			1.0	10	μA

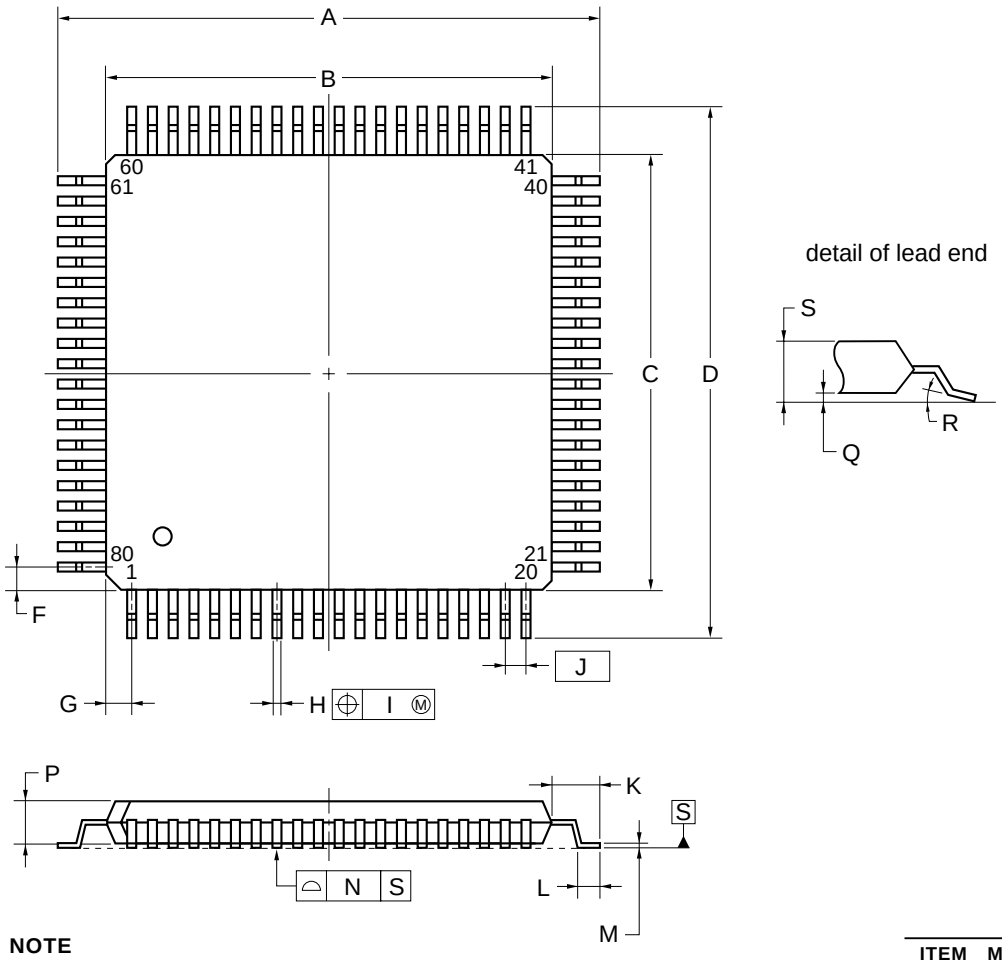
Notes 1. Excluding quantization error (±0.2%FSR).

2. R is the D/A converter output pin load resistance, and C is the D/A converter output pin load capacitance.

3. Value of 1 channel of D/A converter

4. Value of 2 channels of D/A converter

80-PIN PLASTIC QFP (14x14)



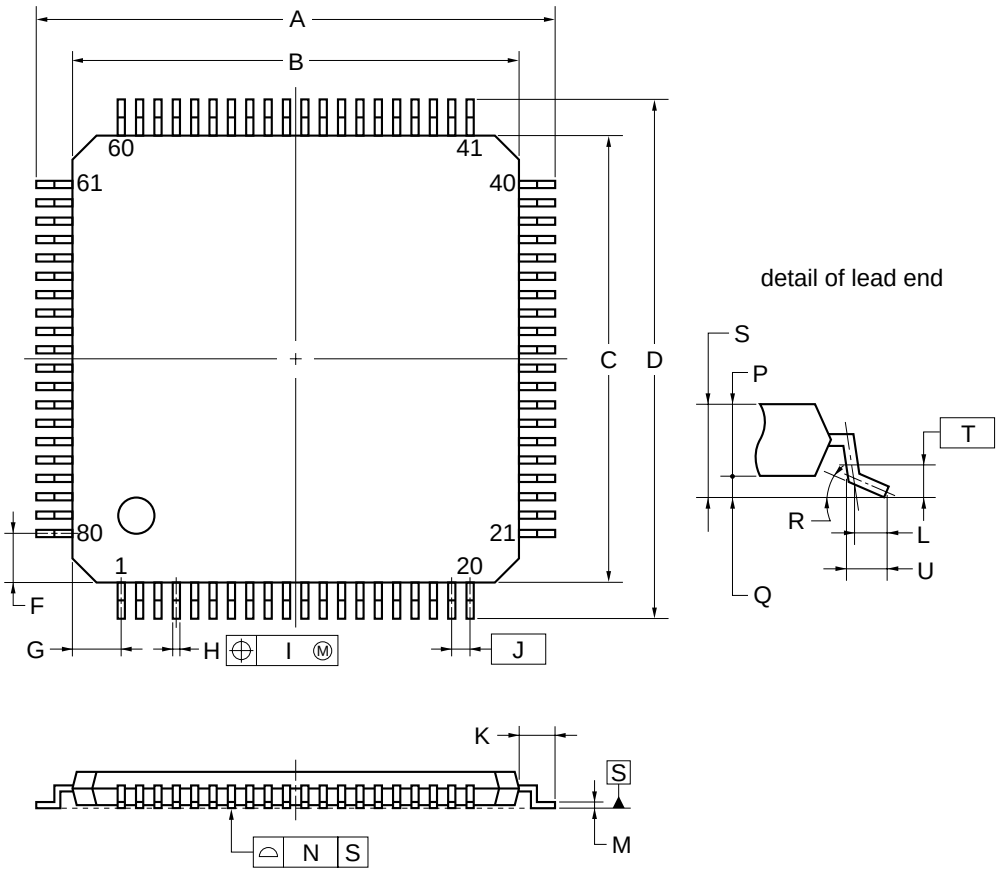
NOTE

Each lead centerline is located within 0.13 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	17.20±0.20
B	14.00±0.20
C	14.00±0.20
D	17.20±0.20
F	0.825
G	0.825
H	0.32±0.06
I	0.13
J	0.65 (T.P.)
K	1.60±0.20
L	0.80±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.10
P	1.40±0.10
Q	0.125±0.075
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.70 MAX.

P80GC-65-8BT-1

80-PIN PLASTIC TQFP (FINE PITCH) (12x12)



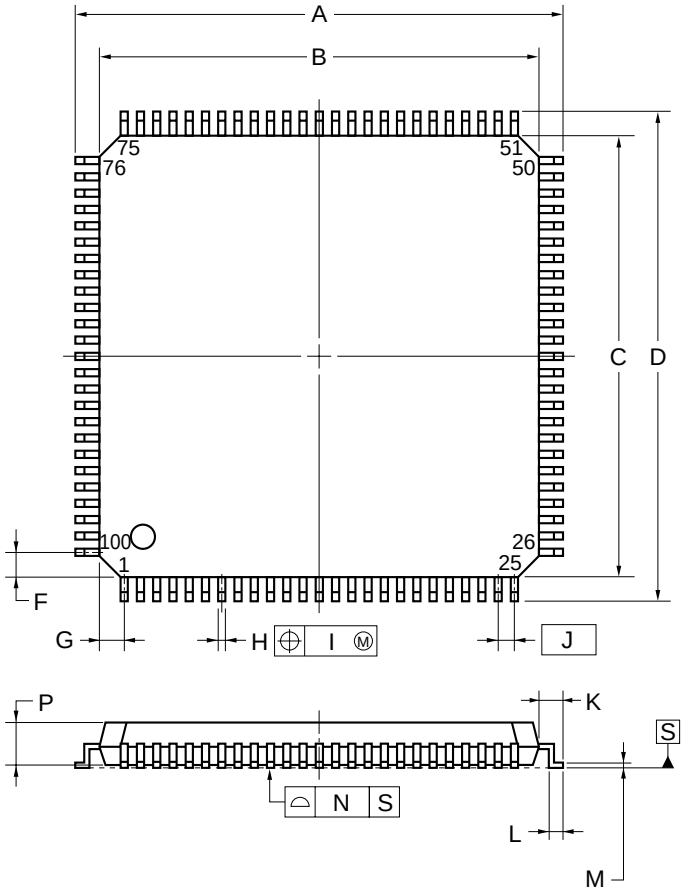
NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

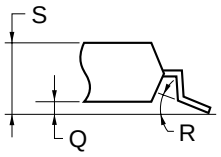
ITEM	MILLIMETERS
A	14.0±0.2
B	12.0±0.2
C	12.0±0.2
D	14.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5
M	0.145±0.05
N	0.08
P	1.0
Q	0.1±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.1±0.1
T	0.25
U	0.6±0.15

P80GK-50-9EU-1

100-PIN PLASTIC LQFP (FINE PITCH) (14x14)



detail of lead end



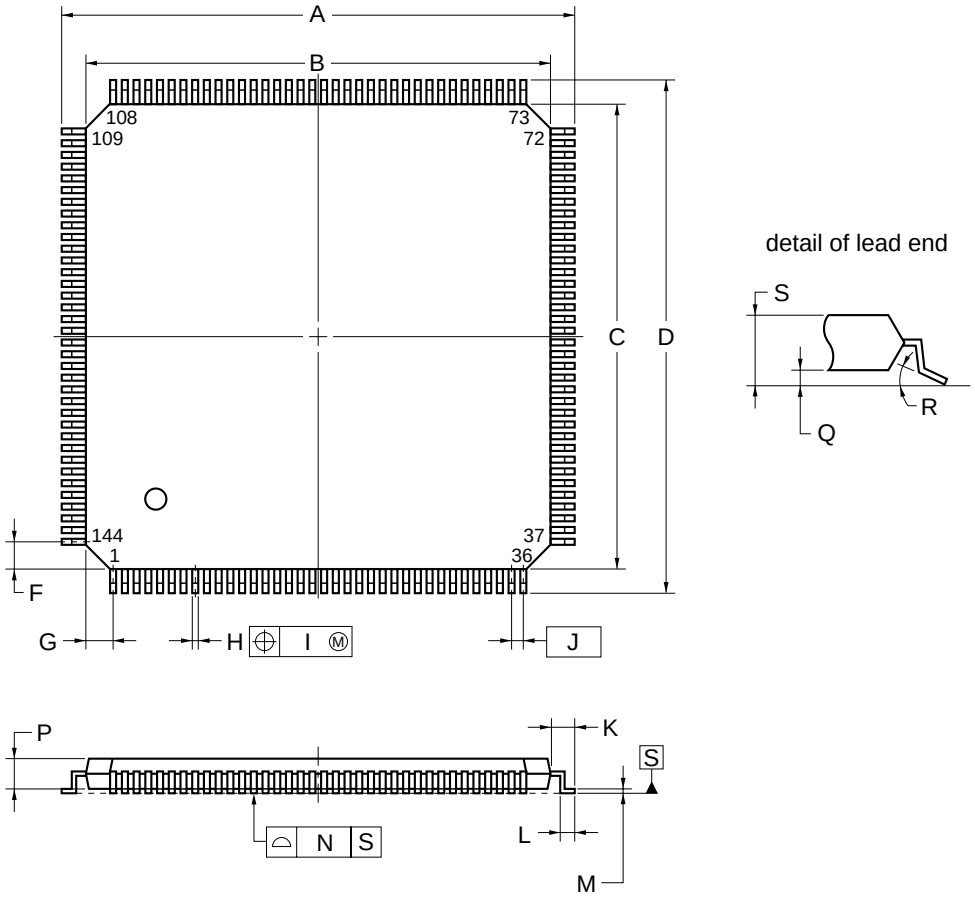
NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	16.00±0.20
B	14.00±0.20
C	14.00±0.20
D	16.00±0.20
F	1.00
G	1.00
H	$0.22^{+0.05}_{-0.04}$
I	0.08
J	0.50 (T.P.)
K	1.00±0.20
L	0.50±0.20
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.40±0.05
Q	0.10±0.05
R	$3^{\circ}{}^{+7^{\circ}}_{-3^{\circ}}$
S	1.60 MAX.

S100GC-50-8EU, 8EA-2

144-PIN PLASTIC LQFP (FINE PITCH) (20x20)



NOTE

Each lead centerline is located within 0.08 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS
A	22.0±0.2
B	20.0±0.2
C	20.0±0.2
D	22.0±0.2
F	1.25
G	1.25
H	0.22±0.05
I	0.08
J	0.5 (T.P.)
K	1.0±0.2
L	0.5±0.2
M	$0.17^{+0.03}_{-0.07}$
N	0.08
P	1.4
Q	0.10±0.05
R	$3^{\circ}{}^{+4^{\circ}}_{-3^{\circ}}$
S	1.5±0.1

S144GJ-50-UEN

CHAPTER 30 RECOMMENDED SOLDERING CONDITIONS

The V850ES/KF1, V850ES/KG1, and V850ES/KJ1 should be soldered and mounted under the following recommended conditions. For details of the recommended soldering conditions, see the Semiconductor Device Mount Manual website (http://www.necel.com/pkg/en/mount/index.html).

For soldering methods and conditions other than those recommended below, contact an NEC Electronics sales representative.

Table 30-1. Surface Mounting Type Soldering Conditions (1/3)

(1) μPD703208GK-xxx-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD703208YGK-xxx-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD703209GK-xxx-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD703209YGK-xxx-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD703210GK-xxx-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD703210YGK-xxx-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD70F3210GK-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD70F3210YGK-9EU: 80-pin plastic TQFP (fine pitch) (12 × 12)
μPD703212GC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703212YGC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703213GC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703213YGC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703214GC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD703214YGC-xxx-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD70F3214GC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)
μPD70F3214YGC-8EU: 100-pin plastic LQFP (fine pitch) (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	VP15-107-2
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remark Soldering conditions for the special grade (A), (A1), and (A2) products are the same as for the standard products.

Table 30. Surface Mounting Type Soldering Conditions (2/3)

(2) μPD703208GC-xxx-8BT: 80-pin plastic QFP (14 × 14)
μPD703208YGC-xxx-8BT: 80-pin plastic QFP (14 × 14)
μPD703209GC-xxx-8BT: 80-pin plastic QFP (14 × 14)
μPD703209YGC-xxx-8BT: 80-pin plastic QFP (14 × 14)
μPD703210GC-xxx-8BT: 80-pin plastic QFP (14 × 14)
μPD703210YGC-xxx-8BT: 80-pin plastic QFP (14 × 14)
μPD70F3210GC-8BT: 80-pin plastic QFP (14 × 14)
μPD70F3210YGC-8BT: 80-pin plastic QFP (14 × 14)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR35-107-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Two times or less, Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	VP15-107-2
Wave soldering	Solder bath temperature: 260°C max., Time: 10 seconds max., Count: Once, Preheating temperature: 120°C max. (package surface temperature), Exposure limit: 7 days[Note] (after that, prebake at 125°C for 10 hours)	WS60-107-1
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remark Soldering conditions for the special grade (A), (A1), and (A2) products are the same as for the standard products.

Table 30-1. Surface Mounting Type Soldering Conditions (3/3)

(3) μPD703216GJ-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
μPD703216YGJ-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
μPD703217GJ-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
μPD703217YGJ-xxx-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	IR35-103-2
VPS	Package peak temperature: 215°C, Time: 25 to 40 seconds (at 200°C or higher), Count: Two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 10 to 72 hours)	VP15-103-2
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

Remark Soldering conditions for the special grade (A), (A1), and (A2) products are the same as for the standard products.

(4) μPD70F3217GJ- UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)
μPD70F3217YGJ-UEN: 144-pin plastic LQFP (fine pitch) (20 × 20)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235°C, Time: 30 seconds max. (at 210°C or higher), Count: Two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 36 hours)	IR35-363-2
VPS	Package peak temperature: 215°C, Time: 40 seconds max. (at 200°C or higher), Count: Two times or less, Exposure limit: 3 days[Note] (after that, prebake at 125°C for 36 hours)	VP15-363-2
Partial heating	Pin temperature: 350°C max., Time: 3 seconds max. (per pin row)	–

Note After opening the dry pack, store it at 25°C or less and 65% RH or less for the allowable storage period.

Caution Do not use different soldering methods together (except for partial heating).

APPENDIX A REGISTER INDEX

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Symbol	Name	Unit	Page
ADCR	A/D conversion result register	ADC	401
ADIC	Interrupt control register	INTC	597
ADM	A/D converter mode register	ADC	398
ADS	Analog input channel specification register	ADC	400
ADTC0	Automatic data transfer address count register 0	CSI	482
ADTC1	Automatic data transfer address count register 1	CSI	482
ADTI0	Automatic data transfer interval specification register 0	CSI	488
ADTI1	Automatic data transfer interval specification register 1	CSI	488
ADTP0	Automatic data transfer address point specification register 0	CSI	486
ADTP1	Automatic data transfer address point specification register 1	CSI	486
ASIF0	Asynchronous serial interface transmission status register 0	UART	428
ASIF1	Asynchronous serial interface transmission status register 1	UART	428
ASIF2	Asynchronous serial interface transmission status register 2	UART	428
ASIM0	Asynchronous serial interface mode register 0	UART	425
ASIM1	Asynchronous serial interface mode register 1	UART	425
ASIM2	Asynchronous serial interface mode register 2	UART	425
ASIS0	Asynchronous serial interface status register 0	UART	427
ASIS1	Asynchronous serial interface status register 1	UART	427
ASIS2	Asynchronous serial interface status register 2	UART	427
AWC	Address wait control register	BCU	245
BCC	Bus cycle control register	BCU	246
BRGC0	Baud rate generator control register 0	UART	446
BRGC1	Baud rate generator control register 1	UART	446
BRGC2	Baud rate generator control register 2	UART	446
BRGCA0	Divisor selection register 0	CSI	486
BRGCA1	Divisor selection register 1	CSI	486
BRGIC	Interrupt control register	INIC	597
BSC	Bus size configuration register	BCU	234
CKSR0	Clock selection register 0	UART	445
CKSR1	Clock selection register 1	UART	445
CKSR2	Clock selection register 2	UART	445
CMP00	8-bit timer H compare register 00	Timer	344
CMP01	8-bit timer H compare register 01	Timer	344
CMP10	8-bit timer H compare register 10	Timer	344
CMP11	8-bit timer H compare register 11	Timer	344
CORAD0	Correction address register 0	ROMC	648
CORAD1	Correction address register 1	ROMC	648
CORAD2	Correction address register 2	ROMC	648
CORAD3	Correction address register 3	ROMC	648

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Symbol	Name	Unit	Page
CORCN	Correction control register	ROMC	649
CR000	16-bit timer capture/compare register 000	Timer	270
CR001	16-bit timer capture/compare register 001	Timer	272
CR010	16-bit timer capture/compare register 010	Timer	270
CR011	16-bit timer capture/compare register 011	Timer	272
CR020	16-bit timer capture/compare register 020	Timer	270
CR021	16-bit timer capture/compare register 021	Timer	272
CR030	16-bit timer capture/compare register 030	Timer	270
CR031	16-bit timer capture/compare register 031	Timer	272
CR040	16-bit timer capture/compare register 040	Timer	270
CR041	16-bit timer capture/compare register 041	Timer	272
CR050	16-bit timer capture/compare register 050	Timer	270
CR051	16-bit timer capture/compare register 051	Timer	272
CR5	16-bit timer compare register 5	Timer	337, 339, 340
CR50	8-bit timer compare register 50	Timer	325
CR51	8-bit timer compare register 51	Timer	325
CRC00	Capture/compare control register 00	Timer	277
CRC01	Capture/compare control register 01	Timer	277
CRC02	Capture/compare control register 02	Timer	277
CRC03	Capture/compare control register 03	Timer	277
CRC04	Capture/compare control register 04	Timer	277
CRC05	Capture/compare control register 05	Timer	277
CSI0IC0	Interrupt control register	INTC	597
CSI0IC1	Interrupt control register	INTC	597
CSI0IC2	Interrupt control register	INTC	597
CSIA0Bn	CSIA0 buffer RAMn (n = 0 to F)	CSI	488
CSIA1Bn	CSIA1 buffer RAMn (n = 0 to F)	CSI	488
CSIAIC0	Interrupt control register	INTC	597
CSIAIC1	Interrupt control register	INTC	597
CSIC0	Clocked serial interface clock selection register 0	CSI	458
CSIC1	Clocked serial interface clock selection register 1	CSI	458
CSIC2	Clocked serial interface clock selection register 2	CSI	458
CSIM00	Clocked serial interface mode register 00	CSI	456
CSIM01	Clocked serial interface mode register 01	CSI	456
CSIM02	Clocked serial interface mode register 02	CSI	456
CSIMA0	Serial operation mode specification register 0	CSI	483
CSIMA1	Serial operation mode specification register 1	CSI	483
CSIS0	Serial status register 0	CSI	484
CSIS1	Serial status register 1	CSI	484
CSIT0	Serial trigger register 0	CSI	485
CSIT1	Serial trigger register 1	CSI	485
DACS0	D/A conversion value setting register 0	DAC	418
DACS1	D/A conversion value setting register 1	DAC	418
DAM	D/A converter mode register	DAC	417

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Symbol	Name	Unit	Page
DWC0	Data wait control register 0	BCU	242
EXIMC	External bus interface mode control register	BCU	233
IIC0	IIC shift register 0	I^2C	515
IIC1	IIC shift register 1	I^2C	515
IICC0	IIC control register 0	I^2C	517
IICC1	IIC control register 1	I^2C	517
IICCL0	IIC clock selection register 0	I^2C	527
IICCL1	IIC clock selection register 1	I^2C	527
IICF0	IIC flag register 0	I^2C	525
IICF1	IIC flag register 1	I^2C	525
IICIC0	Interrupt control register	INTC	597
IICIC1	Interrupt control register	INTC	597
IICS0	IIC status register 0	I^2C	522
IICS1	IIC status register 1	I^2C	522
IICX0	IIC function expansion register 0	I^2C	528
IICX1	IIC function expansion register 1	I^2C	528
IMR0	Interrupt mask register 0	INTC	602
IMR1	Interrupt mask register 1	INTC	602
IMR2	Interrupt mask register 2	INTC	602
INTF0	External interrupt falling edge specification register 0	INTC	609
INTF9H	External interrupt falling edge specification register 9H	INTC	610
INTR0	External interrupt rising edge specification register 0	INTC	609
INTR9H	External interrupt rising edge specification register 9H	INTC	610
ISPR	In-service priority register	INTC	605
KRIC	Interrupt control register	INTC	597
KRM	Key return mode register	KR	623
OSTS	Oscillation stabilization time selection register	Standby	629
P0	Port 0 register	Port	126
P1	Port 1 register	Port	130
P3	Port 3 register	Port	133
P4	Port 4 register	Port	139
P5	Port 5 register	Port	142
P6	Port 6 register	Port	146
P7	Port 7 register	Port	152
P8	Port 8 register	Port	154
P9	Port 9 register	Port	159
PCC	Processor clock control register	CG	260
PCD	Port CD register	Port	170
PCM	Port CM register	Port	173
PCS	Port CS register	Port	177
PCT	Port CT register	Port	181
PDH	Port DH register	Port	185
PDL	Port DL register	Port	189
PF3H	Port 3 function register H	Port	136

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Symbol	Name	Unit	Page
PF4	Port 4 function register	Port	140
PF5	Port 5 function register	Port	143
PF6	Port 6 function register	Port	149
PF8	Port 8 function register	Port	155
PF9H	Port 9 function register H	Port	164
PFC3	Port 3 function control register	Port	136
PFC5	Port 5 function control register	Port	144
PFC6H	Port 6 function control register H	Port	149
PFC8	Port 8 function control register	Port	156
PFC9	Port 9 function control register	Port	164
PFM	Power-fail comparison mode register	ADC	402
PFT	Power-fail comparison threshold value register	ADC	402
PIC0	Interrupt control register	INTC	597
PIC1	Interrupt control register	INTC	597
PIC2	Interrupt control register	INTC	597
PIC3	Interrupt control register	INTC	597
PIC4	Interrupt control register	INTC	597
PIC5	Interrupt control register	INTC	597
PIC6	Interrupt control register	INTC	597
PLLCTL	PLL control register	CG	265, 393
PM0	Port 0 mode register	Port	126
PM1	Port 1 mode register	Port	130
PM3	Port 3 mode register	Port	134
PM4	Port 4 mode register	Port	139
PM5	Port 5 mode register	Port	142
PM6	Port 6 mode register	Port	147
PM8	Port 8 mode register	Port	154
PM9	Port 9 mode register	Port	160
PMC0	Port 0 mode control register	Port	127
PMC3	Port 3 mode control register	Port	135
PMC4	Port 4 mode control register	Port	139
PMC5	Port 5 mode control register	Port	143
PMC6	Port 6 mode control register	Port	148
PMC8	Port 8 mode control register	Port	155
PMC9	Port 9 mode control register	Port	160
PMCCM	Port CM mode control register	Port	175
PMCCS	Port CS mode control register	Port	179
PMCCT	Port CT mode control register	Port	183
PMCDH	Port DH mode control register	Port	187
PMCDL	Port DL mode control register	Port	190
PMCD	Port CD mode register	Port	171
PMCM	Port CM mode register	Port	174
PMCS	Port CS mode register	Port	178
PMCT	Port CT mode register	Port	182

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Symbol	Name	Unit	Page
PMDH	Port DH mode register	Port	186
PMDL	Port DL mode register	Port	189
PRCMD	Command register	CPU	110
PRM00	Prescaler mode register 00	Timer	280
PRM01	Prescaler mode register 01	Timer	280
PRM02	Prescaler mode register 02	Timer	280
PRM03	Prescaler mode register 03	Timer	280
PRM04	Prescaler mode register 04	Timer	280
PRM05	Prescaler mode register 05	Timer	280
PRSCM	Prescaler compare register	Timer	368
PRSM	Prescaler mode register	CG	367
PSC	Power save control register	Standby	627
PSMR	Power save mode register	Standby	628
PU0	Pull-up resistor option register 0	Port	128
PU1	Pull-up resistor option register 1	Port	130
PU3	Pull-up resistor option register 3	Port	137
PU4	Pull-up resistor option register 4	Port	140
PU5	Pull-up resistor option register 5	Port	144
PU6	Pull-up resistor option register 6	Port	150
PU8	Pull-up resistor option register 8	Port	156
PU9	Pull-up resistor option register 9	Port	168
RTBH0	Real-time output buffer register H0	RTP	387
RTBH1	Real-time output buffer register H1	RTP	387
RTBL0	Real-time output buffer register L0	RTP	387
RTBL1	Real-time output buffer register L1	RTP	387
RTPC0	Real-time output port control register 0	RTP	389
RTPC1	Real-time output port control register 1	RTP	389
RTPM0	Real-time output port mode register 0	RTP	388
RTPM1	Real-time output port mode register 1	RTP	388
RXB0	Receive buffer register 0	UART	429
RXB1	Receive buffer register 1	UART	429
RXB2	Receive buffer register 2	UART	429
SIO0	Serial I/O shift register 0	CSI	463
SIO1	Serial I/O shift register 1	CSI	463
SIO2	Serial I/O shift register 2	CSI	463
SIOA0	Serial I/O shift register A0	CSI	482
SIOA1	Serial I/O shift register A1	CSI	482
SIRB0	Clocked serial interface receive buffer register 0	CSI	459
SIRB0L	Clocked serial interface receive buffer register 0L	CSI	459
SIRB1	Clocked serial interface receive buffer register 1	CSI	459
SIRB1L	Clocked serial interface receive buffer register 1L	CSI	459
SIRB2	Clocked serial interface receive buffer register 2	CSI	459
SIRB2L	Clocked serial interface receive buffer register 2L	CSI	459

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Symbol	Name	Unit	Page
SIRBE0	Clocked serial interface read-only receive buffer register 0	CSI	460
SIRBE0L	Clocked serial interface read-only receive buffer register 0L	CSI	460
SIRBE1	Clocked serial interface read-only receive buffer register 1	CSI	460
SIRBE1L	Clocked serial interface read-only receive buffer register 1L	CSI	460
SIRBE2	Clocked serial interface read-only receive buffer register 2	CSI	460
SIRBE2L	Clocked serial interface read-only receive buffer register 2L	CSI	460
SOTB0	Clocked serial interface transmit buffer register 0	CSI	461
SOTB0L	Clocked serial interface transmit buffer register 0L	CSI	461
SOTB1	Clocked serial interface transmit buffer register 1	CSI	461
SOTB1L	Clocked serial interface transmit buffer register 1L	CSI	461
SOTB2	Clocked serial interface transmit buffer register 2	CSI	461
SOTB2L	Clocked serial interface transmit buffer register 2L	CSI	461
SOTBF0	Clocked serial interface first stage transmit buffer register 0	CSI	462
SOTBF0L	Clocked serial interface first stage transmit buffer register 0L	CSI	462
SOTBF1	Clocked serial interface first stage transmit buffer register 1	CSI	462
SOTBF1L	Clocked serial interface first stage transmit buffer register 1L	CSI	462
SOTBF2	Clocked serial interface first stage transmit buffer register 2	CSI	462
SOTBF2L	Clocked serial interface first stage transmit buffer register 2L	CSI	462
SREIC0	Interrupt control register	INTC	597
SREIC1	Interrupt control register	INTC	597
SREIC2	Interrupt control register	INTC	597
SRIC0	Interrupt control register	INTC	597
SRIC1	Interrupt control register	INTC	597
SRIC2	Interrupt control register	INTC	597
STIC0	Interrupt control register	INTC	597
STIC1	Interrupt control register	INTC	597
STIC2	Interrupt control register	INTC	597
SVA1	Slave address register 1	I^2C	515
SVA0	Slave address register 0	I^2C	515
SYS	System status register	CPU	110
TCL50	Timer clock selection register 50	Timer	326
TCL51	Timer clock selection register 51	Timer	326
TM00	16-bit timer counter 00	Timer	270
TM01	16-bit timer counter 01	Timer	270
TM02	16-bit timer counter 02	Timer	270
TM03	16-bit timer counter 03	Timer	270
TM04	16-bit timer counter 04	Timer	270
TM05	16-bit timer counter 05	Timer	270
TM0IC00	Interrupt control register	INTC	597
TM0IC01	Interrupt control register	INTC	597
TM0IC10	Interrupt control register	INTC	597
TM0IC11	Interrupt control register	INTC	597
TM0IC20	Interrupt control register	INTC	597
TM0IC21	Interrupt control register	INTC	597

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Symbol	Name	Unit	Page
TM0IC30	Interrupt control register	INTC	597
TM0IC31	Interrupt control register	INTC	597
TM0IC40	Interrupt control register	INTC	597
TM0IC41	Interrupt control register	INTC	597
TM0IC50	Interrupt control register	INTC	597
TM0IC51	Interrupt control register	INTC	597
TM5	16-bit timer counter 5	Timer	337, 339, 340
TM50	8-bit timer counter 50	Timer	324
TM51	8-bit timer counter 51	Timer	324
TM5IC0	Interrupt control register	INTC	597
TM5IC1	Interrupt control register	INTC	597
TMC00	16-bit timer mode control register 00	Timer	274
TMC01	16-bit timer mode control register 01	Timer	274
TMC02	16-bit timer mode control register 02	Timer	274
TMC03	16-bit timer mode control register 03	Timer	274
TMC04	16-bit timer mode control register 04	Timer	274
TMC05	16-bit timer mode control register 05	Timer	274
TMC50	8-bit timer mode control register 50	Timer	334
TMC51	8-bit timer mode control register 51	Timer	334
TMCYC0	8-bit timer H carrier control register 0	Timer	348
TMCYC1	8-bit timer H carrier control register 1	Timer	348
TMHIC0	Interrupt control register	INTC	597
TMHIC1	Interrupt control register	INTC	597
TMHMD0	8-bit timer H mode register 0	Timer	345
TMHMD1	8-bit timer H mode register 1	Timer	345
TOC00	16-bit timer output control register 00	Timer	278
TOC01	16-bit timer output control register 01	Timer	278
TOC02	16-bit timer output control register 02	Timer	278
TOC03	16-bit timer output control register 03	Timer	278
TOC04	16-bit timer output control register 04	Timer	278
TOC05	16-bit timer output control register 05	Timer	278
TXB0	Transmit buffer register 0	UART	430
TXB1	Transmit buffer register 1	UART	430
TXB2	Transmit buffer register 2	UART	430
VSWC	System wait control register	CPU	112
WDCS	Watchdog timer clock selection register	WDT	378
WDT1IC	Interrupt control register	INTC	597
WDTE	Watchdog timer enable register	WDT	384
WDTM1	Watchdog timer mode register 1	WDT	379, 607
WDTM2	Watchdog timer mode register 2	WDT	383
WTIC	Interrupt control register	INTC	597
WTIIC	Interrupt control register	INTC	597
WTM	Watch timer operation mode register	WT	371

APPENDIX B REVISION HISTORY

B.1 Major Revisions in This Edition

(1/2)

Page	Description
Throughout	Addition of the following special quality grade products μPD703208(A1), 703208(A2), 703208Y(A1), 703208Y(A2), 703209(A1), 703209(A2), 703209Y(A1), 703209Y(A2), 703210(A1), 703210(A2), 703210Y(A1), 703210Y(A2), 703212(A1), 703212(A2), 703212Y(A1), 703212Y(A2), 703213(A1), 703213(A2), 703213Y(A1), 703213Y(A2), 703214(A1), 703214(A2), 703214Y(A1), 703214Y(A2), 703216(A1), 703216(A2), 703216Y(A1), 703216Y(A2), 703217(A1), 703217(A2), 703217Y(A1), 703217Y(A2)
p.54	Addition of **1.5 Overview of Functions**
p.67	Modification of **Table 2-4 Pin Operation Status in Operation Modes of V850ES/KJ1**
p.68	Modification of **Table 2-5 Pin Operation Status in Operation Modes of V850ES/KG1**
p.69	Modification of **Table 2-6 Pin Operation Status in Operation Modes of V850ES/KJ1**
p.94	Addition of **3.4.5 Recommended usage method for address area**
p.120	Addition of **Caution** in **Table 4-7 Alternate-Function Pins of Port 0**
p.131	Addition of **Caution** in **Table 4-9 Alternate-Function Pins of Port 3 (V850ES/KF1)**
p.132	Addition of **Caution** in **Table 4-10 Alternate-Function Pins of Port 3 (V850ES/KG1, V850ES/KJ1)**
p.138	Addition of **Caution** in **Table 4-11 Alternate-Function Pins of Port 4**
p.145	Addition of **Caution** in **Table 4-13 Alternate-Function Pins of Port 5**
p.153	Addition of **Caution** in **Table 4-16 Alternate-Function Pins of Port 8 (V850ES/KJ1)**
p.158	Addition of **Caution** in **Table 4-17Alternate-Function Pins of Port 9 (V850ES/KF1)**
p.158	Addition of **Caution** in **Table 4-18 Alternate-Function Pins of Port 9 (V850ES/KG1, V850ES/KJ1)**
p.168	Modification of **4.3.9 (1) (f) Pull-up resistor option register 9 (PU9)**
p.218	Modification of P38 and P39 in **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**
p.222	Modification of P92 in **Table 4-29 Settings When Port Pins Are Used for Alternate Functions**
p.191	Addition of **4.4 Bock Diagram**
p.225	Addition of **4.6 Cautions**
p.229	Modification of **5.2.1 Pin status when internal ROM, internal RAM, or on-chip peripheral I/O is accessed**
p.256	Addition of **5.11 Cautions**
p.262	Modification of example of setting in **6.3 (1) (a) Example of setting main clock operation → subclock operation**
p.263	Modification of example of setting in **6.3 (1) (b) Example of setting subclock operation → main clock operation**
p.276	Addition of **Table 7-5 I/O Configuration of Each Channel**
p.289	Modification of **Figure 7-4 Timing of Interval Timer Operation**
p.293	Modification of **Figure 7-7 PPG Output Operation Timing**
p.362	Modification of **Figure 9-8 Carrier Generator Mode**
p.404	Modification of **13.5.1 Basic operation**
p.405	Modification of **13.5.3 Power fail monitoring function**
p.407	Modification of **13.6 Cautions**
p.425	Addition of **Caution** in **15.4 (1) Asynchronous serial interface mode register n (ASIMn)**
p.435	Addition of **Caution** in **15.6.3 Continuous transmission operation**

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Page	Description
p.464	Addition of **Table 16-1 Use of Each Buffer Register**
p.563	Addition of **18.14.2 When communication reservation function is disabled (IICRSVn bit of IICFn register = 1)**
p.565	Modification of **Figure 18-16 Master Operation Flowchart (1)**
p.566	Addition of **18.16.2 Master operation 2**
p.567	Modification of **18.16.3 Slave operation**
p.621	Addition of **19.10 Cautions**
p.624	Modification of **Note** in **Table 21-1 Standby Modes**
p.645	Modification of **Figure 23-1 Regulator**
p.650	Modification of **Figure 24-2 ROM Correction Operation and Program Flow**
p.670	Modification of Absolute Maximum Rating in **CHAPTER 26 ELECTRICAL CHARACTERISTICS (STANDARD PRODUCTS, SPECIAL GRADE (a) PRODUCTS)**
p.673	Modification of Operating Conditions in **CHAPTER 26 ELECTRICAL CHARACTERISTICS (STANDARD PRODUCTS, SPECIAL GRADE (a) PRODUCTS)**
p.677	Modification of conditions of DC Characteristics in **CHAPTER 26 ELECTRICAL CHARACTERISTICS (STANDARD PRODUCTS, SPECIAL GRADE (a) PRODUCTS)**
p.681	Addition of Note for DC Characteristics in **CHAPTER 26 ELECTRICAL CHARACTERISTICS (STANDARD PRODUCTS, SPECIAL GRADE (a) PRODUCTS)**
p.690	Modification of timing chart of Bus Hold: In Multiplex Bus Mode in **CHAPTER 26 ELECTRICAL CHARACTERISTICS (STANDARD PRODUCTS, SPECIAL GRADE (a) PRODUCTS)**
p.701	Modification of Basic Operation in **CHAPTER 26 ELECTRICAL CHARACTERISTICS (STANDARD PRODUCTS, SPECIAL GRADE (a) PRODUCTS)**
p.702	Modification of UART timing in **CHAPTER 26 ELECTRICAL CHARACTERISTICS (STANDARD PRODUCTS, SPECIAL GRADE (a) PRODUCTS)**
p.712	Addition of **CHAPTER 27 ELECTRICAL CHARACTERISTICS (SPECIAL GRADE (A1) PRODUCTS)**
p.734	Addition of **CHAPTER 28 ELECTRICAL CHARACTERISTICS (SPECIAL GRADE (A2) PRODUCTS)**
Major Revisions in This Modification	
p.279	Addition of **Caution** in **7.3 (3) 16-bit timer output control register 0n (TOC0n)**
p.328	Modification of description of **Caution 3** in **8.3 (2) 8-bit timer mode control registers 50 and 51 (TMC50, TMC51)**
p.420	Modification of description in **14.4.3 Cautions**
p.420	Addition of **Caution** in **Figure 14-2 Example of External Pin Connection**
p.653	Modification of **Figure 25-1 Wiring Example of V850ES/KF1 Flash Writing Adapter (FA-80GC-8BT, FA-80GK-9EU)**
p.655	Modification of **Figure 25-2 Wiring Example of V850ES/KG1 Flash Writing Adapter (FA-100GC-8EU)**
p.657	Modification of **Figure 25-3 Wiring Example of V850ES/KJ1 Flash Writing Adapter (FA-144GJ-UEN)**

B.2 Revision History up to Previous Edition

The following table shows the revision history up to the previous edition. The “Applied to:” column indicates the chapters of each edition in which the revision was applied.

(1/3)

Edition	Major Revision from Previous Edition	Applied to:
2nd	Change of description in **Figure 12-1 Block Diagram of D/A Converter**	**CHAPTER 12 D/A CONVERTER**
	Addition of **Caution** in **14.3.4 Interrupt control register (xxICn)**	**CHAPTER 14 INTERRUPT/EXCEPTION PROCESSING FUNCTION**
	Addition of **Caution** in **14.3.6 In-service priority register (ISPR)**	
	Addition of **CHAPTER 21 ELECTRICAL SPECIFICATIONS (TARGET VALUES)**	**CHAPTER 21 ELECTRICAL SPECIFICATIONS (TARGET VALUES)**
	Addition of **CHAPTER 22 PACKAGE DRAWINGS**	**CHAPTER 22 PACKAGE DRAWINGS**
	Addition of **APPENDIX A REGISTER INDEX**	**APPENDIX A REGISTER INDEX**
3rd	• Addition of the following special quality grade products. μPD703208(A), 703208Y(A), 703209(A), 703209Y(A), 703210(A), 703210Y(A), 703212(A), 703212Y(A), 703213(A), 703213Y(A), 703214(A), 703214Y(A), 703216(A), 703216Y(A), 703217(A), 703217Y(A), 70F3210(A), 70F3210Y(A), 70F3214(A), 70F3214Y(A), 70F3217(A), 70F3217Y(A)	Throughout
	Addition of **Caution** in **1.2.4 Pin configuration (top view) (V850ES/KF1)**	**CHAPTER 1 INTRODUCTION**
	Addition of **Caution** in **1.3.4 Pin configuration (top view) (V850ES/KG1)**	
	Addition of **Caution** in **1.4.4 Pin configuration (top view) (V850ES/KJ1)**	
	Addition of description in **CHAPTER 2 PIN FUNCTIONS** and addition of **Table 2-1 Pin I/O Buffer Power Supplies**	**CHAPTER 2 PIN FUNCTIONS**
	Modification of description on recommended connection of P70 to P77, P78 to P715, IC, V_{PP}, and XT1 in **2.4 Pin I/O Circuits and Recommended Connection of Unused Pins**	
	Modification of description in **3.4.8 (2) Access to special on-chip peripheral I/O registers**	**CHAPTER 3 CPU FUNCTIONS**
	Modification of description in **5.11 Bus Timing**	**CHAPTER 5 BUS CONTROL FUNCTION**
	Addition of **5.12 Cautions**	
	Addition of description on the main clock oscillator in **6.1 Overview**	**CHAPTER 6 CLOCK GENERATION FUNCTION**
	Addition of description in **6.2 (1) Main clock oscillator**	
	Addition of **Caution 3** in **6.3 (1) Processor clock control register (PCC)**	
	Addition of description in **CHAPTER 7 16-BIT TIMER/EVENT COUNTERS 00 TO 05**	**CHAPTER 7 16-BIT TIMER/EVENT COUNTERS 00 TO 05**
	Modification of description of **Caution 4** in **7.2 (2) 16-bit timer capture/compare register 0n0 (CR0n0)**	
	Modification of description of **Caution 4** in **7.2 (3) 16-bit timer capture/compare register 0n1 (CR0n1)**	
	Modification of description of **Caution 1** in **7.3 (3) 16-bit timer output control register 0n (TOC0n)**	
	Addition of setting procedures and modification of description in **7.4.1 Operation as interval timer (16 bits)**	

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Edition	Major Revision from Previous Edition	Applied to:
3rd	Addition of setting procedures in **7.4.2 PPG output operation**	**CHAPTER 7 16-BIT TIMER/EVENT COUNTERS 00 TO 05**
	Addition of **Figure 7-6 Configuration of PPG Output**	
	Addition of **Figure 7-7 PPG Output Operation Timing**	
	Addition of setting procedures in **7.4.3 Pulse width measurement**	
	Addition of setting procedures and addition of **Caution 2** in **7.4.4 Operation as external event counter**	
	Addition of setting procedures and addition of **Caution** in **7.4.5 Square-wave output operation**	
	Addition of setting procedures in **7.4.6 One-shot pulse output operation**	
	Addition of **Caution 2** in **7.4.6 (1) One-shot pulse output with software trigger (16-bit timer/event counters 00, 01, 04 and 05 only)**	
	Addition of **Caution 2** in **7.4.6 (2) One-shot pulse output with external trigger (16-bit timer/event counters 04 and 05 only)**	
	Addition of **Caution** in **7.4.7 (10) (b) When setting CR0n0, CR0n1 to compare mode**	
	Addition of description in **CHAPTER 8 8-BIT TIMER/EVENT COUNTERS 50 AND 51**	**CHAPTER 8 8-BIT TIMER/EVENT COUNTERS 50 AND 51**
	Addition of description in **CHAPTER 9 8-BIT TIMERS H0 AND H1**	**CHAPTER 9 8-BIT TIMERS H0 AND H1**
	Addition of **Caution 3** in **9.3 (1) (a) 8-bit timer H mode register 0 (TMHMD0)**	
	Addition of **Caution 3** in **9.3 (1) (b) 8-bit timer H mode register 1 (TMHMD1)**	
	Addition of **Caution 2** in **Figure 9-7 Transfer Timing**	
	Addition of **Caution 4** in **9.4.3 (4) Timing chart**	
	Addition of **13.4 Relationship Between Analog Input Voltage and A/D Conversion Result**	**CHAPTER 13 A/D CONVERTER**
	Addition of **13.6 (3) A/D converter sampling time and A/D conversion start delay time**	
	Addition of **13.7 How to Read A/D Converter Characteristics Table**	
	Addition of description in **CHAPTER 15 ASYNCHRONOUS SERIAL INTERFACE (UART)**	**CHAPTER 15 ASYNCHRONOUS SERIAL INTERFACE (UART)**
	Modification of description in **Figure 15-6 Continuous Transmission Starting Procedure**	
	Addition of description in **CHAPTER 16 CLOCKED SERIAL INTERFACE 0 (CSI0)**	**CHAPTER 16 CLOCKED SERIAL INTERFACE 0 (CSI0)**
	Modification of description in **CHAPTER 17 CLOCKED SERIAL INTERFACE A (CSIA) WITH AUTOMATIC TRANSMIT/RECEIVE FUNCTION**	**CHAPTER 17 CLOCKED SERIAL INTERFACE A (CSIA) WITH AUTOMATIC TRANSMIT/RECEIVE FUNCTION**
	Addition of description in **CHAPTER 18 I^2C BUS**	**CHAPTER 18 I^2C BUS**
	Addition to **Cautions** in **Table 25-1 Wiring Between μPD70F3210 and 70F3210Y (V850ES/KF1), and PG-FP3**	**CHAPTER 25 FLASH MEMORY**
	Addition of **Figure 25-1 Wiring Example of V850ES/KF1 Flash Writing Adapter (FA-80GC-8BT, FA-80GK-9EU)**	
	Addition of **Cautions** in **Table 25-2 Wiring Between μPD70F3214 and 70F3214Y (V850ES/KG1), and PG-FP3**	

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Edition	Major Revision from Previous Edition	Applied to:
3rd	Addition of **Figure 25-2 Wiring Example of V850ES/KG1 Flash Writing Adapter (FA-100GC-8EU)**	**CHAPTER 25 FLASH MEMORY**
	Addition of **Cautions** in **Table 25-3 Wiring Between μPD70F3217 and 70F3217Y (V850ES/KJ1), and PG-FP3**	
	Addition of **Figure 25-3 Wiring Example of V850ES/KJ1 Flash Writing Adapter (FA-144GJ-UEN)**	
	Addition of **Note 1** and description in **Absolute Maximum Ratings** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	**CHAPTER 26 ELECTRICAL SPECIFICATIONS**
	Addition of description on storage temperature in **Absolute Maximum Ratings** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Addition of **(i) Murata Manufacturing Co., Ltd.: Ceramic resonator (T_A = –40 to +85°C)** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Change of values of supply current (flash memory version) in **DC Characteristics** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Change of values of supply current (mask ROM version) in **DC Characteristics** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Addition of **Caution** and a timing chart in **Data Retention Characteristics** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Addition of **Caution** in **Bus Timing (1) (a) CLKOUT asynchronous: In multiplex bus mode (2/2)** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Addition of **Caution 2** in **Bus Timing (2) (a) Read cycle (CLKOUT asynchronous): In separate bus mode (1/2)** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Addition of **Cautions** in **Bus Timing (2) (a) Read cycle (CLKOUT asynchronous): In separate bus mode (2/2)** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Addition of **Caution 2** in **Bus Timing (2) (c) Write cycle (CLKOUT asynchronous): In separate bus mode (1/2)** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Addition of **Cautions** in **Bus Timing (2) (c) Write cycle (CLKOUT asynchronous): In separate bus mode (2/2)** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Addition of description in **Basic Operation** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Addition of description in **Flash Memory Programming Characteristics** in **CHAPTER 26 ELECTRICAL SPECIFICATIONS**	
	Addition of **CHAPTER 28 RECOMMENDED SOLDERING CONDITIONS**	**CHAPTER 28 RECOMMENDED SOLDERING CONDITIONS**
	Addition of **APPENDIX B REVISION HISTORY**	**APPENDIX B REVISION HISTORY**