

4M-BIT CMOS STATIC RAM

256K-WORD BY 16-BIT

EXTENDED TEMPERATURE OPERATION

Description

The μ PD444012L-X is a high speed, low power, 4,194,304 bits (262,144 words by 16 bits) CMOS static RAM.

The μ PD444012L-X has two chip enable pins (/CE1, CE2) to extend the capacity.

The μ PD444012L-X is packed in 48-pin plastic TSOP (I).

Features

- 262,144 words by 16 bits organization
- ★ • Fast access time: 70, 85, 100, 120, 150, 200 ns (MAX.)
- Byte data control: /LB (I/O1 - I/O8), /UB (I/O9 - I/O16)
- Low voltage operation
(B version: $V_{CC} = 2.7$ to 3.6 V, C version: $V_{CC} = 2.2$ to 3.6 V, D version: $V_{CC} = 1.8$ to 3.6 V)
- Operating ambient temperature: $T_A = -25$ to $+85$ °C
- Output Enable input for easy application
- Two Chip Enable inputs: /CE1, CE2

Part number	Access time ns (MAX.)	Operating supply voltage V	Operating ambient temperature °C	Supply current		
				At operating mA (MAX.)	At standby μ A (MAX.)	At data retention μ A (MAX.)
μ PD444012L-BxxX	70, 85	2.7 to 3.6	-25 to +85	40	7	7
μ PD444012L-CxxX	100, 120	2.2 to 3.6				
★ μ PD444012L-DxxX ^{Note}	150, 200	1.8 to 3.6				

Note Under development

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Not all devices/types available in every country. Please check with local NEC representative for availability and additional information.

Ordering Information

Part number	Package	Access times (MAX.)	Operating supply voltage V	Operating temperature °C	Remark	
μPD444012LGY-B70X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	70	2.7 to 3.6	-25 to +85	B version	
μPD444012LGY-B70X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)					
μPD444012LGY-B85X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	85				
μPD444012LGY-B85X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)					
μPD444012LGY-C10X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	100	2.2 to 3.6			C version
μPD444012LGY-C10X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)					
μPD444012LGY-C12X-MJH	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	120				
μPD444012LGY-C12X-MKH	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)					
★ μPD444012LGY-D15X-MJH ^{Note}	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	150	1.8 to 3.6			D version
★ μPD444012LGY-D15X-MKH ^{Note}	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)					
★ μPD444012LGY-D20X-MJH ^{Note}	48-pin Plastic TSOP (I) (12×18 mm) (Normal bent)	200				
★ μPD444012LGY-D20X-MKH ^{Note}	48-pin Plastic TSOP (I) (12×18 mm) (Reverse bent)					

Note Under development

Pin Configuration (Marking Side)

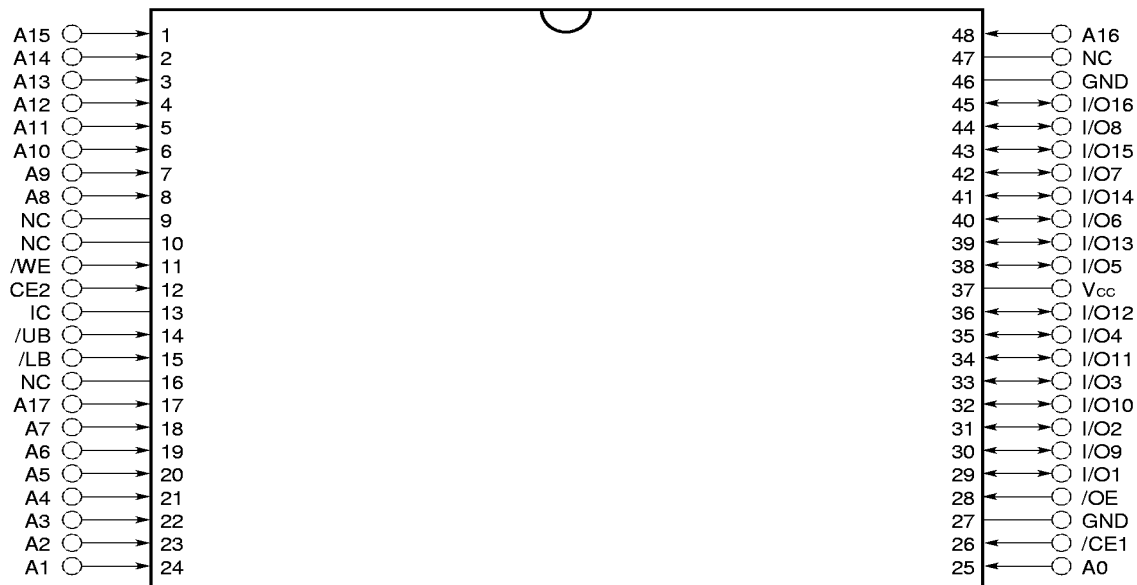
/xxx indicates active low signal.

48-pin Plastic TSOP (I) (12×18 mm) (Normal Bent)

[μPD444012LGY-BxxX-MJH]

[μPD444012LGY-CxxX-MJH]

[μPD444012LGY-DxxX-MJH]



- A0 - A17 : Address inputs
- I/O1 - I/O16 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
- /WE : Write Enable
- /OE : Output Enable
- /LB, /UB : Byte data select
- V_{cc} : Power supply
- GND : Ground
- NC : No Connection
- IC^{Note} : Internal Connection

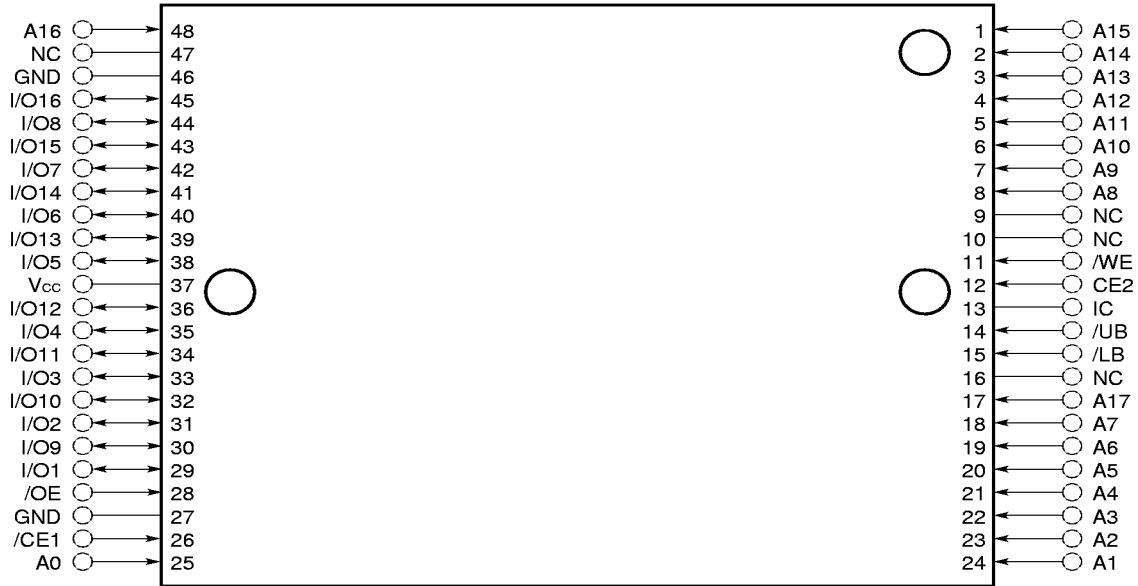
Note Leave this pin unconnected or connect to GND.

48-pin Plastic TSOP (I) (12×18 mm) (Reverse Bent)

[μPD444012LGY-BxxX-MKH]

[μPD444012LGY-CxxX-MKH]

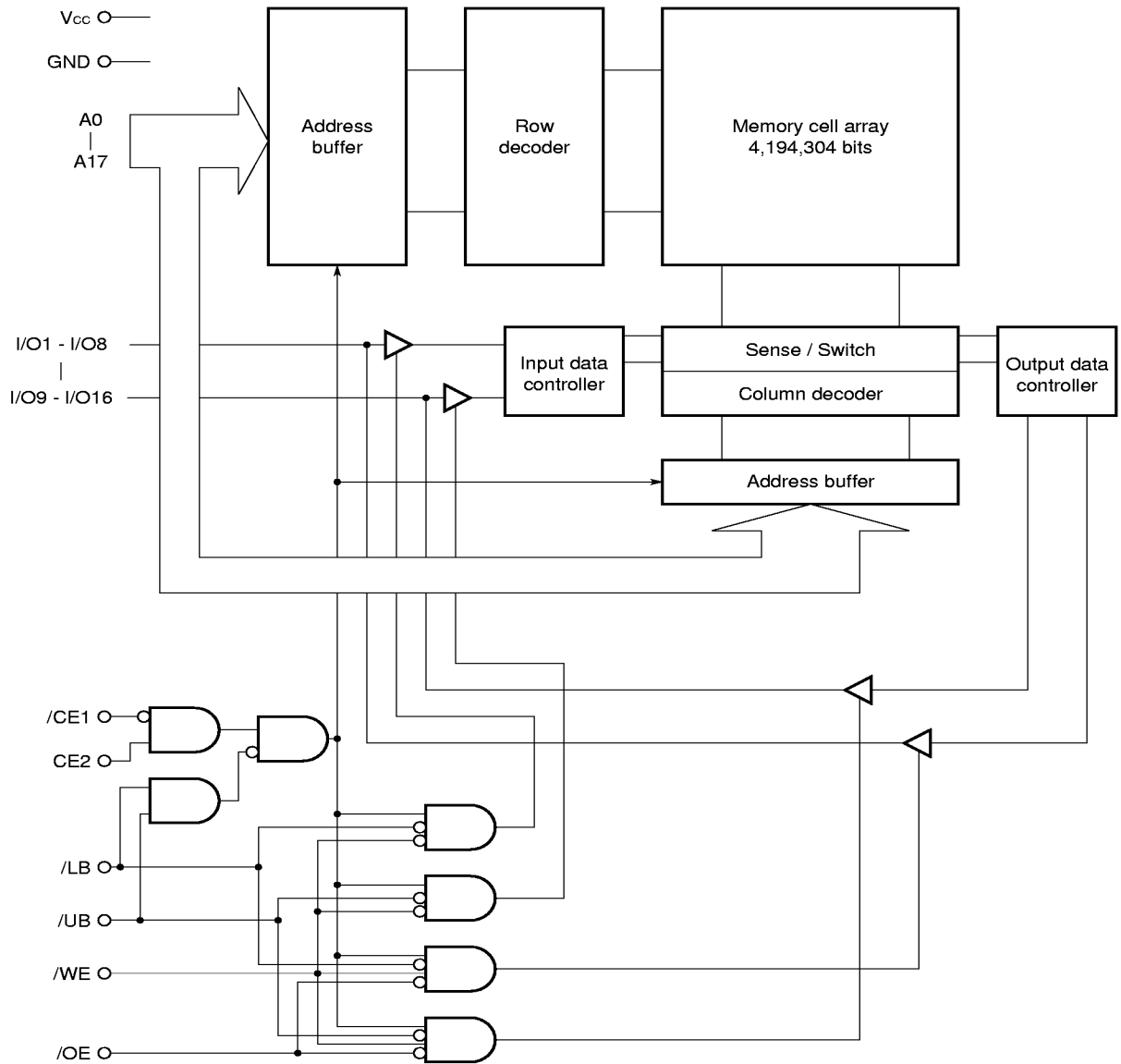
[μPD444012LGY-DxxX-MKH]



- A0 - A17 : Address inputs
- I/O1 - I/O16 : Data inputs / outputs
- /CE1, CE2 : Chip Enable 1, 2
- /WE : Write Enable
- /OE : Output Enable
- /LB, /UB : Byte data select
- V_{cc} : Power supply
- GND : Ground
- NC : No Connection
- IC^{Note} : Internal Connection

Note Leave this pin unconnected or connect to GND.

Block Diagram



Truth Table

/CE1	CE2	/OE	/WE	/LB	/UB	Mode	I/O		Supply current
							I/O1 - I/O8	I/O9 - I/O16	
H	x	x	x	x	x	Not selected	High impedance	High impedance	I _{SB}
x	L	x	x	x	x				
L	H	H	H	x	x	Output disable	High impedance	High impedance	I _{CCA}
		L	H	L	L	Word read	D _{OUT}	D _{OUT}	
				L	H	Lower byte read	D _{OUT}	High impedance	
				H	L	Upper byte read	High impedance	D _{OUT}	
		x	L	L	L	Word write	D _{IN}	D _{IN}	
				L	H	Lower byte write	D _{IN}	High impedance	
				H	L	Upper byte write	High impedance	D _{IN}	
x	x	x	x	H	H	Not selected	High impedance	High impedance	I _{SB} ^{Note}

Note /CE1, CE2 = V_{IH} or V_{IL}

Remark x : Don't care

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V _{CC}		-0.5 ^{Note} to +4.0	V
Input / Output voltage	V _I		-0.5 ^{Note} to V _{CC} + 0.4 (4.0 V MAX.)	V
Operating ambient temperature	T _A		-25 to +85	°C
Storage temperature	T _{stg}		-55 to +125	°C

Note -3.0 V (MIN.) (Pulse width : 30 ns)

Caution Exposing the device to stress above those listed in Absolute Maximum Rating could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Recommended Operating Conditions

Parameter	Symbol	Condition	μPD444012L-BxxX		μPD444012L-CxxX		μPD444012L-DxxX		Unit
			MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	
Supply voltage	V _{CC}		2.7	3.6	2.2	3.6	1.8	3.6	V
High level input voltage	V _{IH}	2.7 V ≤ V _{CC} ≤ 3.6 V	2.4	V _{CC} + 0.4	2.4	V _{CC} + 0.4	2.4	V _{CC} + 0.4	V
		2.2 V ≤ V _{CC} < 2.7 V	-	-	2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	
		1.8 V ≤ V _{CC} < 2.2 V	-	-	-	-	1.6	V _{CC} + 0.2	
Low level input voltage	V _{IL}		-0.3 ^{Note}	+0.5	-0.3 ^{Note}	+0.3	-0.3 ^{Note}	+0.2	V
Operating ambient temperature	T _A		-25	+85	-25	+85	-25	+85	°C

Note -1.5 V (MIN.) (Pulse width: 30 ns)

Capacitance (T_A = 25 °C, f = 1 MHz)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C _{IN}	V _{IN} = 0 V			8	pF
Input / Output capacitance	C _{I/O}	V _{I/O} = 0 V			10	pF

- Remarks**
1. V_{IN} : Input voltage
 2. These parameters are periodically sampled and not 100% tested.

DC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

Parameter	Symbol	Test condition	V _{CC} ≥ 2.7 V			V _{CC} ≥ 2.2 V			V _{CC} ≥ 1.8 V			Unit
			μPD444012L-BxxX			μPD444012L-CxxX			μPD444012L-DxxX			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input leakage current	I _{LI}	V _{IN} = 0 V to V _{CC}	-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
I/O leakage current	I _{LO}	V _{I/O} = 0 V to V _{CC} , /CE1 = V _{IH} or CE2 = V _{IL} or /WE = V _{IL} or /OE = V _{IH}	-1.0		+1.0	-1.0		+1.0	-1.0		+1.0	μA
Operating supply current	I _{CCA1}	/CE1 = V _{IL} , CE2 = V _{IH} , Minimum cycle time, I _{I/O} = 0 mA	V _{CC} ≤ 2.7 V	-	40	-	-	40	-	-	40	mA
			V _{CC} ≤ 2.2 V	-	-	-	-	-	-	-	35	
			V _{CC} ≤ 2.2 V	-	-	-	-	-	-	-	38	
	I _{CCA2}	/CE1 = V _{IL} , CE2 = V _{IH} , I _{I/O} = 0 mA	V _{CC} ≤ 2.7 V	-	10	-	-	10	-	-	10	
			V _{CC} ≤ 2.7 V	-	-	-	-	8	-	-	8	
			V _{CC} ≤ 2.2 V	-	-	-	-	-	-	-	6	
	I _{CCA3}	/CE1 ≤ 0.2 V, CE2 ≥ V _{CC} - 0.2 V, Cycle = 1 MHz, I _{I/O} = 0 mA, V _{IL} ≤ 0.2 V, V _{IH} ≥ V _{CC} - 0.2 V	V _{CC} ≤ 2.7 V	-	8	-	-	8	-	-	8	
			V _{CC} ≤ 2.7 V	-	-	-	-	6	-	-	6	
			V _{CC} ≤ 2.2 V	-	-	-	-	-	-	-	6	
Standby supply current	I _{SB}	/CE1 = V _{IH} or CE2 = V _{IL} or /LB = /UB = V _{IH} , /CE1, CE2 = V _{IH} or V _{IL}	V _{CC} ≤ 2.7 V	-	0.6	-	-	0.6	-	-	0.6	mA
			V _{CC} ≤ 2.7 V	-	-	-	-	0.6	-	-	0.6	
			V _{CC} ≤ 2.2 V	-	-	-	-	-	-	-	0.6	
	I _{SB1}	/CE1 ≥ V _{CC} - 0.2 V, CE2 ≥ V _{CC} - 0.2 V	V _{CC} ≤ 2.7 V	0.5	7	0.5	7	0.5	7	0.5	7	μA
			V _{CC} ≤ 2.7 V	-	-	0.4	6	0.4	6			
			V _{CC} ≤ 2.2 V	-	-	-	-	0.3	5			
	I _{SB2}	CE2 ≤ 0.2 V	V _{CC} ≤ 2.7 V	0.5	7	0.5	7	0.5	7	0.5	7	
			V _{CC} ≤ 2.7 V	-	-	0.4	6	0.4	6			
			V _{CC} ≤ 2.2 V	-	-	-	-	0.3	5			
	I _{SB3}	/LB = /UB ≥ V _{CC} - 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V _{CC} - 0.2 V	V _{CC} ≤ 2.7 V	0.5	7	0.5	7	0.5	7	0.5	7	
			V _{CC} ≤ 2.7 V	-	-	0.4	6	0.4	6			
			V _{CC} ≤ 2.2 V	-	-	-	-	0.3	5			
High level output voltage	V _{OH}	I _{OH} = -0.5 mA	V _{CC} ≤ 2.7 V	2.4		2.4		2.4			V	
			V _{CC} ≤ 2.7 V	-		1.8		1.8				
			V _{CC} ≤ 2.2 V	-		-		1.5				
Low level output voltage	V _{OL}	I _{OL} = 1.0 mA			0.4		0.4			0.4	V	

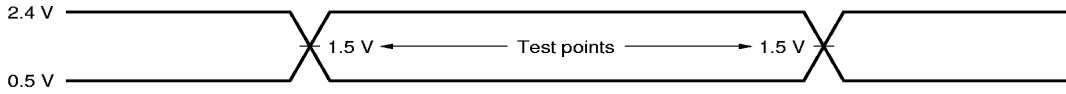
- Remarks**
1. V_{IN} : Input voltage
 2. These DC characteristics are in common regardless of package types and access time.

AC Characteristics (Recommended Operating Conditions Unless Otherwise Noted)

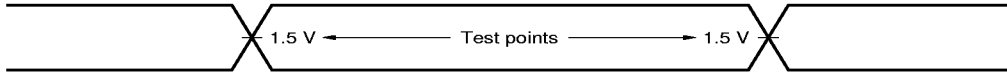
AC Test Conditions

[μPD444012L-B70X, μPD444012L-B85X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

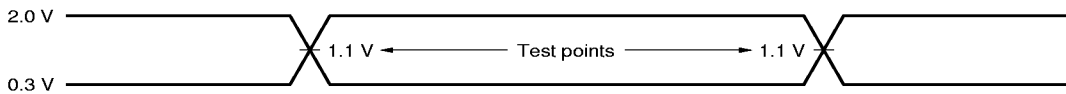


Output Load

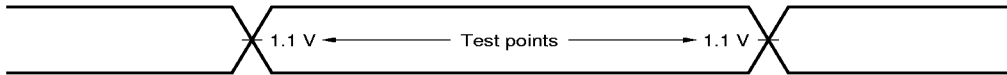
1TTL + 50 pF

[μPD444012L-C10X, μPD444012L-C12X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform

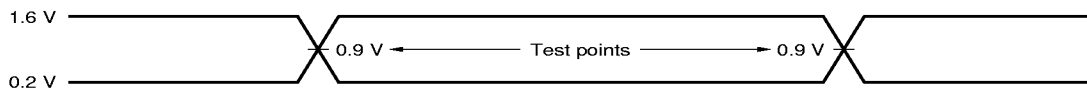


Output Load

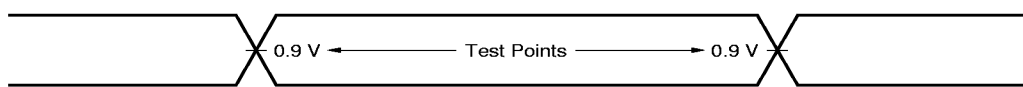
1TTL + 30 pF

★ [μPD444012L-D15X, μPD444012L-D20X]

Input Waveform (Rise and Fall Time ≤ 5 ns)



Output Waveform



Output Load

1TTL + 30 pF

★ Read Cycle

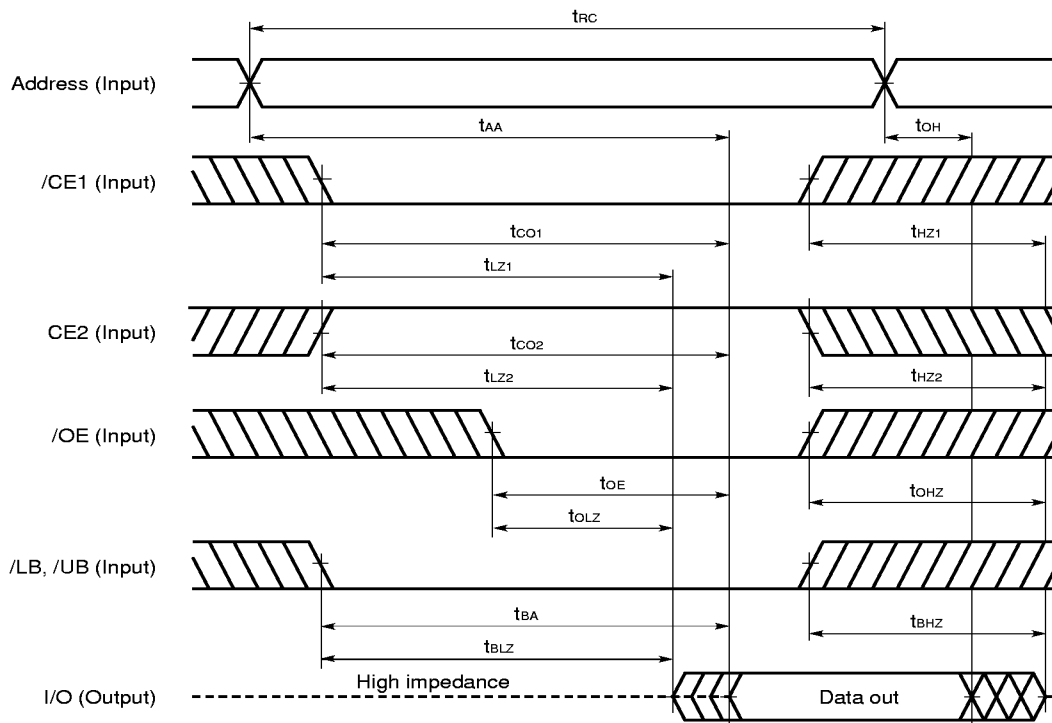
Parameter	Symbol	V _{CC} ≥ 2.7 V				V _{CC} ≥ 2.2 V				V _{CC} ≥ 1.8 V				Unit	Condition
		μPD444012L -B70X		μPD444012L -B85X		μPD444012L -C10X		μPD444012L -C12X		μPD444012L -D15X		μPD444012L -D20X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Read cycle time	t _{RC}	70		85		100		120		150		200		ns	
Address access time	t _{AA}		70		85		100		120		150		200	ns	Note 1
/CE1 access time	t _{CO1}		70		85		100		120		150		200	ns	
CE2 access time	t _{CO2}		70		85		100		120		150		200	ns	
/OE to output valid	t _{OE}		35		40		50		60		70		100	ns	
/LB, /UB to output valid	t _{BA}		70		85		100		120		150		200	ns	
Output hold from address change	t _{OH}	10		10		10		10		10		10		ns	
/CE1 to output in low impedance	t _{LZ1}	10		10		10		10		10		10		ns	Note 2
CE2 to output in low impedance	t _{LZ2}	10		10		10		10		10		10		ns	
/OE to output in low impedance	t _{OLZ}	5		5		5		5		5		5		ns	
/LB, /UB to output in low impedance	t _{BLZ}	10		10		10		10		10		10		ns	
/CE1 to output in high impedance	t _{HZ1}		25		30		35		40		50		70	ns	
CE2 to output in high impedance	t _{HZ2}		25		30		35		40		50		70	ns	
/OE to output in high impedance	t _{OHZ}		25		30		35		40		50		70	ns	
/LB, /UB to output in high impedance	t _{BHZ}		25		30		35		40		50		70	ns	

Notes 1. The output load is 1TTL + 50 pF (μPD444012L-BxxX) or 1TTL + 30 pF (μPD444012L-CxxX, -DxxX).

2. The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

Read Cycle Timing Chart



Remark In read cycle, /WE should be fixed to high level.

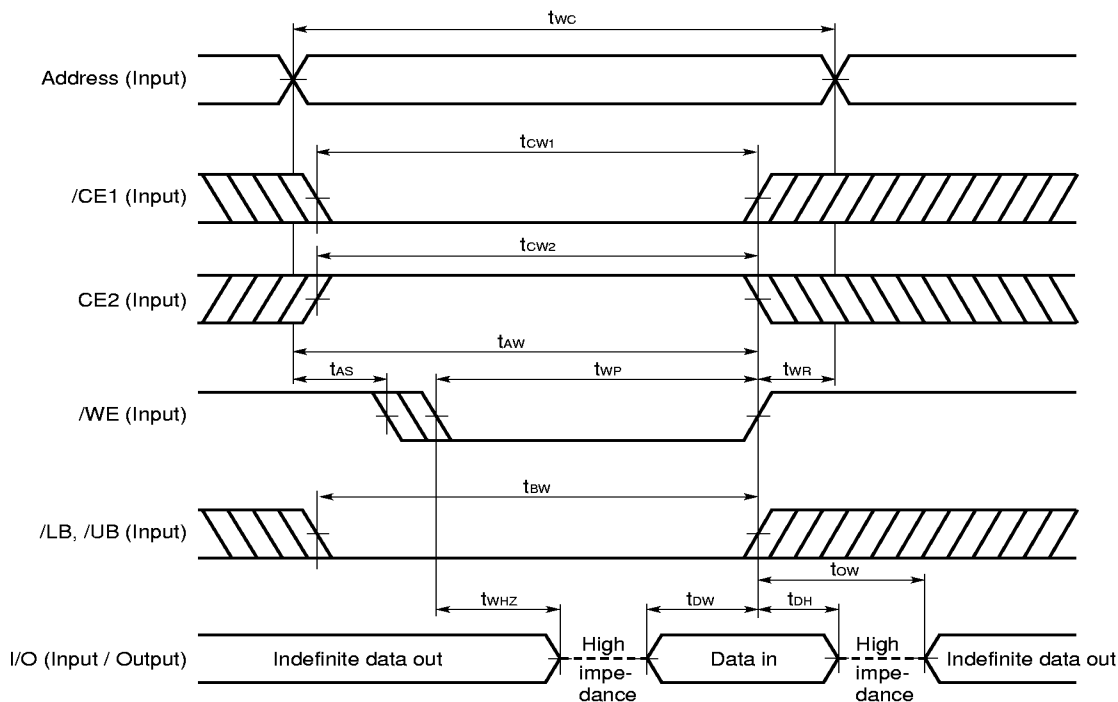
★ Write Cycle

Parameter	Symbol	V _{CC} ≥ 2.7 V				V _{CC} ≥ 2.2 V				V _{CC} ≥ 1.8 V				Unit	Condition
		μPD444012L -B70X		μPD444012L -B85X		μPD444012L -C10X		μPD444012L -C12X		μPD444012L -D15X		μPD444012L -D20X			
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
Write cycle time	t _{wc}	70		85		100		120		150		200		ns	
/CE1 to end of write	t _{cw1}	55		70		80		100		120		160		ns	
CE2 to end of write	t _{cw2}	55		70		80		100		120		160		ns	
/LB, /UB to end of write	t _{bw}	55		70		80		100		120		160		ns	
Address valid to end of write	t _{aw}	55		70		80		100		120		160		ns	
Address setup time	t _{as}	0		0		0		0		0		0		ns	
Write pulse width	t _{wP}	50		55		60		85		100		140		ns	
Write recovery time	t _{wR}	0		0		0		0		0		0		ns	
Data valid to end of write	t _{dW}	30		35		40		60		80		100		ns	
Data hold time	t _{dH}	0		0		0		0		0		0		ns	
/WE to output in high impedance	t _{wHZ}		25		30		35		40		50		70	ns	Note
Output active from end of write	t _{ow}	5		5		5		5		5		5		ns	

Note The output load is 1TTL + 5 pF.

Remark These AC characteristics are in common regardless of package types.

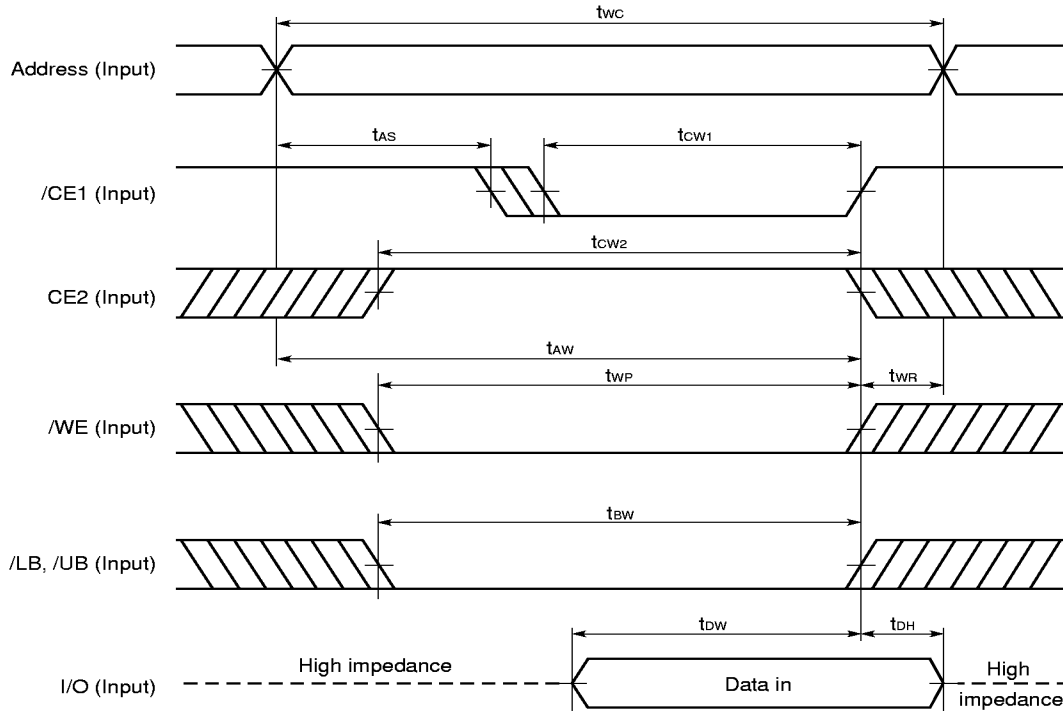
Write Cycle Timing Chart 1 (/WE Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

- Remarks**
1. Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.
 2. If /CE1 changes to low level at the same time or after the change of /WE to low level, or if CE2 changes to high level at the same time or after the change of /WE to low level, the I/O pins will remain high impedance state.
 3. When /WE is at low level, the I/O pins are always high impedance. When /WE is at high level, read operation is executed. Therefore /OE should be at high level to make the I/O pins high impedance.

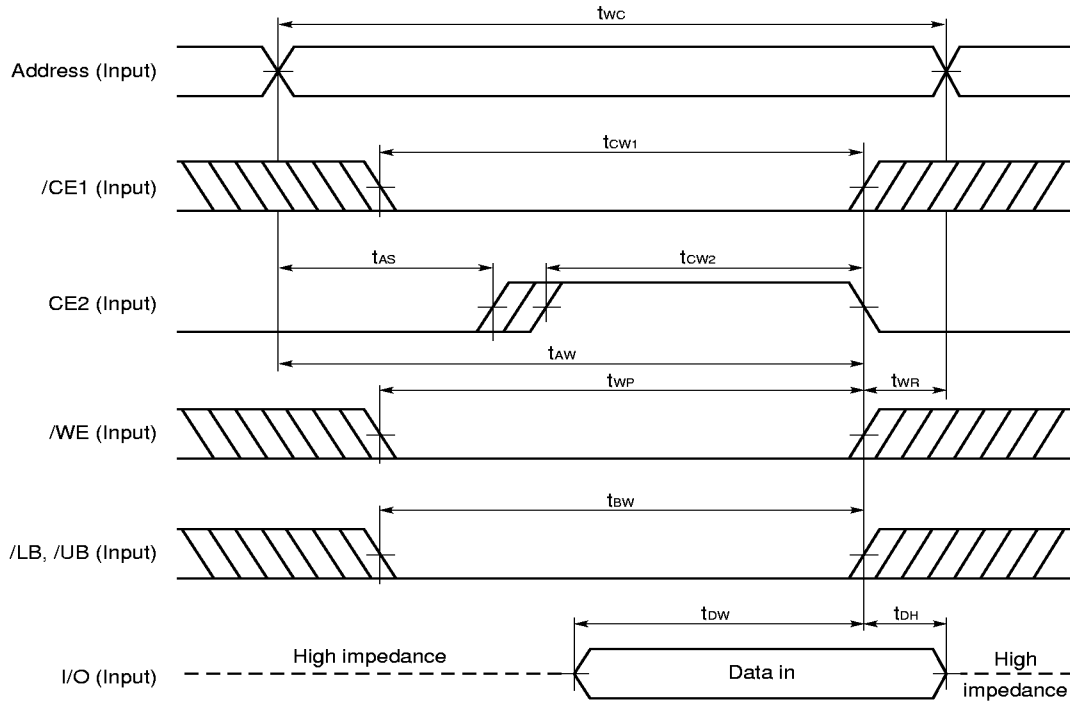
Write Cycle Timing Chart 2 (/CE1 Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

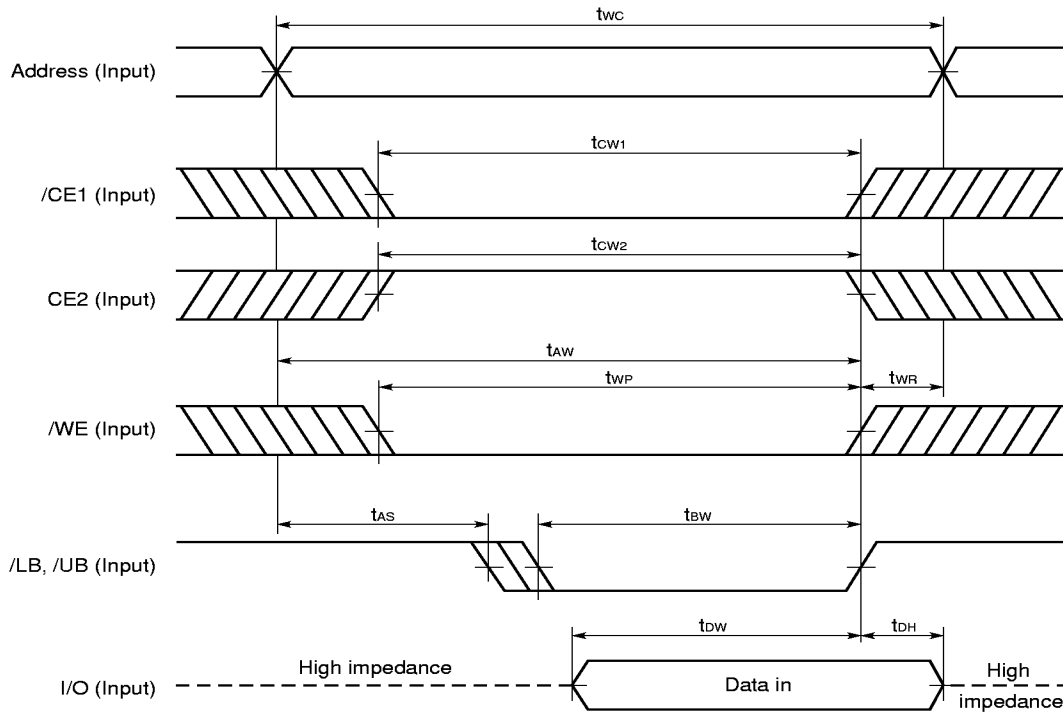
Write Cycle Timing Chart 3 (CE2 Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

Write Cycle Timing Chart 4 (/LB, /UB Controlled)



- Cautions**
1. During address transition, at least one of pins /CE1, CE2, /WE should be inactivated.
 2. When I/O pins are in the output state, do not apply to the I/O pins signals that are opposite in phase with output signals.

Remark Write operation is done during the overlap time of a low level /CE1, /WE, /LB and/or /UB, and a high level CE2.

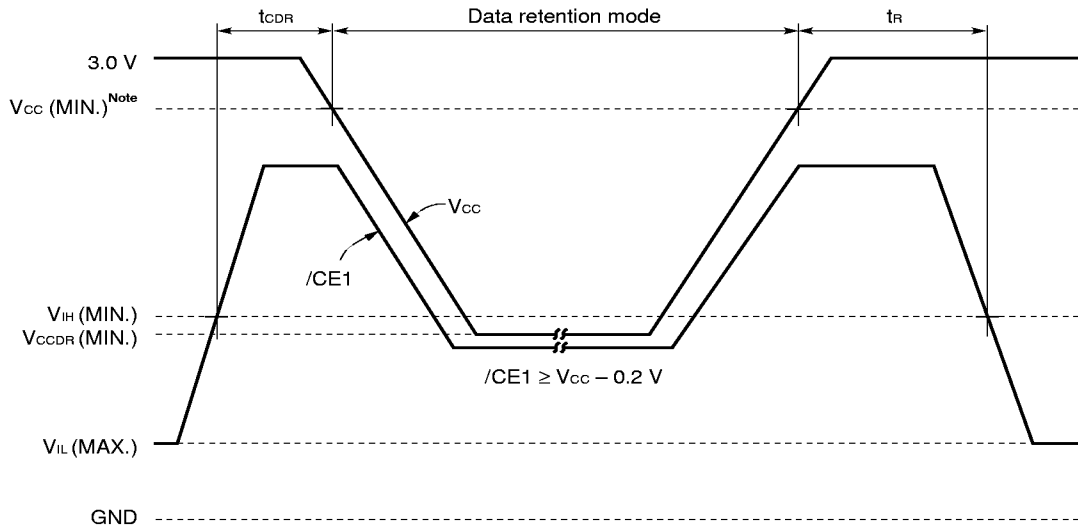
Low V_{CC} Data Retention Characteristics (T_A = -25 to +85 °C)

Parameter	Symbol	Test Condition	V _{CC} ≥ 2.7 V			V _{CC} ≥ 2.2 V			V _{CC} ≥ 1.8 V			Unit
			μPD444012L -BxxX			μPD444012L -CxxX			μPD444012L -DxxX			
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Data retention supply voltage	V _{CCDR1}	/CE1 ≥ V _{CC} - 0.2 V, CE2 ≥ V _{CC} - 0.2 V	2.0		3.6	1.5		3.6	1.5		3.6	V
	V _{CCDR2}	CE2 ≤ 0.2 V	2.0		3.6	1.5		3.6	1.5		3.6	
	V _{CCDR3}	/LB = /UB ≥ V _{CC} - 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V _{CC} - 0.2 V	2.0		3.6	1.5		3.6	1.5		3.6	
Data retention supply current	I _{CCDR1}	V _{CC} = 3.0 V, /CE1 ≥ V _{CC} - 0.2 V, CE2 ≥ V _{CC} - 0.2 V or CE2 ≤ 0.2 V		0.5	7		0.5	7		0.5	7	μA
	I _{CCDR2}	V _{CC} = 3.0 V, CE2 ≤ 0.2 V		0.5	7		0.5	7		0.5	7	
	I _{CCDR3}	V _{CC} = 3.0 V, /LB = /UB ≥ V _{CC} - 0.2 V, /CE1 ≤ 0.2 V, CE2 ≥ V _{CC} - 0.2 V		0.5	7		0.5	7		0.5	7	
Chip deselection to data retention mode	t _{CDR}		0			0			0			ns
Operation recovery time	t _R		t _{RC} ^{Note}			t _{RC} ^{Note}			t _{RC} ^{Note}			ns

Note t_{RC} : Read cycle time

Data Retention Timing Chart

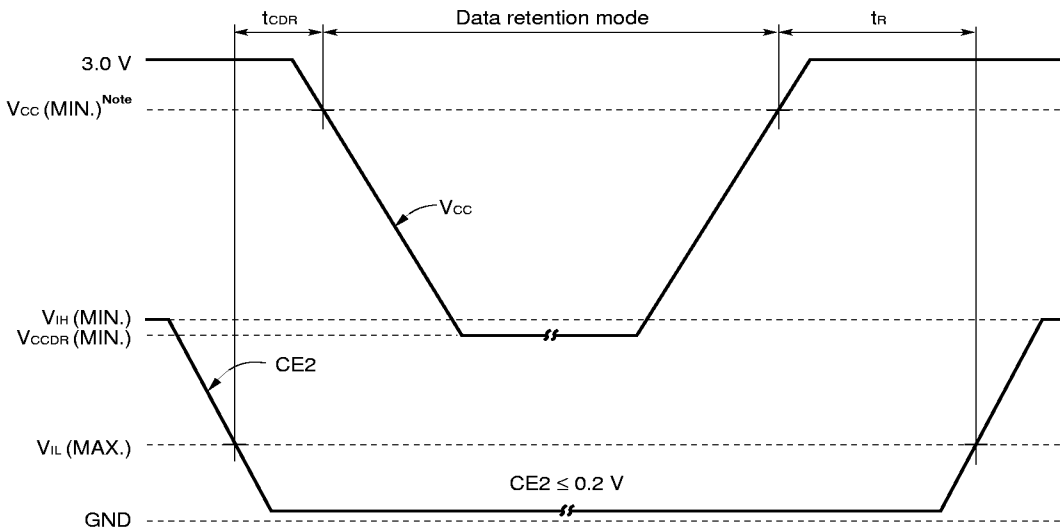
(1) /CE1 Controlled



Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling $/CE1$, the input level of CE2 must be $\geq V_{CC} - 0.2 \text{ V}$ or $\leq 0.2 \text{ V}$. The other pins (Address, I/O, $/WE$, $/OE$, $/LB$, $/UB$) can be in high impedance state.

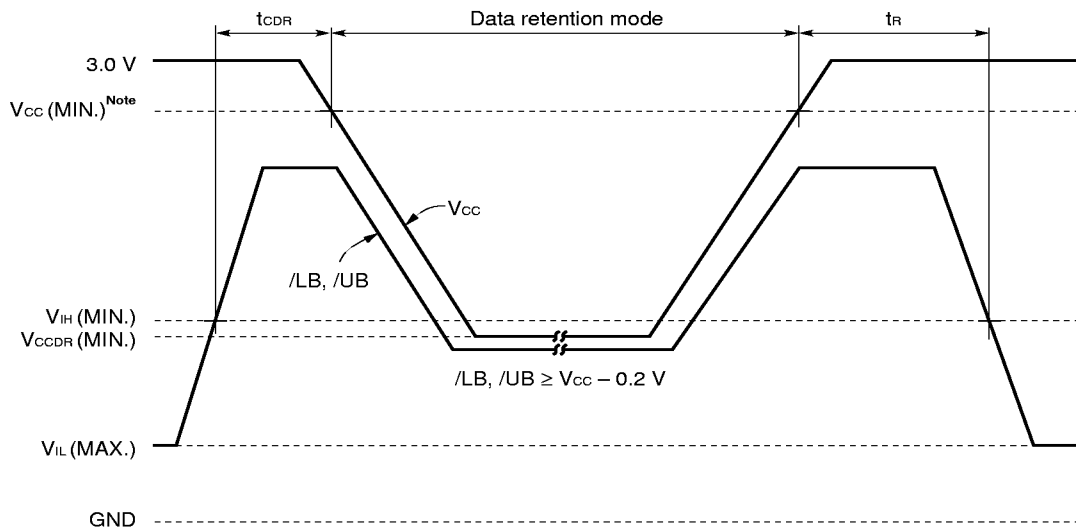
(2) CE2 Controlled



Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark The other pins ($/CE1$, Address, I/O, $/WE$, $/OE$, $/LB$, $/UB$) can be in high impedance state.

(3) /LB, /UB Controlled

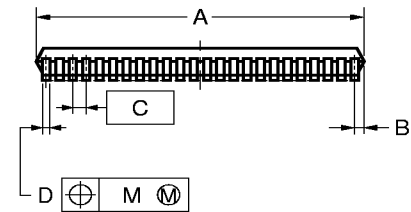
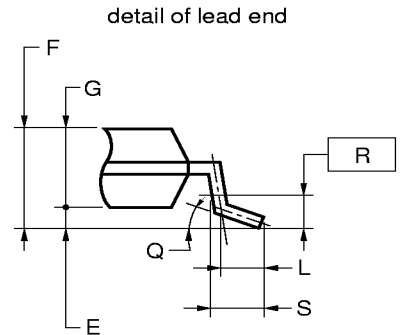
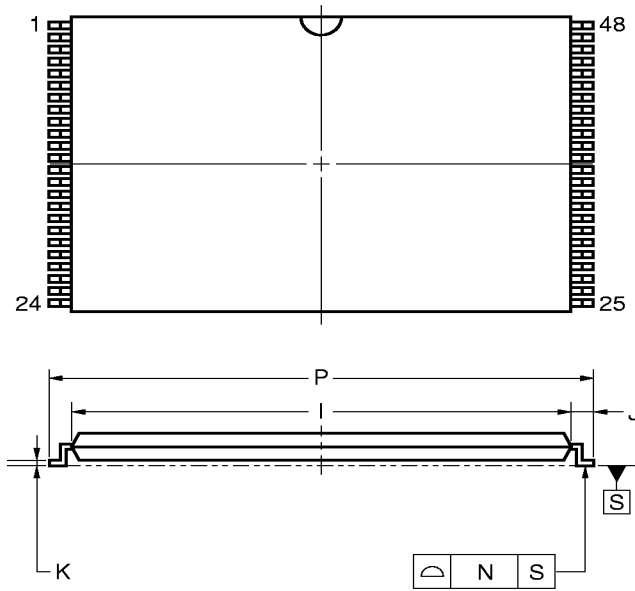


Note B version : 2.7 V, C version : 2.2 V, D version : 1.8 V

Remark On the data retention mode by controlling /LB and /UB, the input level of /CE1 and CE2 must be $\geq V_{CC} - 0.2\text{ V}$ or $\leq 0.2\text{ V}$. The other pins (Address, I/O, /WE, /OE) can be in high impedance state.

Package Drawings

48 PIN PLASTIC TSOP (I) (12×18)



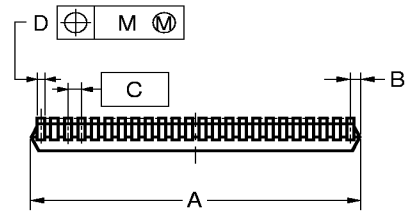
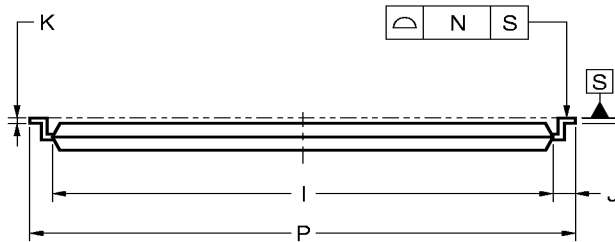
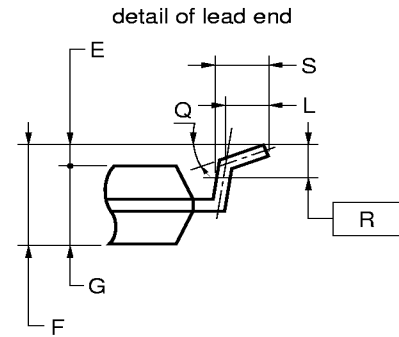
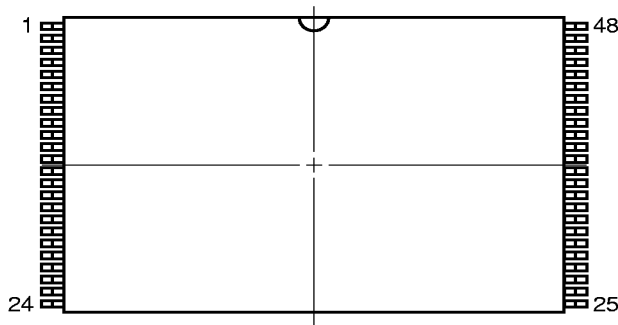
NOTES

1. Controlling dimension — Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

ITEM	MILLIMETERS	INCHES
A	12.0±0.1	0.472 ^{+0.005} _{-0.004}
B	0.45 MAX.	0.018 MAX.
C	0.5 (T.P.)	0.020 (T.P.)
D	0.22±0.05	0.009 ^{+0.002} _{-0.003}
E	0.1±0.05	0.004±0.002
F	1.2 MAX.	0.048 MAX.
G	1.0±0.05	0.039 ^{+0.003} _{-0.002}
I	16.4±0.1	0.646 ^{+0.004} _{-0.005}
J	0.8±0.2	0.031 ^{+0.009} _{-0.008}
K	0.145±0.05	0.006 ^{+0.002} _{-0.003}
L	0.5	0.020
M	0.10	0.004
N	0.10	0.004
P	18.0±0.2	0.709 ^{+0.008} _{-0.009}
Q	3° ^{+5°} _{-3°}	3° ^{+5°} _{-3°}
R	0.25	0.010
S	0.60±0.15	0.024 ^{+0.006} _{-0.007}

S48GY-50-MJH1

48 PIN PLASTIC TSOP (I) (12×18)



NOTES

1. Controlling dimension — Millimeter.
2. Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.
3. "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX. <0.489 inch MAX.>)

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N	0.10	0.004
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Q	3°+5° -3°	3°+5° -3°
R	0.25	0.010
S	0.60±0.15	0.024 ^{+0.006} _{-0.007}

S48GY-50-MKH1