



# STP8NM50 STP8NM50FP

N-CHANNEL 500V - 0.7Ω - 8A TO-220/TO-220FP  
MDmesh™ Power MOSFET

TYPE	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STP8NM50	500V	< 0.8Ω	8 A
STP8NM50FP	500V	< 0.8Ω	8 A

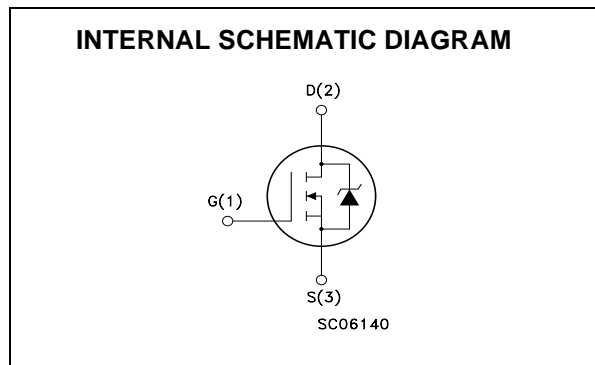
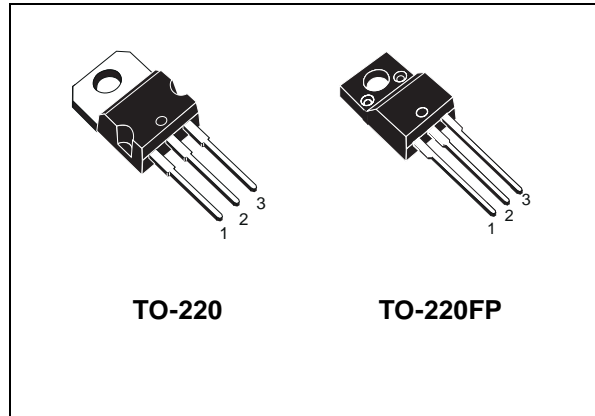
- TYPICAL R<sub>DS(on)</sub> = 0.7Ω
- HIGH dv/dt AND AVALANCHE CAPABILITIES
- 100% AVALANCHE TESTED
- LOW INPUT CAPACITANCE AND GATE CHARGE
- LOW GATE INPUT RESISTANCE

## DESCRIPTION

The MDmesh™ is a new revolutionary MOSFET technology that associates the Multiple Drain process with the Company's PowerMESH™ horizontal layout. The resulting product has an outstanding low on-resistance, impressively high dv/dt and excellent avalanche characteristics. The adoption of the Company's proprietary strip technique yields overall dynamic performance that is significantly better than that of similar competition's products.

## APPLICATIONS

The MDmesh™ family is very suitable for increasing power density of high voltage converters allowing system miniaturization and higher efficiencies.



## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value		Unit
		STP8NM50	STP8NM50FP	
V <sub>DS</sub>	Drain-source Voltage (V <sub>GS</sub> = 0)	500		V
V <sub>DGR</sub>	Drain-gate Voltage (R <sub>GS</sub> = 20 kΩ)	500		V
V <sub>GS</sub>	Gate- source Voltage	±30		V
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 25°C	5	5 (*)	A
I <sub>D</sub>	Drain Current (continuous) at T <sub>C</sub> = 100°C	3.1	3.1 (*)	A
I <sub>DM</sub> (•)	Drain Current (pulsed)	20	20 (*)	A
P <sub>TOT</sub>	Total Dissipation at T <sub>C</sub> = 25°C	120	30	W
	Derating Factor	0.4		W/°C
dv/dt	Peak Diode Recovery voltage slope	15		V/ns
V <sub>ISO</sub>	Insulation Withstand Voltage (DC)	--	2500	V
T <sub>stg</sub>	Storage Temperature	-65 to 150		°C
T <sub>j</sub>	Max. Operating Junction Temperature			

(•)Pulse width limited by safe operating area  
August 2002

(\*)Limited only by maximum temperature allowed

## STP8NM50/STP8NM50FP

### THERMAL DATA

			TO-220 / I <sup>2</sup> PAK	TO-220FP	
Rthj-case	Thermal Resistance Junction-case	Max	1.04	4.21	°C/W
Rthj-amb	Thermal Resistance Junction-ambient	Max	62.5		°C/W
T <sub>l</sub>	Maximum Lead Temperature For Soldering Purpose		300		°C

### AVALANCHE CHARACTERISTICS

Symbol	Parameter	Max Value	Unit
I <sub>AR</sub>	Avalanche Current, Repetitive or Not-Repetitive (pulse width limited by T <sub>j</sub> max)	2.5	A
E <sub>AS</sub>	Single Pulse Avalanche Energy (starting T <sub>j</sub> = 25 °C, I <sub>D</sub> = I <sub>AR</sub> , V <sub>DD</sub> = 50 V)	200	mJ

### ELECTRICAL CHARACTERISTICS (T<sub>CASE</sub> = 25 °C UNLESS OTHERWISE SPECIFIED)

OFF

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0	500			V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = Max Rating V <sub>DS</sub> = Max Rating, T <sub>C</sub> = 125 °C			1 10	μA μA
I <sub>GSS</sub>	Gate-body Leakage Current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±30V			±100	nA

ON (1)

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V <sub>GS(th)</sub>	Gate Threshold Voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	3	4	5	V
R <sub>DS(on)</sub>	Static Drain-source On Resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 2.5A		0.7	0.8	Ω

DYNAMIC

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> (1)	Forward Transconductance	V <sub>DS</sub> > I <sub>D(on)</sub> × R <sub>DS(on)max</sub> , I <sub>D</sub> = 2.5A		2.4		S
C <sub>iSS</sub>	Input Capacitance	V <sub>DS</sub> = 25V, f = 1 MHz, V <sub>GS</sub> = 0		415		pF
C <sub>oSS</sub>	Output Capacitance			88		pF
C <sub>rSS</sub>	Reverse Transfer Capacitance			12		pF
C <sub>oSS eq.</sub> (2)	Equivalent Output Capacitance	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 0V to 400V		50		pF
R <sub>G</sub>	Gate Input Resistance	f=1 MHz Gate DC Bias = 0 Test Signal Level = 20mV Open Drain		3		Ω

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5 %.

2. C<sub>oSS eq.</sub> is defined as a constant equivalent capacitance giving the same charging time as C<sub>oSS</sub> when V<sub>DS</sub> increases from 0 to 80% V<sub>DSS</sub>.

**ELECTRICAL CHARACTERISTICS (CONTINUED)**  
SWITCHING ON

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on Delay Time	$V_{DD} = 250V, I_D = 2.5A$		16		ns
$t_r$	Rise Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 3)		8		ns
$Q_g$	Total Gate Charge	$V_{DD} = 400V, I_D = 5A,$		13		nC
$Q_{gs}$	Gate-Source Charge	$V_{GS} = 10V$		4		nC
$Q_{gd}$	Gate-Drain Charge			6		nC

SWITCHING OFF

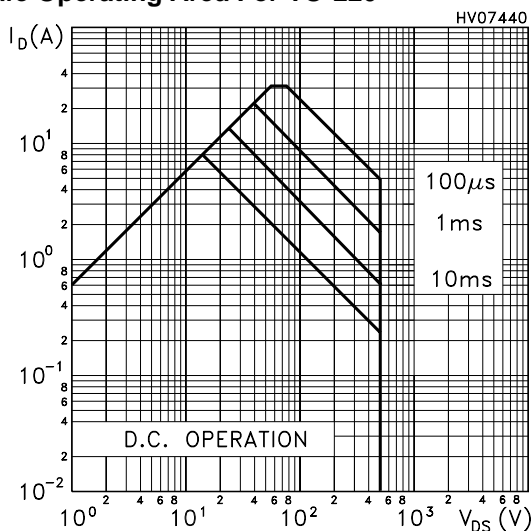
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$t_{r(Voff)}$	Off-voltage Rise Time	$V_{DD} = 400V, I_D = 5A,$		14		ns
$t_f$	Fall Time	$R_G = 4.7\Omega, V_{GS} = 10V$ (see test circuit, Figure 5)		6		ns
$t_c$	Cross-over Time			13		ns

SOURCE DRAIN DIODE

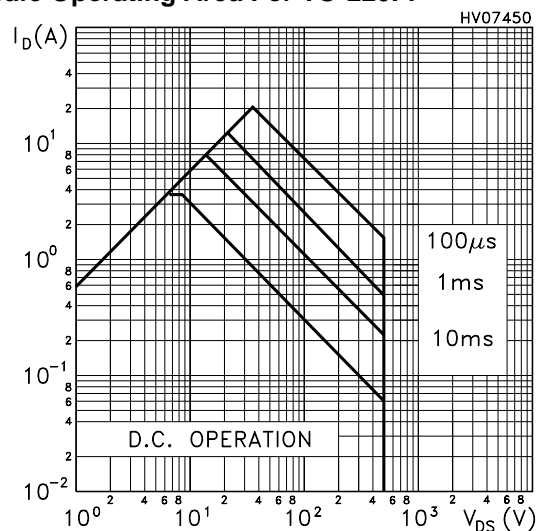
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain Current				5	A
$I_{SDM(2)}$	Source-drain Current (pulsed)				20	A
$V_{SD(1)}$	Forward On Voltage	$I_{SD} = 5A, V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 5A, di/dt = 100A/\mu s,$		185		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 100V, T_j = 25^\circ C$		1.1		$\mu C$
$I_{RRM}$	Reverse Recovery Charge	(see test circuit, Figure 5)		11.5		A
$t_{rr}$	Reverse Recovery Time	$I_{SD} = 5A, di/dt = 100A/\mu s,$		270		ns
$Q_{rr}$	Reverse Recovery Charge	$V_{DD} = 100V, T_j = 150^\circ C$		1.6		$\mu C$
$I_{RRM}$	Reverse Recovery Charge	(see test circuit, Figure 5)		12		A

Note: 1. Pulsed: Pulse duration = 300  $\mu s$ , duty cycle 1.5 %.  
2. Pulse width limited by safe operating area.  
3. Pulse width limited by safe operating area.

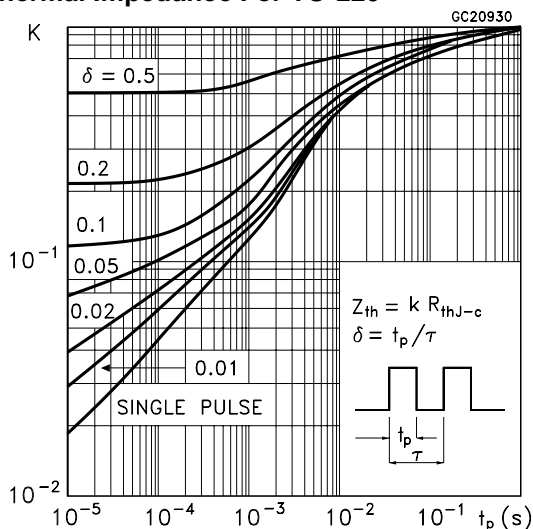
Safe Operating Area For TO-220



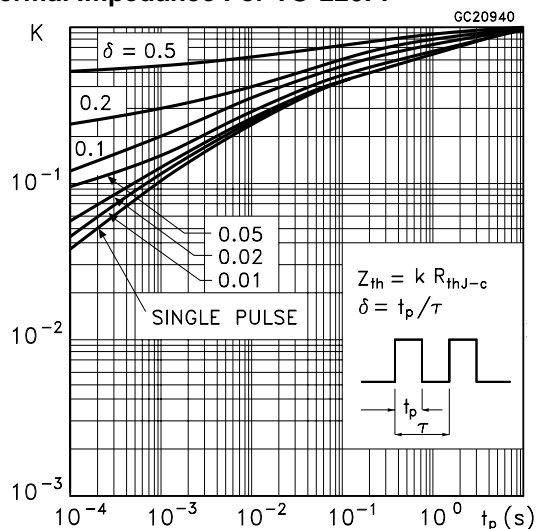
Safe Operating Area For TO-220FP



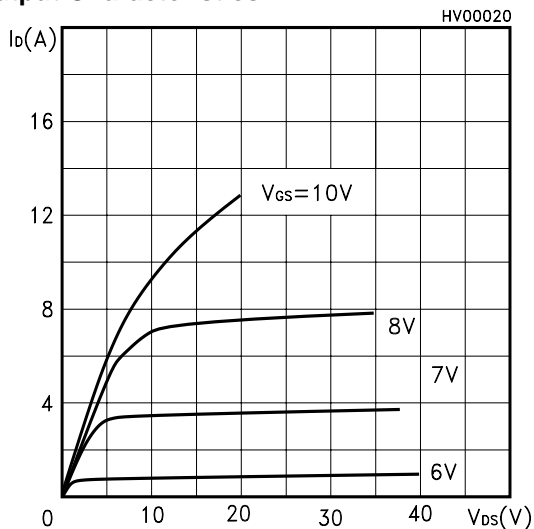
Thermal Impedance For TO-220



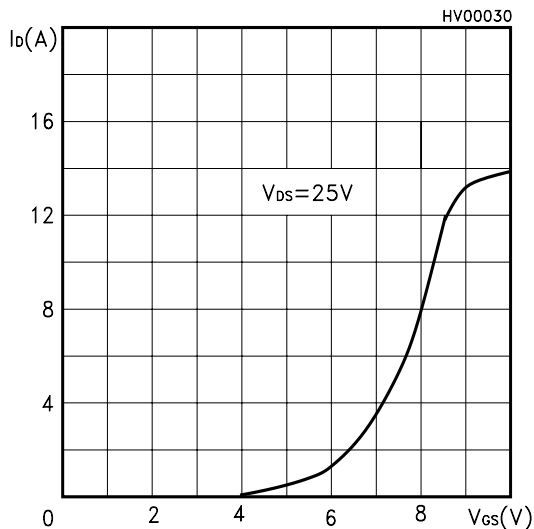
Thermal Impedance For TO-220FP



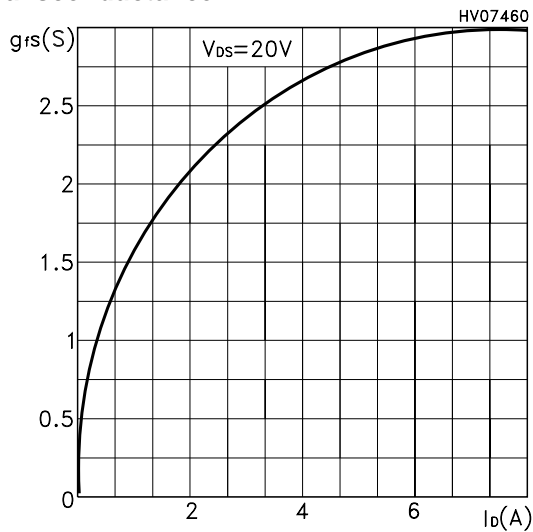
Output Characteristics



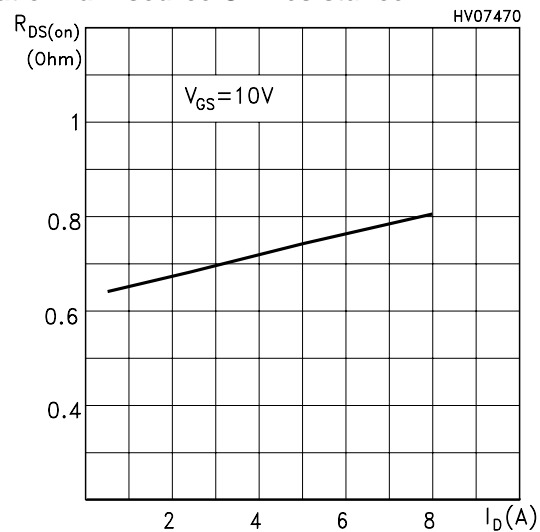
Transfer Characteristics



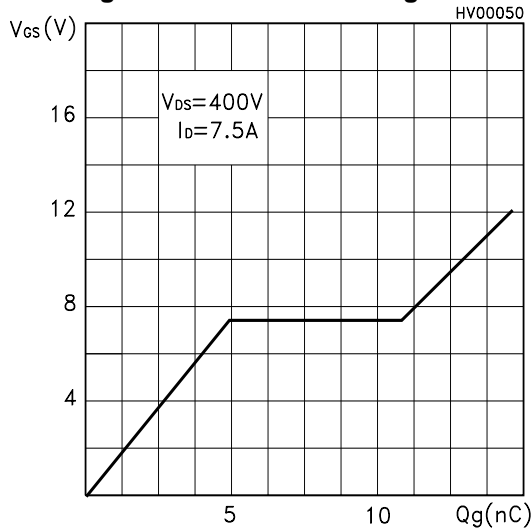
Transconductance



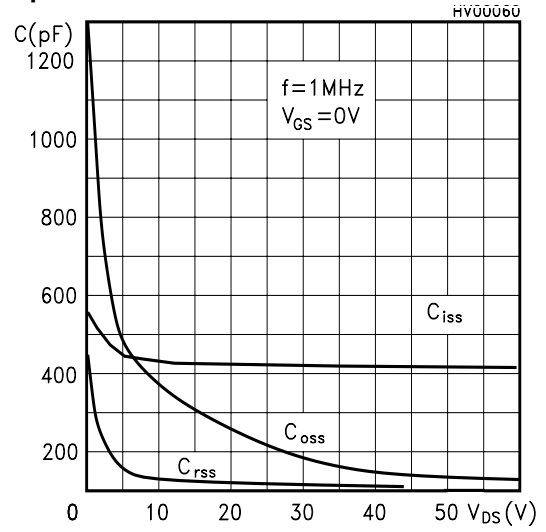
Static Drain-source On Resistance



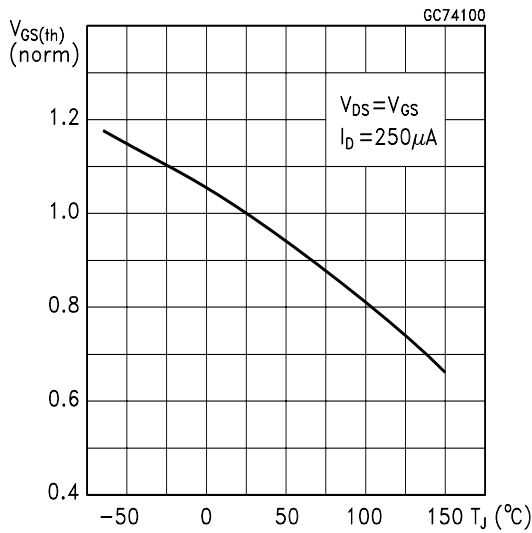
Gate Charge vs Gate-source Voltage



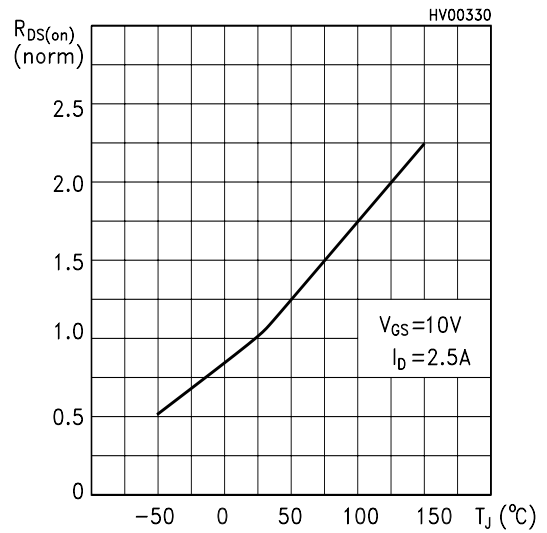
Capacitance Variations



Normalized Gate Threshold Voltage vs Temp.



Normalized On Resistance vs Temperature



Source-drain Diode Forward Characteristics

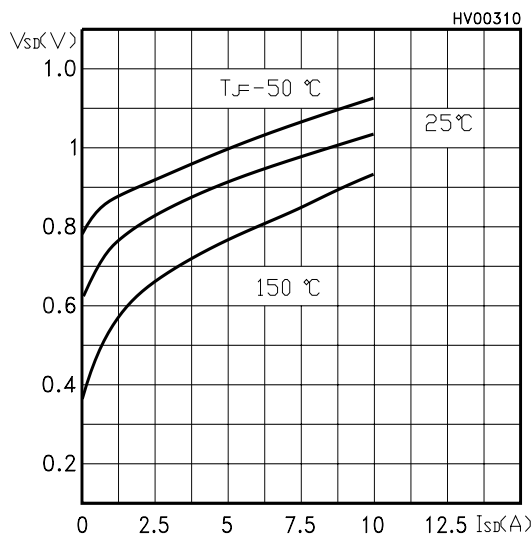


Fig. 1: Unclamped Inductive Load Test Circuit

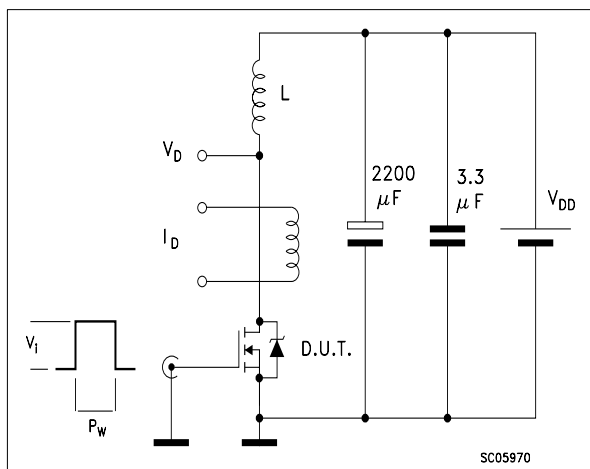


Fig. 2: Unclamped Inductive Waveform



Fig. 3: Switching Times Test Circuit For Resistive Load

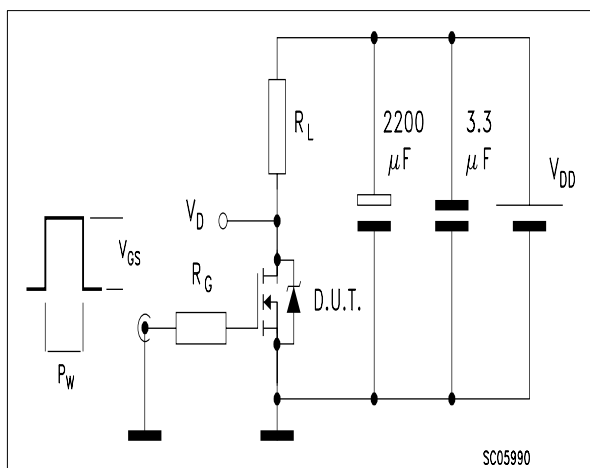
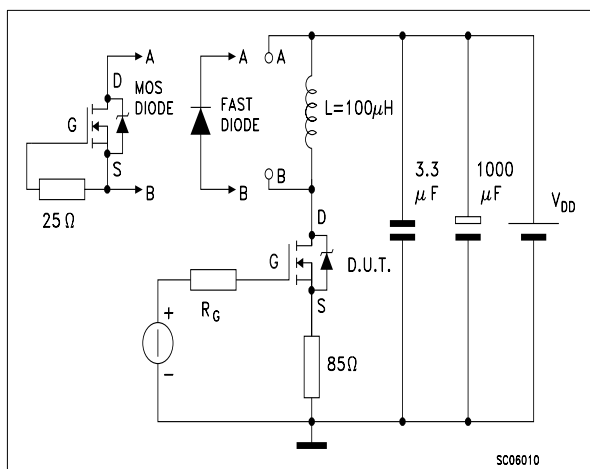


Fig. 4: Gate Charge test Circuit

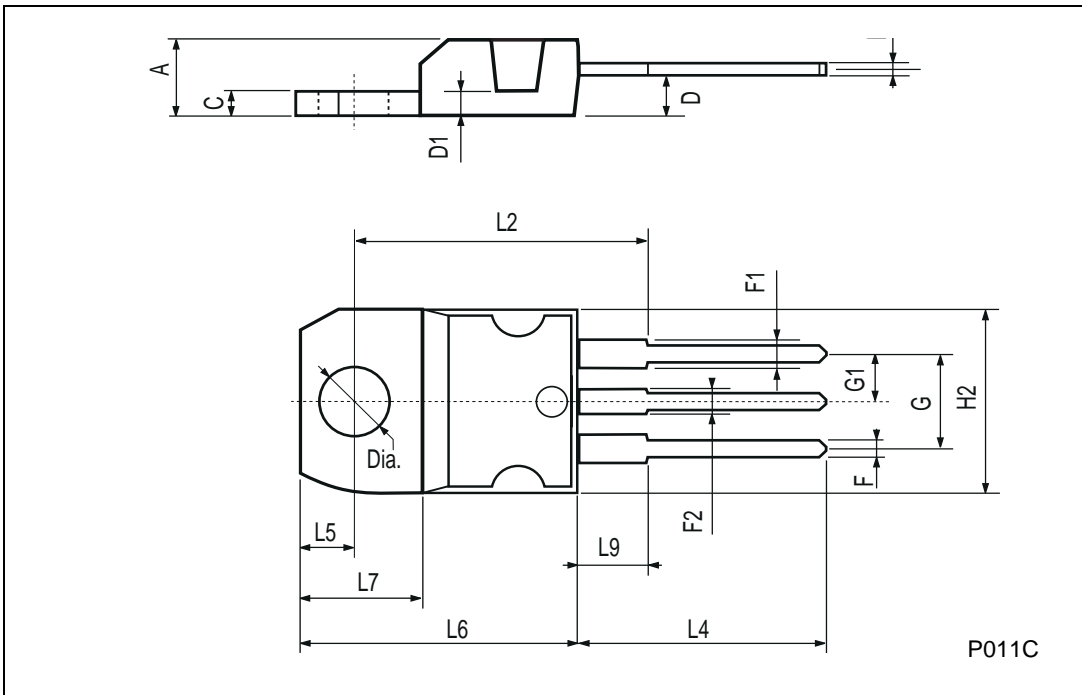


Fig. 5: Test Circuit For Inductive Load Switching And Diode Recovery Times



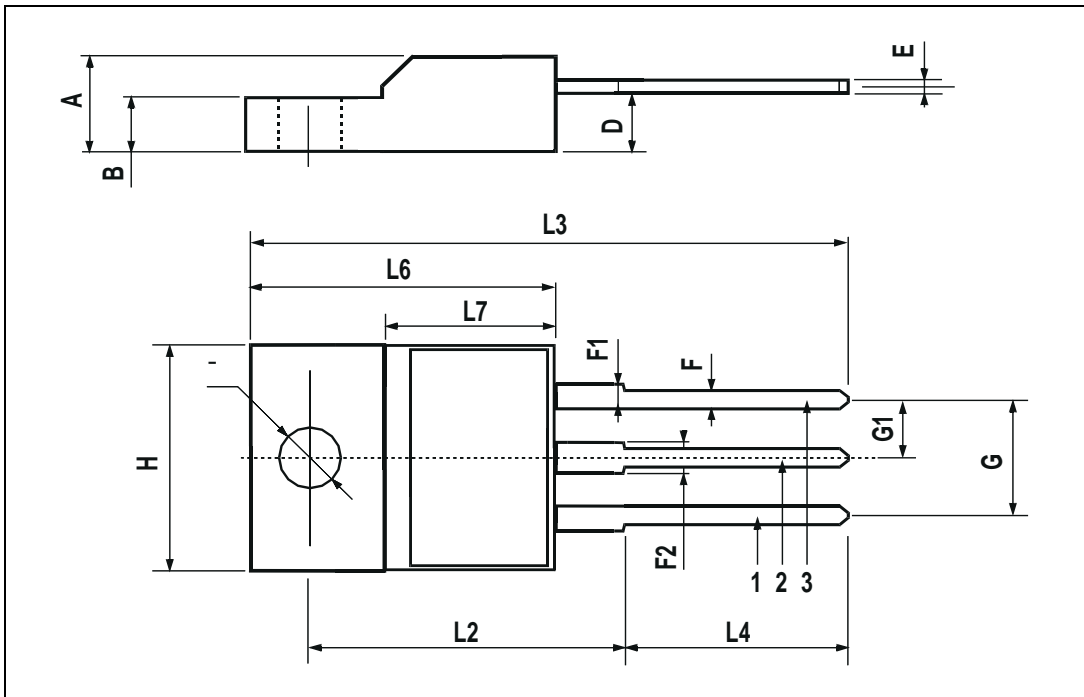
**TO-220 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.40		4.60	0.173		0.181
C	1.23		1.32	0.048		0.051
D	2.40		2.72	0.094		0.107
D1		1.27			0.050	
E	0.49		0.70	0.019		0.027
F	0.61		0.88	0.024		0.034
F1	1.14		1.70	0.044		0.067
F2	1.14		1.70	0.044		0.067
G	4.95		5.15	0.194		0.203
G1	2.4		2.7	0.094		0.106
H2	10.0		10.40	0.393		0.409
L2		16.4			0.645	
L4	13.0		14.0	0.511		0.551
L5	2.65		2.95	0.104		0.116
L6	15.25		15.75	0.600		0.620
L7	6.2		6.6	0.244		0.260
L9	3.5		3.93	0.137		0.154
DIA.	3.75		3.85	0.147		0.151



**TO-220FP MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	4.4		4.6	0.173		0.181
B	2.5		2.7	0.098		0.106
D	2.5		2.75	0.098		0.108
E	0.45		0.7	0.017		0.027
F	0.75		1	0.030		0.039
F1	1.15		1.7	0.045		0.067
F2	1.15		1.7	0.045		0.067
G	4.95		5.2	0.195		0.204
G1	2.4		2.7	0.094		0.106
H	10		10.4	0.393		0.409
L2		16			0.630	
L3	28.6		30.6	1.126		1.204
L4	9.8		10.6	0.385		0.417
L6	15.9		16.4	0.626		0.645
L7	9		9.3	0.354		0.366
∅	3		3.2	0.118		0.126





Information furnished is believed to be accurate and reliable. However, STMicroelectronics assumes no responsibility for the consequences of use of such information nor for any infringement of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of STMicroelectronics. Specifications mentioned in this publication are subject to change without notice. This publication supersedes and replaces all information previously supplied. STMicroelectronics products are not authorized for use as critical components in life support devices or systems without express written approval of STMicroelectronics.

© The ST logo is a registered trademark of STMicroelectronics

© 2002 STMicroelectronics - Printed in Italy - All Rights Reserved  
STMicroelectronics GROUP OF COMPANIES

Australia - Brazil - Canada - China - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco  
Singapore - Spain - Sweden - Switzerland - United Kingdom - United States.

© <http://www.st.com>