Features

512Kx8 bit CMOS Static

Random Access Memory

- Access Times: 17*, 20 and 25ns
- Data Retention Function (LPA version)
- Extended Temperature Testing
- Data Retention Functionality Testing

36 lead, JEDEC Approved Revolutionary Pinout

- Plastic SOJ No. 319

Single +5V (±10%) Supply Operation

*Industrial Temperature Only

512Kx8 Static RAM
CMOS, Monolithic

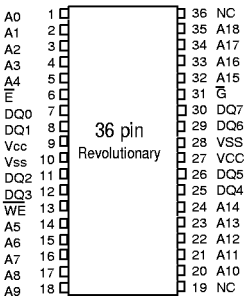
EDI's ruggedized plastic 512Kx8 SRAM allows the user to capitalize on the cost advantage of using a plastic component while not sacrificing all of the reliability available in a full military device.

Extended temperature testing is performed with the test patterns developed for use on EDI's fully compliant 512Kx8 SRAMs. EDI fully characterizes devices to determine the proper test patterns for testing at temperature extremes. This is critical because the operating characteristics of device change when it is operated beyond the commercial temperature range. Using commercial test methods will not guarantee a device that operates reliably in the field at temperature extremes. Users of EDI's ruggedized plastic benefit from EDI's extensive experience in characterizing SRAMs for use in military systems.

EDI ensures Low Power devices will retain data in Data Retention mode by characterizing the devices to determine the appropriate test conditions. This is crucial for systems operating at -40°C or below and using dense memories such as 512K x 8s.

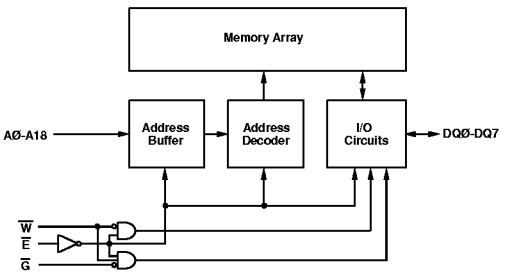
EDI's ruggedized plastic SOJ is footprint compatible with EDI's full military ceramic 36 pin SOJ.

Pin Configurations and Block Diagram



Pin Names

AØ-A18	Address Inputs
$\overline{E}$	Chip Enable
$\overline{W}$	Write Enable
$\overline{G}$	Output Enable
DQØ-DQ7	Common Data Input/Output
VCC	Power (+5V±10%)
VSS	Ground



Absolute Maximum Ratings*

Voltage on any pin relative to VSS	-0.5V to 7.0V
Operating Temperature TA (Ambient)	
Commercial	0°C to +70°C
Industrial	-40°C to +85°C
Military	-55°C to +125°C
Storage Temperature, Plastic	-65°C to +125°C
Power Dissipation	1.5 Watt
Output Current.	20 mA
Junction Temperature, TJ	175°C

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended DC Operating Conditions

Parameter	Sym	Min	Typ	Max	Units
Supply Voltage	VCC	4.5	5.0	5.5	V
Supply Voltage	VSS	0	0	0	V
Input High Voltage	VIH	2.2	--	6.0	V
Input Low Voltage	VIL	-0.3	--	0.8	V

AC Test Conditions

Input Pulse Levels	VSS to 3.0V
Input Rise and Fall Times	5ns
Input and Output Timing Levels	1.5V
Output Load	See Figure 1

(note: For TEHQZ,TGHQZ and TWLQZ see figure 2)

Figure 1

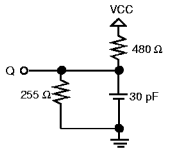
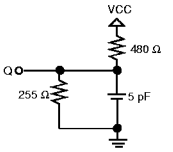


Figure 2



DC Electrical Characteristics

Parameter	Sym	Conditions		Min	Max	Units
Operating Power	ICC1	$\overline{W}$, $\overline{E}$ = VIL, II/O = 0mA,	17ns	--	250	mA
Supply Current		Min Cycle	20-25ns	--	225	mA
Standby (TTL) Power	ICC2	$\overline{E} \geq$ VIH, VIN $\leq$ VIL		--	60	mA
Supply Current		VIN $\geq$ VIH				
Full Standby Power	ICC3	$\overline{E} \geq$ VCC-0.2V	C	--	25	mA
Supply Current		VIN $\geq$ VCC-0.2V or VIN $\leq$ 0.2V	LP	--	10	mA
Input Leakage Current	ILI	VIN = 0V to VCC		-10	10	µA
Output Leakage Current	ILO	V I/O = 0V to VCC		-10	10	µA
Output High Voltage	VOH	IOH =-4mA		2.4	--	V
Output Low Voltage	VOL	IOL = 8mA		--	0.4	V

Truth Table

$\overline{G}$	$\overline{E}$	$\overline{W}$	Mode	Output	Power
X	H	X	Standby	High Z	ICC2, ICC3
H	L	H	Output Deselect	High Z	ICC1
L	L	H	Read	DOUT	ICC1
X	L	L	Write	DIN	ICC1

Capacitance

(f=1.0MHz, VIN=VCC or VSS)

Parameter	Sym	Max	Unit
Address Lines	CI	6	pF
Data Lines	CD/Q	8	pF

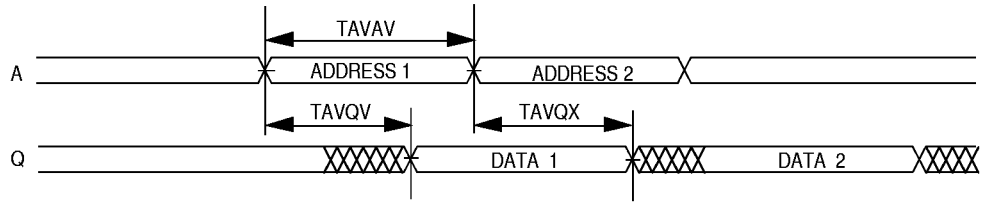
These parameters are sampled, not 100% tested.

AC Characteristics Read Cycle

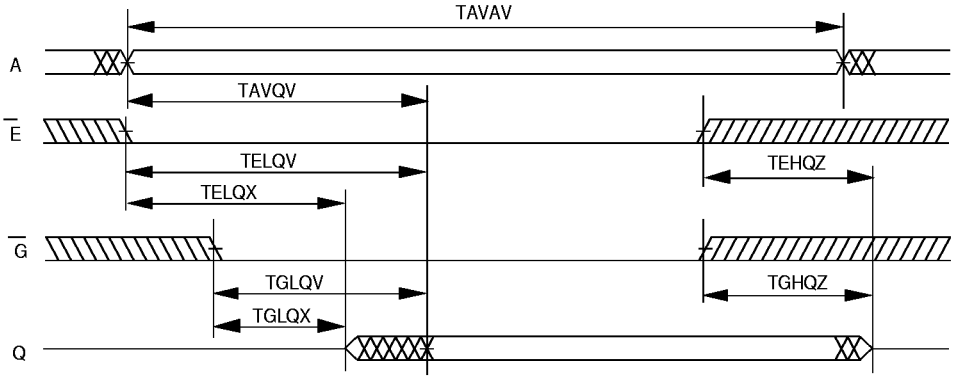
Parameter	Symbol JEDEC	Symbol Alt.	17ns* Min	17ns* Max	20ns Min	20ns Max	25ns Min	25ns Max	Units
Read Cycle Time	TAVAV	TRC	17		20		25		ns
Address Access Time	TAVQV	TAA		17		20		25	ns
Chip Enable Access Time	TELQV	TACS		17		20		25	ns
Chip Enable to Output in Low Z (1)	TELQX	TCLZ	3		3		3		ns
Chip Disable to Output in High Z (1)	TEHQZ	TCHZ	0	7	0	8	0	10	ns
Output Hold from Address Change	TAVQX	TOH	4		5		5		ns
Output Enable to Output Valid	TGLQV	TOE		8		10		12	ns
Output Enable to Output in Low Z (1)	TGLQX	TLOZ	0		0		0		ns
Output Disable to Output in High Z(1)	TGHQZ	TOHZ	0	7	0	8	0	10	ns

* Industrial Temperature Range Only
Note 1: Parameter guaranteed, but not tested.

Read Cycle 1 - $\overline{W}$ High, $\overline{G}$, $\overline{E}$ Low



Read Cycle 2 - $\overline{W}$ High

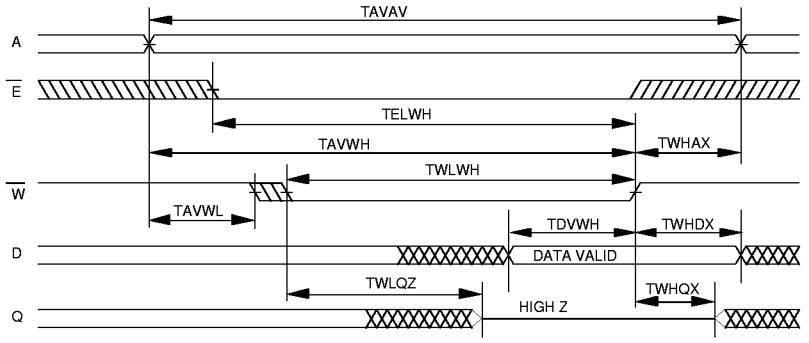


AC Characteristics Write Cycle

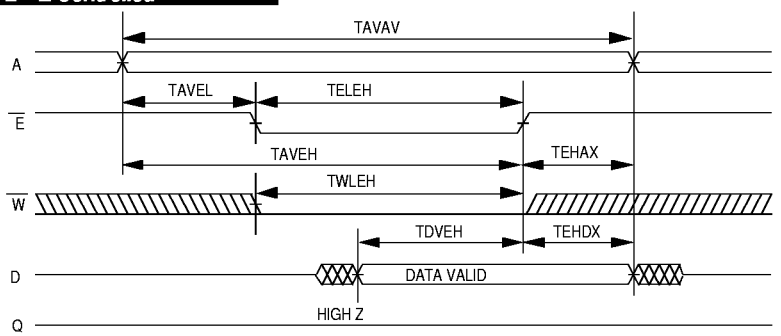
Parameter	Symbol JEDEC	Alt.	17ns* Min	Max	20ns Min	Max	25ns Min	Max	Units
Write Cycle Time	TAVAV	TWC	17		20		25		ns
Chip Enable to End of Write	TELWH	TCW	14		15		17		ns
	TELEH	TCW	14		15		17		ns
Address Setup Time	TAVWL	TAS	0		0		0		ns
	TAVEL	TAS	0		0		0		ns
Address Valid to End of Write	TAVWH	TAW	14		15		17		ns
	TAVEH	TAW	14		15		17		ns
Write Pulse Width	TWLWH	TWP	14		15		17		ns
	TWLEH	TWP	14		15		17		ns
Write Recovery Time	TWHAX	TWR	0		0		0		ns
	TEHAX	TWR	0		0		0		ns
Data Hold Time (1)	TWHDX	TDH	0		0		0		ns
	TEHDX	TDH	0		0		0		ns
Write to Output in High Z (1)	TWLQZ	TWHZ	0	8	0	8	0	10	ns
Data to Write Time	TDVWH	TDW	8		10		12		ns
	TDVEH	TDW	8		10		12		ns
Output Active from End of Write (1)	TWHQX	TWLZ	0		0		0		ns

*Industrial Temp Range Only
Note 1: Parameter guaranteed, but not tested.

Write Cycle 1 - $\overline{W}$ Controlled



Write Cycle 2 - $\overline{E}$ Controlled



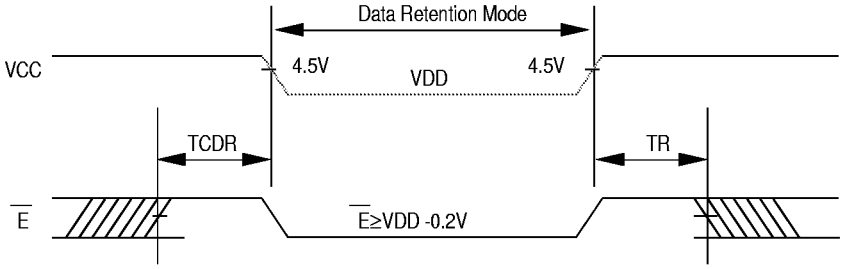
Data Retention Characteristics

EDI88512LPA Only

Characteristic	Sym	Test Conditions	VDD	Min	Typ	Max	Unit
Data Retention Voltage	VDD	E≥ VDD -0.2V VIN ≥VDD -0.2V or VIN ≤0.2V		2	--	--	V
Data Retention Quiescent Current	ICCDR		2V	--	--	2	mA
Chip Disable to Data Retention Time	TCDR			0	--	--	ns
Operation Recovery Time	TR			TAVAV	--	--	ns

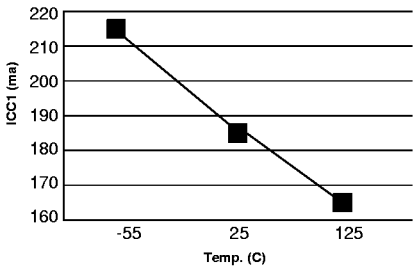
*Read Cycle Time

Data Retention $\overline{E}$ Controlled

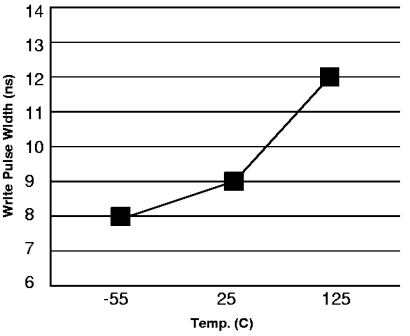


Normalized Operating Graphs

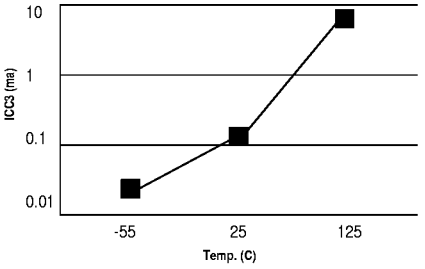
ICC1 (20ns) vs Temp



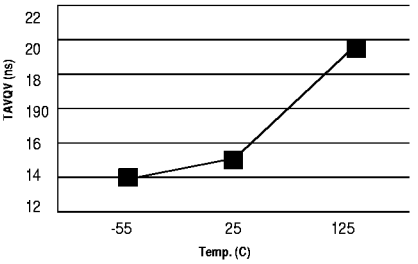
Write Pulse Width vs. Temp.



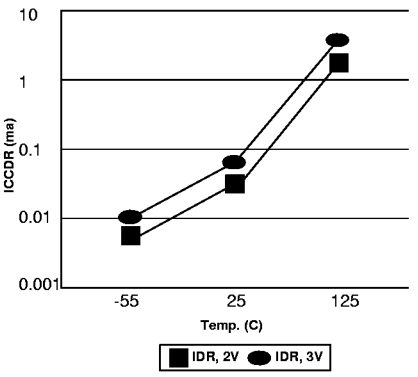
ICC3 vs. Temp



TAVQV vs. Temp



ICCDR vs. Temp



Normalized curves are offered as a service to our customers. They are not to be construed as a guarantee of operating characteristics. Characteristics of actual devices will vary.

Ordering Information

Military (-55°C to +125°C)

Part No.	Speed (ns)	Package No.
Standard Power		
EDI88512CA20MM	20	319
EDI88512CA25MM	25	319
Low Power		
EDI88512LPA20MM	20	319
EDI88512LPA25MM	25	319

Industrial (-40°C to +85°C)

Part No.	Speed (ns)	Package No.
Standard Power		
EDI88512CA17MI	17	319
EDI88512CA20MI	20	319
EDI88512CA25MI	25	319
Low Power		
EDI88512LPA17MI	17	319
EDI88512LPA20MI	20	319
EDI88512LPA25MI	25	319

Package Description

Package No. 319
36 Lead Plastic Small
Outline J-Lead Package
Theta J_A = 50°C/W
Theta J_C = 18°C/W