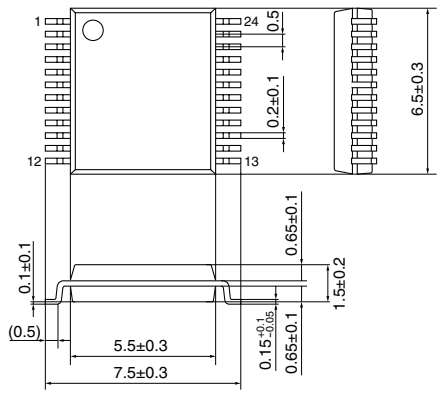
AN8049SH

1.8-volt 3-channel step-up, step-down, and polarity inverting DC-DC converter control IC

Unit : mm



SSOP024-P-0300A

Note) The package of this product will be changed to lead-free type (SSOP024-P-0300D). See the new package dimensions section later of this datasheet.

■ Overview

The AN8049SH is a three-channel PWM DC-DC converter control IC that features low-voltage operation. This IC can form a power supply that provides two step-up outputs and one step-down or polarity inverted output with a minimal number of external components. The AN8049SH features the ability to operate from a supply voltage as low as 1.8 V, and thus can be operated from two dry-batteries.

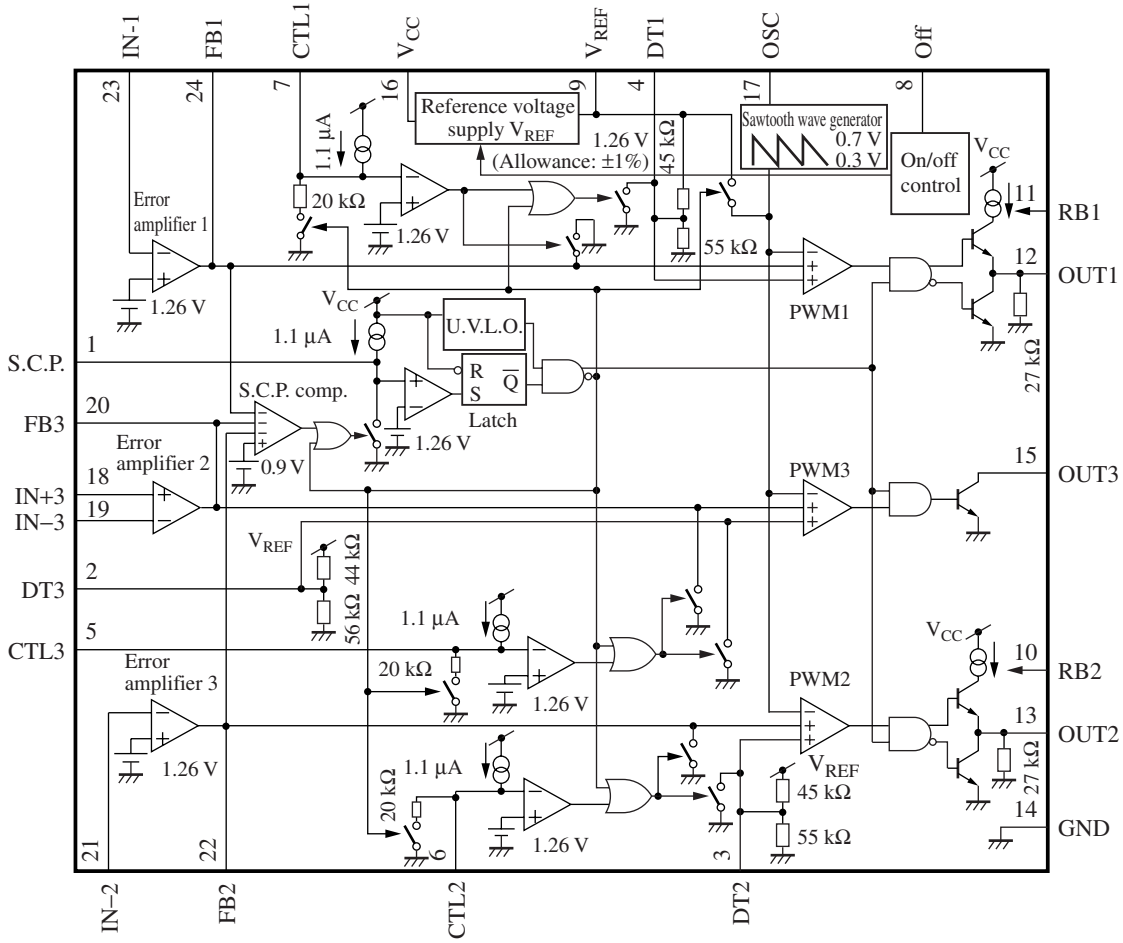
■ Features

- Wide operating supply voltage range: 1.8 V to 14 V
- High-precision reference voltage circuit
  - — V_{REF} pin voltage: ±1%
  - — Error amplifier: ±1.5%
- Surface mounting package for miniaturized and thinner power supplies
- Supports control over a wide output frequency range: 20 kHz to 1 MHz
- On/off (sequence control) pins provided for each channel for easy sequence control setup
- The negative supply error amplifier supports 0-volt input.
  Common-mode input voltage range: − 0.1 V to V_{CC} −1.4 V
  This allows the number of external components to be reduced by two resistors.
- Fixed duty factor: 86%
  However, the duty can be adjusted to anywhere from 0% to 100% with an external resistor.
- Timer latch short-circuit protection circuit (charge current: 1.1 µA typical)
- Low input voltage malfunction prevention circuit (U.V.L.O.) (operation start voltage: 1.67 V typical)
- Standby function (active-high control input, standby mode current: 1 µA maximum)
- Alternate package versions also available.
  Part No.: AN8049FHN
  Package: QFN024-P-0405A (Lead-free package)
  0.5-mm lead pitch
  Width 5.20 mm ± 0.10 mm
  Depth 4.20 mm ± 0.10 mm
  Thickness 0.8 mm (max.)

■ Applications

- Electronic equipment that requires a power supply system

■ Block Diagram



■ Pin Descriptions

Pin No.	Symbol	Description
1	S.C.P.	Connection for the capacitor that provides the short-circuit protection circuit time constant
2	DT3	Channel 3 soft start setting
3	DT2	Channel 2 soft start setting
4	DT1	Channel 1 soft start setting
5	CTL3	Channel 3 on/off control
6	CTL2	Channel 2 on/off control
7	CTL1	Channel 1 on/off control
8	Off	On/off control
9	V_{REF}	Reference voltage output
10	RB2	Connection for the OUT2 block output source current setting resistor
11	RB1	Connection for the OUT1 block output source current setting resistor
12	OUT1	OUT1 block push-pull output
13	OUT2	OUT2 block push-pull output
14	GND	Ground
15	OUT3	OUT3 block open-collector output
16	V_{CC}	Supply voltage
17	OSC	Oscillator circuit timing resistor and capacitor connection
18	IN+3	Error amplifier 3 noninverting input
19	IN−3	Error amplifier 3 inverting input
20	FB3	Error amplifier 3 output
21	IN−2	Error amplifier 2 inverting input
22	FB2	Error amplifier 2 output
23	IN−1	Error amplifier 1 inverting input
24	FB1	Error amplifier 1 output

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC}	14.2	V
Off pin allowable application voltage	V_{OFF}	14.2	V
CTL pin allowable application voltage	V_{CTL}	V_{CC} − 0.2	V
Error amplifier input pin allowable application voltage *2	V_{IN}	6	V
Supply current	I_{CC}	—	mA
OUT1 and OUT2 pin output source current	$I_{SO(OUT)}$	−50	mA
OUT3 pin output current	I_O	+50	mA
Power dissipation *1	P_D	146	mW
Operating temperature	T_{opr}	−30 to +85	°C
Storage temperature	T_{stg}	−55 to +125	°C

Note) 1. Do not apply external currents or voltages to any pins not specifically mentioned. For circuit currents, '+' denotes current flowing into the IC, and '−' denotes current flowing out of the IC.

2. Items other than the storage temperature, operating temperature, and power dissipation are all stipulated for an ambient temperature T_a = 25°C.

3. ∗1: T_a = 85°C. See the "Application Notes" for details on the relationship between IC power dissipation and the ambient temperature.

∗2: When V_{CC} < 6 V, the following condition must hold: $V_{IN-1} = V_{IN-2} = V_{CC} - 0.2$ V.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Off pin application voltage	V_{OFF}	0 to 14	V
OUT1 and OUT2 pin output source current	$I_{SO(OUT)}$	−40 to −1	mA
OUT3 pin output current	I_O	40 (max.)	
Timing resistance	R_T	3 to 33	kΩ
Timing capacitance	C_T	100 to 10 000	pF
Oscillator frequency	f_{OUT}	20 to 1 000	kHz
Short-circuit protection time-constant setting capacitance	C_{SCP}	1 000 (min.)	pF
Output current setting resistance	R_B	750 to 15 000	Ω

■ Electrical Characteristics at V_{CC} = 2.4 V, C_{REF} = 0.1 µF, T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage block						
Reference voltage	V_{REF}	I_{REF} = − 0.1 mA	1.247	1.26	1.273	V
Line regulation with input fluctuation	Line	V_{CC} = 1.8 V to 14 V	—	2	20	mV
Load regulation	Load	I_{REF} = − 0.1 mA to −1 mA	−20	−3	—	mV
U.V.L.O. block						
Circuit operation start voltage	V_{UON}		1.59	1.67	1.75	V

■ Electrical Characteristics at V_{CC} = 2.4 V, C_{REF} = 0.1 µF, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Error amplifier 1 block						
Input threshold voltage 1	V_{TH1}		1.241	1.26	1.279	V
Input bias current 1	I_{B1}		—	0.1	0.2	µA
High-level output voltage 1	V_{EH1}		1.0	1.2	1.4	V
Low-level output voltage 1	V_{EL1}		—	—	0.2	V
Output source current 1	$I_{SO(FB)1}$		–38	–31	–24	µA
Output sink current 1	$I_{SI(FB)1}$		0.5	—	—	mA
Error amplifier 2 block						
Input threshold voltage 2	V_{TH2}		1.241	1.26	1.279	V
Input bias current 2	I_{B2}		—	0.1	0.2	µA
High-level output voltage 2	V_{EH2}		1.0	1.2	1.4	V
Low-level output voltage 2	V_{EL2}		—	—	0.2	V
Output source current 2	$I_{SO(FB)2}$		–38	–31	–24	µA
Output sink current 2	$I_{SI(FB)2}$		0.5	—	—	mA
Error amplifier 3 block						
Input offset voltage	V_{IO}		–6	—	6	mV
Common-mode input voltage range	V_{ICR}		– 0.1	—	V_{CC}–1.4	V
Input bias current 3	I_{B3}		– 0.6	– 0.3	—	µA
High-level output voltage 3	V_{EH3}		1.0	1.2	1.4	V
Low-level output voltage 3	V_{EL3}		—	—	0.2	V
Output source current 3	$I_{SO(FB)3}$		–38	–31	–24	µA
Output sink current 3	$I_{SI(FB)3}$		0.5	—	—	mA
Oscillator block						
Oscillator frequency	f_{OUT}	R_T = 7.5 kΩ, C_T = 680 pF	170	190	210	kHz
Output 1 block						
Output duty factor 1	Du_1	R_T = 7.5 kΩ, C_T = 680 pF	80	86	92	%
High-level output voltage 1	V_{OH1}	I_O = –10 mA, R_B = 1 kΩ	V_{CC} –1	—	—	V
Low-level output voltage 1	V_{OL1}	I_O = 10 mA, R_B = 1 kΩ	—	—	0.2	V
Output source current 1	$I_{SO(OUT)1}$	V_O = 0.7 V, R_B = 1 kΩ	–34	–29	–24	mA
Output sink current 3	$I_{SI(OUT)1}$	V_O = 0.7 V, R_B = 1 kΩ	40	—	—	mA
Pull-down resistor 1	R_{O1}		17	27	37	kΩ
Output 2 block						
Output duty factor 2	Du_2	R_T = 7.5 kΩ, C_T = 680 pF	80	86	92	%
High-level output voltage 2	V_{OH2}	I_O = –10 mA, R_B = 1 kΩ	V_{CC} –1	—	—	V
Low-level output voltage 2	V_{OL2}	I_O = 10 mA, R_B = 1 kΩ	—	—	0.2	V
Output source current 2	$I_{SO(OUT)2}$	V_O = 0.7 V, R_B = 1 kΩ	–34	–29	–24	mA
Output sink current 2	$I_{SI(OUT)2}$	V_O = 0.7 V, R_B = 1 kΩ	40	—	—	mA

■ Electrical Characteristics at V_{CC} = 2.4 V, C_{REF} = 0.1 µF, T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Output 2 block (continued)						
Pull-down resistor 2	R_{O2}		17	27	37	kΩ
Output 3 block						
Output duty factor 3	Du_3	R_T = 7.5 kΩ, C_T = 680 pF	80	86	92	%
Output saturation voltage	$V_{O(SAT)}$	I_O = 40 mA	—	—	0.5	V
Output leakage current	I_{OLE}	V13 = 14 V	—	—	1	µA
Short-circuit protection circuit block						
Input standby voltage	V_{STBY}		—	—	0.1	V
Input threshold voltage	V_{THPC}		0.8	0.9	1.0	V
Input latch voltage	V_{IN}		—	—	0.1	V
Charge current	I_{CHG}	V_{SCP} = 0 V	−1.43	−1.1	− 0.77	µA
On/off control block						
Input threshold voltage	$V_{ON(TH)}$		0.6	0.9	1.2	V
CTL block						
Input threshold voltage	V_{THCTL}		1.07	1.26	1.45	V
Charge current	I_{CTL}	V_{CTL} = 0 V	−1.43	−1.1	− 0.77	µA
Whole Device						
Average consumption current	$I_{CC(OFF)}$	R_B = 9.1 kΩ, duty = 50%	—	4.2	5.5	mA
Standby mode current	$I_{CC(SB)}$		—	—	1	µA

• Design reference data

Note: The characteristics listed below are reference values related to the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference voltage block						
V_{REF} temperature characteristics	V_{RFEdT}	T_a = −30°C to +85°C	—	1	—	%
Error amplifier 1 block						
V_{TH} temperature characteristics	V_{THdT1}	T_a = −30°C to +85°C	—	1.5	—	%
Open loop gain 1	A_{V1}		—	80	—	dB
Error amplifier 2 block						
V_{TH} temperature variation	V_{THdT2}		—	1.5	—	%
Open loop gain 2	A_{V2}		—	80	—	dB
Error amplifier 3 block						
Open loop gain 3	A_{V3}		—	80	—	dB
Oscillator block						
Frequency supply voltage characteristics	f_{DV}	V_{CC} = 1.8 V to 14 V R_T = 7.5 kΩ, C_T = 680 pF	—	1	—	%
Frequency temperature characteristics	f_{DT}	T_a = −30°C to +85°C R_T = 7.5 kΩ, C_T = 680 pF	—	3	—	%

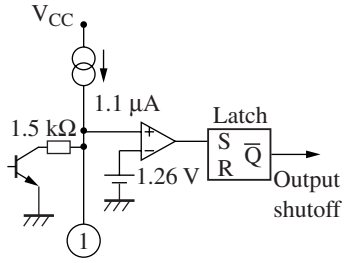
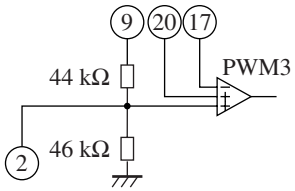
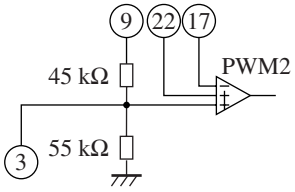
■ Electrical Characteristics at T_a = 25°C (continued)

• Design reference data (continued)

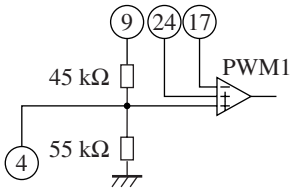
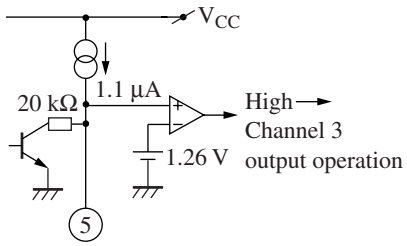
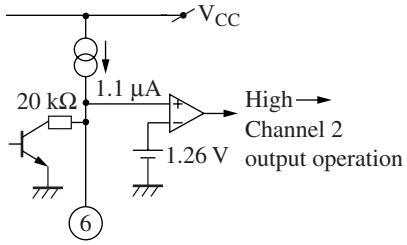
Note: The characteristics listed below are reference values related to the IC design and are not guaranteed.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Short-circuit protection circuit block						
Comparator threshold voltage	V_{THL}		—	1.26	—	V
On/off control block						
Off pin current	I_{OFF}	V_{OFF} = 5 V	—	38	—	µA

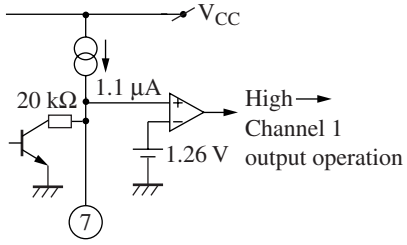
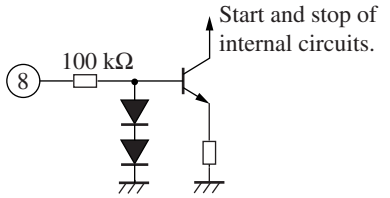
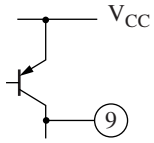
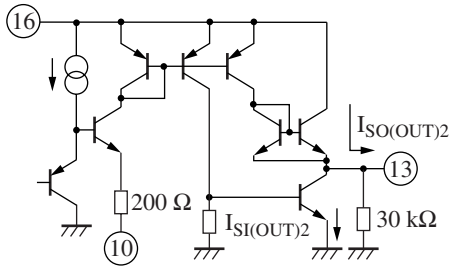
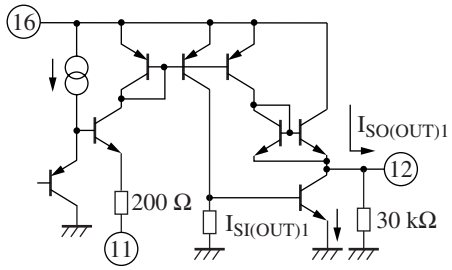
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	I/O
1		S.C.P.: Connection for the capacitor that sets the timer latch short-circuit protection circuit time constant. Use a capacitor with a value of 1 000 pF or higher. The charge current I_{CHG} is 1.1 mA typical.	O
2		DT3: Sets the channel 3 soft start time. Set the time by connecting a capacitor between this pin and ground. (See the "Application Notes, [7]" section.) Note that although the channel 3 maximum on duty is set internally to 86%, the maximum on duty can be adjusted by connecting resistors between this pin and ground, and between this pin and the V_{REF} pin. (See the "Application Notes, [6]" section.)	I
3		DT2: Sets the channel 2 soft start time. Set the time by connecting a capacitor between this pin and ground. (See the "Application Notes, [7]" section.) Note that although the channel 2 maximum on duty is set internally to 86%, the maximum on duty can be adjusted by connecting resistors between this pin and ground, and between this pin and the V_{REF} pin. (See the "Application Notes, [6]" section.)	I

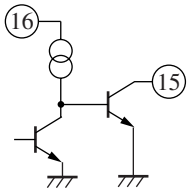
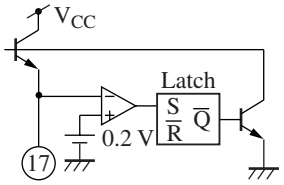
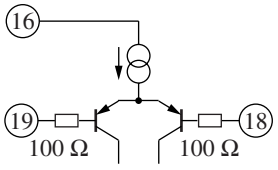
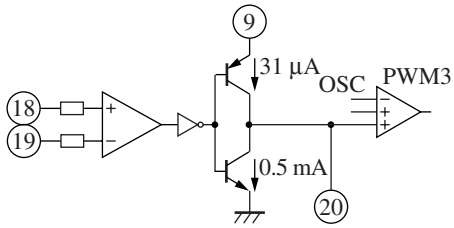
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
4		DT1: Sets the channel 1 soft start time. Set the time by connecting a capacitor between this pin and ground. (See the "Application Notes, [7]" section.) Note that although the channel 1 maximum on duty is set internally to 86%, the maximum on duty can be adjusted by connecting resistors between this pin and ground, and between this pin and the V_{REF} pin. (See the "Application Notes, [6]" section.)	I
5		CTL3: Controls the on/off state of channel 3. A delay can be provided in the power supply turn-on start time by connecting a capacitor between this pin and ground. (See the "Application Notes, [9]" section.) $t_{DLY3} = 1.26\ (V) \times C_{CTL3}\ (\mu F)/1.1\ (\mu A)$ (s) This pin can also be used to control the on/off state with an external signal. In that case, the allowable input voltage range is from 0 V to V_{CC}. Note that during U.V.L.O. and timer latch operation, this pin is connected to ground through a 20 kΩ resistor.	I
6		CTL2: Controls the on/off state of channel 2. A delay can be provided in the power supply turn-on start time by connecting a capacitor between this pin and ground. (See the "Application Notes, [9]" section.) $t_{DLY2} = 1.26\ (V) \times C_{CTL2}\ (\mu F)/1.1\ (\mu A)$ (s) This pin can also be used to control the on/off state with an external signal. In that case, the allowable input voltage range is from 0 V to V_{CC}. Note that during U.V.L.O. and timer latch operation, this pin is connected to ground through a 20 kΩ resistor.	I

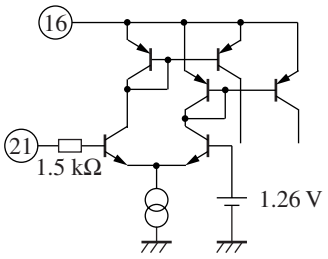
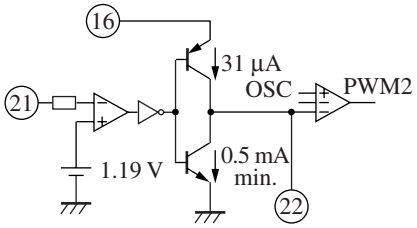
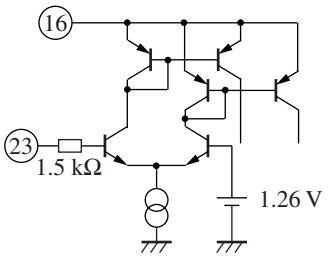
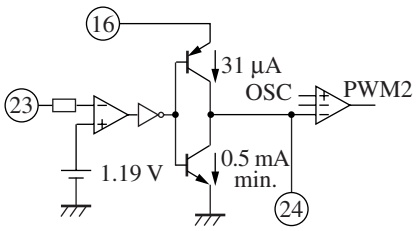
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
7		CTL1: Controls the on/off state of channel 1. A delay can be provided in the power supply turn-on start time by connecting a capacitor between this pin and ground. (See the "Application Notes, [9]" section.) $t_{DLY3} = 1.26\ (V) \times C_{CTL1}\ (\mu F)/1.1\ (\mu A)$ (s) This pin can also be used to control the on/off state with an external signal. In that case, the allowable input voltage range is from 0 V to V_{CC}. Note that during U.V.L.O. and timer latch operation, this pin is connected to ground through a 20 kΩ resistor.	I
8		Off: Controls the on/off state. When the input is high: normal operation ($V_{OFF} > 1.2$ V) When the input is low: standby mode ($V_{OFF} < 0.6$ V) In standby mode, the total current consumption is held to under 1 µA.	I
9		V_{REF}: Outputs the internal reference voltage. The reference voltage is 1.26 V (allowance: ±1%) when V_{CC} is 2.4 V and I_{REF} is − 0.1 mA. Insert a capacitor of at least 0.1 µF between V_{REF} and ground for phase compensation.	O
10		RB2: Connection for a resistor that sets the channel 2 output current. Use a resistor in the range 750 Ω to 15 kΩ.	I
11		RB1: Connection for a resistor that sets the channel 1 output current. Use a resistor in the range 750 Ω to 15 kΩ.	I

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
12	See pin 11.	OUT1: Push-pull output. The absolute maximum rating for the output source current is –50 mA. The output source current is set by the external resistor connected to the RB1 pin.	O
13	See pin 10.	OUT2: Push-pull output. The absolute maximum rating for the output source current is –50 mA. The output source current is set by the external resistor connected to the RB2 pin.	O
14		GND: Ground	—
15		OUT3: Open-collector output. The absolute maximum rating for the output current is +50 mA.	O
16		V_{CC}: Power supply. Provide the operating supply voltage in the range 1.8 V to 14 V.	—
17		OSC: Connection for the capacitor and resistor that determine the oscillator frequency. Use a capacitor in the range 100 pF to 1 000 pF and a resistor in the range 3 kΩ to 33 kΩ. Use an oscillator frequency in the range 20 kHz to 1 MHz.	O
18		IN+3: Noninverting input to the error amplifier 3.	I
19		IN–3: Inverting input to the error amplifier 3.	I
20		FB3: Output from the error amplifier 3. This circuit can provide a source current of –31 µA or a sink current of 0.5 mA (minimum).	O

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	I/O
21		IN−2: Inverting input to the error amplifier 2.	I
22		FB2: Output from the error amplifier 2. This circuit can provide a source current of −31 µA or a sink current of 0.5 mA (minimum).	O
23		IN−1: Inverting input to the error amplifier 1.	I
24		FB1: Output from the error amplifier 1. This circuit can provide a source current of −31 µA or a sink current of 0.5 mA (minimum).	O

■ Usage Notes

[1] Allowable power dissipation

1. Since the power dissipation (P) in this IC increases proportionally with the supply voltage, applications must be careful to operate so that the loss does not exceed the allowable power dissipation, P_D, for the package. See the P_D — T_a curve.

   Reference formula:

   $P = (V_{CC} - V_{BEQ1}) \times I_{SO(OUT)1} \times Du_1 + (V_{CC} - V_{BEQ2}) \times I_{SO(OUT)2} \times Du_2 + V_{O(SAT)3} \times I_{OUT3} \times Du_3 + V_{CC} \times I_{CC} < P_D$

   V_{BEQ1} : The voltage between the base and emitter of the channel 1 npn transistor

   $I_{SO(OUT)1}$: The OUT1 pin output source current
   (This is set by the resistor connected to the RB1 pin. When R_B is 1 kΩ, $I_{SO(OUT)1}$ will be 34 mA, maximum.)

   Du_1 : The output 1 on-duty

   V_{BEQ2} : The voltage between the base and emitter of the channel 2 npn transistor

   $I_{SO(OUT)2}$: The OUT2 pin output source current
   (This is set by the resistor connected to the RB2 pin. When R_B is 1 kΩ, $I_{SO(OUT)2}$ will be 34 mA, maximum.)

   Du_2 : The output 2 on-duty

   $V_{O(SAT)3}$: The OUT3 pin saturation voltage (0.5 V maximum when I_{OUT3} is 40 mA.)

   I_{OUT3} : The OUT3 pin current (This will be $\{V_{CC} - V_{BEQ3} - V_{O(SAT)3}\}/R_{O3}$.)

   Du_3 : The output 3 on-duty

   I_{CC} : The V_{CC} pin current

2. If the IC is shorted to ground, shorted to V_{CC}, or inserted incorrectly, either the device itself or peripheral components will be destroyed.

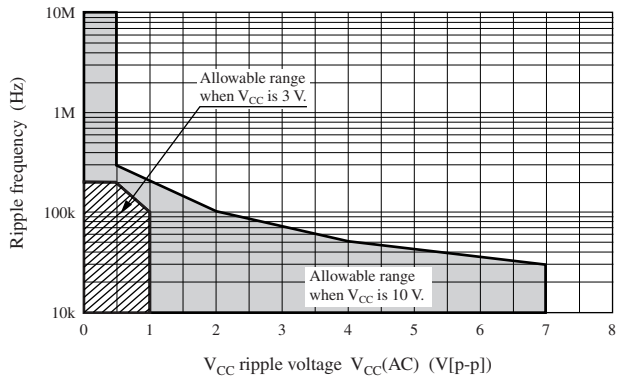
[2] Allowable V_{CC} ripple

V_{CC} ripple due to the switching transistor being turned on and off can cause this IC's U.V.L.O. circuit, which is biased by V_{CC}, to operate incorrectly, and can cause the S.C.P. capacitor charging operation to fail to start when the output is shorted.

The figure shows the allowable range for V_{CC} ripple. Applications should reduce V_{CC} ripple either by inserting a ripple filter in the V_{CC} line or by inserting a capacitor between the IC GND and V_{CC} pins and locating that capacitor as close to the IC as possible.

Note that the allowable range shown here is the result of testing the IC independently, and that the allowable range may differ depending on the actual system of the power supply circuit. Also note that this allowable range is a design target, and is not guaranteed by testing of all samples.

Allowable V_{CC} ripple



■ Usage Notes (continued)

[3] Notes on MOS drive

Since the AN8049SH channel 1 and 2 output circuits were designed to drive bipolar transistors, the following points require care if this device is used to drive n-channel MOS transistors directly.

1. Use an n-channel MOS transistor with a low input capacitance.

   The AN8049SH is designed to drive bipolar transistors, and adopts a circuit structure that can provide a constant-current (50 mA maximum) output source current. Furthermore, it has a sink current capacity of 80 mA maximum. This means that designs must be concerned about increased loss due to longer rise- and fall-times. If a problem occurs, an inverter may be inserted as shown in figure 1 to provide amplification.

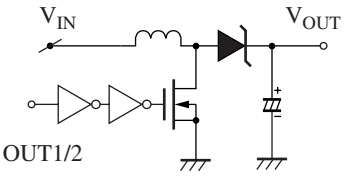
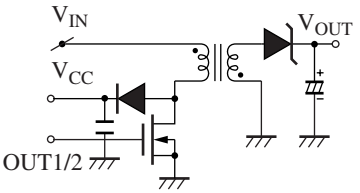


Figure 1. Output bootstrap circuit

2. Use an n-channel MOS transistor with a low gate-threshold voltage.

   Since the AN8049SH OUT1 and OUT2 pin high-level output voltage is V_{CC} − 1.0 V (minimum), low V_T MOS transistors with an adequately low on-resistance must be used. Also, if a large V_{GS} is required, one solution is to use a transformer as shown in figure 2, and apply a voltage that is twice the input voltage to the IC's V_{CC} pin.

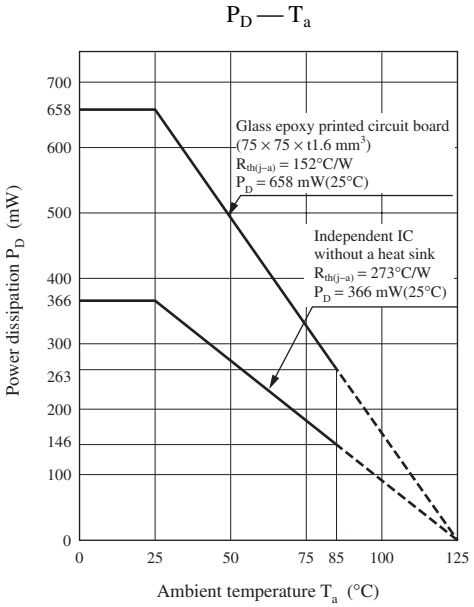


$$V_{CC} \approx 2 \times V_{IN} - VD$$

Figure 2. Gate drive voltage bootstrap technique

■ Application Notes

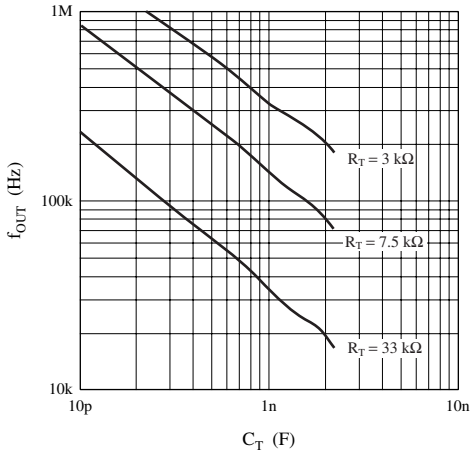
[1] P_D — T_a curves of SSOP024-P-0300A



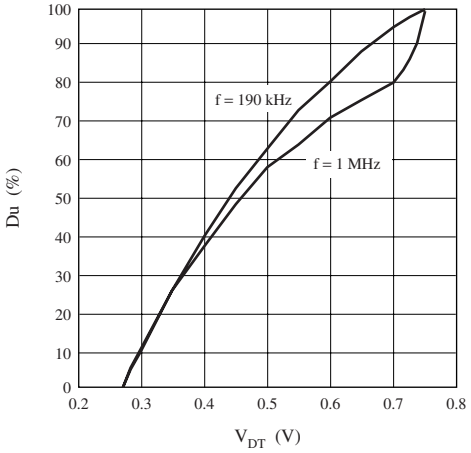
■ Application Notes (continued)

[2] Main characteristics

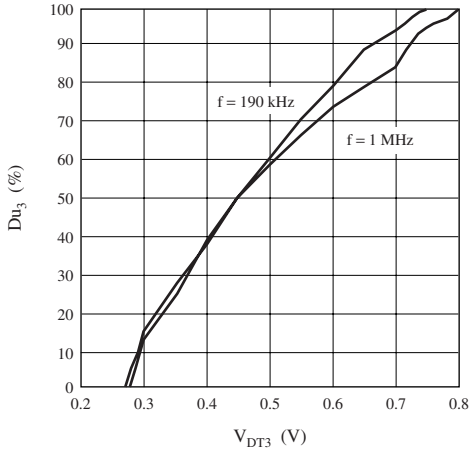
Timing capacitance — Oscillator frequency



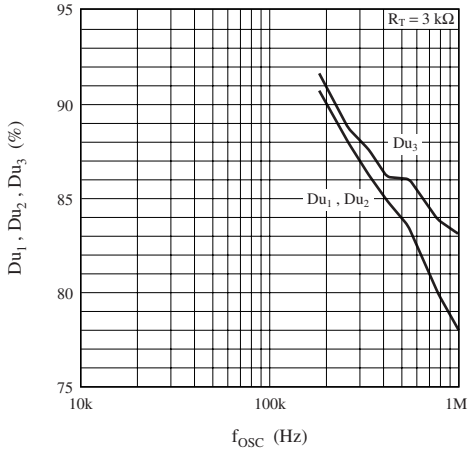
DT1 and DT2 pin voltage — Maximum on-duty



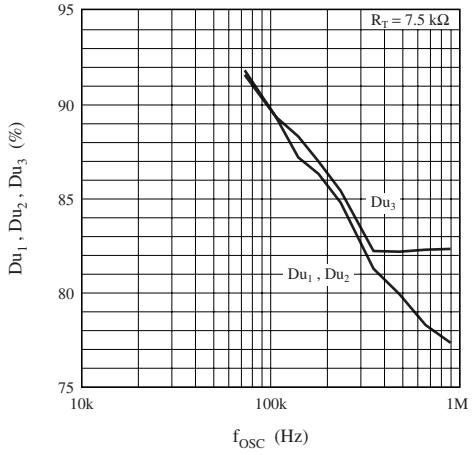
DT3 pin voltage — Maximum on-duty



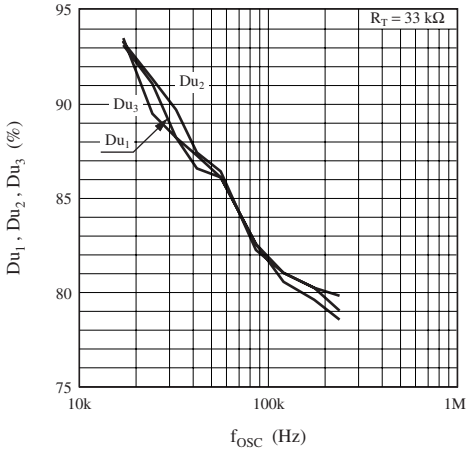
f_{OSC} — Maximum output duty



f_{OSC} — Maximum output duty



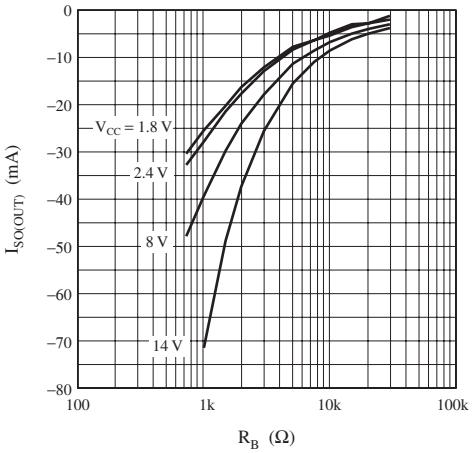
f_{OSC} — Maximum output duty



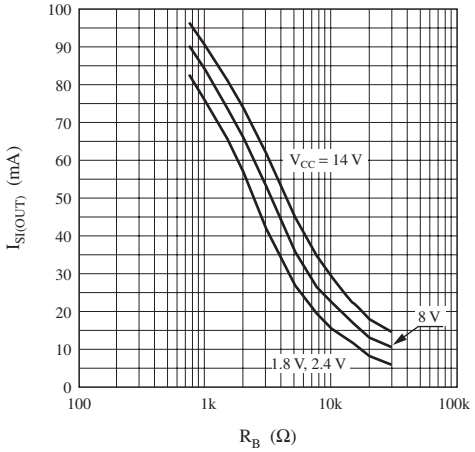
■ Application Notes (continued)

[2] Main characteristics (continued)

R_B — $I_{SO(OUT)}$

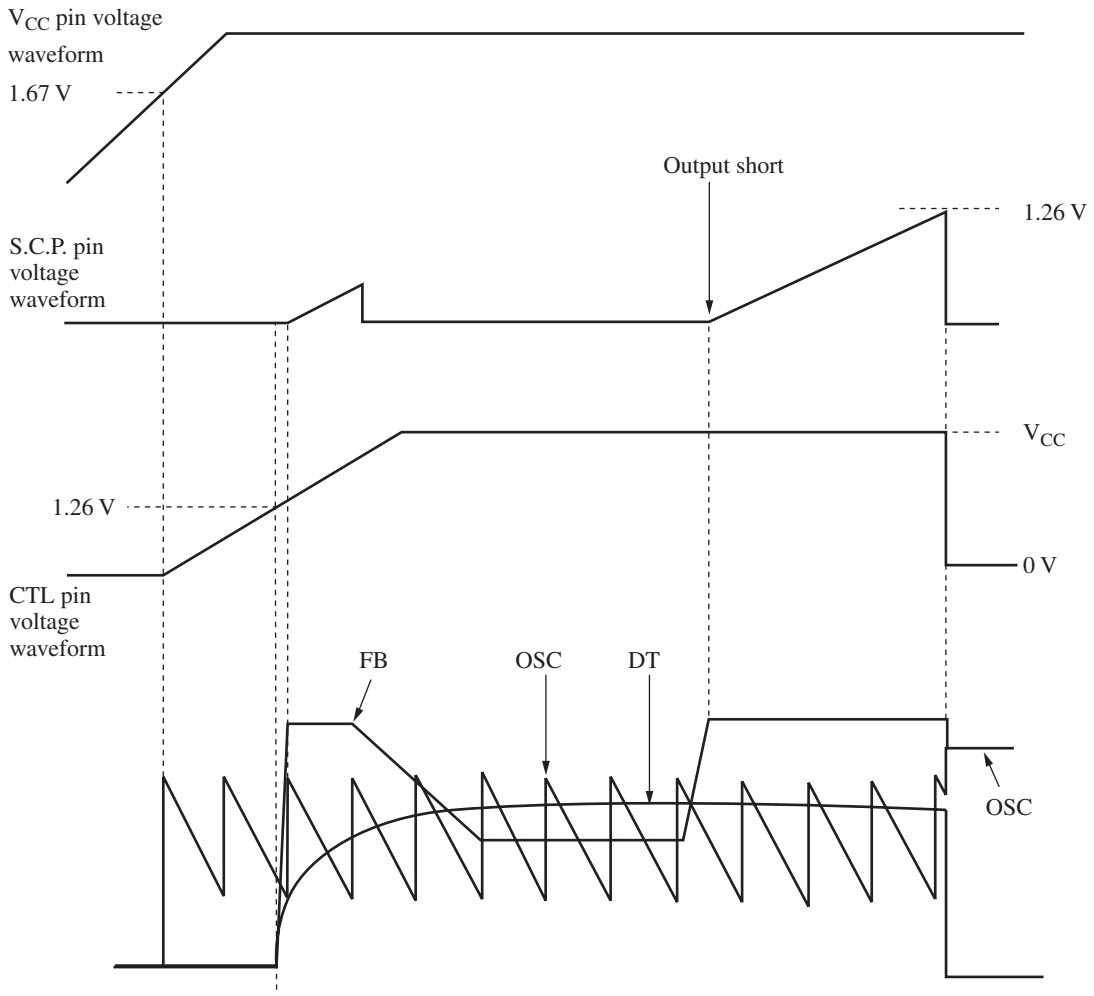


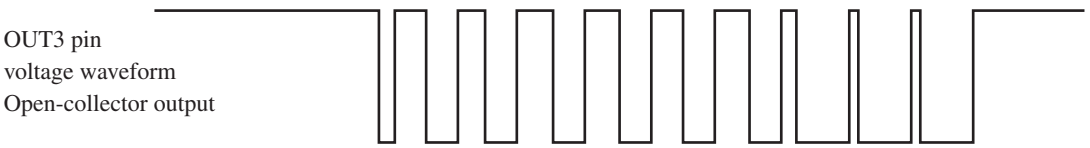
R_B — $I_{SI(OUT)}$



■ Application Notes (continued)

[3] Timing charts





■ Application Notes (continued)

[4] Function descriptions

1. Reference voltage block

This circuit is composed of a band gap circuit, and outputs a 1.26 V (typical) reference voltage that is temperature compensated to a precision of ±1%. This reference voltage is stabilized when the supply voltage is 1.8 V or higher. This reference voltage is used by error amplifiers 1 and 2.

2. Triangular wave generator

This circuit generates a triangular wave like a sawtooth with a peak of 0.7 V and a trough of 0.2 V using a capacitor C_T (for the time constant) and resistor R_T connected to the OSC1 pin (pin 17). The oscillator frequency can be set to an arbitrary value by selecting appropriate values for the external capacitor C_T and resistor R_T. This IC can use an oscillator frequency in the range 20 kHz to 1 MHz. The triangular wave signal is provided to the noninverting input of the PWM comparator in each channel internally to the IC. Use the formulas below for rough calculation of the oscillator frequency.

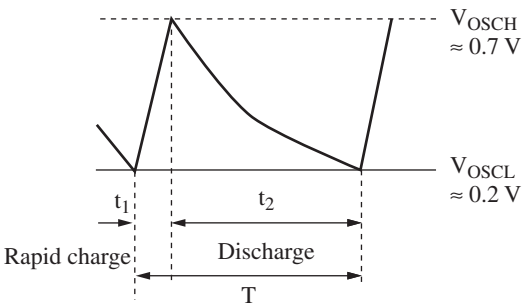


Figure 1. Triangular oscillator waveform

$$f_{OSC} \approx -\frac{1}{C_T \times R_T \times \ln \dfrac{V_{OSCL}}{V_{OSCH}}} \approx 0.8 \times \frac{1}{C_T \times R_T} \quad \text{(Hz)}$$

Note, however, that the above formulas do not take the rapid charge time, overshoot, and undershoot into account. See the experimentally determined graph of the oscillator frequency vs. timing capacitance value provided in the main characteristics section.

3. Error amplifier 1

This circuit is an npn-transistor input error amplifier that detects and amplifies the DC-DC converter output voltage, and inputs that signal to a PWM comparator. The 1.26 V internal reference voltage is applied to the noninverting input. Arbitrary gain and phase compensation can be set up by inserting a resistor and capacitor in series between the FB1 pin (pin 24) and the IN−1 pin (pin 23). The output voltage V_{OUT1} can be set using the circuit shown in the figure.

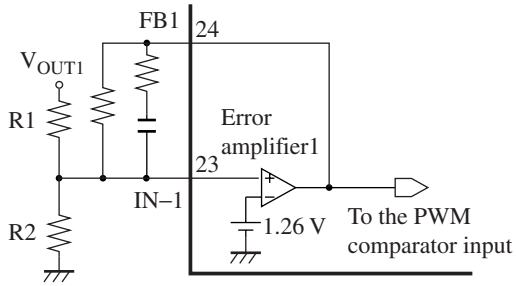


Figure 2. Connection method of error amplifier 1 (Step-up output)

4. Error amplifier 2

This circuit is an npn-transistor input error amplifier that detects and amplifies the DC-DC converter output voltage and inputs that signal to a PWM comparator. The 1.26 V internal reference voltage is applied to the noninverting input. Arbitrary gain and phase compensation can be set up by inserting a resistor and capacitor in series between the FB2 pin (pin 22) and the IN−2 pin (pin 21). The output voltage V_{OUT2} can be set using the circuit shown in the figure.

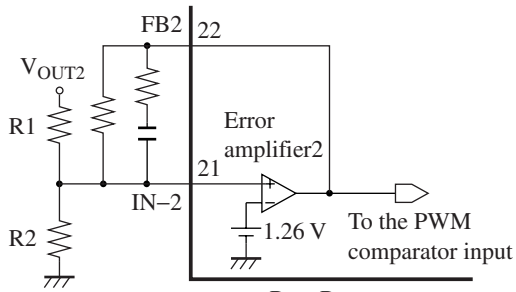


Figure 3. Connection method of error amplifier 2 (Step-up output)

■ Application Notes (continued)

[4] Function descriptions (continued)

5. Error amplifier 3

This circuit is an pnp-transistor input error amplifier that detects and amplifies the DC-DC converter output voltage and inputs that signal to a PWM comparator. Arbitrary gain and phase compensation can be set up by inserting a resistor and capacitor in series between the FB3 pin (pin 20) and the IN−3 pin (pin 19). The output voltage V_{OUT3} can be set using the circuit shown in the figure.

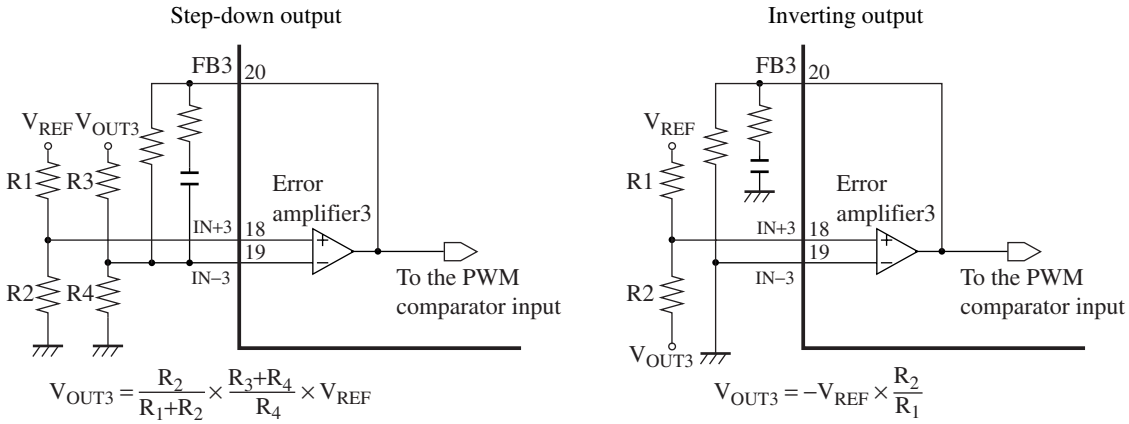


Figure 4. Connection method of error amplifier 3

6. Timer latch short-circuit protection circuit

This circuit protects the external main switching elements, flywheel diodes, choke coils, and other components against degradation or destruction if an excessive load or a short circuit of the power supply output continues for longer than a certain fixed period.

The timer latch short-circuit protection circuit detects the output of the error amplifiers. If the DC-DC converter output voltage drops and an FB pin (pins 20, 22, or 24) voltage exceeds 0.9 V, the S.C.P. comparator outputs a low level and the timer circuit starts. This starts charging the external protection circuit delay time capacitor.

If the error amplifier output does not return to the normal voltage range before that capacitor reaches 1.26 V, the latch circuit latches, the output drive transistors are turned off, and the dead-time is set to 100%. (See the "[5] Time constant setup for the timer latch short-circuit protection circuit" section later in this document.)

7. Low input voltage malfunction prevention circuit (U.V.L.O.)

This circuit protects the system against degradation or destruction due to incorrect control operation when the power supply voltage falls during power on or power off.

The low input voltage malfunction prevention circuit detects the internal reference voltage that changes with the supply voltage level. While the supply voltage is rising, this circuit cuts off the output drive transistor until the reference voltage reaches 1.67 V. It also sets the dead-time to 100 % and at the same time holds the S.C.P. pin (pin 1) and the DT pins (pins 2, 3, and 4) at 0 V, and the OSC pin (pin 17) at about 1.2 V.

8. PWM comparators

The PWM comparators control the on-period of the output pulse according to their input voltage. The PWM 1 and PWM 2 comparators reverse the logic of their inputs when adjusting the on-period of their respective output.

The output transistors are turned on during periods when the OSC pin (pin 17) triangular waveform is lower than both of the corresponding FB pin (pins 20, 22, or 24) and the corresponding DT pin (pins 2, 3, or 4).

The maximum duty is set to 86 % internally, but can be set to a value in the range 0% to 100% by inserting a resistor between the DT pin and ground, or the DT pin and V_{REF} pin. (See the "[6] Setting the maximum duty" section later in this document.)

The IC's soft start function operates to gradually increase the width of the output pulse on-period during startup if a capacitor is inserted between the DT pin and ground. See the "[7] Setting the soft start time" section later in this document.

■ Application Notes (continued)

[4] Function descriptions (continued)

9. Output 1 and output 2 blocks

These output circuits have a totem pole structure. A constant-current source output with good line regulation can be set up freely by connecting current setting resistors to the RB pins (pins 10 and 11).

See the "[2] Main characteristics" section earlier in this document for details on the R_B vs. $I_{SO(OUT)}$ and R_B vs. $I_{SI(OUT)}$ characteristics.

10. Output 3 block

This output circuit has an open collector structure.

An output current of up to 50 mA can be provided, and the output pin has a breakdown voltage of 14.2 V.

11. CTL block

This block controls the on/off state of each channel. See the "[9] Sequential operation" section later in this document.

[5] Time constant setup for the timer latch short-circuit protection circuit

Figure 6 shows the structure of the timer latch short-circuit protection circuit. The short-circuit protection comparator continuously compares a 0.9 V reference voltage with the FB1, FB2, and FB3 error amplifier outputs.

When the DC-DC converter output load conditions are stable, the short-circuit protection comparator holds its average value since there are no fluctuations in the error amplifier outputs. At this time, the output transistor Q1 will be in the conducting state, and the S.C.P. pin will be held at 0 V.

If the output load conditions change rapidly and a high-level signal (0.9 V or higher) is input to the short-circuit protection comparator from the error amplifier output, the short-circuit protection comparator will output a low level and the output transistor Q1 will shut off. Then, the capacitor C_{SCP} connected to the S.C.P. pin will start to charge. When the external capacitor C_{SCP} is charged to about 1.26 V by the constant current of about 1.1 mA, the latch circuit will latch and the dead-time will be set to 100% with the output held fixed at the low level. Once the latch circuit has latched, the S.C.P. pin capacitor will be discharged to about 0 V, but the latch circuit will not reset unless either power is turned off or the power supply is re-started by on/off control.

$$1.26\ \text{V} = I_{CHG} \times \frac{t_{PE}}{C_{SCP}}$$

$$\therefore\ t_{PE}\ (\text{s}) = 1.15 \times C_{SCP}\ (\mu\text{F})$$

At power supply startup, the output appears to be in the shorted state, and the IC starts to charge the S.C.P. pin capacitor. Therefore, users must select an external capacitor that allows the DC-DC converter output voltage to rise before the latch circuit in the later stage latches. In particular, care is required if the soft start function is used, since that function makes the startup time longer.

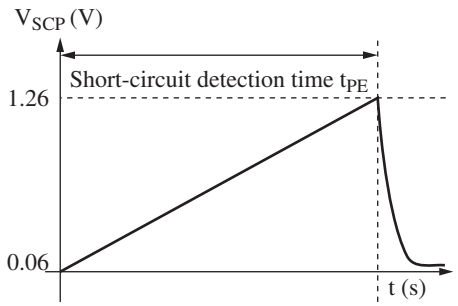


Figure 5. S.C.P. pin charging waveform

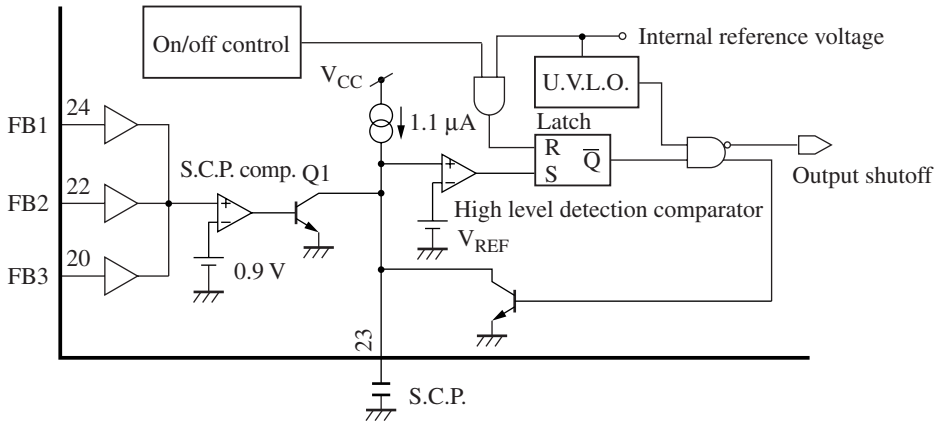


Figure 6. Short-circuit protection circuit

■ Application Notes (continued)

[6] Setting the maximum duty

The maximum duty is set to 86% internally to the IC. However, this setting can be changed to be any value in the range 0% to 100% by adding an external resistor.

1. To use a duty lower than the current duty (80% to 92%)

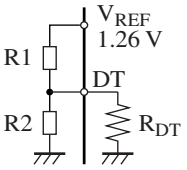
Insert the resistor R_{DT} between the DT pin and ground.

Determine the DT pin voltage for the required duty from the provided DT pin voltage vs. maximum on-duty characteristics in the "[2] Main characteristics" section and determine the value of the external resistor R_{DT} from formula A.

Note that there is a sample-to-sample variation of −19% to +33% due to temperature characteristics and sample-to-sample variations of the internal resistors R1 and R2. (However, the direction of the sample-to-sample variations is identical for R1 and R2.) Determine the size of the sample-to-sample variations in the DT pin voltage V_{DT} from formula B, and estimate the size of the sample-to-sample variation in the duty from the provided DT pin voltage vs. maximum on-duty characteristics in the "[2] Main characteristics" section .

$$R_{DT} = \frac{V_{DT}}{\frac{V_{REF}}{R_1} - (\frac{1}{R_1} + \frac{1}{R_2}) \times V_{DT}} \quad \cdots\cdots\cdots A$$

$$V_{DT} = \frac{R_2 / R_{DT}}{R_1 + R_2 / R_{DT}} \times V_{REF} \quad \cdots\cdots\cdots B$$



	ch.1, 2	ch.3
R1	45 kΩ	44 kΩ
R2	55 kΩ	56 kΩ

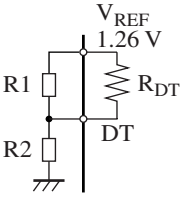
2. To use a duty higher than the current duty (80% to 92%)

Insert the resistor R_{DT} between the DT pin and the V_{REF} pin.

Use formulas C and D to determine the value of the external resistor R_{DT} and the size of the sample-to-sample variations in the same manner as in item 1 above.

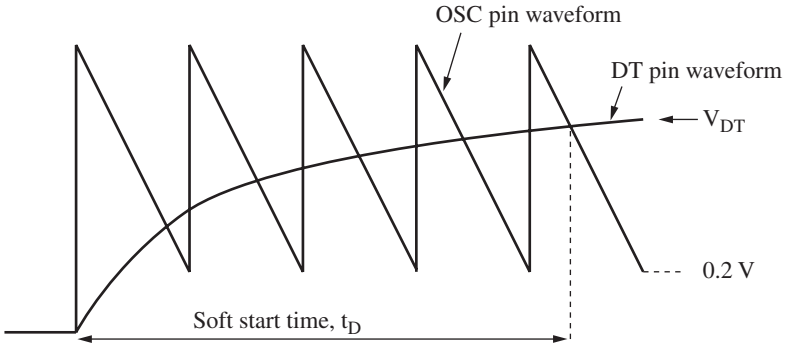
$$R_{DT} = \frac{V_{REF} - V_{DT}}{(\frac{1}{R_1} + \frac{1}{R_2}) \times V_{DT} - \frac{V_{REF}}{R_1}} \quad \cdots\cdots\cdots C$$

$$V_{DT} = \frac{R_2}{R_2 + R_1 / R_{DT}} \times V_{REF} \quad \cdots\cdots\cdots D$$



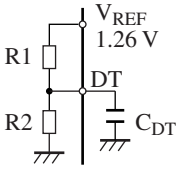
[7] Setting the soft start time

The soft start time is determined by the value of the capacitor connected between the DT pin and ground.



Use the following formula to set the soft start time t_D.

$$t_D = -R_2 \times C_{DT} \times \ln (1 - \frac{V_{DT}}{V_{REF} - V_{DT}} \times \frac{R_1}{R_2})$$



	ch.1, 2	ch.3
R1	45 kΩ	44 kΩ
R2	55 kΩ	56 kΩ

■ Application Notes (continued)

[8] Parallel synchronous operation of multiple ICs

Multiple instances of this IC can be operated in parallel. If the OSC pins (pin 17) and OFF pins (pin 8) are connected to each other as shown in figure 7, the ICs will operate at the same frequency.

It is also possible to operate a one-channel control IC (e.g. the AN8016SH or AN8016NSH) and a two-channel control IC (e.g. the AN8017SA or AN8018SA) in this parallel synchronous mode. In this case, short the OSC and Off pins together.

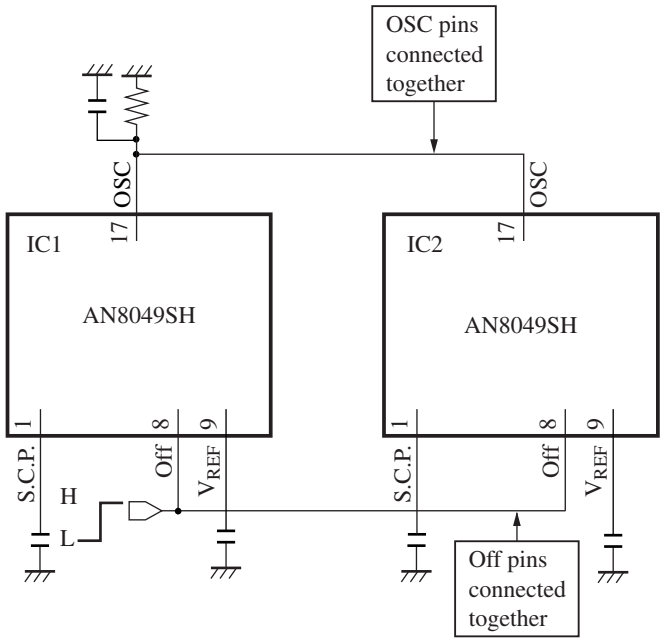


Figure 7. Slave operation circuit example

Notes on parallel operation:

1. The remote on/off state of each individual IC cannot be controlled independently.

   In this sort of circuit, always connect all the Off pins together, and control the on/off states of the multiple ICs at the same time.

   The reason for this is that if, for example, IC1 is solely turned on/off, the sawtooth wave will be stopped temporarily and the OSC pin held fixed at about 1.2 V. As a result the IC2 OUT1 to OUT3 pins will be forced temporarily to the full off-state and the DC-DC converter output voltage will fall.

2. All ICs are shut down when an output shorted state occurs.

   For example, if the IC1 output voltage falls, its output short-circuit protection circuit will operate, and the latch circuit will latch. When this happens, the IC1 output stops, and at the same time the sawtooth oscillator stops, and the OSC pin is held fixed at about 1.2 V.

   As a result, the IC2 OUT1 to OUT3 pins temporarily go to the full off-state, and the DC-DC converter output voltage will drop. Finally, the IC2 output short-circuit protection circuit will operate, and the latch will go to the latched state. This behavior will also occur if the IC2 output falls first.

■ Application Notes (continued)

[9] Sequential operation

Sequential operation under the control of external capacitors

Delays can be provided in the startup times by inserting capacitors (C_{CTL}) between the CTL pins and ground.

Delay time: $t_{DLY} = 1.26\ (V) \times C_{CTL}\ (\mu F)/1.1\ (\mu A)$ (s)

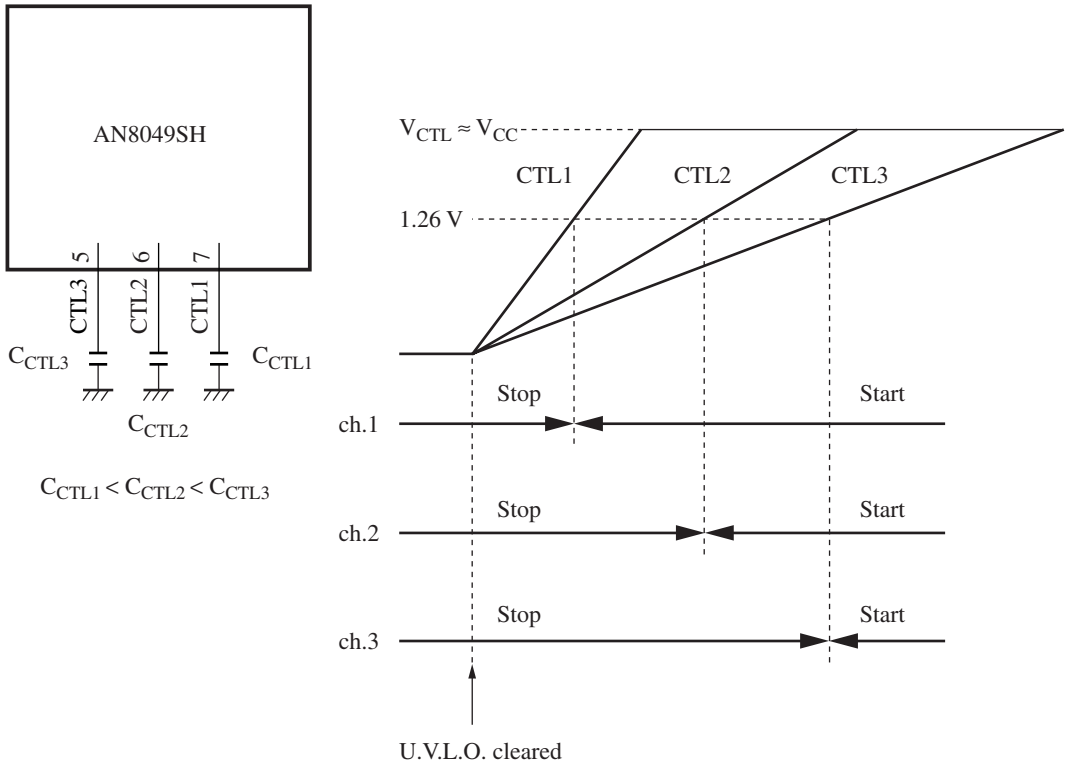


Figure 8. Sequential operation using external capacitors

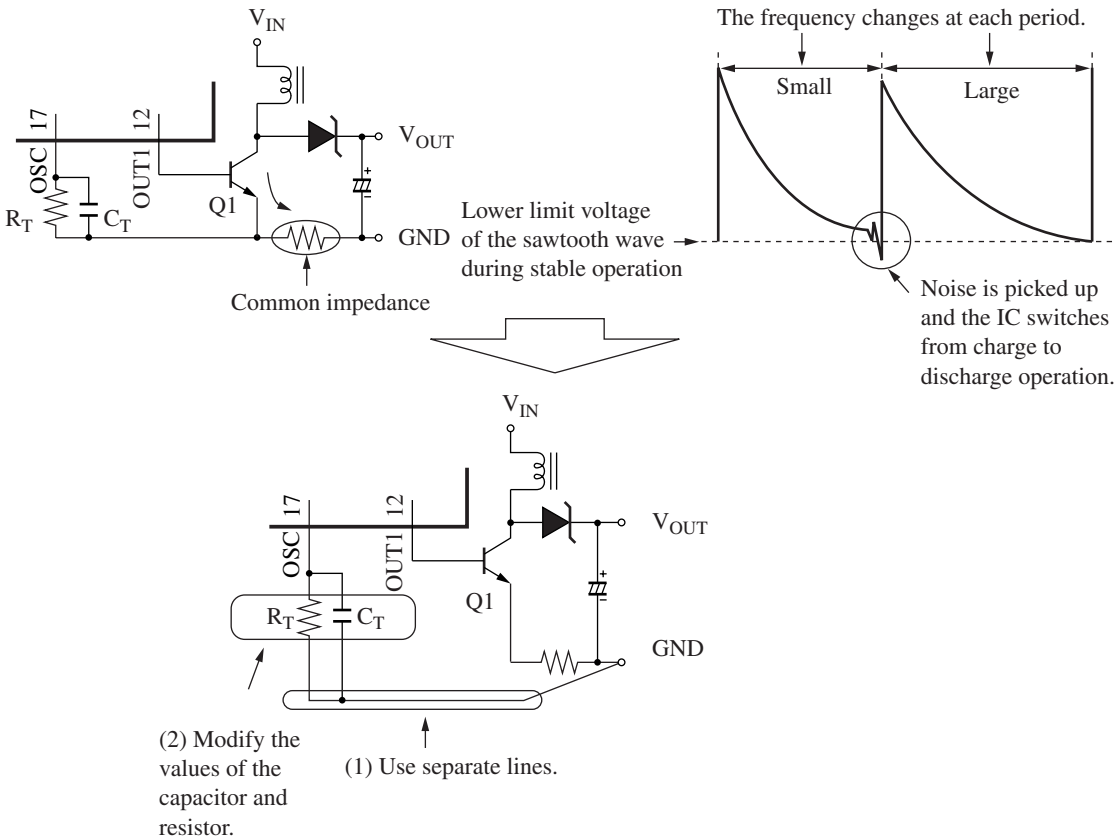
■ Application Notes (continued)

[10] Notes on power supply printed circuit board design

Careful attention must be paid to the following points when designing the printed circuit board layout to achieve low noise and high efficiency.

1. Use extremely wide lines for the ground lines, and isolate the IC ground from the power system ground.
   In particular, during light-load operation (when the on-duty is low) switching noise can enter the system at the lower limit of the sawtooth waveform causing the operating frequency to vary every period and resulting in unstable control.
   Take measures described as 1) and 2) below, and assure that switching noise does not appear on the sawtooth waveform.
   1) Use a ground line separate from the power system ground for the capacitor and resistor connected to the OSC pin.
   2) Lower the OSC pin impedance by either decreasing the value of the resistor R_T or increasing the value of the capacitor C_T.

   (See the figures below.)



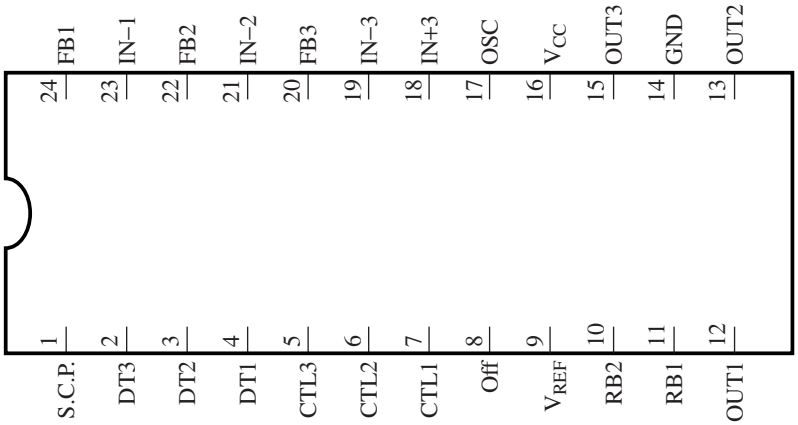
2. Position input filter capacitors as close as possible to the V_{CC} and ground pins.
   If switching noise cannot be suppressed even with exceptionally large capacitors, or if there are limitations on the size of capacitors that can be used, install an CR filter in the input to reduce switching noise. Problems may occur if switching noise enters the IC by any route.
3. Keep the length of the line between the OUT pin and the switching device as short as possible to provide a clean switching waveform to the switching device.
4. Use longer lines for the low-impedance side of the output voltage detection resistors.

■ Application Notes (continued)

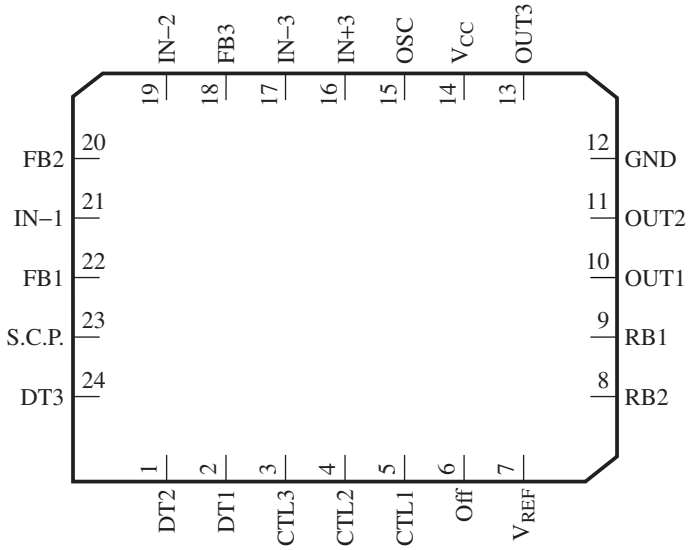
[11] Differences between this IC and the AN8049FHN

The pin arrangements differ. The AN8049FHN is a alternative package version of this IC.

AN8049SH



AN8049FHN

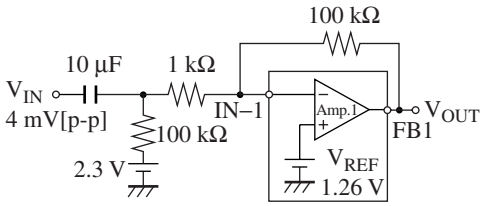


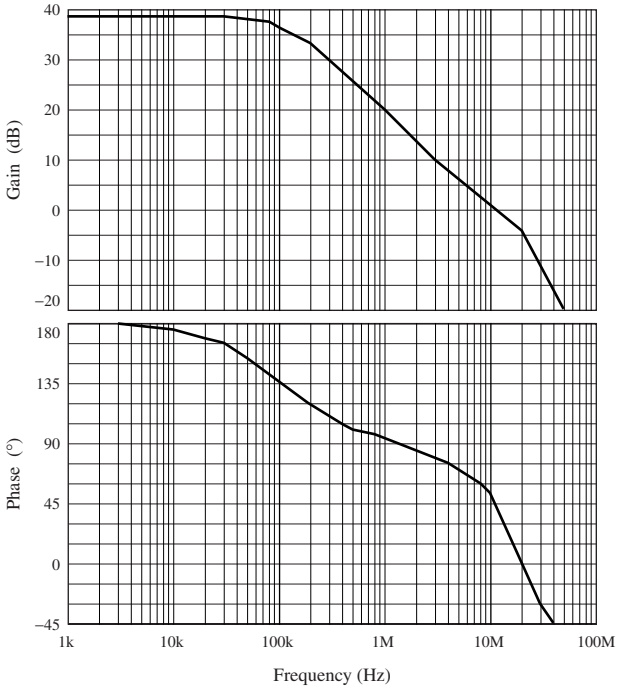
■ Application Notes (continued)

[12] Error amplifier frequency characteristics

1. Error amplifiers 1 and 2

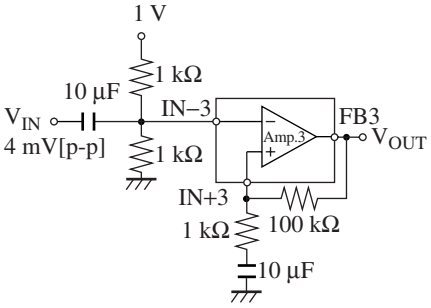
(Test circuit)

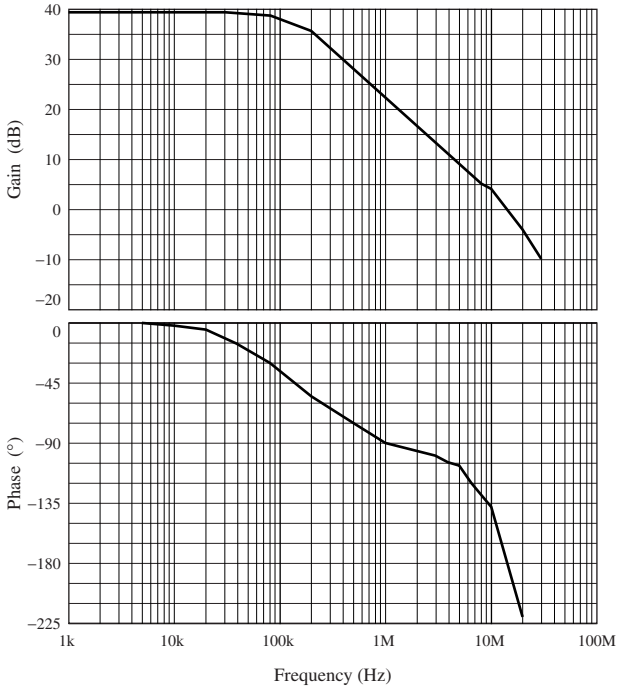




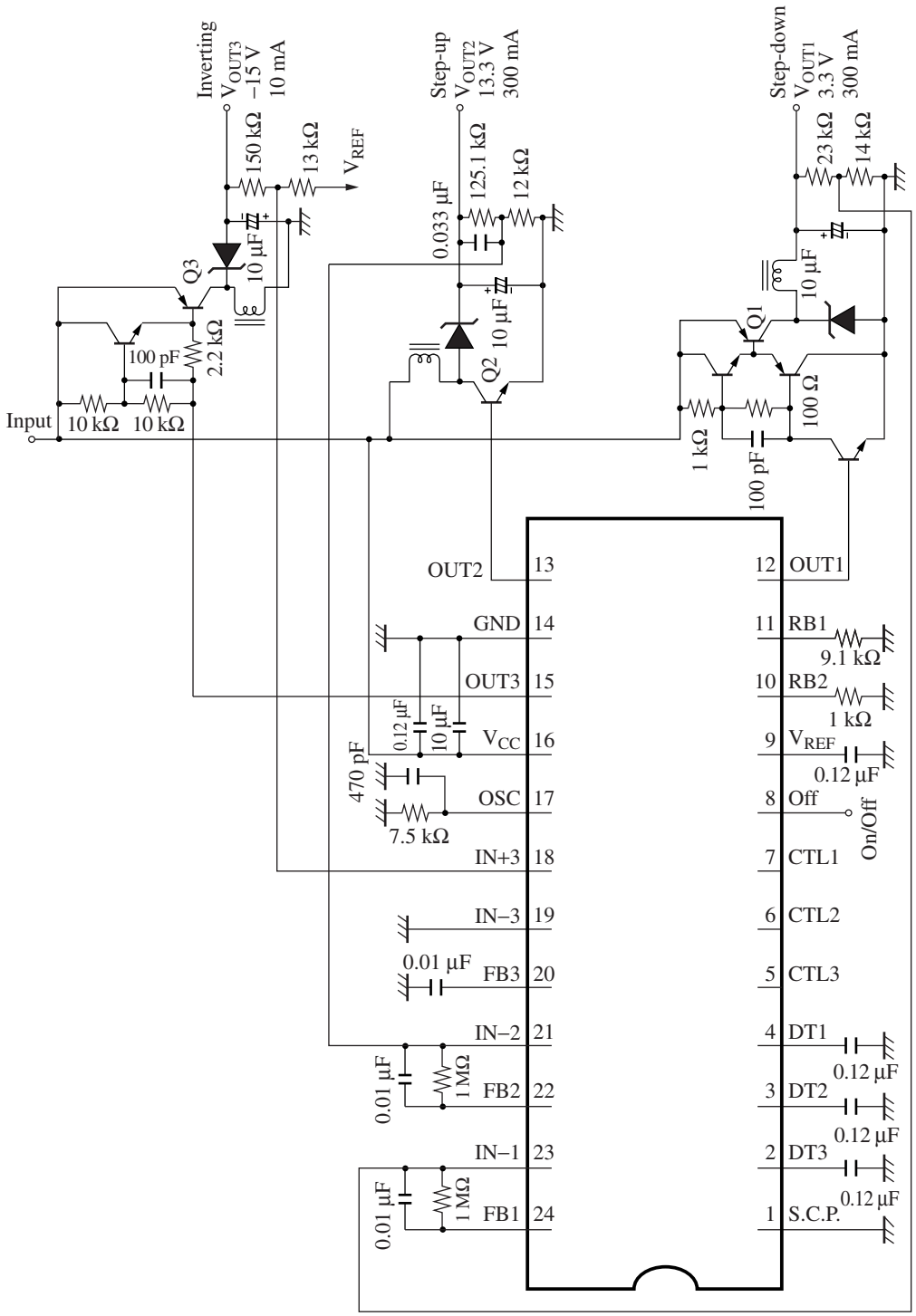
2. Error amplifier 3

(Test circuit)





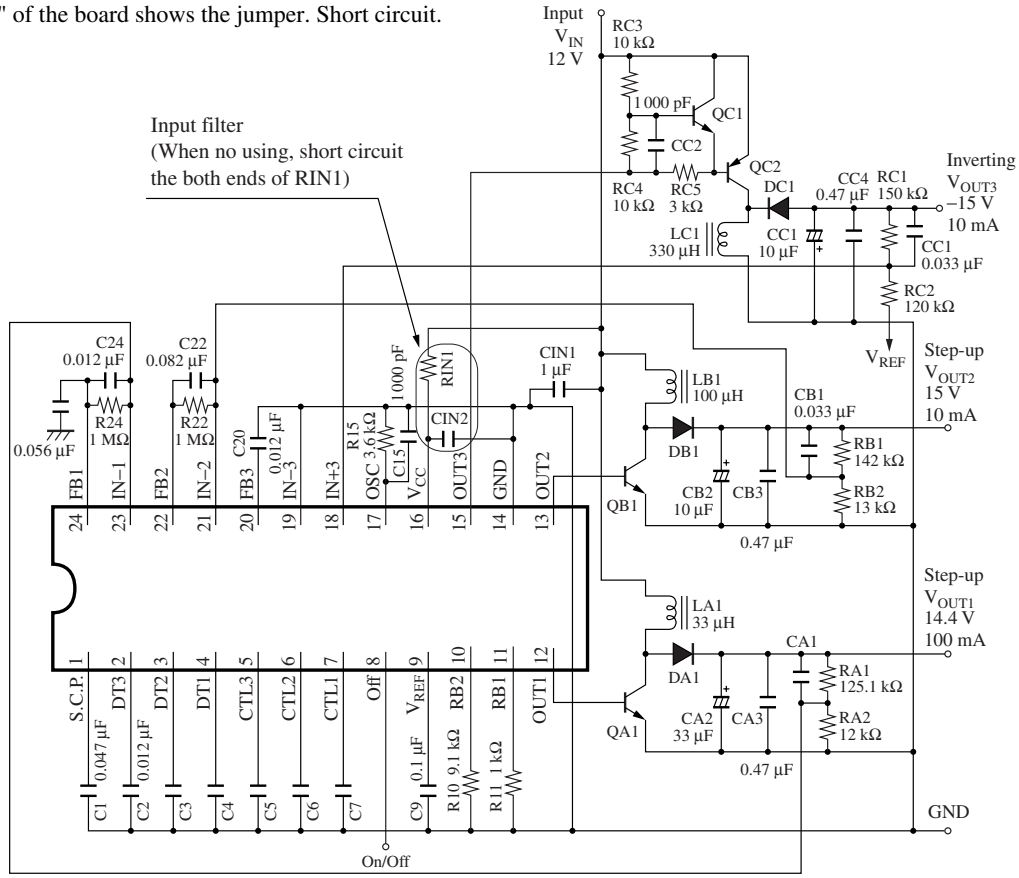
■ Application Circuit Example



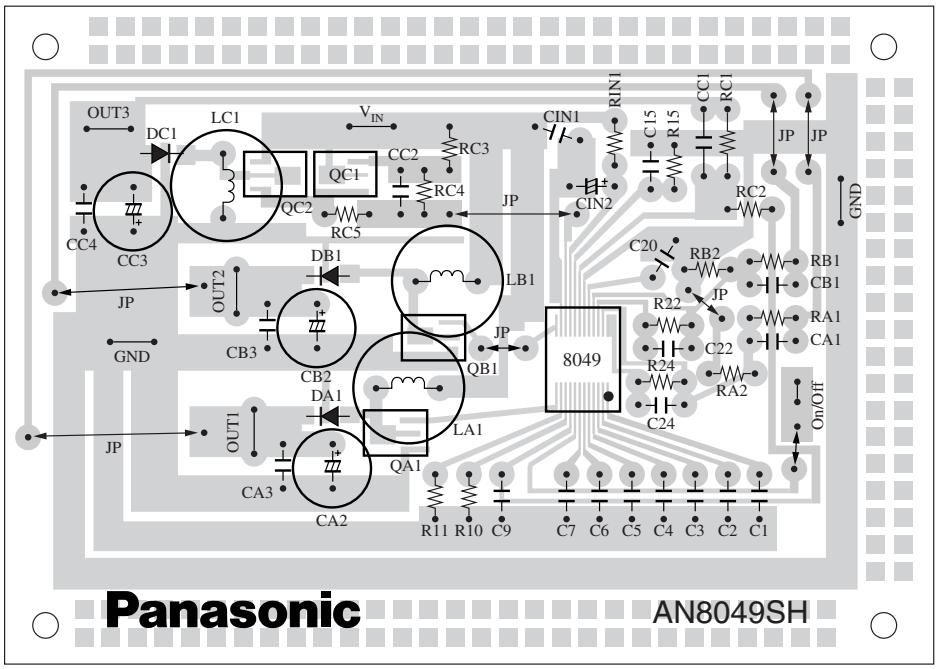
■ Evaluation Board

1. The element numbers of the board pair with the ones of the circuit.
2. "JP" of the board shows the jumper. Short circuit.

• Circuit

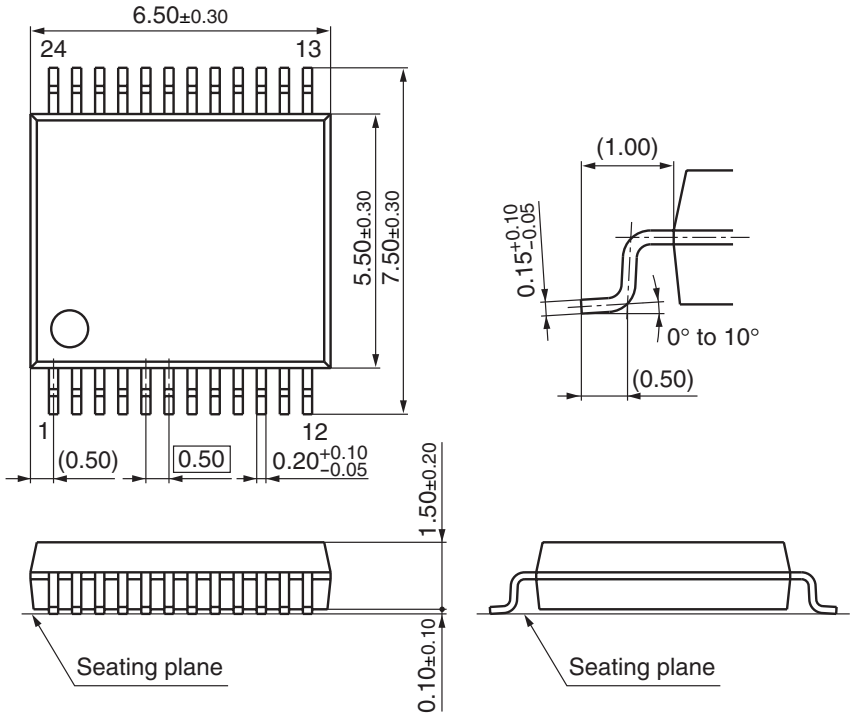


• Board



■ New Package Dimensions (Unit: mm)

• SSOP024-P-0300D (Lead-free package)



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