DATA SHEET

NEC

MOS INTEGRATED CIRCUIT

μPD75206

4-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD75206 is a microcomputer with a CPU capable of 1-, 4-, and 8-bit-wise data processing, a ROM, a RAM, I/O ports, a fluorescent display tube controller/driver, a watch timer, a timer/pulse generator capable of outputting 14-bit PWM, a serial interface and a vectored interrupt function integrated on a single-chip.

It uses the VCR, ECR and CD fluorescent display tubes as display devices and is most suitable for applications requiring the timer/watch function and high-speed interrupt servicing. It can help to provide the unit with many functions and to decrease performance costs.

With the μPD75206, the μPD75P216A, 75P218 one-time PROM products are available for system development evaluation or small production. ★

Detailed functions, etc. are described in the following user's manual. Be sure to read the manual for designing.

μPD75216A User's Manual: IEM-988

FEATURES

- Architecture equal to that of an 8-bit microcomputer
- High-speed operation : Minimum instruction execution time : 0.95 μs (when operated at 4.19 MHz)
- Instruction execution time variable function realizing a wide range of operating voltages
- On-chip large-capacity program memory : 6K bytes
- Watch operation with an ultra low current consumption : 5μA TYP. (at the 3 V operation)
- On-chip programmable fluorescent display tube controller/driver
- Timer function : 4 ch
  - 14-bit PWM output capability with the voltage synthesizer type electronic tuner
  - Buzzer output capability
- Interrupt function with importance attached to applications
  - For power-off detection
  - For remote controlled reception
- Product with an on-chip PROM : μPD75P216A, μPD75P218 (on-chip EPROM : WQFN package) ★

ORDERING INFORMATION ★

Ordering Code	Package	Quality Grade
μPD75206CW-xxx	64-pin plastic shrink DIP (750 mil)	Standard
μPD75206GF-xxx-3BE	64-pin plastic QFP (14 x 20 mm)	Standard

Please refer to "Quality grade on NEC Semiconductor Devices" (Document number IEI-1209) published by NEC Corporation to know the specification of quality grade on the devices and its recommended applications.

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(O. D. No. IC-6969C)
Date Published August 1993 P
Printed in Japan

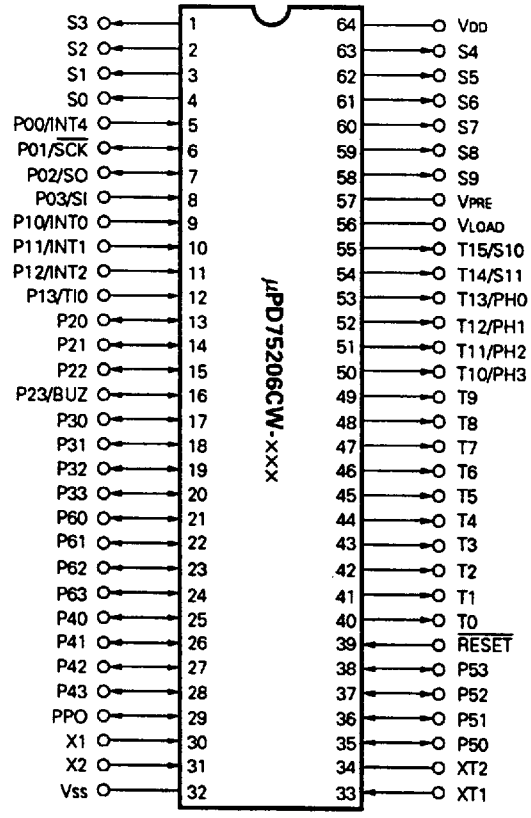
The mark ★ shows major revised points.

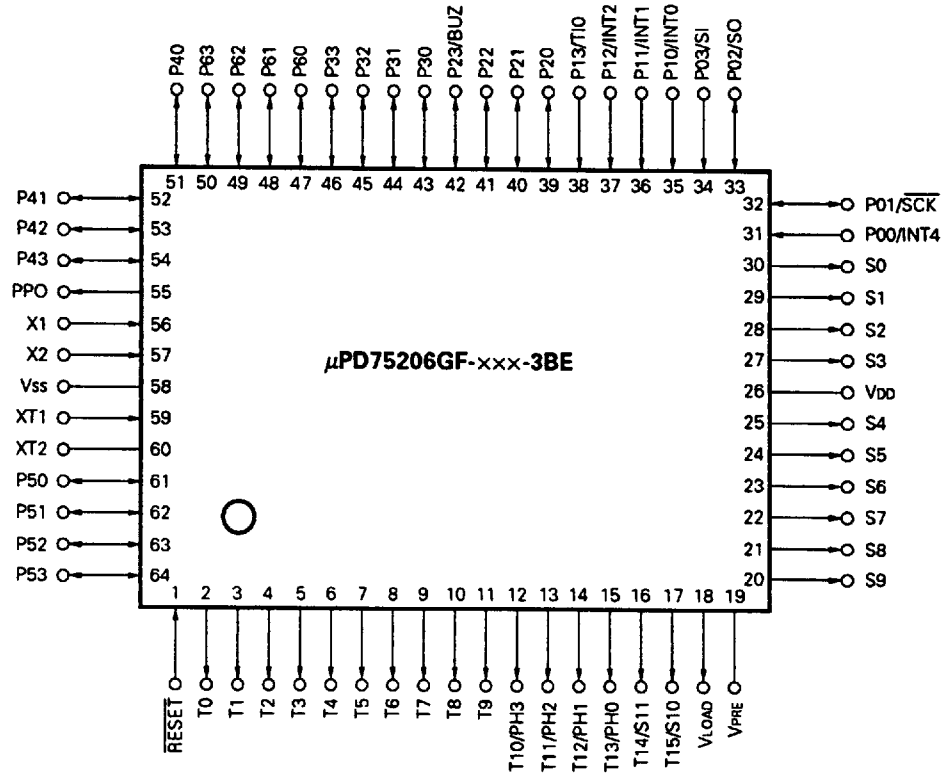
★ LIST OF FUNCTIONS

Item		Function			
Instruction execution time		• 0.95, 1.91, 15.3 μs (Main system clock : 4.19 MHz operation) • 122 μs (Subsystem clock : 32.768 kHz operation)			
On-chip memory	ROM	6016 × 8 bits			
	RAM	369 × 4 bits			
General register		• 4-bit manipulation : 8 × 4 banks • 8-bit manipulation : 4 × 4 banks			
Input/output port (FIP® dual-function pin included FIP dedicated pin excluded)		33	8	CMOS input pin	
			20	CMOS input/output pins	• Direct LED drive capability : 8 • On-chip pull-down resistor by mask option capability : 4
			5	CMOS output pin	• Direct LED drive capability : 4 • PWM/pulse output : 1 • On-chip pull-down resistor by mask option capability : 4
FIP controller/driver		• No. of segments : 9 to 12 segments • No. of digits : 9 to 16 digits • Dimmer function : 8 levels • On-chip pull-down resistor by mask option capability • Key scan interrupt generation			
Timer		4 channels	• Timer/pulse generator : 14-bit PWM output enabled • Watch timer : Buzzer output enabled • Timer/event counter • Basic interval timer : Watchdog timer application capability		
Serial interface		• MSB start/LSB start switchable • Serial bus configuration capability			
Vectored interrupt		External : 3, Internal : 5			
Test input		External : 1, Internal : 1			
System clock oscillator		• Ceramic/crystal oscillator for main system clock oscillation : 4.194304 MHz standard • Crystal oscillator for subsystem clock oscillation : 32.768 kHz standard			
Standby function		STOP/HALT mode			
Mask option		• Power-on reset, power-on flag • High withstand voltage port : Pull-down resistor or open-drain output • Port 6 : Pull-down resistor			
Operating temperature range		–40 to +85 °C			
Operating voltage		2.7 to 6.0 V (standby data hold : 2.0 to 6.0 V)			
Package		• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm)			

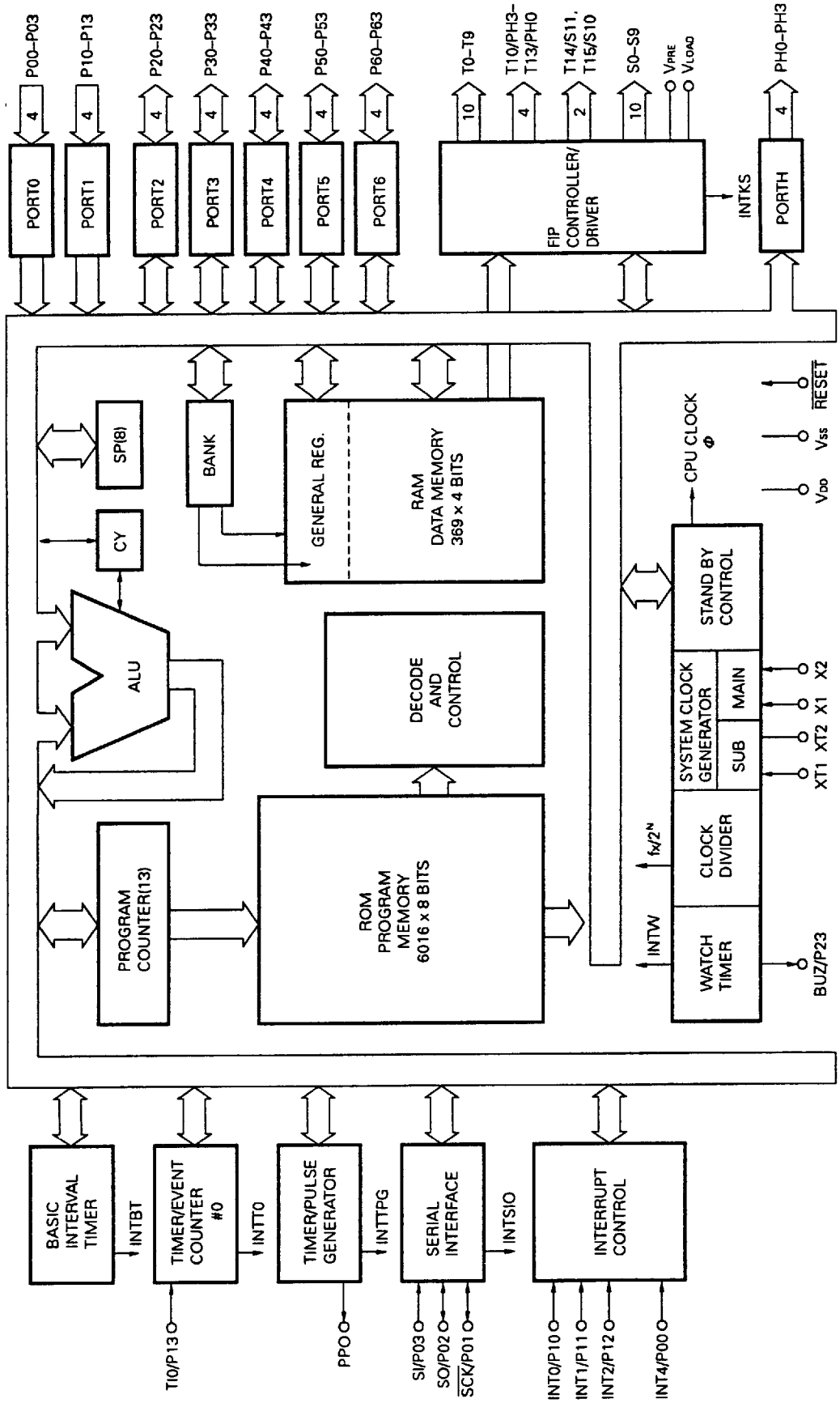
CONTENTS

1. PIN CONFIGURATION (TOP VIEW)





2. BLOCK DIAGRAM



3. PIN FUNCTIONS

3.1 PORT PINS

Pin Name	I/O	Dual-Function Pin	Function	8-Bit I/O	After Reset	Input / Output Circuit Type *1
P00	Input	INT4	4-bit input port (PORT0).	×	Input	Ⓑ
P01	Input/output	$\overline{SCK}$				Ⓕ
P02	Input/output	SO				Ⓖ
P03	Input	SI				Ⓑ
P10	Input	INT0	Noise removing function available		Input	Ⓑ
P11		INT1	Noise removing function available			
P12		INT2	4-bit input port (PORT1).			
P13		TI0				
P20	Input/output	—	4-bit input/output port (PORT2).	×	Input	E
P21		—				
P22		—				
P23		BUZ				
P30–P33	Input/output	—	Programmable 4-bit input/ output port (PORT3). Input/output specifiable in 1-bit units.		Input	E
P40 to P43	Input/output	—	4-bit input/output port (PORT4). LED direct drive capability.	○	Input	E
P50 to P53	Input/output	—	4-bit input/output port (PORT5). LED direct drive capability.		Input	E
P60 to P63	Input/output	—	Programmable 4-bit input/output port (PORT6). Input/output specifiable in 1-bit units. On-chip pull-down resistor available (mask option). Suitable for key input.	×	Input	V
PH0	Output	T13	4-bit P-ch open-drain, high-dielectric, high-current output port (PORTH). LED direct drive capability. On-chip pull-down resistor available (mask option).	×	Low level (with an on-chip pull-down resistor) or high impedance.	I
PH1		T12				
PH2		T11				
PH3		T10				

* Schmitt trigger inputs are circled.

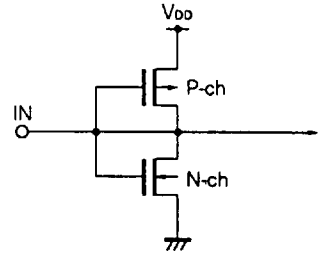
3.2 NON-PORT PINS

Pin Name	I/O	Dual-Function Pin	Function		After Reset	Input / Output Circuit Type *
T0 to T9	Output	—	FIP controller/driver output pins. Pull-down resistor can be incorporated in bit units (mask option).	Digit output high-voltage high-current output.	Low level (With an on-chip pull-down resistor) or high impedance (without a pull-down resistor)	I
T10 to T13		PH3 to PH0		Digit/segment output dual-function high-voltage high-current output. Extra pins can be used as PORTH.		
T14/S11, T15/S10		—		Digit/segment output dual-function high-voltage high-current output. Static output also possible.		
S9				Segment output high voltage output. Static output also possible.		
S0 to S8				Segment high-voltage output.		
PPO	Output	—	Timer/pulse generator pulse output.		High impedance	D
TI0	Input	P13	External event pulse input for timer/event counter.			Ⓑ
$\overline{SCK}$	Input/output	P01	Serial clock input/output.		Input	Ⓕ
SO	Input/output	P02	Serial data input pin or serial data input/output.		Input	Ⓖ
SI	Input	P03	Serial data input or normal input.		Input	Ⓑ
INT4	Input	P00	Edge-detected vectored interrupt input (rising and falling edge detection).			Ⓑ
INT0	Input	P10	Edge-detected vectored interrupt input with noise eliminate function (detection edge selection possible).			Ⓑ
INT1		P11				
INT2	Input	P12	Edge-detected testable input (rising edge detection).			Ⓑ
BUZ	Input/output	P23	Fixed frequency output (for buzzer or system clock trimming).		Input	E
X1, X2	Input	—	Crystal/ceramic connect pin for main system clock oscillation. External clock input to X1 and its inverted clock input to X2.			
XT1	Input	—	Crystal connect pin for subsystem clock oscillation. External clock input to XT1 and XT2 open.			
XT2	—					
$\overline{RESET}$	Input		System reset input (low level active).			Ⓑ
V_{PRE}		—	FIP controller/driver output buffer power supply.			I
V_{LOAD}		—	FIP controller/driver pull-down resistor connect pin.			I
V_{DD}		—	Positive power supply.			
V_{SS}		—	GND potential.			

* Schmitt trigger inputs are circled.

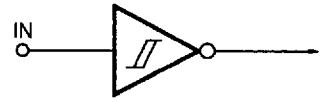
3.3 PIN INPUT/OUTPUT CIRCUIT LIST

TYPE A



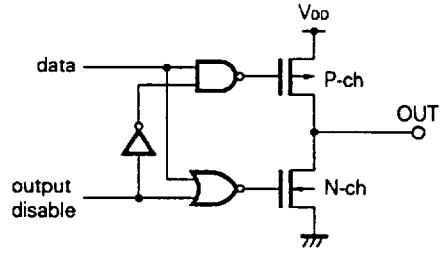
CMOS-Specified Input Buffer

TYPE B



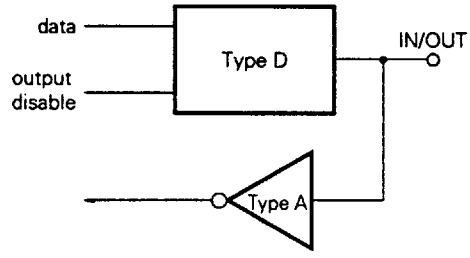
Schmitt Trigger Input Having Hysteresis Characteristics

TYPE D



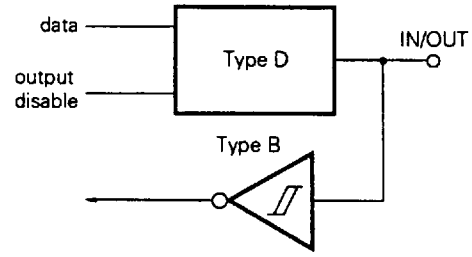
Push-Pull Output which can be Set to Output High Impedance (with Both P-ch and N-ch Set to OFF)

TYPE E



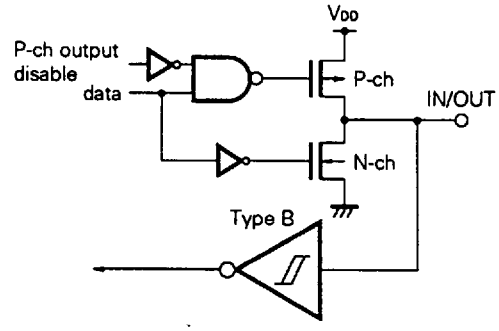
Input/Output Circuit Consisting of Type D Push-Pull Output and Type A Input Buffer

TYPE F



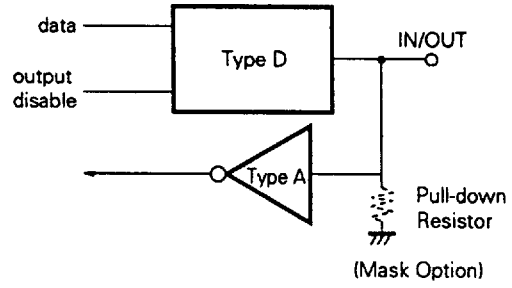
Input/Output Circuit Consisting of Type D Push-Pull Output and Type B Schmitt Trigger Input

TYPE G



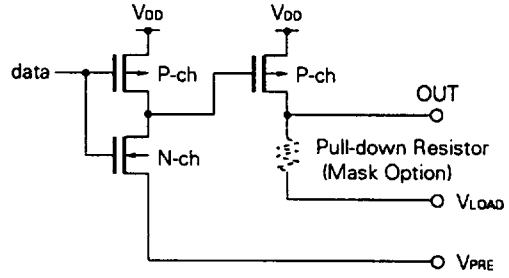
Input/Output Circuit Capable of Switching between Push-Pull Output and N-ch Open-Drain Output (with P-ch OFF).

TYPE V



(Mask Option)

TYPE I



3.4 UNUSED PINS TREATMENT

Pin	Recommended Connection
P00/INT4	Connect to V_{SS}
P01/$\overline{SCK}$	Connect to V_{SS} or V_{DD}
P02/SO	
P03/SI	
P10/INT0 to P12/INT2	Connect to V_{SS}
P13/TI0	
P20 to P22	Input state : Connect to V_{SS} or V_{DD}
P23/BUZ	Ouput state : Leave open
P30 to P33	
P40 to P43	
P50 to P53	
P60 to P63	
PPO	Leave open
S0 to S9	
T15/S10 to T14/S11	
T0 to T9	
T10/PH3 to T13/PH0	
XT1	Connect to V_{SS} or V_{DD}
XT2	Leave open
$\overline{RESET}$ when there is an on-chip power-on reset circuit	Connect to V_{DD}
V_{LOAD} when there is no on-chip load resistor	Connect to V_{SS} or V_{DD}

3.5 P00/INT4 PIN AND $\overline{\text{RESET}}$ PIN OPERATING PRECAUTIONS

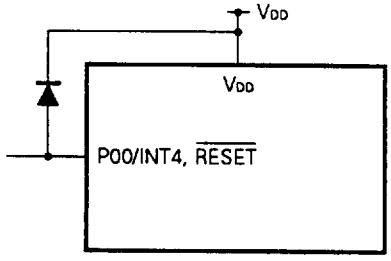
P00/INT4 and $\overline{\text{RESET}}$ pins have the function (especially for IC test) to test μPD75206 internal operations in addition to the functions described in sections 3.1 and 3.2.

The test mode is set when a voltage larger than V_{DD} is applied to one of these pins. If noise larger than V_{DD} is applied in normal operation, the test mode may be set thereby adversely affecting normal operation.

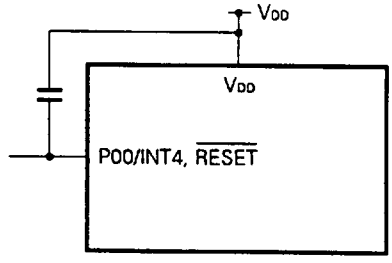
Since there is a display output pin having a high-voltage amplitude (35 V) next to the P00/INT4 and $\overline{\text{RESET}}$ pins, if cables for the related signals are routed in parallel, wiring noise larger than V_{DD} may be applied to the P00/INT4 and $\overline{\text{RESET}}$ pins causing errors.

Thus, carry out wiring so that wiring noise can be minimized, If noise still cannot be suppressed, take the measure against noise using the following external components.

- **Connect diode with small V_F (0.3 V or less) between V_{DD} and P00/INT4.$\overline{\text{RESET}}$**



- **Connect a capacitor between the pins and V_{DD}.**

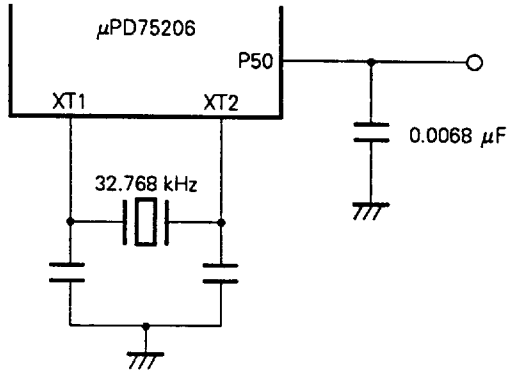


3.6 XT1, XT2 AND P50 PIN OPERATING PRECAUTIONS

When selecting the 32.768 kHz subsystem clock connected to the XT1 and XT2 pins as the watch timer source clock, the signal to be input or output to the P50 pin next to the XT2 pin must be a signal required to be switched between high and low the minimum number of times (once/second or less).

If the P50 pin signal is switched frequently between high and low, a spike is generated in the XT2 pin because of capacitance coupling of the P50 and XT2 pins and the correct watch functions cannot be achieved (the watch becomes fast).

If it is necessary to allow the P50 pin signal to switch between high and low, mount an external capacitor to the P50 pin as shown below.



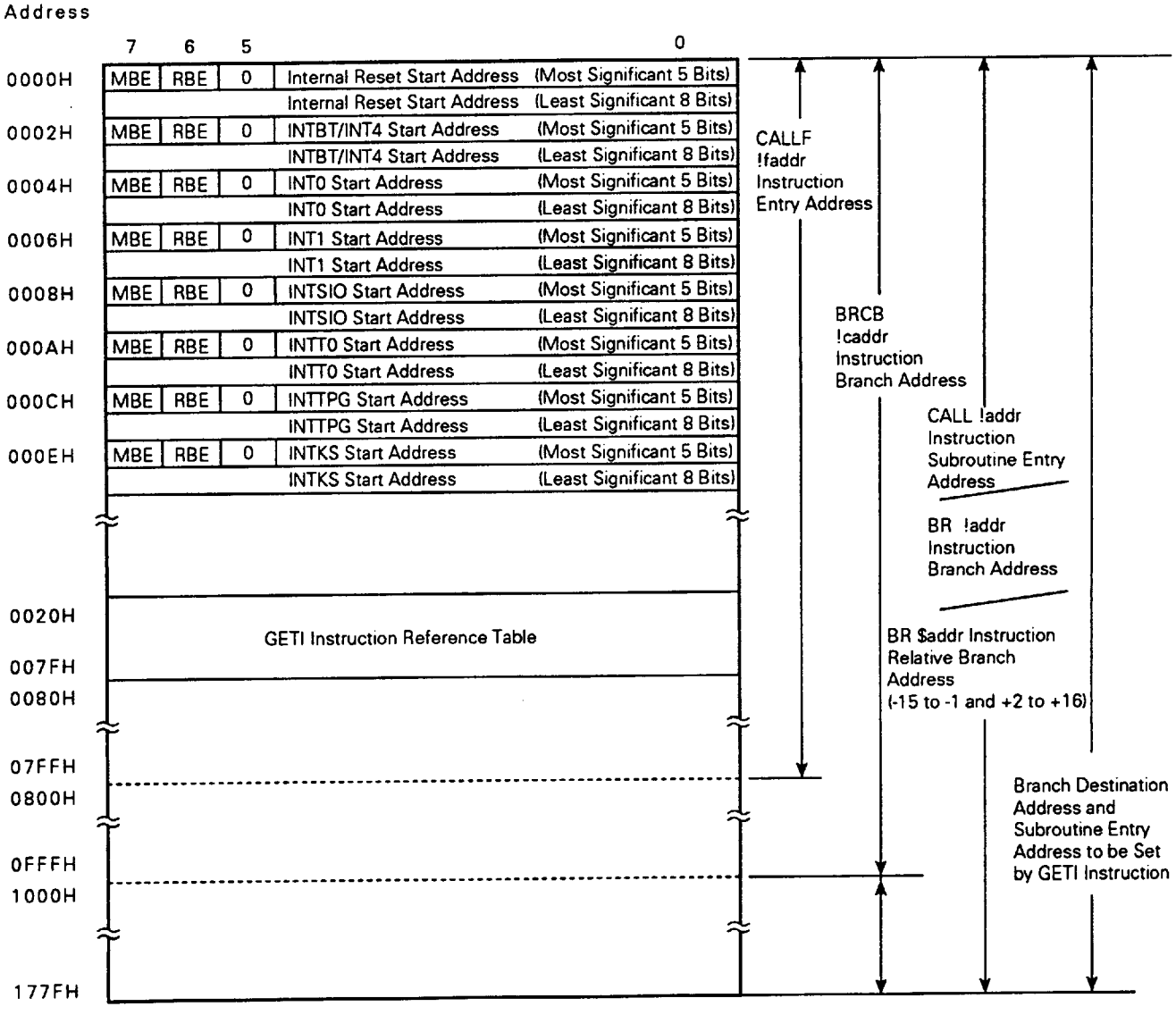
4. μPD75206 ARCHITECTURE AND MEMORY MAP

The μPD75206 has the following three architectural features.

- Data memory bank configuration: Static RAM (320 words x 4 bits)
  Display data memory (49 words x 4 bits)
  Peripheral hardware (128 x 4 bits)
- General register bank configuration: 8 x 4 banks (Operated in 4 bits)
  4 x 4 banks (Operated in 8 bits)
- Memory mapped I/O

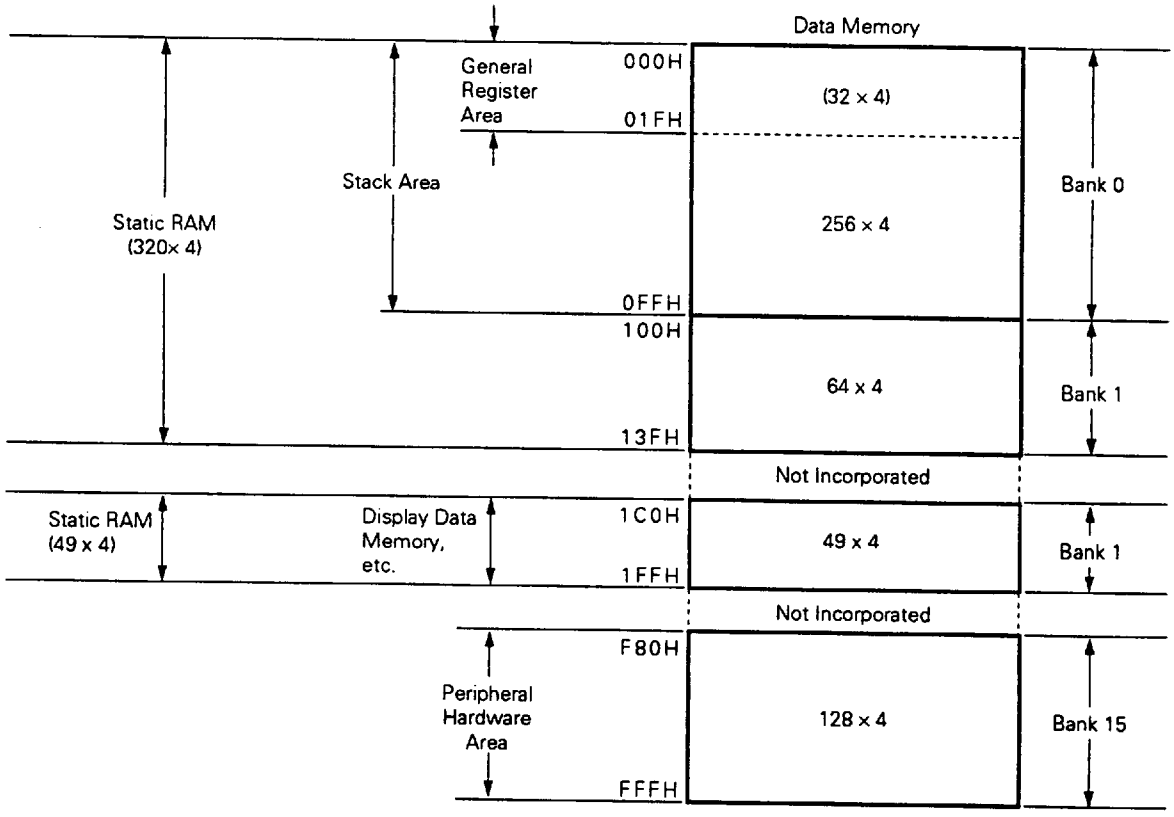
Figures 4-1, 4-2 shows memory maps of μPD75206.

Fig. 4-1 Program Memory Map



Remarks In all cases other than those listed above, branch to the address with only the lower 8 bits of the PC changed is enabled by BR PCDE and BR PCXA instructions.

Fig. 4-2 Data Memory Map



5. PERIPHERAL HARDWARE FUNCTIONS

5.1 PORTS

The following three types of I/O ports are provided:

- CMOS input : 8
- CMOS I/O : 20
- P-ch open-drain, high-voltage, high-current output : 4

Total : 32

Table 5-1 Port Function

Port name	Function	Operation, feature	Remarks:
PORT0	4-bit input	Can always be read or tested regardless of operation mode of multiplexed pin.	Multiplexed with SI, SO, $\overline{SCK}$, and INT4 pins.
PORT1		Can always be read or tested. P10 and P11 are provided with noise rejection function.	Multiplexed witn INT0-2 and TI0 pins.
PORT2 PORT4 PORT5	4-bit I/O	Can be set in input or output mode in 4-bit units. Ports 4 and 5 can be usd in pairs to input/output 8-bit data. Ports 4 and 5 can directly drive LED.	P23 is multiplexed witn BUZ pin.
PORT3 PORT6		Can be set in input or output mode in 1-bit units. Port 6 can be connected to internal pull-down resistor by the mask option.	
PORTH	4-bit output	P-ch open-drain, high-voltage, high-current output port. Can directly drive FIP and LED. Can be connected to internal pull-down resistor in 1-bit units by the mask option.	Multiplexed with T10-T13 pins.

5.2 CLOCK GENERATOR CIRCUIT

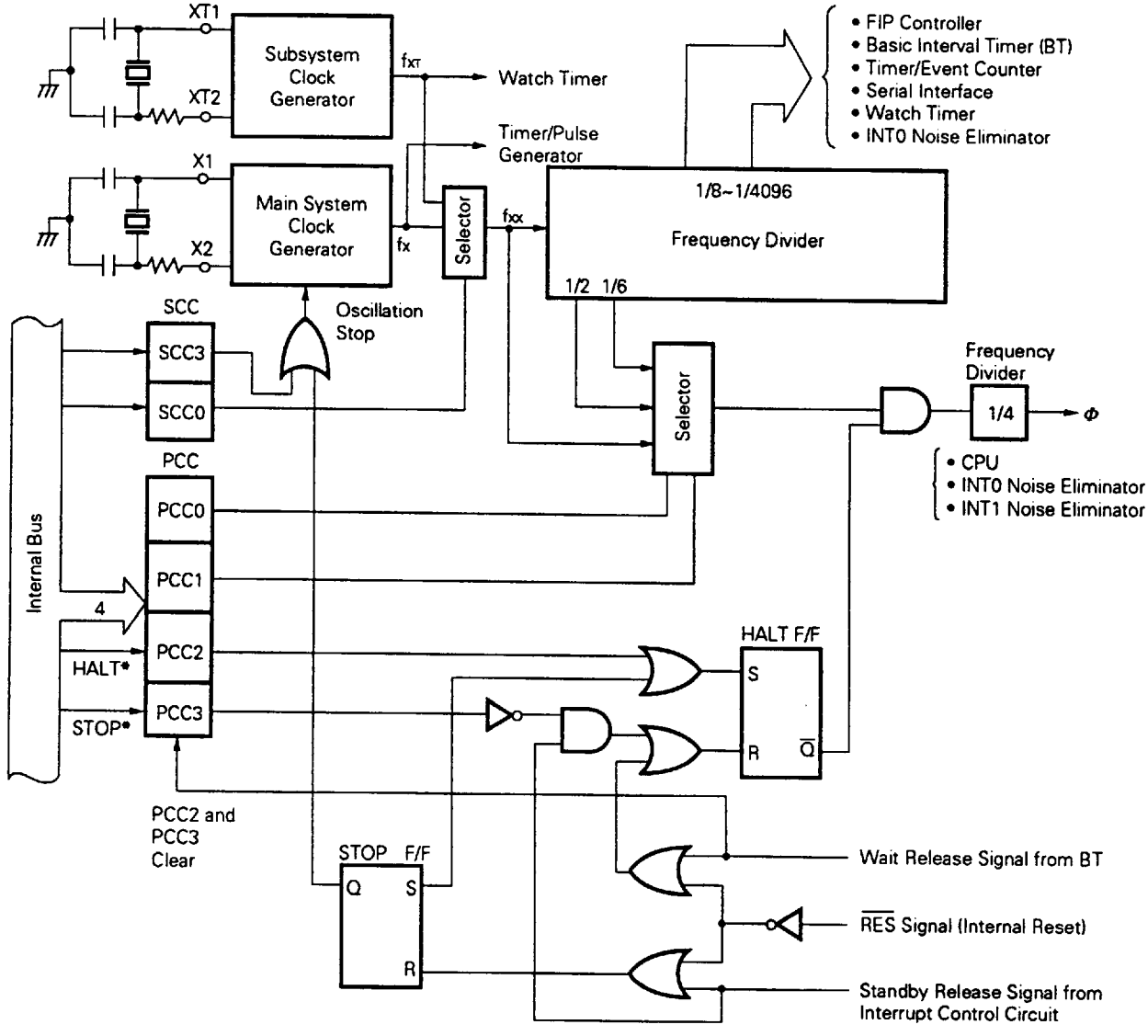
The operation of the clock generator circuit is determined by the processor clock control register (PPC) and system clock control register (SCC).

This circuit can generate two types of clocks: main system clock and subsystem clock.

In addition, it can also change the instruction execution time.

- 0.95 μs, 1.91 μs, 15.3 μs (main system clock: 4.19 MHz)
- 122 μs (subsystem clock: 32.768 kHz)

Fig. 5-1 Clock Generator Block Diagram



* Instruction execution

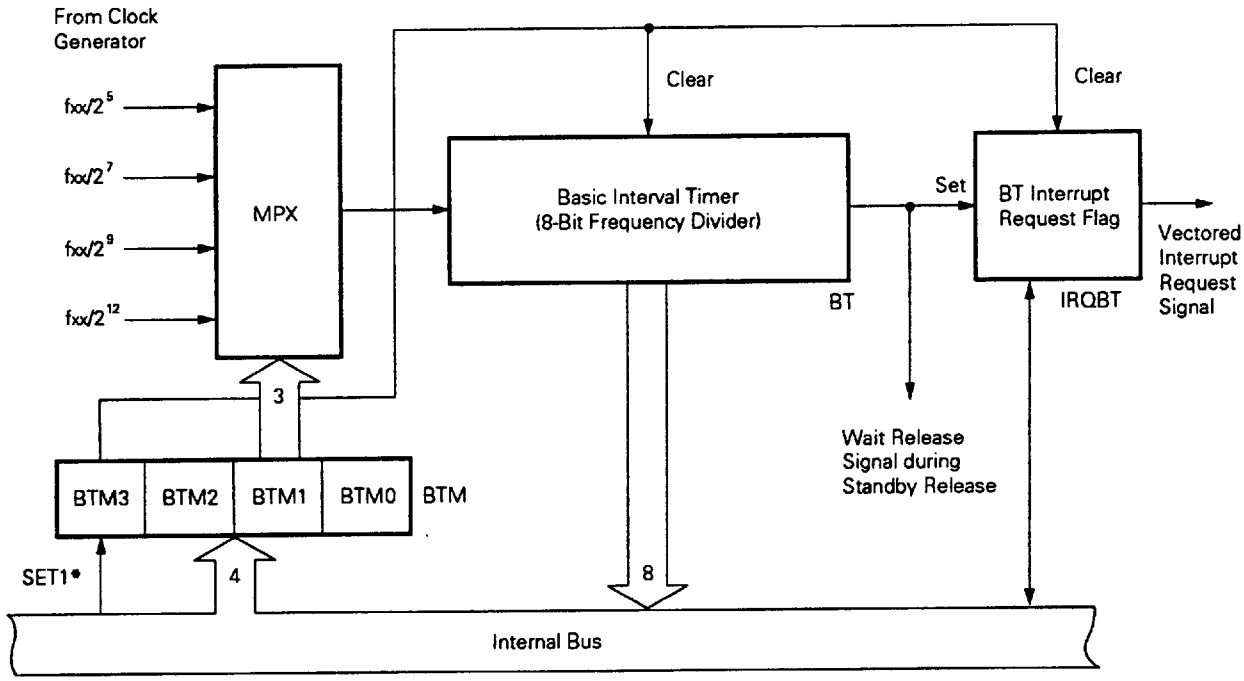
Remarks
1. fx = Main system clock frequency
2. fXT = Subsystem clock frequency
3. fxx = System clock frequency
4. Φ = CPU clock
5. PCC: Processor clock control register
6. SCC: System clock control register
7. 1 clock cycle (tCY) of Φ is 1 machine cycle of an instruction. For tCY, see "AC Characteristics" in **12. ELECTRICAL SPECIFICATIONS.** ★

5.3 BASIC INTERVAL TIMER

The basic interval timer has the following functions:

- Interval timer operation to generate reference time
- Watchdog timer application to detect inadvertent program loop
- Wait time select and count upon standby mode release
- Count contents read

Fig. 5-2 Basic Interval Timer Configuration



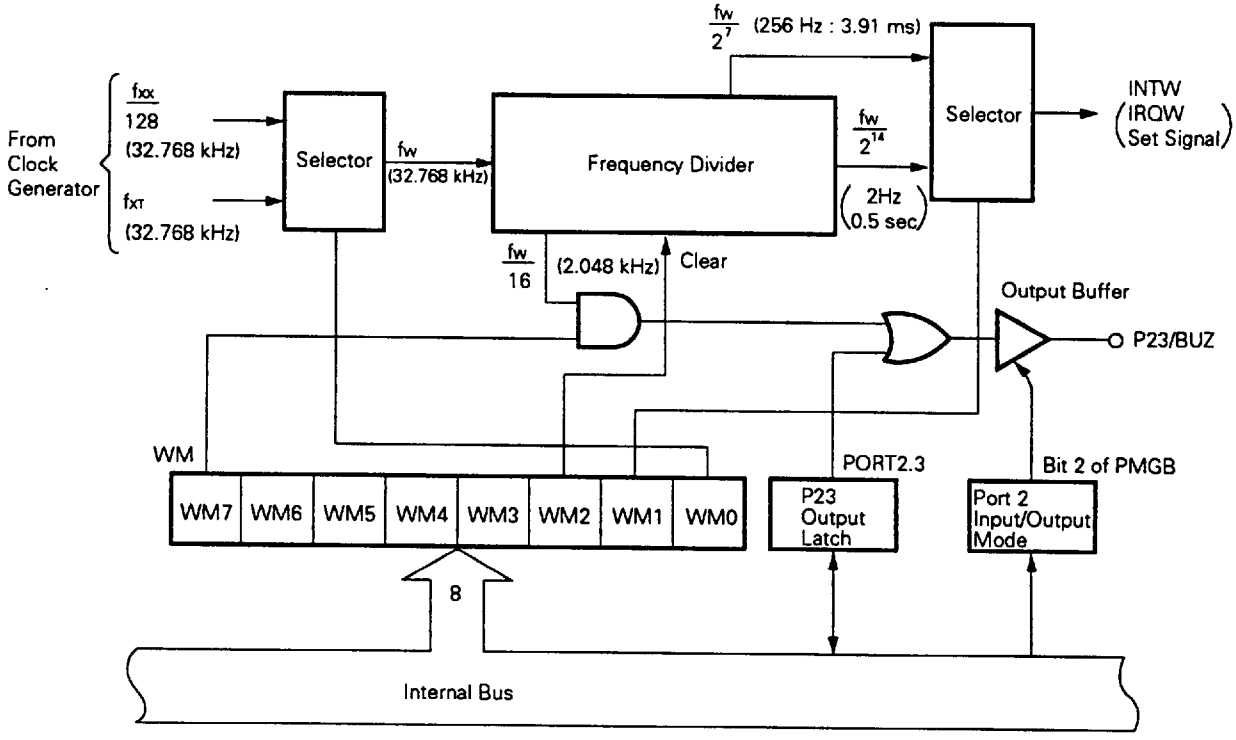
* Instruction execution

5.4 WATCH TIMER

The μPD75206 incorporates one channel of watch timer. The watch timer has the following functions.

- Sets the test flag (IRQW) at 0.5 sec intervals.
  The standby mode can be released by IRQW.
- 0.5 second interval can be set with the main system clock and subsystem clock.
- The fast mode enables to set 128-time (3.91 ms) interval useful to program debugging and inspection.
- The fixed frequencies (2.048 kHz) can be output to the P23/BUZ pin for use to generate buzzer sound and trim the system clock oscillator frequency.
- Since the frequency divider can be cleared, the watch can be started from zero second.

Fig. 5-3 Watch Timer Block Diagram



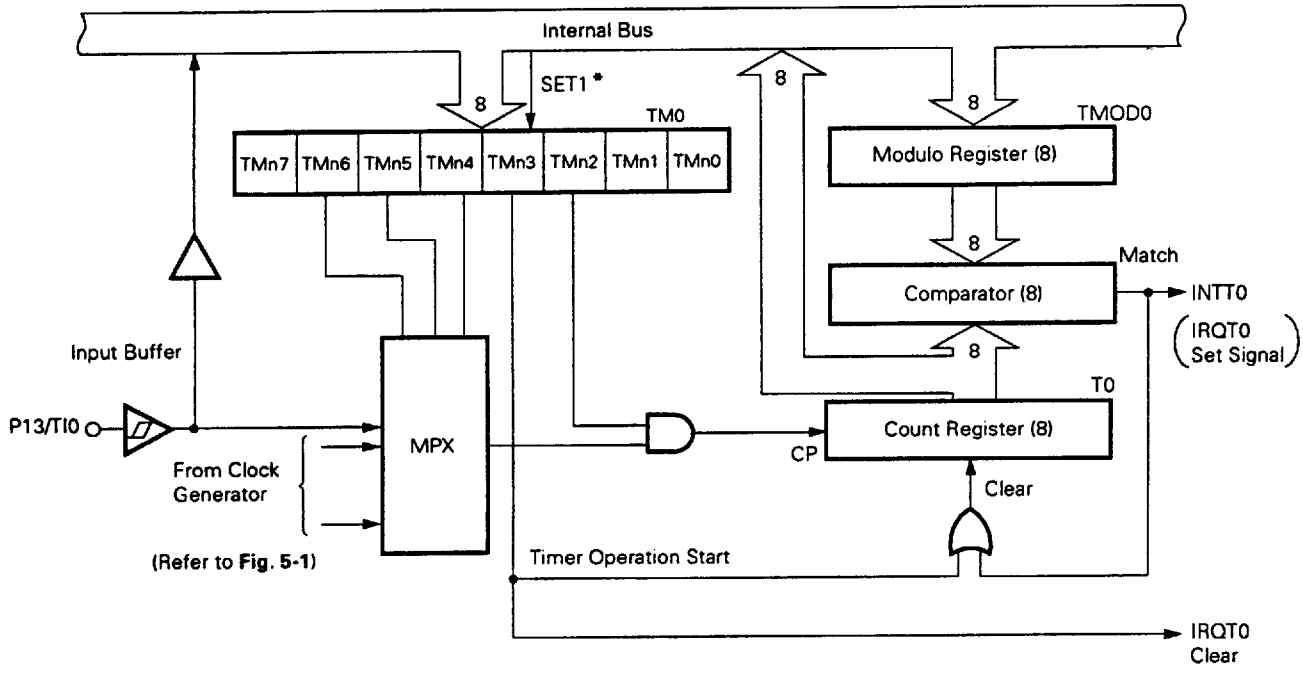
Remarks Values at fxx = 4.194304 MHz and fxT = 32.768 kHz are indicated in parentheses.

5.5 TIMER/EVENT COUNTER

The μPD75206 incorporates one channel of timer/event counter. The timer/event counter has the following functions.

- Program interval timer operation
- Event counter operation
- Count state read function

Fig. 5-4 Timer/Event Counter Block Diagram



* Instruction execution.

5.6 TIMER/PULSE GENERATOR

The μPD75206 incorporates one channel of timer/pulse generator which can be used as a timer or a pulse generator. The timer/pulse generator has the following functions.

(a) Functions available in the timer mode

- 8-bit interval timer operation (IRQTPG generation) enabling the clock source to be varied at 5 levels
- Square wave output to PPO pin

(b) Functions available in the PWM pulse generate mode

- 14-bit accuracy PWM pulse output to the PPO pin (Used as a digital-to-analog converter and applicable to tuning)
- Fixed time interval ($\frac{2^{15}}{fxx}$ = 7.81 ms : at 4.19 MHz operation) interrupt generation

If pulse output is not necessary, the PPO pin can be used as a 1-bit output port.

Note **If the STOP mode is set while the timer/pulse generator is in operation, miss-operation may result. To prevent that from occurring, preset the timer/pulse generator to the stop state using its mode register.**

Fig. 5-5 Block Diagram of Timer/Pulse Generator (Timer Mode)

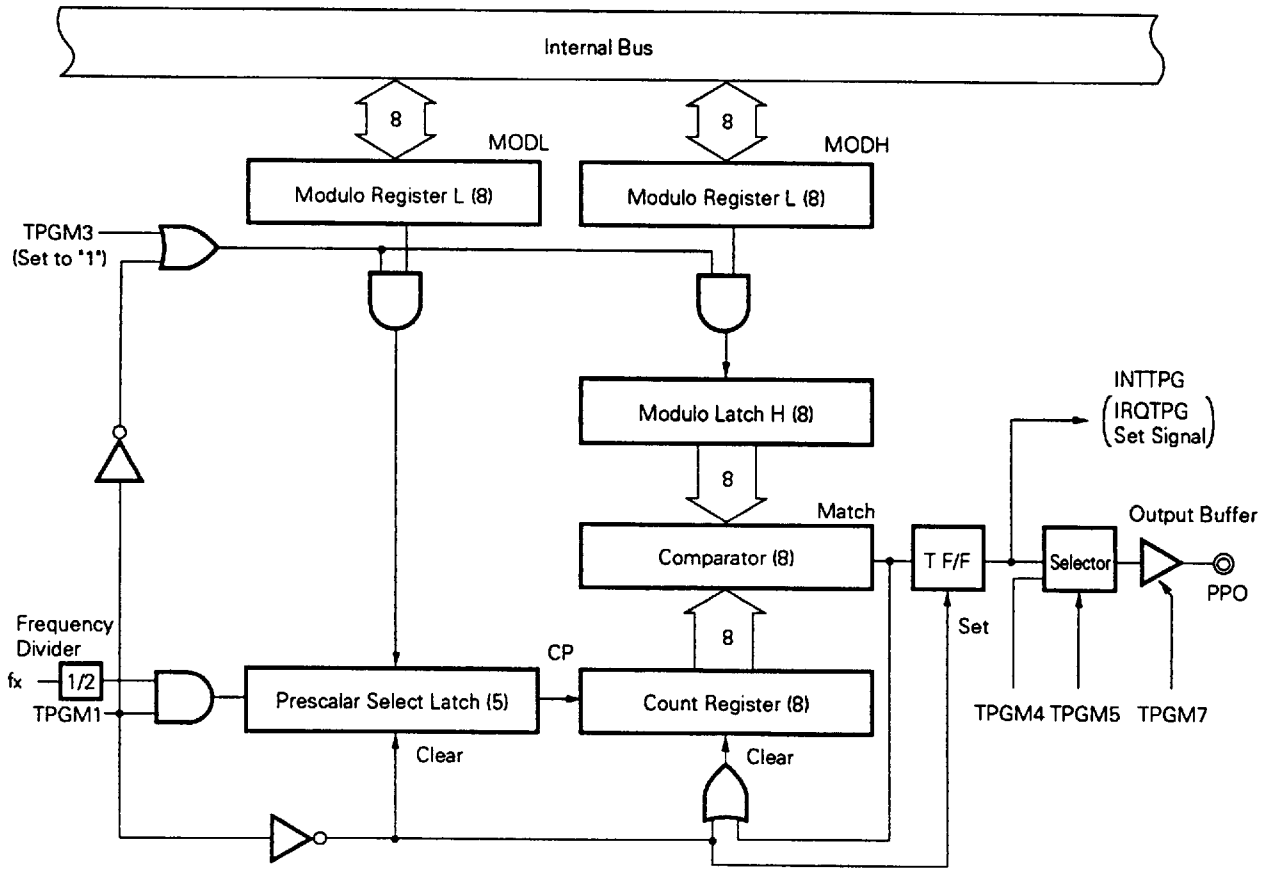
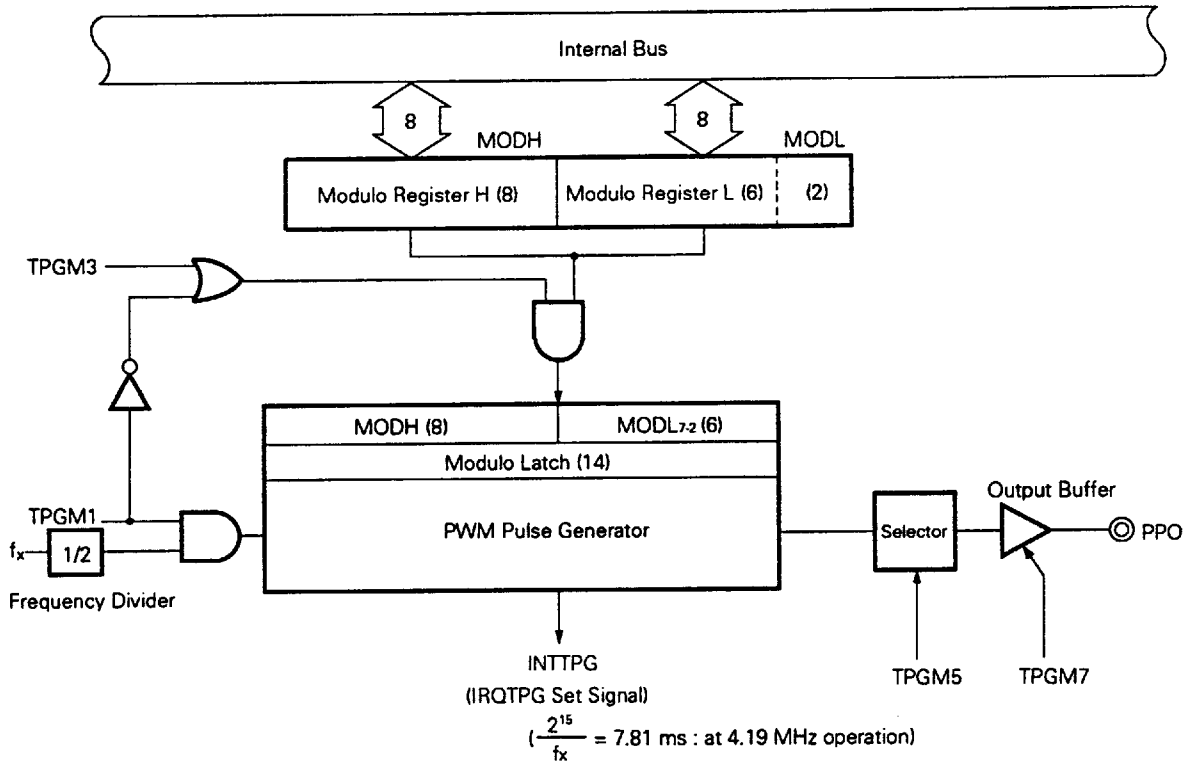


Fig. 5-6 Timer/Pulse Generator Block Diagram (PWM Pulse Generate Mode)



5.7 SERIAL INTERFACE

The serial interface has the following functions:

- Clocked 8-bit transmission/reception operation (synchronous transmission/reception)
- Clocked 8-bit serial bus operation (inputs/outputs data via SO pin. SO output is of N-ch open-drain.)
- LSB first/MSB first selectable

These features allows the serial interface to communicate data with the serial bus of the other microcomputers such as μPD7500 series and 78K series and to be connected with peripheral devices.

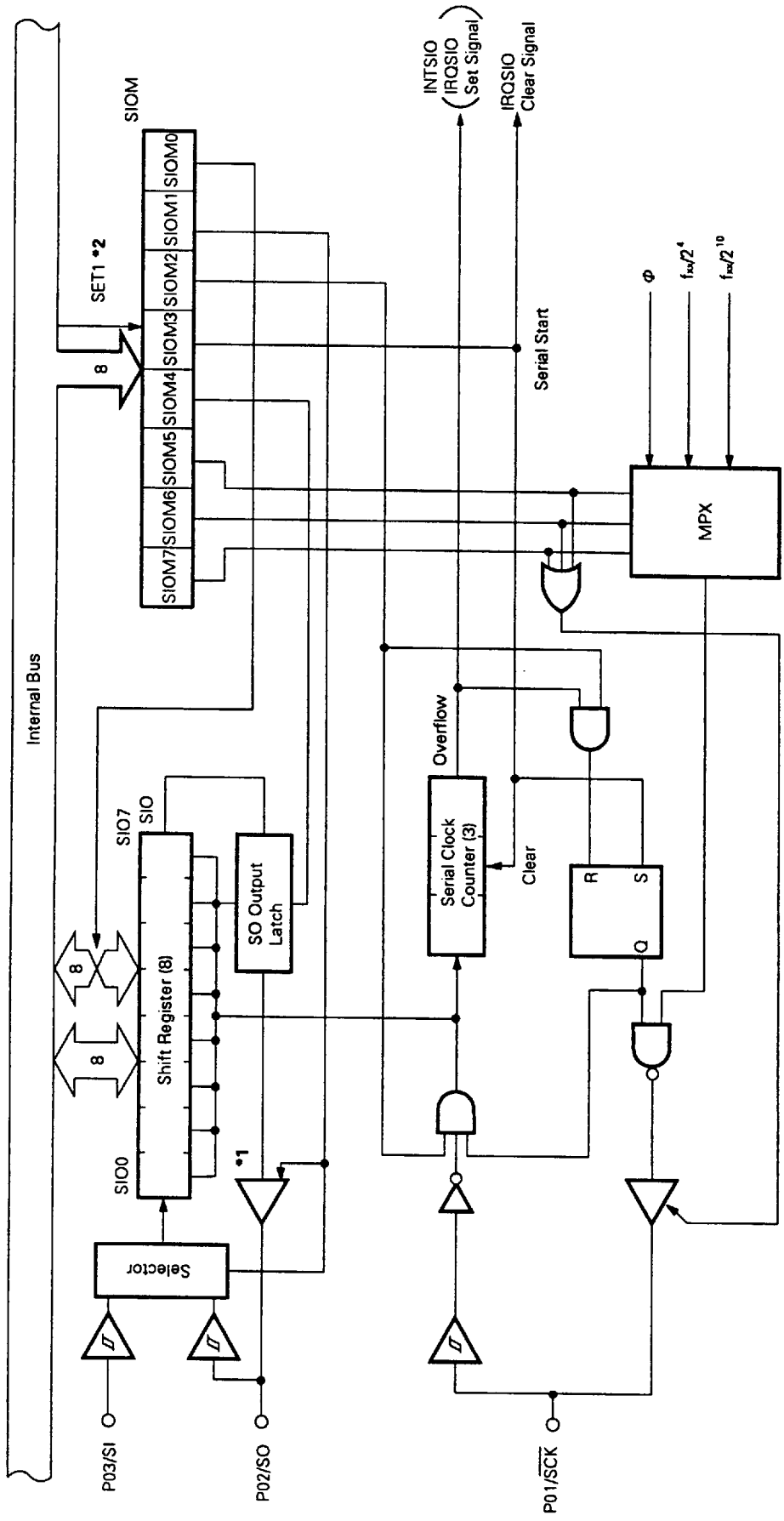


Fig 5-7 Serial Interface Block Diagram

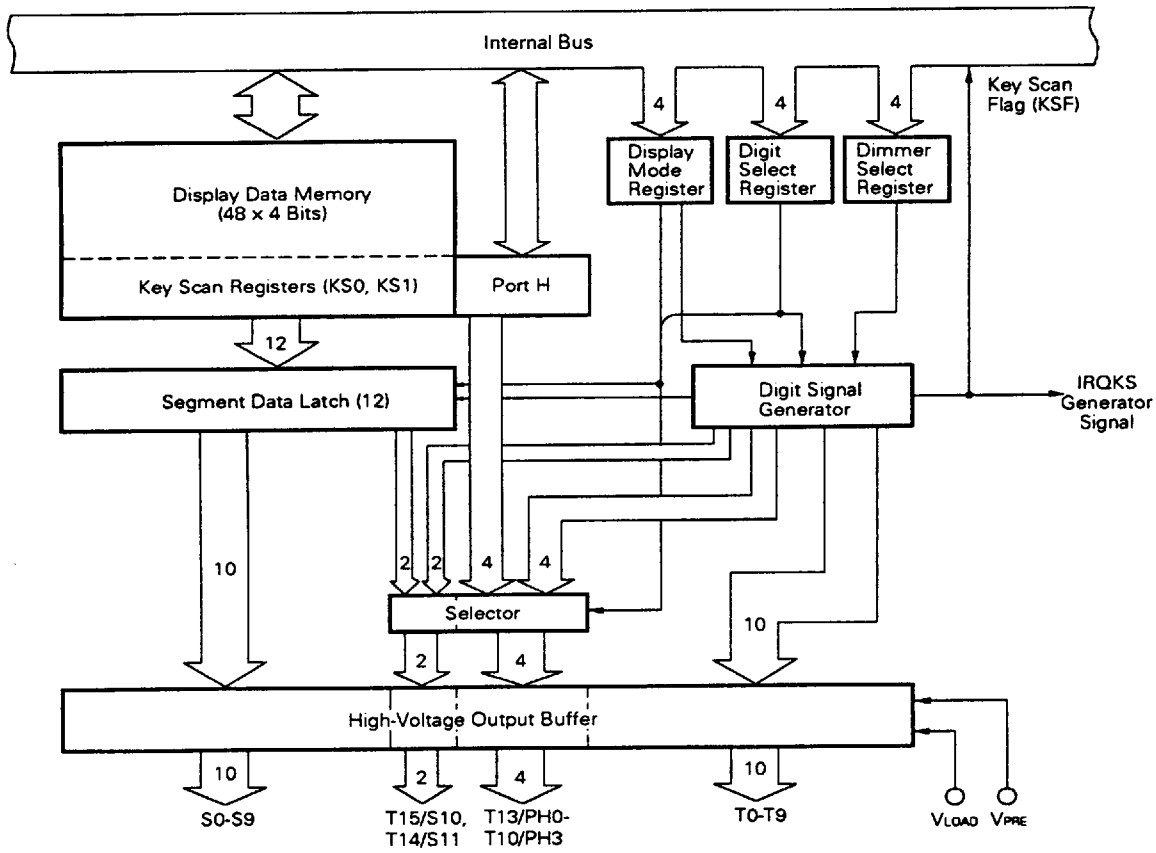
* 1. CMOS output and N-ch open drain output switchable output buffer.
2. Instruction execution

5.8 FIP CONTROLLER/DRIVER

The FIP controller/driver of the μPD75206 has the following functions:

- Automatically read display data memory by means of DMA, and generate segment signals and digit signals.
- Number of display elements can be freely selected in a range of 9 to 12 segments and 9 to 16 digits, and a total of 26 segments/digits or less.
- Unused display outputs can be used as static outputs.
- Luminosity can be adjusted in eight steps by a dimmer function.
- Can be used for key scan.
  - Interrupt (IRQKS) occurs when a specified key is scanned.
  - Key scan data can be output from a segment output pin.
- High-voltage output pins that can directly drive FIP (40 V).
  - Sement pins (S0-S9): V_{OD} = 40 V, I_{OD} = 3mA
  - Digit output pins (T0-T15): V_{OD} = 40 V, I_{OD} = 15 mA
- Can be connected to pull-down resistor in bit units by mask option.

Fig. 5-8 FIP Controller/Driver Block Diagram



Note **The FIP controller/driver can only operate in the high and medium speeds (PCC = 0011B or 0010B) of the main system clock (SCC.0 = 0). It may cause errors with any other clock or in the standby mode. Thus, be sure to stop FIP controller operation (DSPM.3 = 0) and then shift the unit to any other clock mode or the standby mode.**

5.9 POWER-ON FLAG (MASK OPTION)

The power-on flag (PONF) is automatically set (1) when the power-on reset circuit is activated and the power-on reset signal is generated. (See **Fig. 8-1 Reset Signal Generator**)

The PONF is mapped at bit 0 of address FD1H in the data memory space and can be tested by the memory bit manipulation instructions (SKT, SKF, SKTCLR) or cleared (CLR1).

Note The PONF cannot be set by SET1 instruction.

6. INTERRUPT FUNCTIONS

The μPD75206 has eight types of interrupt sources and can generate multiple interrupts with priority order. It is also equipped with two types of test sources. INT2 is an edge detected testable input.
The μPD75206 interrupt control circuit has the following functions:

- Hardware-controller vectored interrupt function which can control interrupt acknowledge with the interrupt enable flag (IExxx) and the interrupt master enable flag (IME).
- Function of setting any interrupt start address.
- Multiple interrupt function which can specify priority order with the interrupt priority select register (IPS).
- Interrupt request flag (IRQxxx) test function. (Interrupt generation can be checked by software.)
- Standby mode release function. (Interrupt to be released by interrupt enable flag can be selected.)

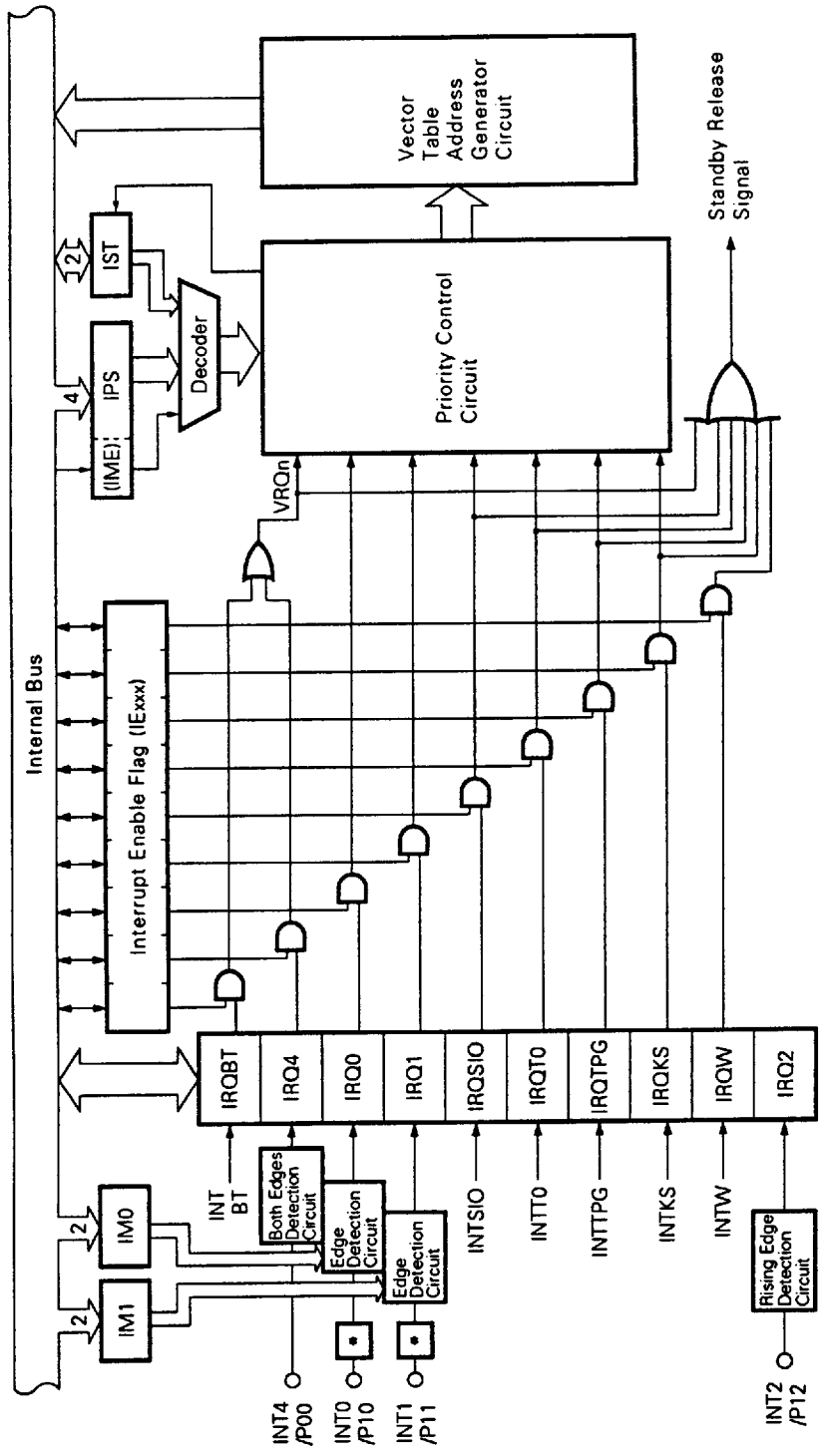


Fig. 6-1 Interrupt Control Circuit Block Diagram

7. STANDBY FUNCTIONS

Two standby modes (STOP mode and HALT mode) are available for the μPD75206 to decrease power consumption in the program standby mode.

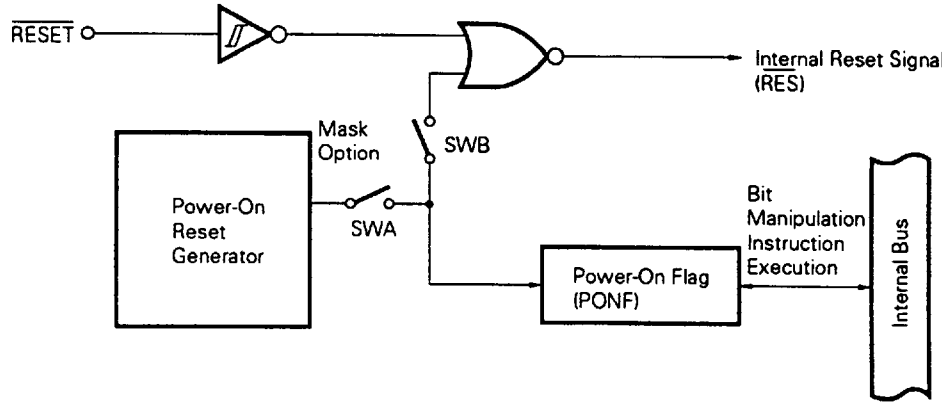
Table 7-1 Operation Status in Standby Mode

		STOP Mode	HALT Mode
Set instruction		STOP instruction	HALT instruction
System clock when set		Setting enabled only with main system clock.	Setting enabled with either main system clock or subsystem clock.
Operating State	Clock oscillator	Oscillator stops only with main system clock.	Stops only with CPU clock Φ (Oscillation continued).
	Basic interval timer	Operation stopped.	Operation (IRQBT set at reference time intervals).
	Serial interface	Operation enabled only when external $\overline{SCK}$ input is selected for serial clock.	Operation enabled when serial clock other than Φ is specified.
	Timer/event counter	Operation enabled only when TI0 pin input is specified for count clock.	Operation enabled.
	Timer/pulse generator	Operation stopped.	Operation enabled.
	Watch timer	Operation enabled only fXT is selected for count clock.	Operation enabled.
	FIP controller/driver	Operation disabled (display off mode set before disabling).	
	CPU	Operation stopped.	
Release signal		Interrupt request signal (except INT0, INT1, INT2) or $\overline{RESET}$ input enabled by interrupt enable flag.	

8. RESET FUNCTIONS

The reset signal ($\overline{RES}$) generator has a configuration shown in Fig.8-1.

Fig. 8-1 Reset Signal Generator



The power-on reset generator is a circuit to generate a one-shot pulse upon detection of the start-up of the power voltage. This pulse is used in the three ways according to SWA, SWB mask option specification shown in Fig. 8-1. (Refer to **10. MASK OPTION SELECTION.**)

9. INSTRUCTION SET

(1) Operand identifier and description

Enter an operand in the operand column of each instruction using the description method relating to the operand identifier of the instruction (refer to **RA75X Assembler Package User's Manual - Language (EEU-730)**). If more than one description method is available, select one. Capital alphabetic letters, plus and minus signs are keywords. Describe them as they are.

In the case of immediate data, describe appropriate numerical values or labels.

* For 8-bit data processing, only even addresses can be specified.

Identifier	Description Method
reg	X, A, B, C, D, E, H, L
reg 1	X, B, C, D, E, H, L
rp	XA, BC, DE, HL
rp1	BC, DE, HL
rp2	BC, DE
rp'	XA, BC, DE, HL, XA', BC', DE', HL'
rp'1	BC, DE, HL, XA', BC', DE', HL'
rpa	HL, HL+, HL-, DE, DL
rpa1	DE, DL
n4	4-bit immediate data or label
n8	8-bit immediate data or label
mem	8-bit immediate data or label*
bit	2-bit immediate data or label
fmem	FB0H to FBFH and FF0H to FFFH immediate data or labels
pmem	FC0H to FFFH immediate data or labels
addr	0000H to 177FH immediate data or labels
caddr	12-bit immediate data or label
faddr	11-bit immediate data or label
taddr	20H to 7FH immediate data (bit0 = 0) or label
PORTn	PORT0 to PORT6
IEXXX	IEBT, IESIO, IET0, IETPG, IE0, IE1, IEKS, IEW, IE4
RBn	RB0 to RB3
MBn	MB0, MB1, MB15

(2) Legend for operation description

A	: A register; 4-bit accumulator
B	: B register
C	: C register
D	: D register
E	: E register
H	: H register
L	: L register
X	: X register
XA	: Register pair (XA); 8-bit accumulator
BC	: Register pair (BC)
DE	: Register pair (DE)
HL	: Register pair (HL)
XA'	: Expanded register pair (XA')
BC'	: Expanded register pair (BC')
DE'	: Expanded register pair (DE')
HL'	: Expanded register pair (HL')
PC	: Program counter
SP	: Stack pointer
CY	: Carry flag; Bit accumulator
PSW	: Program status word
MBE	: Memory bank enable flag
RBE	: Register bank enable flag
PORTn	: Port n (n = 0 to 6)
IME	: Interrupt master enable flag
IPS	: Interrupt priority select register
IExxx	: Interrupt enable flag
RBS	: Register bank select register
MBS	: Memory bank select register
PCC	: Processor clock control register
•	: Address and bit delimiter
(xx)	: Contents addressed by xx
xxH	: Hexadecimal data

(3) Description of symbols in the addressing area column

*1	MB = MBE • MBS (MBS = 0, 1, 15)	Data Memory Addressing
*2	MB = 0	
*3	MBE = 0 : MB = 0 (00H to 7FH) MB = 15 (80H to FFH) MBE = 1 : MB = MBS (MBS = 0, 1, 15)	
*4	MB = 15, fmem = FB0H to FBFH, FF0H to FFFH	
*5	MB = 15, pmem = FC0H to FFFH	
*6	addr = 0000H to 177FH	Program Memory Addressing
*7	addr = (Current PC) − 15 to (Current PC) − 1, (Current PC) + 2 to (Current PC) + 16	
*8	caddr = 0000H to 0FFFH (PC_{12} = 0) or 1000H to 177FH (PC_{12} = 1)	
*9	faddr = 0000H to 07FFH	
*10	taddr = 0020H to 007FH	

Remarks
1. MB indicates accessible memory bank.
2. In *2, MB = 0 irrespective of MBE and MBS.
3. In *4 and *5, MB = 15 irrespective of MBE and MBS.
4. *6 to *10 indicate addressable areas.

(4) Description of the machine cycle column

S indicates the number of machine cycles required for skip operation by an instruction having skip function. The S value varies as follows:

- When not skipped ..... S = 0
- When 1-byte or 2-byte instructions are skipped ..... S = 1
- When 3-byte instructions are skipped (BR !addr, CALL !addr instruction) ..... S = 2

Note GETI instruction is skipped in one machine cycle.

One machine cycle is equal to one cycle(=tcy) of CPU clock Φ and three time periods are available according to PCC setting.

Note 1	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Transfer	MOV	A, #n4	1	1	A←n4		Stack A
		reg1, #n4	2	2	reg1←n4		
		XA, #n8	2	2	XA←n8		Stack A
		HL, #n8	2	2	HL←n8		Stack B
		rp2, #n8	2	2	rp2←n8		
		A, @HL	1	1	A←(HL)	*1	
		A, @HL+	1	2 + S	A←(HL), then L←L+1	*1	L = 0
		A, @HL–	1	2 + S	A←(HL), then L←L–1	*1	L = FH
		A, @rpa1	1	1	A←(rpa1)	*2	
		XA, @HL	2	2	XA←(HL)	*1	
		@HL, A	1	1	(HL)←A	*1	
		@HL, XA	2	2	(HL)←XA	*1	
		A, mem	2	2	A←(mem)	*3	
		XA, mem	2	2	XA←(mem)	*3	
		mem, A	2	2	(mem)←A	*3	
		mem, XA	2	2	(mem)←XA	*3	
		A, reg	2	2	A←reg		
		XA, rp'	2	2	XA←rp'		
		reg1, A	2	2	reg1←A		
		rp'1, XA	2	2	rp'1←XA		
	XCH	A, @HL	1	1	A↔(HL)	*1	
		A, @HL+	1	2 + S	A↔(HL), then L←L+1	*1	L = 0
		A, @HL–	1	2 + S	A↔(HL), then L←L–1	*1	L = FH
		A, @rpa1	1	1	A↔(rpa1)	*2	
		XA, @HL	2	2	XA↔(HL)	*1	
		A, mem	2	2	A↔(mem)	*3	
		XA, mem	2	2	XA↔(mem)	*3	
		A, reg1	1	1	A↔reg1		
		XA, rp'	2	2	XA↔rp'		
Note 2	MOVT	XA, @PCDE	1	3	XA←$(PC_{12-8}+DE)_{ROM}$		
		XA, @PCXA	1	3	XA←$(PC_{12-8}+XA)_{ROM}$		

Note 1. Instruction Group
2. Table reference

Note	Mnemonic	Operand	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Bit transfer	MOV1	CY, fmem.bit	2	2	CY←(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY←(H+mem$_{3-0}$.bit)	*1	
		fmem.bit, CY	2	2	(fmem.bit)←CY	*4	
		pmem.@L, CY	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))←CY	*5	
		@H+mem.bit, CY	2	2	(H+mem$_{3-0}$.bit)←CY	*1	
Operation	ADDS	A, #n4	1	1 + S	A←A+n4		carry
		XA, #n8	2	2 + S	XA←XA+n8		carry
		A, @HL	1	1 + S	A←A+(HL)	*1	carry
		XA, rp'	2	2 + S	XA←XA+rp'		carry
		rp'1, XA	2	2 + S	rp'1←rp'1+XA		carry
	ADDC	A, @HL	1	1	A, CY←A+(HL)+CY	*1	
		XA, rp'	2	2	XA, CY←XA+rp'+CY		
		rp'1, XA	2	2	rp'1, CY←rp'1+XA+CY		
	SUBS	A, @HL	1	1 + S	A←A−(HL)	*1	borrow
		XA, rp'	2	2 + S	XA←XA−rp'		borrow
		rp'1, XA	2	2 + S	rp'1←rp'1−XA		borrow
	SUBC	A, @HL	1	1	A, CY←A−(HL)−CY	*1	
		XA, rp'	2	2	XA, CY←XA−rp'−CY		
		rp'1, XA	2	2	rp'1, CY←rp'1−XA−CY		
	AND	A, #n4	2	2	A←A∧n4		
		A, @HL	1	1	A←A∧(HL)	*1	
		XA, rp'	2	2	XA←XA∧rp'		
		rp'1, XA	2	2	rp'1←rp'1∧XA		
	OR	A, #n4	2	2	A←A∨n4		
		A, @HL	1	1	A←A∨(HL)	*1	
		XA, rp'	2	2	XA←XA∨rp'		
		rp'1, XA	2	2	rp'1←rp'1∨XA		
	XOR	A, #n4	2	2	A←A⊻n4		
		A, @HL	1	1	A←A⊻(HL)	*1	
		XA, rp'	2	2	XA←XA⊻rp'		
		rp'1, XA	2	2	rp'1←rp'1⊻XA		

Note Instruction Group

Note 1	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Note 2	RORC	A	1	1	$CY \leftarrow A_0$, $A_3 \leftarrow CY$, $A_{n-1} \leftarrow A_n$		
	NOT	A	2	2	$A \leftarrow \overline{A}$		
Increment/decrement	INCS	reg	1	1 + S	reg←reg+1		reg = 0
		rp1	1	1 + S	rp1←rp1+1		rp1 = 00H
		@HL	2	2 + S	(HL)←(HL)+1	*1	(HL) = 0
		mem	2	2 + S	(mem)←(mem)+1	*3	(mem) = 0
	DECS	reg	1	1 + S	reg←reg−1		reg = FH
		rp'	2	2 + S	rp'←rp'−1		rp = FFH
Compare	SKE	reg, #n4	2	2 + S	Skip if reg = n4		reg = n4
		@HL, #n4	2	2 + S	Skip if (HL) = n4	*1	(HL) = n4
		A, @HL	1	1 + S	Skip if A = (HL)	*1	A = (HL)
		XA, @HL	2	2 + S	Skip if XA = (HL)	*1	XA = (HL)
		A, reg	2	2 + S	Skip if A = reg		A = reg
		XA.rp'	2	2 + S	Skip if XA = rp'		XA = rp'
Carry flag manipulation	SET1	CY	1	1	CY←1		
	CLR1	CY	1	1	CY←0		
	SKT	CY	1	1 + S	Skip if CY = 1		CY = 1
	NOT1	CY	1	1	$CY \leftarrow \overline{CY}$		

Note 1. Instruction Group
2. Accumulator manipulation

Note	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Memory bit manipulation	SET1	mem.bit	2	2	(mem.bit)←1	*3	
		fmem.bit	2	2	(fmem.bit)←1	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))←1	*5	
		@H + mem.bit	2	2	(H+mem$_{3-0}$.bit)←1	*1	
	CLR1	mem.bit	2	2	(mem.bit)←0	*3	
		fmem.bit	2	2	(fmem.bit)←0	*4	
		pmem.@L	2	2	(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))←0	*5	
		@H+mem.bit	2	2	(H+mem$_{3-0}$.bit)←0	*1	
	SKT	mem.bit	2	2 + S	Skip if (mem.bit) = 1	*3	(mem.bit) = 1
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 1	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 1	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H+mem$_{3-0}$.bit) = 1	*1	(@H+mem.bit) = 1
	SKF	mem.bit	2	2 + S	Skip if (mem.bit) = 0	*3	(mem.bit) = 0
		fmem.bit	2	2 + S	Skip if (fmem.bit) = 0	*4	(fmem.bit) = 0
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$)) = 0	*5	(pmem.@L) = 0
		@H+mem.bit	2	2 + S	Skip if (H+mem$_{3-0}$.bit) = 0	*1	(@H+mem.bit) = 0
	SKTCLR	fmem.bit	2	2 + S	Skip if (fmem.bit) = 1 and clear	*4	(fmem.bit) = 1
		pmem.@L	2	2 + S	Skip if (pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))=1 and clear	*5	(pmem.@L) = 1
		@H+mem.bit	2	2 + S	Skip if (H+mem$_{3-0}$.bit)=1 and clear	*1	(@H+mem.bit)=1
	AND1	CY, fmem.bit	2	2	CY←CY∧(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←CY∧(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY←CY∧(H+mem$_{3-0}$.bit)	*1	
	OR1	CY, fmem.bit	2	2	CY←CY∨(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←CY∨(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY←CY∨(H+mem$_{3-0}$.bit)	*1	
	XOR1	CY, fmem.bit	2	2	CY←CY⊻(fmem.bit)	*4	
		CY, pmem.@L	2	2	CY←CY⊻(pmem$_{7-2}$+L$_{3-2}$.bit(L$_{1-0}$))	*5	
		CY, @H+mem.bit	2	2	CY←CY⊻(H+mem$_{3-0}$.bit)	*1	
Branch	BR	addr	—	—	PC$_{12-0}$←addr (Optimum instruction is selected from among BR !addr, BRCB !caddr and BR $addr by an assembler.)	*6	
		!addr	3	3	PC$_{12-0}$←addr	*6	
		$addr	1	2	PC$_{12-0}$←addr	*7	
	BRCB	!caddr	2	2	PC$_{12-0}$←PC$_{12}$+caddr$_{11-0}$	*8	
	BR	PCDE	2	3	PC$_{12-0}$←PC$_{12-8}$+DE		
		PCXA	2	3	PC$_{12-0}$←PC$_{12-8}$+XA		

Note Instruction Group

Note	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Subroutine stack control	CALL	!addr	3	3	(SP–4) (SP–1) (SP–2)←PC_{11-0} (SP–3)← MBE, RBE, 0, PC_{12} PC_{12-0}←addr, SP←SP–4	*6	
	CALLF	!faddr	2	2	(SP–4) (SP–1) (SP–2)←PC_{11-0} (SP–3)← MBE, RBE, 0, PC_{12} PC_{12-0}←00, faddr, SP←SP–4	*9	
	RET		1	3	MBE, RBE, 0, PC_{12}←(SP+1) PC_{11-0}←(SP) (SP+3) (SP+2) SP←SP+4		
	RETS		1	3 + S	MBE, RBE, 0, PC_{12}←(SP+1) PC_{11-0}←(SP) (SP+3) (SP+2) SP←SP+4, then skip unconditionally		Unconditional
	RETI		1	3	×, ×, ×, PC_{12}←(SP+1) PC_{11-0}←(SP) (SP+3) (SP+2) PSW←(SP+4) (SP+5), SP←SP+6		
	PUSH	rp	1	1	(SP–1) (SP–2)←rp, SP←SP–2		
		BS	2	2	(SP–1)←MBS, (SP–2)←RBS, SP←SP–2		
	POP	rp	1	1	rp←(SP+1) (SP), SP←SP+2		
		BS	2	2	MBS←(SP+1), RBS←(SP), SP←SP+2		
Interrupt control	EI		2	2	IME(IPS.3)←1		
		IExxx	2	2	IExxx←1		
	DI		2	2	IME(IPS.3)←0		
		IExxx	2	2	IExxx←0		
Input/output	IN *1	A, PORTn	2	2	A←PORTn (n = 0 to 6)		
		XA, PORTn	2	2	XA←PORTn+1, PORTn (n = 4)		
	OUT *1	PORTn, A	2	2	PORTn←A (n = 2 to 6)		
		PORTn, XA	2	2	PORTn+1, PORTn←XA (n = 4)		
CPU control	HALT		2	2	Set HALT Mode (PCC.2←1)		
	STOP		2	2	Set STOP Mode (PCC.3←1)		
	NOP		1	1	No Operation		
Special	SEL	RBn	2	2	RBS←n (n = 0 to 3)		
		MBn	2	2	MBS←n (n = 0, 1, 15)		

* 1. MBE = 0 or MBE = 1 and MBE = 15 must be set for execution of IN/OUT instruction

Note Instruction Group

Note	Mnemonic	Operands	No. of Bytes	Machine Cycle	Operation	Addressing Area	Skip Condition
Special	GETI *1	taddr	1	3	• TBR instruction $PC_{12-0} \leftarrow (taddr)_{4-0}+(taddr+1)$	*10	
					• TCALL instruction $(SP-4)(SP-1)(SP-2) \leftarrow PC_{11-0}$ $(SP-3) \leftarrow$ MBE, RBE, 0, PC_{12} $PC_{12-0} \leftarrow (taddr)_{4-0}+(taddr+1)$ $SP \leftarrow SP-4$		
					• (taddr) (taddr+1) instruction executed in the case of instruction except TBR and TCALL instructions		Depends on instructions referred to.

* 1. TBR and TCALL instructions are assembled pseudo-instructions to define the GETI instruction table.

Note Instruction Group

10. MASK OPTION SELECTION ★

The μPD75206 has the following mask options enabling or disabling on-chip components.

(1) Pin

Pin	Mask Option
P60 to P63	Pull-up resistor incorporation enabled bit-wise
T0/T9	
T10/PH3 to T13/PH0	
T14/S11, T15/S10	
S0 to S9	
XT1, XT2	Deletion of sybsystem clock oscillator feedback resistor possible

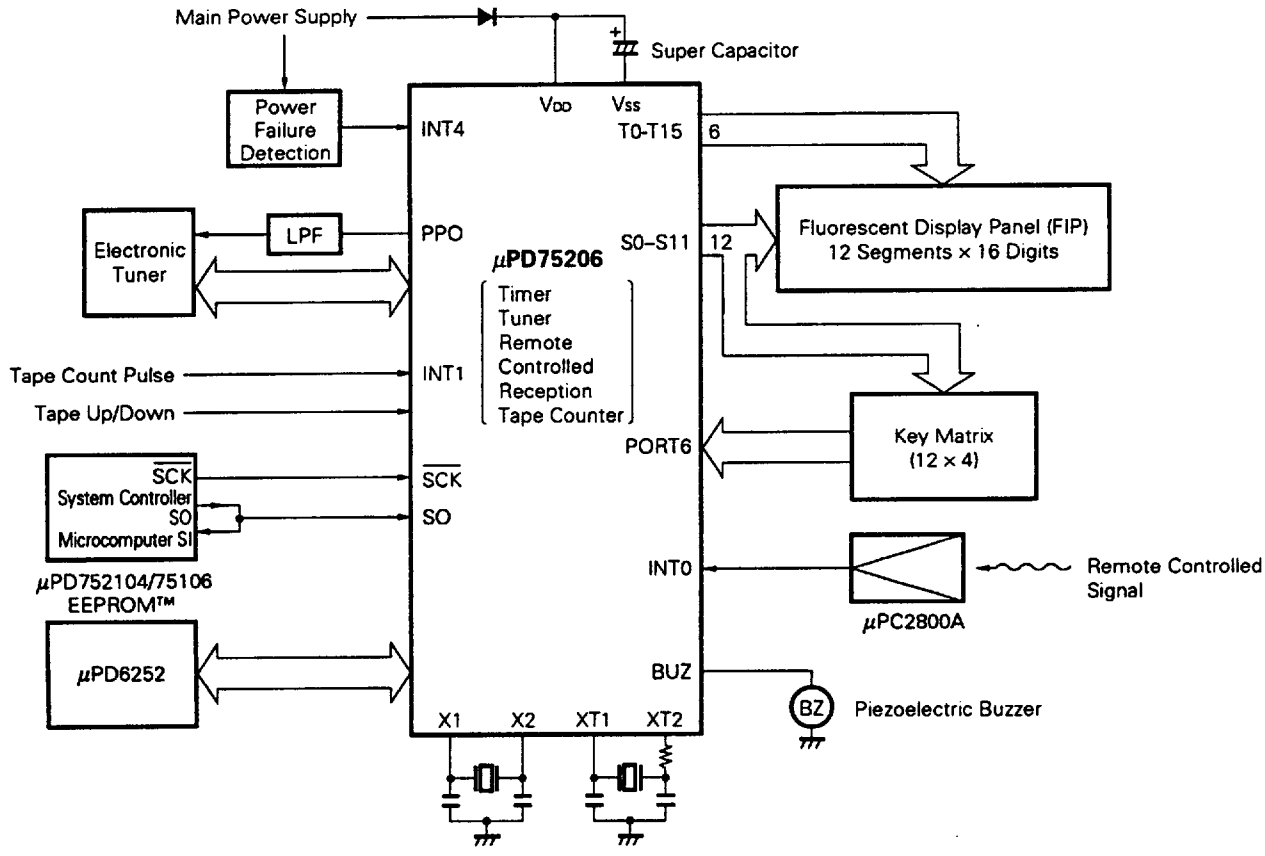
Note 1. In a system not using subsystem clocks, power consumption in the STOP mode can be decreased by removing the feedback resistor from the oscillator.
2. The feedback resistor must be incorporated when use subsystem clock.

(2) Power-on reset generator, power-on flag (PONF)
One of the following three can be selected.

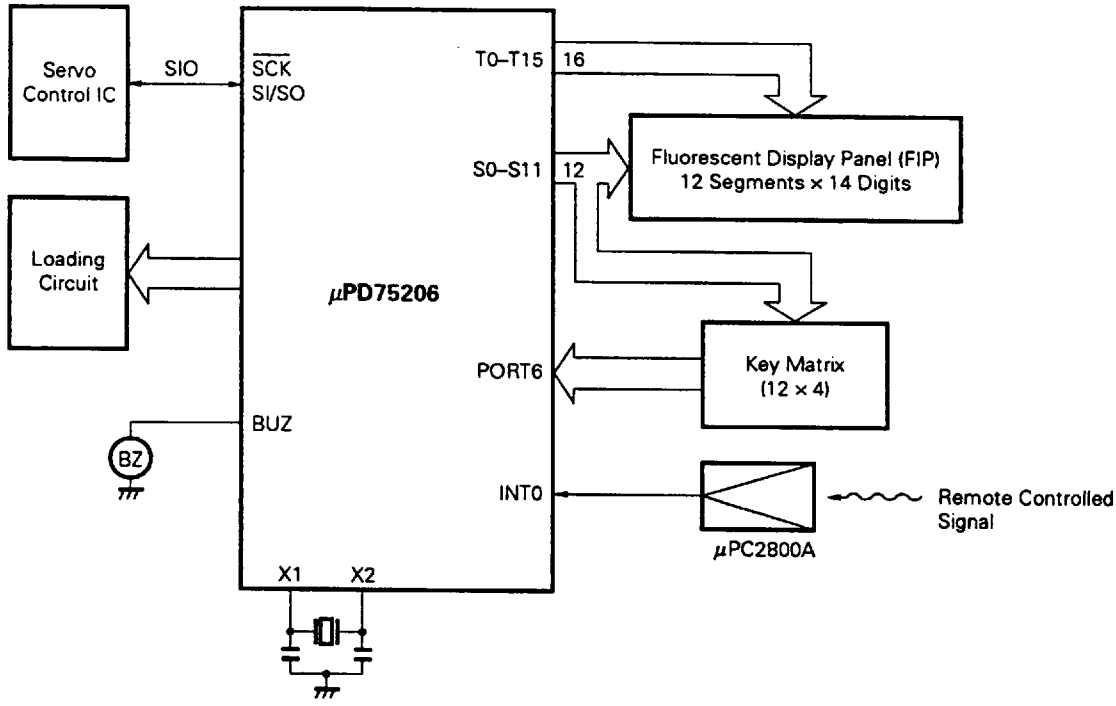
Switch Selection (See Fig. 8-1)		Power-On Reset Generator	Power-On Flag (PONF)	Internal Reset Signal ($\overline{RES}$)
SWA	SWB			
ON	ON	Incorporated	Incorporated	Generate automatically
ON	OFF	Incorporated	Incorporated	Not generate automatically
OFF	OFF	Not incorporated	Not incorporated	——

11. APPLICATION BLOCK DIAGRAM

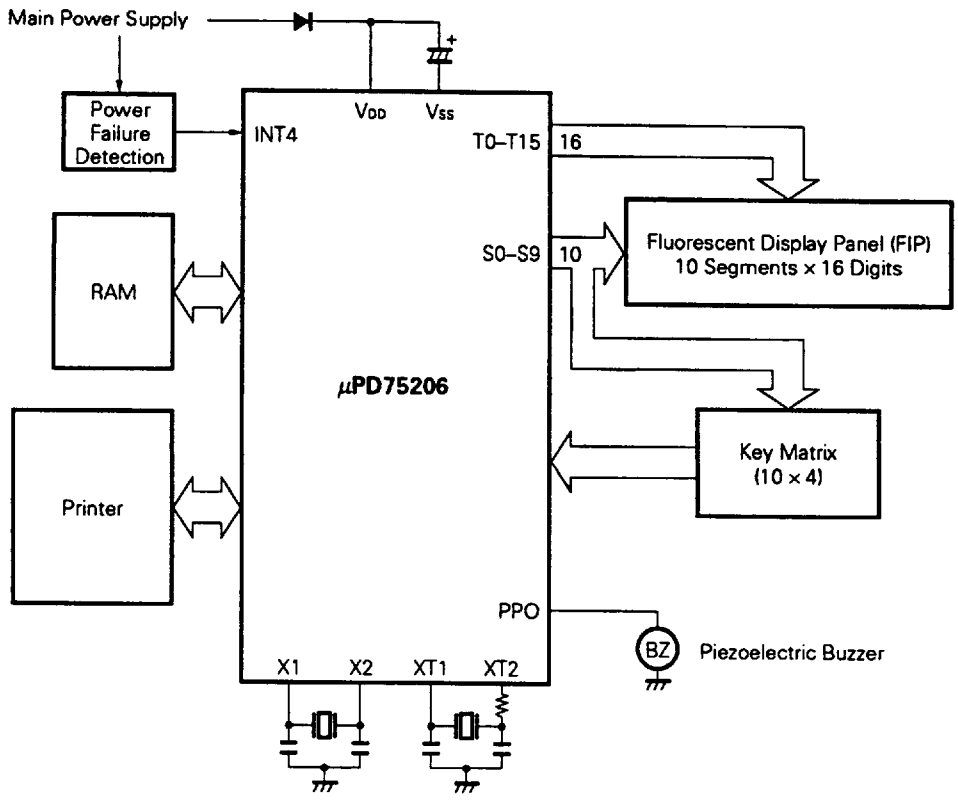
11.1 VCR TIMER TUNER



11.2 COMPACT DISK PLAYER



11.3 ECR



12. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (Ta = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATING	UNIT
Power supply voltage	V_{DD}		−0.3 to +7.0	V
	V_{LOAD}		V_{DD} −40 to V_{DD} +0.3	V
	V_{PRE}		V_{DD} −12 to V_{DD} +0.3	V
Input voltage	V_I		−0.3 to V_{DD} +0.3	V
Output voltage	V_O	Pins except display output pins	−0.3 to V_{DD} +0.3	V
	V_{OD}	Display output pins	V_{DD} −40 to V_{DD} +0.3	V
Output current high	I_{OH}	1 pins except display output pins	−15	mA
		S0 to S9 1 pin	−15	mA
		T0 to T15 1 pin	−30	mA
		Total of pins except display output pins	−20	mA
		Total of display output pins	−120	mA
Output current low	I_{OL}	1 pin	17	mA
		Total of pins	60	mA
Total loss*1	P_T	Plastic QFP	450	mW
		Plastic shrink DIP	600	mW
Operating temperature	T_{opt}		−40 to +85	°C
Storage temperature	T_{stg}		−65 to +150	°C

POWER SUPPLY VOLTAGE RANGE (Ta = −40 to +85 °C)

PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
CPU *2		*3	6.0	V
Display controller		4.5	6.0	V
Time/pulse generator		4.5	6.0	V
Other hardware *2		2.7	6.0	V

* 1. Calculation of total loss

Design so that the sum of the following three power consumption values for the μPD75206CW/GF will be less than the total loss P_T (It is recommended to use the system with 80 % or less of the rating).

① CPU loss : Given as V_{DD} (MAX.) × I_{DD1} (MAX.)

② Output pin loss : There are normal output pin loss and display output pin loss. It is necessary to add a loss derived from the flow of maximum current to each output pin.

③ Pull-down register loss : Power loss due to a pull-down resistor incorporated in the display output pin by mask option.

Example Suppose 4-LED output with $9_{SEG} \times 11_{DIGIT}$, V_{DD} = 5 V + 10 % and 4.19 MHz oscillation and let a maximum of 3 mA, 15 mA and 10 mA flow to the segment pin, timing pin and LED output pin, respectively. Further, let the voltage of fluorescent display tube (V_{LOAD} voltage) be −30 V and normal voltage be small.

① CPU loss : 5.5 V × 9.0 mA = 49.5 mW

② Pin loss : Segment pin ..... 2V × 3 mA × 9 = 54 mW

Timing pin ..... 2V × 15 mA = 30 mW

$$\text{LED output} \ldots\ldots \left(\frac{10}{15} \times 2\ \text{V}\right) \times 10\ \text{mA} \times 4 = 53\ \text{mW}$$

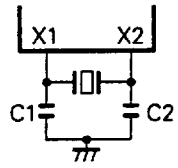
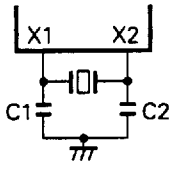
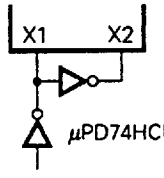
③ Pull-down resistor loss ..... $\dfrac{(30 + 5.5\text{V})^2}{25\ \text{k}\Omega} \times 10 = 504.1\ \text{mW}$

PT = ① + ② + ③ = 690.6 mW

In this example, since the allowable total loss is 600 mW for the shrink DIP package, it is necessary to decrease power consumption by decreasing the number of on-chip pull-down resistors. In this example, power consumption can be adjusted to 528.3 mW by incorporating pull-down resistors in only 11 digit outputs and 7 segment outputs and externally mounting pull-down resistors to the 2 remaining segment outputs.

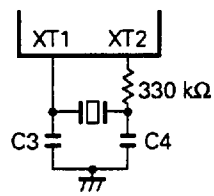
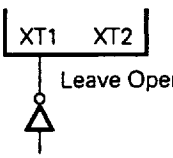
2. Except the system clock oscillator, display controller and timer/pulse generator.
3. The operating voltage range varies depending on the cycle time. Refer to the section describing AC characteristics.

MAIN SYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Ceramic resonator*1		Oscillator frequency (f_{XX}) *2	V_{DD} = Oscillation voltage range	2.0		5.0*4	MHz
		Oscillation stabilization time *3	After V_{DD} reaches the minimum value in the oscillation voltage range			4	ms
Crystal resonator		Oscillator frequency (f_{XX}) *2		2.0	4.19	5.0 *4	MHz
		Oscillation stabilization time *3	V_{DD} = 4.5 to 6.0 V			10	ms
						30	ms
External clock		X1 input frequency (f_X) *2		2.0		5.0*4	MHz
		X1 input high and low level widths (t_{XH}, t_{XL})		100		250	ns

* 1. Resonators are shown in following page.
2. Oscillator characteristics only. Refer to the description of AC characteristics for details of instruction execution time.
3. Time required for oscillation to become stabilized after V_{DD} application or STOP mode release.
★ 4. When oscillator frequency is " 4.19 < fx ≤ 5.0 MHz ", do not select " PCC = 0011 " as instruction execution time. If " PCC = 0011 " is selected, 1 machine cycle becomes less than 0.95 μs, with the result that the specified MIN. value of 0.95 μs cannot be observed.

SUBSYSTEM CLOCK OSCILLATOR CHARACTERISTICS (Ta = –40 to +85 °C, V_{DD} = 2.7 to 6.0 V)

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Crystal resonator*1		Oscillator frequency (f_{XT}) *2		32	32.768	35	kHz
		Oscillation stabilization time *3	V_{DD} = 4.5 to 6.0 V		1.0	2	s
						10	s
External clock		XT1 input frequency (f_{XT})		32		100	kHz
		XT1 input high and low level widths (t_{XTH}, t_{XTL})		10		32	μs

* 1. Recommended resonators are shown in following page.
2. Oscillator characteristics only. Refer to the description of AC characteristics for instruction execution time.
3. Oscillation stabilization time is a time required for oscillation to become stabilized after V_{DD} application or STOP mode release.

CAPACITANCE (Ta = 25 °C, V_{DD} = 0 V)

PARAMETER		SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance		C_{IN}	f = 1 MHz Unmeasured pin returned to 0V			15	pF
Output capacitance	Except display output	C_{OUT}				15	pF
	Display output					35	pF
Input /output capacitance		C_{IO}				15	pF

RECOMMENDED OSCILLATOR CONSTANTS

MAIN SYSTEM CLOCK : CERAMIC (Ta = –40 to +85 °C)

MANUFACTURER	PRODUCT NAME	EXTERNAL CAPACITANCE (pF)		OSCILLATION VOLTAGE RANGE (V)	
		C1	C2	MIN.	MAX.
Murata Mfg. Co., Ltd.	CSA 4.19MG	30	30	4.0	6.0
Kyocera Corp.	KBR–2.09MS	68	68	4.0	6.0
	KBR–3.58MS KBR–4.19MS KBR–4.9MS	33	33		

MAIN SYSTEM CLOCK : CRYSTAL (Ta = –40 to +85 °C)

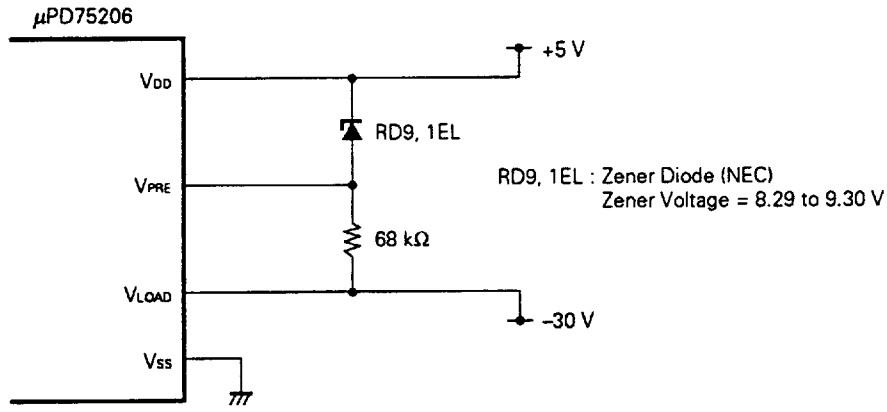
MANUFACTURER	FREQUENCY (MHz)	HOLDER	EXTERNAL CAPACITANCE (pF)		OSCILLATION VOLTAGE RANGE (V)	
			C1	C2	MIN.	MAX.
Kinseki	4.19	HC–49/U	15	15	2.7	6.0

Note **Use a 10 to 33-pF capacitor as the external capacitance C1 of the crystal oscillator for fine-tuning the frequency to a specific value.**

DC CHARACTERISTICS (Ta = –40 to 85 °C, V_{DD} = 2.7 to 6.0 V)

PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH1}	Except below			0.7 V_{DD}		V_{DD}	V
	V_{IH2}	Ports 0, 1, $\overline{RESET}$			0.75 V_{DD}		V_{DD}	V
	V_{IH3}	X1, X2, XT1			V_{DD}–0.4		V_{DD}	V
	V_{IH4}	Port 6	V_{DD} = 4.5 to 6.0 V		0.65 V_{DD}		V_{DD}	V
					0.7 V_{DD}		V_{DD}	V
Input Voltage low	V_{IL1}	Except below			0		0.3 V_{DD}	V
	V_{IL2}	Ports 0, 1, 6, $\overline{RESET}$			0		0.2 V_{DD}	V
	V_{IL3}	X1, X2, XT1			0		0.4	V
Output voltage high	V_{OH}	All output pins	V_{DD} = 4.5 to 6.0V, I_{OH} = –1 mA		V_{DD}–1.0			V
			I_{OH} = –100 μA		V_{DD}–0.5			V
Output voltage low	V_{OL}	Ports 4, 5	V_{DD} = 4.5 to 6.0V, I_{OL} = 15 mA			0.4	2.0	V
		All output pins	V_{DD} = 4.5 to 6.0V, I_{OL} = 1.6 mA				0.4	V
			I_{OL} = 400 μA				0.5	V
Input leakage current high	I_{LIH1}	Except X1,X2,XT1	V_{IN} = V_{DD}				3	μA
	I_{LIH2}	X1, X2, XT1					20	μA
Input leakage current low	I_{LIL1}	Except X1,X2,XT1	V_{IN} = 0 V				–3	μA
	I_{LIL2}	X1, X2, XT1					–20	μA
Output leakage current high	I_{LOH}	All output pins	V_{OUT} = V_{DD}				3	μA
Output leakage current low	I_{LOL1}	Except display output	V_{OUT} = 0 V				–3	μA
	I_{LOL2}	Display output	V_{OUT} = V_{LOAD} = V_{DD} – 35 V				–10	μA
Display output current	I_{OD}	S0 to S9	V_{DD} = 4.5 to 6.0 V, V_{DD} = V_{DD} – 2 V	V_{PRE} = V_{DD} – 9 ±1 V*1	–3	–5.5		mA
				V_{PRE} = 0 V	–1.5	–3.5		mA
		T0 to T15		V_{PRE} = V_{DD} – 9 ±1 V*1	–15	–22		mA
				V_{PRE} = 0 V	–7	–15		mA
Built-in pull-down resistor (mask option)	R_{PS}	Port 6 V_{IN} = V_{DD}	V_{DD} = 4.5 to 6.0 V		30	80	200	kΩ
					30		1000	kΩ
	R_L	Display output	V_{DD} – V_{LOAD} = 35 V		40	70	120	kΩ
Supply current*2	I_{DD1}	4.19 MHz crystal oscillation C1 = C2 = 15pF	V_{DD} = 5 V ±10 %*3			3.0	9.0	mA
			V_{DD} = 3 V ±10 %*4			0.55	1.5	mA
	I_{DD2}		HALT mode	V_{DD} = 5 V ±10 %		600	1800	μA
				V_{DD} = 3 V ±10 %		200	600	μA
	I_{DD3}	32 kHz crystal oscillation*5	V_{DD} = 3 V ±10 %			40	120	μA
	I_{DD4}		HALT mode	V_{DD} = 3 V ±10 %		5	15	μA
	I_{DD5}	XT1 = 0 V STOP mode	V_{DD} = 5 V ±10 %			0.5	20	μA
			V_{DD} = 3 V ±10 %			0.1	10	μA

* 1. The following external circuit is recommended.

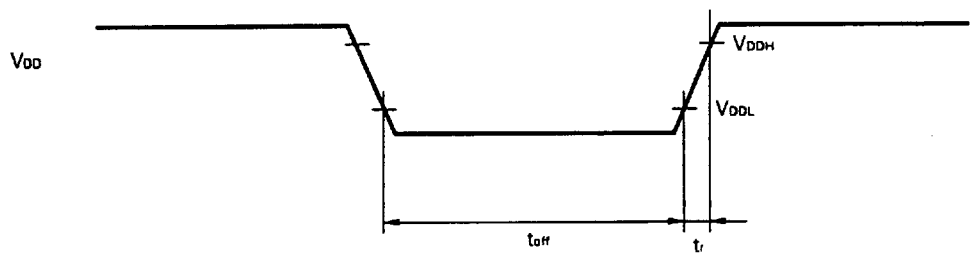


2. Current to the on-chip pull-down resistor and power-on reset circuit (mask option) is not included.
3. When the processor clock control register (PCC) is set to 0011 and is operated in the high-speed mode.
4. When the PCC register is set to 0000 and is operated in the low-speed mode.
5. When the system clock control register (SCC) is set to 1001 and is operated with the subsystem clock with main system clock oscillation stopped.

POWER-ON RESET CIRCUIT CHARACTERISTICS (MASK OPTION) (Ta = 40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Power-on reset operating voltage high	V_{DDH}		4.5		6.0	V
Power-on reset operating voltage low	V_{DDL}		0		0.2	V
Power supply voltage rise time	t_r		10		*1	μs
Power supply voltage off time	t_{off}		1			s
Power-on reset circuit*2 current consumption	I_{DDPR}	V_{DD} = 5 V ±10 %		10	100	μA
		V_{DD} = 2.7 V		2	20	μA

* 1. 2^{17}/fxx (31.3 ms at fxx = 4.19 MHz)
2. Current with on-chip power-on reset circuit or power-on flag.



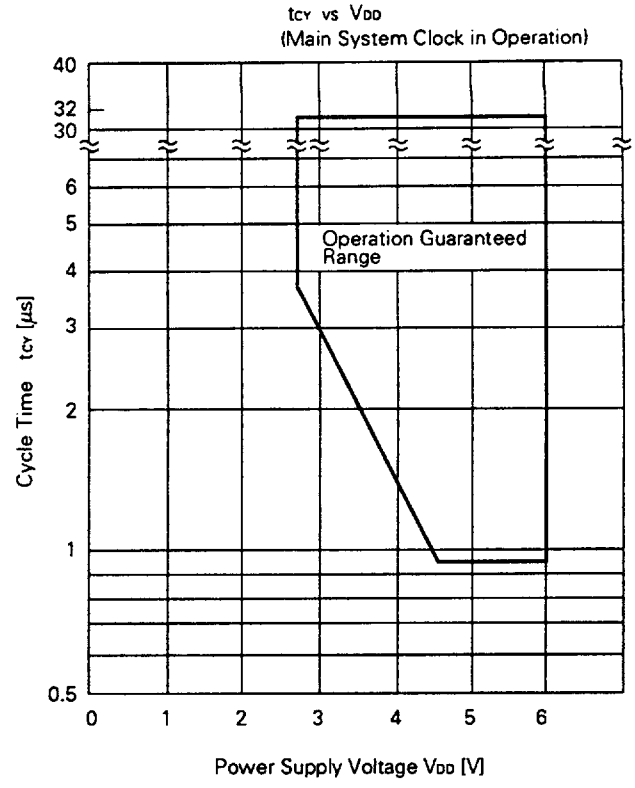
Remarks Start the power supply smoothly.

AC CHARACTERISTICS (Ta = –40 to +85 °C , V_{DD} = 2.7 to 6.0 V)

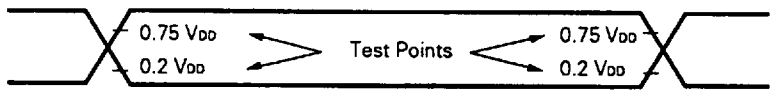
PARAMETER	SYMBOL	TEST CONDITIONS			MIN.	TYP.	MAX.	UNIT
CPU clock cycle time (minimum instruction execution time = 1 machine cycle) *1	t_{CY}	Operation with main system clock	V_{DD} = 4.5 to 6.0 V		0.95		32	μs
					3.8		32	μs
		Operation with sub-system clock			114	122	125	μs
TI0 input frequency	f_{TI}	V_{DD} = 4.5 to 6.0 V			0		0.6	MHz
					0		165	kHz
TI0 input high and low-level widths	t_{TIH}, t_{TIL}	V_{DD} = 4.5 to 6.0 V			0.83			μs
					3			μs
$\overline{SCK}$ cycle time	t_{KCY}	V_{DD} = 4.5 to 6.0 V		Input	0.8			μs
				Output	0.95			μs
				Input	3.2			μs
				Output	3.8			μs
$\overline{SCK}$ high and low-level widths	t_{KH}, t_{KL}	V_{DD} = 4.5 to 6.0 V		Input	0.4			μs
				Output	$t_{KCY}/2-50$			ns
				Input	1.6			μs
				Output	$t_{KCY}/2-150$			ns
SI setup time (to $\overline{SCK}$↑)	t_{SIK}				100			ns
SI hold time (from $\overline{SCK}$↑)	t_{KSI}				400			ns
SO output delay time from $\overline{SCK}$↓	t_{KSO}	V_{DD} = 4.5 to 6.0 V					300	ns
							1000	ns
Interrupt input high and low-level widths	t_{INTH}, t_{INTL}			INT0	*2			μs
				INT1	2t_{CY}			μs
				INT2, 4	10			μs
$\overline{RESET}$ low-level width	t_{RSL}				10			μs

* 1. CPU clock (Φ) cycle time is determined by the oscillator frequency of the connected resonator, the system clock control register (SCC) and the processor clock control register (PCC). The cycle time t_{CY} characteristics for power supply voltage V_{DD} when the main system clock is in operation is shown below.

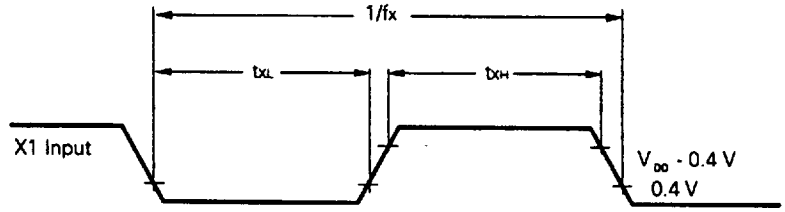
2. $2t_{CY}$ or 128/fxx is set by interrupt mode register (IM0) setting.

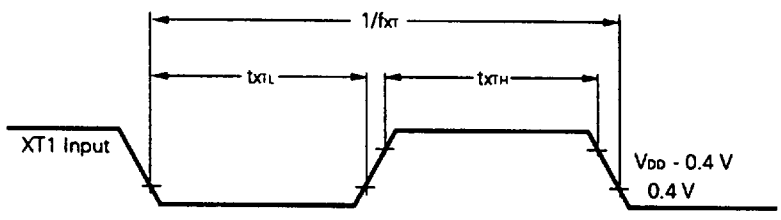


AC Timing Measurement Values (Except X1 and XT1 Inputs)

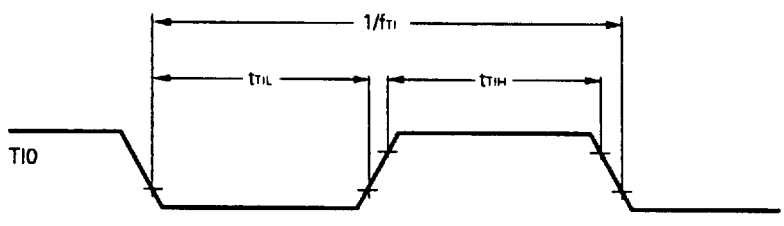


Clock Timing

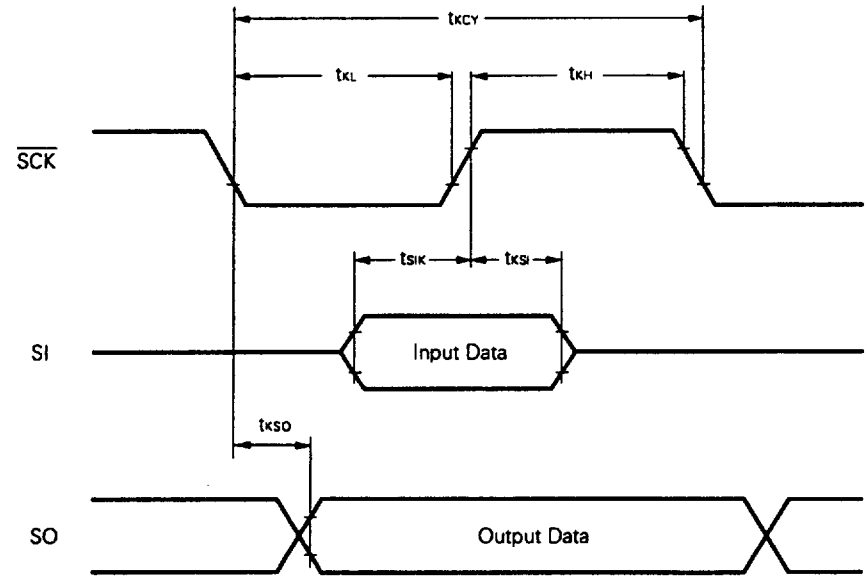




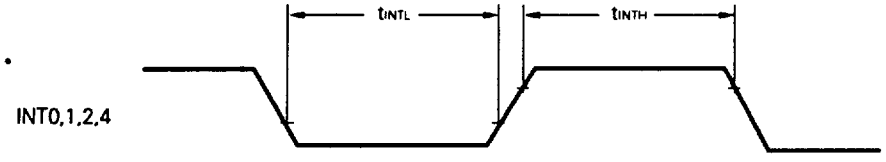
TI0 Timing



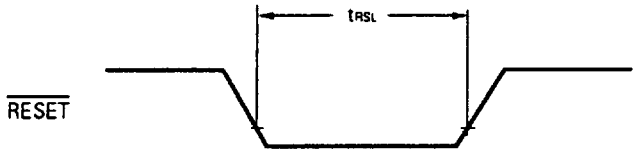
Serial Transfer Timing



Interrupt Input Timing



$\overline{\text{RESET}}$ Input Timing



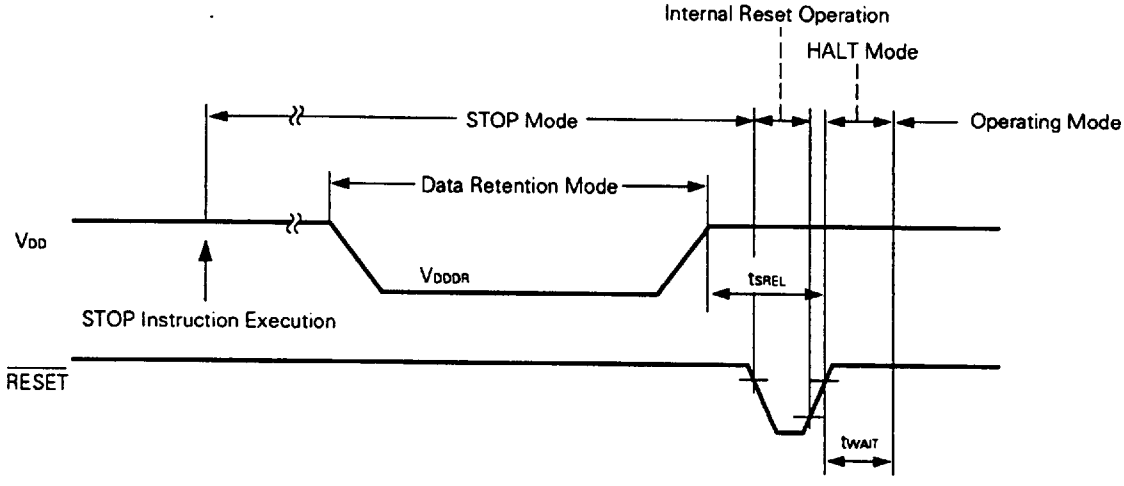
DATA MEMORY STOP MODE LOW POWER SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (Ta = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention power supply voltage	V_{DDDR}		2.0		6.0	V
Data retention power supply current *1	I_{DDDR}	V_{DDDR} = 2.0V		0.1	10	μA
Release signal set time	t_{SREL}		0			μs
Oscillation stabilization wait time *2	t_{WAIT}	Release by $\overline{RESET}$		$2^{17}/fx$		ms
		Release by interrupt request		*3		ms

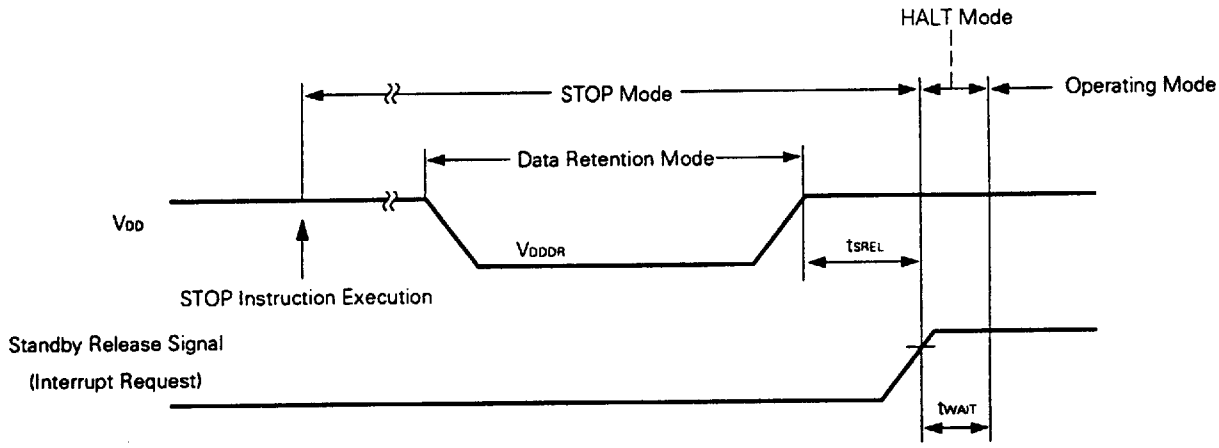
* 1. Current to the on-chip pull-down resistor and power-on reset circuit (mask option) is not included.
2. Oscillation stabilization wait time is time to stop CPU operation to prevent unstable operation upon oscillation start.
3. According to the setting of the basic interval timer mode register (BTM) (see below).

BTM3	BTM2	BTM1	BTM0	Wait Time (Values at fxx = 4.19 MHz in parentheses)
—	0	0	0	$2^{20}/fx$ (approx. 250 ms)
—	0	1	1	$2^{17}/fx$ (approx. 31.3 ms)
—	1	0	1	$2^{15}/fx$ (approx. 7.82 ms)
—	1	1	1	$2^{13}/fx$ (approx. 1.95 ms)

Data Retention Timing (STOP Mode Release by $\overline{RESET}$)

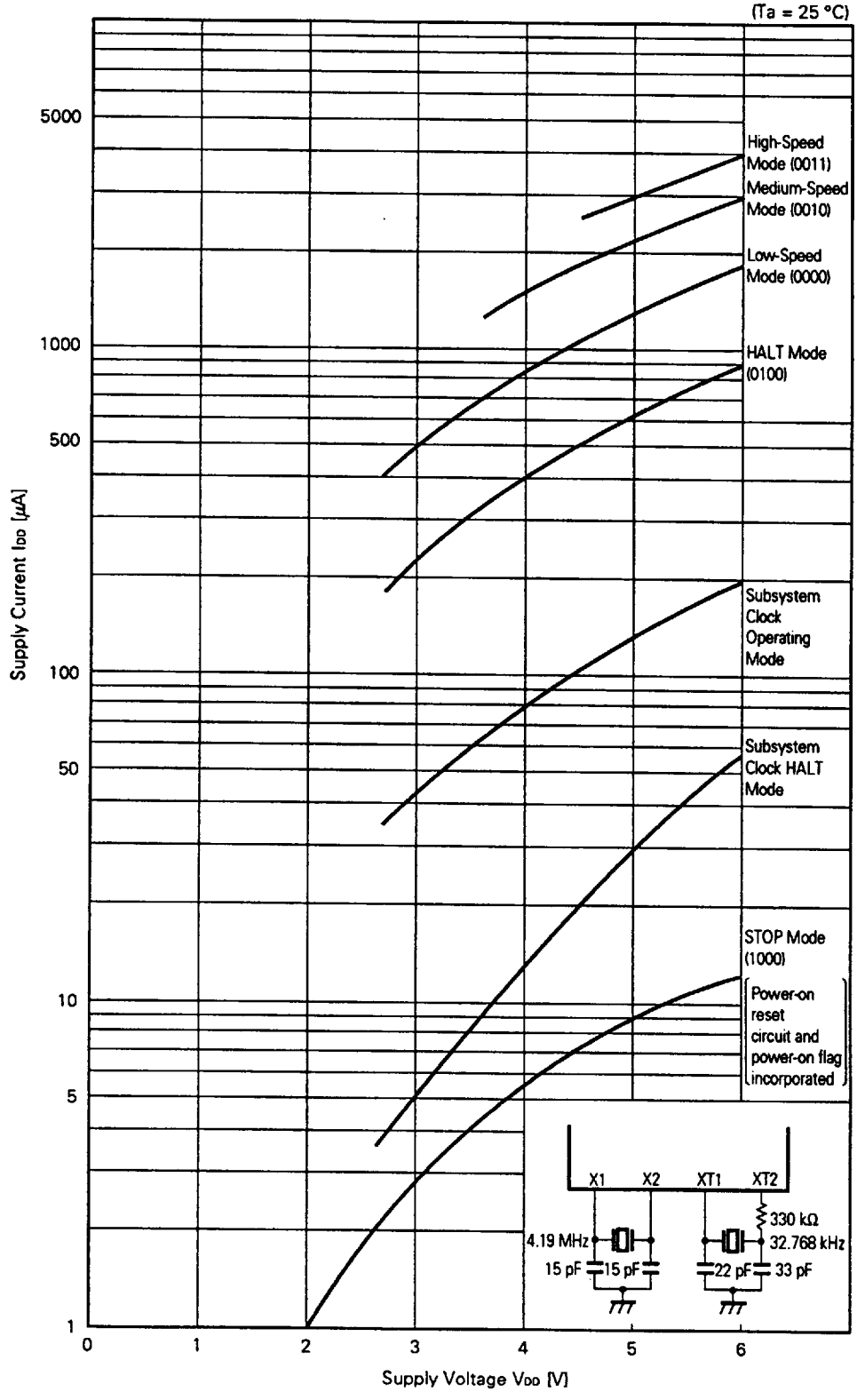


Data Retention Timing (Standby Release Signal: STOP Mode Release by Interrupt Signal)



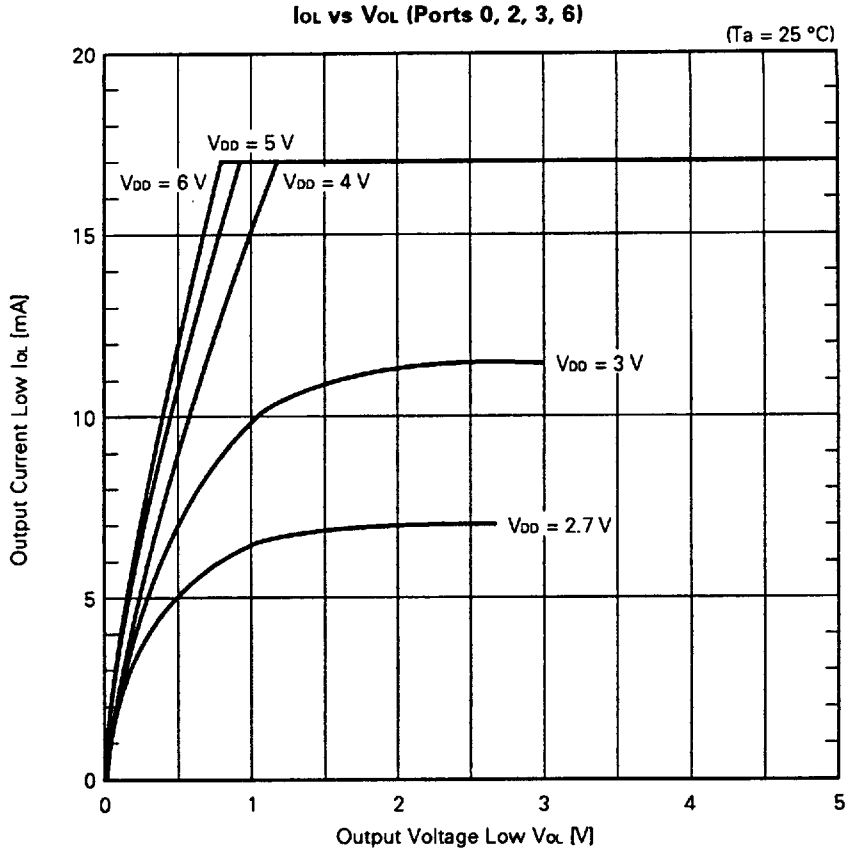
13. CHARACTERISTIC CURVES

I_{DD} vs V_{DD}

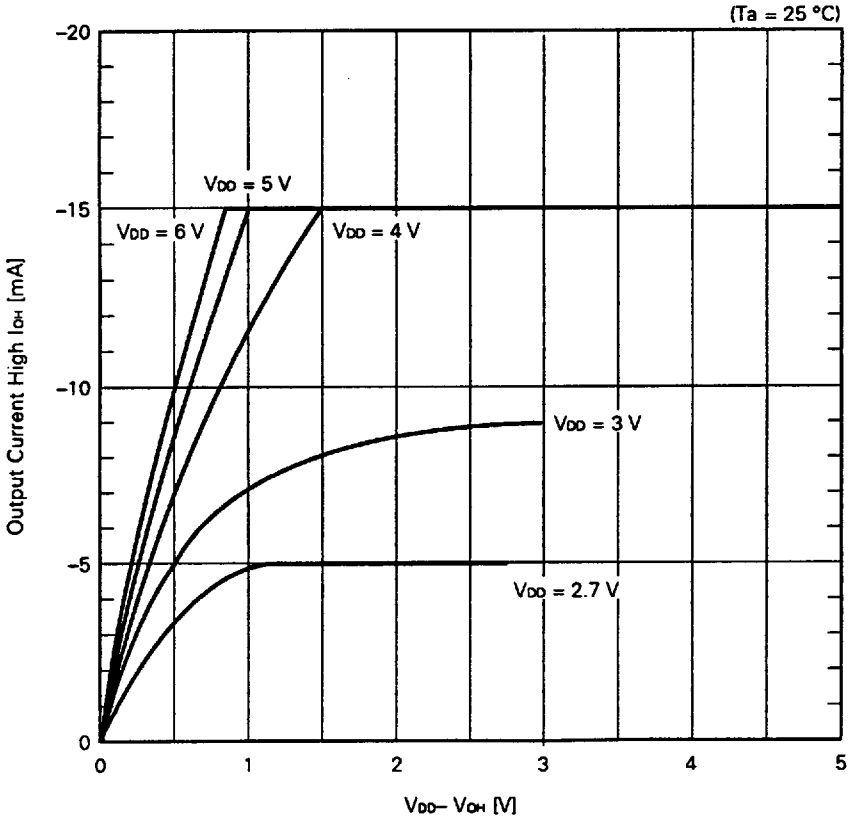


Remarks Values of the processor clock control register (PCC) is indicated in parenthesis.

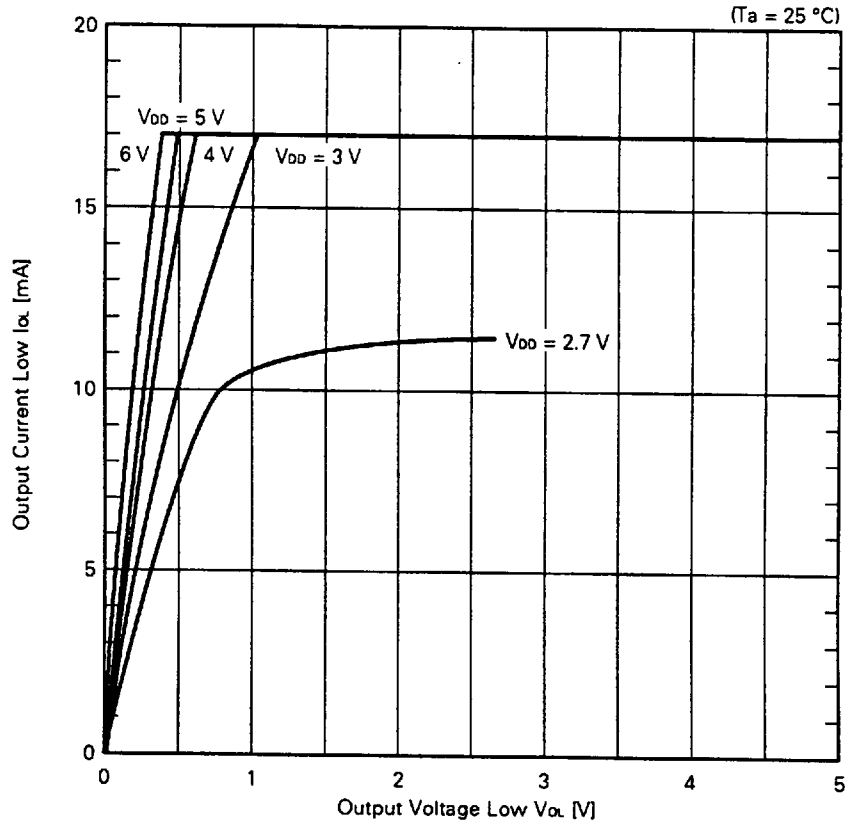
I_{OL} vs V_{OL} (Ports 0, 2, 3, 6)



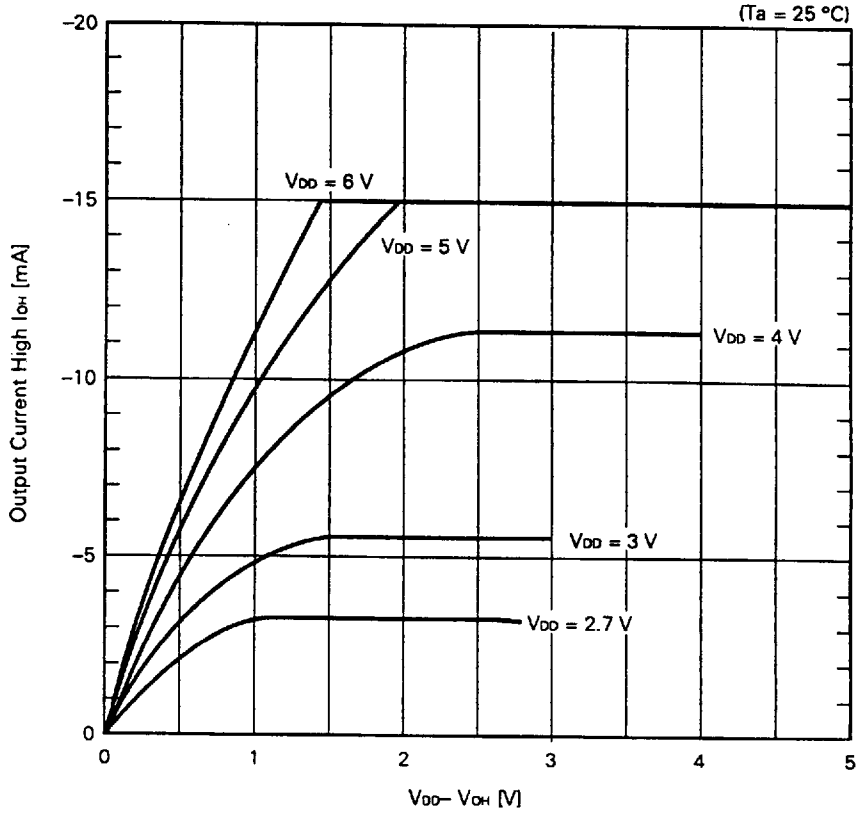
I_{OH} vs (V_{DD} to V_{OH}) (Ports 0, 2, 3, 6)



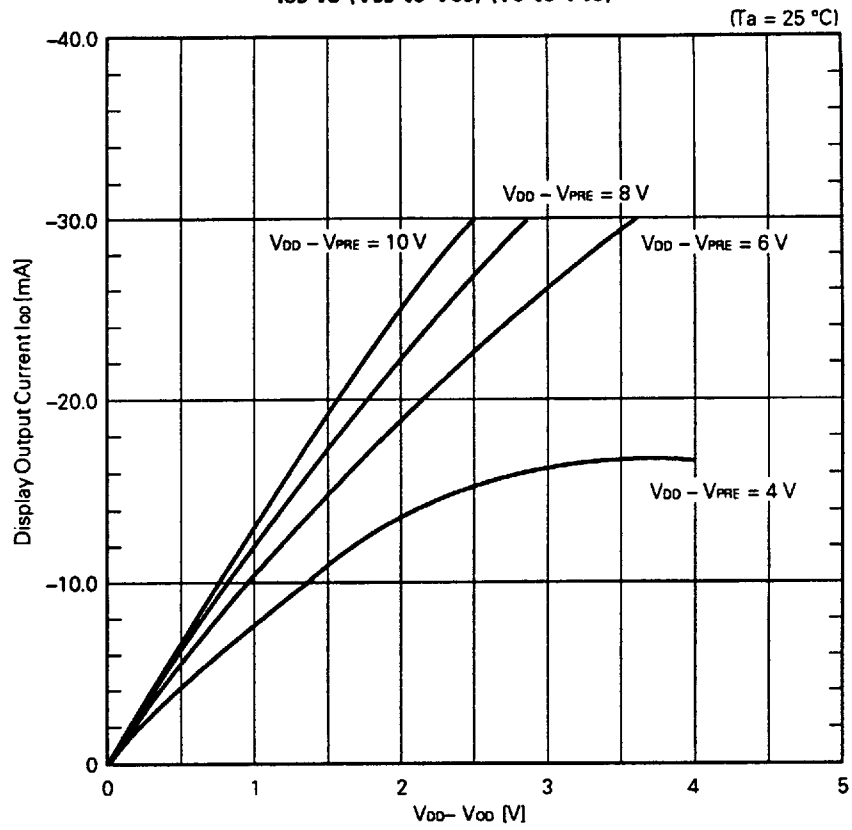
I_{OL} vs V_{OL} (Ports 4, 5)



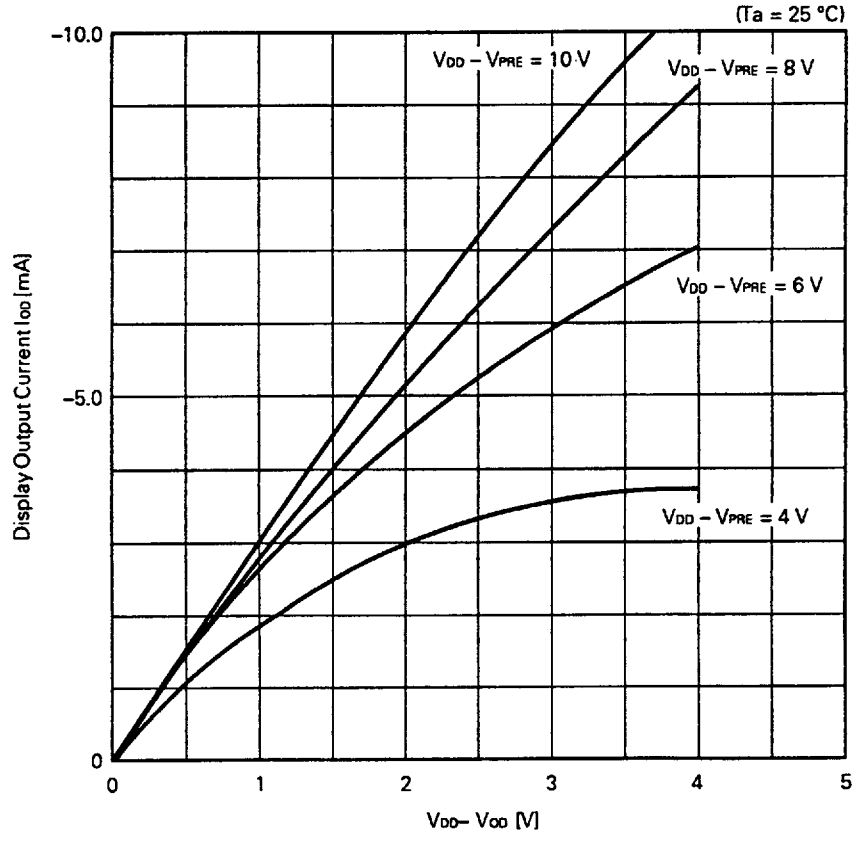
I_{OH} vs (V_{DD} to V_{OH}) (Ports 4, 5)



IOD vs (VDD to VOD) (T0 to T15)

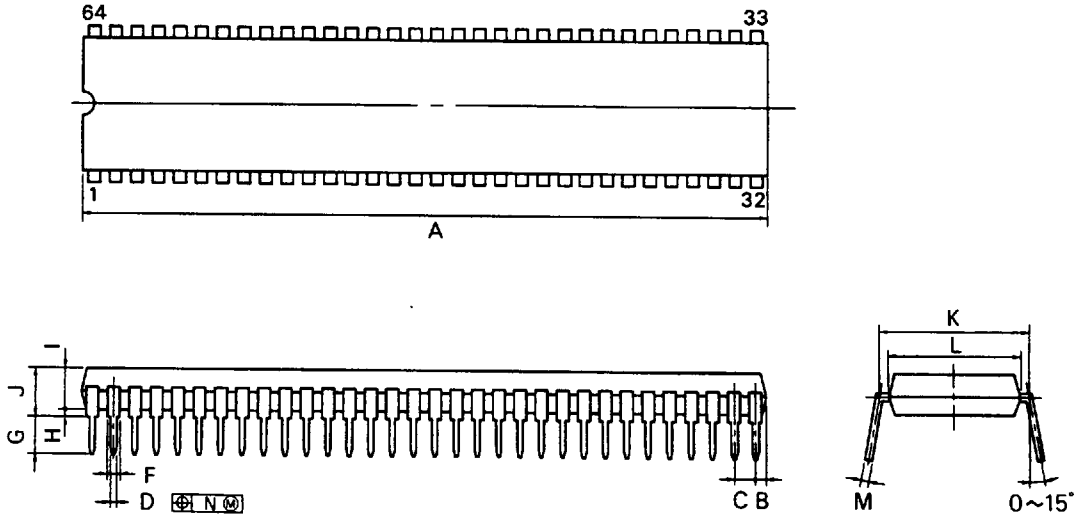


IOD vs (VDD to VOD) (S0 to S9)



14. PACKAGE INFORMATION

64PIN PLASTIC SHRINK DIP (750 mil)



P64C-70-750A,C

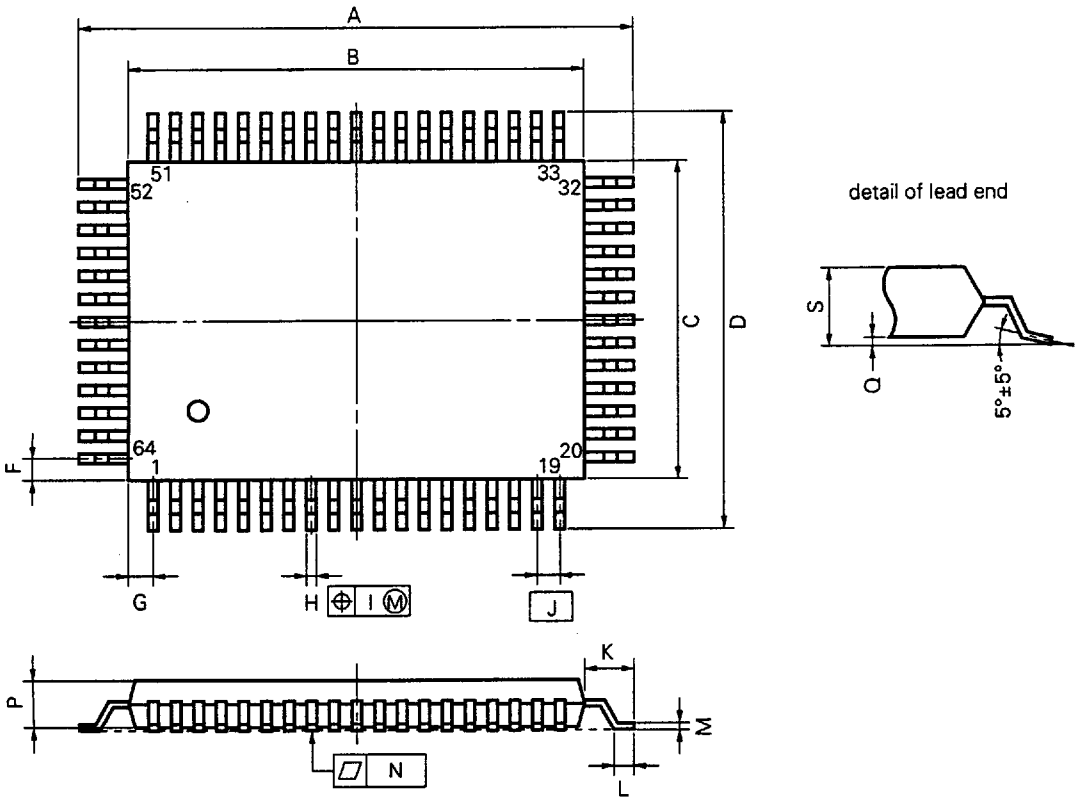
NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.50^{\pm 0.10}$	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	$3.2^{\pm 0.3}$	$0.126^{\pm 0.012}$
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007

64 PIN PLASTIC QFP (14×20)



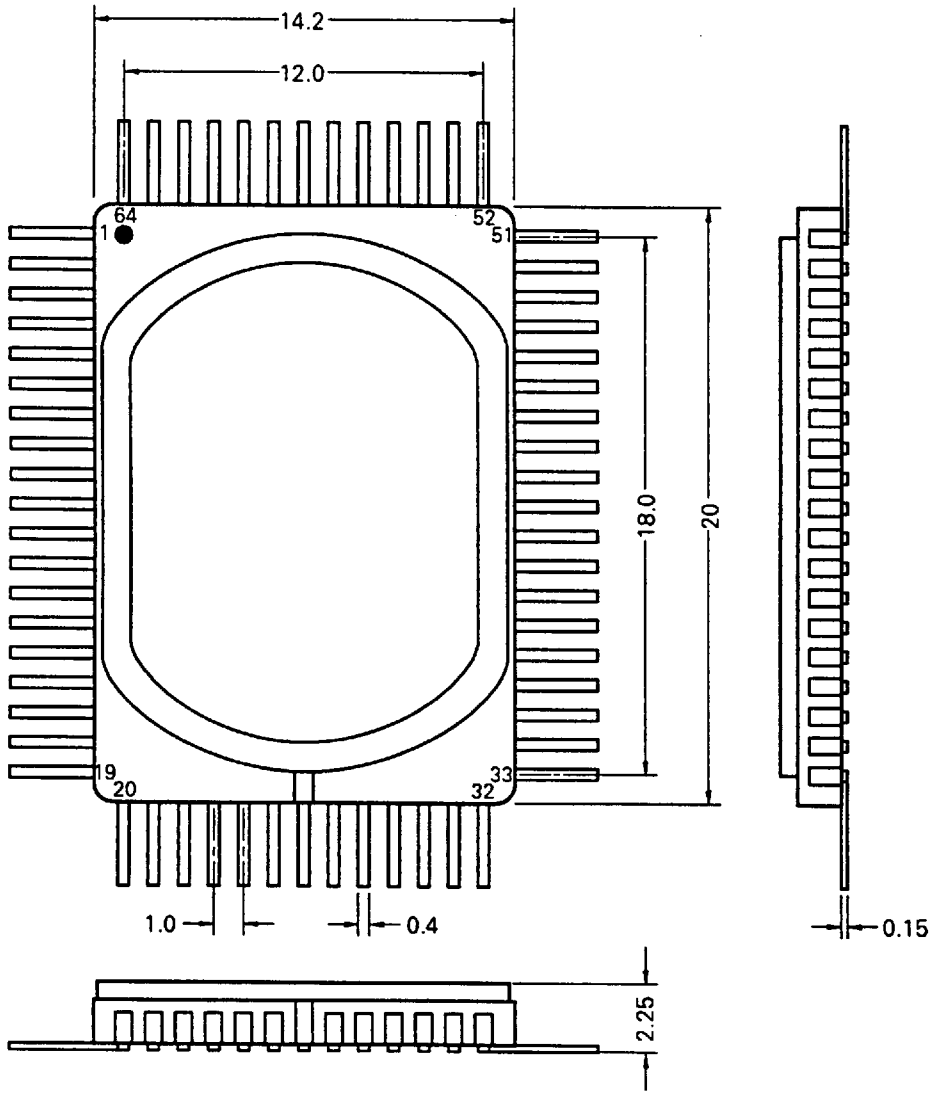
P64GF-100-3B8,3BE,3BR-1

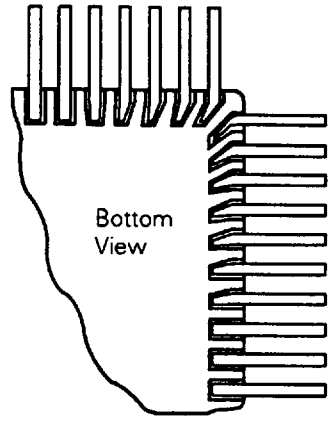
NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

64-pin ceramic QFP for ES (reference) (unit : mm)





Note

1. **Care is needed since the metal cap is connected to pin 26 and set to the positive power supply level.**
2. **Care is needed since the lead of the base is formed obliquely.**
3. **The lead length is not stipulated since the cutting of the lead ends is not progress-controlled.**

★ 15. RECOMMEDED SOLDERING CONDITIONS

This product should be soldered and mounted under the conditions recommended below.

For details of recommended soldering conditions for the surface mounting type, refer to the document **"Semiconductor Device Mount Technology" (IEI-1207).**

For soldering methods and conditions other than those recommended below, contact our salesman.

Table 15-1 Surface Mounting Type Conditions

μPD75206GF-xxx-3BE : 64-pin plastic QFP (body 14 × 20 mm)

Solderring Method	Solderring Conditions	Recommended Condition Symbol
Wave soldering	Solder bath temperature: 260 °C or less, Duration: 10 sec. max., Number of times: Once Preheating temperature : 120 °C max. (package surface temperature)	WS60-00-1
Infrared reflow	Package peak temperature: 230 °C, Duration: 30 sec. max. (at 210 °C or above), Number of times: Once	IR-30-00-1
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max. (at 200 °C or above), Number of times: Once	VP15-00-1
Pin part heating	Pin part temperature: 300 °C or below , Duration: 3 sec. max. (per device side)	—

* For the storage period after dry-pack decompression storage conditions are max. 25 °C, 65 % RH.

Note Use of more than one soldering method should be avoided (except in the case of pin part heating).

Table 15-2 Insertion Type Soldering Conditions

μPD75206CW-xxx : 64-pin plastic shrink DIP (750 mil)

Solderring Method	Solderring Conditions
Wave soldering (lead part only)	Solder bath temperature: 260 °C or below , Duration: 10 sec. max.
Pin part heating	Pin part temperature: 260 °C or below , Duration: 10 sec. max.

Note Ensure that the application of wave soldering is limited to the lead part and no solder touches the main unit directly.

APPENDIX A. DEVELOPMENT TOOLS ★

The following development tools are available for the development of systems using the μPD75206.

Hardware	IE-75000-R *1 IE-75001-R	In-circuit emulator for 75X series
	IE-75000-R-EM*2	Emulation board for IE-75000-R and IE-75001-R
	EP-75216ACW-R	Emulation prove for μPD75216ACW
	EP-75216AGF-R EV-9200G-64	Emulation prov for μPD75216AGF, 64-pin conversion socket EV-9200G-64 is also supplied.
	PG-1500	PROM programmer
	PA-75P216ACW	PROM programmer adapter for μPD75P216ACW and 75P218CW, and is connected to PG-1500.
	PA-75P218GF	PROM programmer adapter for μPD75P218GF, and is connected to PG-1500.
	PA-75P218KB	PROM programmer adapter for μPD75P218KB, and is connected to PG-1500.
Software	IE control program PG-1500 controller RX75X relocatable assembler	Host machine • PC-9800 series (MS-DOS™, Ver. 3.30 to Ver. 5.00A*3) • IBM PC series (PC-DOS ™, Ver. 3.1)

*1 Maintenance products

2 Not provided in IE-75001-R

3 Ver. 5.00/5.00A is provided with task swap function, but this function cannot be used with this software.

★ APPENDIX B. RELATED DOCUMENTS

Documents related on devices

DOCUMENT	DOCUMENT NO.
User's manual	IEM-988
Instruction list	IEM-968
Application note	IEM-989
75X series selection guide	IF-151

Documents related on development tools

	DOCUMENT			DOCUMENT NO.
Hardware	IE-75000-R User's manual			EEU-669
	IE-75001-R User's manual			EEU-846
	IE-75000-R-EM User's manual			EEU-673
	EP-75216ACW-R User's manual			EEU-667
	EP-75216AGF-R User's manual			EEU-668
	PG-15000 User's manual			EEU-651
Software	RA75X assembler package User's manual	Instruction	PC-9800 series (MS-DOS) base IBM PC series (PC DOS) base	EEU-731
		Language		EEU-730
	PG-1500 controller user's manual			EEU-704

Other documents

DOCUMENT	DOCUMENT NO.
Package manual	IEI-635
Semiconductor device - Mounting manual	IEI-616
NEC semiconductor device quality grade	IEI-620
NEC semiconductor device reliability quality control	IEM-5068
Static electricity discharge (ESD) test	MEM-539
Semiconductor device quality guarantee guide	MEI-603
Product guide related on microcomputer - Other manufacturers	MEI-604

Note Be sure to use the latest document for designing.