SHF-0189

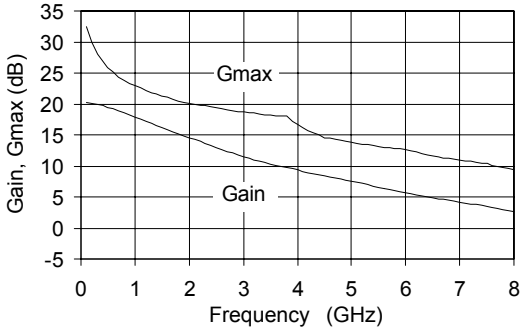
0.05 - 6 GHz, 0.5 Watt GaAs HFET

Product Description

Sirenza Microdevices' SHF-0189 is a high performance AlGaAs/GaAs Heterostructure FET (HFET) housed in a low-cost surface-mount plastic package. The HFET technology improves breakdown voltage while minimizing Schottky leakage current resulting in higher PAE and improved linearity.

Output power at 1dB compression for the SHF-0189 is +27 dBm when biased for Class AB operation at 8V,100mA. The +40 dBm third order intercept makes it ideal for high dynamic range, high intercept point requirements. It is well suited for use in both analog and digital wireless communication infrastructure and subscriber equipment including 3G, cellular, PCS, fixed wireless, and pager systems.

Typical Gain Performance (8V,100mA)



Product Features

- **High Linearity Performance at 1.96 GHz**
  - **+27 dBm P1dB**
  - **+40 dBm Output IP3**
  - **+16.5 dB Gain**
- **High Drain Efficiency**
- **See App Note AN-031 for circuit details**

Applications

- **Analog and Digital Wireless Systems**
- **3G, Cellular, PCS**
- **Fixed Wireless, Pager Systems**

Symbol	Device Characteristics	Test Conditions, 25C V_{DS}=8V, I_{DQ}=100mA (unless otherwise noted)	Test Frequency	Units	Min	Typ	Max
Gmax	Maximum Available Gain	$Z_S=Z_S^*$, $Z_L=Z_L^*$	0.90 GHz 1.96 GHz	dB	-	23.3 20.1	-
S_{21}	Insertion Gain [1]	$Z_S=Z_L$= 50 Ohms	0.90 GHz 1.96 GHz	dB	16.6	18.4 14.7	20.2
Gain	Power Gain [2]	Application Circuit	0.90 GHz 1.96 GHz	dBm	-	18.6 16.7	-
OIP3	Output Third Order Intercept Point [2]	Application Circuit	0.90 GHz 1.96 GHz	dBm	-	40 40	-
P1dB	Output 1dB Compression Point [2]	Application Circuit	0.90 GHz 1.96 GHz	dBm	-	27.2 27.5	-
NF	Noise Figure	Application Circuit	1.96 GHz	dB	-	3.2	-
I_{DSS}	Saturated Drain Current	V_{DS}= V_{DSP}, V_{GS}= 0V		mA	204	294	384
g_m	Tranconductance	V_{DS}= V_{DSP}, V_{GS}= -0.25V		mS	144	198	252
V_P	Pinch-Off Voltage [1]	V_{DS}= 2.0V, I_{DS}= 0.6mA		V	-3.0	-1.9	-1.0
BV_{GS}	Gate-Source Breakdown Voltage [1]	I_{GS}= 1.2mA, drain open		V	-	-17	-15
BV_{GD}	Gate-Drain Breakdown Voltage [1]	I_{GD}= 1.2mA, V_{GS}= -5.0V		V	-	-22	-17
Rth	Thermal Resistance	junction-to-lead		°C/W	-	80	-
V_{DS}	Operating Voltage [3]	drain-source		V	-	-	8.0
I_{DQ}	Operating Current [3]	drain-source, quiescent		mA	-	-	160
P_{DISS}	Power Dissipation [3]			W	-	-	0.8

[1] 100% tested - Insertion gain tested using a 50 ohm contact board (no matching circuitry) during final production test.
[2] Sample tested - Samples pulled from each wafer/package lot. Sample test specifications are based on statistical data from sample test measurements. The test fixture is an engineering application circuit board. The application circuit was designed for the optimum combination of linearity, P1dB, and VSWR.
[3] Maximum recommended power dissipation is specified to maintain T_J<150C at T_L=85C. V_{DS} * I_{DQ}<0.8W is recommended for continuous reliable operation.

522 Almanor Ave., Sunnyvale, CA 94085 Phone: (800) SMI-MMIC http://www.sirenza.com

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Drain Current	I_{DS}	200	mA
Forward Gate Current	I_{GSF}	1.2	mA
Reverse Gate Current	I_{GSR}	1.2	mA
Drain-to-Source Voltage	V_{DS}	+9.0	V
Gate-to-Source Voltage	V_{GS}	<-5 or >0	V
RF Input Power	P_{IN}	200	mW
Operating Lead Temperature	T_L	See Graph	°C
Storage Temperature Range	T_{stor}	-40 to +150	°C
Power Dissipation	P_{DISS}	See Graph	W
Channel Temperature	T_J	+165	°C

Operation of this device beyond any one of these limits may cause permanent damage. For reliable continuous operation, the device voltage and current must not exceed the maximum operating values specified in the table on page 1.

MTTF is inversely proportional to the device junction temperature. For junction temperature and MTTF considerations the bias condition should also satisfy the following expression:

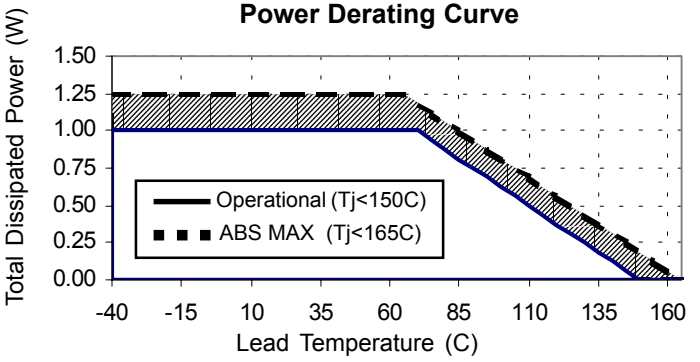
$$P_{DC} < (T_J - T_L) / R_{TH}$$

where:

$P_{DC} = I_{DS} * V_{DS}$ (W)
T_J = Junction Temperature (°C)
T_L = Lead Temperature (pin 4) (°C)
R_{TH} = Thermal Resistance (°C/W)

MTTF @ T_J=150C exceeds 1E7 hours

Power Derating Curve



This area not recommended for continuous reliable operation.

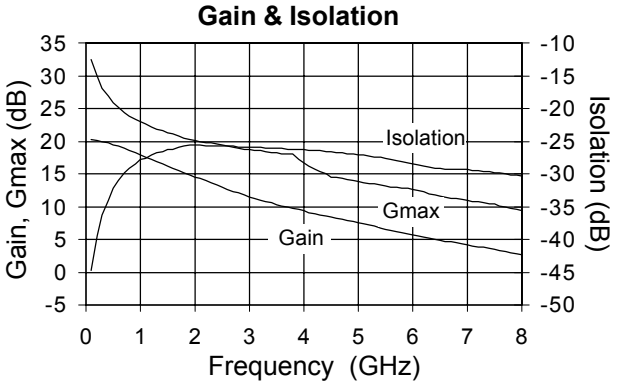
Typical Performance - Engineering Application Circuits (See App Note AN-031)

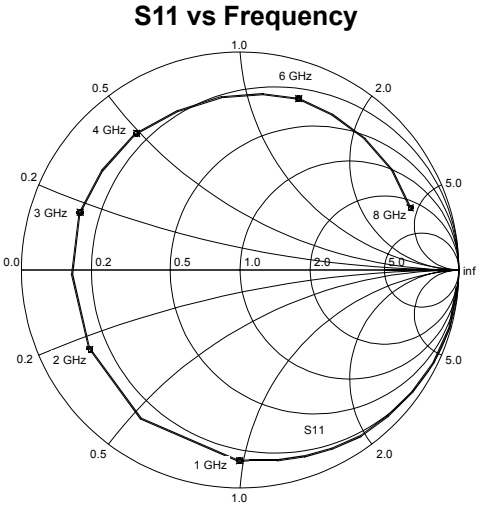
Freq (MHz)	V_{DS} (V)	I_{DQ} (mA)	P1dB (dBm)	OIP3* (dBm)	Gain (dB)	S11 (dB)	S22 (dB)	NF (dB)
900	8	100	27.2	40	18.6	-25	-13	4.7
1960	8	100	27.6	40	16.7	-20	-8	3.2
2140	8	100	27.5	40	15.2	-24	-14	3.8
2450	8	100	27.3	40	15.2	-16	-14	3.1

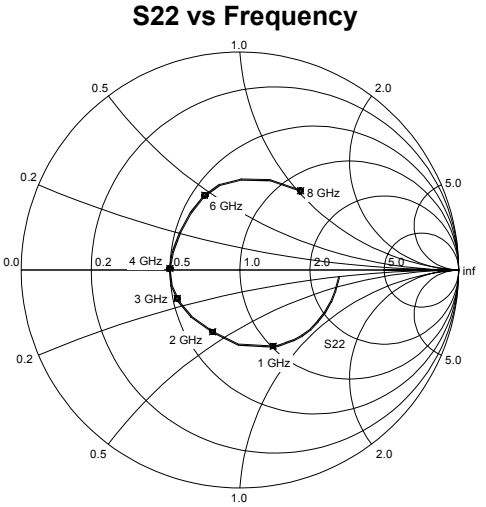
* P_{OUT}= +15dBm per tone, 1MHz tone spacing

Data above represents typical performance of the application circuits noted in Application Note AN-031. Refer to the application note for additional RF data, PCB layouts, and BOMs for each application circuit. The application note also includes biasing instructions and other key issues to be considered. For the latest application notes please visit our site at www.sirenza.com or call your local sales representative.

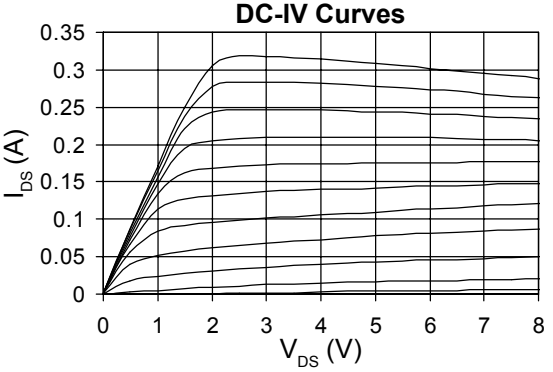
De-embedded S-Parameters (Z_S=Z_L=50 Ohms, V_{DS}=8V, I_{DS}=100mA, 25° C)







Note: S-parameters are de-embedded to the device leads with Z_S=Z_L=50Ω. The data represents typical performace of the device. De-embedded s-parameters can be downloaded from our website (www.sirenza.com).



V_{GS} = -2.0 to 0V, 0.2V steps
T=25°C

Caution: ESD sensitive
Appropriate precautions in handling, packaging and testing devices must be observed.

Pin Description

Pin #	Function	Description
1	Gate	RF Input
2	Source	Connection to ground. Use via holes to reduce lead inductance. Place vias as close to ground leads as possible.
3	Drain	RF Output
4	Source	Same as Pin 2

Part Number Ordering Information

Part Number	Reel Size	Devices/Reel
SHF-0189	7"	1000

Part Symbolization

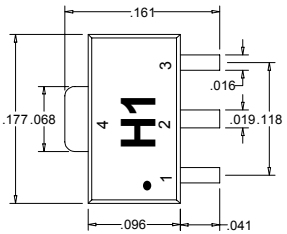
The part will be symbolized with the "H1" designator and a dot signifying pin 1 on the top surface of the package.

Mounting and Thermal Considerations

It is very important that adequate heat sinking be provided to minimize the device junction temperature. The following items should be implemented to maximize MTTF and RF performance.

1. Multiple solder-filled vias are required directly below the ground tab (pin 4). [CRITICAL]
2. Incorporate a large ground pad area with multiple plated-through vias around pin 4 of the device. [CRITICAL]
3. Use two point board seating to lower the thermal resistance between the PCB and mounting plate. Place machine screws as close to the ground tab (pin 4) as possible. [RECOMMENDED]
4. Use 2 ounce copper to improve the PCB's heat spreading capability. [RECOMMENDED]

Package Dimensions



DIMENSIONS ARE IN INCHES

Recommended Mounting Configuration for Optimum RF and Thermal Performance