



# QUAD FUTUREBUS BACKPLANE TRANSCEIVER (3 STATE + OPEN COLLECTOR)

The MC74F3893A is a quad backplane transceiver and is intended to be used in very high speed bus systems.

The MC74F3893A interfaces to "Backplane Transceiver Logic" (BTL). BTL features a reduced (1 V) voltage swing for lower power consumption and a series diode on the drivers to reduce capacitive loading (< 5 pF).

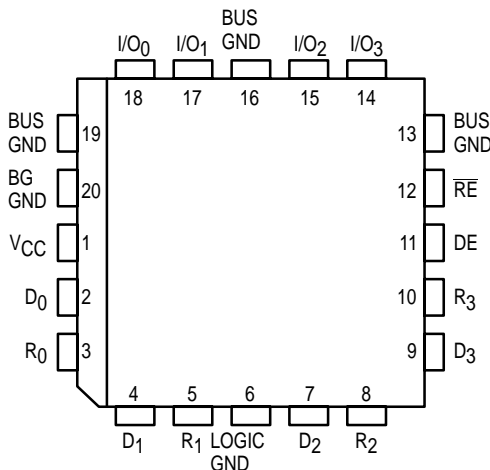
Incident wave switching is employed, therefore BTL propagation delays are short. Although the voltage swing is much less for BTL, so is its receiver threshold region, therefore noise margins are excellent.

BTL offers low power consumption, low ground bounce, reduced EMI and crosstalk, low capacitive loading, superior noise margin and short propagation delays. This results in a high bandwidth, reliable backplane.

The MC74F3893A has four TTL outputs ( $R_n$ ) on the receiver side with a common Receive Enable input ( $\overline{RE}$ ). It has four data inputs ( $D_n$ ) which are also TTL. These data inputs are NANDed with the Data Enable input ( $DE$ ). The four I/O pins (Bus side) are futurebus compatible, sink a minimum of 100 mA, and are designed to drive heavily loaded backplanes with load impedances as low as 10 ohms. All outputs are designed to be glitch-free during power up and power down.

- Quad Backplane Transceiver
- Drives Heavily Loaded Backplanes with Equivalent Load Impedances Down to 10 ohms
- Futurebus Drivers Sink 100 mA
- Reduced Voltage Swing (1 Volt) Produces Less Noise and Reduces Power Consumption
- High Speed Operation Enhances Performance of Backplane Buses and Facilitates Incident Wave Switching
- Compatible with IEEE 896 and IEEE 1194.1 Futurebus Standards
- Built-In Precision Band-Gap (BG) Reference Provides Accurate Receiver Threshold and Improved Noise Immunity
- Glitch-Free Power Up/Power Down Operation On All Outputs
- Pin and Function Compatible with NSC DS3893A and Signetics 74F3893
- Separate Bus Ground Returns for Each Driver to Minimize Ground Noise
- MOS and TTL Compatible High Impedance Inputs

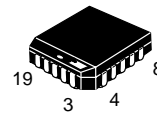
## PINOUT: 20-LEAD PLCC (TOP VIEW)



## MC74F3893A

### QUAD FUTUREBUS BACKPLANE TRANSCEIVER (3 STATE + OPEN COLLECTOR)

FAST™ SCHOTTKY TTL

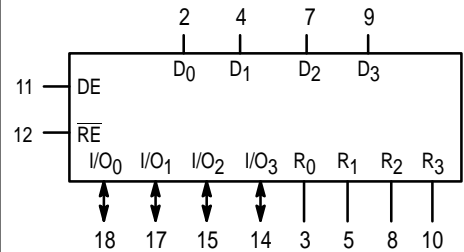


FN SUFFIX  
PLASTIC  
CASE 775-02

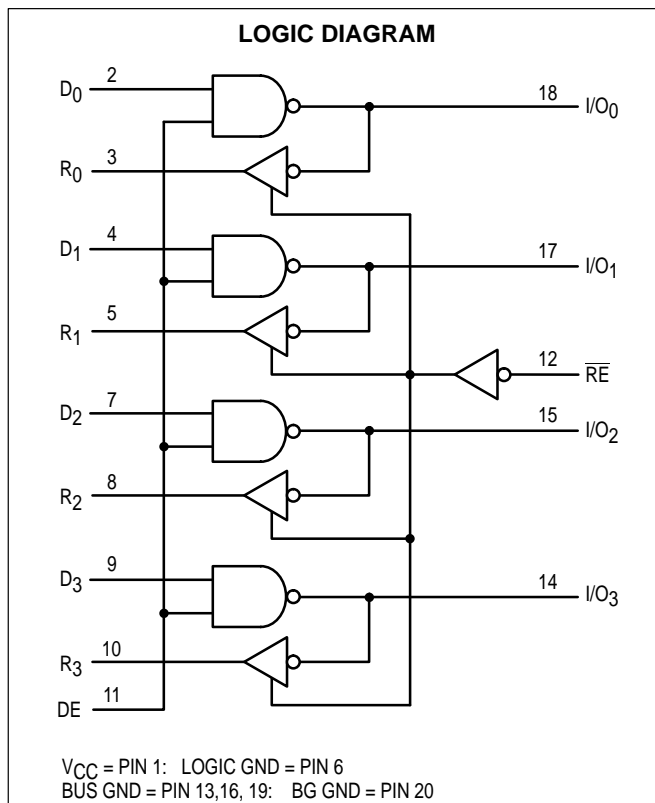
### ORDERING INFORMATION

MC74FXXXXAFN Plastic

### LOGIC SYMBOL



# MC74F3893A



## FUNCTION TABLE

Inputs			Input/Output	Outputs	Operating Mode
DE	RE	$D_n$	$I/O_n$	$R_n$	
H	L	L	H	L	Transmit to Bus
H	L	H	L	H	
H	H	L	$\overline{D_n}$	Z	Receiver 3-State, Transmit to Bus
L	H	H	H	Z	
L	L	X	H	L	Receive, $I/O_n = \text{Inputs}$
L	L	X	L	H	

H = HIGH voltage level:

L = LOW voltage level:

X = Don't care:

Z = HIGH impedance "Off" state.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Limits			Unit
			Min	Typ	Max	
$V_{CC}$	Supply Voltage		4.5	5.0	5.5	V
$V_{IH}$	High-Level Input Voltage	$D_n, DE, RE$	2.0	—	—	V
$V_{IL}$	Low-Level Input Voltage		—	—	0.8	V
$I_{IK}$	Input Clamp Current		—	—	-18	mA
$V_{TH}$	Bus Input Threshold	$I/O_n$ Only	1.475	1.550	1.625	V
$I_{OH}$	Output Current — High	$R_n$ Only	—	—	-3.0	mA
$I_{OL}$	Output Current — Low		—	—	100	mA
$T_A$	Operating Ambient Temperature Range		0	—	70	°C

# MC74F3893A

## DC CHARACTERISTICS (Over Recommended Operating Free-Air Temperature Range Unless otherwise specified)

Symbol	Parameter		Limits			Unit	Test Conditions (Note 1)	
			Min	Typ (2)	Max			
V <sub>OH</sub>	High-Level Output Voltage	R <sub>n</sub>	2.5	—	—	V	V <sub>CC</sub> = MIN: V <sub>IL</sub> = 1.3 V; $\overline{RE}$ = 0.8 V; I <sub>OH</sub> = MAX	
V <sub>OHB</sub>	High-Level Output Bus Voltage	I/O <sub>n</sub>	1.9	—	—	V	V <sub>CC</sub> = MAX: DN = DE = 0.8 V; V <sub>T</sub> = 2.0 V; R <sub>T</sub> = 10Ω; $\overline{RE}$ = 2.0 V; I <sub>OH</sub> = MAX	
V <sub>OL</sub>	Output LOW Voltage	R <sub>n</sub>	—	0.35	0.5	V	V <sub>CC</sub> = MIN: V <sub>IN</sub> = 1.8 V; $\overline{RE}$ = 0.8 V; I <sub>OL</sub> = 6.0 mA	
V <sub>OLB</sub>	Low Level Output Bus Voltage	I/O <sub>n</sub>	0.75	1.0	1.2	V	D <sub>n</sub> = DE = V <sub>IH</sub> ; I <sub>OL</sub> = 100 mA	
			0.75	1.0	1.1		D <sub>n</sub> = DE = V <sub>IH</sub> ; I <sub>OL</sub> = 80 mA	
V <sub>OCB</sub>	Driver Output Positive Clamp Voltage	I/O <sub>n</sub>	—	—	2.9	V	V <sub>CC</sub> = MAX or 0 V: DN = DE = 0.8 V; $\overline{RE}$ = 2.0 V	I/O <sub>n</sub> = 1.0 mA
			—	—	3.2			I/O <sub>n</sub> = 10 mA
V <sub>IK</sub>	Input Clamp Diode Voltage		—	-0.73	-1.2	V	V <sub>CC</sub> = MIN, I <sub>I</sub> = I <sub>IK</sub>	
I <sub>I</sub>	Input Current at Maximum Input Voltage		—	—	100	μA	V <sub>CC</sub> = MAX: V <sub>I</sub> = 7.0 V: DE = $\overline{RE}$ = D <sub>n</sub> = V <sub>CC</sub>	
I <sub>IH</sub>	High Level Input Current	D <sub>n</sub> , $\overline{RE}$ , DE	—	—	20	μA	V <sub>CC</sub> = MAX: DE = $\overline{RE}$ = D <sub>n</sub> = 2.5 V	
I <sub>IHB</sub>	High-Level I/O Bus Current (Power Off)	I/O <sub>n</sub>	—	—	100	μA	V <sub>CC</sub> = 0 V: DN = DE = 0.8 V; I/O <sub>n</sub> = 1.2 V; $\overline{RE}$ = 0 V:	
I <sub>IL</sub>	Low-Level Input Current	$\overline{RE}$	—	—	-100	μA	V <sub>CC</sub> = MAX:	DE = 4.5 V
		D <sub>n</sub>	—	—	-200			V <sub>I</sub> = 0.5V:
		DE	—	—	-500			
I <sub>ILB</sub>	Low-Level I/O Bus Current (Power On)	I/O <sub>n</sub>	-250	—	100	μA	V <sub>CC</sub> = MAX: D <sub>n</sub> = DE = 0.8 V; I/O <sub>n</sub> = 0.75 V; $\overline{RE}$ = 0 V:	
I <sub>OZH</sub>	Off-State Output Current, High-Level Voltage Applied	R <sub>n</sub>	—	—	20	μA	V <sub>O</sub> = 2.5V; $\overline{RE}$ = 2.0 V	V <sub>CC</sub> = MAX:
I <sub>OZL</sub>	Off-State Output Current, Low-Level Voltage Applied		—	—	-20		V <sub>CC</sub> = MAX: V <sub>O</sub> = 0.5 V; $\overline{RE}$ = 2.0 V	
I <sub>OS</sub>	Output Short Circuit Current (Note 3)		-80	—	-200		mA	
I <sub>CC</sub>	Supply Current (Total)		—	55	80	mA	V <sub>CC</sub> = MAX: ( $\overline{RE}$ = V <sub>IH</sub> or V <sub>IL</sub> )	

**NOTES:**

- For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
- All typical values are at V<sub>CC</sub> = 5.0 V, T<sub>A</sub> = + 25°C.
- Not more than one output should be shorted at a time. For testing I<sub>OS</sub>, the use of high-speed test apparatus and/or sample-and-hold techniques are preferable in order to minimize internal heating and more accurately reflect operational values. Otherwise, prolonged shorting of a High output may raise the chip temperature well above normal and thereby cause invalid readings in other parameter tests. In any sequence of parameter tests, I<sub>OS</sub> tests should be performed last.

# MC74F3893A

## AC ELECTRICAL CHARACTERISTICS for Receiver and Receiver Enable

Symbol	Parameter	74F			74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ , $V_T = +2.0\text{V}$ $C_D = 30\text{ pF}$ $R_T = 10\ \Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ , $V_T = +2.0\text{V}$ $C_D = 30\text{ pF}$ $R_T = 10\ \Omega$		
		Min	Typ	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $D_n$ to $I/O_n$	—	—	—	1.0	7.0	ns
$t_{PLH}$ $t_{PHL}$	Propagation Delay DE to $I/O_n$	—	—	—	1.0	7.0	ns
$t_{TLH}$ $t_{THL}$	$D_n$ to $I/O_n$ Transition Time 10% to 90%, 90% to 10%	—	—	—	1.0	5.0	ns
$t_{Dskew}$	Skew Between Receivers in Same Package	—	1.0	—	—	—	ns

## AC ELECTRICAL CHARACTERISTICS for Receiver

Symbol	Parameter	74F			74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ $R_L = 1.0\text{K}\ \Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 1.0\text{K}\ \Omega$		
		Min	Typ	Max	Min	Max	
$t_{PLH}$ $t_{PHL}$	Propagation Delay $I/O_n$ to $R_n$	—	—	—	2.0	8.0	ns
$t_{Dskew}$	Skew Between Receivers in Same Package	—	1.0	—	—	—	ns

## AC ELECTRICAL CHARACTERISTICS for Receiver Enable

Symbol	Parameter	74F			74F		Unit
		$T_A = +25^\circ\text{C}$ $V_{CC} = +5.0\text{V}$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$			$T_A = 0^\circ\text{C to } +70^\circ\text{C}$ $V_{CC} = +5.0\text{V} \pm 10\%$ $C_L = 50\text{ pF}$ $R_L = 500\ \Omega$		
		Min	Typ	Max	Min	Max	
$t_{PZH}$ $t_{PZL}$	Output Enable to High or Low Level $\overline{RE}$ to $R_n$	—	—	—	2.0	12.0	ns
$t_{PHZ}$ $t_{PLZ}$	Output Disable From High or Low Level $\overline{RE}$ to $R_n$	—	—	—	1.0	8.0	ns

