



400ksp/300ksp, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

General Description

The MAX1284/MAX1285 12-bit analog-to-digital converters (ADCs) combine a high-bandwidth track/hold (T/H), a serial interface with high conversion speed, an internal +2.5V reference, and low power consumption. The MAX1284 operates from a single +4.5V to +5.5V supply; the MAX1285 operates from a single +2.7V to +3.6V supply.

The 3-wire serial interface connects directly to SPI™/QSPI™/MICROWIRE™ devices without external logic. The devices use an external serial-interface clock to perform successive-approximation analog-to-digital conversions.

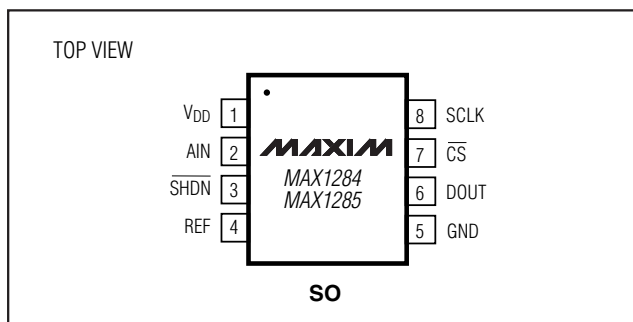
Low power, ease of use, and small package size make these converters ideal for remote-sensor and data-acquisition applications or for other circuits with demanding power consumption and space requirements. The MAX1284/MAX1285 are available in 8-pin SO packages.

These devices are pin-compatible, higher-speed versions of the MAX1240/MAX1241; for more information, refer to the respective data sheets.

Applications

Portable Data Logging
Data Acquisition
Medical Instruments
Battery-Powered Instruments
Pen Digitizers
Process Control

Pin Configuration



SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Features

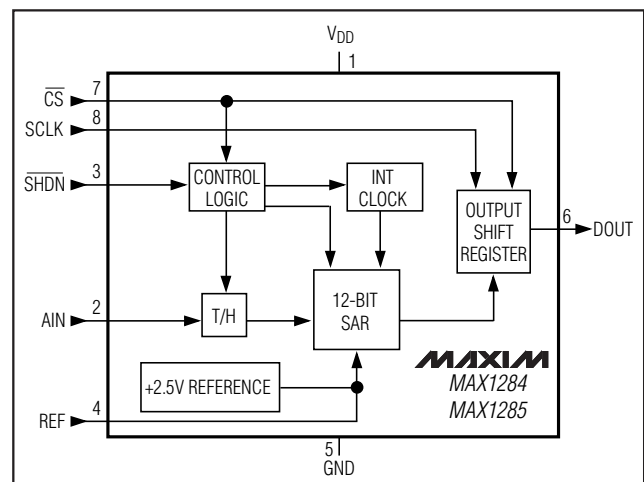
- ◆ Single-Supply Operation
 - +4.5V to +5.5V (MAX1284)
 - +2.7V to +3.6V (MAX1285)
- ◆ ± 1 LSB (max) DNL, ± 1 LSB (max) INL
- ◆ 400ksp Sampling Rate (MAX1284)
- ◆ Internal Track/Hold
- ◆ Internal +2.5V Reference
- ◆ Low Power: 2.5mA (400ksp)
- ◆ SPI/QSPI/MICROWIRE 3-Wire Serial Interface
- ◆ Pin-Compatible, High-Speed Upgrades to MAX1240/MAX1241
- ◆ 8-Pin SO Package

Ordering Information

| PART | TEMP. RANGE | PIN-PACKAGE | SUPPLY VOLTAGE (V) |
|--------------|----------------|-------------|--------------------|
| MAX1284BCSA | 0°C to +70°C | 8 SO | 5 |
| MAX1284BESA* | -40°C to +85°C | 8 SO | 5 |
| MAX1285BCSA | 0°C to +70°C | 8 SO | 2.7 to 3.6 |
| MAX1285BESA | -40°C to +85°C | 8 SO | 2.7 to 3.6 |

*Future product—contact factory for availability.

Functional Diagram



400ksp/300ksp, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

ABSOLUTE MAXIMUM RATINGS

| | |
|---|-----------------------------------|
| V _{DD} to GND | -0.3V to +6V |
| AIN to GND | -0.3V to (V _{DD} + 0.3V) |
| REF to GND | -0.3V to (V _{DD} + 0.3V) |
| Digital Inputs to GND..... | -0.3V to +6V |
| DOUT to GND..... | -0.3V to (V _{DD} + 0.3V) |
| DOUT Current..... | ±25mA |
| Continuous Power Dissipation (T _A = +70°C) | |
| 8-Pin SO (derate 5.88mW/°C above +70°C) | 471mW |

| | |
|--|-----------------|
| Operating Temperature Ranges | |
| MAX1284BCSA/MAX1285BCSA | 0°C to +70°C |
| MAX1284BESA/MAX1285BESA | -40°C to +85°C |
| Storage Temperature Range..... | -60°C to +150°C |
| Lead Temperature (soldering, 10s)..... | +300°C |

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS—MAX1284

(V_{DD} = +4.5V to +5.5V; f_{SCLK} = 6.4MHz, 50% duty cycle, 16 clocks/conversion cycle (400ksp); 4.7µF capacitor at REF, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------|---|-----|------|------|--------|
| DC ACCURACY (Note 1) | | | | | | |
| Resolution | | | 12 | | | Bits |
| Relative Accuracy (Note 2) | INL | | | | ±1.0 | LSB |
| Differential Nonlinearity | DNL | No missing codes over temperature | | | ±1.0 | LSB |
| Offset Error | | | | | ±6.0 | LSB |
| Gain Error (Note 3) | | | | | ±6.0 | LSB |
| Gain Error Temperature Coefficient | | | | ±0.8 | | ppm/°C |
| DYNAMIC SPECIFICATIONS (100kHz sine wave, 2.5Vp-p, clock = 6.4MHz) | | | | | | |
| Signal-to-Noise Plus Distortion Ratio | SINAD | | | 70 | | dB |
| Total Harmonic Distortion | THD | Up to the 5th harmonic | | -80 | | dB |
| Spurious-Free Dynamic Range | SFDR | | | 80 | | dB |
| Intermodulation Distortion | IMD | f _{IN1} = 99Hz, f _{IN2} = 102Hz | | 76 | | dB |
| Full-Power Bandwidth | | -3dB point | | 6 | | MHz |
| Full-Linear Bandwidth | | SINAD > 68dB | | 350 | | kHz |
| CONVERSION RATE | | | | | | |
| Conversion Time (Note 4) | t _{CONV} | | 2.5 | | | µs |
| Track/Hold Acquisition Time | t _{ACQ} | | | | 468 | ns |
| Aperture Delay | | | | 10 | | ns |
| Aperture Jitter | | | | <50 | | ps |
| Serial Clock Frequency | f _{SCLK} | | 0.5 | | 6.4 | MHz |
| Duty Cycle | | | 40 | | 60 | % |
| ANALOG INPUT (AIN) | | | | | | |
| Input Voltage Range | V _{AIN} | | 0 | | 2.5 | V |
| Input Capacitance | | | | 18 | | pF |

400ksps/300ksps, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

MAX1284/MAX1285

ELECTRICAL CHARACTERISTICS—MAX1284 (continued)

($V_{DD} = +4.5V$ to $+5.5V$; $f_{SCLK} = 6.4MHz$, 50% duty cycle, 16 clocks/conversion cycle (400ksps); 4.7 μF capacitor at REF, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|--------------|---|------|-----------|-----------|-----------------|
| INTERNAL REFERENCE | | | | | | |
| REF Output Voltage | V_{REF} | $T_A = +25^\circ C$ | 2.48 | 2.50 | 2.52 | V |
| REF Short-Circuit Current | | | | 30 | | mA |
| REF Output Tempco | TC V_{REF} | | | ± 15 | | ppm/ $^\circ C$ |
| Load Regulation (Note 5) | | 0 to 1mA output load | | 0.1 | 2.0 | mV/mA |
| Capacitive Bypass at REF | | | 4.7 | | 10 | μF |
| DIGITAL INPUTS (SCLK, \overline{CS} , \overline{SHDN}) | | | | | | |
| Input High Voltage | V_{INH} | | 3.0 | | | V |
| Input Low Voltage | V_{INL} | | | | 0.8 | V |
| Input Hysteresis | V_{HYST} | | | 0.2 | | V |
| Input Leakage | I_{IN} | $V_{IN} = 0$ or V_{DD} | | | ± 1 | μA |
| Input Capacitance | C_{IN} | | | 15 | | pF |
| DIGITAL OUTPUT (DOUT) | | | | | | |
| Output Voltage Low | V_{OL} | $I_{SINK} = 5mA$ | | | 0.4 | V |
| Output Voltage High | V_{OH} | $I_{SOURCE} = 1mA$ | 4 | | | V |
| Three-State Leakage Current | I_L | $\overline{CS} = 5V$ | | | ± 10 | μA |
| Three-State Output Capacitance | C_{OUT} | $\overline{CS} = 5V$ | | 15 | | pF |
| POWER SUPPLY | | | | | | |
| Positive Supply Voltage (Note 6) | V_{DD} | | 4.5 | | 5.5 | V |
| Positive Supply Current (Note 7) | I_{DD} | $V_{DD} = 5.5V$ | | 2.5 | 4.0 | mA |
| Shutdown Supply Current | I_{SHDN} | $SCLK = V_{DD}$, $\overline{SHDN} = GND$ | | 2 | 10 | μA |
| Power-Supply Rejection | PSR | $V_{DD} = 5V \pm 10\%$, midscale input | | ± 0.5 | ± 2.0 | mV |

ELECTRICAL CHARACTERISTICS—MAX1285

($V_{DD} = +2.7V$ to $+3.6V$; $f_{SCLK} = 4.8MHz$, 50% duty cycle, 16 clocks/conversion cycle (300ksps); 4.7 μF capacitor at REF, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|------------------------------------|--------|-----------------------------------|-----|-----------|-----------|-----------------|
| DC ACCURACY (Note 1) | | | | | | |
| Resolution | | | 12 | | | Bits |
| Relative Accuracy (Note 2) | INL | | | | ± 1.0 | LSB |
| Differential Nonlinearity | DNL | No missing codes over temperature | | | ± 1.0 | LSB |
| Offset Error | | | | | ± 6.0 | LSB |
| Gain Error (Note 3) | | | | | ± 6.0 | LSB |
| Gain Error Temperature Coefficient | | | | ± 1.6 | | ppm/ $^\circ C$ |

400ksps/300ksps, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

ELECTRICAL CHARACTERISTICS—MAX1285 (continued)

($V_{DD} = +2.7V$ to $+3.0V$; $f_{SCLK} = 4.8MHz$, 50% duty cycle, 16 clocks/conversion cycle (300ksps); $4.7\mu F$ capacitor at REF, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted. Typical values are at $T_A = +25^\circ C$.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|--------------|--|----------------|-----------|-----------|-----------------|
| DYNAMIC SPECIFICATIONS (75kHz sine wave, 2.5Vp-p, $f_{SAMPLE} = 300ksps$, $f_{SCLK} = 4.8MHz$) | | | | | | |
| Signal-to-Noise Plus Distortion Ratio | SINAD | | | 70 | | dB |
| Total Harmonic Distortion | THD | Up to the 5th harmonic | | -80 | | dB |
| Spurious-Free Dynamic Range | SFDR | | | 80 | | dB |
| Intermodulation Distortion | IMD | $f_{IN1} = 73kHz$, $f_{IN2} = 77kHz$ | | 76 | | dB |
| Full-Power Bandwidth | | -3dB point | | 3 | | MHz |
| Full-Linear Bandwidth | | SINAD > 68dB | | 250 | | kHz |
| CONVERSION RATE | | | | | | |
| Conversion Time (Note 4) | t_{CONV} | | 3.3 | | | μs |
| Track/Hold Acquisition Time | t_{ACQ} | | | | 625 | ns |
| Aperture Delay | | | | 10 | | ns |
| Aperture Jitter | | | | <50 | | ps |
| Serial Clock Frequency | f_{SCLK} | | 0.5 | | 4.8 | MHz |
| Duty Cycle | | | 40 | | 60 | % |
| ANALOG INPUT (AIN) | | | | | | |
| Input Voltage Range | V_{AIN} | | 0 | | 2.5 | V |
| Input Capacitance | C_{IN} | | | 18 | | pF |
| INTERNAL REFERENCE | | | | | | |
| REF Output Voltage | V_{REF} | $T_A = +25^\circ C$ | 2.48 | 2.50 | 2.52 | V |
| REF Short-Circuit Current | | | | 15 | | mA |
| REF Output Tempco | TC V_{REF} | | | ± 15 | | ppm/ $^\circ C$ |
| Load Regulation (Note 5) | | 0 to 0.75mA output load | | 0.1 | 2.0 | mV/mA |
| Capacitive Bypass at REF | | | 4.7 | | 10 | mV/mA |
| DIGITAL INPUTS (\overline{SCLK} , \overline{CS} , \overline{SHDN}) | | | | | | |
| Input High Voltage | V_{INH} | | 2.0 | | | V |
| Input Low Voltage | V_{INL} | | | | 0.8 | V |
| Input Hysteresis | V_{HYST} | | | 0.2 | | V |
| Input Leakage | I_{IN} | $V_{IN} = 0$ or V_{DD} | | | ± 1 | μA |
| Input Capacitance | C_{IN} | | | 15 | | μF |
| DIGITAL OUTPUTS (DOUT) | | | | | | |
| Output Voltage Low | V_{OL} | $I_{SINK} = 5mA$ | | | 0.4 | V |
| Output Voltage High | V_{OH} | $I_{SOURCE} = 0.5mA$ | $V_{DD} - 0.5$ | | | V |
| Three-State Leakage Current | I_L | $\overline{CS} = 3V$ | | | ± 10 | μA |
| Three-State Output Capacitance | C_{OUT} | $\overline{CS} = 3V$ | | 15 | | pF |
| POWER SUPPLY | | | | | | |
| Positive Supply Voltage (Note 6) | V_{DD} | | 2.7 | | 3.6 | V |
| Positive Supply Current (Note 7) | I_{DD} | $V_{DD} = 3.6V$ | | 2.5 | 3.5 | mA |
| Shutdown Supply Current | I_{SHDN} | $SCLK = V_{DD}$, $\overline{SHDN} = GND$ | | 2 | 10 | μA |
| Power-Supply Rejection | PSR | $V_{DD} = 2.7V$ to $3.6V$, midscale input | | ± 0.5 | ± 2.0 | mV |

400ksp/300ksp, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

MAX1284/MAX1285

TIMING CHARACTERISTICS—MAX1284 (Figures 1, 2, 8, 9)

($V_{DD} = +4.5V$ to $+5.5V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------------|--------------------------|-----|-----|-----|-------|
| SCLK Period | t _{CP} | | 156 | | | ns |
| SCLK Pulse Width High | t _{CH} | | 62 | | | ns |
| SCLK Pulse Width Low | t _{CL} | | 62 | | | ns |
| \overline{CS} Fall to SCLK Rise Setup | t _{CSS} | | 35 | | | ns |
| SCLK Rise to \overline{CS} Rise Hold | t _{CSH} | | 0 | | | ns |
| SCLK Rise to \overline{CS} Fall Ignore | t _{CSO} | | 35 | | | ns |
| \overline{CS} Rise to SCLK Rise Ignore | t _{CS1} | | 35 | | | ns |
| SCLK Rise to DOUT Hold | t _{DOH} | C _{LOAD} = 20pF | 10 | | | ns |
| SCLK Rise to DOUT Valid | t _{DOV} | C _{LOAD} = 20pF | | | 80 | ns |
| \overline{CS} Rise to DOUT Disable | t _{DOD} | C _{LOAD} = 20pF | 10 | | 65 | ns |
| \overline{CS} Fall to DOUT Enable | t _{DOE} | C _{LOAD} = 20pF | | | 65 | ns |
| \overline{CS} Pulse Width High | t _{CSW} | | 100 | | | ns |

TIMING CHARACTERISTICS—MAX1285 (Figures 1, 2, 8, 9)

($V_{DD} = +2.7V$ to $+3.6V$, $T_A = T_{MIN}$ to T_{MAX} , unless otherwise noted.)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|------------------|--------------------------|-----|-----|-----|-------|
| SCLK Period | t _{CP} | | 208 | | | ns |
| SCLK Pulse Width High | t _{CH} | | 83 | | | ns |
| SCLK Pulse Width Low | t _{CL} | | 83 | | | ns |
| \overline{CS} Fall to SCLK Rise Setup | t _{CSS} | | 45 | | | ns |
| SCLK Rise to \overline{CS} Rise Hold | t _{CSH} | | 0 | | | ns |
| SCLK Rise to \overline{CS} Fall Ignore | t _{CSO} | | 45 | | | ns |
| \overline{CS} Rise to SCLK Rise Ignore | t _{CS1} | | 45 | | | ns |
| SCLK Rise to DOUT Hold | t _{DOH} | C _{LOAD} = 20pF | 13 | | | ns |
| SCLK Rise to DOUT Valid | t _{DOV} | C _{LOAD} = 20pF | | | 100 | ns |
| \overline{CS} Rise to DOUT Disable | t _{DOD} | C _{LOAD} = 20pF | 13 | | 85 | ns |
| \overline{CS} Fall to DOUT Enable | t _{DOE} | C _{LOAD} = 20pF | | | 85 | ns |
| \overline{CS} Pulse Width High | t _{CSW} | | 100 | | | ns |

Note 1: Tested at $V_{DD} = V_{DD,MIN}$.

Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after the full-scale range has been calibrated.

Note 3: Internal reference, offset, and reference errors nulled.

Note 4: Conversion time is defined as the number of clock cycles multiplied by the clock period; clock has 50% duty cycle.

Note 5: External load should not change during conversion for specified accuracy. Guaranteed specification limit of 2mV/mA due to production test limitations.

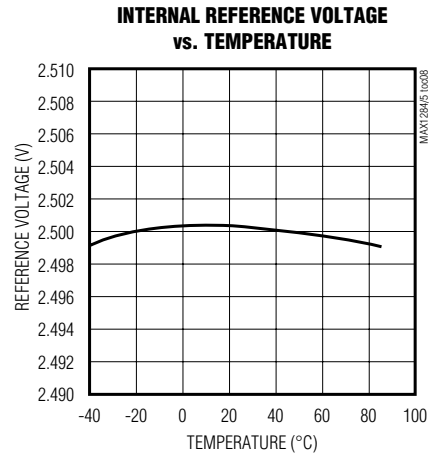
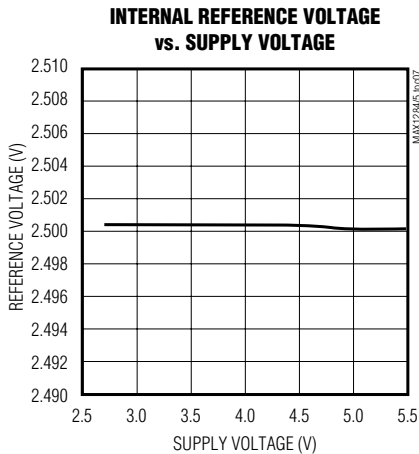
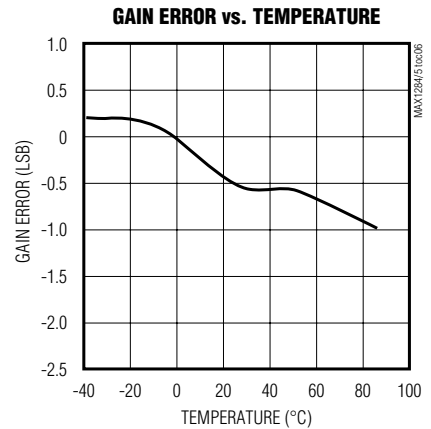
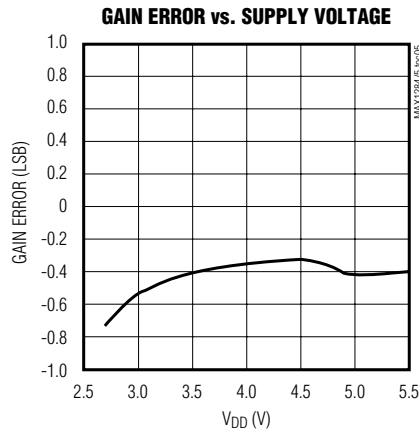
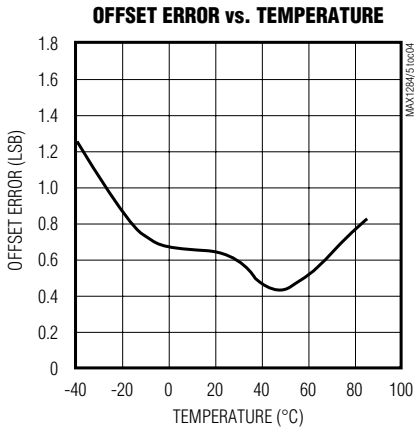
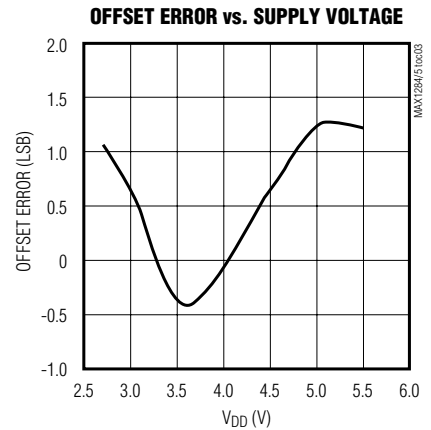
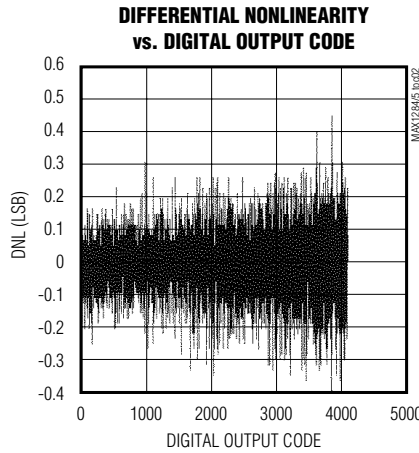
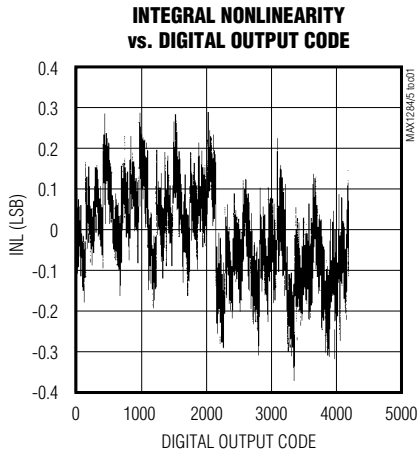
Note 6: Electrical characteristics are guaranteed from $V_{DD,MIN}$ to $V_{DD,MAX}$. For operations beyond this range, see *Typical Operating Characteristics*.

Note 7: MAX1284 tested with 20pF on DOUT and $f_{SCLK} = 6.4MHz$, 0 to 5V. MAX1285 tested with same loads, $f_{SCLK} = 4.8MHz$, 0 to 3V. DOUT = full scale.

400kps/300kps, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

Typical Operating Characteristics

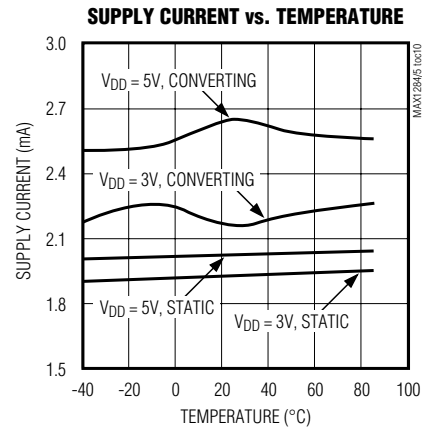
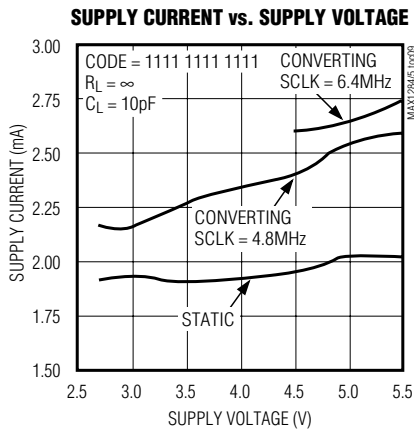
(MAX1284: $V_{DD} = +5.0V$, $f_{SCLK} = 6.4MHz$; MAX1285: $V_{DD} = +3.0V$, $f_{SCLK} = 4.8MHz$; $C_{LOAD} = 20pF$, $4.7\mu F$ capacitor at REF, $T_A = +25^\circ C$, unless otherwise noted.)



400ksp/300ksp, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

Typical Operating Characteristics (continued)

(MAX1284: $V_{DD} = +5.0V$, $f_{SCLK} = 6.4MHz$; MAX1285: $V_{DD} = +3.0V$, $f_{SCLK} = 4.8MHz$; $C_{LOAD} = 20pF$, $4.7\mu F$ capacitor at REF, $T_A = +25^\circ C$, unless otherwise noted.)



MAX1284/MAX1285

Pin Description

| PIN | NAME | FUNCTION |
|-----|-------------------|--|
| 1 | V_{DD} | Positive Supply Voltage |
| 2 | AIN | Sampling Analog Input, 0 to V_{REF} range |
| 3 | \overline{SHDN} | Active-Low Shutdown Input. Pulling \overline{SHDN} low shuts down the device and reduces the supply current to $2\mu A$ (typ). |
| 4 | REF | Reference Voltage for Analog-to-Digital Conversion. Internal 2.5V reference output. Bypass with $4.7\mu F$ capacitor. |
| 5 | GND | Analog and Digital Ground |
| 6 | DOUT | Serial Data Output. DOUT changes state at SCLK's rising edge. High impedance when \overline{CS} is high. |
| 7 | \overline{CS} | Active-Low Chip Select. Initiates conversions on the falling edge. When \overline{CS} is high, DOUT is high impedance. |
| 8 | SCLK | Serial Clock Input. SCLK drives the conversion process and clocks data out at rates up to 6.4MHz (MAX1284) or 4.8MHz (MAX1285). |

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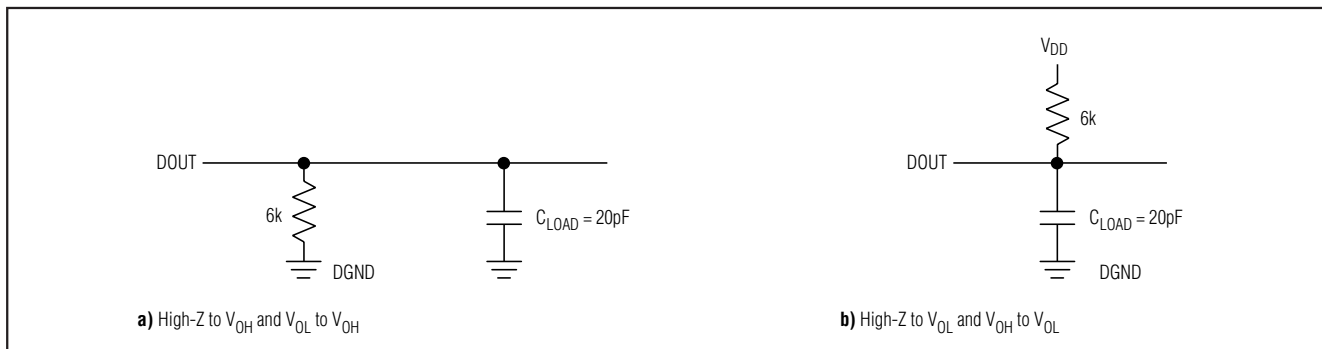


Figure 1. Load Circuits for DOUT Enable Time

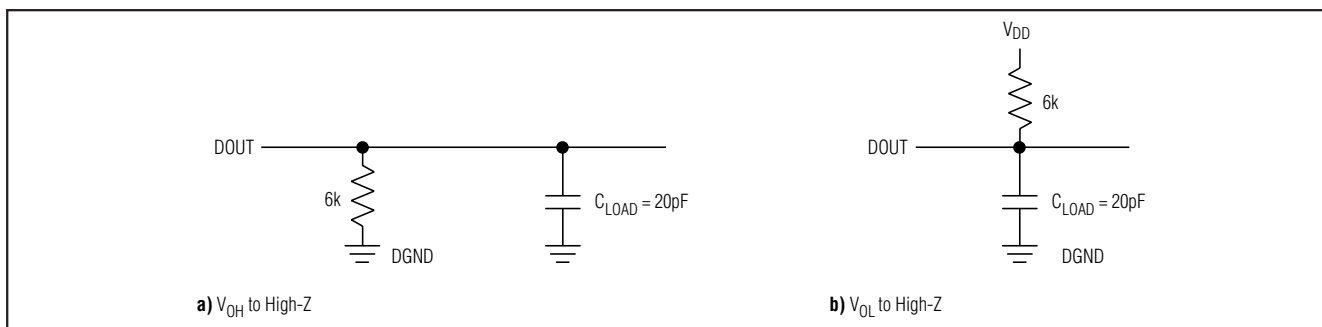


Figure 2. Load Circuits for DOUT Disable Time

Detailed Description

Converter Operation

The MAX1284/MAX1285 use an input T/H and successive-approximation register (SAR) circuitry to convert an analog input signal to a digital 12-bit output. Figure 3 shows the MAX1284/MAX1285 in its simplest configuration. The internal reference is trimmed to 2.5V. The serial interface requires only three digital lines (SCLK, \overline{CS} , and DOUT) and provides an easy interface to microprocessors (μ Ps).

The MAX1284/MAX1285 have two modes: normal and shutdown. Pulling \overline{SHDN} low shuts the device down and reduces supply current to below 2 μ A (typ), while pulling \overline{SHDN} high puts the device into operational mode. Pulling \overline{CS} low initiates a conversion that is driven by SCLK. The conversion result is available at DOUT in unipolar serial format. The serial data stream consists of three zeros, followed by the data bits (MSB first). All transitions on DOUT occur 20ns after the rising edge of SCLK. Figures 8 and 9 show the interface timing information.

Analog Input

Figure 4 illustrates the sampling architecture of the ADC's comparator. The full-scale input voltage is set by the internal reference ($V_{REF} = +2.5V$).

Track/Hold

In track mode, the analog signal is acquired and stored in the internal hold capacitor. In hold mode, the T/H switch opens and maintains a constant input to the ADC's SAR section.

During acquisition, the analog input (AIN) charges capacitor $CHOLD$. Bringing \overline{CS} low ends the acquisition interval. At this instant, the T/H switches the input side of $CHOLD$ to GND. The retained charge on $CHOLD$ represents a sample of the input, unbalancing node ZERO at the comparator's input.

In hold mode, the capacitive digital-to-analog converter (DAC) adjusts during the remainder of the conversion cycle to restore node ZERO to 0 within the limits of 12-bit resolution. This action is equivalent to transferring a charge from $CHOLD$ to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal. At the conversion's end, the input

400kps/300kps, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

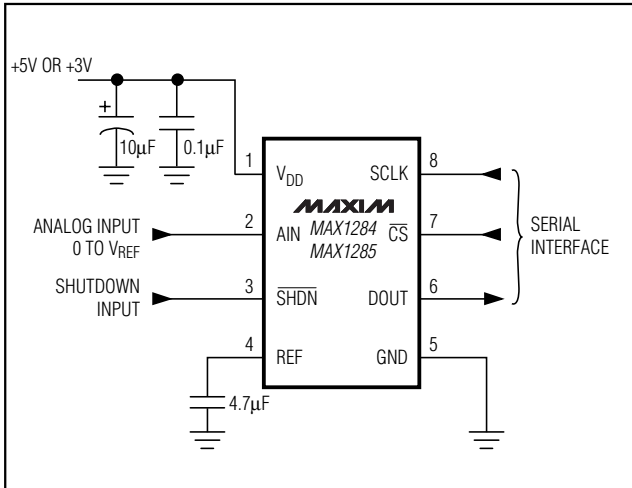


Figure 3. Typical Operating Circuit

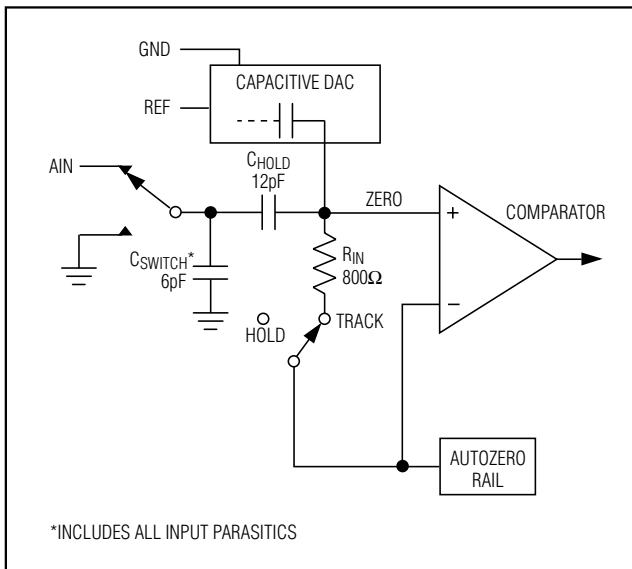


Figure 4. Equivalent Input Circuit

side of CHOLD switches back to AIN, and CHOLD charges to the input signal again.

The time required for the T/H to acquire an input signal is a function of how quickly its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens and more time must be allowed between conversions. The acquisition time (t_{ACQ}) is the maximum time the device takes to acquire the signal, and is also the minimum time needed for the

signal to be acquired. Acquisition time is calculated by:

$$t_{ACQ} = 9(R_S + R_{IN}) \times 12\text{pF}$$

where $R_{IN} = 800\Omega$, R_S = the input signal's source impedance, and t_{ACQ} is never less than 468ns (MAX1284) or 625ns (MAX1285). Source impedances below $2\text{k}\Omega$ do not significantly affect the ADC's AC performance.

Higher source impedances can be used if a $0.01\mu\text{F}$ capacitor is connected to the analog input. Note that the input capacitor forms an RC filter with the input source impedance, limiting the ADC's input signal bandwidth.

Input Bandwidth

The ADCs' input tracking circuitry has a 6MHz (MAX1284) or 3MHz (MAX1285) small-signal bandwidth, so it is possible to digitize high-speed transient events and measure periodic signals with bandwidths exceeding the ADC's sampling rate by using undersampling techniques. To avoid aliasing of unwanted high-frequency signals into the frequency band of interest, anti-alias filtering is recommended.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow the input to swing from $GND - 0.3\text{V}$ to $V_{DD} + 0.3\text{V}$ without damage.

If the analog input exceeds 50mV beyond the supplies, limit the input current to 2mA.

Internal Reference

The MAX1284/MAX1285 have an on-chip voltage reference trimmed to 2.5V. The internal reference output is connected to REF and also drives the internal capacitive DAC. The output can be used as a reference voltage source for other components and can source up to $800\mu\text{A}$. Bypass REF with a $4.7\mu\text{F}$ capacitor. Larger capacitors increase wake-up time when exiting shutdown (see the *Using SHDN to Reduce Supply Current* section). The internal reference is disabled in shutdown ($\overline{\text{SHDN}} = 0$).

Serial Interface

Initialization after Power-Up and Starting a Conversion

When power is first applied, and if $\overline{\text{SHDN}}$ is not pulled low, it takes the fully discharged $4.7\mu\text{F}$ reference bypass capacitor up to 2ms to provide adequate charge for specified accuracy. No conversions should be performed during this time.

400ksp/300ksp, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

To start a conversion, pull \overline{CS} low. At \overline{CS} 's falling edge, the T/H enters its hold mode and a conversion is initiated. Data can then be shifted out serially with the external clock.

Using \overline{SHDN} to Reduce Supply Current

Power consumption can be reduced significantly by shutting down the MAX1284/MAX1285 between conversions. Figure 5 shows a plot of average supply current versus conversion rate. The wake-up time (t_{WAKE}) is the time from when \overline{SHDN} is deasserted to the time when a conversion may be initiated (Figure 6). This time depends on the time in shutdown (Figure 7) because the external 4.7 μ F reference bypass capacitor loses charge slowly during shutdown and can be as long as 2ms.

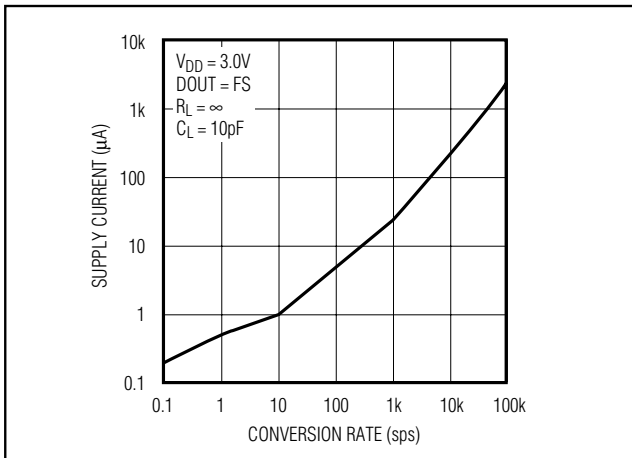


Figure 5. Supply Current vs. Conversion Rate

Timing and Control

Conversion-start and data-read operations are controlled by the \overline{CS} and SCLK digital inputs. The timing diagrams of Figures 8 and 9 outline serial-interface operation.

A \overline{CS} falling edge initiates a conversion sequence: the T/H stage holds the input voltage, the ADC begins to convert, and DOUT changes from high impedance to logic low. SCLK is used to drive the conversion process, and it shifts data out as each bit of conversion is determined.

SCLK begins shifting out the data after the rising edge of the third SCLK pulse. DOUT transitions 20ns after each SCLK rising edge. The third rising clock edge produces the MSB of the conversion at DOUT, followed by the remaining bits. Since there are 12 data bits and three leading zeros, at least 15 rising clock edges are needed to shift out these bits. Extra clock pulses occurring after the conversion result has been clocked out, and prior to a rising edge of \overline{CS} , produce trailing zeros at DOUT and have no effect on converter operation.

Pull \overline{CS} high after reading the conversion's LSB. For maximum throughput, \overline{CS} can be pulled low again to initiate the next conversion immediately after the specified minimum time (t_{CS}).

Output Coding and Transfer Function

The data output from the MAX1284/MAX1285 is binary, and Figure 10 depicts the nominal transfer function. Code transitions occur halfway between successive-integer LSB value $V_{REF} = 2.5V$, and $1LSB = 610\mu V$ or $2.5V/4096$.

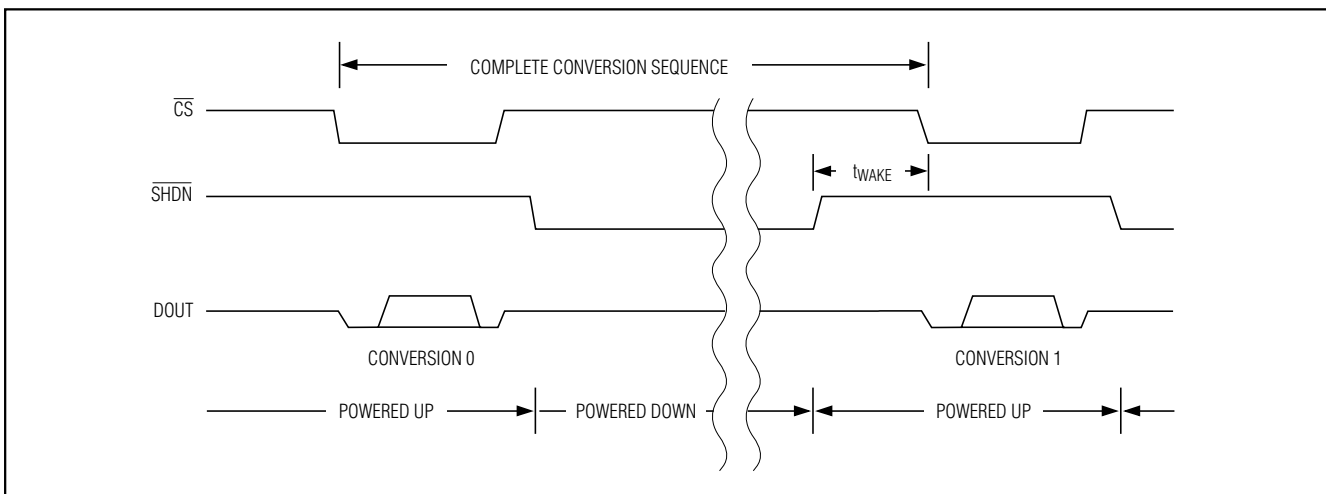


Figure 6. Shutdown Sequence

400ksp/300ksp, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

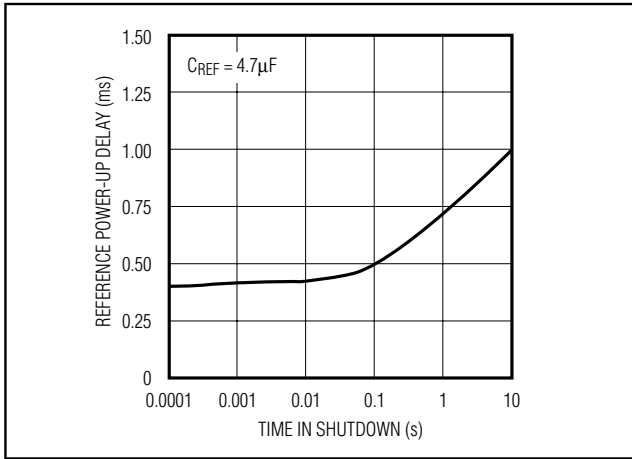


Figure 7. Reference Power-Up vs. Time in Shutdown

Applications Information

Connection to Standard Interfaces

The MAX1284/MAX1285 serial interface is fully compatible with SPI/QSPI and MICROWIRE (Figure 11).

If a serial interface is available, set the CPU's serial interface in master mode so the CPU generates the serial clock. Choose a clock frequency up to 6.4MHz (MAX1284) or 4.8MHz (MAX1285).

- 1) Use a general-purpose I/O line on the CPU to pull \overline{CS} low. Keep SCLK low.
- 2) Activate SCLK for a minimum of 15 clock cycles. The first two clocks produce zeros at DOUT. DOUT output data transitions 20ns after the third SCLK rising edge and is available in MSB-first format. Observe the

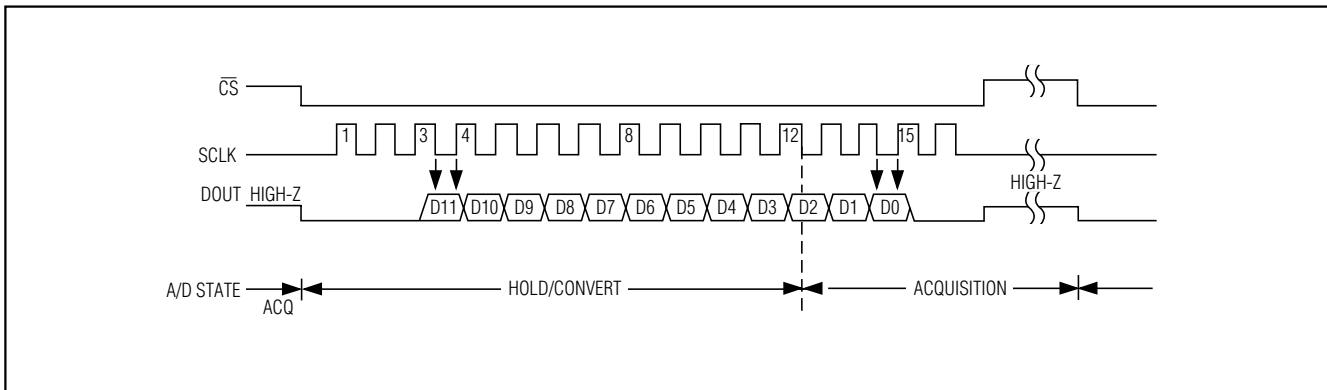


Figure 8. Interface Timing Sequence

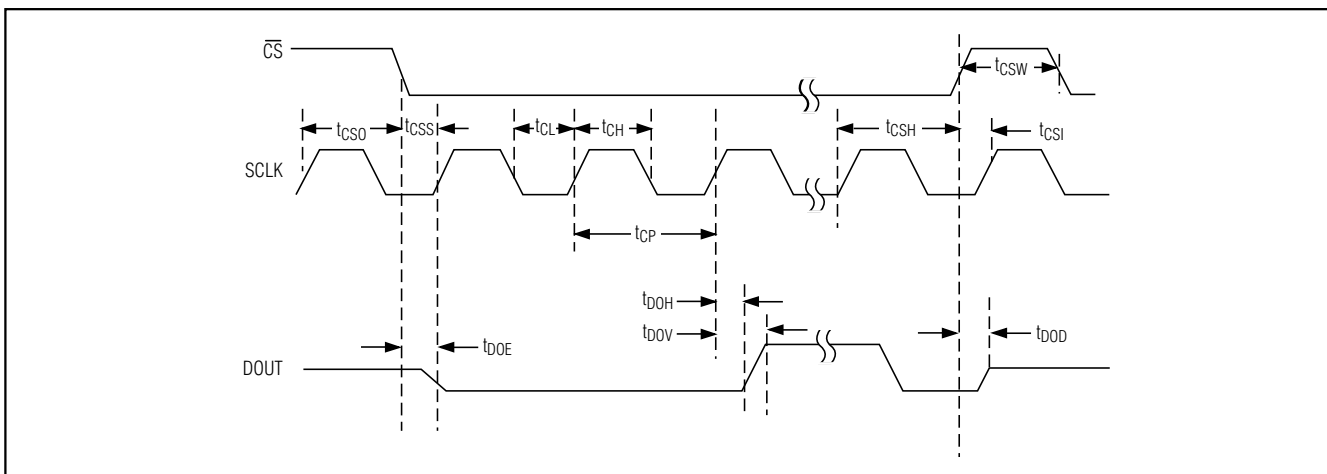


Figure 9. Detailed Serial-Interface Timing

400kps/300kps, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

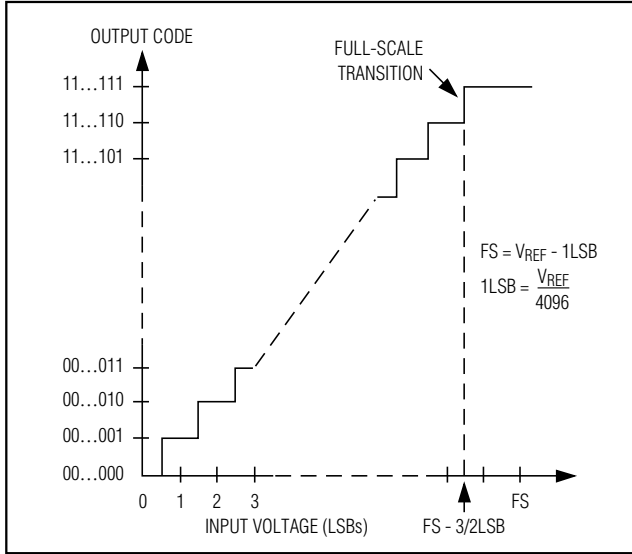


Figure 10. Unipolar Transfer Function, Full Scale (FS) = V_{REF} - 1LSB, Zero Scale (ZS) = GND

SCLK to DOUT valid timing characteristic. Data can be clocked into the μ P on SCLK rising edge.

- 3) Pull \overline{CS} high at or after the 15th rising clock edge. If \overline{CS} remains low, trailing zeros are clocked out after the LSB.
- 4) With \overline{CS} = high, wait the minimum specified time, t_{CS}, before initiating a new conversion by pulling \overline{CS} low. If a conversion is aborted by pulling \overline{CS} high before the conversion completes, wait for the minimum acquisition time, t_{ACQ}, before starting a new conversion.

\overline{CS} must be held low until all data bits are clocked out. Data can be output in 2 bytes or continuously, as shown in Figure 8. The bytes contain the result of the conversion padded with three leading zeros and three trailing zeros.

SPI and MICROWIRE

When using SPI or MICROWIRE, set CPOL = 0 and CPHA = 0. Conversion begins with a \overline{CS} falling edge. DOUT goes low, indicating a conversion in progress. Two consecutive 1-byte reads are required to get the full 12 bits from the ADC. DOUT output data transitions on SCLK's rising edge and is clocked into the following μ P on the rising edge.

The first byte contains three leading zeros, and 5 bits of conversion result. The second byte contains the remaining 7 bits and one trailing zero. See Figure 11 for connections and Figure 12 for timing.

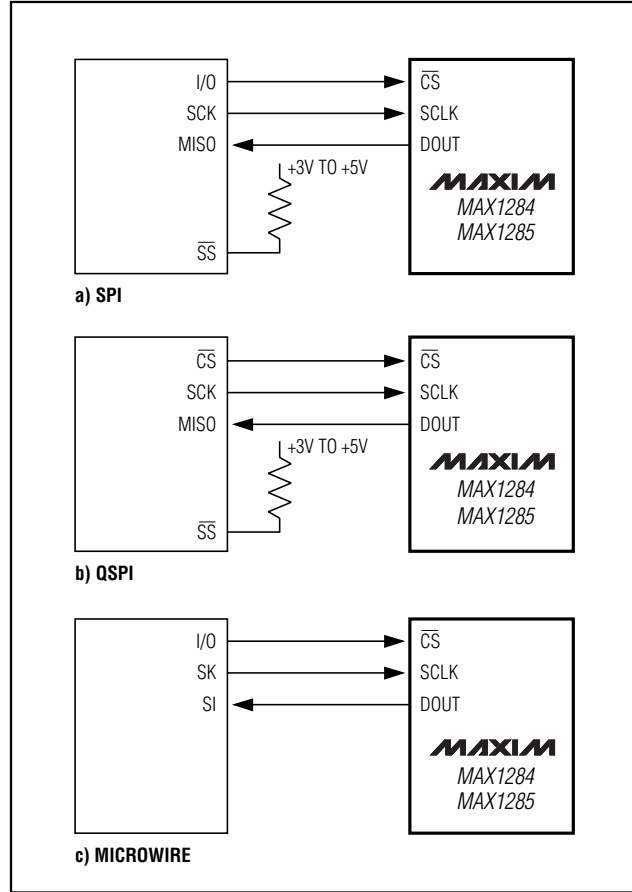


Figure 11. Common Serial-Interface Connections to the MAX1284/MAX1285

QSPI

Unlike SPI, which requires two 1-byte reads to acquire the 12 bits of data from the ADC, QSPI allows the minimum number of clock cycles necessary to clock in the data. The MAX1284/MAX1285 require 15 clock cycles from the μ P to clock out the 12 bits of data. Figure 13 shows a transfer using CPOL = 0 and CPHA = 1. The conversion result contains two zeros followed by the 12 bits of data in MSB-first formatted.

Layout, Grounding, and Bypassing

For best performance, use PC boards. Wire-wrap boards are not recommended. Board layout should ensure that digital and analog signal lines are separated from each other. Do not run analog and digital (especially clock) lines parallel to one another, or digital lines underneath the ADC package.

400ksp/300ksp, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

Figure 14 shows the recommended system ground connections. Establish a single-point analog ground (“star” ground point) at GND, separate from the logic ground. Connect all other analog grounds and DGND to this star ground point for further noise reduction. No other digital system ground should be connected to this single-point analog ground. The ground return to the power supply for this ground should be low impedance and as short as possible for noise-free operation.

High-frequency noise in the V_{DD} power supply may affect the ADC’s high-speed comparator. Bypass this supply to the single-point analog ground with 0.1μF and 10μF bypass capacitors. Minimize capacitor lead lengths for best supply noise rejection. To reduce the effects of supply noise, a 10Ω resistor can be connected as a lowpass filter to attenuate supply noise (Figure 14).

Definitions

Integral Nonlinearity

Integral nonlinearity (INL) is the deviation of the values on an actual transfer function from a straight line. This straight line can be either a best-straight-line fit or a line drawn between the endpoints of the transfer function, once offset and gain errors have been nullified. The static linearity parameters for the MAX1284/MAX1285 are measured using the endpoints method.

Differential Nonlinearity

Differential nonlinearity (DNL) is the difference between an actual step width and the ideal value of 1LSB. A DNL error specification of 1LSB or less guarantees no missing codes and a monotonic transfer function.

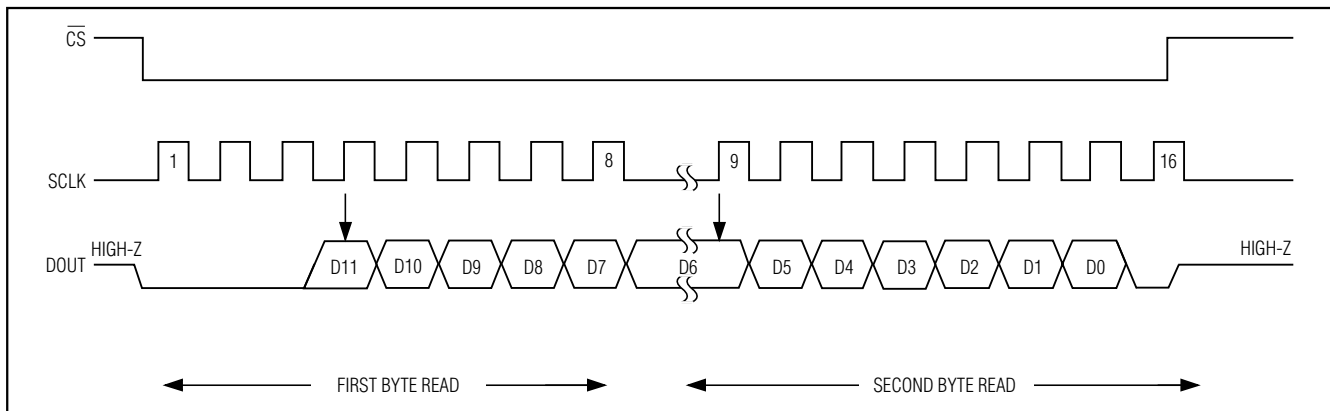


Figure 12. SPI/MICROWIRE Serial Interface Timing (CPOL = CPHA = 0)

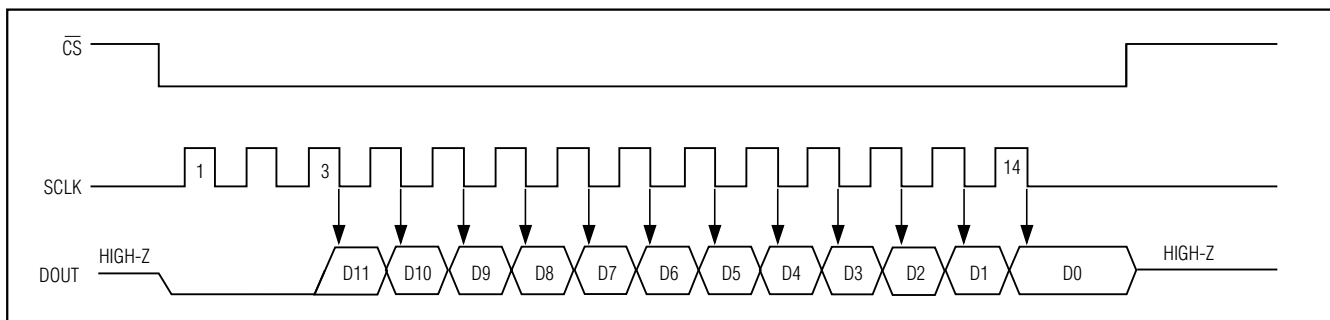


Figure 13. QSPI Serial Interface Timing (CPOL = 0, CPHA = 1)

400kps/300kps, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

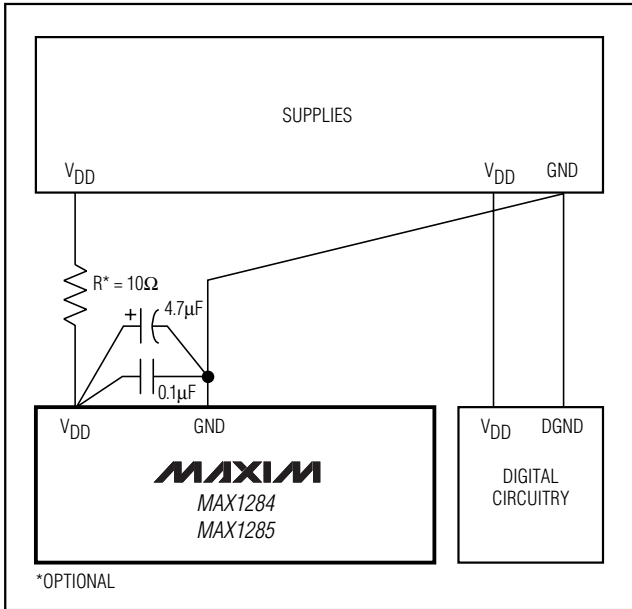


Figure 14. Power-Supply Grounding Condition

Aperture Jitter

Aperture jitter (t_{AJ}) is the sample-to-sample variation in the time between the samples.

Aperture Delay

Aperture delay (t_{AD}) is the time defined between the falling edge of CS and the instant when an actual sample is taken.

Signal-to-Noise Ratio

For a waveform perfectly reconstructed from digital samples, signal-to-noise ratio (SNR) is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The theoretical minimum analog-to-digital noise is caused by quantization error, and results directly from the ADC's resolution, (N bits):

$$SNR = (6.02 \times N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise, including thermal noise, reference noise, clock jitter, etc. Therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise, which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion

Signal-to-noise plus distortion (SINAD) is the ratio of the fundamental input frequency's RMS amplitude to RMS equivalent of all other ADC output signals.

$$SINAD (dB) = 20 \times \log (\text{Signal}_{RMS}/\text{Noise}_{RMS})$$

Effective Number of Bits

Effective number of bits (ENOB) indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists of quantization noise only. With an input range equal to the full-scale range of the ADC, calculate the effective number of bits as follows:

$$ENOB = \frac{(SINAD - 1.76)}{6.02}$$

Total Harmonic Distortion

Total harmonic distortion (THD) is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \times \log \left(\frac{\sqrt{V_2^2 + V_3^2 + V_4^2 + V_5^2}}{V_1} \right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd through 5th-order harmonics.

Spurious-Free Dynamic Range

Spurious-free dynamic range (SFDR) is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next-largest distortion component.

Chip Information

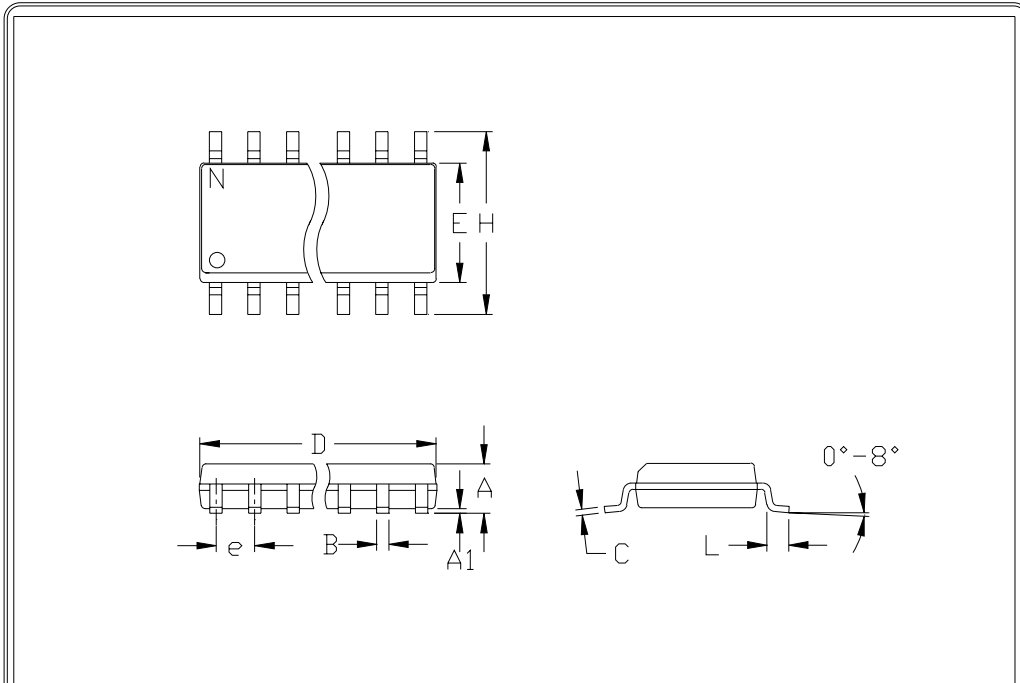
TRANSISTOR COUNT: 4286

PROCESS: BiCMOS

400ksp/300ksp, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

Package Information

MAX1284/MAX1285



| | INCHES | | MILLIMETERS | |
|----|--------|-------|-------------|------|
| | MIN | MAX | MIN | MAX |
| A | 0.053 | 0.069 | 1.35 | 1.75 |
| A1 | 0.004 | 0.010 | 0.10 | 0.25 |
| B | 0.014 | 0.019 | 0.35 | 0.49 |
| C | 0.007 | 0.010 | 0.19 | 0.25 |
| e | 0.050 | | 1.27 | |
| E | 0.150 | 0.157 | 3.80 | 4.00 |
| H | 0.228 | 0.244 | 5.80 | 6.20 |
| h | 0.010 | 0.020 | 0.25 | 0.50 |
| L | 0.016 | 0.050 | 0.40 | 1.27 |

| | INCHES | | MILLIMETERS | | N | MS012 |
|---|--------|-------|-------------|-------|----|-------|
| | MIN | MAX | MIN | MAX | | |
| D | 0.189 | 0.197 | 4.80 | 5.00 | 8 | A |
| D | 0.337 | 0.344 | 8.55 | 8.75 | 14 | B |
| D | 0.386 | 0.394 | 9.80 | 10.00 | 16 | C |

NOTES:

1. D & E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. LEADS TO BE COPLANAR WITHIN .102mm (.004")
4. CONTROLLING DIMENSION: MILLIMETER
5. MEETS JEDEC MS012-XX AS SHOWN IN ABOVE TABLE
6. N = NUMBER OF PINS

MAXIM
1201 SAN GABRIEL DR. SUNNYVALE, CA 94086 FAX (408) 737-7794
PROPRIETARY INFORMATION

PACKAGE FAMILY OUTLINE: SOIC .150" TITLE

1/1

21-0041 A
DOCUMENT CONTROL NUMBER REV

400ksps/300ksps, Single-Supply, Low-Power, Serial 12-Bit ADCs with Internal Reference

NOTES

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