FAIRCHILD SEMICONDUCTOR™

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# DM9374
# 7-Segment Decoder/Driver/Latch with Constant Current Sink Outputs

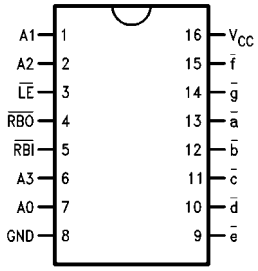
## General Description

The DM74 is a 7-segment decoder driver incorporating input latches and output circuits to directly drive common anode LED displays.

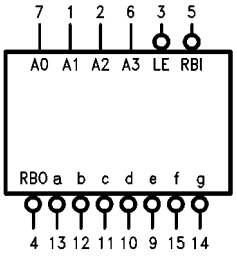
## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| DM9374N | N16E | 16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

## Connection Diagram




## Logic Symbol




$V_{CC}$ = Pin 16
GND = Pin 8

## Pin Descriptions

| Pin Names | Description |
|---|---|
| A0–A3 | Address (Data Inputs) |
| $\overline{LE}$ | Latch Enable Input (Active LOW) |
| $\overline{RBI}$ | Ripple Blanking Input (Active LOW) |
| $\overline{RBO}$ | Ripple Blanking as Output (Active LOW) as Input (Active LOW) |
| $\overline{a}$ –$\overline{g}$ | Constant Current Outputs (Active LOW) |

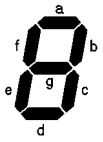
## Truth Table

| Binary State | Inputs | | | | | | Outputs | | | | | | | | Display |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| | $\overline{LE}$ | $\overline{RBI}$ | A3 | A2 | A1 | A0 | $\overline{a}$ | $\overline{b}$ | $\overline{c}$ | $\overline{d}$ | $\overline{e}$ | $\overline{f}$ | $\overline{g}$ | $\overline{RBO}$ | |
| — | H | (Note 1) | X | X | X | X | STABLE | | | | | | | H | Stable |
| 0 | L | L | L | L | L | L | H | H | H | H | H | H | H | L | Blank |
| 0 | L | H | L | L | L | L | L | L | L | L | L | L | H | H | 0 |
| 1 | L | X | L | L | L | H | H | L | L | H | H | H | H | H | 1 |
| 2 | L | X | L | L | H | L | L | L | H | L | L | H | L | H | 2 |
| 3 | L | X | L | L | H | H | L | L | L | L | H | H | L | H | 3 |
| 4 | L | X | L | H | L | L | H | L | L | H | H | L | L | H | 4 |
| 5 | L | X | L | H | L | H | L | H | L | L | H | L | L | H | 5 |
| 6 | L | X | L | H | H | L | L | H | L | L | L | L | L | H | 6 |
| 7 | L | X | L | H | H | H | L | L | L | H | H | H | H | H | 7 |
| 8 | L | X | H | L | L | L | L | L | L | L | L | L | L | H | 8 |
| 9 | L | X | H | L | L | H | L | L | L | L | H | L | L | H | 9 |
| 10 | L | X | H | L | H | L | H | H | H | H | H | H | L | H | — |
| 11 | L | X | H | L | H | H | L | H | H | L | L | L | L | H | E |
| 12 | L | X | H | H | L | L | H | L | L | H | L | L | L | H | H |
| 13 | L | X | H | H | L | H | H | H | H | L | L | L | H | H | L |
| 14 | L | X | H | H | H | L | L | L | H | H | L | L | L | H | P |
| 15 | L | X | H | H | H | H | H | H | H | H | H | H | H | H | BLANK |
| X | X | X | X | X | X | X | H | H | H | H | H | H | H | L (Note 2) | BLANK |

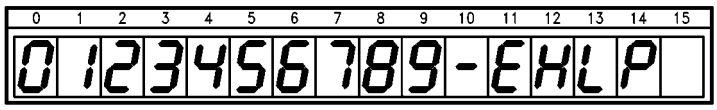
H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

**Note 1:** The $\overline{RBI}$ will blank the display only if a binary zero is stored in the latches.

**Note 2:** $\overline{RBO}$ used as an input overrides all other input conditions.




**Numerical Designations**



## Functional Description

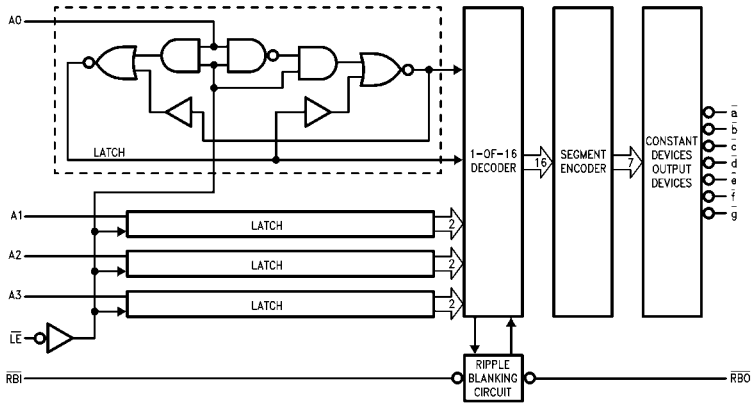
The DM9374 is a 7-segment decoder/driver with latches on the address inputs and active LOW constant current outputs to drive LEDs directly. This device accepts a 4-bit binary code and produces output drive to the appropriate segments of the 7-segment display. It has a decode format which produces numeric codes “0” through “9” and other codes.

Latches on the four data inputs are controlled by an active LOW Latch Enable, $\overline{LE}$. When $\overline{LE}$ is LOW, the state of the outputs is determined by the input data. When $\overline{LE}$ goes HIGH, the last data present at the inputs is stored in the latches and the outputs remain stable. The $\overline{LE}$ pulse width necessary to accept and store data is typically 50 ns, which allows data to be strobed into the DM9374 at normal TTL speeds. This feature means that data can be routed directly from high speed counters and frequency dividers into the display without slowing down the system clock or providing intermediate data storage.

The latch/decoder combination is a simple system which drives LED displays with multiplexed data inputs from MOS time clocks, DVMs, calculator chips, etc. Data inputs are multiplexed while the displays are in static mode. This lowers component and insertion costs, since several circuits—seven resistors per display, strobe drivers, a separate display voltage source, and clock failure detect circuits—traditionally found in multiplexed display systems are eliminated. It also allows low strobing rates to be used without display flicker.

Another DM9374 feature is the reduced loading on the data inputs when the Latch Enable is HIGH (only 10 µA typ). This allows many DM9374s to be driven from a MOS device in multiplex mode without the need for drivers on the data lines. The DM9374 also provides automatic blanking of the leading and/or trailing-edge zeroes in a multidigit decimal number, resulting in an easily readable decimal display conforming to normal writing practice. In an 8-digit mixed integer fraction decimal representation, using the automatic blanking capability 0060.0300 would be displayed as 60.03. Leading-edge zero suppression is obtained by connecting the Ripple Blanking Output ($\overline{RBO}$) of a decoder to the Ripple Blanking Input ($\overline{RBI}$) of the next lower stage device. The most significant decoder stage should have the $\overline{RIB}$ input grounded; and since suppression of the least significant integer zero in a number is not usually desired, the $\overline{RBI}$ input of this decoder stage should be left open. A similar procedure for the fractional part of a display will provide automatic suppression of trailing-edge zeroes. The $\overline{RBO}$ terminal of the decoder can be OR-tied with a modulating signal via an isolating buffer to achieve duration intensity modulation. A suitable signal can be generated for this purpose by forming a variable frequency multivibrator with a cross coupled pair of TTL or DTL gates.

## Logic Diagram



## Applications

It is possible with common anode 7-segment LED displays and constant current sink decoder drivers to save substantial amounts of power by carefully choosing operating points on display supply voltage. First, examine the power used in the normal display driving method where the display and decoder driver are both operated from a +5.0V regulated supply ($V_{CC} = V_S$).

The power dissipated by the LED and the driver outputs is ($V_{CC}$ x $I_{seg}$ x n Segments). The total power dissipated with a 15 mA LED displaying an eight (8) would be:

$P_{TOT}$ = 5.0V x 15 mA x 7

= 525 mW

Of this 525 mW, the power actually required to drive the LED is dependent on the $V_F$ drop of each segment. Most GaAsP LEDs exhibit either a 1.7V or a 3.4V forward voltage drop. Therefore, the required total power for seven segments would be:

$P_{(1.7)}$ = 1.7V x 15 mA x 7

= 178.5 mW

$P_{(3.4)}$= 3.4V x 15 mA x 7

= 357 mW

The remaining power is dissipated by the driver outputs which are maintaining the 15 mA constant current required by the LEDs. Most of this power is wasted, since the driver can maintain approximately 15 mA with as little as 0.5V across the output device. By using a separate power source ($V_S$, Figure 1) for the LEDs, which is set to the LED $V_F$ plus the offset voltage of the driver, as much as 280 mW can be saved per digit. i.e.,

$V_S = V_F$ (Max) + $V_{offset}$

= 2.0V + 0.5V

= 2.5V

$P_T$= 2.5V x 14 mA (from Figure 6) x 7

= 245 mW

These figures show that using a separate supply to drive the LEDs can offer significant display power savings. In battery powered equipment, two rechargeable nickel-cadmium cells in series would be sufficient to drive the display, while four such cells would be needed to operate the logic units.

Another method to save power is to apply intensity modulation to the displays (Figure 2). It is well known that LED displays are more efficient when operated in pulse mode. There are two reasons: one, the quantum efficiency of the LED material is better; secondly the eye tends to peak detect. Typically a 20% off duty cycle to displays (GaAsP) will produce the same brightness as operating under dc conditions.

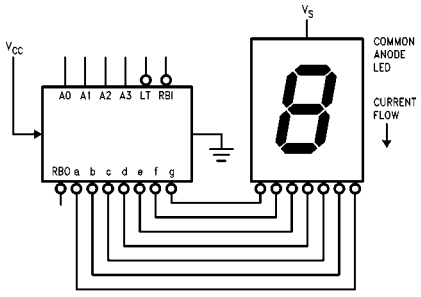
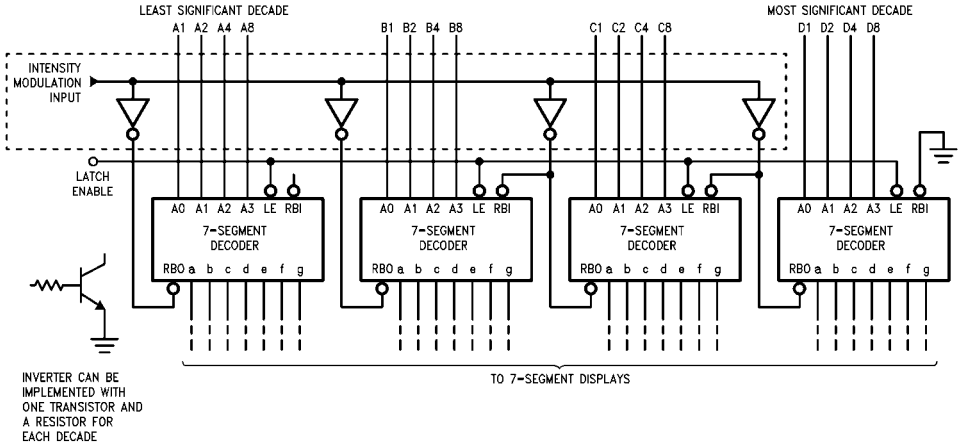



**FIGURE 1. Separate Supply for LED Displays**




All Inverters are DTL 9936 or Open Collector TTL 7405

**FIGURE 2. Intensity Control by $\overline{\text{RBO}}$ Pulse Duty Cycle**

**Low Power, Low Cost Display Power Sources**—In small line operated systems using TTL/MSI and LED or incandescent displays, a significant portion of the total dc power is consumed to drive the displays. Since it is irrelevant whether displays are driven from unfiltered dc or pulsed dc (at fast rates), a dual power system can be used that makes better utilization of transformer rms ratings. The system utilizes a full wave rectified but unsmoothed dc voltage to provide the displays with 120 Hz pulsed power while the reset of the system is driven by a conventional dc power circuit. The frequency of 120 Hz is high enough to avoid display flicker problems. The main advantages of this system are:

- Reduced transformer rating
- Much smaller smoothing capacitor
- Increased LED light output due to pulsed operation

With the standard capacitor filter circuit, the rms current (full wave) loading of the transformer is approximately twice the dc output. Most commercial transformer manufacturers rate transformers with capacitive input filters as follows:

Full Wave Bridge Rectifier Circuit

Transformer rms current = 1.8 x dc current required

Full Wave Center Tapped Rectifier Circuit

Transformer rms current = 1.2 x dc current required

Therefore, the removal of a large portion of the filtered dc current requirement (display power) substantially reduces the transformer loading.

There are two basic approaches. First (Figure 3) is the direct full wave rectified unregulated supply to power the displays. The '74 decoder driver constant current feature maintains the specified segment current after the LED diode drop and 0.5V saturation voltage has been reached (≅2.2V). Care must be exercised not to exceed the '74 power ratings and the maximum voltage that the decoder driver sees in both the “on” and “off” modes.

The second approach (Figure 4) uses a 3-terminal voltage regulator such as the 7805 to provide dc pulsed power to the display with the peak dc voltage limited to +5.0V. This approach allows easier system thermal management by heat sinking the regulator rather than the display or display drivers. When this power source is used with an intensity modulation scheme or with a multiplexed display system, the frequencies must be chosen such that they do not beat with the 120 Hz full wave rectified power frequency.

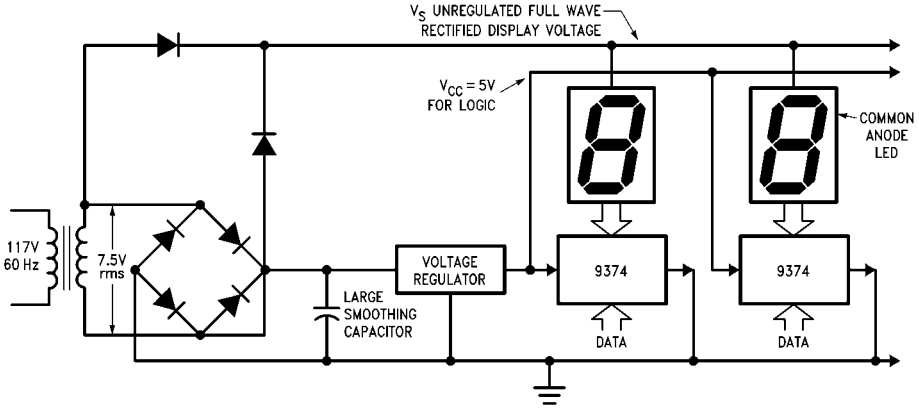



**FIGURE 3. Direct Unregulated Display Supply**

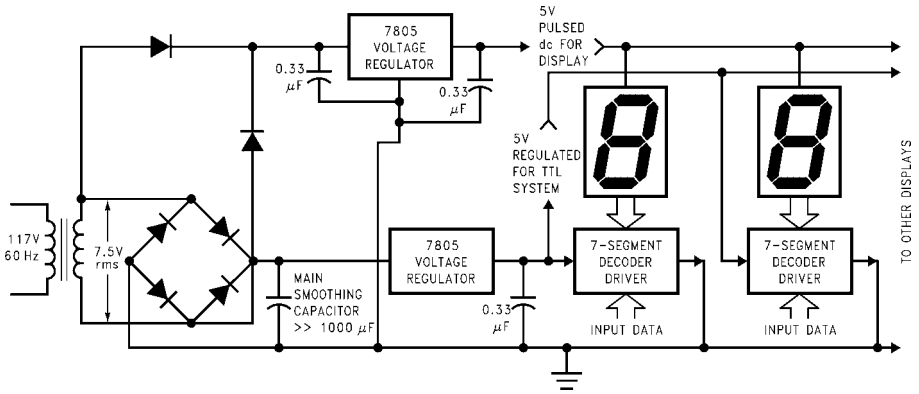



**FIGURE 4. Pulsed Regulated Display Supply**

## Absolute Maximum Ratings(Note 3)

| | |
|---|---|
| Supply Voltage | 7V |
| Input Voltage | 5.5V |
| Operating Free Air Temperature Range | 0°C to +70°C |
| Storage Temperature Range | −65°C to +150°C |

**Note 3:** The "Absolute Maximum Ratings" are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the absolute maximum ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

## Recommended Operating Conditions

| Symbol | Parameter | | Min | Nom | Max | Units |
|---|---|---|---|---|---|---|
| $V_{CC}$ | Supply Voltage | | 4.75 | 5 | 5.25 | V |
| $V_{OUT}$ | Output Voltage Applied | OFF | | | 10 | V |
| | | ON | | | (Figure 5) | |
| $V_{IH}$ | HIGH Level Input Voltage | | 2 | | | V |
| $V_{IL}$ | LOW Level Input Voltage | | | | 0.8 | V |
| $I_{OH}$ | HIGH Level Output Current, $\overline{a}$–$\overline{g}$, $V_{OUT}$ = 5.5V | | | | 250 | µA |
| $I_{OL}$ | LOW Level Output Current, $\overline{a}$–$\overline{g}$, $V_{OL}$ = 3.0V | | 12 | | 18 | mA |
| $T_A$ | Free Air Operating Temperature | | 0 | | 70 | °C |
| $t_S$ (H) | Setup Time HIGH or LOW | | 75 | | | ns |
| $t_S$ (L) | An to $\overline{LE}$ | | 30 | | | |
| $t_H$ (H) | Hold Time HIGH or LOW | | 0 | | | ns |
| $t_H$ (L) | An to $\overline{LE}$ | | 0 | | | |
| $t_W$ (L) | $\overline{LE}$ Pulse Width LOW | | 85 | | | ns |

## Electrical Characteristics

over recommended operating free air temperature range (unless otherwise noted)

| Symbol | Parameter | Conditions | Min | Typ (Note 4) | Max | Units |
|---|---|---|---|---|---|---|
| $V_I$ | Input Clamp Voltage | $V_{CC}$ = Min, $I_I$ = −12 mA | | | −1.5 | V |
| $V_{OH}$ | HIGH Level Output Voltage | $V_{CC}$ = Min, $I_{OH}$ = Max, $V_{IL}$ = Max | 2.4 | 3.4 | | V |
| $V_{OL}$ | LOW Level Output Voltage | $V_{CC}$ = Min, $I_{OL}$ = Max, $V_{IH}$ = Min | | 0.2 | 0.4 | V |
| $I_I$ | Input Current @ Max Input Voltage | $V_{CC}$ = Max, $V_I$ = 5.5V | | | 1 | mA |
| $I_{IH}$ | HIGH Level Input Current | $V_{CC}$ = Max, $V_I$ = 2.4V | | | 40 | µA |
| $I_{IL}$ | LOW Level Input Current | $V_{CC}$ = Max, $V_I$ = 0.4V | | | −1.6 | mA |
| $I_{OS}$ | Short Circuit Output Current | $V_{CC}$ = Max (Note 5) | −18 | | −57 | mA |
| $I_{CCH}$ | Supply Current | $V_{CC}$ = Max, $V_{IN}$ = 0V, $V_{OUT}$ = 3.0V | | | 50 | mA |

**Note 4:** All typicals are at $V_{CC}$ = 5V, $T_A$ = 25°C.

**Note 5:** Not more than one output should be shorted at a time.

## Switching Characteristics

$V_{CC}$ = +5.0V, $T_A$ = +25°C

| Symbol | Parameter | $C_L$ = 15 pF, $R_L$ = 1 kΩ | | Units |
|---|---|---|---|---|
| | | Min | Max | |
| $t_{PLH}$ | Propagation Delay | | 140 | ns |
| $t_{PHL}$ | An to $\overline{a}$–$\overline{g}$ | | 140 | |
| $t_{PLH}$ | Propagation Delay | | 140 | ns |
| $t_{PHL}$ | $\overline{LE}$ to $\overline{a}$–$\overline{g}$ | | 140 | |

## Typical Performance Characteristics

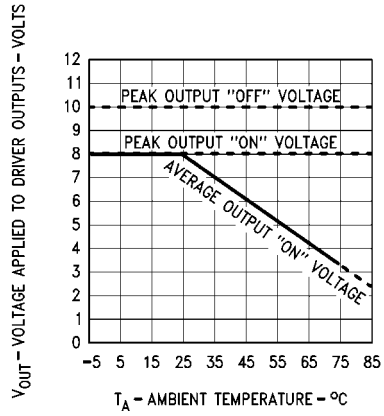



**FIGURE 5. Output Voltage Safe Operating Area**

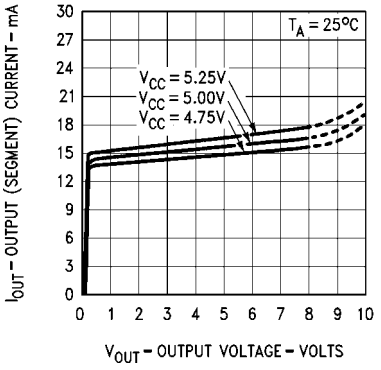
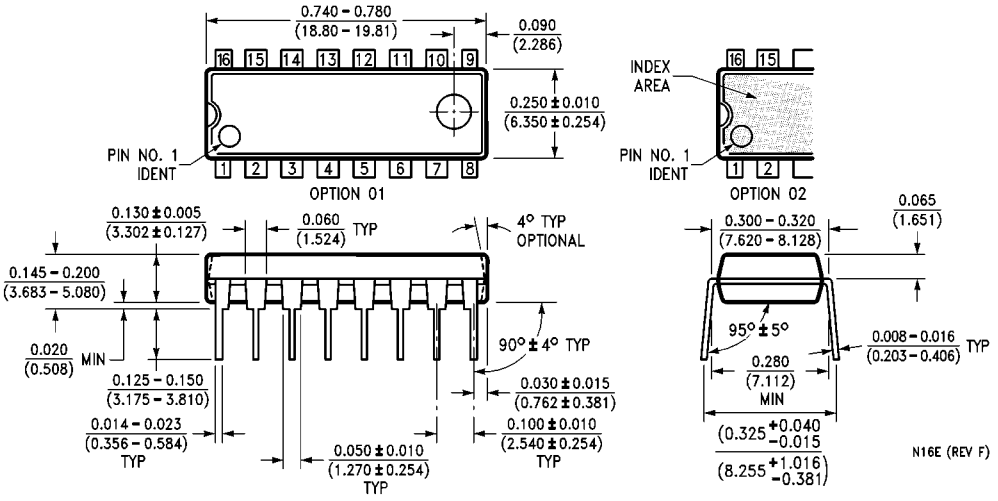



**FIGURE 6. Typical Constant Segment Current Versus Output Voltage**

## Physical Dimensions inches (millimeters) unless otherwise noted




**16-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N16E**