Low Voltage, 300 MHz Quad 2:1 Mux Analog HDTV Audio/Video Switch

ADG794

FEATURES

Bandwidth: 300 MHz
Low insertion loss and on resistance: 5 Ω typical
On resistance flatness: 0.68 Ω typical
Single 3 V/5 V supply operation
Low quiescent supply current: 1 nA typical
Fast switching times:
t_{ON}, 7 ns
t_{OFF}, 5 ns
TTL/CMOS compatible

APPLICATIONS

RGB switches
HDTV
DVD-R
Audio/video switches

FUNCTIONAL BLOCK DIAGRAM

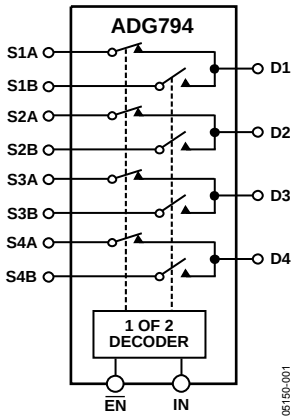

Figure 1.

GENERAL DESCRIPTION

The ADG794 is a monolithic CMOS device comprising four 2:1 multiplexer/demultiplexers with high impedance outputs. The CMOS process provides low power dissipation yet gives high switching speed and low on resistance. The on resistance variation is typically less than 1.2 Ω over the input signal range.

The bandwidth of the ADG794 is typically 300 MHz and this, coupled with low distortion (typically 0.68%), makes the part suitable for switching analog audio/video signals.

The ADG794 operates from a single 3.3 V/5 V supply and is TTL logic compatible. The switches are controlled by the logic inputs IN and $\overline{EN}$ as shown in Table 4. The $\overline{EN}$ pin allows the user to disable all switches.

These switches conduct equally well in both directions when on. In the off condition, signal levels up to the supplies are blocked. The ADG794 switches exhibit break-before-make switching action.

The ADG794 is available in a 16-pin QSOP package.

PRODUCT HIGHLIGHTS

1. Wide bandwidth: 300 MHz.
2. Ultralow power dissipation.
3. Crosstalk is typically −70 dB at 10 MHz.
4. Off isolation is typically −65 dB at 10 MHz.

Rev. 0

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REVISION HISTORY

10/04—Revision 0: Initial Version

SPECIFICATIONS

SINGLE SUPPLY

V_{DD} = 5 V ± 10%, GND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 1.

Parameter	B Version[1] 25°C	B Version[1] T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to 2.5	V	
On Resistance (R_{ON})	5		Ω typ	V_D = 0 V to 1 V; I_S = −10 mA; Figure 6
	7	8	Ω max	
On Resistance Match between Channels (ΔR_{ON})	0.4		Ω typ	V_D = 0 V to 1 V; I_S = −10 mA
		1.2	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	0.7		Ω typ	V_D = 0 V to 1 V; I_S = −10 mA
		1.35	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	±0.001		nA typ	V_S = 3 V/1 V; V_D = 1 V/3 V; Figure 7
Drain Off Leakage, I_D (Off)	±0.001		nA typ	V_S = 3 V/1 V; V_D = 1 V/3 V; Figure 7
Channel On Leakage, I_D, I_S (On)	±0.001		nA typ	V_D = V_S = 3 V/1 V; Figure 8
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.4	V min	
Input Low Voltage, V_{INL}		0.8	V max	
Input Current				
I_{INL} or I_{INH}	0.001		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}		3	pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}, t_{ON} ($\overline{EN}$)	7		ns typ	C_L = 35 pF; R_L = 50 Ω
		14	ns max	V_S = 2 V; Figure 9
t_{OFF}, t_{OFF} ($\overline{EN}$)	5		ns typ	C_L = 35 pF; R_L = 50 Ω
		8	ns max	V_S = 2 V; Figure 9
Break-Before-Make Time Delay, t_D	3		ns typ	C_L = 35 pF; R_L = 50 Ω
		1	ns min	V_{S1} = V_{S2} = 2 V; Figure 10
Off Isolation	−65		dB typ	f = 10 MHz; R_L = 50 Ω; Figure 12
Channel-to-Channel Crosstalk	−70		dB typ	f = 10 MHz; R_L = 50 Ω; Figure 13
Bandwidth −3 dB	300		MHz typ	R_L = 50 Ω; Figure 11
Distortion	0.7		% typ	R_L = 100 Ω
Charge Injection	6		pC typ	C_L = 1 nF; V_S = 0 V; Figure 14
C_S (Off)	6		pF typ	
C_D (Off)	7.5		pF typ	
C_D, C_S (On)	13.5		pF typ	
POWER REQUIREMENTS				V_{DD} = 5.5 V; digital inputs = 0 V or V_{DD}
I_{DD}	0.001		μA typ	
		1	μA max	

[1] Temperature range for B Version is −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

V_{DD} = 3 V ± 10%, GND = 0 V. All specifications T_{MIN} to T_{MAX}, unless otherwise noted.

Table 2.

Parameter	B Version[1] 25°C	B Version[1] T_{MIN} to T_{MAX}	Unit	Test Conditions/Comments
ANALOG SWITCH				
Analog Signal Range		0 to 1.5	V	
On Resistance (R_{ON})	7		Ω typ	V_D = 0 V to 1 V; I_S = −10 mA; Figure 6
	9.5	11	Ω max	
On Resistance Match between Channels (ΔR_{ON})	0.3		Ω typ	V_D = 0 V to 1 V; I_S = −10 mA
		0.9	Ω max	
On Resistance Flatness ($R_{FLAT(ON)}$)	2.6		Ω typ	V_D = 0 V to 1 V; I_S = −10 mA
		5	Ω max	
LEAKAGE CURRENTS				
Source Off Leakage, I_S (Off)	±0.001		nA typ	V_S = 2 V/1 V; V_D = 1 V/2 V; Figure 7
Drain Off Leakage, I_D (Off)	±0.001		nA typ	V_S = 2 V/1 V; V_D = 1 V/2 V; Figure 7
Channel On Leakage, I_D, I_S (On)	±0.001		nA typ	V_D = V_S = 2 V/1 V; Figure 8
DIGITAL INPUTS				
Input High Voltage, V_{INH}		2.0	V min	
Input Low Voltage, V_{INL}		0.4	V max	
Input Current				
I_{INL} or I_{INH}	0.001		μA typ	V_{IN} = V_{INL} or V_{INH}
		±0.1	μA max	
Digital Input Capacitance, C_{IN}		3	pF typ	
DYNAMIC CHARACTERISTICS[2]				
t_{ON}, t_{ON} ($\overline{EN}$)	8		ns typ	C_L = 35 pF; R_L = 50 Ω
		16	ns max	V_S = 1.5 V; Figure 9
t_{OFF}, t_{OFF} ($\overline{EN}$)	6		ns typ	C_L = 35 pF; R_L = 50 Ω
		10	ns max	V_S = 1.5 V; Figure 9
Break-Before-Make Time Delay, t_D	3		ns typ	C_L = 35 pF; R_L = 50 Ω
		1	ns min	V_{S1} = V_{S2} = 1.5 V; Figure 10
Off Isolation	−65		dB typ	f = 10 MHz; R_L = 50 Ω; Figure 12
Channel-to-Channel Crosstalk	−70		dB typ	f = 10 MHz; R_L = 50 Ω; Figure 13
Bandwidth −3 dB	300		MHz typ	R_L = 50 Ω; Figure 11
Distortion	2.6		% typ	R_L = 100 Ω
Charge Injection	4		pC typ	C_L = 1 nF; V_S = 0 V; Figure 14
C_S (Off)	6		pF typ	
C_D (Off)	7.5		pF typ	
C_D, C_S (On)	13.5		pF typ	
POWER REQUIREMENTS				V_{DD} = 3.3 V; digital inputs = 0 V or V_{DD}
I_{DD}	0.001		μA typ	
		1	μA max	

[1] Temperature range for B Version is −40°C to +85°C.
[2] Guaranteed by design, not subject to production test.

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C, unless otherwise noted.

Table 3.

Parameters	Ratings
V_{DD} to GND	−0.3 V to +6 V
Analog, Digital Inputs[1]	−0.3 V to V_{DD} + 0.3 V or 30 mA, whichever occurs first
Continuous Current, S or D	100 mA
Peak Current, S or D	300 mA (pulsed at 1 ms, 10% duty cycle max)
Operating Temperature Range	
Industrial (B Version)	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
QSOP Package, Power Dissipation	566 mW
θ_{JA} Thermal Impedance	149.97°C/W
Lead Temperature, Soldering	
Vapor Phase (60 s)	215°C
Infrared (15 s)	220°C

[1] Overvoltages at IN, S, or D are clamped by internal diodes. Current should be limited to the maximum ratings given.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those listed in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Only one absolute maximum rating may be applied at any one time.

Table 4. Truth Table

$\overline{EN}$	IN	D1	D2	D3	D4	Function
1	X	Hi-Z	Hi-Z	Hi-Z	Hi-Z	Disable
0	0	S1A	S2A	S3A	S4A	IN = 0
0	1	S1B	S2B	S3B	S4B	IN = 1

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000 V readily accumulate on the human body and test equipment and can discharge without detection. Although this product features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

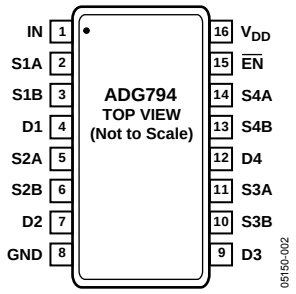

Figure 2. Pin Configuration

Table 5. Pin Function Descriptions

Pin Number	Mnemonic	Description
1	IN	Logic Control Input. The logic level at this input controls the operation of the multiplexers (see Table 4).
2	S1A	A-Side Source Terminal of MUX1. Can be an input or output.
3	S1B	B-Side Source Terminal of MUX1. Can be an input or output.
4	D1	Drain Terminal of MUX1. Can be an input or output.
5	S2A	A-Side Source Terminal of MUX2. Can be an input or output.
6	S2B	B-Side Source Terminal of MUX2. Can be an input or output.
7	D2	Drain Terminal of MUX2. Can be an input or output.
8	GND	Ground Reference.
9	D3	Drain Terminal of MUX3. Can be an input or output.
10	S3B	B-Side Source Terminal of MUX3. Can be an input or output.
11	S3A	A-Side Source Terminal of MUX3. Can be an input or output.
12	D4	Drain Terminal of MUX4. Can be an input or output.
13	S4B	B-Side Source Terminal of MUX4. Can be an input or output.
14	S4A	A-Side Source Terminal of MUX4. Can be an input or output.
15	$\overline{EN}$	MUX Enable Logic Input. Enables or disables the multiplexers (see Table 4).
16	V_{DD}	Positive Power Supply Voltage.

TERMINOLOGY

V_{DD}
Most positive power supply potential.

I_{DD}
Positive supply current.

GND
Ground (0 V) reference.

S
Source terminal. Can be either an input or an output.

D
Drain terminal. Can be either an input or an output.

IN
Logic control input.

V_D (V_S)
Analog voltage on terminals D, S.

R_{ON}
Ohmic resistance between D and S.

$R_{FLAT (ON)}$
Flatness is defined as the difference between the maximum and minimum value of on resistance as measured.

ΔR_{ON}
On resistance match between any two channels.

I_S (Off)
Source leakage current with the switch off.

I_D (Off)
Drain leakage current with the switch off.

I_D, I_S (On)
Channel leakage current with the switch on.

V_{INL}
Maximum input voltage for Logic 0.

V_{INH}
Minimum input voltage for Logic 1.

I_{INL} (I_{INH})
Input current of the digital input.

C_S (Off)
Off switch source capacitance. Measured with reference to ground.

C_D (Off)
Off switch drain capacitance. Measured with reference to ground.

C_D, C_S (On)
On switch capacitance. Measured with reference to ground.

C_{IN}
Digital input capacitance.

t_{ON}
Delay time between the 50% and the 90% points of the digital input and switch on condition.

t_{OFF}
Delay time between the 50% and the 90% points of the digital input and switch off condition.

t_{BBM}
On or off time measured between the 80% points of both switches when switching from one to another.

Charge Injection
A measure of the glitch impulse transferred from the digital input to the analog output during on/off switching.

Off Isolation
A measure of unwanted signal coupling through an off switch.

Crosstalk
A measure of unwanted signal that is coupled through from one channel to another as a result of parasitic capacitance.

–3 dB Bandwidth
The frequency at which the output is attenuated by 3 dB.

On Response
The frequency response of the on switch.

Insertion Loss
The loss due to the on resistance of the switch.

THD + N
The ratio of the harmonic amplitudes plus noise of a signal to the fundamental.

TYPICAL PERFORMANCE CHARACTERISTICS

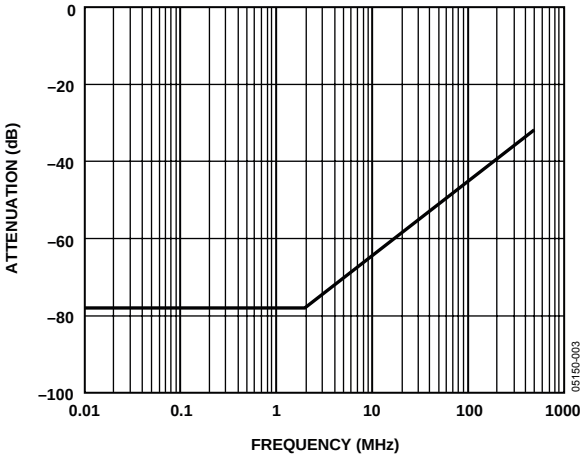

Figure 3. Off Isolation vs. Frequency

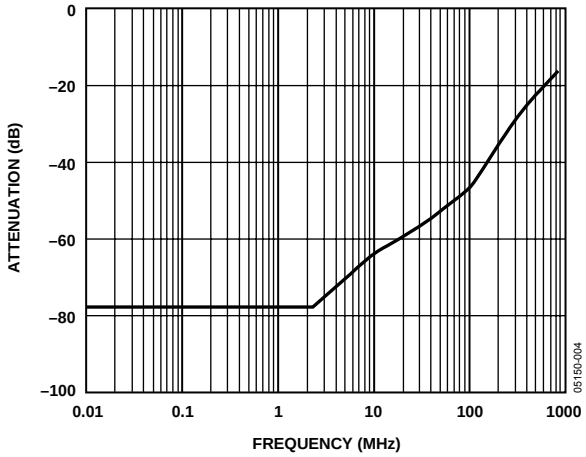

Figure 4. Crosstalk vs. Frequency

TYPICAL APPLICATION

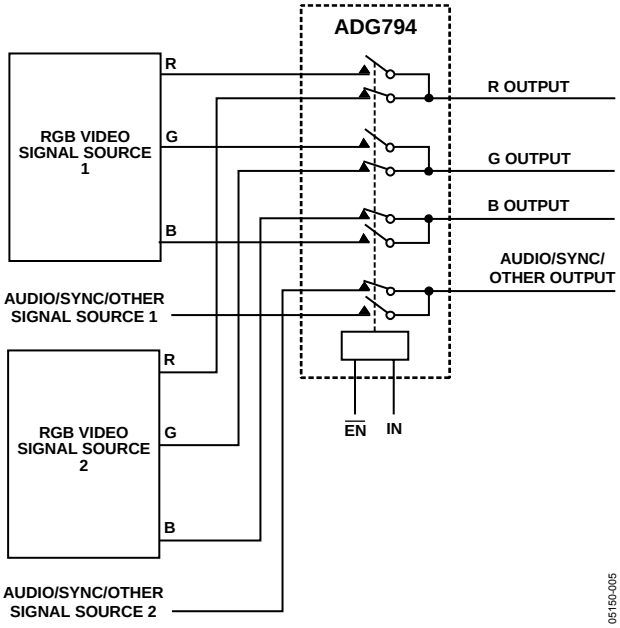

Figure 5. Audio/Video Switch

TEST CIRCUITS

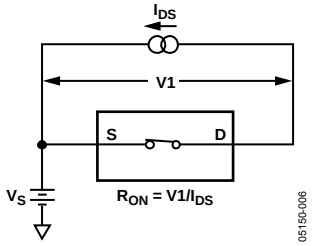

Figure 6. On Resistance

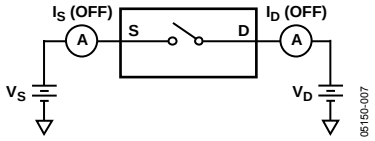

Figure 7. Off Leakage

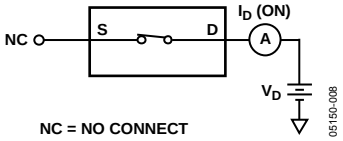

Figure 8. On Leakage

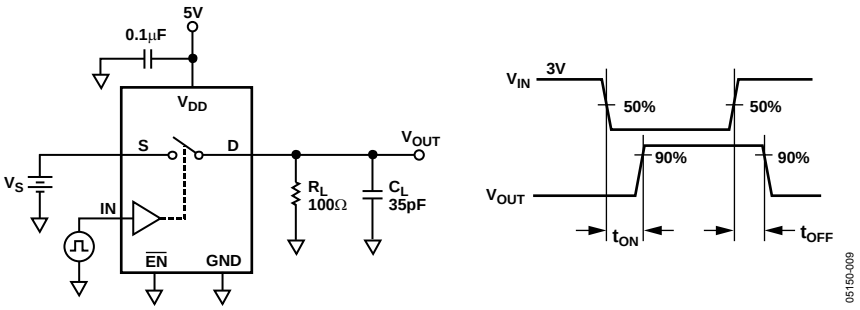

Figure 9. Switching Times

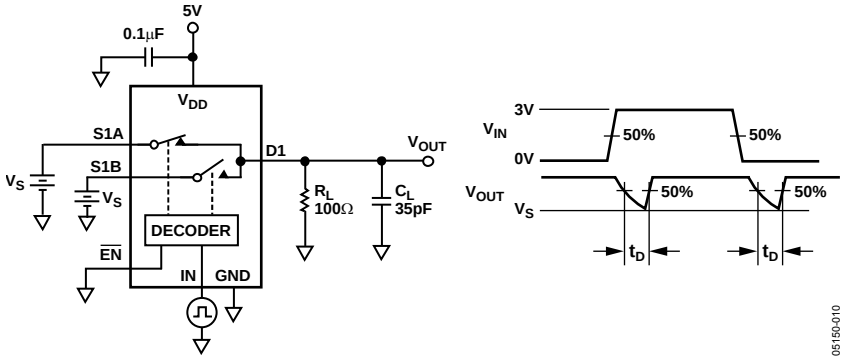

Figure 10. Break-Before-Make Time Delay

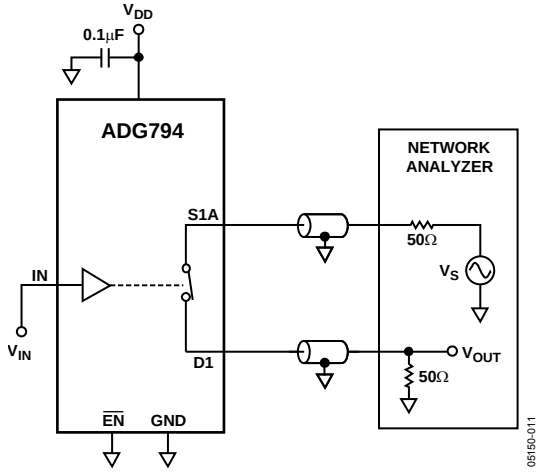

Figure 11. Bandwidth

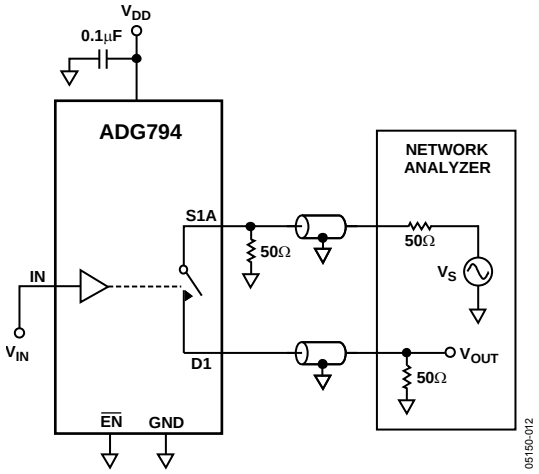

Figure 12. Off Isolation

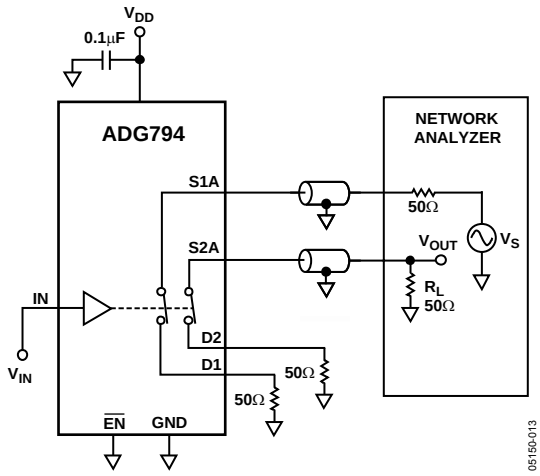

Figure 13. Channel-to-Channel Crosstalk

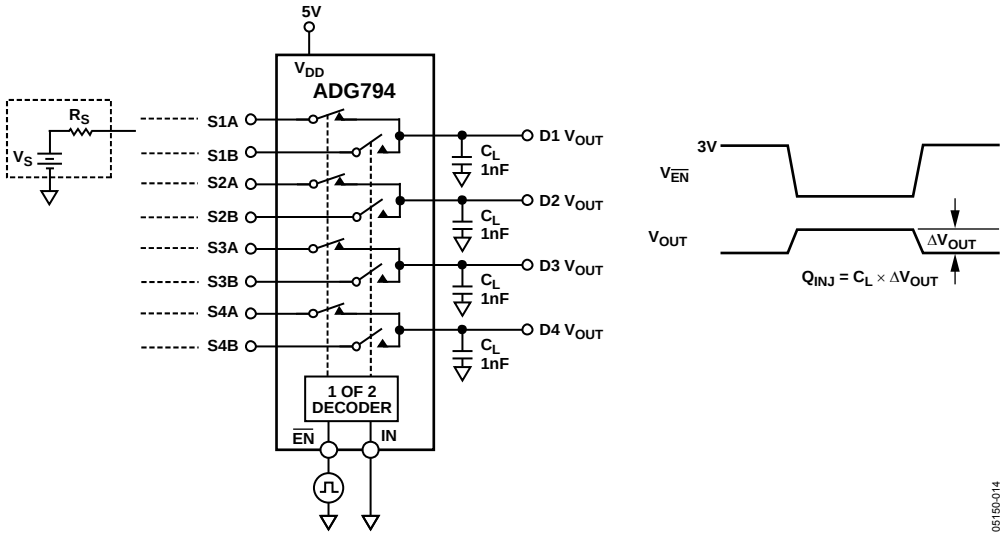

Figure 14. Charge Injection

OUTLINE DIMENSIONS

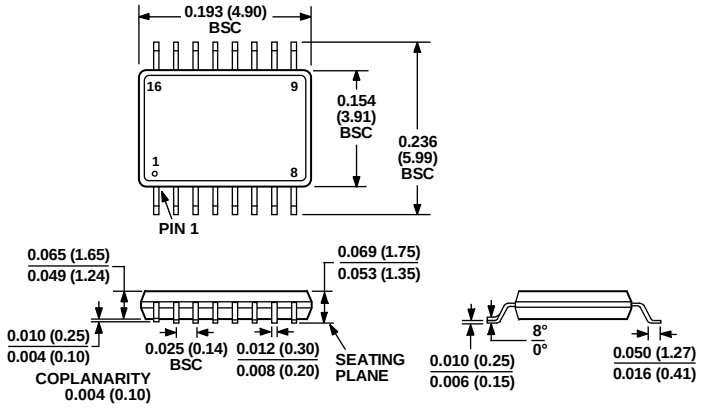

Figure 15. 16-Lead Shrink Small Outline Package [QSOP]
(RQ-16)
Dimensions shown in inches and (millimeters)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADG794BRQZ[1]	−40°C to +85°C	16-Lead Shrink Small Outline Package (QSOP)	RQ-16
ADG794BRQZ-500RL7[1]	−40°C to +85°C	16-Lead Shrink Small Outline Package (QSOP)	RQ-16
ADG794BRQZ-REEL[1]	−40°C to +85°C	16-Lead Shrink Small Outline Package (QSOP)	RQ-16
ADG794BRQZ-REEL7[1]	−40°C to +85°C	16-Lead Shrink Small Outline Package (QSOP)	RQ-16

[1] Z = Pb-free part.

NOTES

D05150–0–10/04(0)