CYPRESS

ICD2062B

Dual Programmable ECL/TTL Clock Generator

Features

- **Second generation dual oscillator graphics clock generator**
- **PECL Video Outputs: 508 kHz to 165 MHz**
- **TTL Outputs: 508 kHz to 120 MHz**
- **Individually programmable PLLs using a highly reliable, Manchester-encoded, 21-bit serial data word**
- **2-pin serial programming interface allows direct connection to most graphics chip sets with no external hardware required**
- **Programmable video clock dividers allow for easy interface to most RAMDACs and VRAMs**
- **Three-state oscillator control disables outputs for test purposes**
- **Phase-locked loop oscillator input derived from single 14.318 MHz crystal**
- **Sophisticated internal loop-filter requires no external components**
- **5V operation**
- **Low-power, high-speed CMOS technology**
- **Available in 20-pin SOIC package configuration**

Functional Description

The ICD2062B is a clock generator for high-resolution video displays. It uses a low-frequency, low-cost reference crystal to produce the following: a 10 K compatible complementary ECL output signal for high-speed video RAMDACs, a high-speed TTL output signal for video RAMs and system logic operation, and the requisite load, control, and clock signals to control the loading of data between the CRT controller, VRAM, and RAMDACs.

The ICD2062B Dual Programmable Clock Generator offers two fully user-programmable phase-locked loops in a single package. The outputs may be changed "on the fly" to any desired frequency value in the range 508 kHz to 165 MHz (VCLKOUT) and 508 kHz to 120 MHz (MCLKOUT). The ICD2062B is ideally suited for any design where multiple or varying frequencies are required, replacing more expensive metal can oscillators, particularly where the application requires expensive complementary ECL oscillators.

The Video Clock output may be programmatically divided—by 1, 2, 3, 4, 5, or 8—in order to generate the Load Signal, which is further divided by 2 and 4 for clocking video timing logic. A second Load Signal may be synchronously gated in order to enable starting and stopping the clocking of video RAMs. The ICD2062B can also configure the pipeline delay of certain RAMDACs (such as the Bt457/458) to a fixed pipeline delay.

Some examples of the uses for this device include: graphics board dot clocks to allow dynamic synchronization with different brands of monitors or display formats; and on-board test strategies where the ability to skew a system's desired frequency (for example: ±10%) allows worst case evaluations.

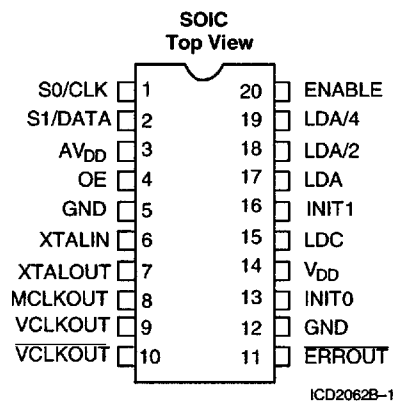
ICD2062A vs. ICD2062B

The ICD2062B revision of the ICD2062A is a complete mask redesign which includes feature enhancements as well as minor bug fixes. The following points detail the differences between the two versions.

The ICD2062B offers the following new features:

- **New VCO**—The primary difference between the A and B versions is the design of the internal VCO. The ICD2062B video VCO has been redesigned to support frequencies up to 165 MHz (see above);
- **Higher Upper Frequency Limit (VCLKOUT)**—165 MHz;
- **New Register Initialization ROM**—A new ROM allows the ICD2062B to be initialized to higher default frequencies;
- **More Load Clock divisors**—The ICD2062B Load Clock divisors of 1, 2, 3, 4, 5, and 8.

Pin Configuration



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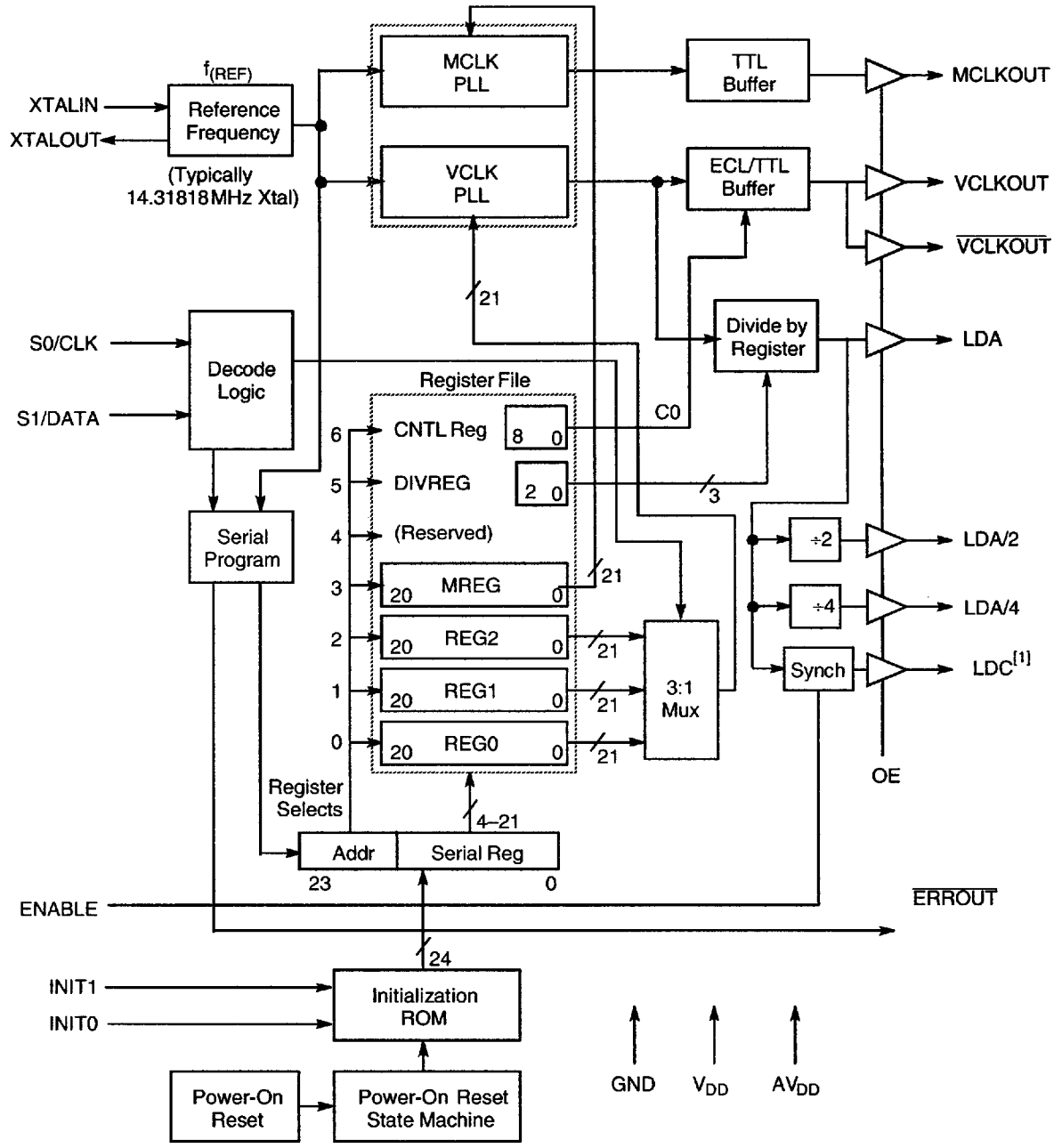
March 1995 – Revised July 16, 1997

Logic Block Diagram



Note:
1. If ENABLE =1, then LDC = synch. copy of LDA, else LDC = 0.

Pin Summary

Name	Number	Description
S0/CLK	1	Bit 0 (LSB) of frequency select logic, used to select output frequencies. Clock Input in serial programming mode. (Internal pull-down allows no-connect.)
S1/DATA	2	Bit 1 (MSB) of frequency select logic, used to select output frequencies. Data Input in serial programming mode. (Internal pull-down allows no-connect.)
AV_{DD}	3	+5V to Analog Core
$\overline{OE}$	4	Output Enable three-states output when signal is LOW (pin has internal pull-up.)
GND	5	Ground
XTALIN[2]	6	Reference Oscillator input for all phase-locked loops (nominally from a parallel-resonant 14.31818 MHz crystal). Optionally PC System Bus Clock.
XTALOUT[2]	7	Oscillator Output to a reference crystal. (Pin is no-connect if external reference oscillator or PC System Bus clock signal is used.)
MCLKOUT	8	Memory Clock output
VCLKOUT	9	Differential clock outputs. Connect directly to RAMDAC CLOCK inputs. Can drive 4 RAMDACs. Output levels equivalent to 10 K ECL circuit operating from single supply. $\overline{VCLKOUT}$ is skew-free.
$\overline{VCLKOUT}$	10	Differential clock outputs. Connect directly to RAMDAC CLOCK inputs. Can drive 4 RAMDACs. Output levels equivalent to 10 K ECL circuit operating from single supply. $\overline{VCLKOUT}$ is skew-free.
$\overline{ERROUT}$	11	Error Output: a LOW signals an error during serial programming.
GND	12	Ground
INIT0	13	Select power-up initial conditions (LSB) (Internal pull-down allows no-connect.)
V_{DD}	14	+5V to I/O Ring
LDC	15	Load output (TTL compatible). When ENABLE is HIGH, has same timing as LDA output. Can drive up to 4 capacitive loads without buffering.
INIT1	16	Select power-up initial conditions (MSB) (Internal pull-down allows no-connect.)
LDA	17	Skew-free Load Outputs (TTL compatible). Generated by dividing VCLKOUT by Div Register (1, 2, 3, 4, 5, or 8). Each output can drive up to 4 capacitive loads without buffering.
LDA/2	18	Generated by dividing LDA by two.
LDA/4	19	Generated by dividing LDA by four.
ENABLE	20	Synchronous load enable input. Internally synched to LDA, used to start/stop LDC output synchronously. If ENABLE is LOW, LDC is held LOW; when HIGH, LDC is free-running.

Note:
2. For best accuracy, use a parallel-resonant crystal, assume C_{LOAD}=17 pF.

Register Definitions

Register File

The Register File consists of the following registers and their selection addresses:

Table 1. Register Addressing

Address	Register	Usage
000	REG0	Video Clock Register 1
001	REG1	Video Clock Register 2
010	REG2	Video Clock Register 3
011	MREG	Memory or I/O Timing Clock
100	(Reserved)	
101	DIVREG	Load Divisor Register
110	CNTL Reg	Control Register

Register Selection

The Video Clock output is controlled not only by the S0 and S1 bits, but also by the OE signal as shown in *Table 2.*

Table 2. VCLKOUT Selection

OE	S1	S0	VCLKOUT
0	X	X	High-Z
1	0	0	REG0
1	0	1	REG1
1	1	X	REG2

The Memory Clock output is controlled by the OE signal as indicated in *Table 3.*

Table 3. MCLKOUT Selection

OE	VCLKOUT
0	High-Z
1	MREG

The Clock Select pins S0 and S1 have a dual purpose. When these pins are performing serial download, the VCLKOUT signal remains unchanged (unless the currently selected register is the one being programmed). When the pins S0 and S1 are functioning as register selects, a timeout interval is required to determine whether the user desires register select or serial programming. At the end of the timeout interval, new register selection occurs. At this point, the VCLKOUT signal will be multiplexed to the reference signal $f_{(REF)}$ for an additional timeout interval to allow the VCO to settle to its new value. (The timeout interval in both cases is approximately 5 msec—see the timeout interval spec in *Switching Characteristics.*)

When a new frequency is being set for MCLK, or if the active VCLK register is being programmed, then a glitch-free multiplexing to the Reference Frequency is performed. Once the STOP bit is sent after the MCLK or active VCLK Programming Word, the appropriate output signal will be multiplexed to the reference signal $f_{(REF)}$ for an extra timeout interval (See *Switching Characteristics* for further details).

Control Register Definition

The Control Register (CNTL Reg) allows the user to adjust various internal options. Most of these options are for special cases, and should have no applicability to standard graphics usage. The register word is defined in *Figure 1.*

MUXREF—This control bit determines which clock is multiplexed to the VCLKOUT output during frequency changes. While the VCLK VCO changes to a different frequency, a known clock is multiplexed to the output. The default is to multiplex the $f_{(REF)}$ reference frequency, but some graphics controllers cannot run as slow as $f_{(REF)}$. This bit, when set, allows the MCLK to be used as an alternative frequency.

Timeout Interval—The timeout interval is normally defined as in the *Switching Characteristics.* It is derived from the MCLK VCO, and if this VCO is programmed to certain extremes, then the timeout may be too short. If this control bit is set, then the timeout interval is doubled.

RAMDAC Reset—This control bit, when set, will cause the ICD2062B to issue a RAMDAC reset sequence, which is required by some specific RAMDACs (such as the Bt457/458). For more specifics on this operation, refer to the section *Internal RESET Sequence.* NOTE: This operation will only take place the first time this bit is set.

Duty Cycle Adjust—This control bit causes a 1 ns decrease in the output waveform high time. The default is no adjustment. In situations in which the capacitive load is beyond device specifications, or where the threshold voltage V_{TH} is to be changed from CMOS to TTL levels, this adjustment can sometimes bring the output closer to 50% duty cycle.

VCLKOUT Pad—This control bit determines whether the VCLKOUT Pad is at ECL or TTL levels. The default is ECL levels. When in TTL mode, the $\overline{\text{VCLKOUT}}$ Pad is nonfunctional, and remains three-stated.

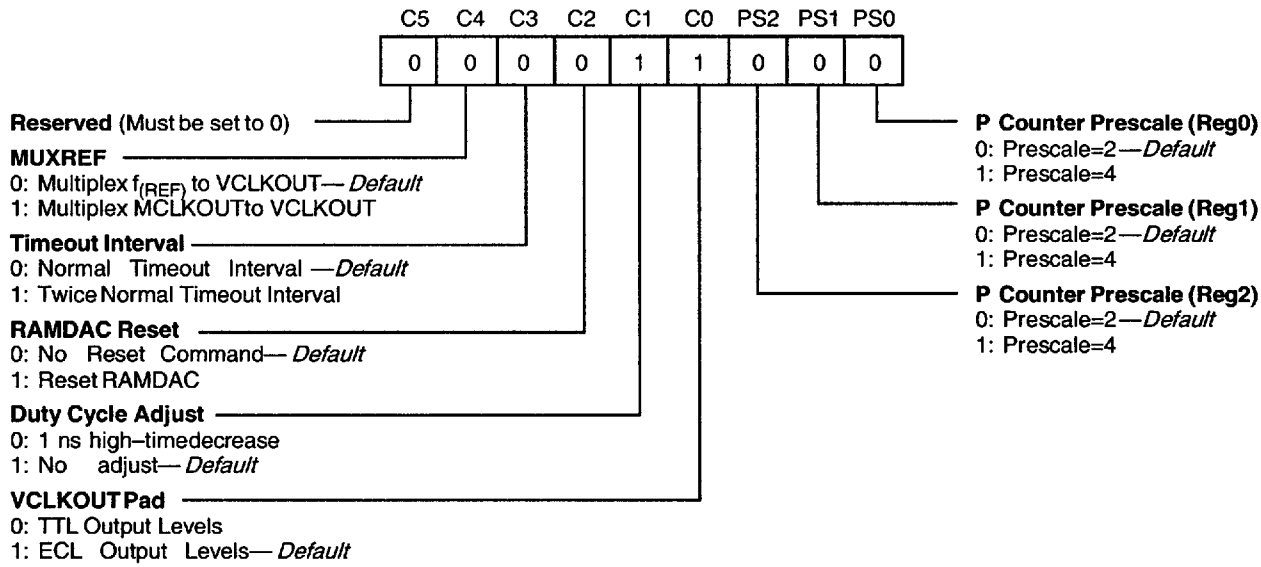


Figure 1. Control Register Definition

P Counter Prescale (REG0, REG1, REG2)—These control bits determine whether or not to prescale the P Counter value, which allows fine tuning the output frequency of the respective register. Prescaling is explained in more detail later in this datasheet.

Divide Register Definition

The output signals LDA, LDA/2, LDA/4, and LDC are all a function of the VCLK VCO value divided by the division factor stored in the Divide Register (DIVREG). The maximum LDA and LDC output is 100 MHz.

Table 4. DIVREG Division Factors

D2	D1	D0	Division Factor	Clock LOW (cycles)	Clock HIGH (cycles)	Device Version
1	0	X	÷1	1/2	1/2	A&B
1	1	X	÷2	1	1	A&B
0	0	0	÷3	1	2	B
0	0	1	÷4	2	2	B[3]
0	1	0	÷5	2	3	B
0	1	1	÷8	4	4	B

Note:
3. Default on power-up.

Serial Programming Architecture

The ICD2062B programming scheme is simple, yet impenetrable to accidental access. Because the only common denominator between most VGA and 8514 controllers is a few clock select pins, these have to perform the dual functions of clock selection and serial programming. The Serial Program Block (see *Figure 2*) contains several components: a Serial Unlock Decoder (containing the unlocking mechanism and Manchester decoder), a watchdog timer, the Serial Data register and a Demultiplexer to the Register File.

Unlocking Mechanism

The Unlocking Mechanism watches for an initial break sequence, detailed in *Figure 3*.

The initial unlock sequence consists of at least five LOW-to-HIGH transitions of CLK with DATA HIGH, followed immediately by a single LOW-to-HIGH transition of CLK with DATA LOW. Following this unlock sequence, the encoded serial data is clocked into the Serial Data register (Serial Reg).

Watchdog Timer

Following any transition of CLK or DATA, the watchdog timer is reset and begins counting. Throughout the entire programming process, the watchdog timer ensures that successive edges of CLK or DATA do not violate the timeout specification (of 2 msec—see *Switching Characteristics*) If a timeout does occur, the lock mechanism is rearmed and the current data in the Serial Data register is ignored.

Since the VCLK registers are selected by the S0 or S1 bits, and since any change in their state may affect the resultant output frequency, new data input on the Selection Bits is only permitted to pass through to the Decode Logic after the Watchdog Timer has timed out. This delay of S0 or S1 data permits a serial program cycle to take place without affecting the current register selection. The process of serial programming has no effect on the performance of the graphics subsystem. Note that there is a latency amounting to the duration of the Watchdog Timer before any new VCLK register selections take effect.

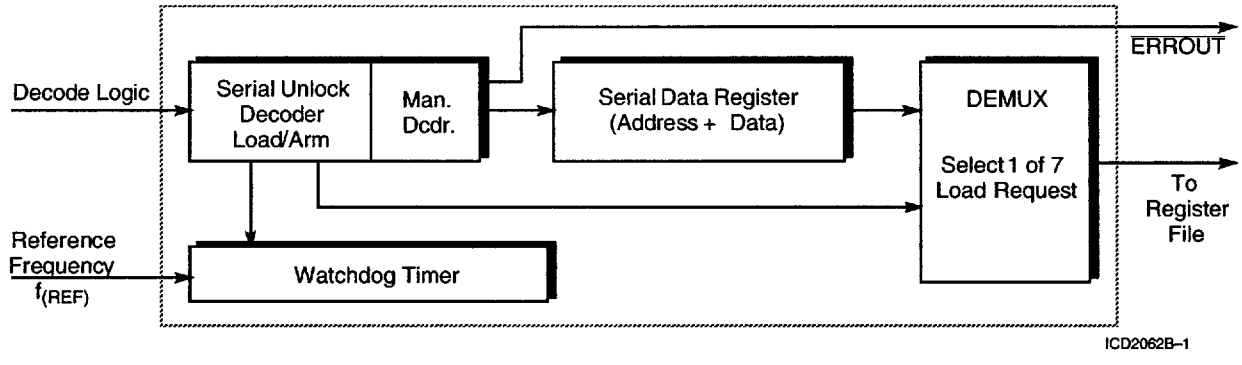


Figure 2. Serial Programming Block Diagram—Detail

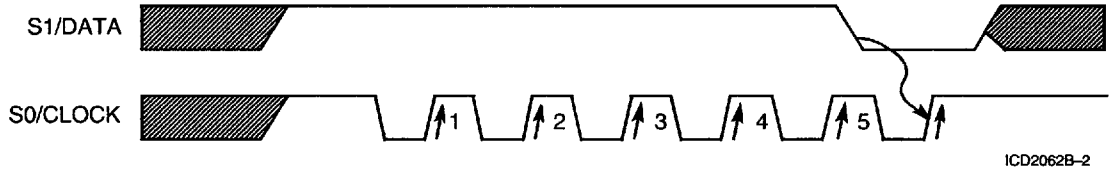


Figure 3. Unlock Sequence

Register Initialization

The ICD2062B Clock Synthesizer has all of its registers in a known state upon power-up. This is implemented by the Power-On initialization circuitry. Three pixel clock registers and the Memory Clock register are initialized based on the state of the INIT1 and INIT0 pins at power-up.

On power-on, when the supply voltage rises above a certain threshold voltage (typically 3V, may vary with temperature), the part recognizes the first 16 rising edges of the reference clock, using them as a clocking signal for internal state machines for initialization. Hence for proper initialization and programmability, the power-on reference clock pulses seen by the ICD2062B, should have as good signal integrity and rail-to-rail characteristics as the clock pulses seen under stable working conditions. This is not an issue when using a crystal as reference.

The Power-On Reset function operates transparently to the video subsystem. It performs its initialization function and is cleared before the system Power-On Reset permits the system to begin its boot process. The INIT pins must ramp up with V_{DD} if a 1 on either of these pins is desired. They are internally pulled down, and so will default to 0 if left unconnected.

The various registers are initialized as shown in *Table 5* (all frequencies in MHz).

Table 5. Register Initialization

INIT1	INIT0	MREG	REG0	REG1	REG2
0	0	32.500	25.175	28.322	28.322
0	1	40.000	25.175	28.322	28.322
1	0	50.350	110.000	135.000	165.000
1	1	56.644	110.000	135.000	185.000

Serial Data Register

Serial data is clocked into the Serial Data register in the order shown in *Figure 4.*

The serial data is sent using a modified Manchester-encoded data format. This is defined as:

1. An individual data bit is sampled on the rising edge of CLK.
2. The complement of the data bit must be sampled on the previous falling edge of CLK.
3. The Set-Up and Hold Time requirements must be met on both CLK edges.
4. The unlock sequence, start, and stop bits are not Manchester-encoded.

For specifics on timing, see the "Serial Programming Timing" section in the switching waveforms.

The bits are shifted in this order: a start bit, 21 data bits, 3 address bits (which designate the desired register), and a stop bit (which also functions as a load strobe to transfer the data from the Serial Reg into the desired register). For the VCO registers (REG0, REG1, REG2, MREG), the data is made up of 4 fields: D[20:17] = Index; D[16:10]=P'; D[9:7]=Mux; D[6:0]=Q'. (See the *Programming the ICD2062B* section for more details on the VCO data word.) For the other registers with fewer than 21 bits (DIVREG, CNTL Reg), the upper bits are used (starting with the MSB). A total of 24 bits must always be loaded into the Serial Data register (or an error is issued). Undefined bits should always be set to zero to maintain software compatibility with future enhancements.

Following the entry of the last data bit, a stop bit or Load command is issued by bringing DATA HIGH and toggling CLK HIGH-to-LOW and LOW-to-HIGH. The unlocking mechanism then automatically rearms itself following the load. Only when the watchdog timer has timed out are the S0 and S1 selection pins permitted to return to their normal register select function.

Note that the Serial Data register that receives the address and data bits is exactly the correct length to accept the data being sent. The stop bit is used as a load command that passes the Serial Data Reg contents on to the register file location indicated by the address bits. If a stop bit is not received after the Serial Data register has been filled, but rather more valid encoded data is received, then all of the received serial data is ignored, the unlocking mechanism rearmed, and an error is issued. The device counts the serial data clock edges to know exactly when the serial buffer is full, and thus to know which bit is the stop bit. Following the stop bit, the unlocking mechanism rearms itself. If corrupt data is detected (i.e., incorrectly Manchester-encoded data), then the unlocking mechanism is rearmed, the serial counter reset, all received data ignored, and $\overline{\text{ERROUT}}$ is asserted.

$\overline{\text{ERROUT}}$ Operation

The $\overline{\text{ERROUT}}$ signal is used to announce when a program error has been detected internally by the ICD2062B. The signal remains LOW until the next unlock sequence.

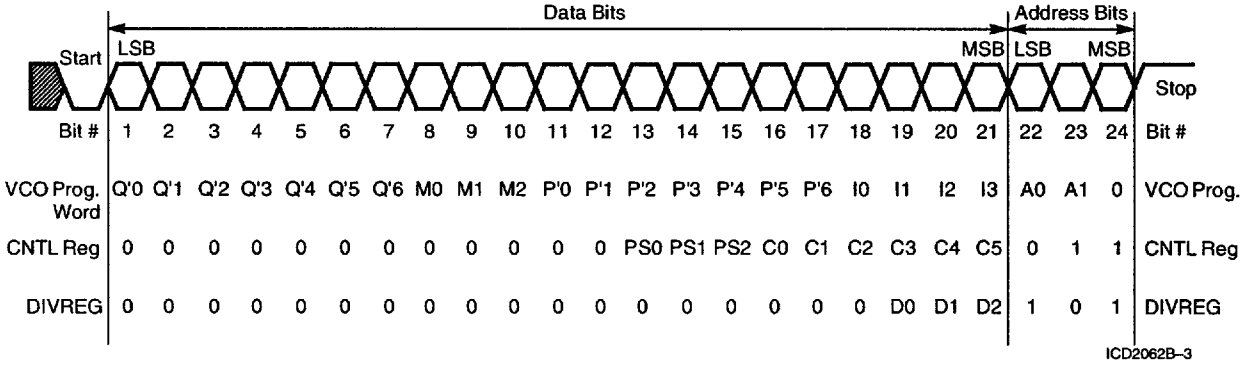


Figure 4. Serial Data Timing

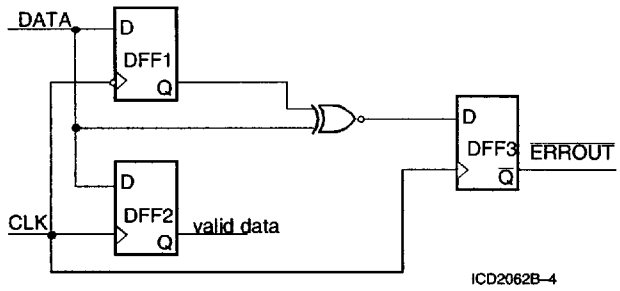


Figure 5. Modified Manchester Decoder Circuit

Figure 5 shows the basic mechanism used to detect erroneous serial data. Note that the circuit must have different values on the rising and falling edge when sampling the falling edge first. Valid data is read on the rising edge of CLK.

The $\overline{\text{ERROUT}}$ signal is invoked for any of the following error conditions: incorrect start bit, incorrect Manchester encoding; incorrect length of data word; incorrect stop bit.

Note that if there is no input pin available on the target VGA controller chip to monitor $\overline{\text{ERROUT}}$, a software routine which counts VSYNC pulses in order to measure output frequency may be used as a determination of programming success.

Programming the ICD2062B

The desired output frequency is defined via a serial interface, with a 21-bit number shifted in. The ICD2062B has two programmable oscillators, requiring a 21-bit programming word (W) to be loaded into each channel's respective registers independently. This word contains 4 fields, as shown in *Table 6*.

Table 6. Programming Word Bit Fields

Field	# of bits	Notes
Index (I)	4	MSB (Most Significant Bits)
P Counter value (P')	7	
Mux (M)	3	
Q Counter value (Q')	7	LSB (Least Significant Bits)

The frequency of the Programmable Oscillator $f_{(VCO)}$ is determined by these fields as follows:

P'=P–3
Q'=Q–2
$f_{(VCO)}=(2 \times f_{(REF)} \times P/Q)$

where $f_{(REF)}$=Reference frequency (typically 14.31818 MHz)

Note that if a reference frequency other than 14.31818 MHz is used, then the initially loaded ROM frequencies will not be correct.

The value of $f_{(VCO)}$ must remain between a minimum and maximum frequency. These limits vary depending on the clock (MCLK or VCLK). See *Table 7* for the actual boundary frequencies in each case. For output frequencies below the minimum, $f_{(VCO)}$ must be brought into range. To accomplish this, a post-VCO divisor is selected by setting the values of the Mux field (M). See *Table 7*.

Table 7. Post-VCO Divisor

M	Divisor
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The Index Field (I) is used to preset the VCO to an appropriate range. The value for this field should be chosen from *Table 8*. (This table is referenced to the VCO frequency, $f_{(VCO)}$, rather than to the desired output frequency.) Note that VCLK may be shut off, but that MCLK must be left running.

When the Index Field is set to 1111, VCLK is turned off and both channels run from the same MCLK VCO. To reduce jitter, the two VCOs should not run at integral multiples of each other; therefore, to allow the output clocks to run at 2^n (n=0, 1, 2 .. 7) multiples of each other, turn off the VCLK VCO and multiplex the MCLK VCO over to VCLKOUT, dividing down to the desired frequency. This will significantly reduce heterodyne jitter.

If the desired VCO frequency lies on a boundary in the table—in other words, if it is exactly the upper limit of one entry and the lower limit of the next—then either index value may be used (since both limits are tested) but the higher value should be used.

To assist with these calculations, Cypress/IC Designs provides *BitCalc* (Part #ICD/BCALC), a Windows™ program that automatically generates the appropriate programming words from the user's reference input and desired output frequencies, as well as assembling the program words for such things as control and power-down registers.

Table 8. Index Field (I)

I	VCLK f_{VCO} (MHz)	MCLK f_{VCO} (MHz)
0000	65.0 – 70.7	Reserved
0001	70.7 – 77.8	52.0 – 55.0
0010	77.8 – 85.6	55.0 – 60.0
0011	85.6 – 88.0	60.0 – 68.0
0100	88.0 – 94.2	68.0 – 70.0
0101	94.2 – 96.8	70.0 – 75.0
0110	96.8 – 106.5	75.0 – 80.0
0111	106.5 – 111.7	80.0 – 84.5
1000	111.7 – 117.2	84.5 – 90.0
1001	117.2 – 122.8	90.0 – 95.0
1010	122.8 – 135.1	95.0 – 100.0
1011	135.1 – 148.6	100.0 – 104.0
1100	148.6 – 160.0	104.0 – 110.0
1101	160.0 – 165.0	110.0 – 120.0
1110	Turn off VCLK	110.0 – 120.0
1111	Mux MCLK > VCLK	110.0 – 120.0

Programming Constraints

There are five primary programming constraints of which the user must be aware:

Table 9. Programming Constraints

Parameter	Minimum	Maximum
$f_{(REF)}$	1 MHz	25 MHz
$f_{(REF)}/Q$	200 kHz	1 MHz
$f_{(VCO)}$	VCLK: 65 MHz MCLK: 52 MHz	VCLK: 165 MHz MCLK: 120 MHz
Q	3	129
P	4	130

The constraints have to do with trade-offs between optimum speed with lowest noise, VCO stability, and factors affecting the loop equation. The factors are listed here for completeness' sake; however, by using the *BitCalc* program, these constraints become transparent.

Programming Example—Prescaling=2 (default)

The following is an example of the calculations *BitCalc* performs:

Derive the proper programming word for a 39.5 MHz VCLK output frequency, using 14.31818 MHz as the reference frequency:

Since 39.5 MHz<50 MHz, double it to 79.0 MHz. Set M to 001. Set I to 0010. The result:

$f_{(VCO)}=79.0=(2 \times 14.31818 \times P/Q)$
$P/Q = 2.7587$

Table 10. P&Q Value Pairs

P	Q	$f_{(VCO)}$ (MHz)	Error (PPM)
69	25	79.0363	460
80	29	78.9969	40
91	33	78.9669	419

Choose (P, Q)=(80,29) for best accuracy (40 PPM).

Therefore:

P'=P–3=80–3=77=1001101 (4dH)
Q'=Q–2=29–2=27=0011011 (1bH)

and the full programming word, W is obtained by concatenating:

I=0010, P'=1001101, M=001, Q'=0011011
=001010011010010011011 (05349bH)

The programming word W is then sent as a serial bit stream, LSB first. Appropriate start and stop bits must also be included as defined in the Serial Programming Architecture section.

Programming Example—Prescaling=4

Assume the desired VCLKOUT frequency is 100 MHz. *Table 11* compares the results of using the default prescaling value of 2 and the optional prescaling value of 4.

Table 11. Prescale Values

Prescale	Actual Frequency (MHz)	P	Q	Error (PPM)
2	99.84028	129	37	1600
4	99.99998	110	63	0

But this precision has its price, namely that the user now has to set and reset the Prescale Bits PS0-2 (corresponding to REG0-2), which involves loading a Control Word (taking care to preserve the current values of the other Control Bits), before the VCO Program Word can be loaded. Once the appropriate Prescale Bits are set, then frequency programming can proceed as before, unless and until it is desired to program a new frequency without prescaling, at which point a new Control Word must first be loaded with the proper bits set, and observing the precautions noted above.

To summarize, the sequence is:

1. Set the Prescale bits (load a Control Word)
2. Program the VCO (load a Program Word)

Note that care must be taken not to change the Prescale Bit of the currently active register: The results will be unpredictable at best, and it could cause the VCO to go out of lock.

RAMDAC/VRAM Interface

Interfacing to the RAMDAC

Figure 6 shows how to interface the ICD2062B to a RAMDAC. The part should be located as close to the RAMDAC as possible. Termination resistors are needed on the VCLKOUT outputs, and should be located as close as possible to the RAMDAC. For specific information, please refer to the Cypress/IC Designs application note *ECL Outputs*.

The ICD2062B may drive the CLOCK inputs of up to four RAMDACs, if they are located physically adjacent to each other. In this case, only 2 sets of termination resistors should be used, and these should be located closest to the farthest RAMDAC from the ICD2062B.

Typical ICD2062B Usage

The DIVREG register holds the divisor, which can be 1, 2, 3, 4, 5, or 8, by which the pixel clock is divided to generate the load signals: LDA, LDA/2, and LDA/4.

The ENABLE input is synchronized internally to LDA; it may be used to start and stop the LDC output synchronously. When ENABLE is LOW, LDC is held LOW. When ENABLE is HIGH, then LDC will be free-running and in phase with LDA. This allows the video DRAM shift registers to be non-clocked during the retrace intervals. Note that for fanouts greater than 4, LDC needs to be buffered.

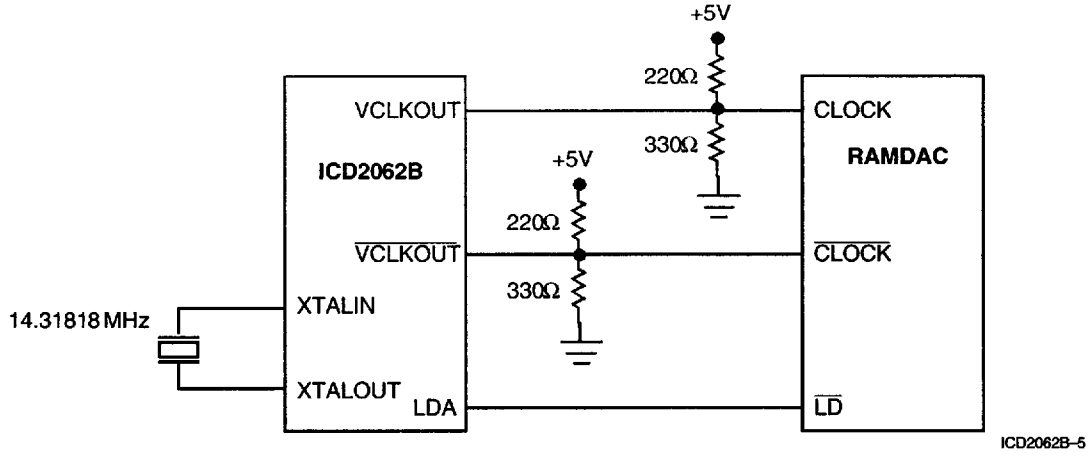


Figure 6. ICD2062B to RAMDAC Interface Example

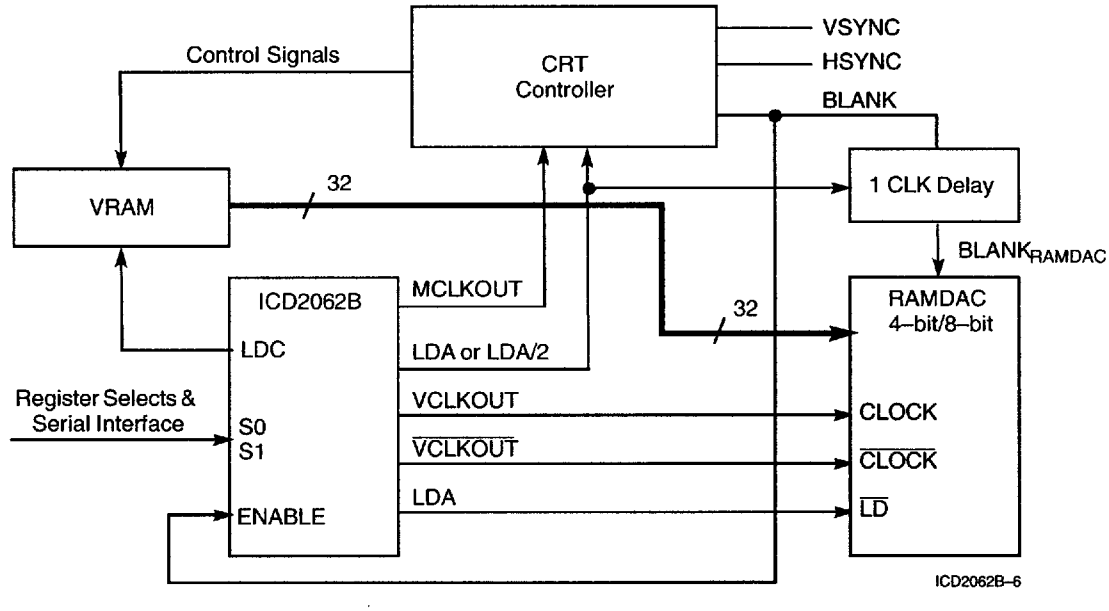


Figure 7. ICD2062B Typical Interface Circuit

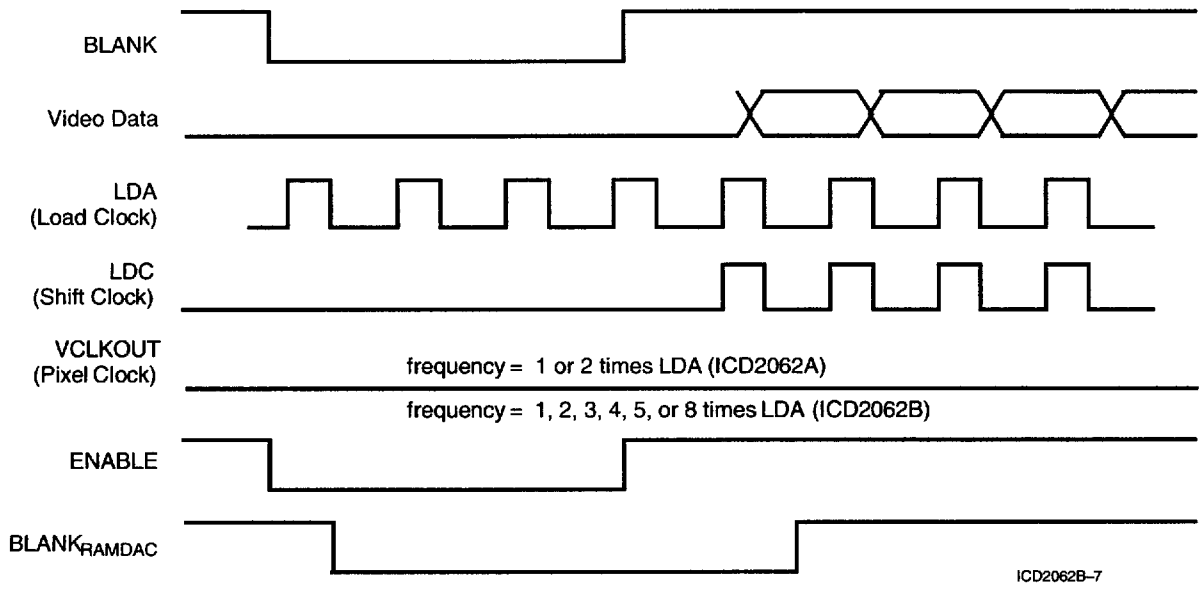


Figure 8. Timing Diagram for Interface Circuit

Internal RESET Sequence

The internal RESET signal allows the ICD2062B to set the RAMDAC pipeline delay to a specific cycle count, depending on the RAMDAC. Reset takes place the first time the Control Register's Reset Bit is set. Following the rising edge of LDA/4 after the Reset Bit is set, the VCLKOUT and $\overline{\text{VCLKOUT}}$ outputs are stopped HIGH and LOW, respectively; at the next rising edge of LDA/4, these outputs are again allowed to be free-running. *Figure 9* shows the operation of the internal RESET signal.

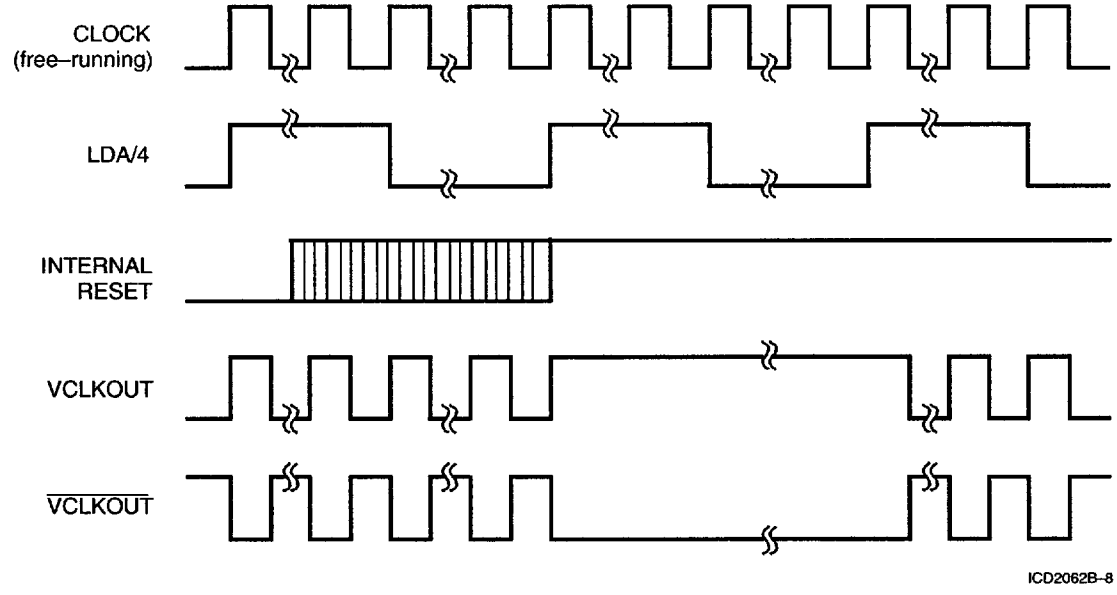


Figure 9. Internal RESET Timing

Power Management Issues

Estimating Total Current Drain

Actual current drain is a function of frequency and of circuit loading. The operating current of a given output is given by the equation: I=C • V • f, where

I=current,
C=load capacitance (max. 25 pF),
V=output voltage (usually 5V for TTL pads, 1.5V for ECL pads),
f=output frequency (in MHz).

To calculate total operating current, sum the following:

MCLKOUT ⇒ $C \bullet V \bullet f_{(MCLKOUT)}$
VCLKOUT ⇒ $C \bullet V \bullet f_{(VCLKOUT)}$; (ECL pad, V=1.5V)
$\overline{VCLKOUT}$ ⇒ $C \bullet V \bullet f_{(\overline{VCLKOUT})}$; (ECL pad, V=1.5V)
LDA ⇒ $C \bullet V \bullet f_{(LDA)}$
LDA/2 ⇒ $C \bullet V \bullet f_{(LDA/2)}$
LDA/4 ⇒ $C \bullet V \bullet f_{(LDA/4)}$
LDC ⇒ $C \bullet V \bullet f_{(LDC)}$
Internal ⇒ 12 mA

This gives an approximation of the actual operating current. For unconnected output pins, one can assume 5 to 10 pF loading, depending on package type.

Table 12. Typical Values

Frequency	Capacitive Load	Current (mA)
LOW	LOW	15
HIGH	LOW	50
HIGH	HIGH	100

Output Enable Pin

When the OE pin is asserted (active HIGH), all the output pins except XTALOUT and $\overline{ERROUT}$ enter a high-impedance mode, to support automated board testing.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Supply Voltage to Ground Potential ..... −0.5V to +7.0V
DC Input Voltage ..... −0.5V to V_{DD} +0.5V
Storage Temperature ..... −65°C to +150°C
Max soldering temperature (10 sec) ..... 260°C
Junction temperature ..... 125°C

Operating Range

Ambient Temperature	V_{DD} & AV_{DD}
$0°C \le T_{AMBIENT} \le 70°C$	5V ±5%

Electrical Characteristics Over the Operating Range[4]

Parameter	Description	Test Conditions	Min.	Max.	Unit
$V_{OH(ECL)}$	ECL Output HIGH Voltage[5]		V_{DD}−1.0	V_{DD}−0.8	V
$V_{OL(ECL)}$	ECL Output LOW Voltage		V_{DD}−2.0	V_{DD}−1.6	V
$V_{OH(TTL)}$	TTL Output HIGH Voltage[6]	I_{OH} = −4.0mA	2.4		V
$V_{OL(TTL)}$	TTL Output LOW Voltage	I_{OL} = 4.0 mA		0.4	V
V_{IH}	Input HIGH Voltage	Except on Crystal Pins	2.0		V
V_{IL}	Input LOW Voltage	Except on Crystal Pins		0.8	V
I_{IH}	Input HIGH Current	$V_{IH} = V_{DD}$−0.5V		150	µA
I_{IL}	Input LOW Current	V_{IL} = 0.5V		−250	µA
I_{OZ}	Output Leakage Current	Three-state outputs		10	µA
I_{DD}	Power Supply Current	A/B, Inputs @ V_{DD} and GND	15	150/200	mA
I_{DD-TYP}	Power Supply Current	Typical= 45, @ 60 MHz			mA
$C_{OUT(ECL)}$	ECL Output Capacitance			10	pF

Notes:
4. Input capacitance is typically 10 pF, except for the crystal pins.
5. ECL outputs: VCLKOUT, $\overline{VCLKOUT}$.
6. TTL outputs: MCLKOUT, LDA, LDA/2, LDA/4, LDC, $\overline{ERROUT}$.

Switching Characteristics Over the Operating Range

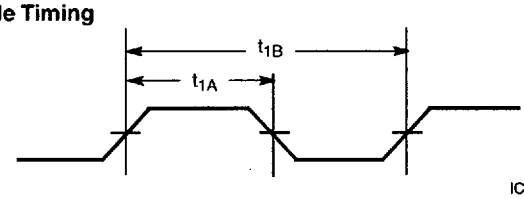
Parameter	Name	Description		Min.	Typ.	Max.	Unit
$f_{(REF)}$	Reference Frequency	Reference Oscillator nominal value (Note: for references of other than 14.318 MHz, the pre-loaded ROM frequencies will not be accurate.)		1	14.318	25	MHz
$t_{(REF)}$	Reference Clock Period	$1 \div f_{(REF)}$		40		1000	ns
t_1	Input Duty Cycle	Duty cycle for the inputs defined as $t_{1A} \div t_{1B}$		25%	50%	75%	
t_2	Output Clock Periods	Output values	ECL	6.1 165 MHz		1970 508 kHz	ns
t_2	Output Clock Periods	Output values	TTL	8.3 120 MHz		1970 508 kHz	ns
t_3	Output Duty Cycle	Duty cycle for the outputs[7]		40%		60%	
t_4	Rise Times	Rise time for the outputs into a 25-pF load				4	ns
t_5	Fall Times	Fall time for the outputs into a 25-pF load				4	ns
$t_{skew-ECL}$		Skew between the VCLKOUT complementary outputs				1	ns
t_{freq1}	freq1 Output	Old frequency output					
t_{freq2}	freq2 Output	New frequency output					
t_A	$f_{(REF)}$ Mux Time	Time clock output remains HIGH while output muxes to reference frequency		$t_{(REF)}/2$		$3(t_{(REF)}/2)$	ns
$t_{timeout}$	Timeout Interval	Internal interval for serial programming and for VCO changes to settle[8]		2	5	10	msec
t_B	t_{freq2} Mux Time	Time clock output remains HIGH while output muxes to new frequency value		$t_{freq2}/2$		$3/(t_{freq2}/2)$	ns
t_6	Three-state	Time for the outputs to go into three-state mode after OE signal assertion		0		12	ns
t_7	CLK Valid	Time for the outputs to recover from three-state mode after OE signal goes HIGH		0		12	ns
t_{LD}	Load Clock Period	Maximum LDA and LDC period		10			ns
$t_{SKEW-LDA}$		VCLKOUT to LDA output skew		2		6	ns
$t_{SKEW-LDA/2}$		LDA to LDA/2 output skew		0	1	2	ns
$t_{SKEW-LDA/4}$		LDA to LDA/4 output skew		0	1	2	ns
$t_{SKEW-LDC}$		LDA to LDC output skew		0	1	2	ns
t_{EN-SU}		ENABLE set-up time to LDA		12			ns
t_{EN-HD}		ENABLE hold time to LDA		0			ns
t_{serclk}		Clock period of serial clock		$2 \times t_{(REF)}$		2	msec
t_{HI}		Minimum HIGH time of serial clock		$t_{(REF)}$			ns
t_{LO}		Minimum LOW time of serial clock		$t_{(REF)}$			ns
t_{SU}		Set-Up time		20			ns
t_{HD}		Hold time		10			ns
t_{ldcmd}		Load command		0		t_1+30	ns

Notes:

7. For non-ECL outputs, duty cycle is measured at CMOS threshold levels. At 5V, V_{TH}=2.5V.
8. If the interval is too short, see the Timeout Interval section in the Control register definition.

Switching Waveforms

Duty Cycle Timing



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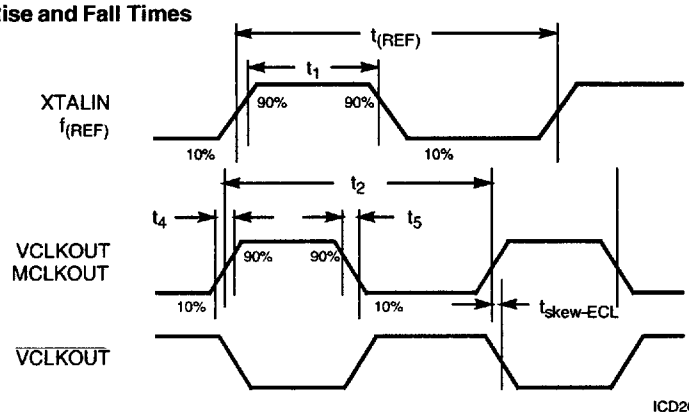
Rise and Fall Times



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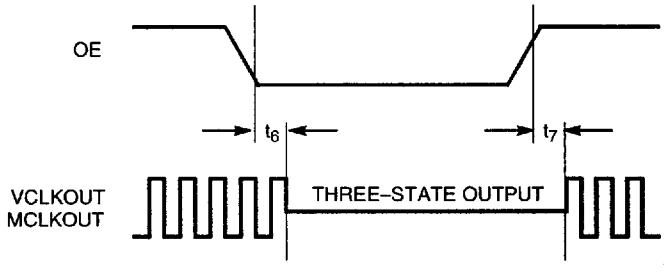
Three-State Timing



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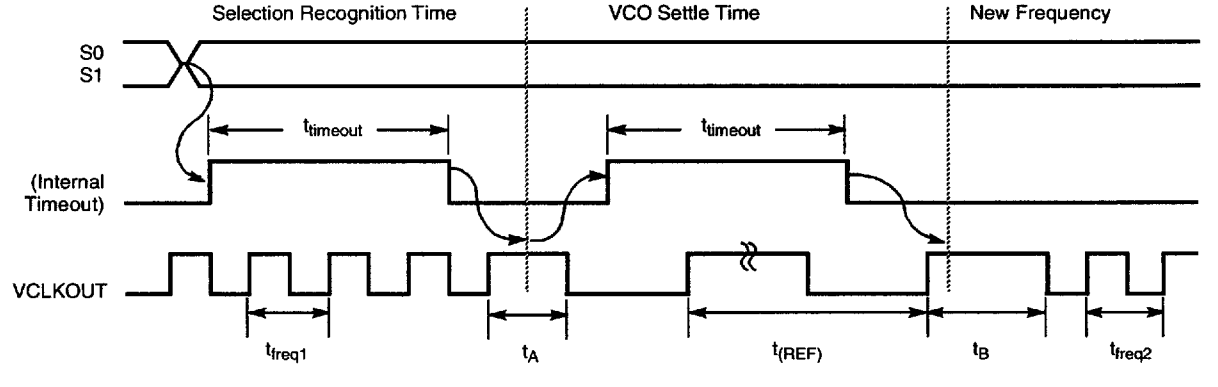
Selection Timing



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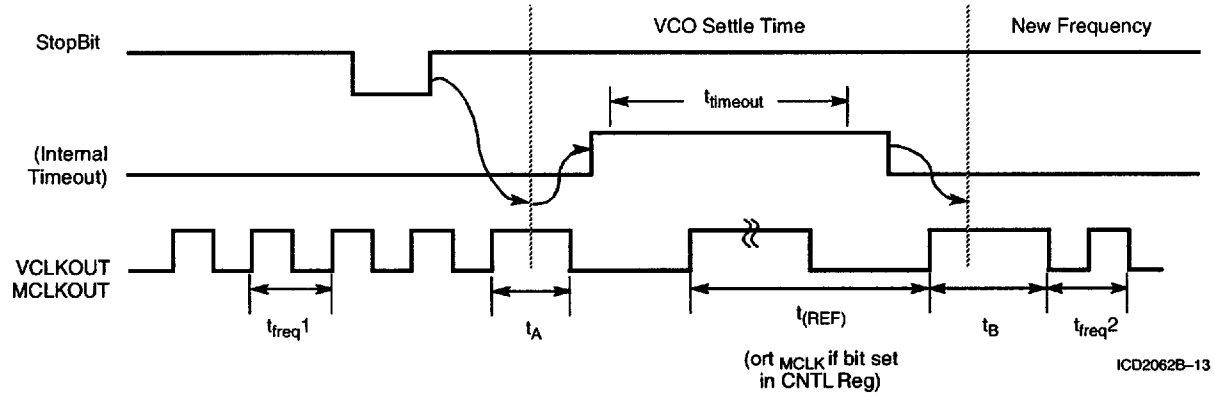
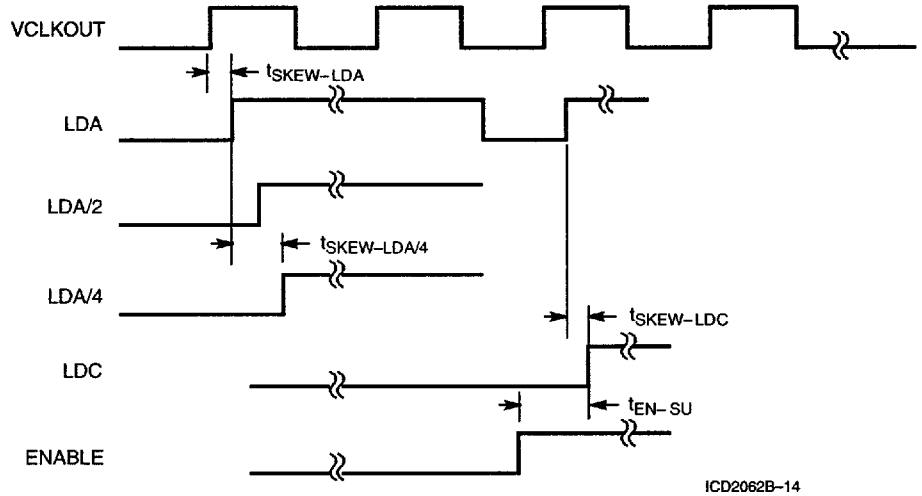
Switching Waveforms (continued)

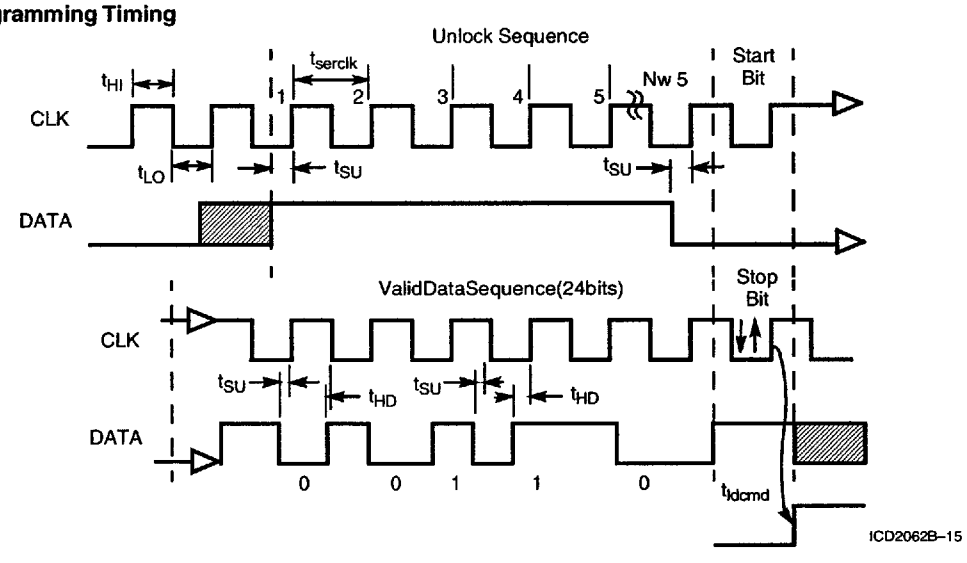
MCLK and Active VCLK Register Programming Timing



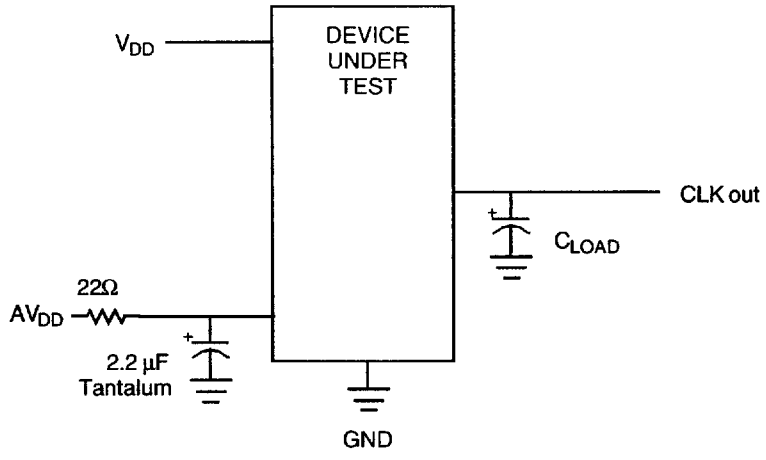
RAMDAC/VRAM Interface Timing



Serial Programming Timing



Test Circuit



Ordering Information[9]

Ordering Code	Package Name	Package Type	Operating Range
ICD2062B	S5	20-Pin SOIC	Commercial[10]

Notes:
9. Please call your local Cypress representative.
10. 0°C to +70°C

Example: order ICD2062BSC-2 for the ICD2062B, 20-pin plastic SOIC, commercial temperature range device with a top Video Clock frequency range of 165 MHz.

Document #: 38-00404-A

Package Diagram

20-Lead (300-Mil) Molded SOIC S5