

Radiation Hardened 3-Line to 8-Line Decoder/Demultiplexer

February 1996

Features

- Devices QML Qualified in Accordance With MIL-PRF-38535
- Detailed Electrical and Screening Requirements are Contained in SMD# 5962-95825 and Intersil' QM Plan
- Radiation Hardened EPI-CMOS
 - Total Dose 1×10^5 RAD (Si)
 - Latch-Up Immune $> 1 \times 10^{12}$ RAD (Si)/s
- Multiple Input Enable for Easy Expansion
- Single Power Supply +5V
- Outputs Active Low
- Low Standby Power (0.5mW Max at +5V)
- High Noise Immunity
- Equivalent to Sandia SA2995
- Bus Compatible with Intersil Rad-Hard 80C85RH
- Full Military Temperature Range -55°C to +125°C

Description

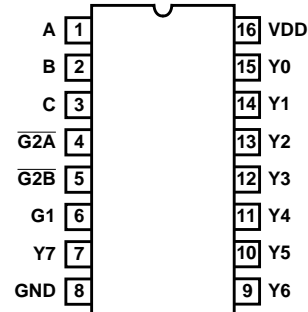
The Intersil HS-54C138RH is a radiation hardened 3- to 8-line decoder fabricated using a radiation hardened EPI-CMOS process. It features low power consumption, high noise immunity, and high speed. Also featured are pin and function compatibility with the 54LS138 industry standard part. The HS-54C138RH is ideally suited for high speed memory chip select address decoding. It is intended for use with the Intersil HS-80C85RH radiation hardened microprocessor, but it can also be utilized as a demultiplexer in any low power rad-hard application.

The HS-54C138RH contains a one of eight binary decoder. A three bit binary input is used to select and activate each of the eight outputs, provided the three chip enable inputs are also present (see truth table).

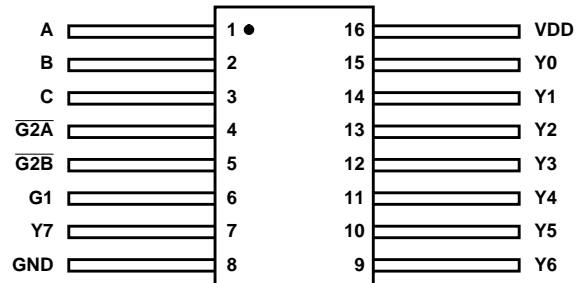
The HS-54C138RH has an on-chip enable gate. The active high (G1) and both active low ($\overline{G2A}$, $\overline{G2B}$) inputs are Anded together to provide a single enable input to the device. The use of both active high and active low inputs minimizes the need for external gates when expanding a system.

Pinouts

16 LEAD CERAMIC DUAL-IN-LINE
METAL SEAL PACKAGE (SBDIP)
MIL-STD-1835 CDIP2-T16
TOP VIEW



16 LEAD CERAMIC METAL SEAL
FLATPACK PACKAGE (FLATPACK)
MIL-STD-1835 CDFP4-F16
TOP VIEW



Ordering Information

| PART NUMBER | TEMPERATURE RANGE | SCREENING LEVEL | PACKAGE |
|---------------------|-------------------|-----------------------|--------------------------|
| 5962R9582501QEC | -55°C to +125°C | MIL-PRF-38535 Level Q | 16 Lead SBDIP |
| 5962R9582501QXC | -55°C to +125°C | MIL-PRF-38535 Level Q | 16 Lead Ceramic Flatpack |
| 5962R9582501VEC | -55°C to +125°C | MIL-PRF-38535 Level V | 16 Lead SBDIP |
| 5962R9582501VXC | -55°C to +125°C | MIL-PRF-38535 Level V | 16 Lead Ceramic Flatpack |
| HS1-54C138RH/SAMPLE | +25°C | Sample | 16 Lead SBDIP |
| HS9-54C138RH/SAMPLE | +25°C | Sample | 16 Lead Ceramic Flatpack |

Specifications HS-54C138RH

Absolute Maximum Ratings

| | |
|----------------------------------|------------------------------|
| Supply Voltage |+7.0V |
| I/O Voltage Applied | GND -0.3V to VDD +0.3V |
| Storage Temperature Range |-65°C to +150°C |
| Junction Temperature | +175°C |
| Lead Temperature (Soldering 10s) | +300°C |
| ESD Classification | Class 1 |

Reliability Information

| | | |
|--|-----------------|---------------|
| Thermal Resistance | θ_{JA} | θ_{JC} |
| SBDIP Package | 73°C/W | 24°C/W |
| Ceramic Flatpack Package | 114°C/W | 29°C/W |
| Maximum Package Power Dissipation at +125°C Ambient | | |
| SBDIP Package | 0.68W | |
| Ceramic Flatpack Package | 0.44W | |
| If device power exceeds package dissipation capability, provide heat sinking or derate linearly at the following rate: | | |
| SBDIP Package | 13.7mW/°C | |
| Ceramic Flatpack Package | 8.8mW/°C | |

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Operating Conditions

| | | | |
|-----------------------------|------------------------|--------------------|-----------------------|
| Operating Voltage Range | +4.75V to +5.25V | Input Low Voltage | 0V to 1.0V |
| Operating Temperature Range | -55°C to +125°C | Input High Voltage | VDD-1.0V to VDD |

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | GROUP A SUBGROUPS | TEMPERATURE | LIMITS | | UNITS |
|----------------------------|------------------|---|-------------------|----------------------|--------|-----|-------|
| | | | | | MIN | MAX | |
| Input Leakage Current High | I _{IH} | VDD = 5.25V, V _{IN} = 0V, Pin Under Test = VDD | 1, 2, 3 | -55°C, +25°C, +125°C | - | 1 | μA |
| Input Leakage Current Low | I _{IL} | VDD = 5.25V, V _{IN} = 5.25V, Pin Under Test = 0V | 1, 2, 3 | -55°C, +25°C | -1 | - | μA |
| High Level Output Voltage | V _{OH} | VDD = 4.75V, I _{IN} = -2mA | 1, 2, 3 | -55°C, +25°C, +125°C | 4.25 | - | V |
| Low Level Output Voltage | V _{OL} | VDD = 5.25V, I _{IN} = 2mA | 1, 2, 3 | -55°C, +25°C, +125°C | 0.5 | - | V |
| Static Current | S _{IDD} | VDD = 5.25V, V _{IN} = GND | 1, 2, 3 | -55°C, +25°C, +125°C | - | 100 | μA |
| Functional Tests | FT | VDD = 5.25V and 4.75V, V _{IH} = VDD - 1.0V, V _{IL} = 1.0V | 7, 8A, 8B | -55°C, +25°C, +125°C | - | - | - |

NOTE: All devices are guaranteed at worst case limits and conditions.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | GROUP A SUB-GROUPS | TEMPERATURE | LIMITS | | UNITS |
|---|--------------------|--------------------|----------------------|--------|-----|-------|
| | | | | MIN | MAX | |
| SELECT TO OUTPUT PROPAGATION DELAY TIME | | | | | | |
| Low to high level input, High to low level output | T _{PHL11} | 9, 10, 11 | -55°C, +25°C, +125°C | - | 110 | ns |
| Low to high level input, Low to high level output | T _{PLH11} | 9, 10, 11 | -55°C, +25°C, +125°C | - | 65 | ns |
| High to low level input, Low to high level output | T _{PLH12} | 9, 10, 11 | -55°C, +25°C, +125°C | - | 75 | ns |
| High to low level input, high to low level output | T _{PHL12} | 9, 10, 11 | -55°C, +25°C, +125°C | - | 90 | ns |
| ENABLE TO OUTPUT PROPAGATION DELAY TIME | | | | | | |
| Low to high level input, Low to high level output | T _{PLH21} | 9, 10, 11 | -55°C, +25°C, +125°C | - | 70 | ns |

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TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

| PARAMETER | SYMBOL | GROUP A SUB-GROUPS | TEMPERATURE | LIMITS | | UNITS |
|---|--------|--------------------|----------------------|--------|-----|-------|
| | | | | MIN | MAX | |
| Low to high level input, High to low level output | TPHL21 | 9, 10, 11 | -55°C, +25°C, +125°C | - | 105 | ns |
| High to low level input, Low to high level output | TPLH22 | 9, 10, 11 | -55°C, +25°C, +125°C | - | 70 | ns |
| High to low level input, High to low level output | TPHL22 | 9, 10, 11 | -55°C, +25°C, +125°C | - | 105 | ns |

NOTE: Output timings are measured with a capacitive load, CL = 100pF, VIH = 3.75V, and VIL = 1.0V.

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS

| PARAMETER | SYMBOL | CONDITIONS | TEMPERATURE | LIMITS | | UNITS |
|--------------------|--------|--|-------------|--------|-----|-------|
| | | | | MIN | MAX | |
| Input Capacitance | CIN | VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground | +25°C | - | 10 | pF |
| Output Capacitance | COUT | VDD = Open, f = 1MHz, All Measurements Referenced to Device Ground | +25°C | - | 10 | pF |

NOTE: The parameters listed in Table 3 are controlled via design or process parameters and are not directly tested. These parameters are characterized upon initial design release and upon design changes which would affect these characteristics.

TABLE 4. POST 100K RAD ELECTRICAL PERFORMANCE CHARACTERISTICS

NOTE: The Post Irradiation test conditions and limits are the same as those listed in Table 1 and Table 2.

TABLE 5. BURN-IN DELTA PARAMETERS (+25°C; In Accordance With SMD)

HS-54C138RH

Metallization Topology

DIE DIMENSIONS:

76 mils x 63 mils x 14 mils ± 1 mil

METALLIZATION:

Type: AlSi

Thickness: $11\text{k}\text{\AA} \pm 2\text{k}\text{\AA}$

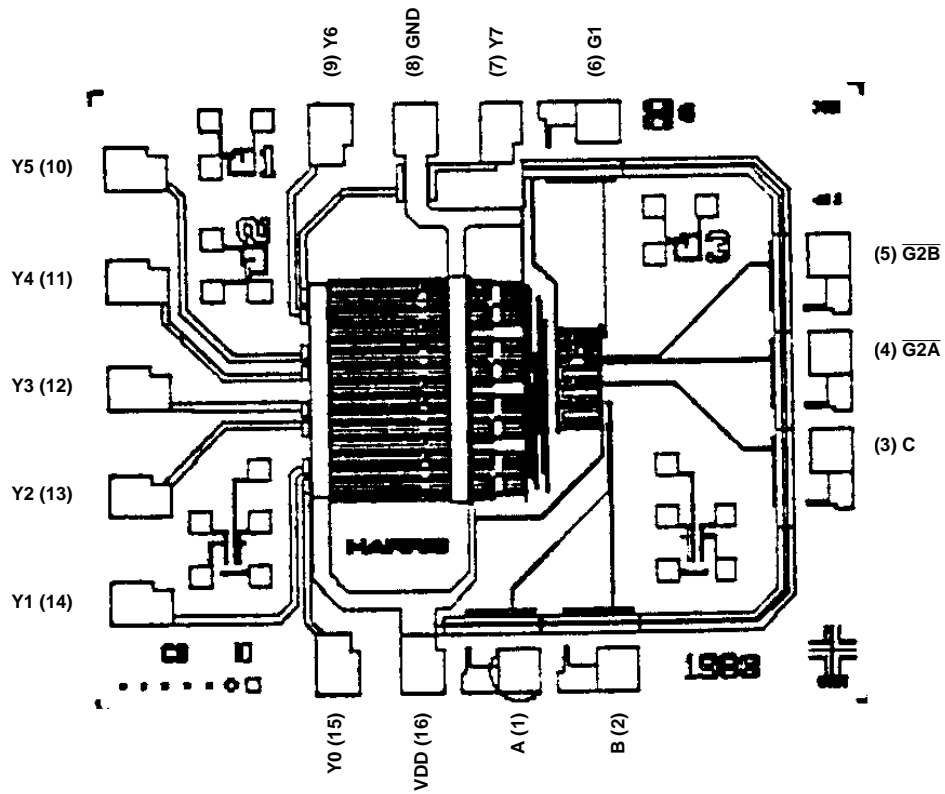
GLASSIVATION:

Type: SiO₂

Thickness: $8\text{k}\text{\AA} \pm 1\text{k}\text{\AA}$

Metallization Mask Layout

HS-54C138RH



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Typical applications include systems which require multiple input/output ports and memories. When the HS-54C138RH is enabled one of the eight outputs will go low. This output can be used to select a particular device or a group of devices. The HS-54C138RH can also be cascaded to provide an enabling scheme for larger systems and allow one decoder to control eight other decoders as in Figure 1.

Figure 2 shows a configuration that can be used to enable multiple I/O ports or memory devices. Up to 24 memory devices or I/O ports can be controlled using this circuit.

For demultiplexer operation, one of the three enable inputs is used as the data input while the other two inputs are enable. The transmitted data is distributed to the proper output as determined by the 3-line select inputs. See Figure 3.

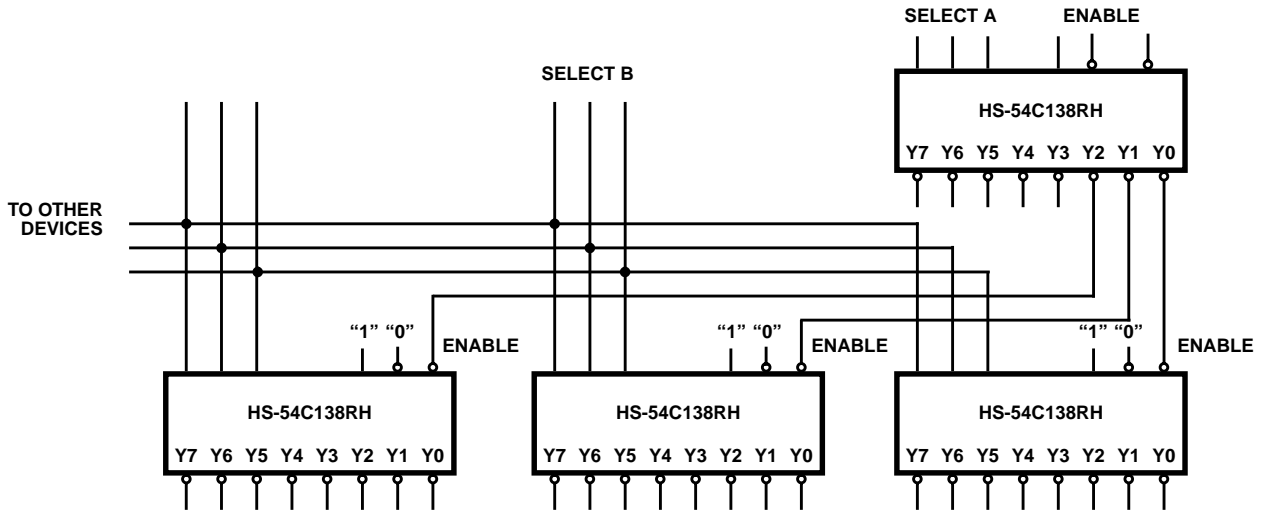


FIGURE 1

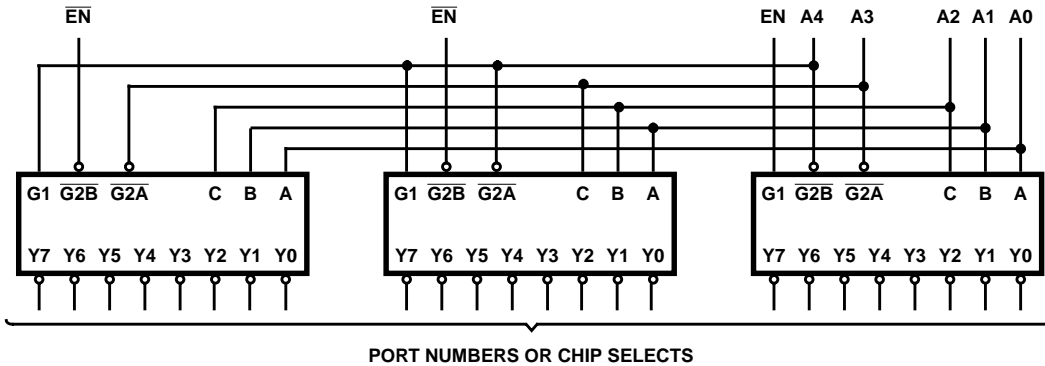


FIGURE 2

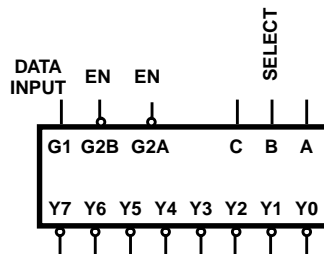


FIGURE 3

All Intersil semiconductor products are manufactured, assembled and tested under **ISO9000** quality systems certification.

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