

Data Sheet June 1999 File Number 2169.3

# 14A, 275V, 0.280 Ohm, N-Channel Power MOSFET

This N-Channel enhancement mode silicon gate power field effect transistor is an advanced power MOSFET designed, tested, and guaranteed to withstand a specified level of energy in the breakdown avalanche mode of operation. All of these power MOSFETs are designed for applications such as switching regulators, switching convertors, motor drivers, relay drivers, and drivers for high power bipolar switching transistors requiring high speed and low gate drive power. These types can be operated directly from integrated circuits.

Formerly developmental type TA17423.

### **Ordering Information**

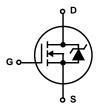
PART NUMBER	PACKAGE	BRAND		
IRF646	TO-220AB	IRF646		

NOTE: When ordering, use the entire part number.

### **Features**

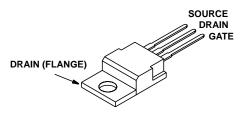
- 14A, 275V
- $r_{DS(ON)} = 0.280\Omega$
- Single Pulse Avalanche Energy Rated
- · SOA is Power Dissipation Limited
- · Nanosecond Switching Speeds
- · Linear Transfer Characteristics
- High Input Impedance
- 275VDC Rating-120VAC Line System Operation
- · Related Literature
  - TB334 "Guidelines for Soldering Surface Mount Components to PC Boards"

### Symbol



### **Packaging**

### **JEDEC TO-220AB**



# **Absolute Maximum Ratings** $T_C = 25^{\circ}C$ , Unless Otherwise Specified

	IRF646	UNITS
Drain to Source Voltage (Note 1)V <sub>DS</sub>	275	V
Drain to Gate Voltage (R <sub>GS</sub> = 20kΩ) (Note 1)	275	V
Continuous Drain Current	14	Α
$T_C = 100^{\circ}C$	8.8	Α
Pulsed Drain Current (Note 3)	56	Α
Gate to Source Voltage	±20	V
Maximum Power Dissipation	125	W
Linear Derating Factor	1.0	W/oC
Single Pulse Avalanche Energy Rating (Note 4)	550	mJ
Operating and Storage Temperature	-55 to 150	°C
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s	300	°C
Package Body for 10s, See TB334	260	°C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

#### NOTE:

1.  $T_J = 25^{\circ}C$  to  $125^{\circ}C$ 

# $\textbf{Electrical Specifications} \hspace{0.5cm} \textbf{T}_{C} = 25^{o}\text{C, Unless Otherwise Specified}$

PARAMETER	SYMBOL	TEST CONI	DITIONS	MIN	TYP	MAX	UNITS
Drain to Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V (Figure 10)		275	-	-	V
Gate Threshold Voltage	V <sub>GS(TH)</sub>	$V_{GS} = V_{DS}, I_{D} = 250 \mu A$		2	-	4	V
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = Rated BV <sub>DSS</sub> , V <sub>GS</sub> = 0V		-	-	25	μА
		V <sub>DS</sub> = 0.8 x Rated BV <sub>DSS</sub> ,	$V_{GS} = 0V, T_J = 125^{\circ}C$	-	-	250	μΑ
On-State Drain Current (Note 2)	I <sub>D(ON)</sub>	$V_{DS} > I_{D(ON)} \times r_{DS(ON)MAX}, V_{GS} = 10V \text{ (Figure 7)}$		14	-	-	Α
Gate to Source Leakage Current	I <sub>GSS</sub>	$V_{GS} = \pm 20V$		-	-	±100	nA
Drain to Source On Resistance (Note 2)	r <sub>DS(ON)</sub>	$I_D = 8A$ , $V_{GS} = 10V$ (Figure	s 8, 9)	-	0.200	0.280	Ω
Forward Transconductance (Note 2)	9 <sub>fs</sub>	V <sub>DS</sub> ≥ 50V, I <sub>D</sub> = 8A (Figure 12)		6.7	10	-	S
Turn-On Delay Time	t <sub>d</sub> (ON)	$V_{DD}$ = 125V, $I_D$ ≈ 14A, $R_{GS}$ = 9.1Ω, $R_L$ = 8.6Ω, MOSFET Switching Times are Essentially Independent of Operating Temperature		-	16	24	ns
Rise Time	t <sub>r</sub>			-	67	100	ns
Turn-Off Delay Time	t <sub>d</sub> (OFF)	independent of Operating 1	emperature	-	53	80	ns
Fall Time	t <sub>f</sub>	-		-	49	74	ns
Total Gate Charge (Gate to Source + Gate to Drain)	Q <sub>g(TOT)</sub>	$V_{GS}$ = 10V, $I_D$ = 14A, $V_{DS}$ = 0.8 x Rated BV <sub>DSS</sub> , $I_{G(REF)}$ = 1.5mA, (Figure 14) Gate Charge is Essentially Independent of Operating Temperature		-	39	59	nC
Gate to Source Charge	Q <sub>gs</sub>			-	6.6	-	nC
Gate to Drain "Miller" Charge	Q <sub>gd</sub>			-	20	-	nC
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz (Figure 11)		-	1300	-	pF
Output Capacitance	C <sub>OSS</sub>			-	320	-	pF
Reverse Transfer Capacitance	C <sub>RSS</sub>			-	69	-	pF
Internal Drain Inductance	L <sub>D</sub>	Measured from the Contact Screw on Tab to Center of Die	Modified MOSFET Symbol Showing the Internal Devices	-	4.5	-	nH
		Measured from the Drain Lead, 6mm (0.25in) from Package to Center of Die	Inductances	-	7.5	-	nH
Internal Source Inductance	L <sub>S</sub>	Measured from the Source Lead, 6mm (0.25in) from Header to Source Bonding Pad	G G ELS	-	7.5	-	nH
Thermal Resistance Junction to Case	$R_{ heta JC}$		,	-	-	1	oC/W
Thermal Resistance Junction to Ambient	$R_{\theta JA}$	Free Air Operation		-	-	80	oC/W

### **Source to Drain Diode Specifications**

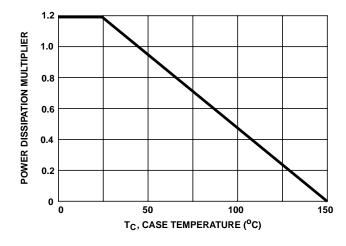
PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Continuous Source to Drain Current	I <sub>SD</sub>	Modified MOSFET Symbol	-	-	14	Α
Pulse Source to Drain Current (Note 3)	<sup>I</sup> SDM	Showing the Integral Reverse P-N Junction Diode	-	-	56	А
Source to Drain Diode Voltage (Note 2)	V <sub>SD</sub>	$T_J = 25^{\circ}C$ , $I_{SD} = 14A$ , $V_{GS} = 0V$ (Figure 13)	-	-	1.8	V
Reverse Recovery Time	t <sub>rr</sub>	$T_J = 25^{\circ}C$ , $I_{SD} = 14A$ , $dI_{SD}/dt = 100A/\mu s$		300	640	ns
Reverse Recovery Charge	Q <sub>RR</sub>	$T_J = 25^{\circ}C$ , $I_{SD} = 14A$ , $dI_{SD}/dt = 100A/\mu s$		3.4	7.2	μC

15

### NOTES:

- 2. Pulse Test: Pulse width  $\leq 300 \mu s, \, \text{Duty Cycle} \leq 2\%.$
- 3. Repetitive rating: Pulse width limited by maximum junction temperature. See Transient Thermal Impedance curve (Figure 3).
- 4.  $V_{DD}$  = 50V, starting  $T_J$  = 25°C, L = 4.5mH,  $R_G$  = 25 $\Omega$ , peak  $I_{AS}$  = 14A.

# Typical Performance Curves Unless Otherwise Specified



12 9 9 0 25 50 75 100 125 150 T<sub>C</sub>, CASE TEMPERATURE (°C)

FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

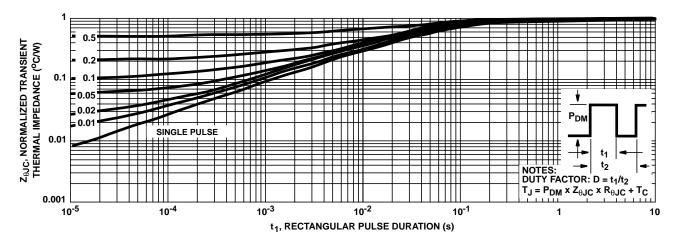


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

# Typical Performance Curves Unless Otherwise Specified (Continued)

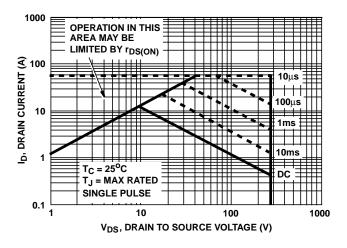


FIGURE 4. FORWARD BIAS SAFE OPERATING AREA

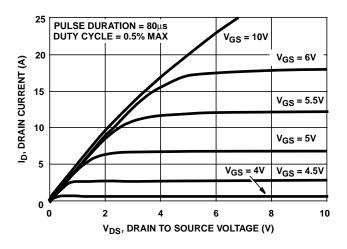


FIGURE 6. SATURATION CHARACTERISTICS

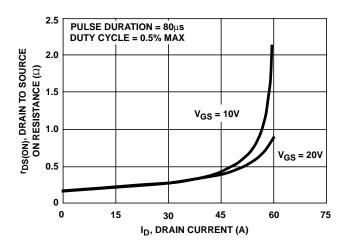


FIGURE 8. DRAIN TO SOURCE ON RESISTANCE vs GATE VOLTAGE AND DRAIN CURRENT

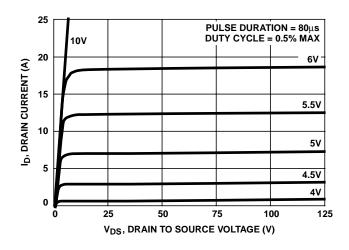


FIGURE 5. OUTPUT CHARACTERISTICS

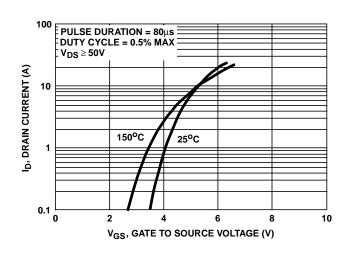


FIGURE 7. TRANSFER CHARACTERISTICS

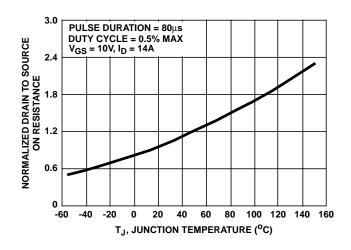


FIGURE 9. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs JUNCTION TEMPERATURE

### Typical Performance Curves Unless Otherwise Specified (Continued)

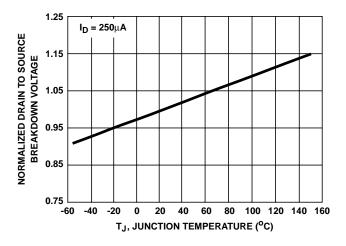


FIGURE 10. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

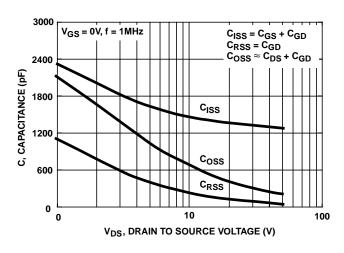


FIGURE 11. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE

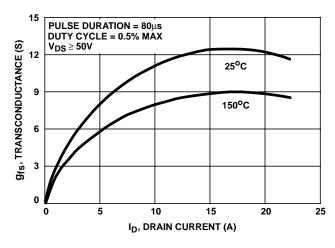


FIGURE 12. TRANSCONDUCTANCE vs DRAIN CURRENT

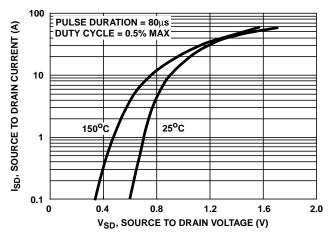


FIGURE 13. SOURCE TO DRAIN DIODE FORWARD VOLTAGE

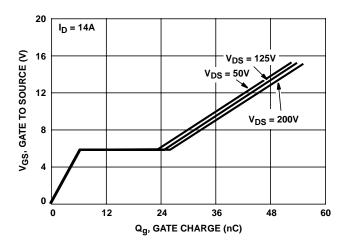


FIGURE 14. GATE TO SOURCE VOLTAGE vs GATE CHARGE

### Test Circuits and Waveforms

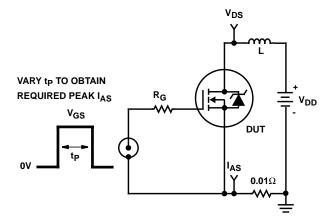


FIGURE 15. UNCLAMPED ENERGY TEST CIRCUIT

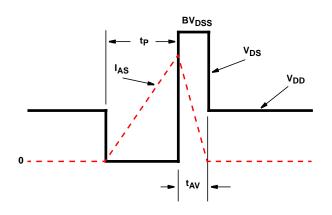


FIGURE 16. UNCLAMPED ENERGY WAVEFORMS

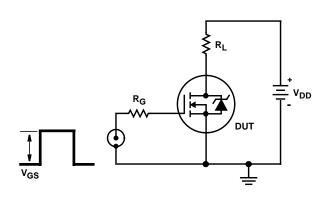


FIGURE 17. SWITCHING TIME TEST CIRCUIT

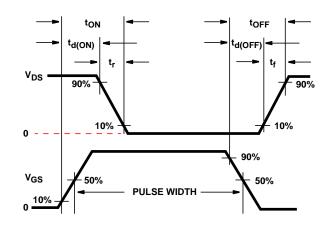


FIGURE 18. RESISTIVE SWITCHING WAVEFORMS

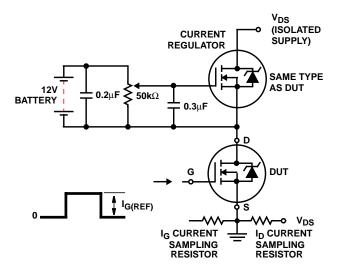


FIGURE 19. GATE CHARGE TEST CIRCUIT

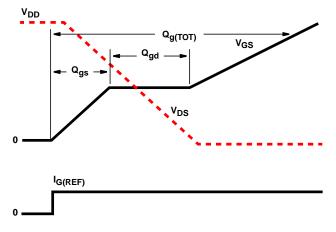


FIGURE 20. GATE CHARGE WAVEFORMS

All Intersil semiconductor products are manufactured, assembled and tested under ISO9000 quality systems certification.

Intersil semiconductor products are sold by description only. Intersil Corporation reserves the right to make changes in circuit design and/or specifications at any time without notice. Accordingly, the reader is cautioned to verify that data sheets are current before placing orders. Information furnished by Intersil is believed to be accurate and reliable. However, no responsibility is assumed by Intersil or its subsidiaries for its use; nor for any infringements of patents or other rights of third parties which may result from its use. No license is granted by implication or otherwise under any patent or patent rights of Intersil or its subsidiaries.

For information regarding Intersil Corporation and its products, see web site http://www.intersil.com

### Sales Office Headquarters

**NORTH AMERICA** 

Intersil Corporation P. O. Box 883, Mail Stop 53-204 Melbourne, FL 32902 TEL: (407) 724-7000

TEL: (407) 724-7000 FAX: (407) 724-7240 **EUROPE** 

Intersil SA Mercure Center 100, Rue de la Fusee 1130 Brussels, Belgium TEL: (32) 2.724.2111 FAX: (32) 2.724.22.05 **ASIA** 

Intersil (Taiwan) Ltd.
7F-6, No. 101 Fu Hsing North Road
Taipei, Taiwan
Republic of China
TEL: (886) 2 2716 9310
FAX: (886) 2 2715 3029