Errata (All Date Codes): Missed Watchdog Timer Reset

Problem

There is a synchronization problem between the watchdog clock and the AVR[®] clock. Even though the clock inputs to both the watchdog timer and the AVR core are generated through the same crystal, the two clock sources are not going through the same PLL. The AVR is clocked at 12 MHz and the watchdog timer is clocked at 1MHz. The WDR (Watchdog Reset) instruction is a one-clock-cycle instruction. As such, when a watchdog timer reset occurs due to a WDR, the watchdog timer may miss the reset. This happens frequently if the AVR is clocked much faster than the watchdog timer.

Fix/Workaround

A workaround is to invoke the WDR repetitively to ensure that the watchdog timer will be able to receive the reset signal. If the AVR runs at 12 MHz, the WDR command must be invoked fourteen times back to back.

The following is the sample code for resetting and arming the watchdog timer, assuming the AVR is running at 12 MHz:

asm ("ldi r16,15\n WDR\n 0x21,r16 ");

To disarm and disable the watchdog, do the following:

asm ("ldi r16,0x18\nldi r17,0x10\n\n out 0x21,r16\n out 0x21,r17 ");

Please note that if the AVR runs at 24 MHz, the WDR should be invoked twenty-six times.



USB Microcontrollers

AT43USB320A AT43USB325 AT43USB326 AT43USB351M AT43USB353M AT43USB355

Errata Sheet

3469A-USB-4/04





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