
HM62V8512B Series

4 M SRAM (512-kword × 8-bit)

HITACHI

ADE-203-905G (Z)
Rev. 6.0
Mar. 31, 2000

Description

The Hitachi HM62V8512B is a 4-Mbit static RAM organized 512-kword × 8-bit. It realizes higher density, higher performance and low power consumption by employing 0.35 μm Hi-CMOS process technology. The device, packaged in a 525-mil SOP (foot print pitch width) or 400-mil TSOP TYPE II is available for high density mounting. The HM62V8512B is suitable for battery backup system.

Features

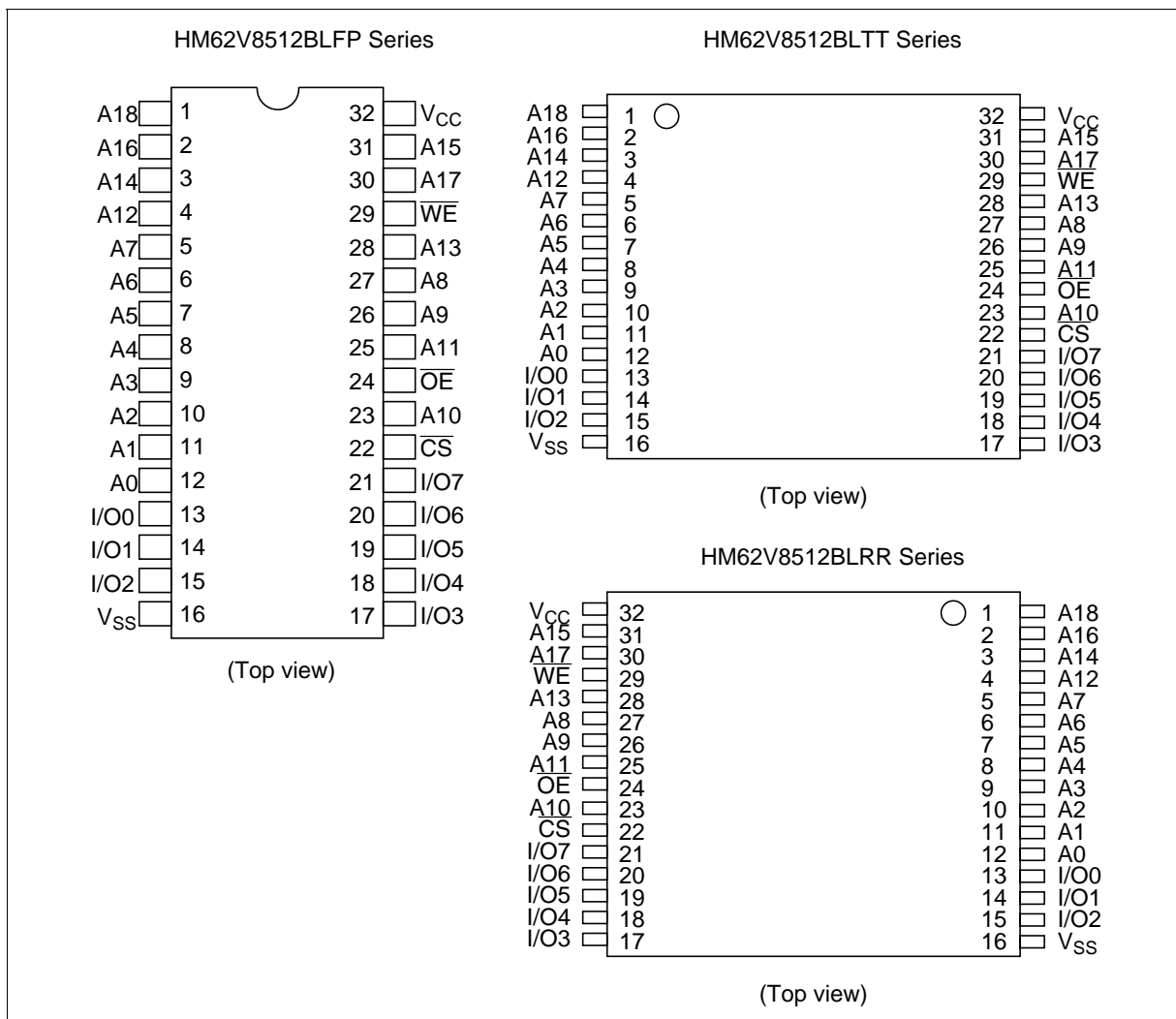
- Single 3.0 V supply: 2.7 V to 3.6 V
- Access time: 70/85 ns (max)
- Power dissipation
 - Active: 15 mW/MHz (typ)
 - Standby: 3 μW (typ)
- Completely static memory. No clock or timing strobe required
- Equal access and cycle times
- Common data input and output: Three state output
- Directly LV-TTL compatible: All inputs
- Battery backup operation

HM62V8512B Series

Ordering Information

Type No.	Access time	Package
HM62V8512BLFP-7	70 ns	525-mil 32-pin plastic SOP (FP-32D)
HM62V8512BLFP-8	85 ns	
HM62V8512BLFP-7SL	70 ns	
HM62V8512BLFP-8SL	85 ns	
HM62V8512BLFP-7UL	70 ns	
HM62V8512BLFP-8UL	85 ns	
HM62V8512BLTT-7	70 ns	400-mil 32-pin plastic TSOP II (TTP-32D)
HM62V8512BLTT-8	85 ns	
HM62V8512BLTT-7SL	70 ns	
HM62V8512BLTT-8SL	85 ns	
HM62V8512BLTT-7UL	70 ns	
HM62V8512BLTT-8UL	85 ns	
HM62V8512BLRR-7	70 ns	400-mil 32-pin plastic TSOP II reverse (TTP-32DR)
HM62V8512BLRR-8	85 ns	
HM62V8512BLRR-7SL	70 ns	
HM62V8512BLRR-8SL	85 ns	
HM62V8512BLRR-7UL	70 ns	
HM62V8512BLRR-8UL	85 ns	

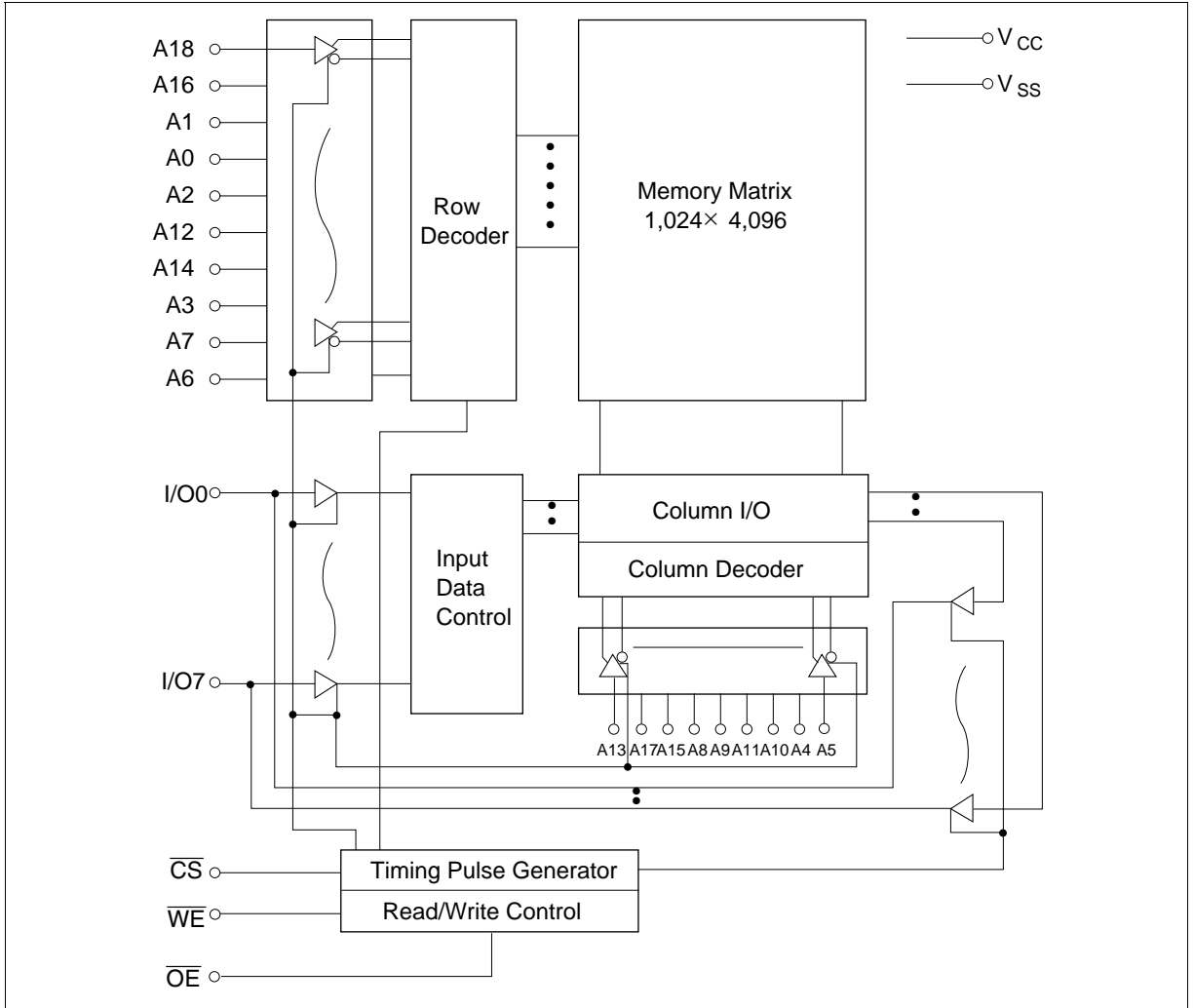
Pin Arrangement



Pin Description

Pin name	Function
A0 to A18	Address input
I/O0 to I/O7	Data input/output
\overline{CS}	Chip select
\overline{OE}	Output enable
\overline{WE}	Write enable
V _{CC}	Power supply
V _{SS}	Ground

Block Diagram



Function Table

\overline{WE}	\overline{CS}	\overline{OE}	Mode	V_{CC} current	Dout pin	Ref. cycle
x	H	x	Not selected	I_{SB}, I_{SB1}	High-Z	—
H	L	H	Output disable	I_{CC}	High-Z	—
H	L	L	Read	I_{CC}	Dout	Read cycle
L	L	H	Write	I_{CC}	Din	Write cycle (1)
L	L	L	Write	I_{CC}	Din	Write cycle (2)

Note: x: H or L

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Power supply voltage	V_{CC}	-0.5 to +4.6	V
Voltage on any pin relative to V_{SS}	V_T	-0.5* ¹ to $V_{CC} + 0.5$ * ²	V
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	-20 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C
Storage temperature under bias	T_{bias}	-20 to +85	°C

Notes: 1. -3.0 V for pulse half-width \leq 30 ns

2. Maximum voltage is 4.6 V

Recommended DC Operating Conditions ($T_a = -20$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit
Supply voltage	V_{CC}	2.7	3.0	3.6	V
	V_{SS}	0	0	0	V
Input high voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V
Input low voltage	V_{IL}	-0.3* ¹	—	0.8	V

Note: 1. -3.0 V for pulse half-width \leq 30 ns

DC Characteristics (Ta = -20 to +70°C, V_{CC} = 2.7 V to 3.6 V, V_{SS} = 0 V)

Parameter	Symbol	Min	Typ* ¹	Max	Unit	Test conditions	
Input leakage current	I _{Ij}	—	—	1	μA	V _{in} = V _{SS} to V _{CC}	
Output leakage current	I _{Lo}	—	—	1	μA	$\overline{CS} = V_{IH}$ or $\overline{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, V _{I/O} = V _{SS} to V _{CC}	
Operating power supply current: DC	I _{CC}	—	—	10	mA	$\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} , I _{I/O} = 0 mA	
Operating power supply current	I _{CC1}	—	—	40	mA	Min cycle, duty = 100% $\overline{CS} = V_{IL}$, others = V _{IH} /V _{IL} I _{I/O} = 0 mA	
Operating power supply current	I _{CC2}	—	5	10	mA	Cycle time = 1 μs, duty = 100% I _{I/O} = 0 mA, $\overline{CS} \leq 0.2$ V V _{IH} ≥ V _{CC} - 0.2 V, V _{IL} ≤ 0.2 V	
Standby power supply current: DC	I _{SB}	—	0.1	0.3	mA	$\overline{CS} = V_{IH}$	
Standby power supply current (1): DC	I _{SB1}	—	1* ²	40* ²	μA	V _{in} ≥ 0 V, $\overline{CS} \geq V_{CC} - 0.2$ V	
			—	1* ³	20* ³		μA
			—	1* ⁴	5* ⁴		μA
Output low voltage	V _{OL}	—	—	0.4	V	I _{OL} = 2.1 mA	
				0.2	V	I _{OL} = 100 μA	
Output high voltage	V _{OH}	V _{CC} - 0.2	—	—	V	I _{OH} = -100 μA	
						2.4	—

Notes: 1. Typical values are at V_{CC} = 3.0 V, Ta = +25°C and specified loading, and not guaranteed.

2. This characteristics is guaranteed only for L version.

3. This characteristics is guaranteed only for L-SL version.

4. This characteristics is guaranteed only for L-UL version.

Capacitance (Ta = +25°C, f = 1 MHz)

Parameter	Symbol	Typ	Max	Unit	Test conditions
Input capacitance* ¹	C _{in}	—	8	pF	V _{in} = 0 V
Input/output capacitance* ¹	C _{I/O}	—	10	pF	V _{I/O} = 0 V

Note: 1. This parameter is sampled and not 100% tested.

AC Characteristics ($T_a = -20$ to $+70^\circ\text{C}$, $V_{CC} = 2.7$ V to 3.6 V, unless otherwise noted.)

Test Conditions

- Input pulse levels: 0.4 V to 2.4 V
- Input rise and fall time: 5 ns
- Input timing reference levels: 1.4 V
- Output timing reference level: 1.5 V/1.5 V(HM62V8512B-7)
0.8 V/2.0 V(HM62V8512B-8)

Output load: 1 TTL Gate + C_L (50 pF)
(Including scope & jig)

Read Cycle

Parameter	Symbol	HM62V8512B				Unit	Notes
		-7		-8			
		Min	Max	Min	Max		
Read cycle time	t_{RC}	70	—	85	—	ns	
Address access time	t_{AA}	—	70	—	85	ns	
Chip select access time	t_{CO}	—	70	—	85	ns	
Output enable to output valid	t_{OE}	—	35	—	45	ns	
Chip selection to output in low-Z	t_{LZ}	10	—	10	—	ns	2
Output enable to output in low-Z	t_{OLZ}	5	—	5	—	ns	2
Chip deselection to output in high-Z	t_{HZ}	0	30	0	35	ns	1, 2
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	ns	1, 2
Output hold from address change	t_{OH}	10	—	10	—	ns	

Write Cycle

Parameter	Symbol	HM62V8512B				Unit	Notes
		-7		-8			
		Min	Max	Min	Max		
Write cycle time	t_{WC}	70	—	85	—	ns	
Chip selection to end of write	t_{CW}	60	—	75	—	ns	4
Address setup time	t_{AS}	0	—	0	—	ns	5
Address valid to end of write	t_{AW}	60	—	75	—	ns	
Write pulse width	t_{WP}	50	—	55	—	ns	3, 12
Write recovery time	t_{WR}	0	—	0	—	ns	6
\overline{WE} to output in high-Z	t_{WHZ}	0	30	0	35	ns	1, 2, 7
Data to write time overlap	t_{DW}	30	—	35	—	ns	
Data hold from write time	t_{DH}	0	—	0	—	ns	
Output active from output in high-Z	t_{OW}	5	—	5	—	ns	2
Output disable to output in high-Z	t_{OHZ}	0	30	0	35	ns	1, 2, 7

Notes: 1. t_{HZ} , t_{OHZ} and t_{WHZ} are defined as the time at which the outputs achieve the open circuit conditions and are not referred to output voltage levels.

2. This parameter is sampled and not 100% tested.

3. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} . A write begins at the later transition of \overline{CS} going low or \overline{WE} going low. A write ends at the earlier transition of \overline{CS} going high or \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.

4. t_{CW} is measured from \overline{CS} going low to the end of write.

5. t_{AS} is measured from the address valid to the beginning of write.

6. t_{WR} is measured from the earlier of \overline{WE} or \overline{CS} going high to the end of write cycle.

7. During this period, I/O pins are in the output state so that the input signals of the opposite phase to the outputs must not be applied.

8. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, the output remain in a high impedance state.

9. Dout is the same phase of the write data of this write cycle.

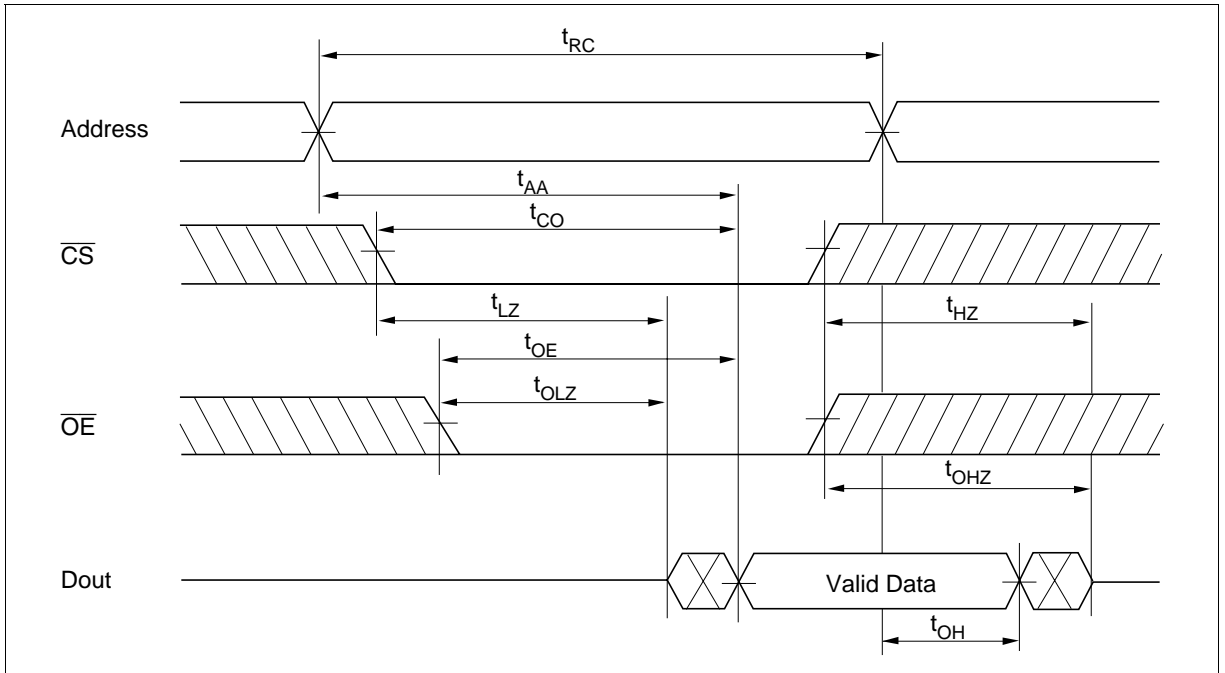
10. Dout is the read data of next address.

11. If \overline{CS} is low during this period, I/O pins are in the output state. Therefore, the input signals of the opposite phase to the outputs must not be applied to them.

12. In the write cycle with \overline{OE} low fixed, t_{WP} must satisfy the following equation to avoid a problem of data bus contention. $t_{WP} \geq t_{DW} \text{ min} + t_{WHZ} \text{ max}$

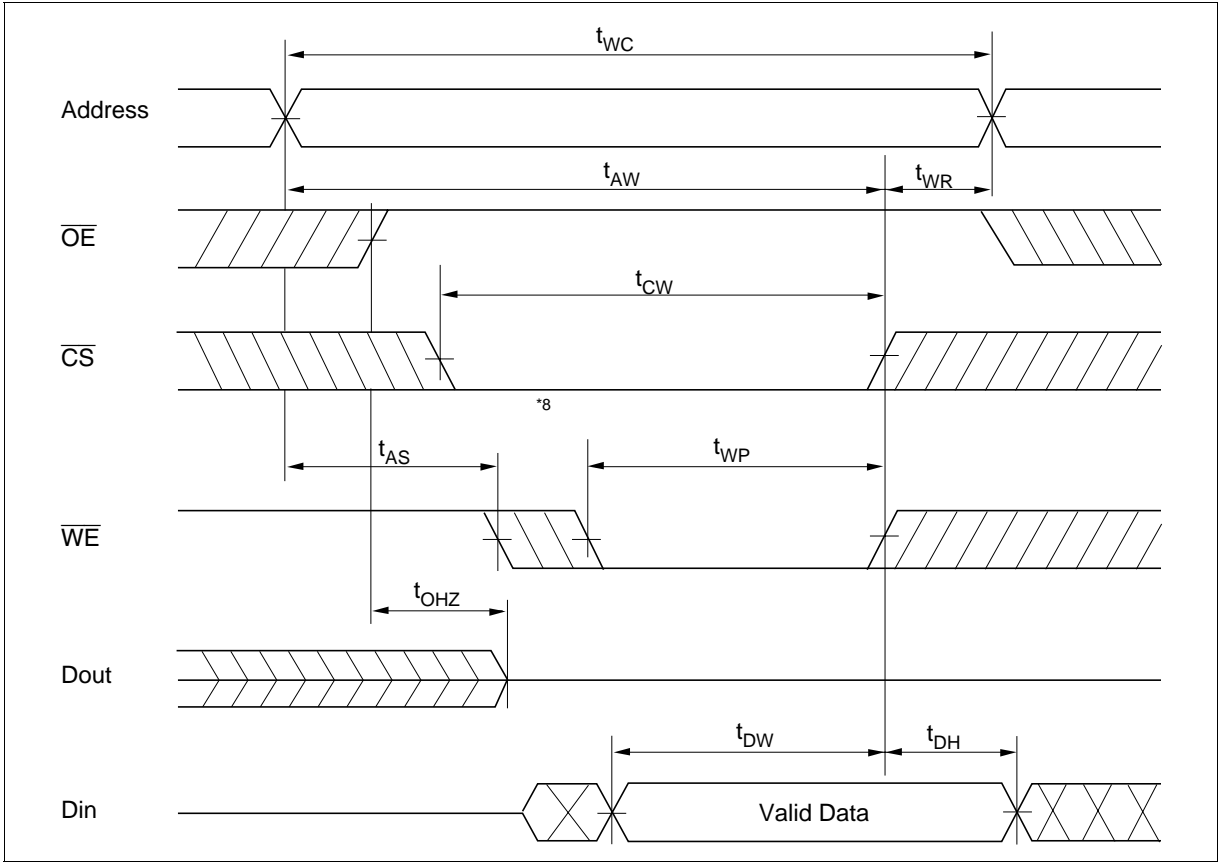
Timing Waveforms

Read Timing Waveform ($\overline{WE} = V_{IH}$)

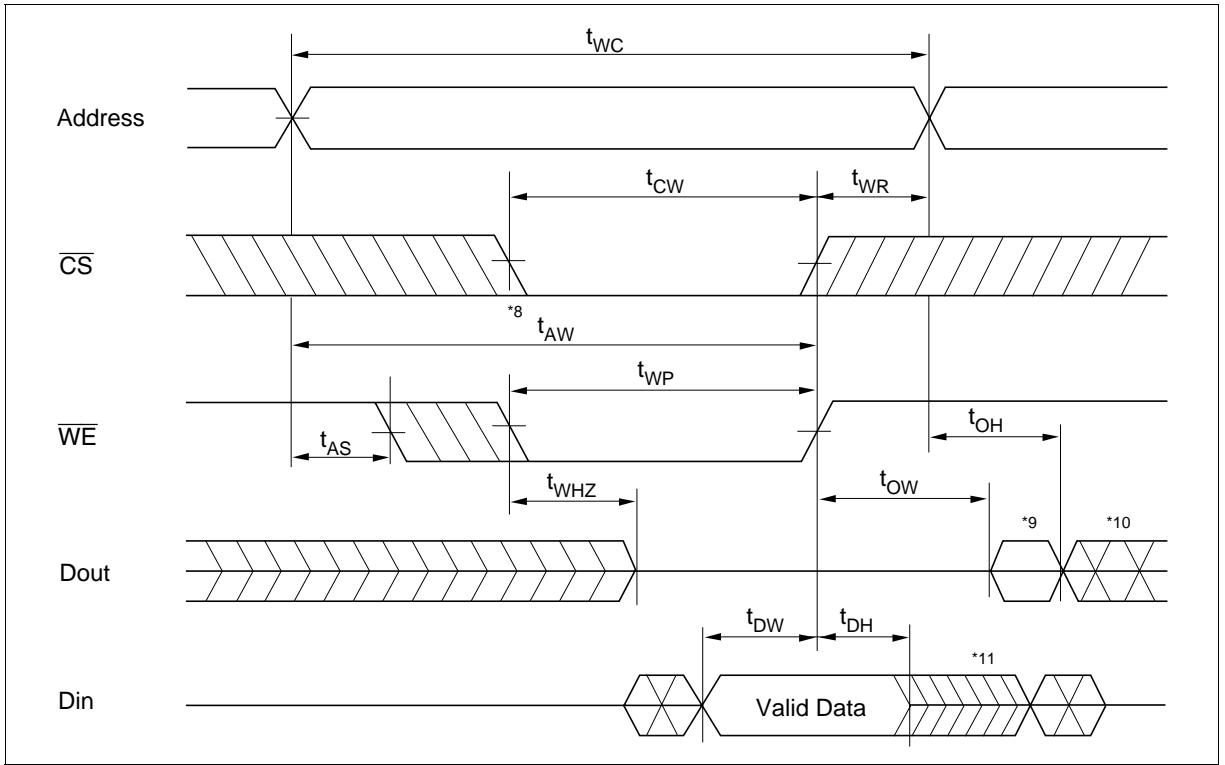


HM62V8512B Series

Write Timing Waveform (1) ($\overline{\text{OE}}$ Clock)



Write Timing Waveform (2) (\overline{OE} Low Fixed)



Low V_{CC} Data Retention Characteristics ($T_a = -20$ to $+70^\circ\text{C}$)

Parameter	Symbol	Min	Typ	Max	Unit	Test conditions**4
V_{CC} for data retention	V_{DR}	2	—	—	V	$\overline{CS} \geq V_{CC} - 0.2 \text{ V}$, $V_{in} \geq 0 \text{ V}$
Data retention current	I_{CCDR}	—	0.8^{*5}	20^{*1}	μA	$V_{CC} = 3.0 \text{ V}$, $V_{in} \geq 0 \text{ V}$ $\overline{CS} \geq V_{CC} - 0.2 \text{ V}$
		—	0.8^{*5}	10^{*2}	μA	
		—	0.8^{*5}	2^{*3}	μA	
Chip deselect to data retention time	t_{CDR}	0	—	—	ns	See retention waveform
Operation recovery time	t_R	t_{RC}^{*6}	—	—	ns	

Notes: 1. For L-version and $10 \mu\text{A}$ (max.) at $T_a = -20$ to $+40^\circ\text{C}$.

2. For L-SL-version and $3 \mu\text{A}$ (max.) at $T_a = -20$ to $+40^\circ\text{C}$.

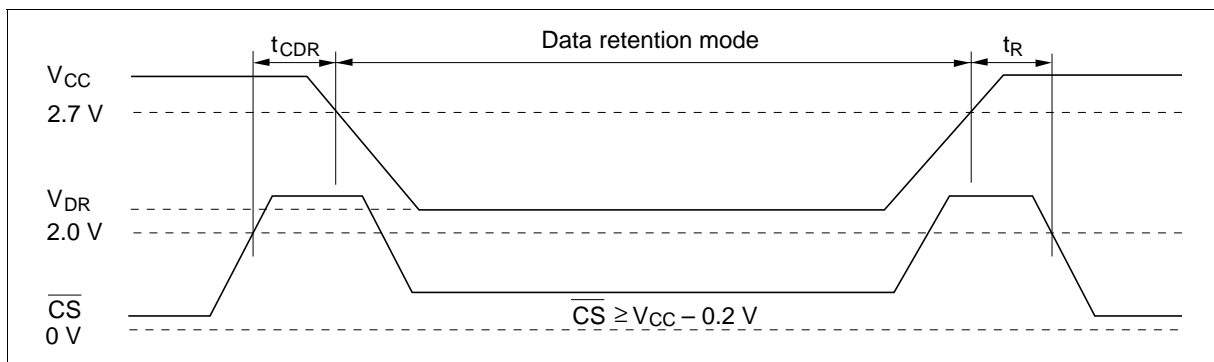
3. For L-UL-version and $2 \mu\text{A}$ (max.) at $T_a = -20$ to $+40^\circ\text{C}$.

4. \overline{CS} controls address buffer, \overline{WE} buffer, \overline{OE} buffer, and D_{in} buffer. In data retention mode, V_{in} levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

5. Typical values are at $V_{CC} = 3.0 \text{ V}$, $T_a = +25^\circ\text{C}$ and specified loading, and not guaranteed.

6. t_{RC} = read cycle time.

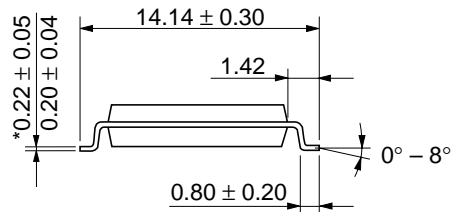
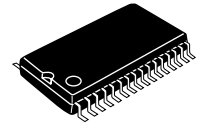
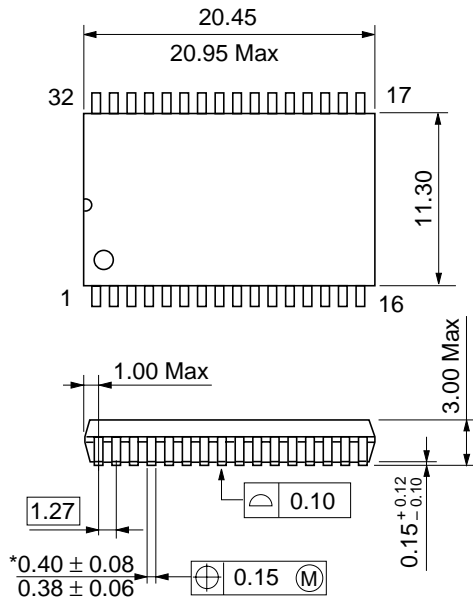
Low V_{CC} Data Retention Timing Waveform (\overline{CS} Controlled)



Package Dimensions

HM62V8512BLFP Series (FP-32D)

Unit: mm



*Dimension including the plating thickness
Base material dimension

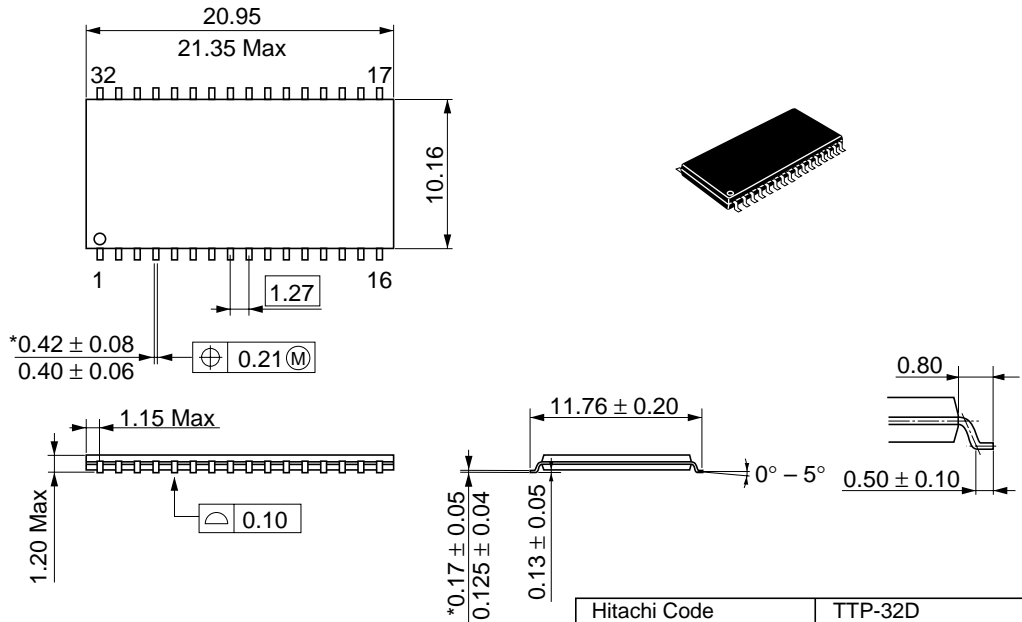
Hitachi Code	FP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	1.3 g

HM62V8512B Series

Package Dimensions (cont.)

HM62V8512BLTT Series (TTP-32D)

Unit: mm



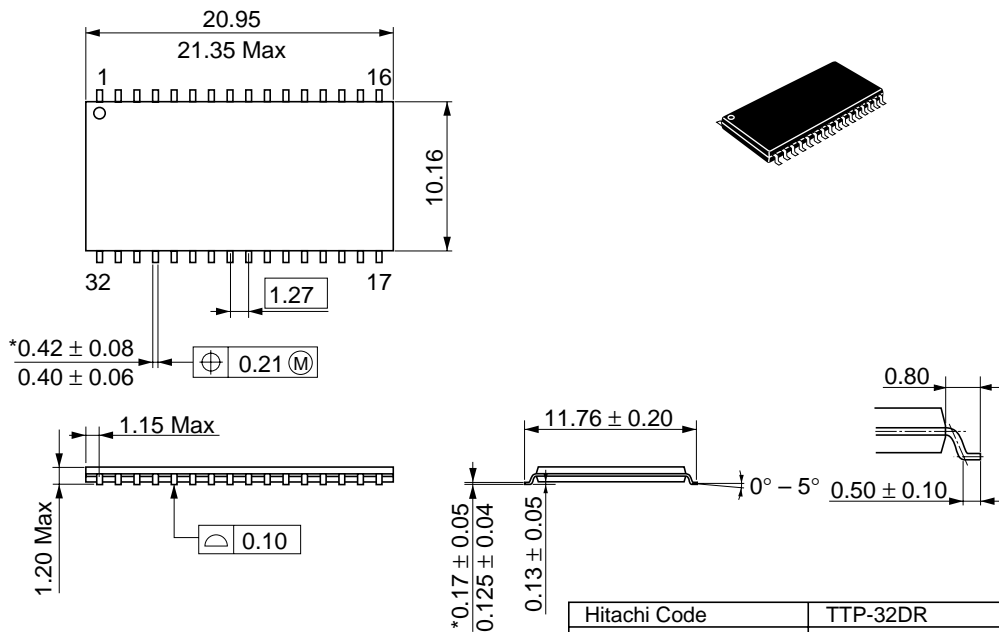
*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-32D
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.51 g

Package Dimensions (cont.)

HM62V8512BLRR Series (TTP-32DR)

Unit: mm



*Dimension including the plating thickness
Base material dimension

Hitachi Code	TTP-32DR
JEDEC	Conforms
EIAJ	—
Weight (reference value)	0.51 g

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HITACHI

Hitachi, Ltd.

Semiconductor & Integrated Circuits.

Nippon Bldg., 2-6-2, Ōhte-machi, Chiyoda-ku, Tokyo 100-0004, Japan

Tel: Tokyo (03) 3270-2111 Fax: (03) 3270-5109

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For further information write to:

Hitachi Semiconductor
(America) Inc.
179 East Tasman Drive,
San Jose, CA 95134
Tel: <1> (408) 433-1990
Fax: <1> (408) 433-0223

Hitachi Europe GmbH
Electronic components Group
Dornacher Straße 3
D-85622 Feldkirchen, Munich
Germany
Tel: <49> (89) 9 9180-0
Fax: <49> (89) 9 29 30 00

Hitachi Europe Ltd.
Electronic Components Group.
Whitebrook Park
Lower Cookham Road
Maidenhead
Berkshire SL6 8YA, United Kingdom
Tel: <44> (1628) 585000
Fax: <44> (1628) 778322

Hitachi Asia Pte. Ltd.
16 Collyer Quay #20-00
Hitachi Tower
Singapore 049318
Tel: 535-2100
Fax: 535-1533

Hitachi Asia Ltd.
Taipei Branch Office
3F, Hung Kuo Building, No.167,
Tun-Hwa North Road, Taipei (105)
Tel: <886> (2) 2718-3666
Fax: <886> (2) 2718-8180

Hitachi Asia (Hong Kong) Ltd.
Group III (Electronic Components)
7/F., North Tower, World Finance Centre,
Harbour City, Canton Road, Tsim Sha Tsui,
Kowloon, Hong Kong
Tel: <852> (2) 735 9218
Fax: <852> (2) 730 0281
Telex: 40815 HITEC HX

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Revision Record

Rev.	Date	Contents of Modification	Drawn by	Approved by
0.0	Apr. 24, 1998	Initial issue	M. Higuchi	K. Imato
0.1	Nov. 19, 1998	DC Characteristics I_{CC1} max: 30 mA to 40 mA I_{SB1} max: 20/2 μ A to 40/20 μ A Low V_{CC} Data Retention Characteristics I_{CCDR} max: 10/1 μ A to 20/10 μ A Change of note1 and 2	S. Kunito	K. Imato
1.0	Dec. 17, 1998	Deletion of Preliminary Features Change of Power dissipation Active: TBD (typ) to 15 mW/MHz (typ) Standby: TBD (typ) to 3 μ W (typ) DC Characteristics I_{CC2} typ: TBD to 5 mA I_{SB1} typ: TBD/TBD to 1/1 μ A Low V_{CC} Data Retention Characteristics I_{CCDR} typ: TBD/TBD to 0.8/0.8 μ A	S. Kunito	K. Imato
2.0	Jan. 29, 1999	Low V_{CC} Data Retention Characteristics Change of Low V_{CC} Data Retention Timmng Waveform	S. Kunito	K. Imato
3.0	Apr. 8, 1999	Addition of L-UL-version DC Characteristics I_{SB1} typ: 1/1 μ A to 1/1/1 μ A I_{SB1} max: 40/20 μ A to 40/20/5 μ A Addition of note4 Low V_{CC} Data Retention Characteristics I_{CCDR} typ: 0.8/0.8 μ A to 0.8/0.8/0.8 μ A I_{CCDR} max: 20/10 μ A to 20/10/2 μ A Addition of note3	S. Kunito	K. Imato
4.0	Aug. 24, 1999	Low V_{CC} Data Retention Characteristics Correct error: t_R unit ms to ns	S. Kunito	K. Imato
5.0	Oct. 20, 1999	Low V_{CC} Data Retention Characteristics Change of Low V_{CC} Data Retention Timmng Waveform	I. Ogiwara	K. Imato
6.0	Mar. 31, 2000	AC Characteristics Test Conditions: Output timing reference level 0.8 V/2.0 V to 1.5 V/1.5 V (HM62V8512B-7) 0.8 V/2.0 V (HM62V8512B-8)		