Ordering number: EN3803

CMOS LSI

No. 3803

LC7802

Output Port Expansion IC for VTR Applications

Advanced Information

OVERVIEW

The LC7802 is an output port expansion IC that incorporates a 10-bit serial-to-parallel converter, controlled by an external microcontroller, making it ideal for video tape recorder (VTR) applications.

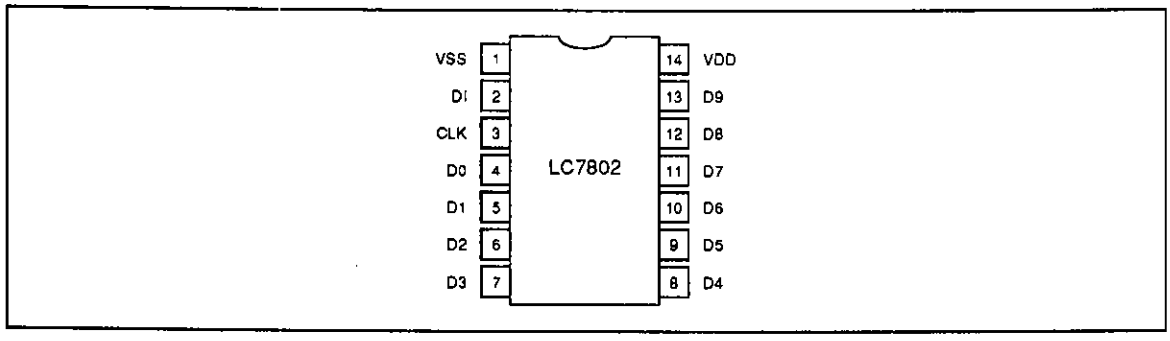
The LC7802 features tristate outputs and an automatically generated latch signal. It also features reset initialization at power-ON to initialize the outputs in the high-impedance state.

The LC7802 operates from a 5 V supply and is available in 14-pin DIPs.

FEATURES

- 10-bit serial-to-parallel converter
- Tristate outputs
- Reset initialization at power-ON
- Latch signal generated automatically
- 5 V supply
- 14-pin DIP

PINOUT



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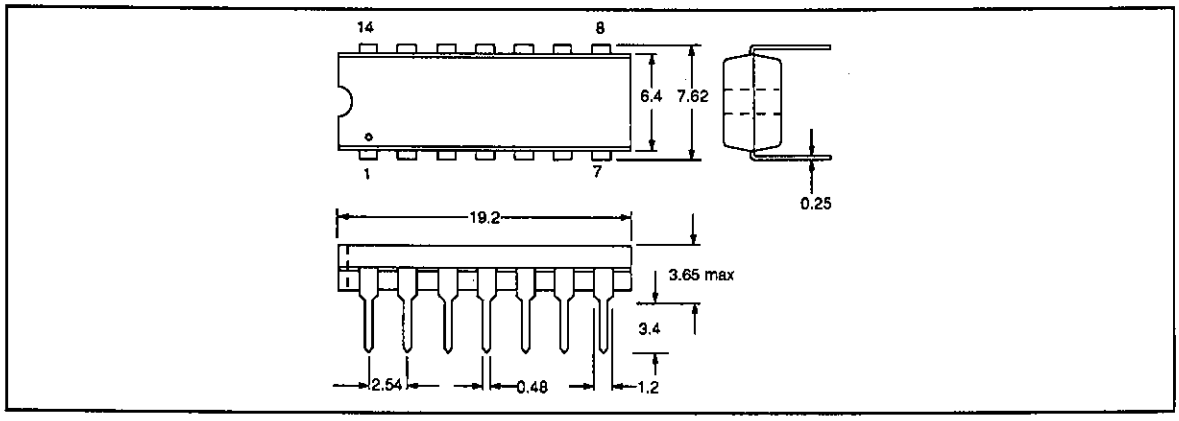
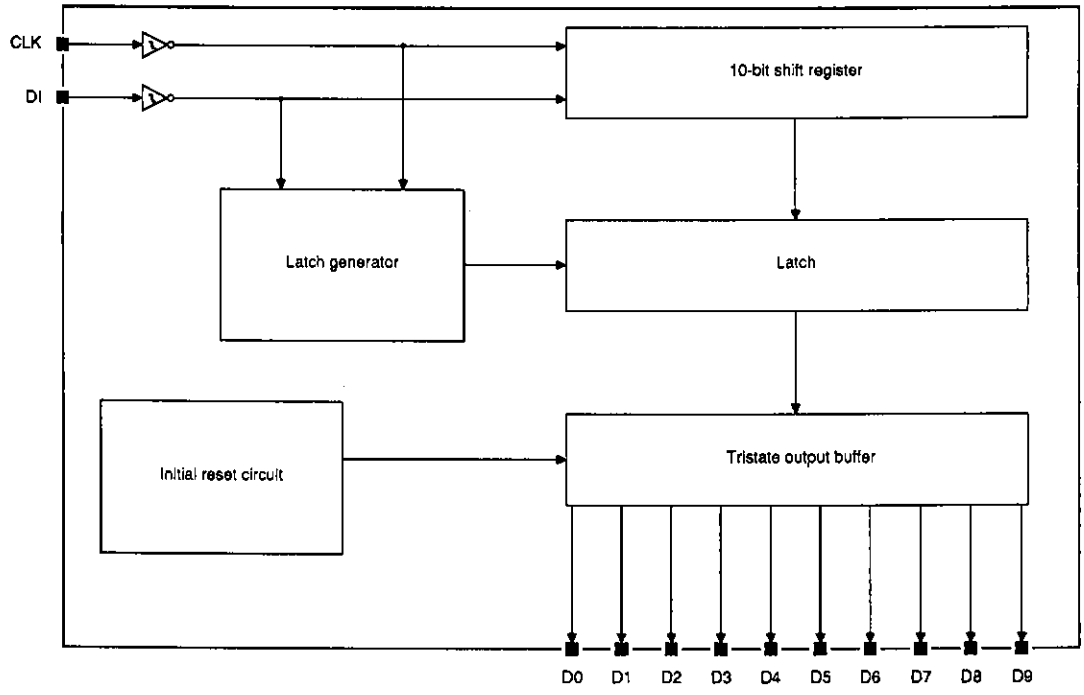
PACKAGE DIMENSIONS

Unit: mm

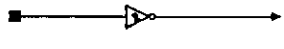
3003A-DIP14

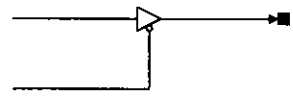


BLOCK DIAGRAM



PIN DESCRIPTION

Number	Name	Equivalent circuit	• Description
1	VSS		Ground
2	DI		Serial data input
3	CLK		Clock input

Number	Name	Equivalent circuit	Description
4 to 13	D0 to D9		Data outputs
14	VDD		5 V supply

SPECIFICATIONS

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage range	V_{DD}	–0.3 to 7.0	V
DI and CLK input voltage range	V_I	–0.3 to V_{DD} + 0.3	V
D0 to D9 output voltage range	V_O	–0.3 to V_{DD} + 0.3	V
D0 to D9 output current	I_O	2	mA
Power dissipation	P_D	200	mW
Operating temperature range	Topr	–30 to 70	°C
Storage temperature range	T_{stg}	–40 to 125	°C

Recommended Operating Conditions

T_a = 25 °C

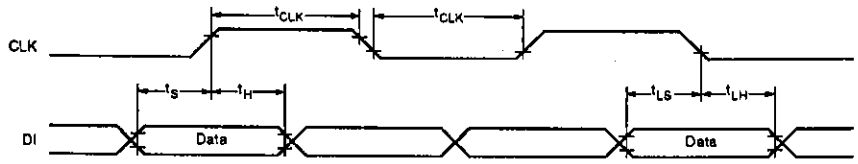
Parameter	Symbol	Rating	Unit
Supply voltage	V_{DD}	5	V
Supply voltage range	V_{DD}	4.5 to 5.5	V

Electrical Characteristics

V_{DD} = 5 V, T_a = –30 to 70 °C

Parameter	Symbol	Condition	Rating			Unit
			min	typ	max	
DI and CLK LOW-level input voltage	V_{IL}		V_{SS} – 0.3	–	$0.2V_{DD}$	V
DI and CLK HIGH-level input voltage	V_{IH}		$0.8V_{DD}$	–	V_{DD} + 0.3	V
D0 to D9 LOW-level output voltage	V_{OL}	I_{OL} = 1.0 mA	–	–	0.4	V
D0 to D9 HIGH-level output voltage	V_{OH}	I_{OH} = –1.0 mA	V_{DD} – 0.4	–	–	V
Hysteresis voltage	V_{HYS}		–	$0.1V_{DD}$	–	V
Standby supply current	I_{DD}	V_{IN} = V_{DD} or V_{SS}, outputs open	–	–	3	μA

Timing Characteristics



V_{DD} = 5 ±0.5 V, T_a = −30 to 70 °C

Parameter	Symbol	Rating			Unit
		min	typ	max	
CLK input minimum clock pulsewidth	t_{CLK}	500	–	–	ns
DI input data shift setup time	t_S	200	–	–	ns
DI input data shift hold time	t_H	200	–	–	ns
DI input data latch setup time	t_{LS}	200	–	–	ns
DI input data latch hold time	t_{LH}	250	–	–	ns

FUNCTIONAL DESCRIPTION

System Timing

At power-ON, a reset initialization occurs to ensure that the outputs are in the high-impedance state before the first latch signal.

Data is shifted into the shift register on the rising edge of the clock, CLK. The shift register contents are latched on the falling edge of CLK when DI is HIGH. The system timing is shown in figure 1.

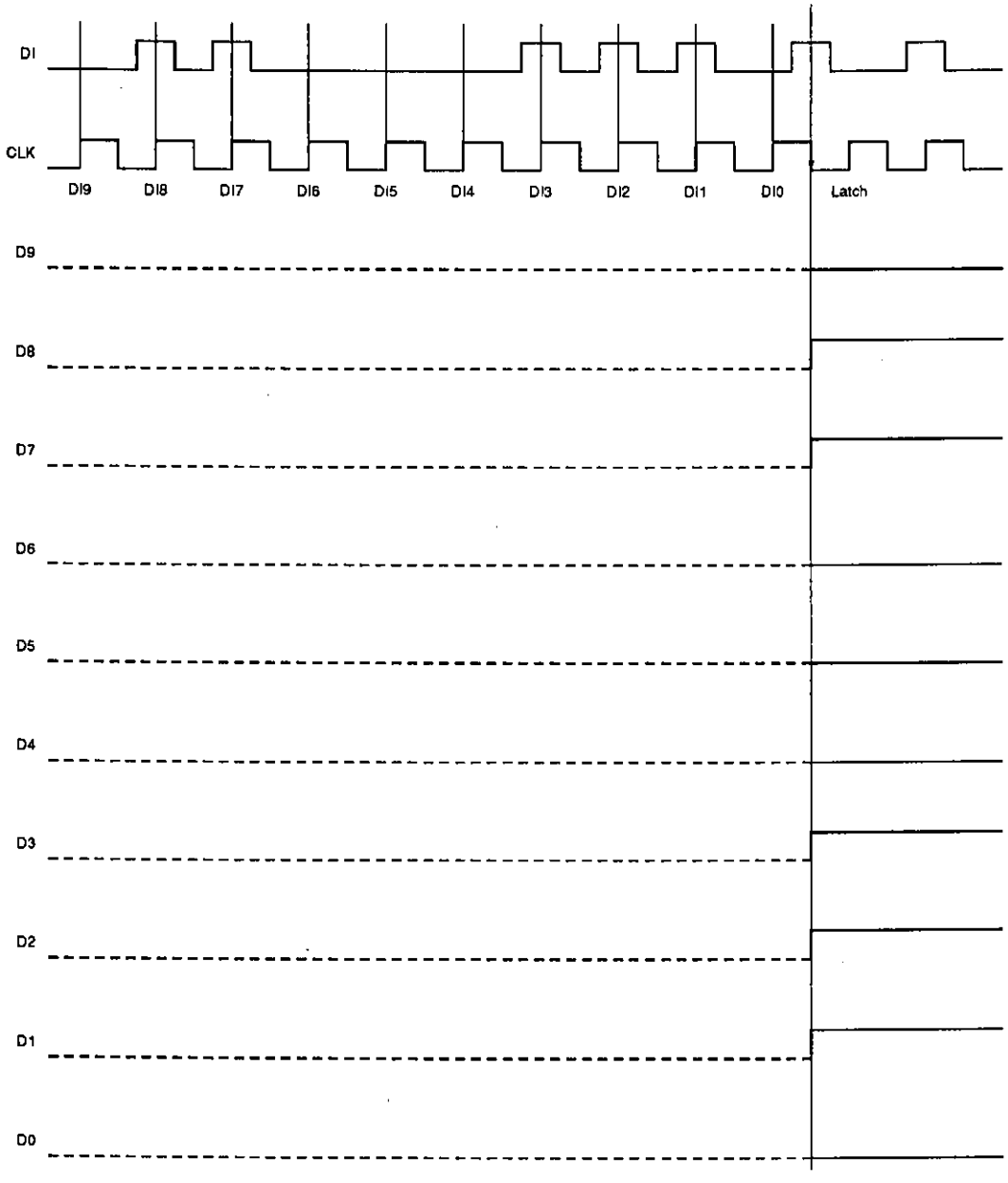


Figure 1. System timing