

CMOS 8-bit Single Chip Microcomputer

Piggyback/
evaluator type

Description

The CXP87300 is a CMOS 8-bit single chip micro-computer of piggyback/evaluator combined type, which is developed for evaluating the function of the CXP87352/87360.

Features

- A wide instruction set (213 instructions) which cover various types of data.
 - 16-bit operation/multiplication and division/boolean bit operation instructions

- Minimum instruction cycle
 - 333ns at 12MHz operation (3.0 to 5.5V)
 - 250ns at 16MHz operation (4.5 to 5.5V)
 - 122μs at 32kHz operation

- Applicable EPROM
 - LCC type 27C256, LCC type 27C512 (Maximum 60Kbytes are available.)

- Incorporated RAM capacity
 - 2048 bytes

- Peripheral functions

- A/D converter

8-bit, 12-channel, successive approximation method
(Conversion time of 20μs/16MHz)

- Serial interface

Incorporated buffer RAM

(Auto transfer for 1 to 32 bytes), 1 channel

Incorporated 8-bit and 8-stage FIFO

(Auto transfer for 1 to 8 bytes), 1 channel

- Timer

8-bit timer, 8-bit timer/counter

19-bit time base timer, 32kHz timer/counter

- High precision timing pattern generator

PPG 19-pin, 32-stage programmable

RTG 5 pins, 2 channels

- PWM/DA gate output

PWM output 12 bits, 2 channels

(Repetitive frequency 62.5kHz/16MHz)

DA gate pulse output 13 bits, 4channels

Capstan FG, drum FG/PG, CTL input

- Servo input control

- VSYNC separator

- FRC capture unit

- PWM output

Incorporated 26-bit and 8-stage FIFO

14 bits, 1 channel

- VISS/VASS circuit

Pulse duty auto detection circuit

- Remote control receiving circuit

8-bit pulse measurement counter with on-chip 6-stage FIFO

- General purpose prescaler

7 bits (SYNC1 input frequency division, FRC capture possible.)

- HSYNC counter

12-bit event counter (SYNC1 input count)

- Interruption

22 factors, 15 vectors, multi-interruption possible

- Standby mode

SLEEP/STOP

- Package

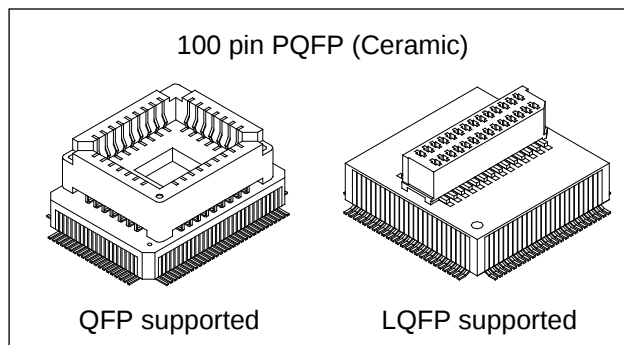
100-pin ceramic PQFP

Note) Mask option depends on the type of the CXP87300. Refer to the Products List for details.

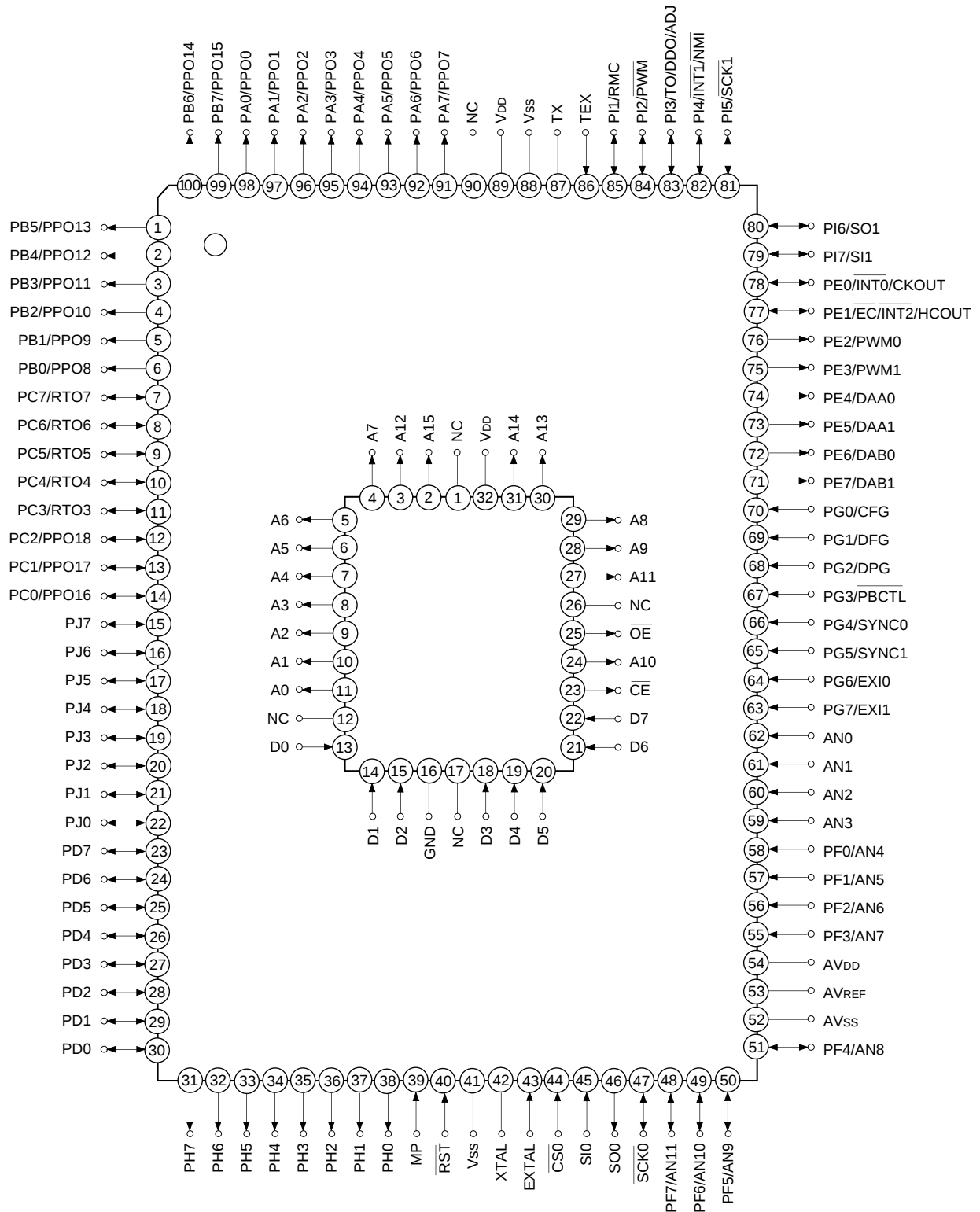
Structure

Silicon gate CMOS IC

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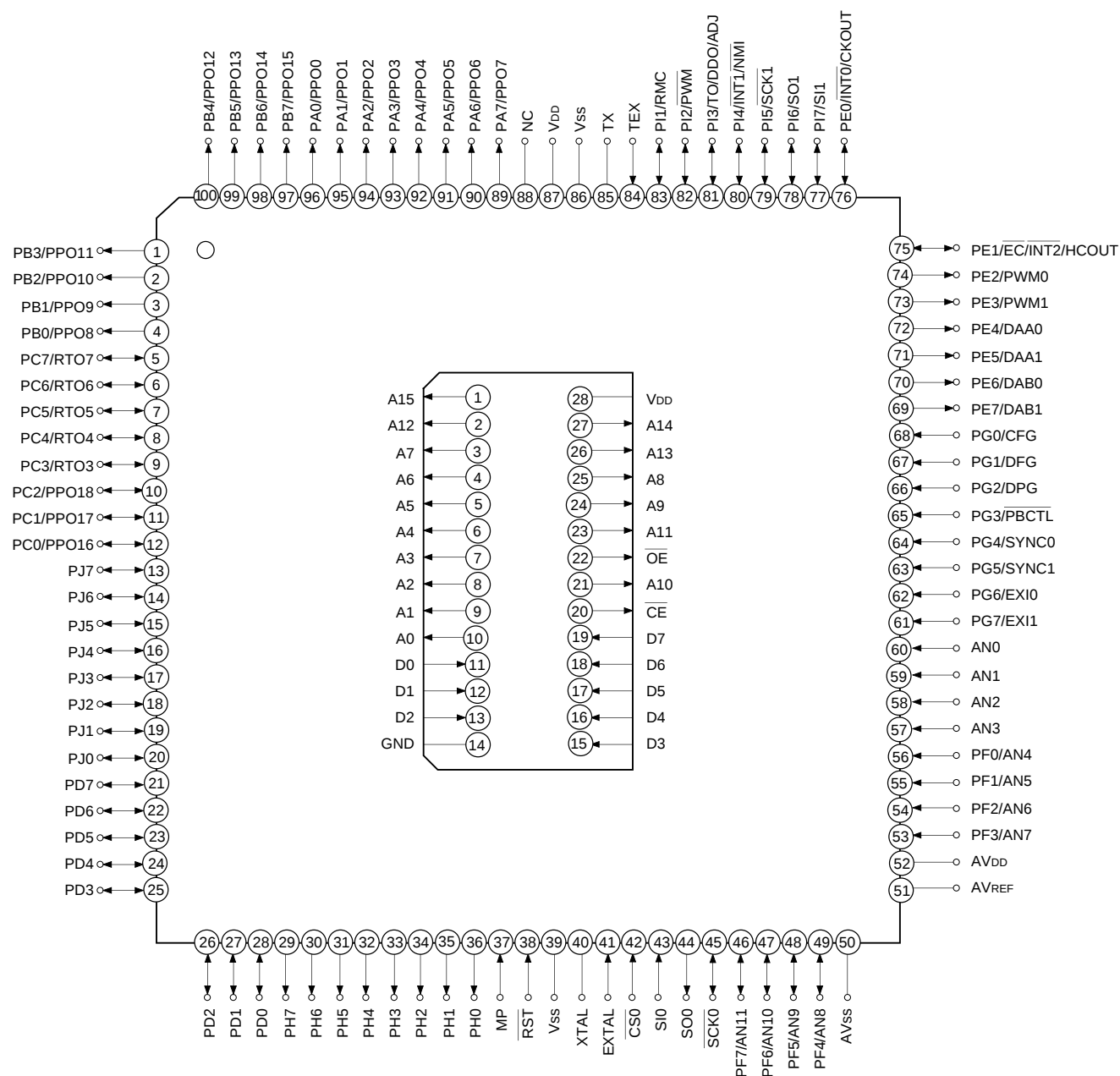


Pin Assignment in Piggyback Mode (QFP package)



- Note)** 1. NC (Pin 90) is always connected to V_{DD}.
 2. V_{ss} (Pins 41 and 88) are both connected to GND.
 3. MP (Pin 39) is always connected to GND.

Pin Assignment in Piggyback Mode (LQFP package)



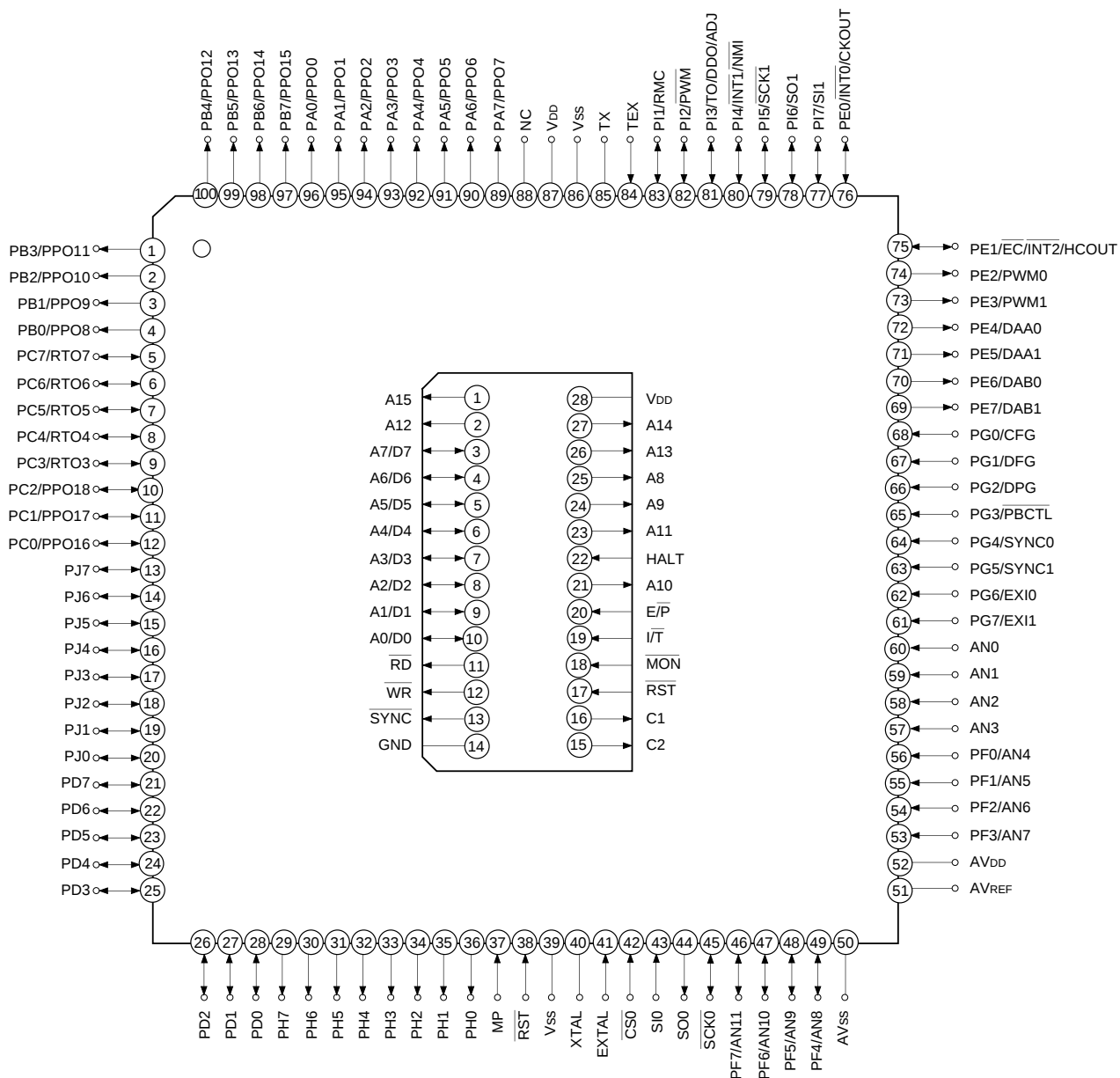
- Note)**
1. NC (Pin 88) is always connected to VDD.
 2. Vss (Pins 39 and 86) are both connected to GND.
 3. MP (Pin 37) is always connected to GND.

The diagram shows the ATmega328P microcontroller with pins numbered 1 to 50. The functions for each pin are as follows:

- Pin 1:** PB5/PPO13
- Pin 2:** PB4/PPO12
- Pin 3:** PB3/PPO11
- Pin 4:** PB2/PPO10
- Pin 5:** PB1/PPO9
- Pin 6:** PB0/PPO8
- Pin 7:** PC7/RTO7
- Pin 8:** PC6/RTO6
- Pin 9:** PC5/RTO5
- Pin 10:** PC4/RTO4
- Pin 11:** PC3/RTO3
- Pin 12:** PC2/PPO18
- Pin 13:** PC1/PPO17
- Pin 14:** PC0/PPO16
- Pin 15:** PJ7
- Pin 16:** PJ6
- Pin 17:** PJ5
- Pin 18:** PJ4
- Pin 19:** PJ3
- Pin 20:** PJ2
- Pin 21:** PJ1
- Pin 22:** PJ0
- Pin 23:** PD7
- Pin 24:** PD6
- Pin 25:** PD5
- Pin 26:** PD4
- Pin 27:** PD3
- Pin 28:** PD2
- Pin 29:** PD1
- Pin 30:** PD0
- Pin 31:** PH7
- Pin 32:** PH6
- Pin 33:** PH5
- Pin 34:** PH4
- Pin 35:** PH3
- Pin 36:** PH2
- Pin 37:** PH1
- Pin 38:** PH0
- Pin 39:** MP
- Pin 40:** RST
- Pin 41:** Vss
- Pin 42:** XTAL
- Pin 43:** EXTAL
- Pin 44:** CS0
- Pin 45:** SIO
- Pin 46:** SO0
- Pin 47:** SCK0
- Pin 48:** PF7/AN11
- Pin 49:** PF6/AN10
- Pin 50:** PF5/AN9

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Pin Assignment in Evaluator Mode (LQFP package)



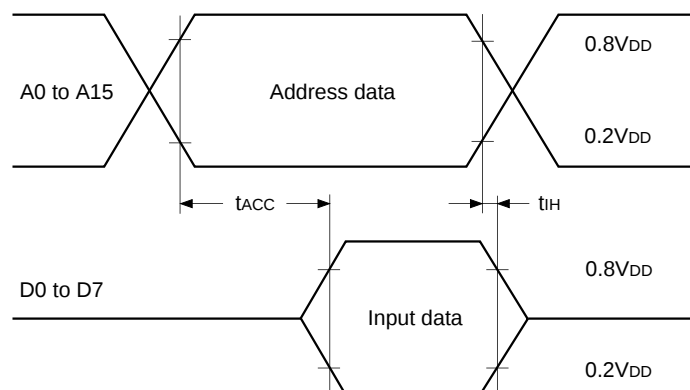
- Note)** 1. NC (Pin 88) is always connected to V_{DD}.
 2. V_{SS} (Pins 39 and 86) are both connected to GND.
 3. MP (Pin 37) is always connected to GND.

EPROM Read Timing ($T_a = -20$ to $+75^{\circ}\text{C}$, $V_{DD} = 3.0$ to 5.5V , $V_{SS} = 0\text{V}$)

Item	Symbol	Pin	Min.	Max.	Unit
Address → data input delay time	t_{ACC}	A0 to A15 D0 to D7		100 ^{*1}	ns
				75 ^{*2}	
Address → data hold time	t_{IH}	A0 to A15 D0 to D7	0		ns

^{*1} At 12MHz operation ($V_{DD} = 4.5$ to 5.5V)

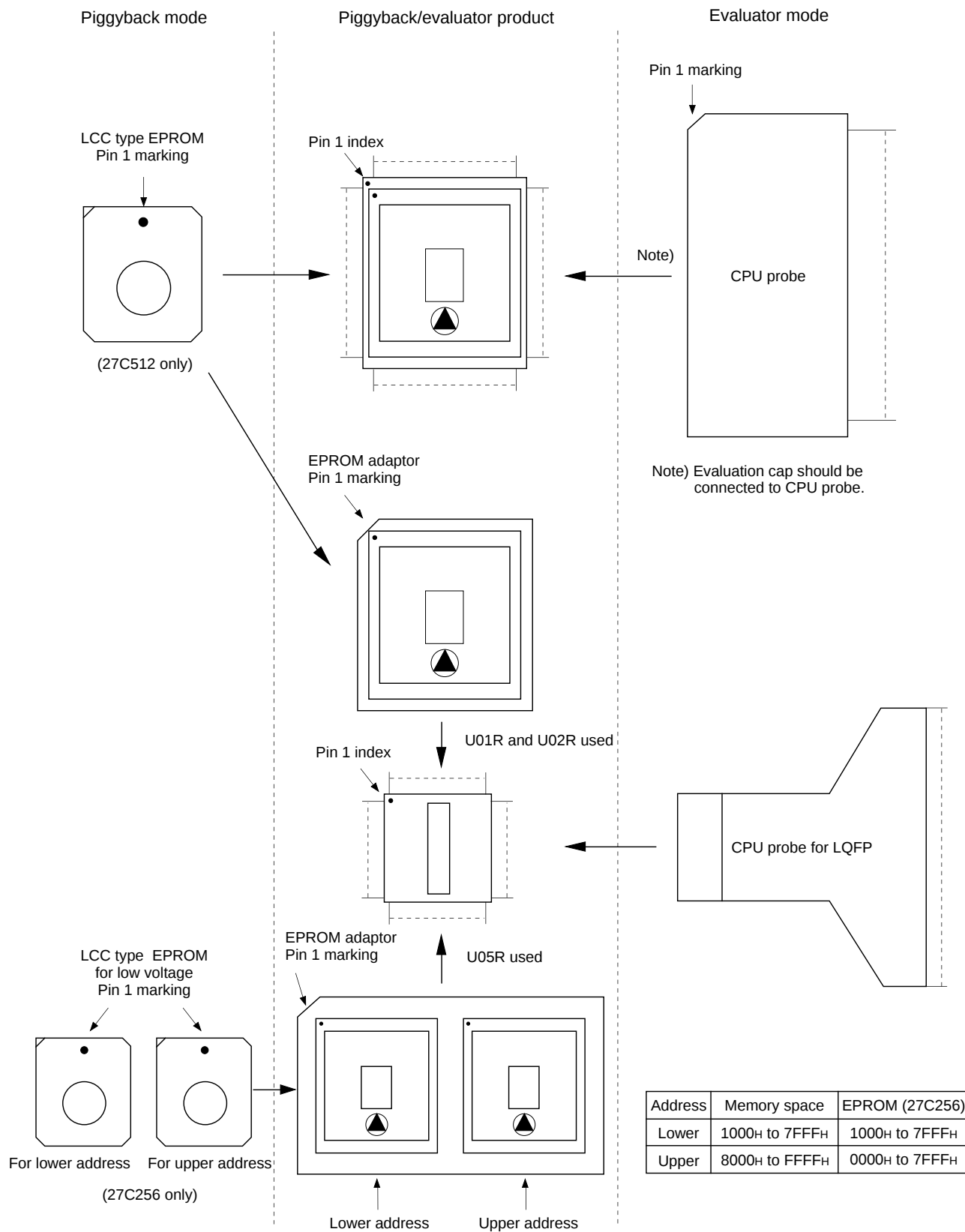
^{*2} At 12MHz operation ($V_{DD} = 3.0$ to 5.5V), At 16MHz operation ($V_{DD} = 4.5$ to 5.5V)

**Products List**

Option item	Products				
	Mask product		Piggyback/evaluator product		
	CXP87352	CXP87360	CXP87300-U01Q CXP87300-U01R	CXP87300-U02Q CXP87300-U02R	CXP87300-U05R
Package	100-pin plastic QFP/LQFP		100-pin ceramic PQFP		
ROM capacity	52Kbytes	60Kbytes	EPROM 60Kbytes		
			27C512 × 1	27C512 × 1	27C256 × 2
Pull-up resistor for reset pin	Existent/Non-existent		Existent		
Input circuit format*1	CMOS schmitt/TTL schmitt		TTL schmitt	CMOS schmitt	CMOS schmitt

^{*1} On PG4/SYNC0 pin and PG5/SYNC1 pin, the input circuit format can be selected to every pin.

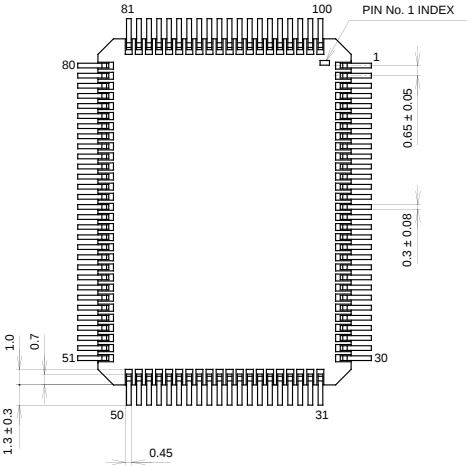
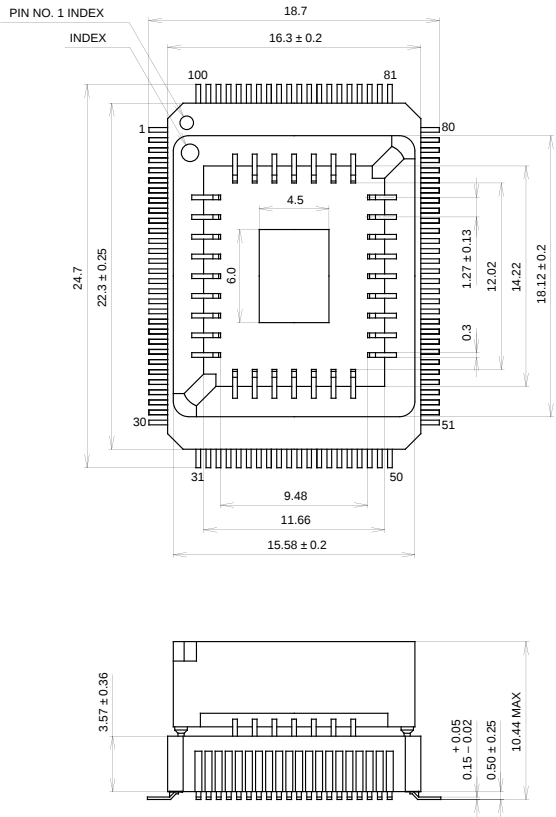
Piggyback mode/evaluator mode can be switched as shown below.



Package Outline

Unit: mm

100PIN PQFP (CERAMIC)

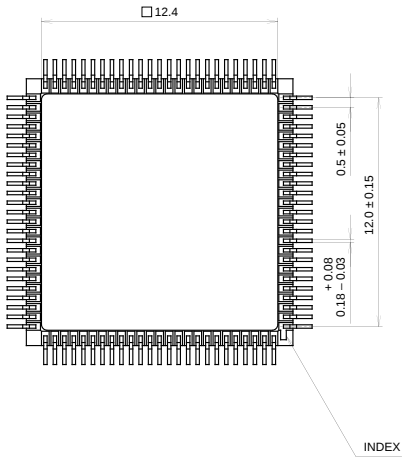
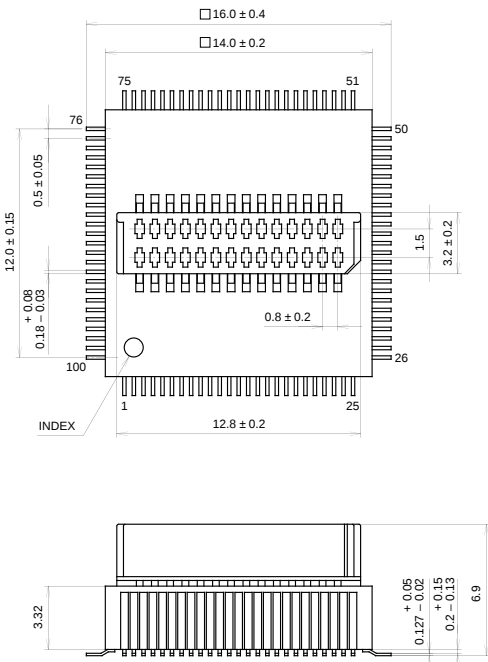


PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L01
EIAJ CODE	AQFP100-C-0000-A
JEDEC CODE	

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	5.7g

100PIN PQFP (CERAMIC)



PACKAGE STRUCTURE

SONY CODE	PQFP-100C-L02
EIAJ CODE	AQFP100-C-1414-A
JEDEC CODE	

PACKAGE MATERIAL	CERAMIC
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE WEIGHT	2.2g