Micro Linear

ML4621

Data Quantizer

GENERAL DESCRIPTION

The ML4621 data quantizer is a low noise, wideband monolithic IC designed specifically for signal recovery applications in fiber-optic receiver systems. It contains a two stage wideband limiting amplifier which is capable of accepting an input signal as low as 2mV with a 55dB dynamic range. This high level of sensitivity is achieved by using a DC restoration feedback loop which nulls any offset voltage produced in the limiting amplifier.

The output stage is a high speed comparator circuit with both TTL and ECL outputs. An enable pin is included for added control.

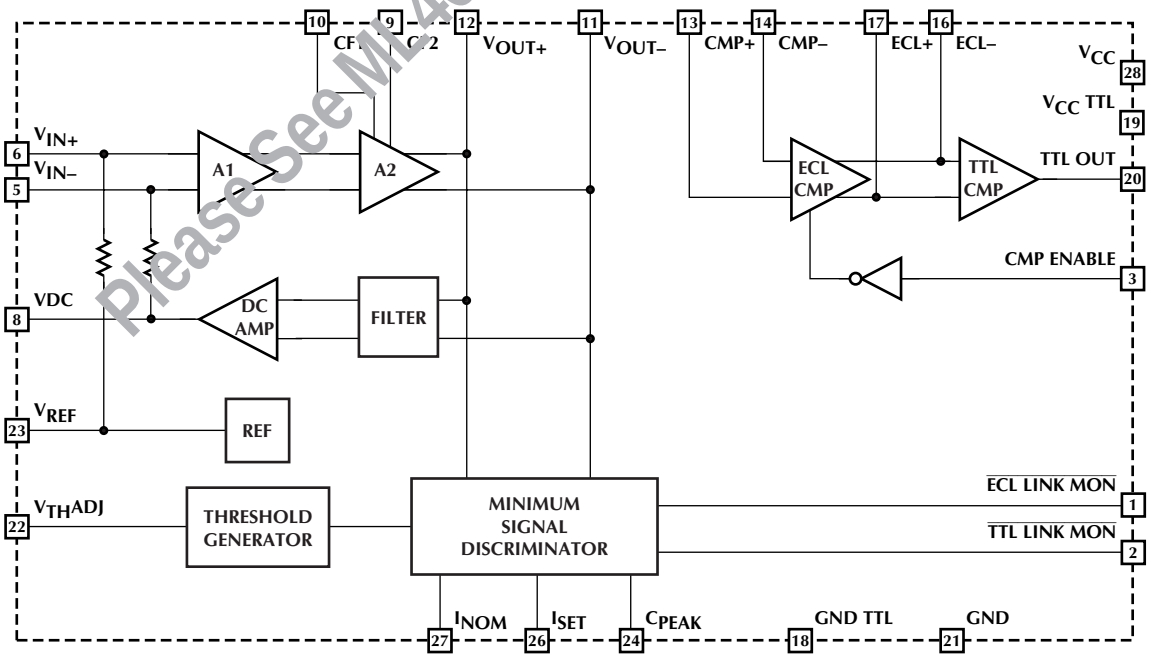
The minimum signal discriminator circuit provides a link monitor function with a user selectable reference voltage. This circuit monitors the peaks of the input signal and provides a logic level output indicating when the input falls below an acceptable level. This output can be used to disable the quantizer and/or drive an LED, providing a visible link status.

FEATURES

- 50MHz minimum bandwidth for data rates of up to 100MBd
- Can be powered by either 5V providing TTL level outputs, or -5.2V providing ECL level outputs
- Low noise design: 25µV RMS over 50MHz noise bandwidth
- Adjustable link monitor function
- Wide 55dB input dynamic range
- 10ns minimum input pulse

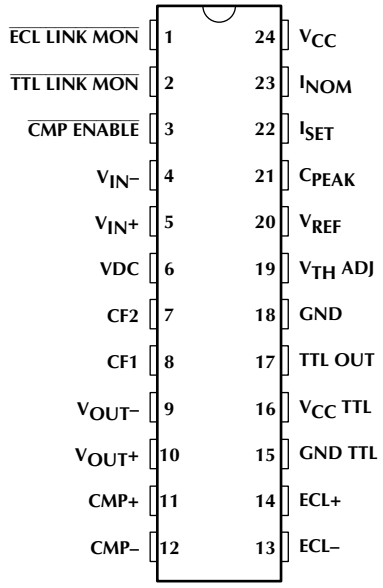
Please See ML4622/ML4624 for New Designs

BLOCK DIAGRAM (Pin Configuration Shown is for PLCC Version)



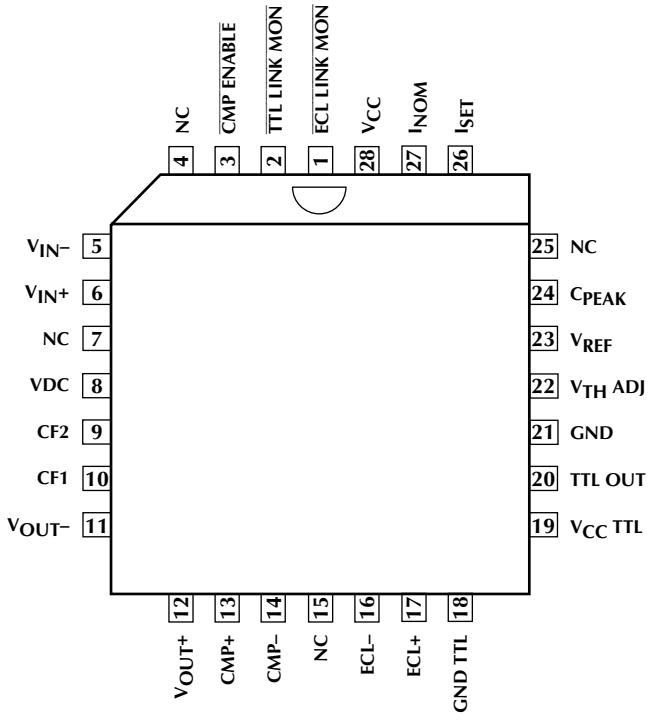
PIN CONFIGURATION

ML4621
24-Pin Narrow DIP (P24N)



TOP VIEW

ML4621
28-Pin PLCC (Q28)



TOP VIEW

PIN DESCRIPTION (Pin Number in Parenthesis is for DIP Version)

PIN	NAME	FUNCTION
1 (1)	$\overline{\text{ECL LINK MON}}$	ECL link monitor output. Signal is low when the V_{IN}+ and V_{IN}– inputs exceed the minimum threshold set by a voltage on V_{TH} ADJ. Signal is high when input signal level is below that threshold.
2 (2)	$\overline{\text{TTL LINK MON}}$	TTL link monitor output. Same logic function as the $\overline{\text{ECL LINK MON}}$. Capable of driving a 10mA LED indicator. This pin is normally tied to $\overline{\text{CMP ENABLE}}$.
3 (3)	$\overline{\text{CMP ENABLE}}$	Low voltage at this TTL input enables both the ECL and TTL outputs. A high TTL voltage disables the comparator output with ECL+ high, ECL– low, and TTL OUT high.
5 (4)	V_{IN}–	This input should be capacitively coupled to the input source or to ground. (Input resistance is approximately 8kΩ).
6 (5)	V_{IN}+	This input should be capacitively coupled to the input source or to ground. (Input resistance is approximately 8kΩ).
8 (6)	VDC	An external capacitor on this pin integrates an error signal which nulls the offset of the input amplifier. If the DC feedback loop is not being used, this pin should be connected to V_{REF}.
9 (7)	CF2	A capacitor from this pin to ground controls the maximum bandwidth of the amplifier to accommodate lower operating frequencies.
10 (8)	CF1	The capacitor on this pin should match the one on CF2.
11 (9)	V_{OUT}-	Negative output of the amplifier, which is normally tied to CMP–.
12 (10)	V_{OUT}+	Positive output of the amplifier, which is normally tied to CMP+.
13 (11)	CMP+	Comparator input pin. Open base configuration relies on the DC bias of the amp output to set proper DC operating voltage. Reestablish voltage if filtering is used between V_{OUT}+ and CMP+.
14(12)	CMP–	Comparator input pin. Open base configuration relies on the DC bias of the amp output to set the proper DC operating voltage. Reestablish voltage if filtering is used between V_{OUT}– and CMP–.
16(13)	ECL–	ECL comparator negative output.
17(14)	ECL+	ECL comparator positive outout.
18(15)	GND TTL	Negative supply for the TTL comparator stage. If the TTL output is not necessary, connect GND TTL and V_{CC} TTL to V_{CC}.
19(16)	V_{CC} TTL	Positive supply for the TTL comparator stage. If the TTL output is not necessary, connect GND TTL and V_{CC} TTL to V_{CC}.
20(17)	TTL OUT	TTL data output (totem pole type output stage).
21(18)	GND	Negative supply. Connect to –5.2V for ECL operation, or to source ground for TTL operation.
22(19)	V_{TH} ADJ	This input sets the minimum amplitude of the input signal required to cause the link monitors to go low.
23(20)	V_{REF}	A 2.5V reference with respect to GND.
24(21)	C_{PEAK}	A capacitor from this pin to GND determines the link monitor response time.
26(22)	I_{SET}	Current into an internal diode connected between this pin and GND is turned around and pulled from C_{PEAK}. This pin is normally connected to I_{NOM}.
27(23)	I_{NOM}	Sets a current of approximately 125µA when connected to I_{SET}.
28(24)	V_{CC}	Positive supply. Connect to source ground for ECL operation, or to 5V for TTL operation.

ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are those values beyond which the device could be permanently damaged. Absolute maximum ratings are stress ratings only and functional device operation is not implied.

V_{CC} – GND ..... –0.3V to 7.0V
V_{CC} TTL – GND TTL ..... –0.3V to 7.0V
GND ..... –0.3V to V_{CC} + 0.3V
Junction Temperature ..... 150°C
Storage Temperature Range ..... –65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 260°C
Thermal Resistance (θ_{JA})
24 Pin Narrow PDIP ..... 54°C/W
28 Pin PLCC ..... 68°C/W

OPERATING CONDITIONS

Temperature Range ..... 0°C to 70°C
–5.2V Supply Range ..... –5.2V ± 5%
+5V Supply Range ..... 5.0V ± 5%

ELECTRICAL CHARACTERISTICS

Unless otherwise specified, V_{CC} = 5V ± 5%, GND = 0V, T_A = Operating Temperature Range (Note 1)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
I_{CC1}	V_{CC} Supply Current	V_{CC} TTL = GND TTL = V_{CC}		65	100	mA
I_{CC2}	V_{CC} Supply Current (TTL OUT Enabled)	V_{CC} TTL = V_{CC} GND TTL = GND		70	110	mA
$I_{V_{REF}}$	V_{REF} Output Current		–5.0		0.5	mA
V_{REF}	Reference Voltage		2.40	2.55	2.65	V
A_V	A1, A2 Amplifier Gain	V_{IN} = 5mV		75		V/V
V_{IN}	Input Signal Range		2		1400	mV_{P-P}
V_{TH} ADJ Range	External Voltage at V_{TH} ADJ to set V_{TH}		1		2.5	V
V_{OS}	Input Offset	VDC = V_{REF} (DC Loop Inactive)		3		mV
E_N	Input Referred Noise	50MHz BW		25		µV
BW	3dB Bandwidth		50	65		MHz
V_{IN} PW	Minimum Input Pulsewidth			10		ns
R_{IN}	Input Resistance	V_{IN}+, V_{IN}–		8		kΩ
t_{PD} AMP	Amplifier Propagation Delay Time	From V_{IN}+, V_{IN}– to V_{OUT}+, V_{OUT}– V_{IN}+, = $10mV_{P-P}$	4		8	ns
t_{PD} ECL	ECL Comparator Propagation Delay Time	From CMP+, CMP– to ECL+, ECL– V_{IN}+, = $10mV_{P-P}$	4		8	ns
t_{PD} TTL	TTL Comparator Propagation Delay Time	From ECL+, ECL– to TTL OUT V_{IN}+, = $10mV_{P-P}$	4		8	ns
$R_{V_{TH}\ ADJ}$	V_{TH} ADJ Input Resistance			6.8		kΩ
$I_{V_{OUT}}$	V_{OUT}+, V_{OUT}– Output Current				3	mA
I_{CMP}	CMP+, CMP– Leakage Current			25		µA
VCM_{CMP}	CMP+, CMP– Common Mode Range		GND + 2		V_{CC} – 1	V
ECL V_{OH}	ECL+, ECL– Output High Voltage	With 200Ω Load Tied to V_{CC} – 2V T_A = 25ºC	3.90		4.30	V
ECL V_{OL}	ECL+, ECL– Output Low Voltage	With 200Ω Load Tied to V_{CC} – 2V T_A = 25ºC	3.11		3.38	V

ELECTRICAL CHARACTERISTICS (Continued)

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
A_V ECL	ECL CMP Gain			100		V/V
TTL V_{OH}	TTL Output High Voltage	V_{CC} TTL = 5V, I_{OH} = –50µA	2.4			V
TTL V_{OL}	TTL Output Low Voltage	V_{CC} TTL = 5V, I_{OL} = 2mA			0.4	V
TTL V_{IH}	TTL Input High Voltage Level		2.0			V
TTL V_{IL}	TTL Input Low Voltage Level				0.8	V
TTL I_{IH}	TTL Input High Current Level	V_{IH} = 2.4V	–50		50	µA
TTL I_{IL}	TTL Input Low Current Level	V_{IH} = 0.4V	–1.6		0	mA
I_{NOM}		$I_{NOM} = I_{SET}$		125		µA

Note 1: Limits are guaranteed by 100% testing, sampling, or correlation with worst case test conditions.

FUNCTIONAL DESCRIPTION

AMPLIFIER

The quantizer has a two stage limiting amplifier with an input common mode range of (GND + 1.8V) to (V_{CC} – 1.5V). Maximum sensitivity is achieved through the use of a DC restoration feedback loop and AC coupling on the input. The input DC bias voltage is set by an on-chip network at about 1.9V when it is AC coupled. These coupling capacitors, in conjunction with the input impedance of the amplifier, establish a highpass filter with a 3dB corner frequency, f_L, at:

$$f_L = \frac{1}{2\pi \times 8000 \times C} \quad (1)$$

Two capacitors of equal value are required since the amplifier has a differential input. One of the coupling capacitors can be tied to V_{CC} as shown in Figure 1 if the signal driving the input is single ended. The high corner frequency can also be adjusted by attaching capacitors to CF1 and CF2. The equation for adjusting this corner is:

$$f_H = \frac{1}{2\pi \times 425 \times C} \quad (2)$$

The offset voltage within the amplifier will be present at the amplifier's output even though the input is AC coupled. This is represented by V_{OS} in Figure 2. In order to reduce this error a DC feedback loop is incorporated. This negative feedback loop nulls the offset voltage, forcing V_{OS} to be zero. An external capacitor at V_{DC} is used to store the offset voltage. Although the value of this capacitor is noncritical, the pole it creates can affect the stability of the feedback loop. The value of this capacitor should be at least 100 times smaller than the input coupling capacitors to avoid stability problems using the ML4621.

The output of the ML4621 amplifier is isolated from the comparator and made available to the user. This allows the user to add circuitry between the amplifier and the comparator for wave shaping and other signal conditioning.

COMPARATOR

Two types of comparators are employed in the output section of these quantizers. The high speed ECL comparator is used to provide the ECL level outputs, and in turn drives the TTL comparator. The enable pin, $\overline{\text{CMP ENABLE}}$, is provided to control the ECL comparator. When $\overline{\text{CMP ENABLE}}$ is low the comparators function normally. When it is high it forces ECL+ high, ECL– low, and TTL OUT high. The $\overline{\text{CMP ENABLE}}$ pin can be controlled with TTL level signals when the quantizer is powered by 5V and ground.

LINK MONITOR

This function is implemented by the minimum signal discriminator and the threshold generator circuits. The purpose of this function is to monitor the input signal and provide a status signal indicating when the input falls below a preset voltage level. This is done by peak detecting the output of the amplifier section and comparing this level with the voltage at V_{TH}ADJ.

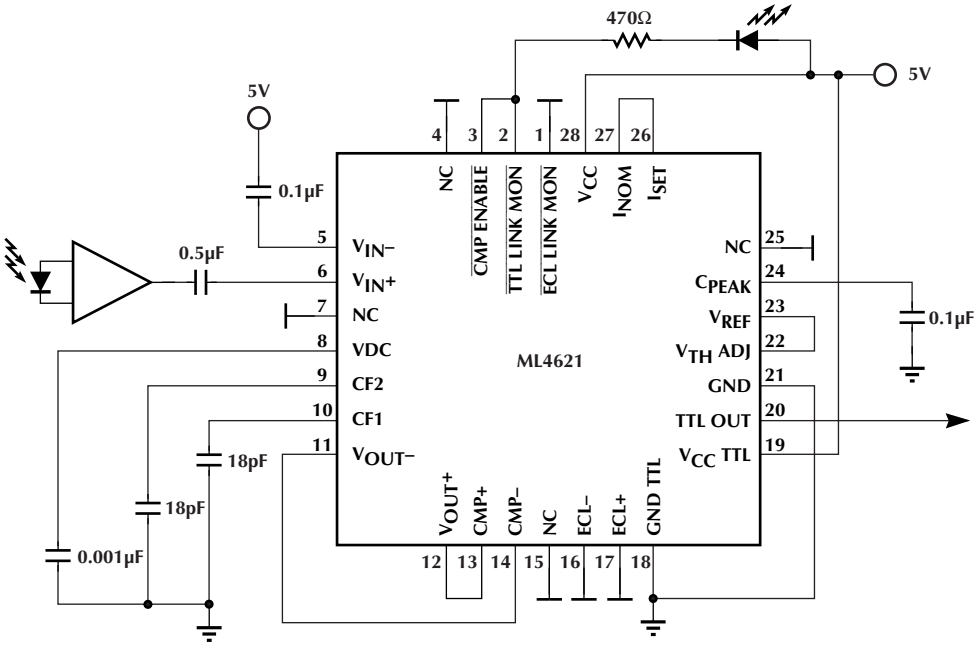


Figure 1. ML4621 Configured for 20MHz Bandwidth with TTL Output

FUNCTIONAL DESCRIPTION (Continued)

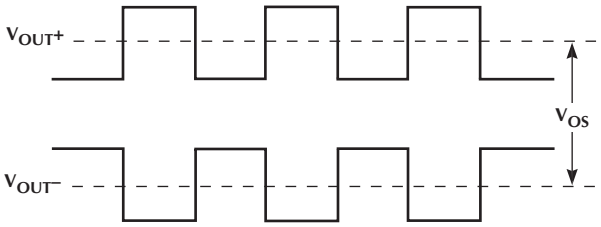


Figure 2.

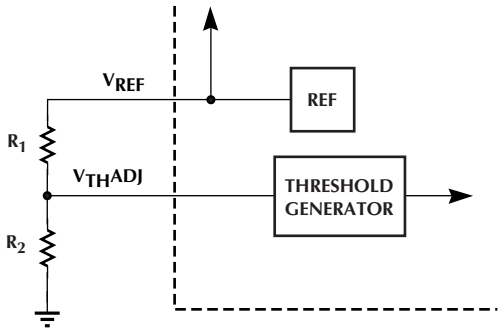


Figure 3.

The equation which determines the droop rate of the peak detector is:

$$\frac{dV}{dt} = \frac{I_{ISET}}{C} \quad (3)$$

In this equation C is the peak capacitor at C_{PEAK}. On the ML4621 the droop rate of the peak detector can be adjusted two ways:

1) By adjusting the value of the peak capacitor at C_{PEAK}.

2) By adjusting the charge current into the peak capacitor at I_{SET}.

The charge current, I_{ISET}, can be controlled externally by connecting a resistor, R_{EXT}, between I_{SET} and V_{CC}. I_{ISET} will then be:

$$I_{ISET} = \frac{V_{CC} - 0.7}{R_{EXT} + 1700} \quad (4)$$

For convenience an on-chip current source of 125µA is available by connecting I_{NOM} to I_{SET}.

The threshold generator level-shifts the reference voltage at $V_{TH}ADJ$ through a circuit which has a temperature coefficient matching that of the limiting amplifier. The relationship between $V_{TH}ADJ$ and V_{TH} (the minimum peak voltage at the input which will trigger the link monitor) is:

$$V_{TH}ADJ = (600 \times V_{TH}) + 0.7 \quad (5)$$

The on-chip reference voltage, V_{REF}, can be tied directly to $V_{TH}ADJ$ to set the threshold level. This will set the minimum input signal on the ML4621 at about 3mV (peak). A lower threshold level can be set by dividing down V_{REF} with a resistor string, as in Figure 3.

Since the ML4621 has a relatively low input impedance of 6.8kΩ and is offset by one diode drop, the equation which accounts for the load and offset is:

$$V_{TH}ADJ = \frac{R_2 \times ((6800 \times V_{REF}) + (0.7 \times R_1))}{6800 \times (R_1 + R_2) + R_1 \times R_2} \quad (6)$$

THRESHOLD ADJUSTMENT EXAMPLE

To make the link monitor trigger when the received optical power goes below 1µW (-30dBm), you first need to calculate the resultant voltage at $V_{IN}+$ and $V_{IN}-$. If a Hewlett-Packard HFBR-24X6 fiber-optic receiver with a responsive level of 8mV/µW is used, the peak-to-peak voltage would be:

$$1\mu W \times \frac{8mV}{\mu W} = 8mV_{P-P} \quad (7)$$

Then the link monitor should trigger at some point slightly lower than 4mV peak. Setting V_{TH} in Equation 5 to 3mV and solving for $V_{TH}ADJ$ yields:

$$V_{TH}ADJ = (600 \times 0.003) + 0.7 = 2.5V \quad (8)$$

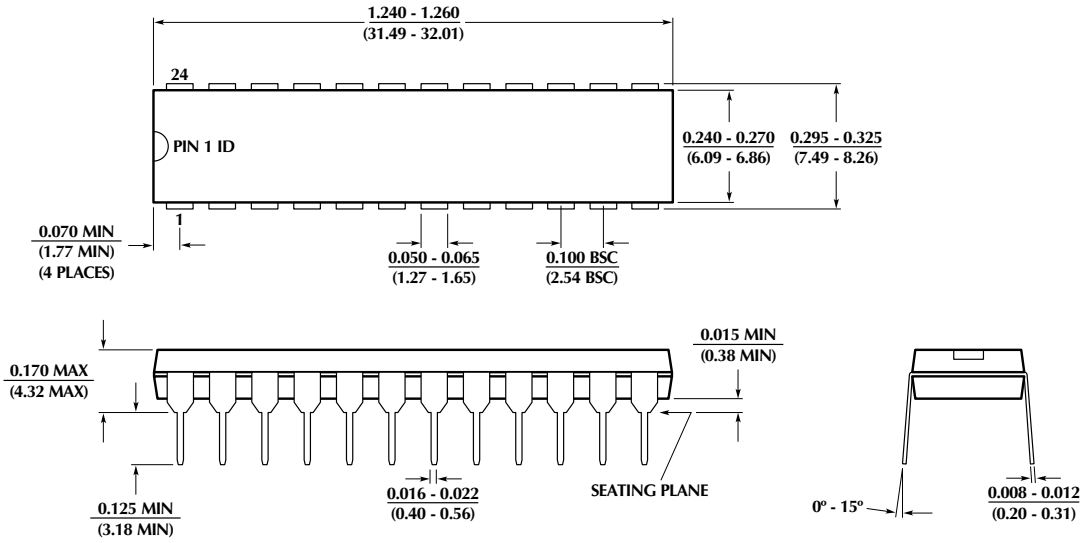
This is a convenient value since the reference voltage supplied by the quantizer, V_{REF}, is 2.5V.

The link monitor has about 0.4mV (peak) hysteresis built-in. More hysteresis can be induced by connecting a resistor between $\overline{\text{TTL LINK MON}}$ and $V_{TH}ADJ$ creating a positive feedback loop.

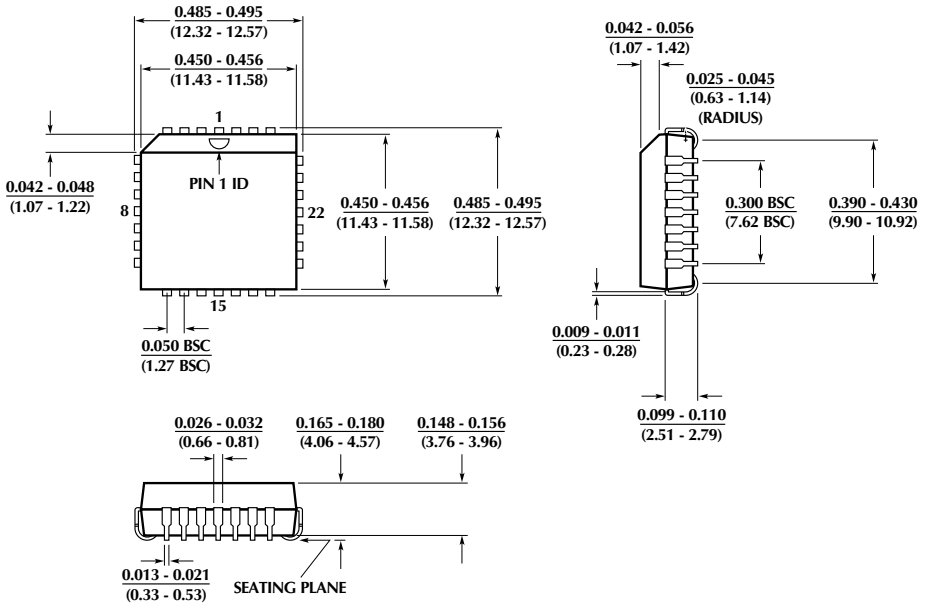
Refer to Micro Linear's Application Note 6 for more detail.

PHYSICAL DIMENSIONS inches (millimeters)

Package: P24N
24-Pin Narrow PDIP



Package: Q28
28-Pin PLCC



ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ML4621CP	0°C to 70°C	24 Pin Narrow PDIP (P24N)
ML4621CQ	0°C to 70°C	28 Pin PLCC (Q28)

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Products described herein may be covered by one or more of the following U.S. patents: 4,897,611; 4,964,026; 5,027,116; 5,281,862; 5,283,483; 5,418,502; 5,508,570; 5,510,727; 5,523,940; 5,546,017; 5,559,470; 5,565,761; 5,592,128; 5,594,376; 5,652,479; 5,661,427; 5,663,874; 5,672,959; 5,689,167; 5,714,897; 5,717,798. Japan: 2,598,946; 2,619,299; 2,704,176. Other patents are pending.

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