

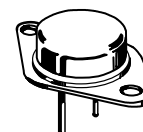
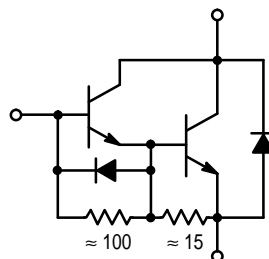
*Designer's™ Data Sheet*  
**SWITCHMODE Series**  
**NPN Silicon Power Darlington**  
**Transistors with Base-Emitter**  
**Speedup Diode**

**MJ10020**  
**MJ10021**

**60 AMPERE**  
**NPN SILICON**  
**POWER DARLINGTON**  
**TRANSISTORS**  
**200 AND 250 VOLTS**  
**250 WATTS**

The MJ10020 and MJ10021 Darlington transistors are designed for high-voltage, high-speed, power switching in inductive circuits where fall time is critical. They are particularly suited for line operated switchmode applications such as:

- AC and DC Motor Controls
- Switching Regulators
- Inverters
- Solenoid and Relay Drivers
- Fast Turn-Off Times
  - 150 ns Inductive Fall Time at 25°C (Typ)
  - 75 ns Inductive Storage Time at 25°C (Typ)
- Operating Temperature Range -65 to +200°C
- 100°C Performance Specified for:
  - Reversed Biased SOA with Inductive Loads
  - Switching Times with Inductive Loads
  - Saturation Voltages
  - Leakage Currents



**CASE 197A-05**  
**TO-204AE (TO-3)**

**MAXIMUM RATINGS**

Rating	Symbol	MJ10020	MJ10021	Unit
Collector-Emitter Voltage	$V_{CEO}$	200	250	Vdc
Collector-Emitter Voltage	$V_{CEV}$	300	350	Vdc
Emitter Base Voltage	$V_{EB}$	8.0		Vdc
Collector Current — Continuous	$I_C$	60		Adc
— Peak (1)	$I_{CM}$	100		
Base Current — Continuous	$I_B$	20		Adc
— Peak (1)	$I_{BM}$	30		
Total Power Dissipation @ $T_C = 25^\circ\text{C}$	$P_D$	250		Watts
@ $T_C = 100^\circ\text{C}$		143		
Derate above 25°C		1.43		W/°C
Operating and Storage Junction Temperature Range	$T_J, T_{stg}$	-65 to +200		°C

**THERMAL CHARACTERISTICS**

Characteristic	Symbol	Max	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	0.7	°C/W
Maximum Lead Temperature for Soldering Purposes: 1/8" from Case for 5 Seconds	$T_L$	275	°C

(1) Pulse Test: Pulse Width = 5 ms, Duty Cycle ≤ 10%.

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**Designer's Data for "Worst Case" Conditions** — The Designer's Data Sheet permits the design of most circuits entirely from the information presented. SOA Limit curves — representing boundaries on device characteristics — are given to facilitate "worst case" design.

# MJ10020 MJ10021

## ELECTRICAL CHARACTERISTICS (T<sub>C</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
<b>OFF CHARACTERISTICS</b>					
Collector–Emitter Sustaining Voltage (Table 1) (I <sub>C</sub> = 100 mA, I <sub>B</sub> = 0)	MJ10020 MJ10021 V <sub>CEO(sus)</sub>	200 250	— —	— —	Vdc
Collector Cutoff Current (V <sub>CEV</sub> = Rated Value, V <sub>BE(off)</sub> = 1.5 Vdc) (V <sub>CEV</sub> = Rated Value, V <sub>BE(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 150°C)	I <sub>CEV</sub>	— —	— —	0.25 5.0	mAdc
Collector Cutoff Current (V <sub>CE</sub> = Rated V <sub>CEV</sub> , R <sub>BE</sub> = 50 Ω, T <sub>C</sub> = 100°C)	I <sub>CER</sub>	—	—	5.0	mAdc
Emitter Cutoff Current (V <sub>EB</sub> = 2.0 V, I <sub>C</sub> = 0)	I <sub>EBO</sub>	—	—	175	mAdc

## SECOND BREAKDOWN

Second Breakdown Collector Current with base forward biased	I <sub>S/b</sub>			See Figure 13	
Clamped Inductive SOA with Base Reverse Biased	RBSOA			See Figure 14	

## ON CHARACTERISTICS (1)

DC Current Gain (I <sub>C</sub> = 15 Adc, V <sub>CE</sub> = 5.0 V)	h <sub>FE</sub>	75	—	1000	—
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 30 Adc, I <sub>B</sub> = 1.2 Adc) (I <sub>C</sub> = 60 Adc, I <sub>B</sub> = 4.0 Adc) (I <sub>C</sub> = 30 Adc, I <sub>B</sub> = 1.2 Adc, T <sub>C</sub> = 100°C)	V <sub>CE(sat)</sub>	— — —	— — —	2.2 4.0 2.4	Vdc
Base–Emitter Saturation Voltage (I <sub>C</sub> = 30 Adc, I <sub>B</sub> = 1.2 Adc) (I <sub>C</sub> = 30 Adc, I <sub>B</sub> = 1.2 Adc, T <sub>C</sub> = 100°C)	V <sub>BE(sat)</sub>	— —	— —	3.0 3.5	Vdc
Diode Forward Voltage (I <sub>F</sub> = 30 Adc)	V <sub>f</sub>	—	2.5	5.0	Vdc

## DYNAMIC CHARACTERISTICS

Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f <sub>test</sub> = 1.0 kHz)	C <sub>ob</sub>	175	—	700	pF
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## SWITCHING CHARACTERISTICS

Resistive Load (Table 1)						
Delay Time	(V <sub>CC</sub> = 175 Vdc, I <sub>C</sub> = 30 A, I <sub>B1</sub> = Adc, V <sub>BE(off)</sub> = 5.0 V, t <sub>p</sub> = 25 μs Duty Cycle ≤ 2.0%).	t <sub>d</sub>	—	0.02	0.2	μs
Rise Time		t <sub>r</sub>	—	0.30	1.0	μs
Storage Time		t <sub>s</sub>	—	1.0	3.5	μs
Fall Time		t <sub>f</sub>	—	0.07	0.5	μs
Inductive Load, Clamped (Table 1)						
Storage Time	I <sub>CM</sub> = 30 A(pk), V <sub>CEM</sub> = 200 V, I <sub>B1</sub> = 1.2 A, V <sub>BE(off)</sub> = 5 V, T <sub>C</sub> = 100°C	t <sub>sv</sub>	—	1.2	3.5	μs
Crossover Time		t <sub>c</sub>	—	0.45	2.0	μs
Storage Time	(I <sub>CM</sub> = 30 A(pk), V <sub>CEM</sub> = 200 V, I <sub>B1</sub> = 1.2 A, V <sub>BE(off)</sub> = 5 V, T <sub>C</sub> = 25°C)	t <sub>sv</sub>	—	0.75	—	μs
Crossover Time		t <sub>c</sub>	—	0.25	—	μs
Fall Time		t <sub>fi</sub>	—	0.15	—	μs

(1) Pulse Test: PW = 300 μs, Duty Cycle ≤ 2%.

TYPICAL ELECTRICAL CHARACTERISTICS

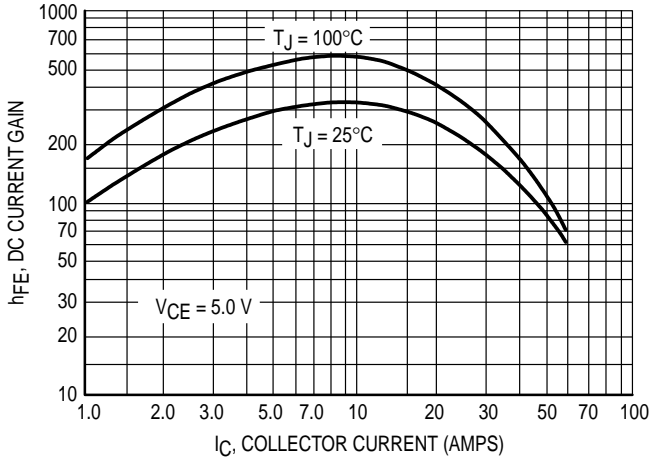


Figure 1. DC Current Gain

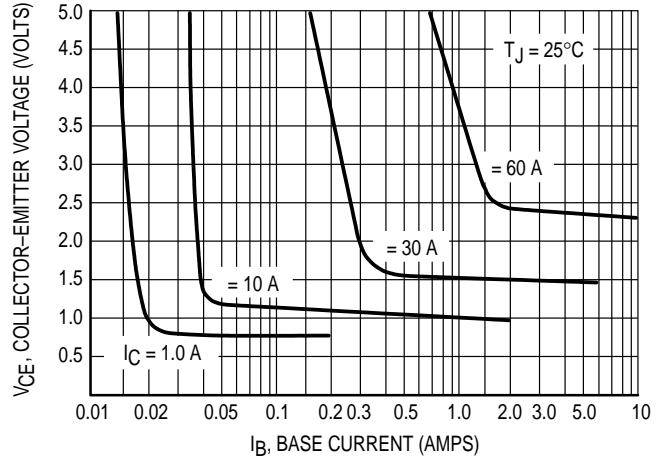


Figure 2. Collector Saturation Region

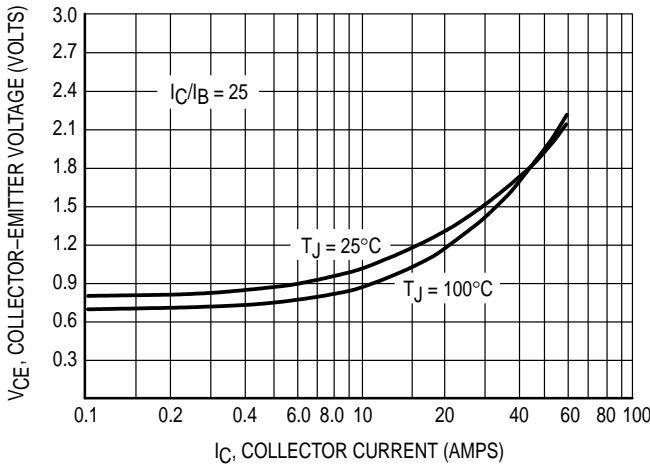


Figure 3. Collector-Emitter Saturation Voltage

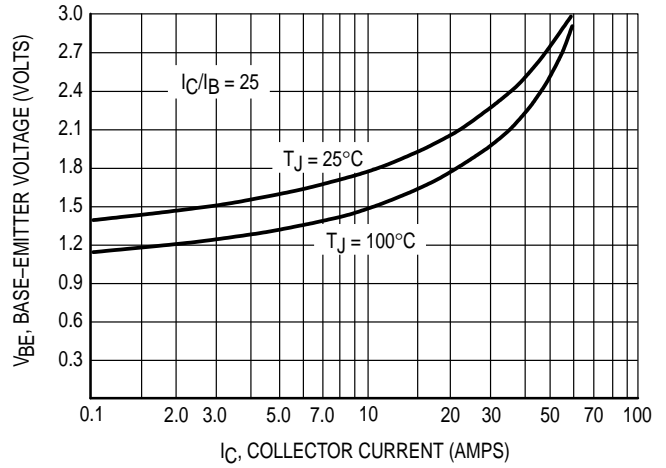


Figure 4. Base-Emitter Voltage

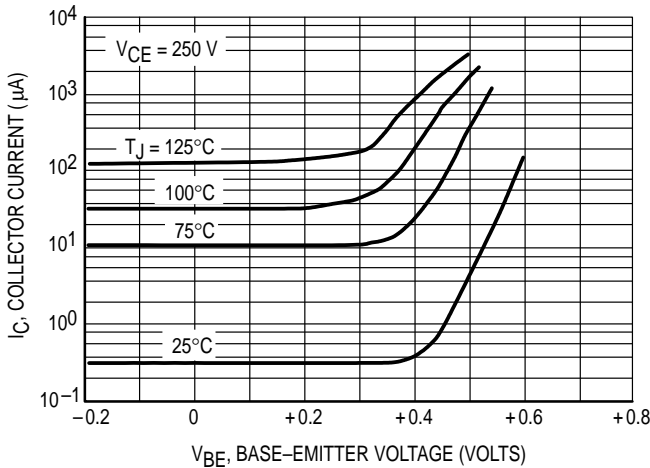


Figure 5. Collector Cutoff Region

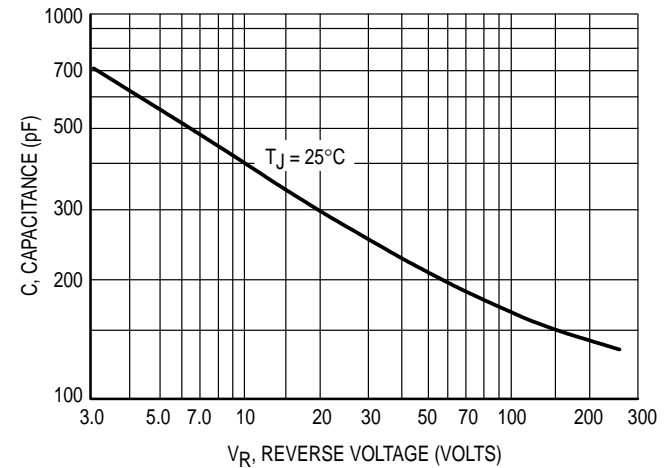
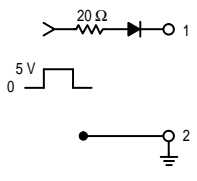
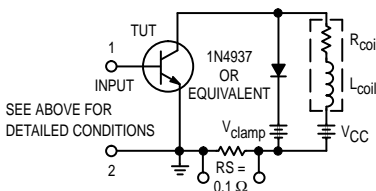
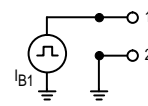
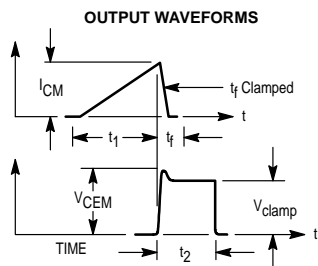
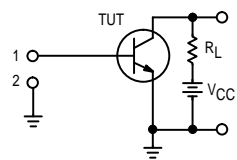


Figure 6. Output Capacitance

Table 1. Test Conditions for Dynamic Performance

	V <sub>CEO(sus)</sub>	RBSOA AND INDUCTIVE SWITCHING	RESISTIVE SWITCHING
INPUT CONDITIONS	 <p>PW Varied to Attain I<sub>C</sub> = 100 mA</p>	<p>INDUCTIVE TEST CIRCUIT</p>  <p>SEE ABOVE FOR DETAILED CONDITIONS</p>	<p>TURN-ON TIME</p>  <p>IB1 adjusted to obtain the forced h<sub>FE</sub> desired</p> <p>TURN-OFF TIME</p> <p>Use inductive switching driver as the input to the resistive test circuit.</p>
CIRCUIT VALUES	<p>L<sub>coil</sub> = 10 mH, V<sub>CC</sub> = 10 V                      R<sub>coil</sub> = 0.7 Ω                      V<sub>clamp</sub> = V<sub>CEO(sus)</sub></p>	<p>L<sub>coil</sub> = 180 μH                      R<sub>coil</sub> = 0.05 Ω                      V<sub>CC</sub> = 20 V</p>	<p>V<sub>CC</sub> = 175 V                      R<sub>L</sub> = 5.6 Ω                      Pulse Width = 25 μs</p>
TEST CIRCUITS	<p>OUTPUT WAVEFORMS</p>  <p>t<sub>1</sub> Adjusted to Obtain I<sub>C</sub></p> $t_1 \approx \frac{L_{coil} (I_{CM})}{V_{CC}}$ $t_2 \approx \frac{L_{coil} (I_{CM})}{V_{Clamp}}$ <p>Test Equipment Scope — Tektronix 475 or Equivalent</p>	<p>RESISTIVE TEST CIRCUIT</p> 	

\* Adjust -V such that V<sub>BE(off)</sub> = 5 V except as required for RBSOA (Figure 14).

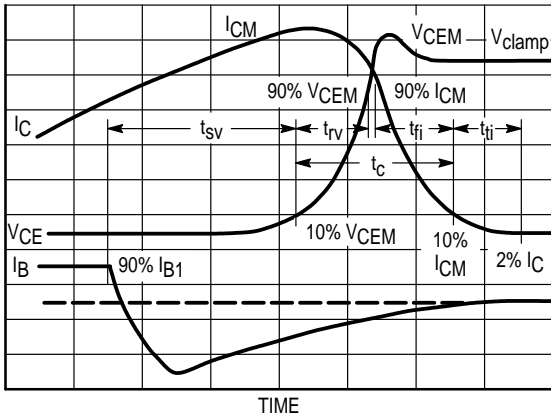


Figure 7. Inductive Switching Measurements

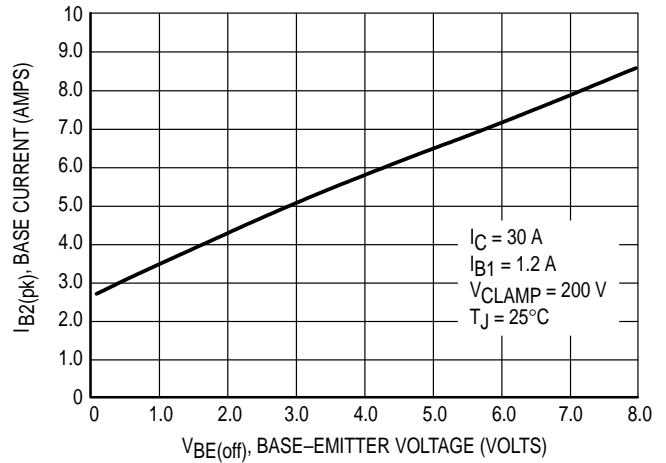


Figure 8. Typical Peak Reverse Base Current

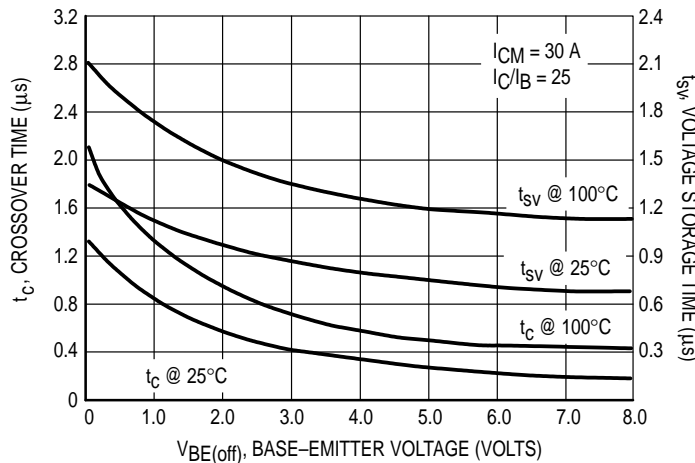


Figure 9. Typical Inductive Switching Times

SWITCHING TIMES NOTE

In resistive switching circuits, rise, fall, and storage times have been defined and apply to both current and voltage waveforms since they are in phase. However, for inductive loads which are common to SWITCHMODE power supplies and hammer drivers, current and voltage waveforms are not in phase. Therefore, separate measurements must be made on each waveform to determine the total switching time. For this reason, the following new terms have been defined.

- $t_{SV}$  = Voltage Storage Time, 90%  $I_{B1}$  to 10%  $V_{CEM}$
- $t_{RV}$  = Voltage Rise Time, 10–90%  $V_{CEM}$
- $t_{fi}$  = Current Fall Time, 90–10%  $I_{CM}$
- $t_{ti}$  = Current Tail, 10–2%  $I_{CM}$
- $t_C$  = Crossover Time, 10%  $V_{CEM}$  to 10%  $I_{CM}$

An enlarged portion of the inductive switching waveforms is

shown in Figure 7 to aid in the visual identity of these terms.

For the designer, there is minimal switching loss during storage time and the predominant switching power losses occur during the crossover interval and can be obtained using the standard equation from AN-222A:

$$P_{SWT} = 1/2 V_{CC} I_C (t_C) f$$

In general,  $t_{RV} + t_{fi} \approx t_C$ . However, at lower test currents this relationship may not be valid.

As is common with most switching transistors, resistive switching is specified at 25°C and has become a benchmark for designers. However, for designers of high frequency converter circuits, the user oriented specifications which make this a "SWITCHMODE" transistor are the inductive switching speeds ( $t_C$  and  $t_{SV}$ ) which are guaranteed at 100°C.

RESISTIVE SWITCHING

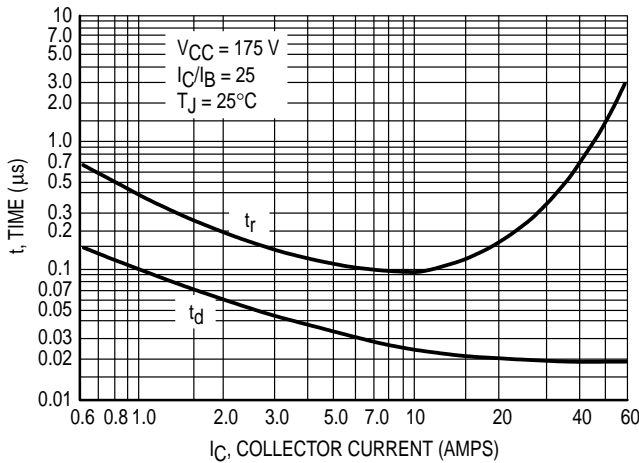


Figure 10. Typical Turn-On Switching Times

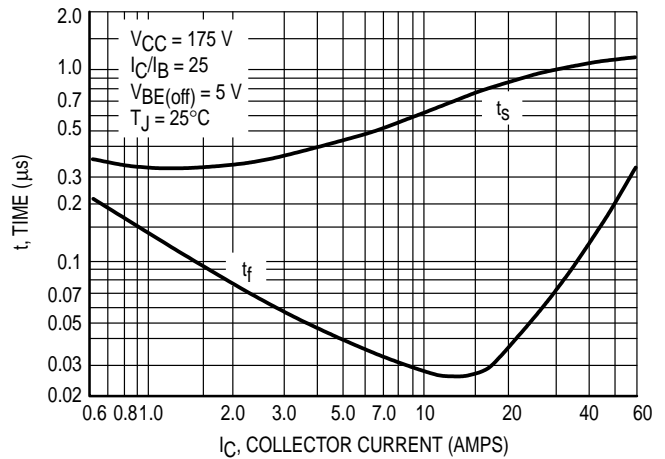


Figure 11. Typical Turn-Off Switching Times

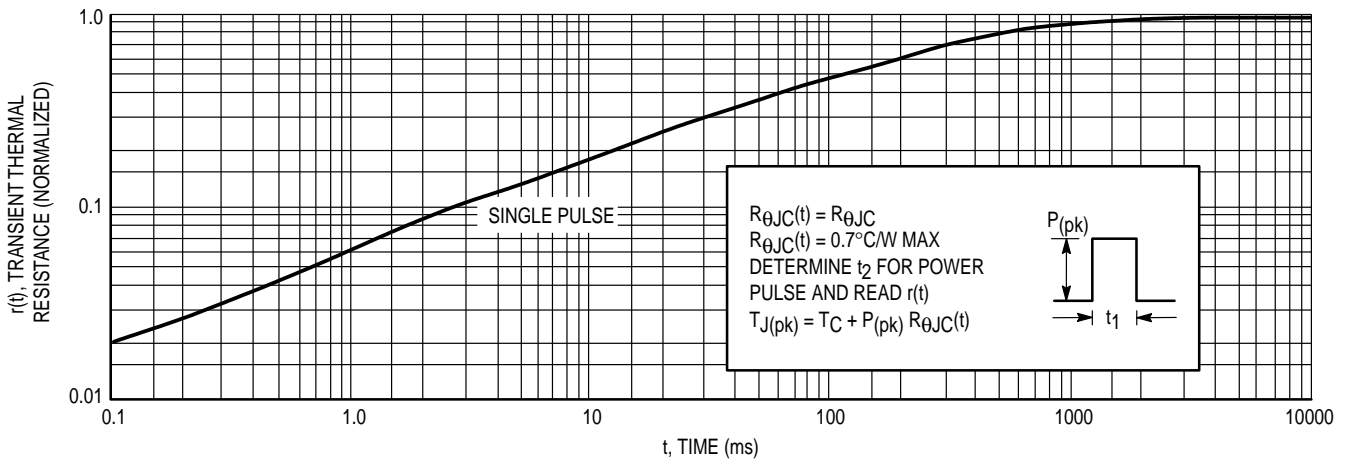
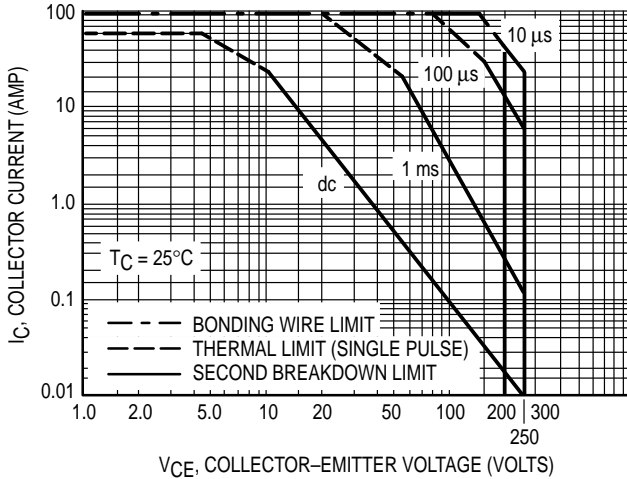


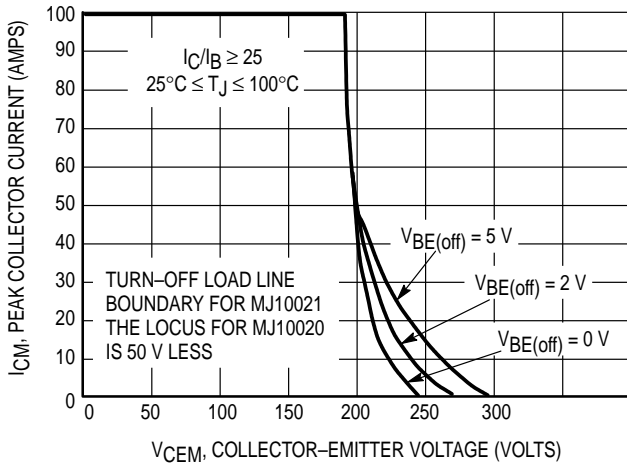
Figure 12. Thermal Response

## MJ10020 MJ10021

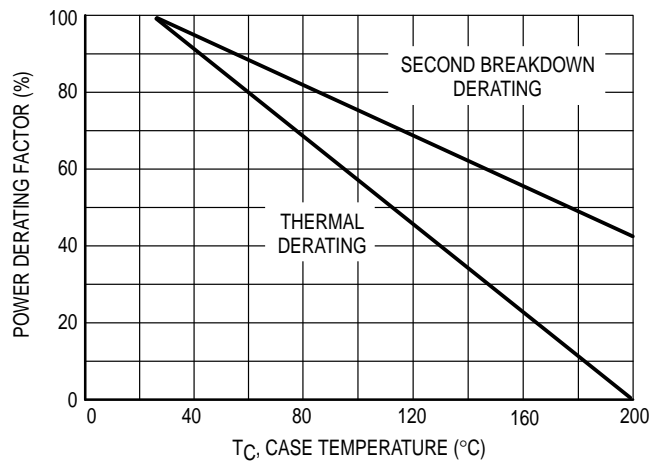
The Safe Operating Area figures shown in Figures 13 and are specified for these devices under the test conditions shown.



**Figure 13. Maximum Forward Bias Safe Operating Area**



**Figure 14. Maximum RBSOA, Reverse Bias Safe Operating Area**



**Figure 15. Power Derating**

## SAFE OPERATING AREA INFORMATION

### FORWARD BIAS

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation, i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

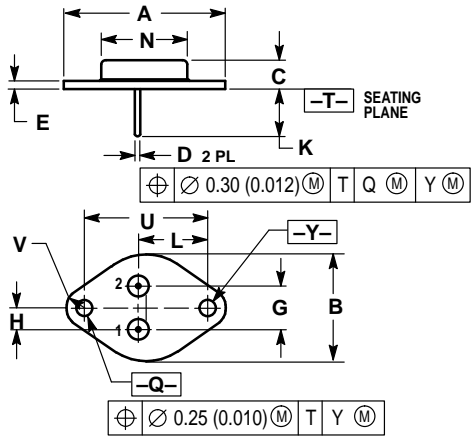
The data of Figure 13 is based on  $T_C = 25^\circ\text{C}$ ;  $T_{J(pk)}$  is variable depending on power level. Second breakdown pulse limits are valid for duty cycles to 10% but must be derated when  $T_C \geq 25^\circ\text{C}$ . Second breakdown limitations do not derate the same as thermal limitations. Allowable current at the voltages shown on Figure 13 may be found at any case temperature by using the appropriate curve on Figure 15.

$T_{J(pk)}$  may be calculated from the data in Figure 12. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

### REVERSE BIAS

For Inductive loads, high voltage and high current must be sustained simultaneously during turn-off, in most cases, with the base to emitter junction reverse biased. Under these conditions the collector voltage must be held to a safe level at or below a specific value of collector current. This can be accomplished by several means such as active clamping, RC snubbing, load line shaping, etc. The safe level for these devices is specified as Reverse Bias Safe Operating Area and represents the voltage-current condition allowable during reverse biased turn-off. This rating is verified under clamped conditions so that the device is never subjected to an avalanche mode. Figure 14 gives the RBSOA characteristics.

PACKAGE DIMENSIONS




NOTES:  
 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.  
 2. CONTROLLING DIMENSION: INCH.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	1.530 REF		38.86 REF	
B	0.990	1.050	25.15	26.67
C	0.250	0.335	6.35	8.51
D	0.057	0.063	1.45	1.60
E	0.060	0.070	1.53	1.77
G	0.430 BSC		10.92 BSC	
H	0.215 BSC		5.46 BSC	
K	0.440	0.480	11.18	12.19
L	0.665 BSC		16.89 BSC	
N	0.760	0.830	19.31	21.08
Q	0.151	0.165	3.84	4.19
U	1.187 BSC		30.15 BSC	
V	0.131	0.188	3.33	4.77

STYLE 1:  
 PIN 1: BASE  
 2: EMITTER  
 CASE: COLLECTOR

CASE 197A-05  
 TO-204AE (TO-3)  
 ISSUE J

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P.O. Box 20912; Phoenix, Arizona 85036. 1-800-441-2447

**JAPAN:** Nippon Motorola Ltd.; Tatsumi-SPD-JLDC, Toshikatsu Otsuki,  
6F Seibu-Butsuryu-Center, 3-14-2 Tatsumi Koto-Ku, Tokyo 135, Japan. 03-3521-8315

**MFAX:** RMFAX0@email.sps.mot.com - TOUCHTONE (602) 244-6609  
**INTERNET:** <http://Design-NET.com>

**HONG KONG:** Motorola Semiconductors H.K. Ltd.; 8B Tai Ping Industrial Park,  
51 Ting Kok Road, Tai Po, N.T., Hong Kong. 852-26629298

