19-1387; Rev 0; 11/98

MAXIM

+2.7V, Low-Power, 2-Channel, 108ksps, Serial 12-Bit ADCs in 8-Pin µMAX

General Description

The MAX144/MAX145 low-power, 12-bit analog-to-digital converters (ADCs) are available in 8-pin µMAX and DIP packages. Both devices operate with a single +2.7V to +5.25V supply and feature a 7.4µs successive-approximation ADC, automatic power-down, fast wake-up (2.5µs), an on-chip clock, and a high-speed, 3-wire serial interface.

Power consumption is only 3.2mW (V_{DD} = +3.6V) at the maximum sampling rate of 108ksps. At slower throughput rates, the automatic shutdown (0.2µA) further reduces power consumption.

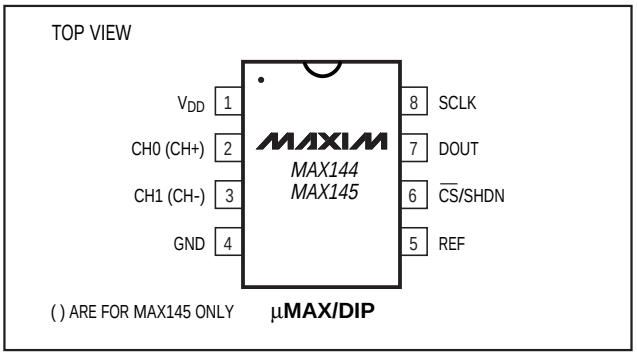
The MAX144 provides 2-channel, single-ended operation and accepts input signals from 0 to V_{REF}. The MAX145 accepts pseudo-differential inputs ranging from 0 to V_{REF}. An external clock accesses data through the 3-wire serial interface, which is SPI™, QSPI™, and MICROWIRE™-compatible.

Excellent dynamic performance and low power, combined with ease of use and small package size, make these converters ideal for battery-powered and data-acquisition applications, or for other circuits with demanding power-consumption and space requirements. For pin-compatible 10-bit ADCs, see the MAX157 and MAX159.

Applications

Battery-Powered Systems
Portable Data Logging
Isolated Data Acquisition
Process-Control Monitoring
Instrumentation
Test Equipment
Medical Instruments
System Supervision

Pin Configuration



SPI and QSPI are trademarks of Motorola, Inc.
MICROWIRE is a trademark of National Semiconductor Corp.

Features

- ♦ **Single-Supply Operation (+2.7V to +5.25V)**
- ♦ **Two Single-Ended Channels (MAX144)**
  One Pseudo-Differential Channel (MAX145)
- ♦ **Low Power**
  0.9mA (108ksps, +3V Supply)
  100µA (10ksps, +3V Supply)
  10µA (1ksps, +3V Supply)
  0.2µA (Power-Down Mode)
- ♦ **Internal Track/Hold**
- ♦ **108ksps Sampling Rate**
- ♦ **SPI/QSPI/MICROWIRE-Compatible 3-Wire Serial Interface**
- ♦ **Space-Saving 8-Pin µMAX Package**
- ♦ **Pin-Compatible 10-Bit Versions Available**

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE	INL (LSB)
MAX144ACUA	0°C to +70°C	8 µMAX	±0.5
MAX144BCUA	0°C to +70°C	8 µMAX	±1
MAX144ACPA	0°C to +70°C	8 Plastic DIP	±0.5
MAX144BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX144BC/D	0°C to +70°C	Dice*	±1
MAX144AEUA	-40°C to +85°C	8 µMAX	±0.5
MAX144BEUA	-40°C to +85°C	8 µMAX	±1
MAX144AEPA	-40°C to +85°C	8 Plastic DIP	±0.5
MAX144BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX144AMJA	-55°C to +125°C	8 CERDIP**	±0.5
MAX144BMJA	-55°C to +125°C	8 CERDIP**	±1
MAX145ACUA	0°C to +70°C	8 µMAX	±0.5
MAX145BCUA	0°C to +70°C	8 µMAX	±1
MAX145ACPA	0°C to +70°C	8 Plastic DIP	±0.5
MAX145BCPA	0°C to +70°C	8 Plastic DIP	±1
MAX145BC/D	0°C to +70°C	Dice*	±1
MAX145AEUA	-40°C to +85°C	8 µMAX	±0.5
MAX145BEUA	-40°C to +85°C	8 µMAX	±1
MAX145AEPA	-40°C to +85°C	8 Plastic DIP	±0.5
MAX145BEPA	-40°C to +85°C	8 Plastic DIP	±1
MAX145AMJA	-55°C to +125°C	8 CERDIP**	±0.5
MAX145BMJA	-55°C to +125°C	8 CERDIP**	±1

**Dice are specified at T_A = +25°C, DC parameters only.*
***Contact factory for availability.*

+2.7V, Low-Power, 2-Channel, 108ksps, Serial 12-Bit ADCs in 8-Pin µMAX

ABSOLUTE MAXIMUM RATINGS

V_{DD} to GND .....-0.3V to +6V
CH0, CH1 (CH+, CH-) to GND ..... -0.3V to (V_{DD} + 0.3V)
REF to GND ..... -0.3V to (V_{DD} + 0.3V)
Digital Inputs to GND. ..... -0.3V to +6V
DOUT to GND..... -0.3V to (V_{DD} + 0.3V)
DOUT Sink Current 25mA
Continuous Power Dissipation (T_A = +70°C)
µMAX (derate 4.1mW/°C above +70°C) 330mW
Plastic DIP (derate 9.09mW/°C above +70°C) 727mW
CERDIP (derate 8.00mW/°C above +70°C) 640mW
Operating Temperature Ranges (T_A)
MAX144/MAX145_C_A .....0°C to +70°C
MAX144/MAX145_E_A. .....-40°C to +85°C
MAX144/MAX145_M_A ..... -55°C to +125°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10sec) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{DD} = +2.7V to +5.25V, V_{REF} = 2.5V, 0.1µF capacitor at REF, f_{SCLK} = 2.17MHz, 16 clocks/conversion cycle (108ksps), CH- = GND for MAX145, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DC ACCURACY (Note 1)						
Resolution	RES		12			Bits
Relative Accuracy (Note 2)	INL	MAX14_A			±0.5	LSB
		MAX14_B			±1	
Differential Nonlinearity	DNL	No missing codes over temperature			±0.75	LSB
Offset Error					±3	LSB
Gain Error (Note 3)					±3	LSB
Gain Temperature Coefficient				±0.8		ppm/°C
Channel-to-Channel Offset Matching				±0.05		LSB
Channel-to-Channel Gain Matching				±0.05		LSB
DYNAMIC SPECIFICATIONS ($f_{IN(sine-wave)}$ = 10kHz, V_{IN} = 2.5Vp-p, 108ksps, f_{SCLK} = 2.17MHz, CH- = GND for MAX145)						
Signal-to-Noise Plus Distortion Ratio	SINAD		70			dB
Total Harmonic Distortion (including 5th-order harmonic)	THD				-80	dB
Spurious-Free Dynamic Range	SFDR		80			dB
Channel-to-Channel Crosstalk		f_{IN} = 65kHz, V_{IN} = 2.5Vp-p (Note 4)		-85		dB
Small-Signal Bandwidth		-3dB rolloff		2.25		MHz
Full-Power Bandwidth				1.0		MHz
CONVERSION RATE						
Conversion Time (Note 5)	t_{CONV}	External clock, f_{SCLK} = 2.17MHz, 16 clocks/conversion cycle	7.4			µs
		Internal clock	5		7	
T/H Acquisition Time	t_{ACQ}				2.5	µs
Aperture Delay				25		ns
Aperture Jitter				<50		ps
Serial Clock Frequency	f_{SCLK}	External clock mode	0.1		2.17	MHz
		Internal clock mode, for data transfer only	0		5	

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = +2.7V to +5.25V, V_{REF} = 2.5V, 0.1µF capacitor at REF, f_{SCLK} = 2.17MHz, 16 clocks/conversion cycle (108ksps), CH- = GND for MAX145, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ANALOG INPUTS						
Analog Input Voltage Range (Note 6)	V_{IN}		0		V_{REF}	V
Multiplexer Leakage Current		On/off leakage current, V_{IN} = 0 to V_{DD}		±0.01	±1	µA
Input Capacitance	C_{IN}			16		pF
EXTERNAL REFERENCE						
Input Voltage Range (Note 7)	V_{REF}		0		V_{DD} + 50mV	V
Input Current		V_{REF} = 2.5V		100	140	µA
Input Resistance			18	25		kΩ
Shutdown REF Input Current				0.01	10	µA
DIGITAL INPUTS ($\overline{CS}$/SHDN) AND OUTPUT (DOUT)						
Input High Voltage	V_{IH}	$V_{DD} \le 3.6V$	2.0			V
		$V_{DD} > 3.6V$	3.0			
Input Low Voltage	V_{IL}				0.8	V
Input Hysteresis	V_{HYS}			0.2		V
Input Leakage Current	I_{IN}	V_{IN} = 0 or V_{DD}			±1	µA
Input Capacitance	C_{IN}	(Note 8)			15	pF
Output Low Voltage	V_{OL}	I_{SINK} = 5mA			0.4	V
		I_{SINK} = 16mA		0.5		
Output High Voltage	V_{OH}	I_{SOURCE} = 0.5mA	V_{DD} - 0.5			V
Three-State Output Leakage Current		$\overline{CS}$/SHDN = V_{DD}			±10	µA
Three-State Output Capacitance	C_{OUT}	$\overline{CS}$/SHDN = V_{DD} (Note 8)			15	pF
POWER REQUIREMENTS						
Positive Supply Voltage	V_{DD}		2.7		5.25	V
Positive Supply Current	I_{DD}	Operating mode		0.9	2.0	mA
		Shutdown, $\overline{CS}$/SHDN = GND		0.2	5	µA
Power-Supply Rejection (Note 9)	PSR	V_{DD} = 2.7V to 5.25V, V_{REF} = 2.5V, full-scale input		±0.15		mV

TIMING CHARACTERISTICS (Figure 7)

(V_{DD} = +2.7V to +5.25V, V_{REF} = 2.5V, 0.1µF capacitor at REF, f_{SCLK} = 2.17MHz, 16 clocks/conversion cycle (108ksps), CH- = GND for MAX145, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.)

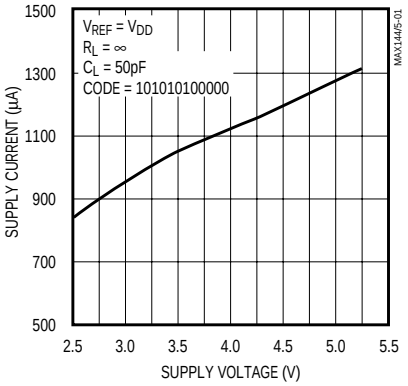
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Wake-Up Time (Note 10)	t_{WAKE}		2.5			µs
$\overline{CS}$/SHDN Fall to Output Enable	t_{DV}	C_L = 100pF			120	ns
$\overline{CS}$/SHDN Rise to Output Disable	t_{TR}	C_L = 100pF, Figure 1			120	ns
SCLK Fall to Output Data Valid	t_{DO}	C_L = 100pF, Figure 1	20		120	ns
SCLK Clock Frequency	f_{SCLK}	External clock	0.1		2.17	MHz
		Internal clock, SCLK for data transfer only	0		5	
SCLK Pulse Width High	t_{CH}	External clock	215			ns
		Internal clock, SCLK for data transfer only (Note 8)	50			
SCLK Pulse Width Low	t_{CL}	External clock	215			ns
		Internal clock, SCLK for data transfer only (Note 8)	50			
SCLK to $\overline{CS}$/SHDN Setup	t_{SCLKS}		60			ns
$\overline{CS}$/SHDN Pulse Width	t_{CS}		60			ns

Note 1: Tested at V_{DD} = +2.7V.
Note 2: Relative accuracy is the deviation of the analog value at any code from its theoretical value after full-scale range has been calibrated.
Note 3: Offset nulled.
Note 4: "On" channel is grounded; sine wave applied to "off" channel (MAX144 only).
Note 5: Conversion time is defined as the number of clock cycles times the clock period; clock has 50% duty cycle.
Note 6: The common-mode range for the analog inputs is from GND to V_{DD} (MAX145 only).
Note 7: ADC performance is limited by the converter's noise floor, typically 300µVp-p.
Note 8: Guaranteed by design. Not subject to production testing.
Note 9: Measured as $V_{FS(2.7V)}$ - $V_{FS(5.25V)}$.
Note 10: SCLK must remain stable during this time.

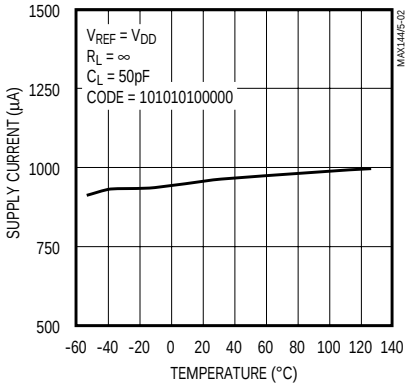
Typical Operating Characteristics

(V_{DD} = +3.0V, V_{REF} = 2.5V, 0.1µF at REF, f_{SCLK} = 2.17MHz, 16 clocks/conversion cycle (108ksps), CH- = GND for MAX145, T_A = +25°C, unless otherwise noted.)

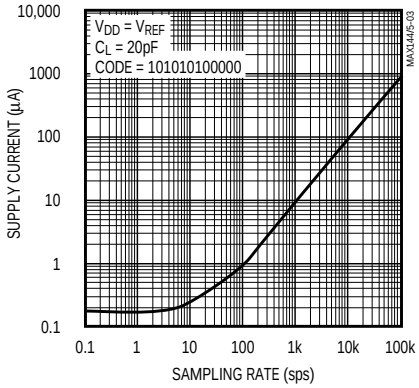
SUPPLY CURRENT vs. SUPPLY VOLTAGE



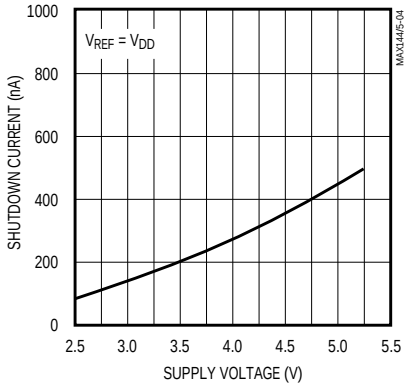
SUPPLY CURRENT vs. TEMPERATURE



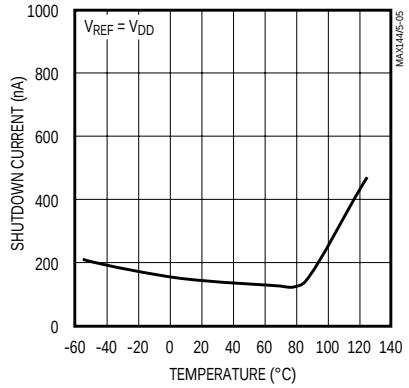
SUPPLY CURRENT vs. SAMPLING RATE



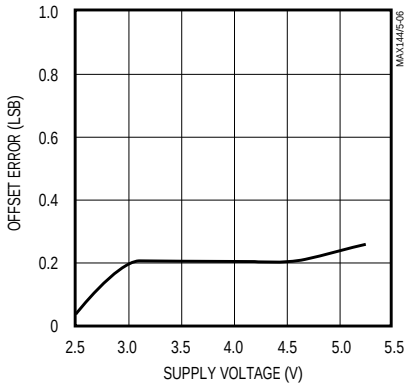
SHUTDOWN CURRENT vs. SUPPLY VOLTAGE



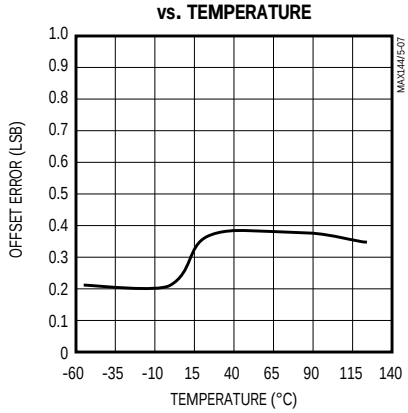
SHUTDOWN CURRENT vs. TEMPERATURE



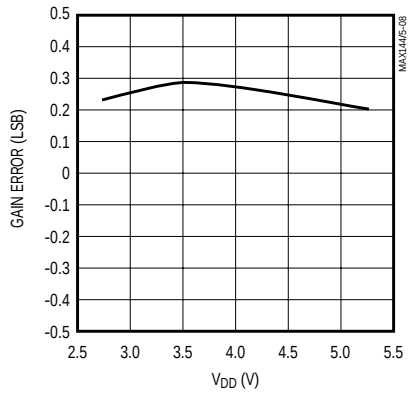
OFFSET ERROR vs. SUPPLY VOLTAGE



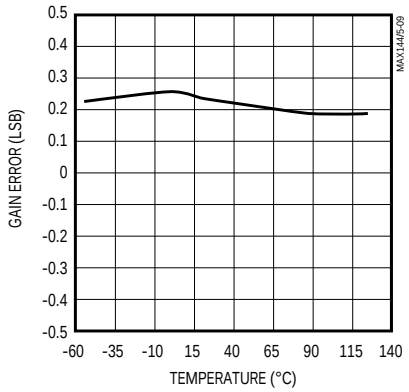
OFFSET ERROR vs. TEMPERATURE



GAIN ERROR vs. SUPPLY VOLTAGE



GAIN ERROR vs. TEMPERATURE

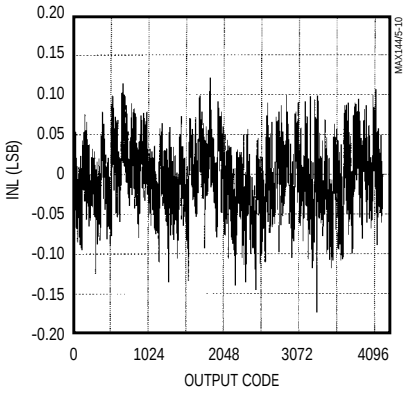


+2.7V, Low-Power, 2-Channel, 108ksps, Serial 12-Bit ADCs in 8-Pin µMAX

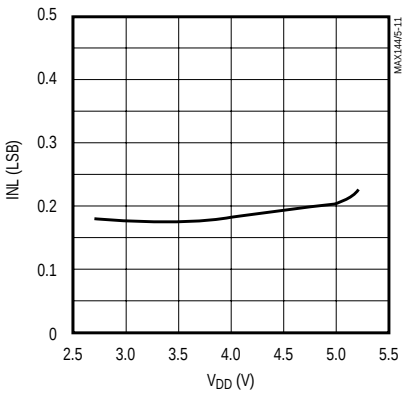
Typical Operating Characteristics (continued)

(V_{DD} = +3.0V, V_{REF} = 2.5V, 0.1µF at REF, f_{SCLK} = 2.17MHz, 16 clocks/conversion cycle (108ksps), CH- = GND for MAX145, T_A = +25°C, unless otherwise noted.)

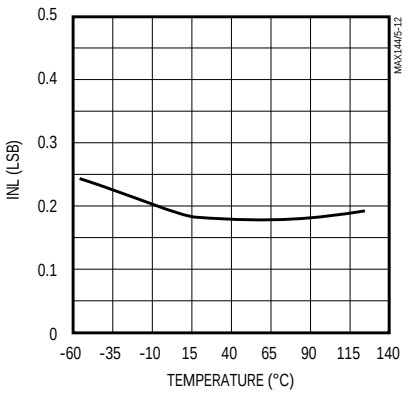
INTEGRAL NONLINEARITY vs. OUTPUT CODE



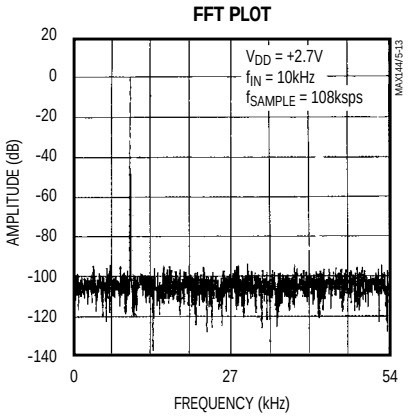
INTEGRAL NONLINEARITY vs. SUPPLY VOLTAGE



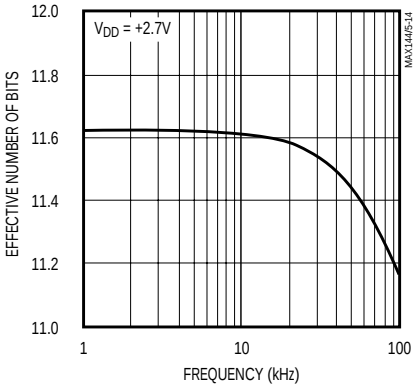
INTEGRAL NONLINEARITY vs. TEMPERATURE



FFT PLOT



EFFECTIVE NUMBER OF BITS vs. FREQUENCY



Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	Positive Supply Voltage, +2.7V to +5.25V
2	CH0 (CH+)	Analog Input: MAX144 = single-ended (CH0); MAX145 = differential (CH+)
3	CH1 (CH-)	Analog Input: MAX144 = single-ended (CH1); MAX145 = differential (CH-)
4	GND	Analog and Digital Ground
5	REF	External Reference Voltage Input. Sets the analog voltage range. Bypass with a 100nF capacitor close to the device.
6	$\overline{CS}$/SHDN	Active-Low Chip-Select Input/Active-High Shutdown Input. Pulling $\overline{CS}$/SHDN high puts the device into shutdown with a maximum current of 5µA.
7	DOUT	Serial Data Output. Data changes state at SCLK's falling edge. High impedance when $\overline{CS}$/SHDN is high.
8	SCLK	Serial Clock Input. DOUT changes on the falling edge of SCLK.

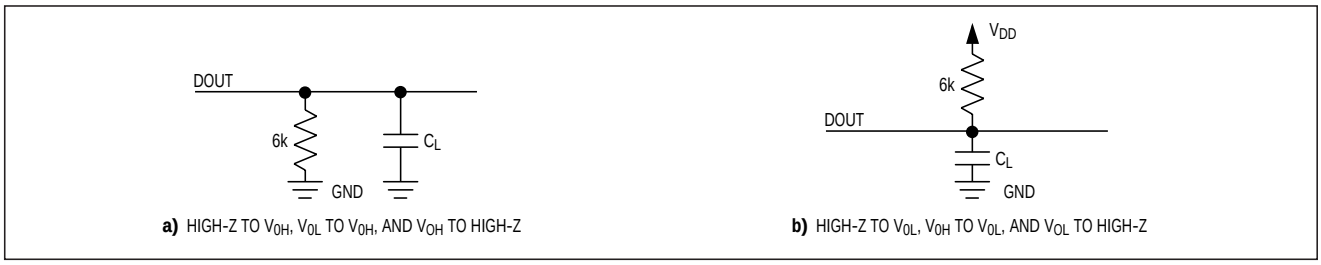


Figure 1. Load Circuits for Enable and Disable Time

Detailed Description

The MAX144/MAX145 analog-to-digital converters (ADCs) use a successive-approximation conversion (SAR) technique and on-chip track-and-hold (T/H) structure to convert an analog signal to a serial 12-bit digital output data stream.

This flexible serial interface provides easy interface to microprocessors (µPs). Figure 2 shows a simplified functional diagram of the internal architecture for both the MAX144 (2 channels, single-ended) and the MAX145 (1 channel, pseudo-differential).

Analog Inputs: Single-Ended (MAX144) and Pseudo-Differential (MAX145)

The sampling architecture of the ADC's analog comparator is illustrated in the equivalent input circuit of Figure 3. In single-ended mode (MAX144), both channels CH0 and CH1 are referred to GND and can be connected to two different signal sources. Following the power-on reset, the ADC is set to convert CH0. After CH0 has been converted, CH1 will be converted and the conversions will continue to alternate between channels. Channel switching is performed by toggling the $\overline{CS}$/SHDN pin. Conversions can be performed on the same channel by toggling $\overline{CS}$/SHDN twice between conversions. If only one channel is required, CH0 and CH1 may be connected together; however, the output data will still contain the channel identification bit (before the MSB).

For the MAX145, the input channels form a single differential channel pair (CH+, CH-). This configuration is pseudo-differential to the effect that only the signal at IN+ is sampled. The return side IN- must remain stable within ±0.5LSB (±0.1LSB for optimum results) with respect to GND during a conversion. To accomplish this, connect a 0.1µF capacitor from IN- to GND.

During the acquisition interval, the channel selected as the positive input (IN+) charges capacitor C_{HOLD}. The acquisition interval spans from when $\overline{CS}$/SHDN falls to the falling edge of the second clock cycle (external clock mode) or from when $\overline{CS}$/SHDN falls to the first falling edge of SCLK (internal clock mode). At the end of the acquisition interval, the T/H switch opens, retaining charge on C_{HOLD} as a sample of the signal at IN+.

The conversion interval begins with the input multiplexer switching C_{HOLD} from the positive input (IN+) to the negative input (IN-). This unbalances node ZERO at the comparator's positive input.

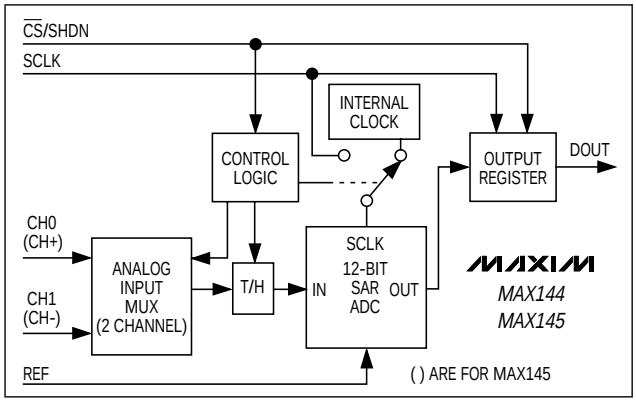


Figure 2. Simplified Functional Diagram

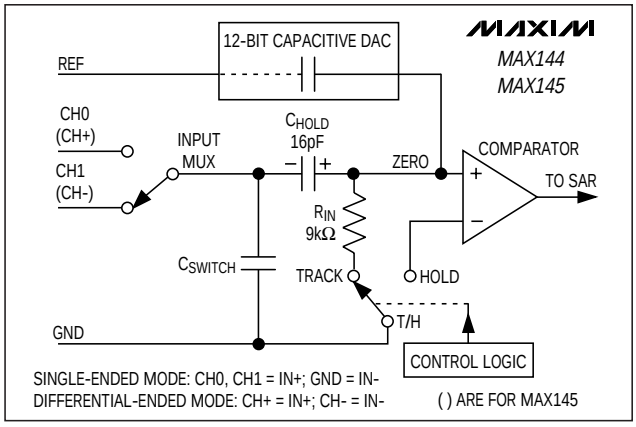


Figure 3. Analog Input Channel Structure

+2.7V, Low-Power, 2-Channel, 108ksps, Serial 12-Bit ADCs in 8-Pin µMAX

The capacitive digital-to-analog converter (DAC) adjusts during the remainder of the conversion cycle to restore node ZERO to 0V within the limits of 12-bit resolution. This action is equivalent to transferring a 16pF · [(V_{IN+}) - (V_{IN-})] charge from C_{HOLD} to the binary-weighted capacitive DAC, which in turn forms a digital representation of the analog input signal.

Track/Hold (T/H)

The ADC's T/H stage enters its tracking mode on the falling edge of $\overline{CS}$/SHDN. For the MAX144 (single-ended inputs), IN- is connected to GND and the converter samples the positive ("+") input. For the MAX145 (pseudo-differential inputs), IN- connects to the negative input ("-") and the difference of [(V_{IN+}) - (V_{IN-})] is sampled. At the end of the conversion, the positive input connects back to IN+ and C_{HOLD} charges to the input signal.

The time required for the T/H stage to acquire an input signal is a function of how fast its input capacitance is charged. If the input signal's source impedance is high, the acquisition time lengthens, and more time must be allowed between conversions. The acquisition time, t_{ACQ}, is the maximum time the device takes to acquire the signal, and is also the minimum time required for the signal to be acquired. Calculate this with the following equation:

$$t_{ACQ} = 9(R_S + R_{IN})C_{IN}$$

where R_S is the source impedance of the input signal, R_{IN} (9kΩ) is the input resistance, and C_{IN} (16pF) is the input capacitance of the ADC. Source impedances below 1kΩ have no significant impact on the AC performance of the MAX144/MAX145.

Higher source impedances can be used if a 0.01µF capacitor is connected to the individual analog inputs. Together with the input impedance, this capacitor forms an RC filter, limiting the ADC's signal bandwidth.

Input Bandwidth

The MAX144/MAX145 T/H stage offers a 2.25MHz small-signal and a 1MHz full-power bandwidth, which make it possible to use the parts for digitizing high-speed transients and measuring periodic signals with bandwidths exceeding the ADCs sampling rate by using undersampling techniques. To avoid high-frequency signals being aliased into the frequency band of interest, anti-alias filtering is recommended. Most aliasing problems can be fixed easily with an external resistor and a capacitor. However, if DC precision is required, it is usually best to choose a continuous or switched-capacitor filter, such as the MAX7410/MAX7414 (Figure 4). Their Butterworth characteristic generally provides the best compromise (with regard to rolloff and attenuation) in filter configurations, is easy to design, and provides a maximally flat passband response.

Analog Input Protection

Internal protection diodes, which clamp the analog input to V_{DD} and GND, allow each input channel to swing within GND - 300mV to V_{DD} + 300mV without damage. However, for accurate conversions, both inputs must not exceed V_{DD} + 50mV or be less than GND - 50mV.

If an off-channel analog input voltage exceeds the supplies, limit the input current to 4mA.

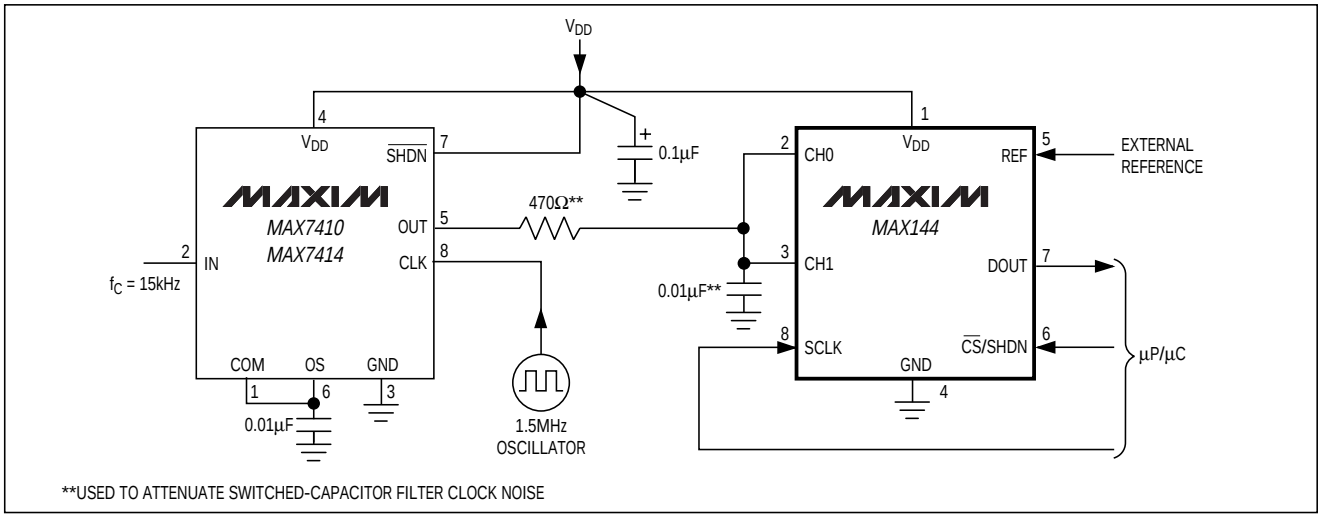


Figure 4. Analog Input with Anti-Aliasing Filter Structure

Selecting Clock Mode

To start the conversion process on the MAX144/MAX145, pull $\overline{CS}$/SHDN low. At $\overline{CS}$/SHDN's falling edge, the part wakes up and the internal T/H enters track mode. In addition, the state of SCLK at $\overline{CS}$/SHDN's falling edge selects internal (SCLK = high) or external (SCLK = low) clock mode.

Internal Clock (f_{SCLK} < 100kHz or f_{SCLK} > 2.17MHz)

In internal clock mode, the MAX144/MAX145 run from an internal, laser-trimmed oscillator to within 20% of the 2MHz specified clock rate. This releases the system microprocessor from running the SAR conversion clock and allows the conversion results to be read back at the processor's convenience, at any clock rate from 0 to 5MHz. Operating the MAX144/MAX145 in internal clock mode is necessary for serial interfaces operating with clock frequencies lower than 100kHz or greater than 2.17MHz. Select internal clock mode (Figure 5), by holding SCLK high during a high/low transition of $\overline{CS}$/SHDN. The first SCLK falling edge samples the data and initiates a conversion using the integrated on-chip oscillator. After the conversion, the oscillator shuts off and DOUT goes high, signaling the end of conversion (EOC). Data can then be read out with SCLK.

External Clock (f_{SCLK} = 100kHz to 2.17MHz)

The external clock mode (Figure 6) is selected by transitioning $\overline{CS}$/SHDN from high to low while SCLK is low. The external clock signal not only shifts data out, but also drives the analog-to-digital conversion. The input is sampled and conversion begins on the falling edge of the second clock pulse. Conversion must be completed within 140µs to prevent degradation in the conversion results caused by droop on the T/H capacitors. External clock mode provides the best throughput for clock frequencies between 100kHz and 2.17MHz.

Output Data Format

Table 1 illustrates the 16-bit, serial data stream output format for both the MAX144 and MAX145. The first three bits are always logic high (including the EOC bit for internal clock mode), followed by the channel identification (CHID = 0 for CH0, CHID = 1 for CH1, CHID = 1 for the MAX145), and then 12 bits of data in MSB-first format. After the last bit has been read out, additional SCLK pulses will clock out trailing zeros. DOUT transitions on the falling edge of SCLK. The output remains high-impedance when $\overline{CS}$/SHDN is high.

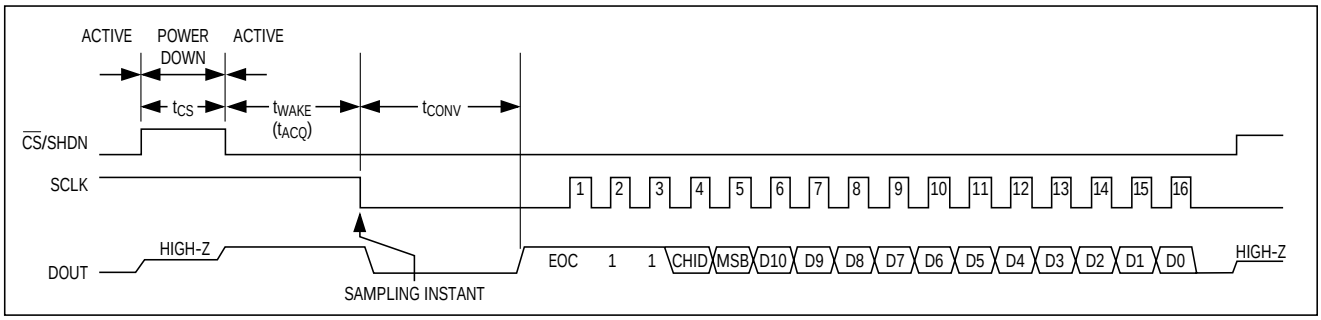


Figure 5. Internal Clock Mode Timing

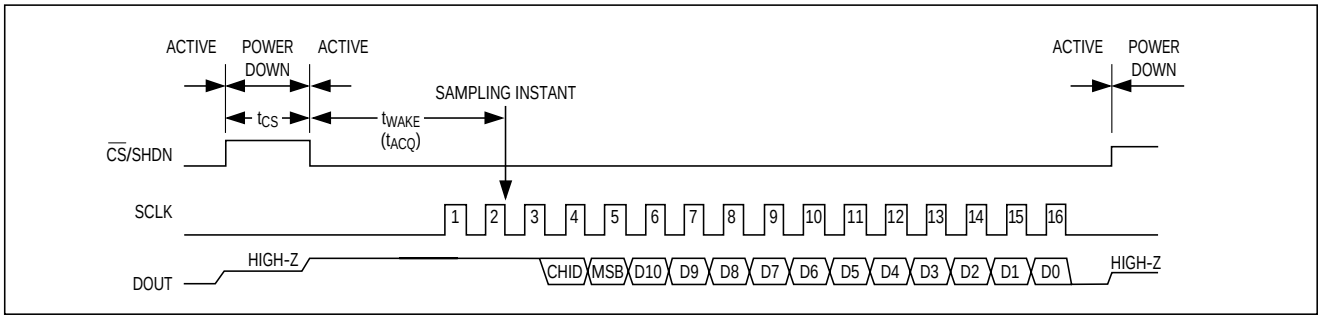


Figure 6. External Clock Mode Timing

+2.7V, Low-Power, 2-Channel, 108ksps, Serial 12-Bit ADCs in 8-Pin µMAX

Table 1. Serial Output Data Stream for Internal and External Clock Mode

SCLK CYCLE	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
DOUT (Internal Clock)	EOC	1	1	CHID	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
DOUT (External Clock)	1	1	1	CHID	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

External Reference

An external reference is required for both the MAX144 and the MAX145. At REF, the DC input resistance is a minimum of 18kΩ. During a conversion, a reference must be able to deliver 250µA of DC load current and have an output impedance of 10Ω or less. Use a 0.1µF bypass capacitor for best performance. The reference input structure allows a voltage range of 0 to V_{DD} + 50mV, although noise levels will decrease effective resolution at lower reference voltages.

Automatic Power-Down Mode

Whenever the MAX144/MAX145 are not selected ($\overline{CS}$/SHDN = V_{DD}), the parts enter their shutdown mode. In shutdown all internal circuitry turns off, reducing supply current to typically less than 0.2µA. With an external reference stable to within 1LSB, the wake-up time is 2.5µs. If the external reference is not stable within 1LSB, the wake-up time must be increased to allow the reference to stabilize.

Applications Information

Signal-to-Noise Ratio (SNR)

For a waveform perfectly reconstructed from digital samples, the theoretical maximum SNR is the ratio of full-scale analog input (RMS value) to the RMS quantization error (residual error). The ideal, theoretical minimum analog-to-digital noise is caused by quantization error only and results directly from the ADC's resolution (N bits):

$$SNR_{(MAX)} = (6.02 \cdot N + 1.76)dB$$

In reality, there are other noise sources besides quantization noise: thermal noise, reference noise, clock jitter, etc. Therefore, SNR is computed by taking the ratio of the RMS signal to the RMS noise which includes all spectral components minus the fundamental, the first five harmonics, and the DC offset.

Signal-to-Noise Plus Distortion (SINAD)

SINAD is the ratio of the fundamental input frequency's RMS amplitude to RMS equivalent of all other ADC output signals:

$$SINAD(dB) = 20 \cdot \log\left[\frac{Signal_{RMS}}{(Noise + Distortion)_{RMS}}\right]$$

Effective Number of Bits (ENOB)

ENOB indicates the global accuracy of an ADC at a specific input frequency and sampling rate. An ideal ADC's error consists only of quantization noise. With an input range equal to the full-scale range of the ADC, the effective number of bits can be calculated as follows:

$$ENOB = (SINAD - 1.76) / 6.02$$

Total Harmonic Distortion (THD)

THD is the ratio of the RMS sum of the first five harmonics of the input signal to the fundamental itself. This is expressed as:

$$THD = 20 \cdot \log\left(\frac{\sqrt{\left(V_2^2 + V_3^2 + V_4^2 + V_5^2\right)}}{V_1}\right)$$

where V_1 is the fundamental amplitude, and V_2 through V_5 are the amplitudes of the 2nd- through 5th-order harmonics.

Spurious-Free Dynamic Range (SFDR)

SFDR is the ratio of RMS amplitude of the fundamental (maximum signal component) to the RMS value of the next largest spurious component, excluding DC offset.

Connection to Standard Interfaces

The MAX144/MAX145 interface is fully compatible with SPI, QSPI, and MICROWIRE standard serial interfaces.

If a serial interface is available, establish the CPU's serial interface as master so that the CPU generates the serial clock for the MAX144/MAX145. Select a clock frequency from 100kHz to 2.17MHz (external clock mode).

1) Use a general-purpose I/O line on the CPU to pull $\overline{CS}$/SHDN low while SCLK is low.
2) Wait for the minimum wake-up time (t_{WAKE}) specified before activating SCLK.
3) Activate SCLK for a minimum of 16 clock cycles. The serial data stream of three leading ones, the channel identification, and the MSB of the digitized input signal begin at the first falling clock edge. DOUT transitions on SCLK's falling edge and is available in MSB-first format. Observe the SCLK to

DOUT valid timing characteristic. Data should be clocked into the µP on SCLK's rising edge.

4) Pull $\overline{CS}$/SHDN high at or after the 16th falling clock edge. If $\overline{CS}$/SHDN remains low, trailing zeros will be clocked out after the LSB.
5) With $\overline{CS}$/SHDN high, wait at least 60ns (t_{CS}) before starting a new conversion by pulling $\overline{CS}$/SHDN low. A conversion can be aborted by pulling $\overline{CS}$/SHDN high before the conversion ends; wait at least 60ns before starting a new conversion.

Data can be output in two 8-bit sequences or continuously. The bytes will contain the result of the conversion padded with three leading ones and the channel identification before the MSB. If the serial clock hasn't been idled after the last LSB and $\overline{CS}$/SHDN is kept low, DOUT sends trailing zeros.

SPI and MICROWIRE Interface

When using SPI (Figure 8a) or MICROWIRE (Figure 8b) interfaces, set CPOL = 0 and CPHA = 0. Conversion begins with a falling edge on $\overline{CS}$/SHDN (Figure 8c). Two consecutive 8-bit readings are necessary to obtain the entire 12-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the µP on SCLK's rising edge. The first 8-bit data stream contains three leading ones, the channel identi-

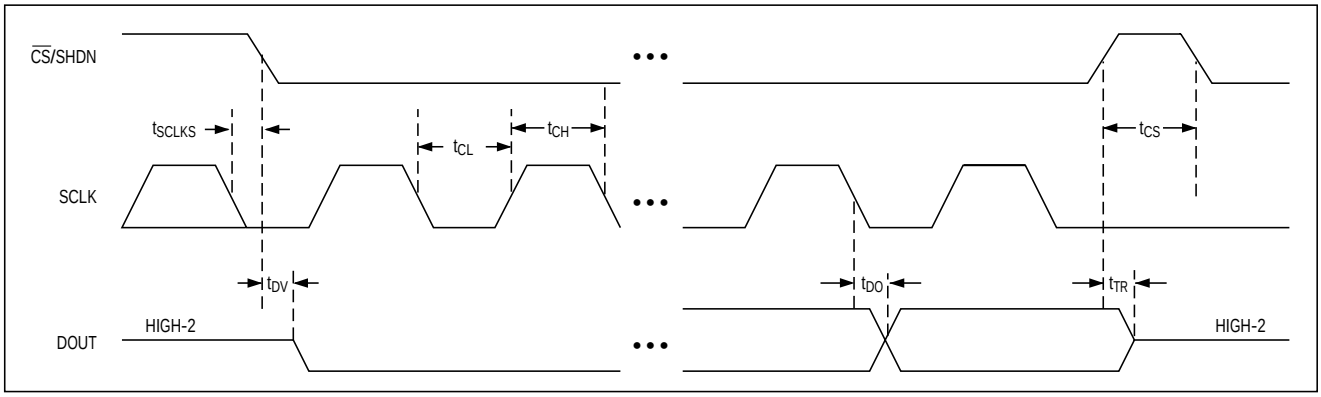


Figure 7. Detailed Serial-Interface Timing Sequence

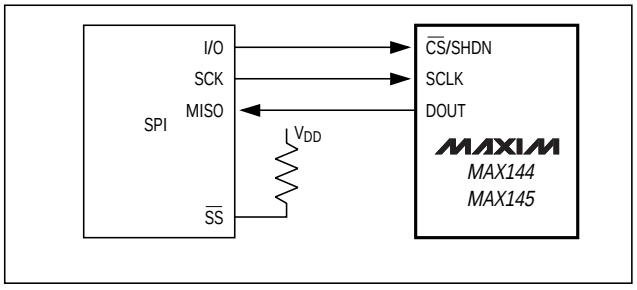
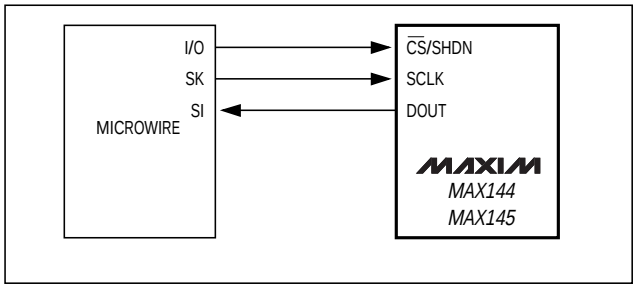


Figure 8a. SPI Connections



8b. MICROWIRE Connections

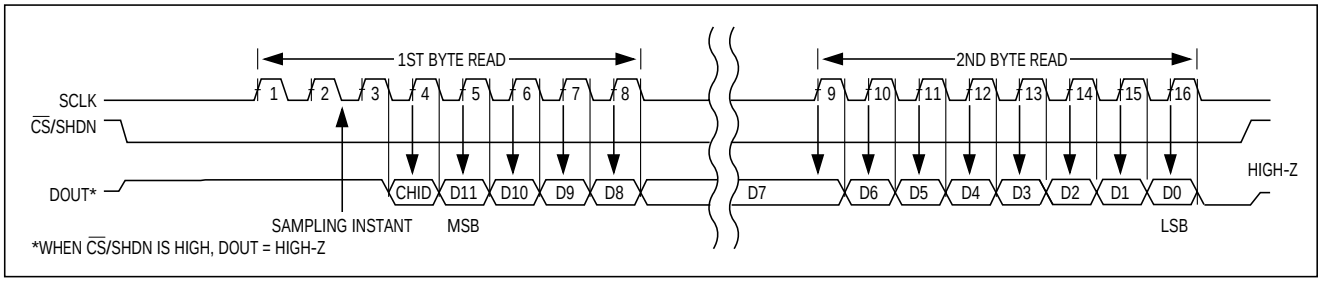


Figure 8c. SPI/MICROWIRE Interface Timing Sequence (CPOL = CPHA = 0)

fication, and the first four data bits starting with the MSB. The second 8-bit data stream contains the remaining bits, D7 through D0.

QSPI Interface

Using the high-speed QSPI interface with CPOL = 0 and CPHA = 0, the MAX144/MAX145 support a maximum f_{SCLK} of 2.17MHz. The QSPI circuit in Figure 9a can be programmed to perform a conversion on each of the two channels for the MAX144. Figure 9b shows the QSPI interface timing.

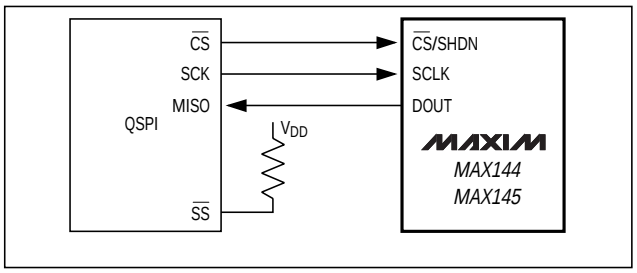


Figure 9a. QSPI Connections

PIC16 with SSP Module and PIC17 Interface

The MAX144/MAX145 are compatible with a PIC16/PIC17 controller (µC), using the synchronous serial-port (SSP) module.

To establish SPI communication, connect the controller as shown in Figure 10a and configure the PIC16/PIC17 as system master by initializing its synchronous serial-port control register (SSPCON) and synchronous serial-port status register (SSPSTAT) to the bit patterns shown in Tables 2 and 3.

In SPI mode, the PIC16/PIC17 µCs allow 8 bits of data to be synchronously transmitted and received simultaneously. Two consecutive 8-bit readings (Figure 10b) are necessary to obtain the entire 12-bit result from the ADC. DOUT data transitions on the serial clock's falling edge and is clocked into the µC on SCLK's rising edge. The first 8-bit data stream contains three leading ones, the channel identification, and the first four data bits starting with the MSB. The second 8-bit data stream contains the remaining bits, D7 through D0.

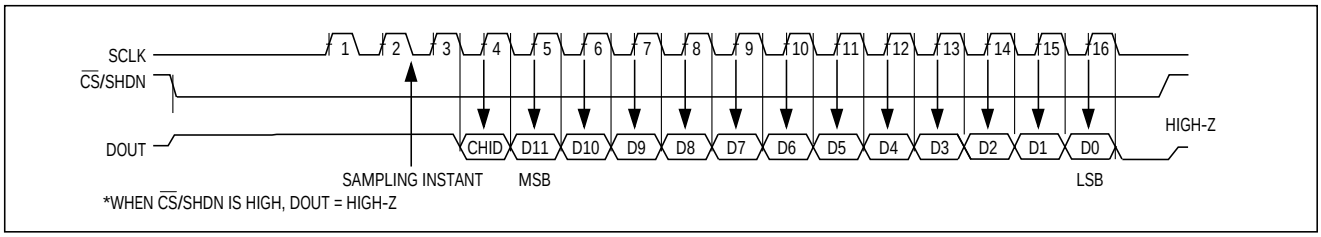


Figure 9b. QSPI Interface Timing Sequence (CPOL = CPHA = 0)

Table 2. Detailed SSPCON Register Contents

CONTROL BIT		MAX144/MAX145 SETTINGS	SYNCHRONOUS SERIAL-PORT CONTROL REGISTER (SSPCON)
WCOL	BIT7	X	Write Collision Detection Bit
SSPOV	BIT6	X	Receive Overflow Detect Bit
SSPEN	BIT5	1	Synchronous Serial-Port Enable Bit. 0: Disables serial port and configures these pins as I/O port pins. 1: Enables serial port and configures SCK, SDO and SCI pins as serial port pins.
CKP	BIT4	0	Clock Polarity Select Bit. CKP = 0 for SPI master mode selection.
SSPM3	BIT3	0	Synchronous Serial-Port Mode Select Bit. Sets SPI master mode and selects $f_{CLK} = f_{OSC} / 16$.
SSPM2	BIT2	0	
SSPM1	BIT1	0	
SSPM0	BIT0	1	

X = Don't care

Table 3. Detailed SSPSTAT Register Contents

CONTROL BIT		MAX144/MAX145 SETTINGS	SYNCHRONOUS SERIAL-PORT STATUS REGISTER (SSPSTAT)
SMP	BIT7	0	SPI Data Input Sample Phase. Input data is sampled at the middle of the data output time.
CKE	BIT6	1	SPI Clock Edge Select Bit. Data will be transmitted on the rising edge of the serial clock.
D/A	BIT5	X	Data Address Bit
P	BIT4	X	Stop Bit
S	BIT3	X	Start Bit
R/W	BIT2	X	Read/Write Bit Information
UA	BIT1	X	Update Address
BF	BIT0	X	Buffer Full Status Bit

X = Don't care

Layout, Grounding, and Bypassing

For best performance, use printed circuit boards (PCBs). Wire-wrap configurations are not recommended, since the layout should ensure proper separation of analog and digital traces. Run analog and digital lines anti-parallel to each other, and don't lay out digital signal paths underneath the ADC package. Use separate analog and digital PCB ground sections with only one star-point (Figure 11) connecting the two ground systems (analog and digital). For lowest-noise operation, ensure the ground return to the star ground's power supply is low impedance and as short as possible. Route digital signals far away from sensitive analog and reference inputs.

High-frequency noise in the power supply V_{DD} could influence the proper operation of the ADC's fast comparator. Bypass V_{DD} to the star ground with a network of two parallel capacitors (0.1µF and 1µF) located as close as possible to the power supply pin of MAX144/MAX145. Minimize capacitor lead length for best supply-noise rejection and add an attenuation resistor (10Ω) if the power supply is extremely noisy.

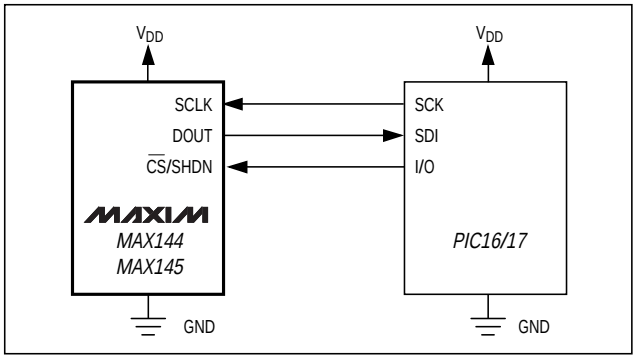


Figure 10a. SPI Interface Connection for a PIC16/PIC17 Controller

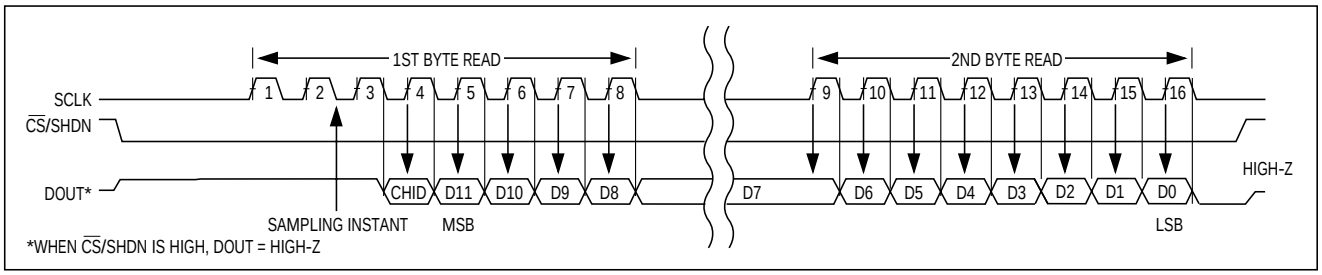


Figure 10b. SPI Interface Timing with PIC16/PIC17 in Master Mode (CKE = 1, CKP = 0, SMP = 0, SSPM3–SSPM0 = 0001)

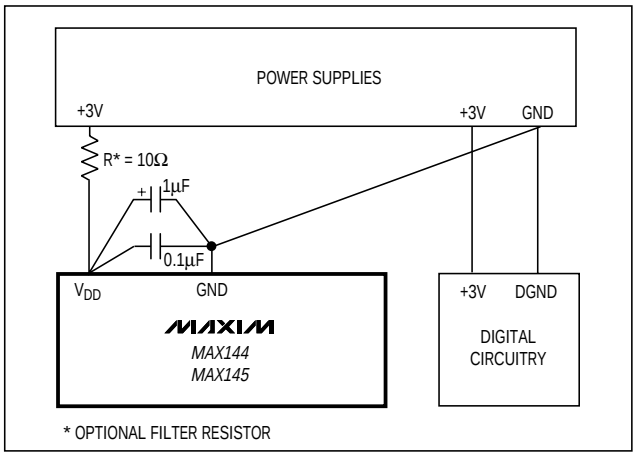


Figure 11. Power-Supply Bypassing and Grounding

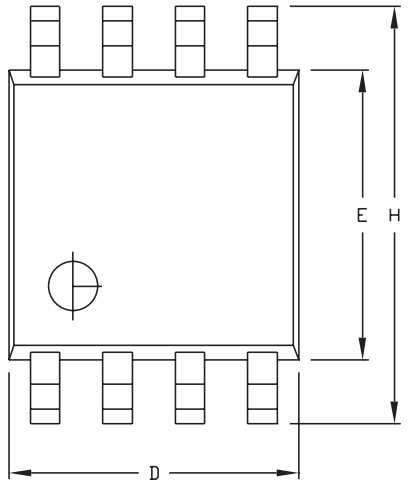
Chip Information

TRANSISTOR COUNT: 2,058

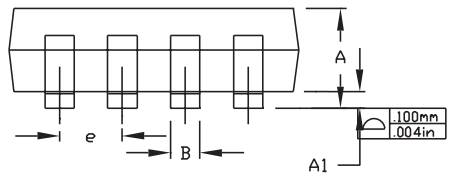
SUBSTRATE CONNECTED TO GND

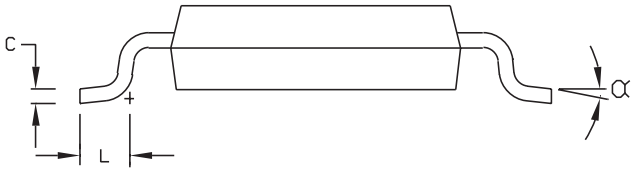
Package Information

8LUMAXD.EPS



	INCHES		MILLIMETERS		JEDEC INCHES		JEDEC MILLIMETERS	
	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX
A	0.037	0.043	0.94	1.10	---	0.043	---	1.10
A1	0.002	0.006	0.05	0.15	0.002	0.006	0.05	0.15
B	0.010	0.014	0.25	0.36	0.010	0.016	0.25	0.40
C	0.005	0.007	0.13	0.18	0.005	0.009	0.13	0.23
D	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
e	0.0256 BSC		0.65 BSC		0.0256 BSC		0.64 BSC	
E	0.116	0.120	2.95	3.05	0.114	0.122	2.9	3.1
H	0.188	0.198	4.78	5.03	0.193 BSC		4.9 BSC	
L	0.016	0.026	0.41	0.66	0.016	0.027	0.40	0.70
α	0°	6°	0°	6°	0°	6°	0°	6°





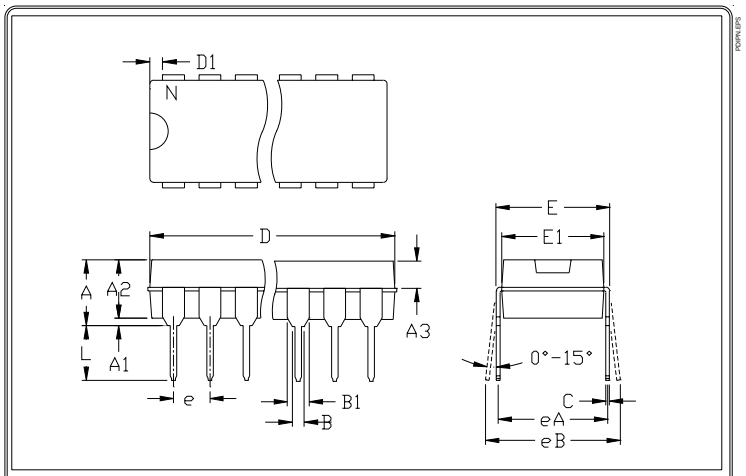
NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm(.006").
3. CONTROLLING DIMENSION: INCHES.
4. MEETS JEDEC MO-187.

MAXIM
PROPRIETARY INFORMATION

TITLE: 8LD µMAX PACKAGE OUTLINE DWG.			
APPROVAL	DOCUMENT CONTROL NO. 21-0036	REV E	1/1

+2.7V, Low-Power, 2-Channel, 108ksps, Serial 12-Bit ADCs in 8-Pin µMAX

Package Information (continued)



	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	---	0.200	---	5.08
A1	0.015	---	0.38	---
A2	0.125	0.175	3.18	4.45
A3	0.055	0.080	1.40	2.03
B	0.016	0.022	0.41	0.56
B1	0.045	0.065	1.14	1.65
C	0.008	0.012	0.20	0.30
D1	0.005	0.080	0.13	2.03
E	0.300	0.325	7.62	8.26
E1	0.240	0.310	6.10	7.87
e	0.100	---	2.54	---
eA	0.300	---	7.62	---
eB	---	0.400	---	10.16
L	0.115	0.150	2.92	3.81

	INCHES		MILLIMETERS			
	MIN	MAX	MIN	MAX	N	MS001
D	0.348	0.390	8.84	9.91	8	AB
D	0.735	0.765	18.67	19.43	14	AC
D	0.745	0.765	18.92	19.43	16	AA
D	0.885	0.915	22.48	23.24	18	AD
D	1.015	1.045	25.78	26.54	20	AE
D	1.14	1.265	28.96	32.13	24	AF
D	1.360	1.380	34.54	35.05	28	✱5

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED .15mm (.006")
3. CONTROLLING DIMENSION: MILLIMETER
4. MEETS JEDEC MS001-XX AS SHOWN IN ABOVE TABLE
5. SIMILIAR TO JEDEC MO-058AB
6. N = NUMBER OF PINS

MAXIM 120 SAN GABRIEL DR SUNNYVALE CA 94086 FAX (408) 737 7194 PROPRIETARY INFORMATION

TITLE: PACKAGE FAMILY OUTLINE: PDIP .300" | 1/1 | 21-0043 A (DOCUMENT CONTROL NUMBER, REV.)