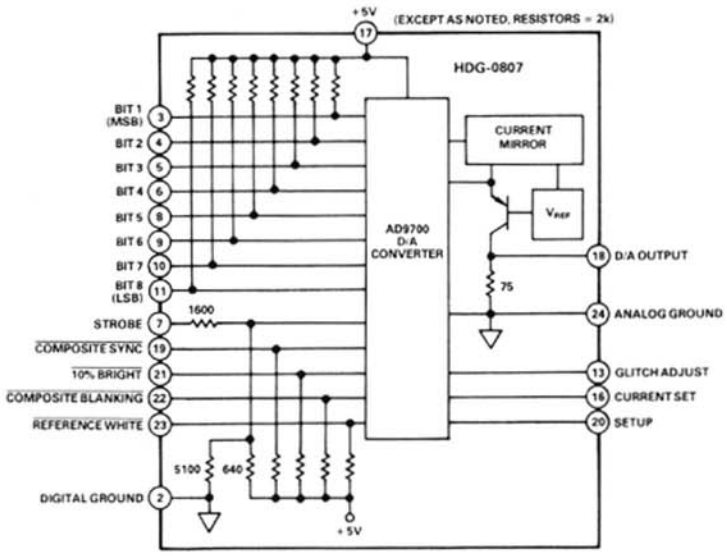
Hybrid Video Digital-to-Analog Converter

HDG-0807

FEATURES
- Update Rates to 50MHz
- Low Glitch
- Complete Composite Inputs
- Single +5V Power Supply
- TTL-Compatible Inputs
- Directly Drives 75Ω to Ground

APPLICATIONS
- Raster Scan Displays
- Color Graphics
- Analytical Instrumentation
- TV Video Reconstruction

HDG-0807 FUNCTIONAL BLOCK DIAGRAM



GENERAL DESCRIPTION

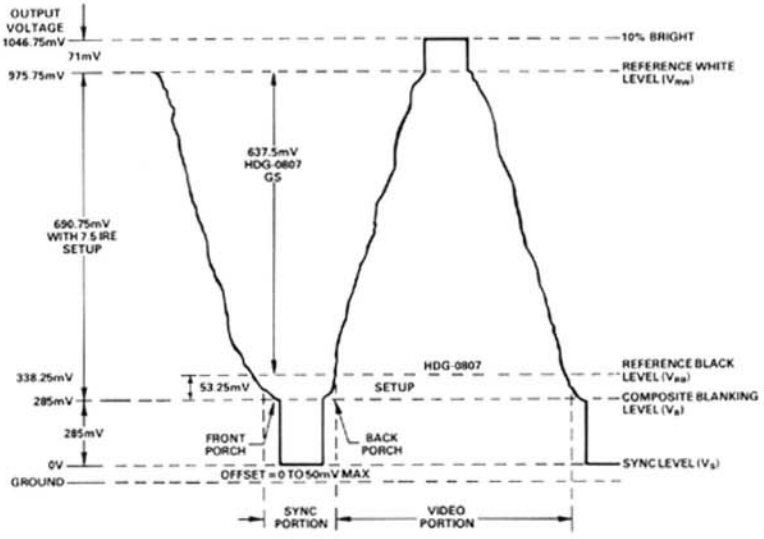
The HDG-0807 D/A Converters are extensions of the technology and capabilities of the HDG-Series high-speed raster scan D/A converters. They offer the user increased flexibility because of their ability to operate on a single +5V power supply, and their compatibility with TTL signals.

The HDG-0807 is an eight-bit (256 levels) device.

Both versions have complete composite controls, including self-contained, digitally-controlled sync and blanking; and a reference white control input to help assure compatibility with EIA Standards RS-170, RS-330, and RS-343-A. Performance is enhanced even more with a 10% bright input capability.

Output impedance is 75Ω and the full-scale output current is capable of developing standard video levels across video loads. An output current mirror shifts the output to ground reference while attenuating power supply noise by means of common-mode rejection.

Model numbers with "BW" suffixes are housed in 24-pin non-hermetic ceramic dual-in-line packages. Versions with "BD" suffixes are housed in hermetically-sealed ceramic DIP packages.



HDG-0807 Composite Waveform

SPECIFICATIONS (typical @ +25°C with nominal power supplies unless otherwise noted)

Parameter	Units	HDG-0807BD/BW
RESOLUTION	Bits	8
LEAST SIGNIFICANT BIT (LSB) WEIGHT		
Voltage (adjustable)	mV	2.5
Current (adjustable)	μA	67
ACCURACY		
(GS = Gray Scale; FS = Full-Scale)		
Linearity	±% GS	0.2
Differential Linearity	±% GS, max	0.2
Zero Offset (Initial)		
Voltage	mV, max	50
Monotonicity		Guaranteed
TEMPERATURE COEFFICIENTS		
Linearity	ppm/°C (max)	15 (30)
Gain	ppm/°C (max)	350 (1,000)
Zero Offset	mV/°C (max)	1.0 (2.0)
DYNAMIC CHARACTERISTICS – GS OUTPUT[1]		
Settling Time	% GS;	0.4
1LSB Midscale Voltage Change	ns (max)	14 (16)
0V to FS GS Voltage Change	ns (max)	15 (18)
Slew Rate	V/μs	250
Rise Time	ns	2.2
Glitch Impulse[2]	pV-s	50
DIGITAL DATA INPUTS		
Logic Compatibility		TTL
Coding		Binary (BIN)
Logic Levels[3]		
"1"	V (min/max)	(+3.8/+5.0)
"0"	V (min/max)	(0/+3.0)
Loading (each bit)		5pF and 2kΩ to +5V
Data Update Rate	MHz (Guaranteed)	50 (45)
STROBE INPUT		
Logic Compatibility		TTL
Logic Levels		
"1"	V (min/max)	(+2.5/+5.0)
"0"	V (min/max)	(0/+1.5)
Loading		1pF and 2.2kΩ to +4.4V
Setup Time (Data)	ns, min	3
Hold Time (Data)	ns, min	3
Propagation Delay	ns (max)	8
$\overline{\text{10\% BRIGHT}}$, $\overline{\text{REFERENCE WHITE}}$, $\overline{\text{COMPOSITE SYNC}}$, AND $\overline{\text{COMPOSITE BLANKING}}$ INPUTS		
Logic Compatibility		TTL
Logic Levels		
"1"	V (min/max)	(+3.8/+5)
"0"	V (min/max)	(0/+3.5)
Loading		5pF and 2kΩ to +5V
SPEED PERFORMANCE – CONTROL INPUTS		
Settling Time to 10% of Final Value for:		
$\overline{\text{10\% Bright}}$	ns (max)	15
$\overline{\text{Reference White}}$	ns (max)	15
$\overline{\text{Composite Sync}}$	ns (max)	15
$\overline{\text{Composite Blanking}}$	ns (max)	15
SETUP CONTROL		
+5V	mV (IRE Units)	0 (0)
Open	mV (IRE Units)	53.25 (7.5)
ANALOG OUTPUT		
GS Voltage p-p[4]	mV (±4%)	637.5
Compliance	V	−3 to +3
Internal Impedance	Ω (min/max)	75 (71/79)

Parameter	Units	HDG-0807BD/BW
OUTPUT – $\overline{\text{REFERENCE WHITE}}$[5]		
(Assumes Setup is Open, Which is Equivalent to 7.5 IRE Units)		
Voltage		
Logic "1"	mV (±4%)	Normal Operation
Logic "0"		
$\overline{\text{10% Bright}}$ @ "0"	mV	1046.75
$\overline{\text{10% Bright}}$ @ "1"	mV	975.75
OUTPUT – $\overline{\text{10% BRIGHT}}$[6]		
Voltage		
Logic "1"	mV (±4%)	0
Logic "0"	mV (±4%)	71
OUTPUT – $\overline{\text{COMPOSITE SYNC}}$[6,7]		
Voltage		
Logic "1"	mV (±4%)	0
Logic "0"	mV (±4%)	285
OUTPUT – $\overline{\text{COMPOSITE BLANKING}}$[6,7]		
(Assumes Setup is Open)		
Voltage		
Logic "1"	mV (±4%)	0
Logic "0"	mV (±4%)	53.25
POWER REQUIREMENTS		
+5V to ±0.25V	mA (max)	185 (225)
Power Supply Rejection Ratio	%/V	0.025/0.25
Power Dissipation	mW (max)	925 (1125)
TEMPERATURE RANGE		
Operating (Case)	°C	−25 to +85
Storage	°C	−55 to +150
THERMAL RESISTANCE[8]		
Junction to Air, θ_{JA} (Free Air)	°C/W, max	45
Junction to Case, θ_{JC}	°C/W, max	12
PACKAGE OPTION[9]		
DH-24B		HDG-0807BD HDG-0807BW

For applications assistance, phone Computer Labs Division at (919) 668-9511

NOTES

[1]Settling to GS percentage includes FS and MSB transitions. Inherent 3ns register delay (50% points) is not included.

[2]Glitch can be reduced with glitch adjustment.

[3]Internal 2k pull-up resistors help assure compatibility with logic levels of multiple TTL families.

[4]LSB value used for calibration causes Gray Scale output to be 637.5mV rather than 643mV shown in idealized composite waveform; both values are well within the output and EIA Standard RS-170 tolerances.

[5]Effect on analog output of logic "0" at $\overline{\text{Reference White}}$ input depends on $\overline{\text{10% Bright}}$ signal input.

[6]$\overline{\text{10% Bright}}$, $\overline{\text{Composite Sync}}$, and $\overline{\text{Composite Blanking}}$ outputs shown add to Gray scale analog output at Pin 18 and are measured with respect to sync level (V_S) shown in waveform.

[7]$\overline{\text{Composite Sync}}$ or $\overline{\text{Composite Blanking}}$ control signals reset input registers. $\overline{\text{Composite Sync}}$ or $\overline{\text{Composite Blanking}}$ should not be operated simultaneously with $\overline{\text{Reference White}}$, which sets input registers.

[8]Maximum junction temperature = 150°C.

[9]See Section 14 for package outline information.

Specifications subject to change without notice.

PIN DESIGNATIONS
(As Viewed from Bottom)

Pin	Function	Pin	Function
24	ANALOG GROUND	1	+5V
23	$\overline{\text{REFERENCE WHITE}}$	2	DIGITAL GROUND
22	$\overline{\text{COMPOSITE BLANKING}}$	3	BIT 1 (MSB)
21	$\overline{\text{10% BRIGHT}}$	4	BIT 2
20	SETUP	5	BIT 3
19	$\overline{\text{COMPOSITE SYNC}}$	6	BIT 4
18	ANALOG OUTPUT	7	STROBE
17	+5V	8	BIT 5
16	+5V	9	BIT 6
15	+5V	10	BIT 7
14	+5V	11	BIT 8 (LSB)
13	GLITCH ADJUST	12	+5V

NOTES: Connect Pins 2 and 24 together and to low-impedance ground plane as close to case as possible.
+5V must be applied to all designated pins.

THEORY OF OPERATION

Refer to the block diagram of the HDG-0807 D/A Converter and the HDG-0807 composite output waveform.

The digital input bits represent the Gray Scale values (the discrete levels between Reference Black and Reference White) in a composite video signal. For HDG-0807 units, there are 256 (2^8) levels.

Input bits are applied to Pins 3-6 and Pins 8-11 for the HDG-0807.

The output analog signal (at Pin 18) will be a function of these digital inputs. The output will also be affected by the TTL levels at the control inputs of $\overline{10\%\ \text{Bright}}$, $\overline{\text{Reference White}}$, $\overline{\text{Composite Sync}}$, and $\overline{\text{Composite Blanking}}$; and the level of the control signal (expressed in terms of IRE units) at the Setup input.

The total effect of these combined signals can be illustrated in a truth table format if arbitrary values are assigned for Gray scale inputs, and various combinations of control inputs are selected.

Refer to Table I.

Analog Devices uses 2.5mV for weighting the LSB during calibration of the converter, which causes the full-scale 637.5mV output of the HDG-0807 to be different from the ideal 643mV output shown in the composite waveform in the RS-170 standard.

This disparity does not cause any problems in using the device, since both the ideal value and the actual value are well within the tolerances of the output and the RS-170 standard.

Referring again to the block diagram, the Strobe input applied to the HDG D/A clocks the input registers when the strobe signal makes the transition from a logic "0" to a logic "1". The purpose of the registers is to remove time skew from the digital input bits and minimize perturbations or "glitches" in the analog output signal.

A logic "0" applied to either the $\overline{\text{Composite Sync}}$ or $\overline{\text{Composite Blanking}}$ input resets the input registers to 00 000 000. A logic "0" signal applied to the $\overline{\text{Reference White}}$ input sets the input registers, thereby overriding the video input word. When this occurs, the analog output of the converter goes to $\overline{1046.75\text{mV}}$ or to 975.75mV, depending upon whether or not the $\overline{10\%\ \text{Bright}}$ signal is also operated.

When $\overline{\text{Composite Blanking}}$ is operated, the analog output will go to a Reference Black value of 338.25mV less some amount, as determined by the voltage at Setup. The 53.25mV example used in the Specifications section of the data sheet is based on the Setup input floating, which is equivalent to 7.5 IRE units. (For this example, the analog output would be 285mV.)

APPLICATIONS

The HDG-0807 is specifically designed for operation in raster scan graphics applications, in which digital input data are being changed at a relatively high rate.

The D/A output is generally ac-coupled to the monitor, which eliminates the changing dc offset associated with the thermal drift of the level shift circuits. This offset drift, which is a function of output level, is held to a maximum of 50mV and will not affect dynamic video levels.

For optimum performance, ground pins 2 and 24 should be connected together and to a large ground plane near the unit. As indicated in the footnotes on the pin designations table, +5V must be applied to all pins which are called out to receive it.

The performance of the HDG devices can be enhanced with external bypass capacitors which will supplement the internal components. Low-frequency bypassing should be provided with 1μF (or larger) tantalum capacitors between the +5V supply pins and ground. High-frequency bypassing can be provided with ceramic capacitors of 0.1μF or larger. All bypass capacitors should be tied as closely as possible to the hybrid power supply pins.

A 200Ω potentiometer between +5V and ground with the center arm connected to Pin 13 changes the threshold of the internal current switches; this can reduce the amount of glitch from the typical 50pV-s to a lesser value when required.

For best performance, standard 24-pin hybrid sockets should be avoided. Individual pin sockets are preferable for evaluating devices and are available from Analog Devices; in final designs, the D/A should be soldered directly into the printed circuit board without sockets.

If it is necessary to route digital signals and/or strobe signals for distances greater than one inch (2.54cm), microstrip techniques should be used. Otherwise, the performance of the D/A converter may be affected adversely.

ORDERING INFORMATION

There are two versions of the 8-bit converter; both units operate over a temperature range of −25°C to +85°C. The model numbers are HDG-0807BD or HDG-0807BW. In these model numbers, the "D" in the suffix indicates a ceramic, hermetically-sealed DIP; and the "W" indicates a non-hermetic ceramic DIP.

Versions are available screened to military requirements; contact the factory for details. It is also possible to order units with synchronous functions on a "special order" basis; detailed information is available from the factory.

DIGITAL INPUTS VS. ANALOG OUTPUT

BIT 1	BIT 2	BIT 3	BIT 4	BIT 5	BIT 6	BIT 7	BIT 8	$\overline{10\%\ \text{BRIGHT}}$	$\overline{\text{REF. WHITE}}$	$\overline{\text{BLANKING}}$	$\overline{\text{COMP. SYNC}}$	ANALOG OUTPUT IN mV[1] (HDG-0807)
1	1	1	1	1	1	1	1	0	1	1	1	1046.75
1	1	1	1	1	1	1	1	1	1	1	1	975.75
1	0	0	0	0	0	0	0	0	1	1	1	729.25
0	0	0	0	0	0	0	0	0	1	1	1	409.25
0	0	0	0	0	0	0	0	1	1	1	1	338.25
X	X	X	X	X	X	X	X	0	0	1	1	1046.75
X	X	X	X	X	X	X	X	1	0	1	1	975.75
X	X	X	X	X	X	X	X	0	1	0	1	338.25[2]
X	X	X	X	X	X	X	X	0	1	0	1	285[3]
X	X	X	X	X	X	X	X	0	1	0	0	124.25[2]
X	X	X	X	X	X	X	X	0	1	0	0	71[3]
X	X	X	X	X	X	X	X	1	1	0	0	53.25[2]
X	X	X	X	X	X	X	X	1	1	0	0	0[3]

NOTES
[1]Values are for Gray Scale output of HDG-0807 measured with respect to Sync level.
[2]Setup (Pin 20) to +5V. (0 IRE units)
[3]Setup (Pin 20) open. (7.5 IRE units)

Table I. Digital Inputs vs. Analog Output