SONY

CXA1819Q

RGB Driver for LCD

Description

The CXA1819Q is an RGB driver designed for LCD panel LCX007. It supports a line alternative RGB drive system. In addition, three-panel projectors can be supported by using three CXA1819Q ICs.

Features

- Built-in RGB signal phase matching sample-and-hold circuit
- Effective frequency response (horizontal resolution of 600 TV lines achieved in combination with the LCX007AL)
- Built-in γ control circuit
- Built-in side black generation circuit for 4:3/16:9 aspect conversion
- Built-in VCOM voltage output circuit

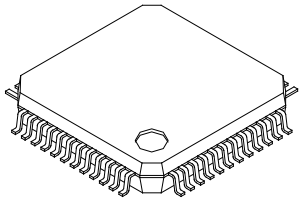
Absolute Maximum Ratings

• Supply voltage	V_{CC}	14	V
• Operating temperature	Topr	–20 to +75	°C
• Storage temperature	Tstg	–65 to +150	°C
• Allowable power dissipation	P_D	600	mW

Operating Condition

Supply voltage	$V_{CC}1$	5	V
	$V_{CC}2$	12.2 to 13.3	V

48 pin QFP (Plastic)



Structure

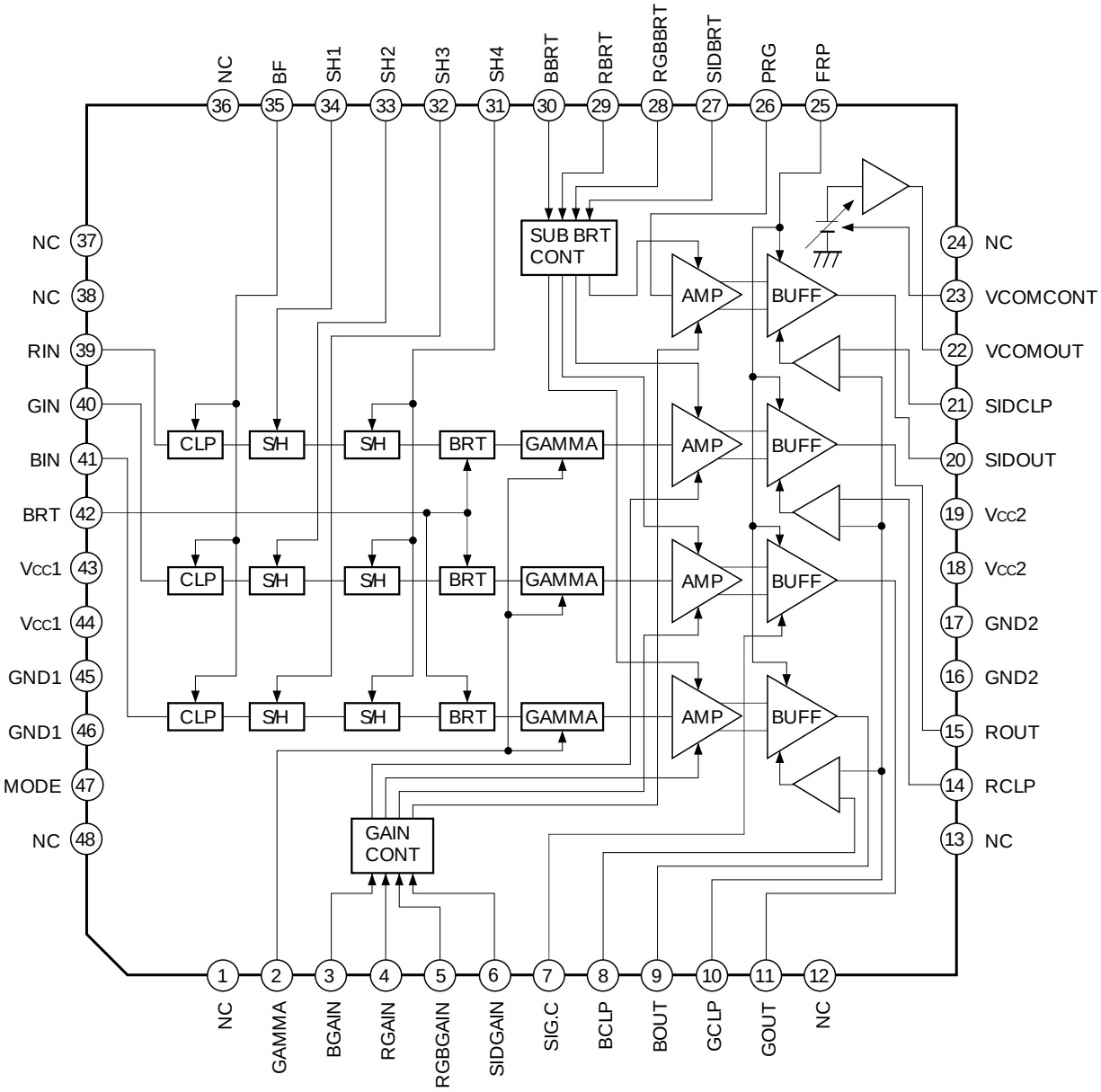
Bipolar silicon monolithic IC

Applications

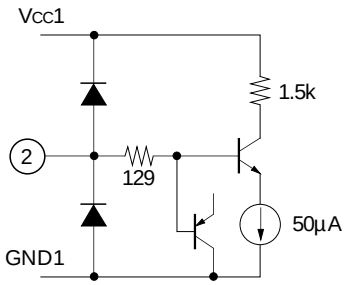
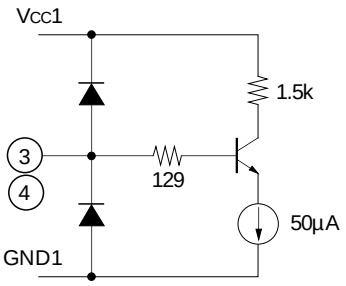
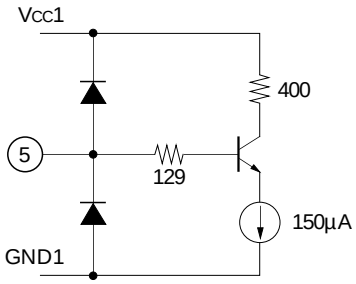
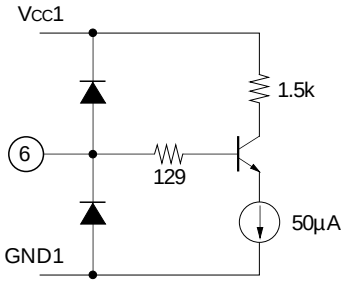
Liquid crystal projectors
Liquid crystal viewfinders
Compact liquid crystal monitors

E94634A77

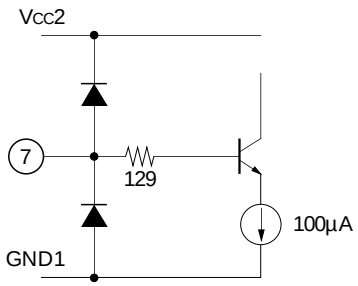
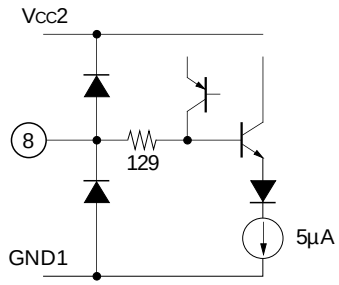
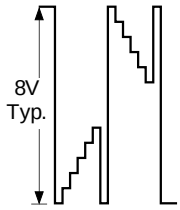
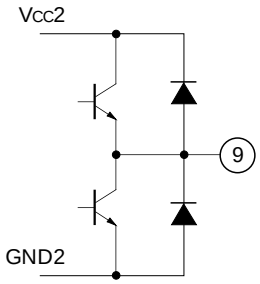
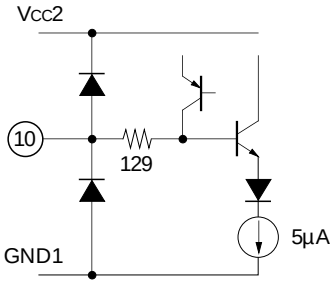
Block Diagram



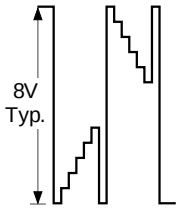
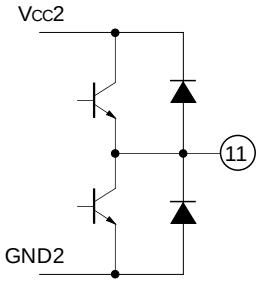
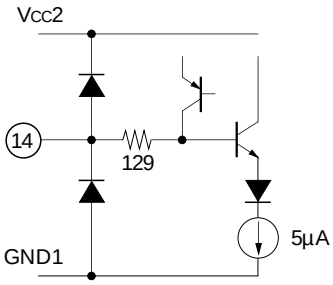
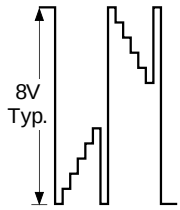
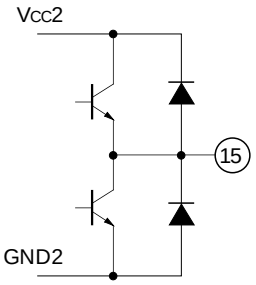
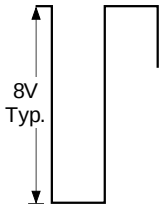
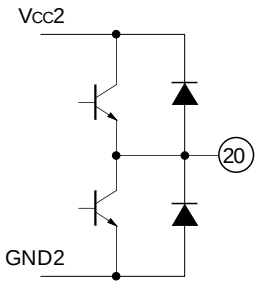
Pin Description

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
2	GAMMA	0 to 5V*		Gamma control. Gamma variable range: 3.7 to 15dB Preset mode (pin 0V) ≈ 0dB
3	B GAIN	1.6 to 5V*		B signal gain control. Gain variable range: –2.0 to +2.0dB
4	R GAIN	1.6 to 5V*		R signal gain control. Gain variable range: –2.0 to +2.0dB
5	RGB GAIN	1.6 to 5V*		RGB signal common gain control. Gain variable range: 5.5 to 11dB
6	SID GAIN	1.6 to 5V*		SID signal gray level control.

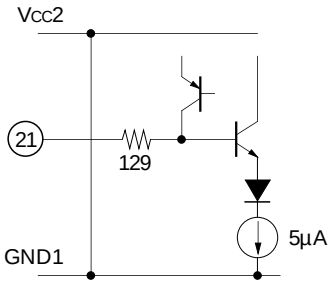
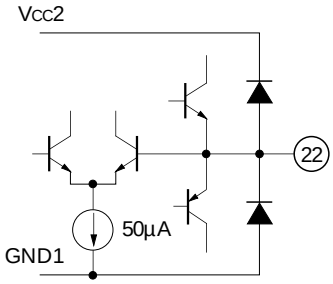
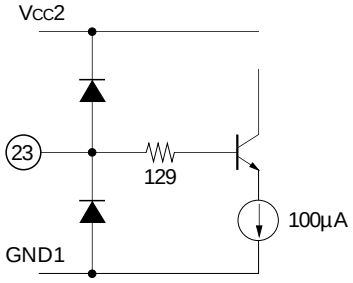
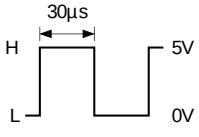
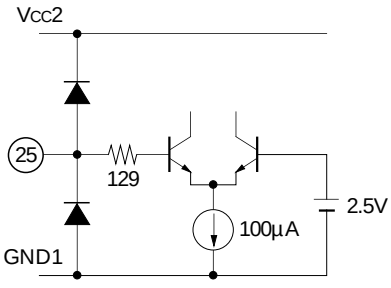
Note) * in the Pin voltage indicates external applied voltage.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
7	SIG CENT	1.6 to 5V*		RGB signal center voltage control. Center voltage variable range: 6.2 to 7.6V
8	B CLP	6.2 to 7.6V*		B output detection signal input.
9	B OUT			B signal output. The output is fed back to provide sufficiently low impedance (less than few Ω).
10	G CLP	6.2 to 7.6V*		G output detection signal input.

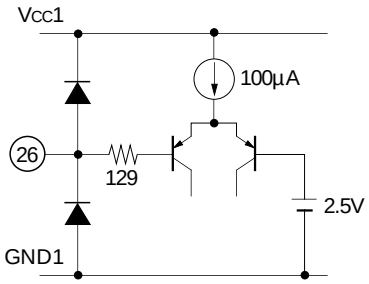
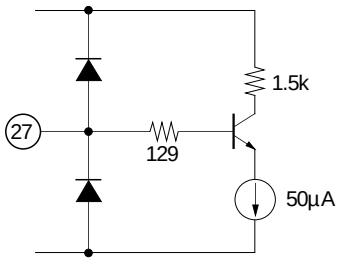
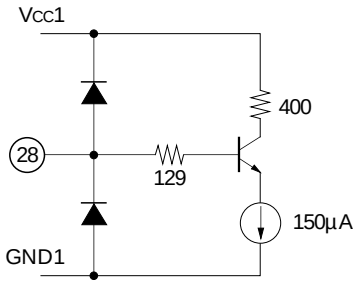
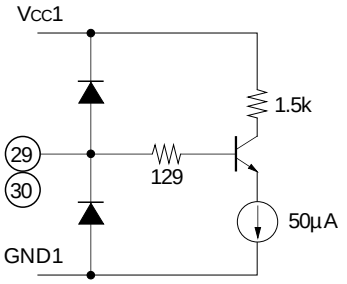
Note) * in the Pin voltage indicates external applied voltage.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
11	G OUT			G signal output. The output is fed back to provide sufficiently low impedance (less than few Ω).
14	R CLP	6.2 to 7.6V*		R output detection signal input.
15	R OUT			R signal output. The output is fed back to provide sufficiently low impedance (less than few Ω).
16 17	GND2	GND		GND.
18 19	Vcc2	13V		13V power supply.
20	SID OUT			SID signal output. The output is fed back to provide sufficiently low impedance (less than few Ω).

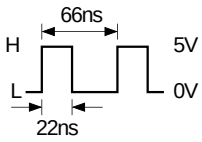
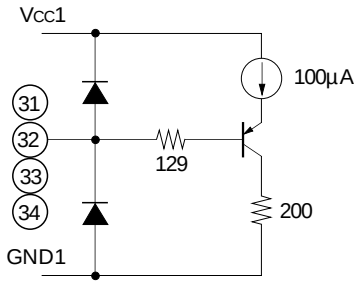
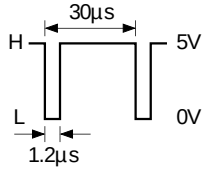
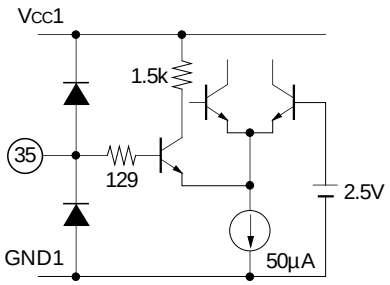
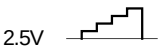
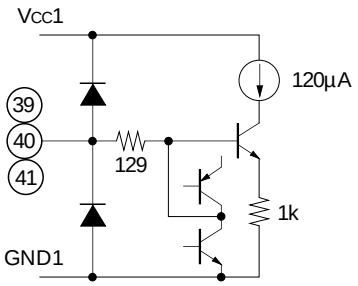
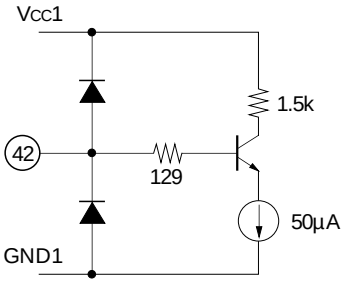
Note) * in the Pin voltage indicates external applied voltage.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
21	SID CLP	6.2 to 7.6V*		SID output detection signal input.
22	VCOM OUT	6.2 to 8.0V		VCOM voltage output. The output is fed back to provide sufficiently low impedance (less than few Ω).
23	VCOM CONT	1.6 to 5V*		VCOM voltage control. VCOM voltage variable range: 6.2 to 8.0V
25	FRP			Flyback pulse input. This pulse is used to invert the polarity of R, G and B outputs. Input level: High ≥ 4V, Low ≤ 1V

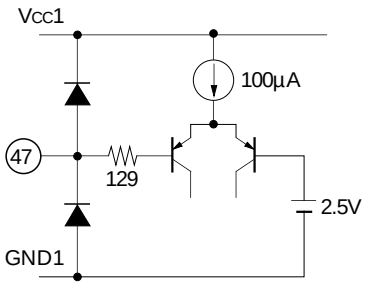
Note) * in the Pin voltage indicates external applied voltage.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
26	PRG	0V*		This pin switches black level and gray level output of the SID signal. Black level is output for 0V and gray level is output for 5V. This pin should normally be set to 0V.
27	SID BRT	1.6 to 5V*		SID signal black level control.
28	RGB BRT	1.6 to 5V*		RGB signal common brightness control. Brightness variable range: 5 to 9.8V
29	R BRT	1.6 to 5V*		R signal brightness control. Brightness variable range (difference with G signal): –1.0 to +0.7V
30	B BRT	1.6 to 5V*		B signal brightness control. Brightness variable range (difference with G signal): –1.0 to +0.7V

Note) * in the Pin voltage indicates external applied voltage.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
31	SH4			Resampling sample-and-hold pulse input. Input level: High ≥ 4.2V, Low ≤ 0.4V
32	SH3			B signal sample-and-hold pulse input. Input level: High ≥ 4.2V, Low ≤ 0.4V
33	SH2			G signal sample-and-hold pulse input. Input level: High ≥ 4.2V, Low ≤ 0.4V
34	SH1			R signal sample-and-hold pulse input. Input level: High ≥ 4.2V, Low ≤ 0.4V
35	BF			Burst flag pulse input. Used as an input clamp pulse. Input level: High ≥ 4V, Low ≤ 1V
39	R IN	 (PEDESTAL LEVEL) Signal more than 1V from pedestal is sliced after input to IC.		R signal input.
40	G IN			G signal input.
41	B IN			B signal input.
42	BRT	1.6 to 5V*		User brightness control. Adjusts the input DC level for the gamma breakpoint. Control voltage: 1.6 to 5V

Note) * in the Pin voltage indicates external applied voltage.

Pin No.	Symbol	Pin voltage	Equivalent circuit	Description
43 44	Vcc1	5V		5V power supply.
45 46	GND1	GND		GND.
47	MODE	5V*		Gain control mode selector. Normal mode for 5V and high gain mode for 0V. This pin should normally be set to 5V.

Note) * in the Pin voltage indicates external applied voltage.

Electrical Characteristics (Ta = 25°C, Vcc1 = 5V, Vcc2 = 13V, see the Electrical Characteristics Measurement Circuit.)

No.	Item		Symbol	Measurement conditions			Measurement method	Min.	Typ.	Max.	Unit
				Input pin	Conditions	Measurement point					
1	Current consumption 1		Icc1			43 44	5V power supply current consumption I43 + I44	16.6	22	27.4	mA
2	Current consumption 2		Icc2			18 19	13V power supply current consumption I18 + I19	11.4	14	21.1	mA
3	Frequency response		FR	39	Input waveform diagram 1 Output waveform diagram 1	15	Frequency which is –3dB at 200kHz		11		MHz
			FG	40		11					
			FB	41		9					
4	R, G, B standard gains		GR	39	Input waveform diagram 2 Output waveform diagram 2	15	I/O gain		8.6		dB
			GG	40		11					
			GB	41		9					
5	RGB gain adjust-ment range	Min.	GGL	40	Input waveform diagram 2 Output waveform diagram 2 RGB gain pin = 1.6V	11	G I/O gain		3.5	5.50	dB
6		Max.	GGH		Input waveform diagram 2 Output waveform diagram 2 RGB gain pin = 5.0V		G I/O gain	11.0	12.5		
7	R gain adjust-ment range	Min.	GRL	39	Input waveform diagram 2 Output waveform diagram 2 R gain pin = 1.6V	15	R I/O gain difference with G I/O gain		–3.5	–2.0	dB
8		Max.	GRH		Input waveform diagram 2 Output waveform diagram 2 R gain pin = 5.0V		R I/O gain difference with G I/O gain	2.0	+3.5		
9	B gain adjust-ment range	Min.	GBL	41	Input waveform diagram 2 Output waveform diagram 2 B gain pin = 1.6V	9	B I/O gain difference with G I/O gain		–3.5	–2.0	dB
10		Max.	GBH		Input waveform diagram 2 Output waveform diagram 2 B gain pin = 5.0V		B I/O gain difference with G I/O gain	2.0	+3.5		
11	SID gain adjust-ment range	Min.	GSL	26	Input waveform diagram 4 Output waveform diagram 6 SID gain pin = 1.6V	20	Black level and gray level difference of SID output		0.75	0.94	V
12		Max.	GSH		Input waveform diagram 4 Output waveform diagram 6 SID gain pin = 5.0V		Black level and gray level difference of SID output	2.1	2.4		

No.	Item		Symbol	Measurement conditions			Measurement method	Min.	Typ.	Max.	Unit
				Input pin	Conditions	Measurement point					
13	Gamma adjust-ment range	Min.	γ RL	39	Input waveform diagram 3 Output waveform diagram 3 GAMMA pin = 1.6V	15	I/O gain–GR		1	3.7	dB
			γ GL	40		11	I/O gain–GG				
			γ BL	41		9	I/O gain–GB				
14		Max.	γ RH	39	Input waveform diagram 3 Output waveform diagram 3 GAMMA pin = 5.0V	15	I/O gain–GR	15	18		
			γ GH	40		11	I/O gain–GG				
			γ BH	41		9	I/O gain–GB				
15	RGB BRT adjust-ment range	Min.	BGL	40	Output waveform diagram 4 RGB BRT pin = 1.6V	11	Voltage between pedestals of odd and even lines at G output		3.9	5.0	V
16		Max.	BGH		Output waveform diagram 4 RGB BRT pin = 5.0V			9.8	10.5		
17	R BRT adjust-ment range	Min.	BRL	39	Output waveform diagram 4 R BRT pin = 1.6V	15	Voltage difference between R output pedestals of odd and even lines to G output		–2.2	–1.0	V
18		Max.	BRH		Output waveform diagram 4 R BRT pin = 5.0V			0.7	2.1		
19	B BRT adjust-ment range	Min.	BBL	41	Output waveform diagram 4 B BRT pin = 1.6V	9	Voltage difference between B output pedestals of odd and even lines to G output		–2.2	–1.0	V
20		Max.	BBH		Output waveform diagram 4 B BRT pin = 5.0V			0.7	2.1		
21	SID BRT adjust-ment range	Min.	BSL	26	Input waveform diagram 4 Output waveform diagram 7 SID BRT pin = 1.6V	20	Voltage difference between SID output black levels		4.1	5.2	V
22		Max.	BSH		Input waveform diagram 4 Output waveform diagram 7 SID BRT pin = 5.0V			9.3	10.8		

No.	Item		Symbol	Measurement conditions			Measurement method	Min.	Typ.	Max.	Unit
				Input pin	Conditions	Measurement point					
23	SIG CENT adjust -ment range	Min.	SL	40	Output waveform diagram 5 SIG.C pin = 5.0V	11	G output center voltage		5.2	6.2	V
24		Max.	SH		Output waveform diagram 5 SIG.C pin = 1.6V			7.6	9.0		
25	VCOM adjust -ment range	Min.	VL		VCOM CONT pin = 1.6V	22	VCOM OUT DC voltage		5.6	6.2	V
26		Max.	VH		VCOM CONT pin = 5.0V			8.0	8.6		

When there is no description in the Conditions, the pin voltages are as follows.

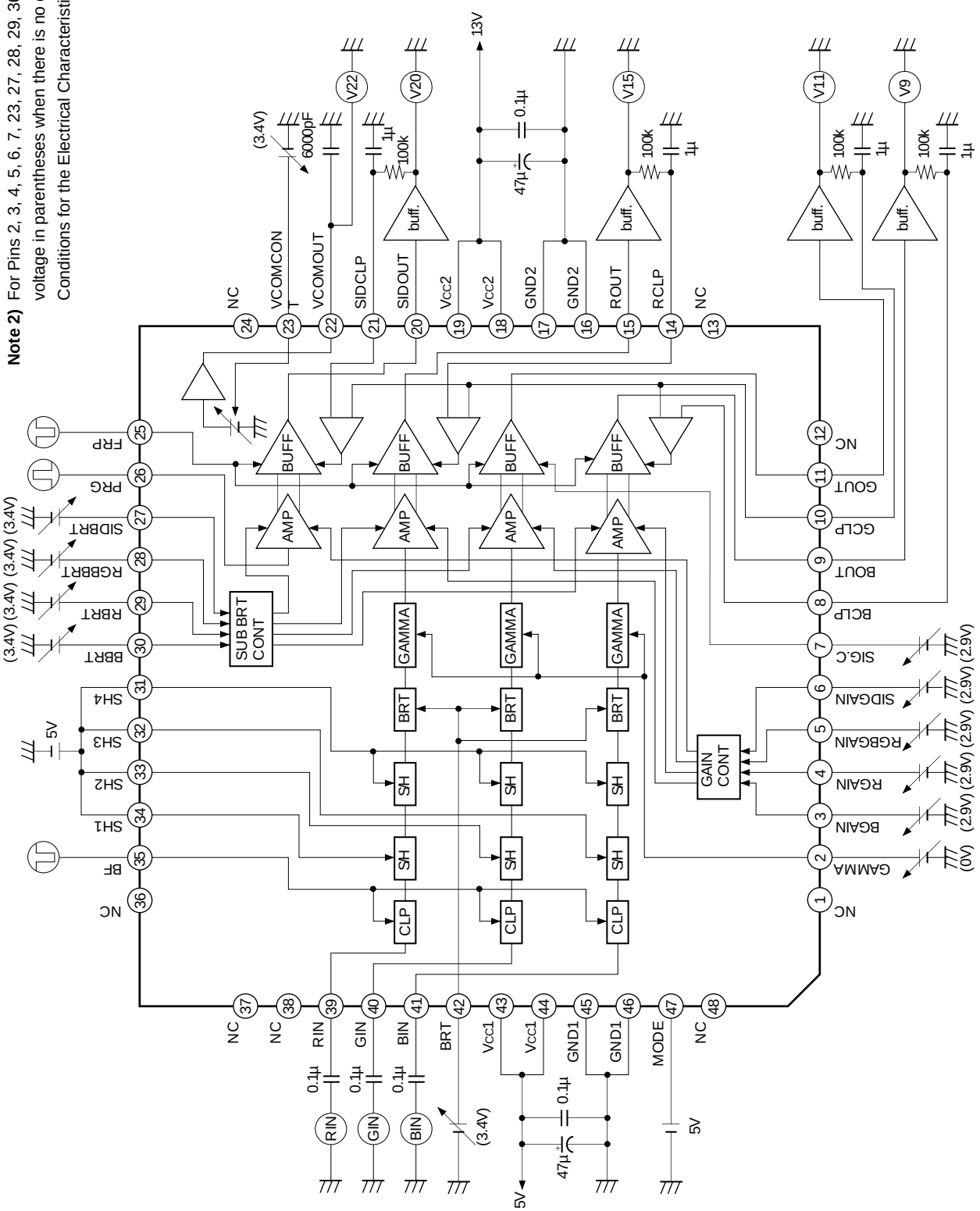
GAMMA (Pin 2) = 0V, RGB GAIN (Pin 5) R GAIN (Pin 4) B GAIN (Pin 3) = 2.9V, BRT (Pin 42)

RGB BRT (Pin 28) R BRT (Pin 29) B BRT (Pin 30)

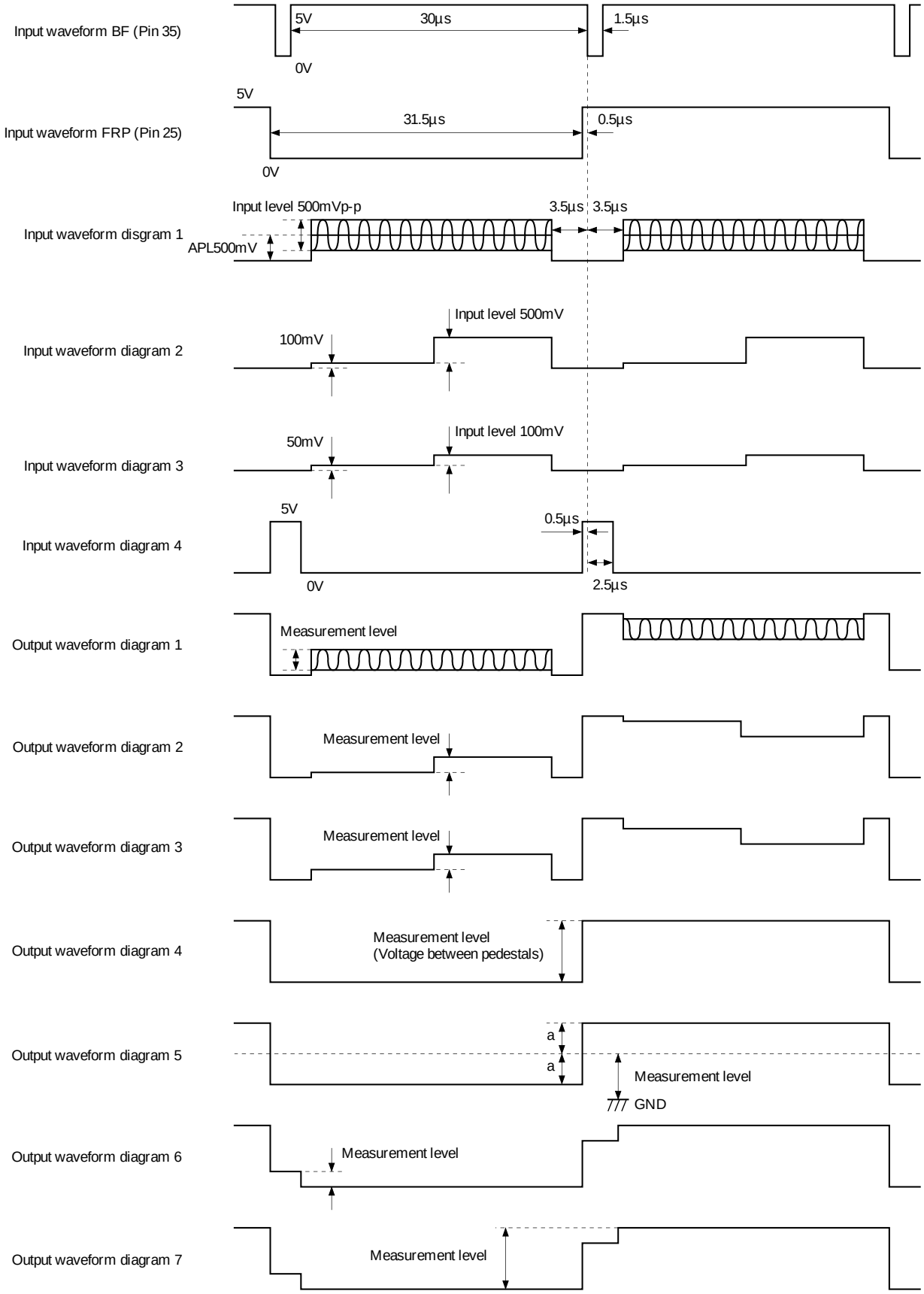
VCOM CONT (Pin 23) SIG.C (Pin 7) = 3.4V, MODE (Pin 47) = 5V, PRG (Pin 26) = 0V

Electrical Characteristics Measurement Circuit

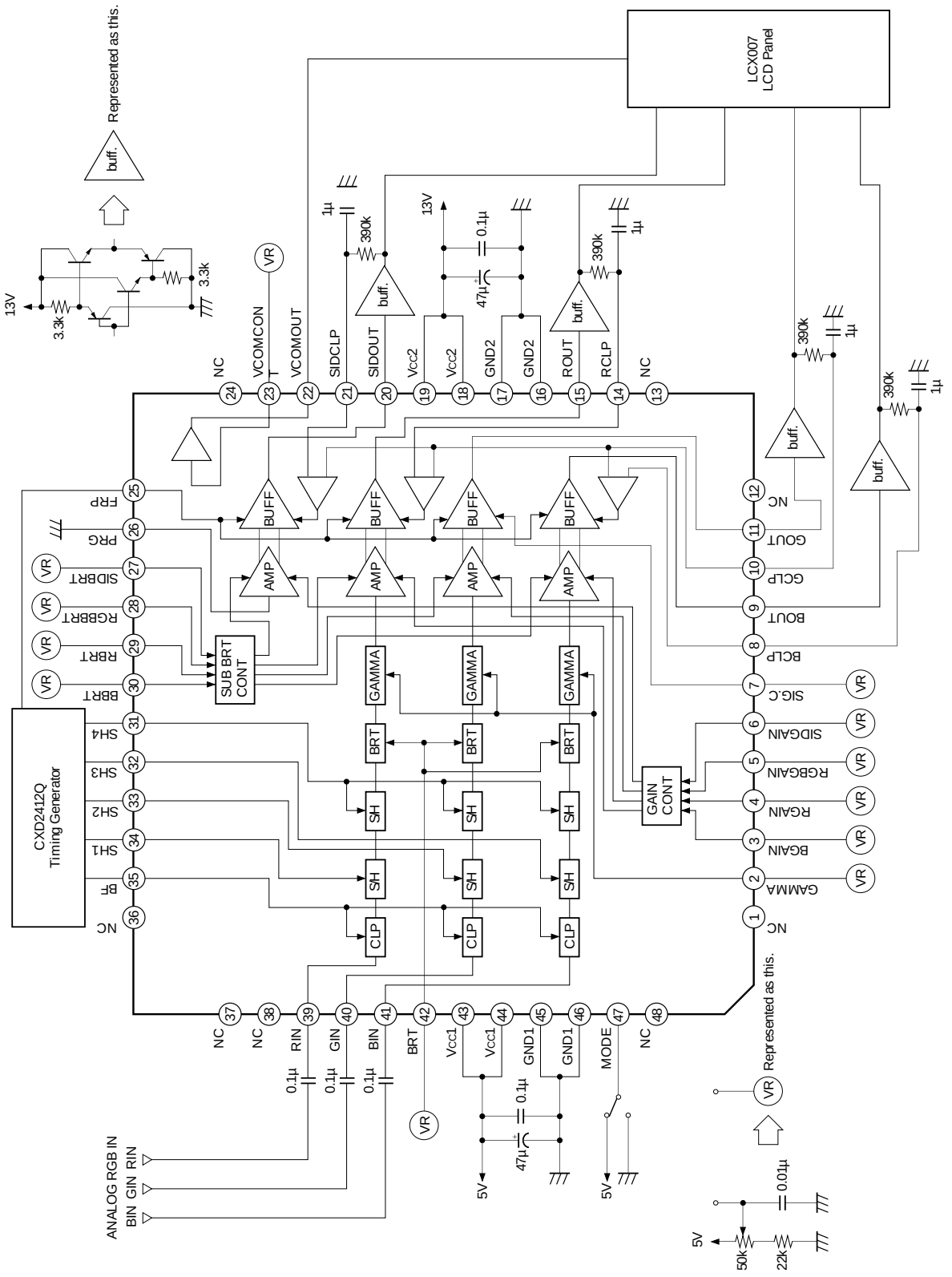
Note 1) Always input BF signal (Pin 35) and FRP signal (Pin 25).
Note 2) For Pins 2, 3, 4, 5, 6, 7, 23, 27, 28, 29, 30, and 42, apply the voltage in parentheses when there is no description in the Conditions for the Electrical Characteristics.



Measurement Circuit I/O Waveform Diagram



Application Circuit

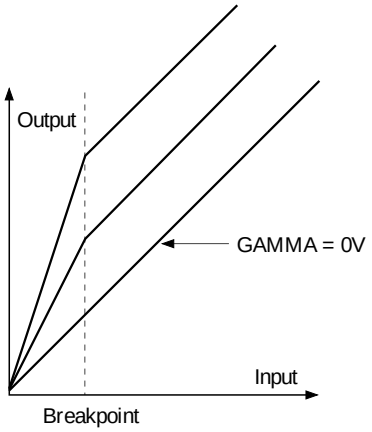


Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Description of Operation

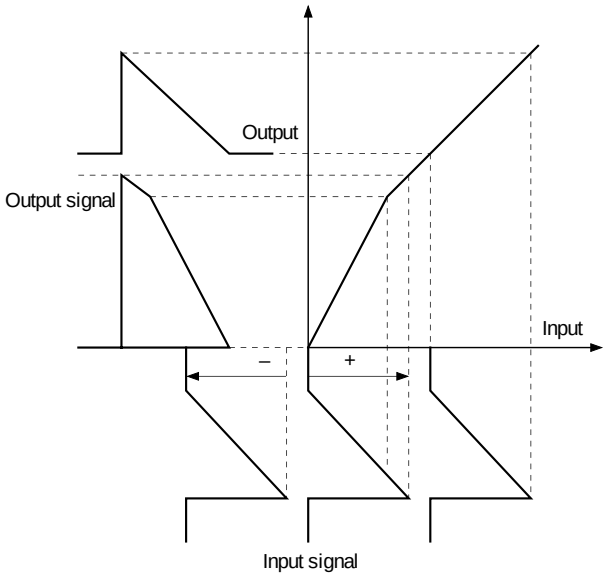
• Gamma Control

This pin controls the gain of the low brightness range as shown in the figure at right. The breakpoints are constant and only the gain is changed.
Gamma is OFF when the GAMMA pin (Pin 2) is 0V.



• BRT Control

This pin controls the pedestal of the input signal to the gamma circuit.
BRT can be controlled without changing the γ characteristics to the panel because the input bias is changed with the breakpoint for output kept constant.
In the figure at right, when the input signal pedestal is moved to the left of 0, the signal at that point is sliced.
The input signal pedestal can be varied by ±500mV (R, G, and B IN input conversion).

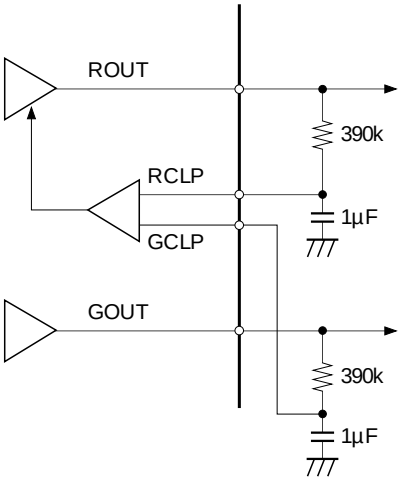


• Side Black Output (SID OUT)

The CXA1819Q outputs a side black signal for 4:3/16:9 aspect conversion.
The black level is controlled by the SID BRT pin (Pin 27).

• Output CLP

The average value of each RGB output signal and SID output signal is detected with external RC and input to the RGB CLP and SID CLP pins. Then the center voltage offsets among R, G and B outputs are reduced by feedback which equalizes the averages of G and R, B and SID outputs thus eliminating the need to adjust the center voltages among R, G and B.

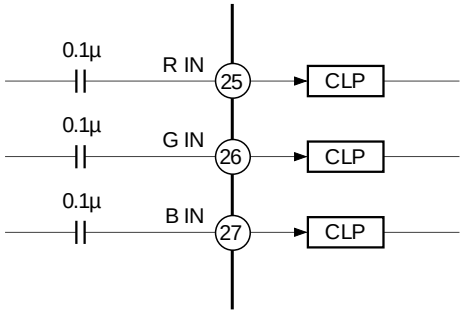


Notes on Operation

Take the following precautions when using the CXA1819Q.

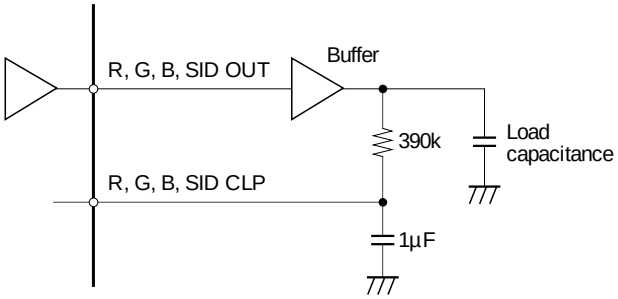
1. R, G, B IN input signal impedance

An external capacitor is used as a hold capacitor for the clamp at the input of this IC. Therefore, the input signal impedance must be sufficiently low (70Ω or less).
Note that if the impedance is too high, the characteristics may change or oscillation may tend to occur.



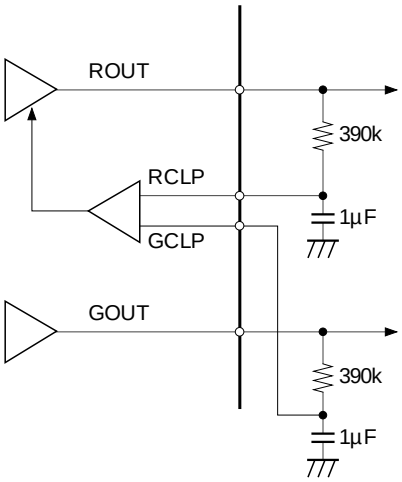
2. R, G, B SID OUT load capacitance

RGB OUT and SID OUT will tend to oscillate if a load capacitance of greater than 50pF is attached.
Therefore, when a LCD panel with an input capacitance of greater than 50pF is connected to the output, a buffer should be used as shown in the figure at right. In addition, when not using a buffer, design to keep this load capacitance from exceeding 50pF.



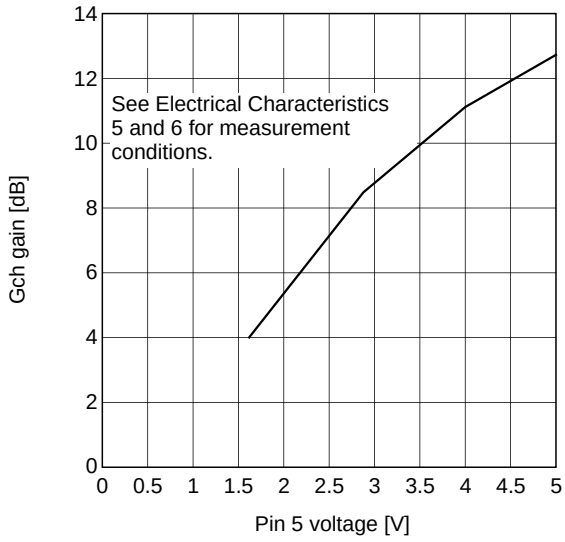
3. External capacitor at the output

The absolute value and tolerance of leak current for the average value detecting external capacitor in the figure at right should be small.
Note that if there is an offset in the leak current between R, G, B and SID, offset voltage is also generated between R, G, B and SID, of the external resistor which causes a DC offset of the output signal.

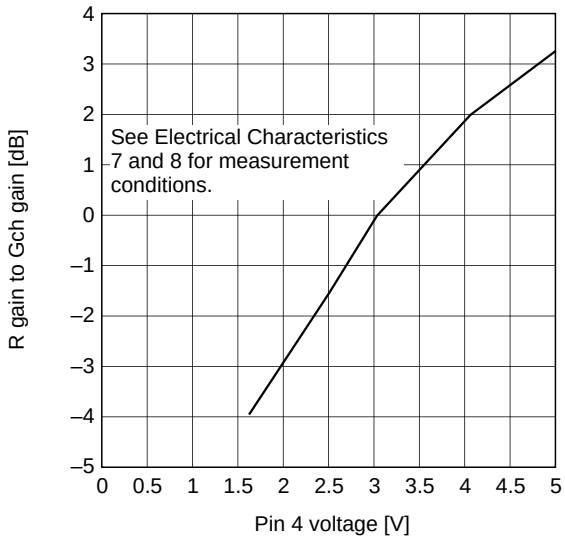


Characteristics Graphs (Vcc = 5V, 13V, Ta = 25°C)

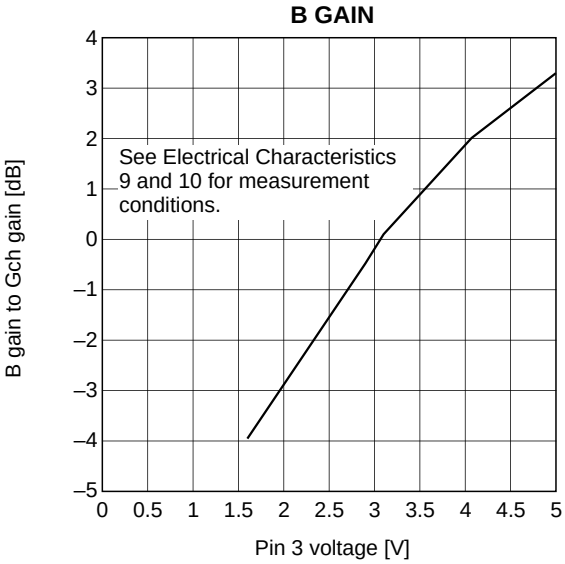
RGB GAIN



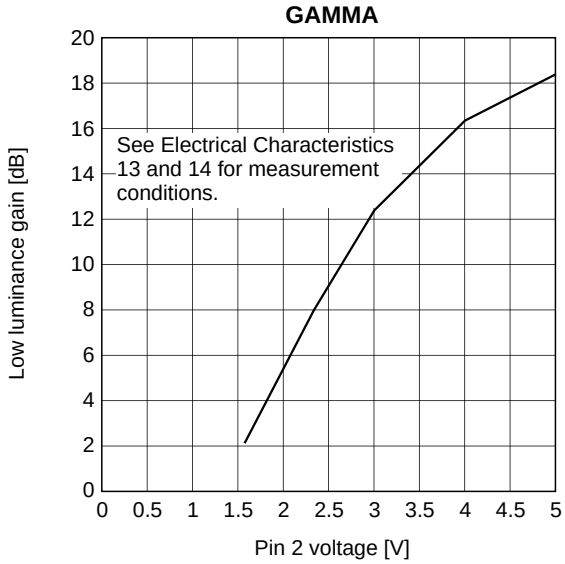
R GAIN



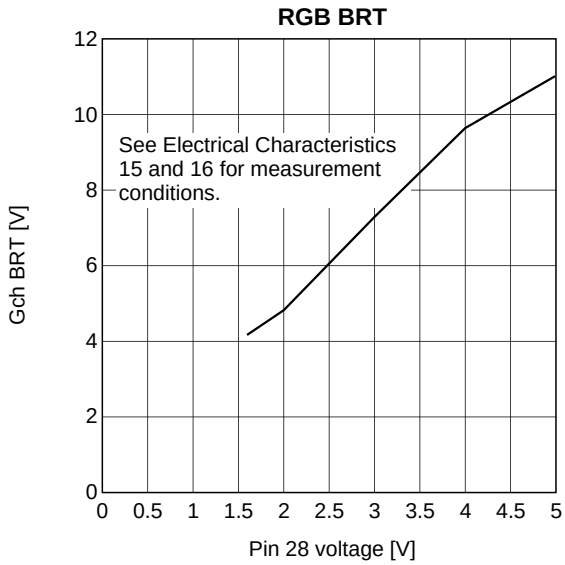
B GAIN



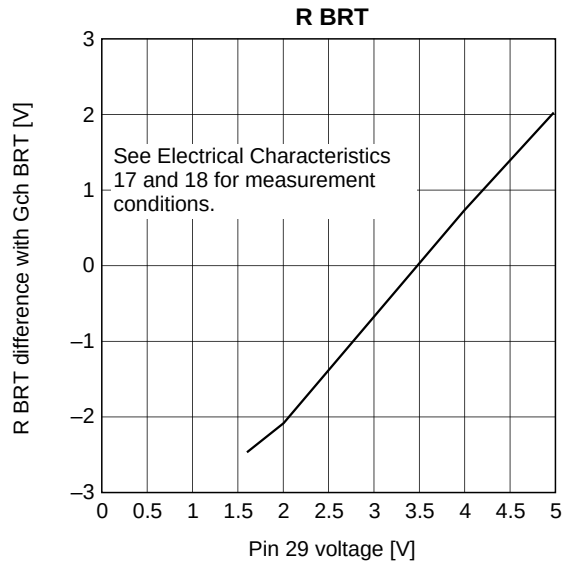
GAMMA



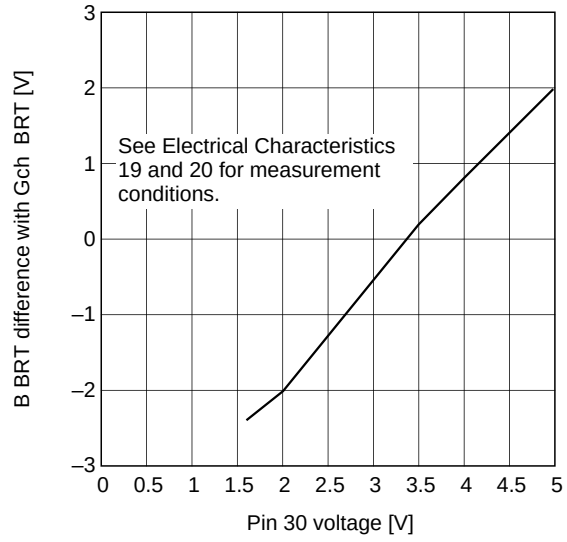
RGB BRT



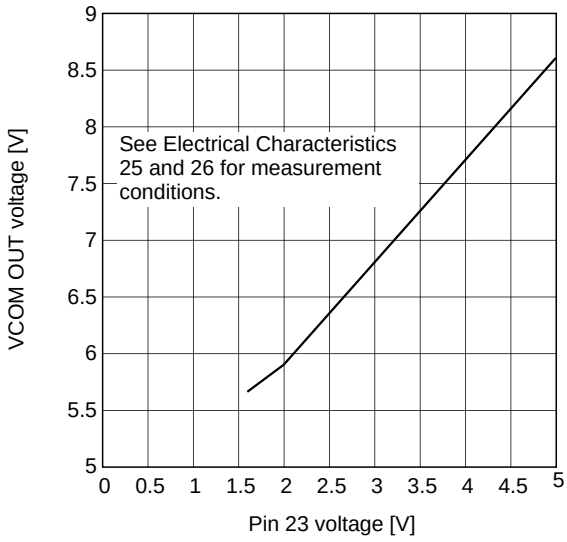
R BRT



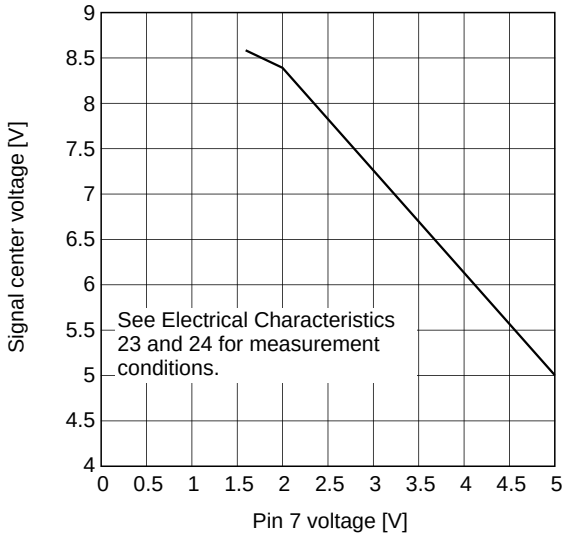
B BRT



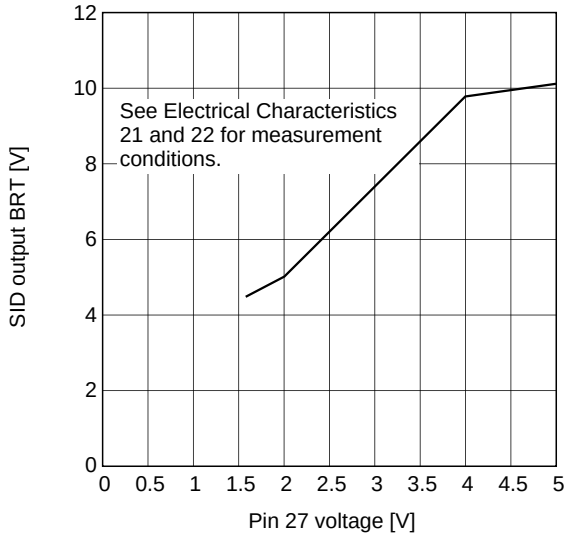
VCOM



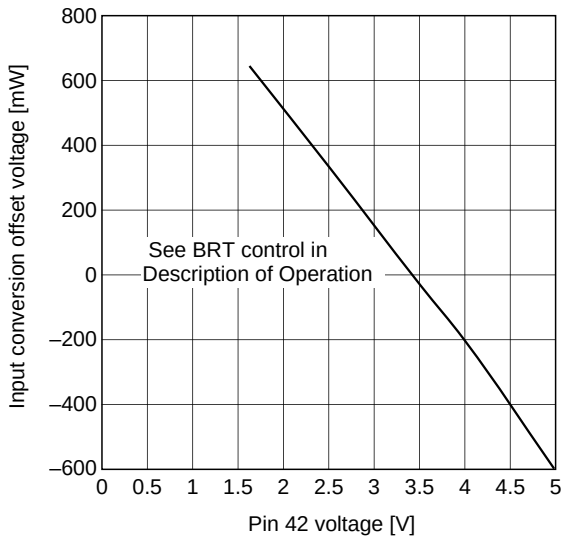
SIG.C



SID BRT

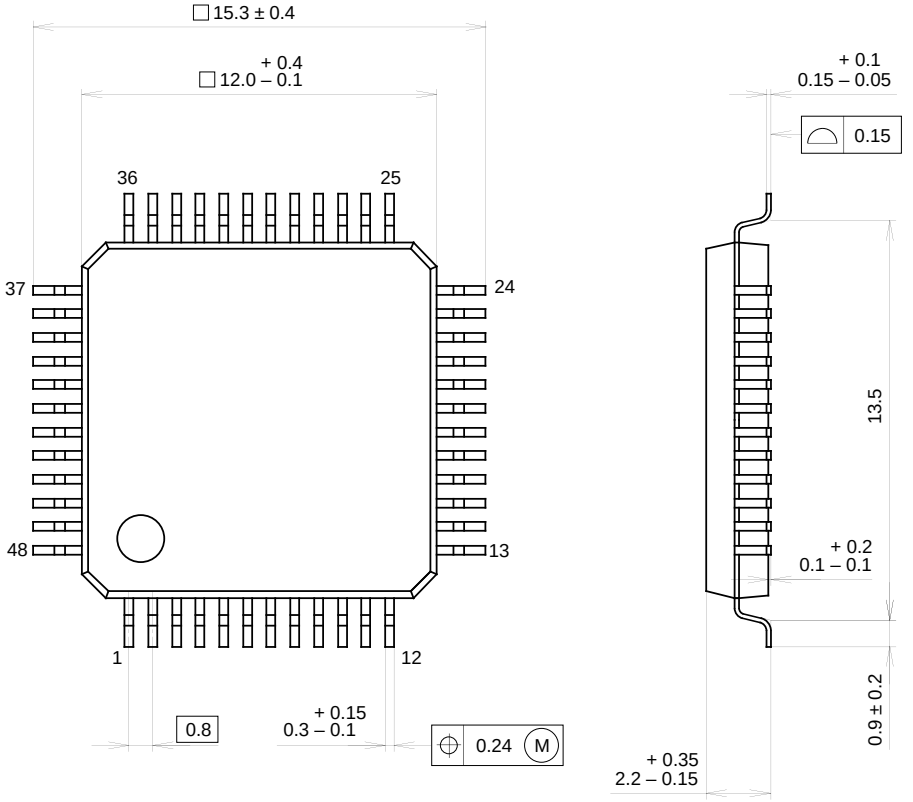


BRT



Package Outline Unit: mm

48PIN QFP (PLASTIC)



PACKAGE STRUCTURE

SONY CODE	QFP-48P-L04
EIAJ CODE	QFP048-P-1212
JEDEC CODE	————

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER / PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.7g

NOTE : PALLADIUM PLATING
This product uses S-PdPPF (Sony Spec.-Palladium Pre-Plated Lead Frame).