Integrated Device Technology, Inc.

HIGH-SPEED 3.3V 2K x 8 DUAL-PORT STATIC RAM WITH INTERRUPT

IDT71V321S/L

FEATURES:

- High-speed access
  - —Commercial: 25/35/55ns (max.)
- Low-power operation
  - —IDT71V321S
    - Active: 250mW (typ.)
    - Standby: 3.3mW (typ.)
  - —IDT71V321L
    - Active: 250mW (typ.)
    - Standby: 660µW (typ.)
- Two $\overline{INT}$ flags for port-to-port communications
- On-chip port arbitration logic
- $\overline{BUSY}$ output flag
- Fully asynchronous operation from either port
- Battery backup operation—2V data retention
- TTL-compatible, single 3.3V ±0.3V power supply
- Available in popular plastic packages

DESCRIPTION:

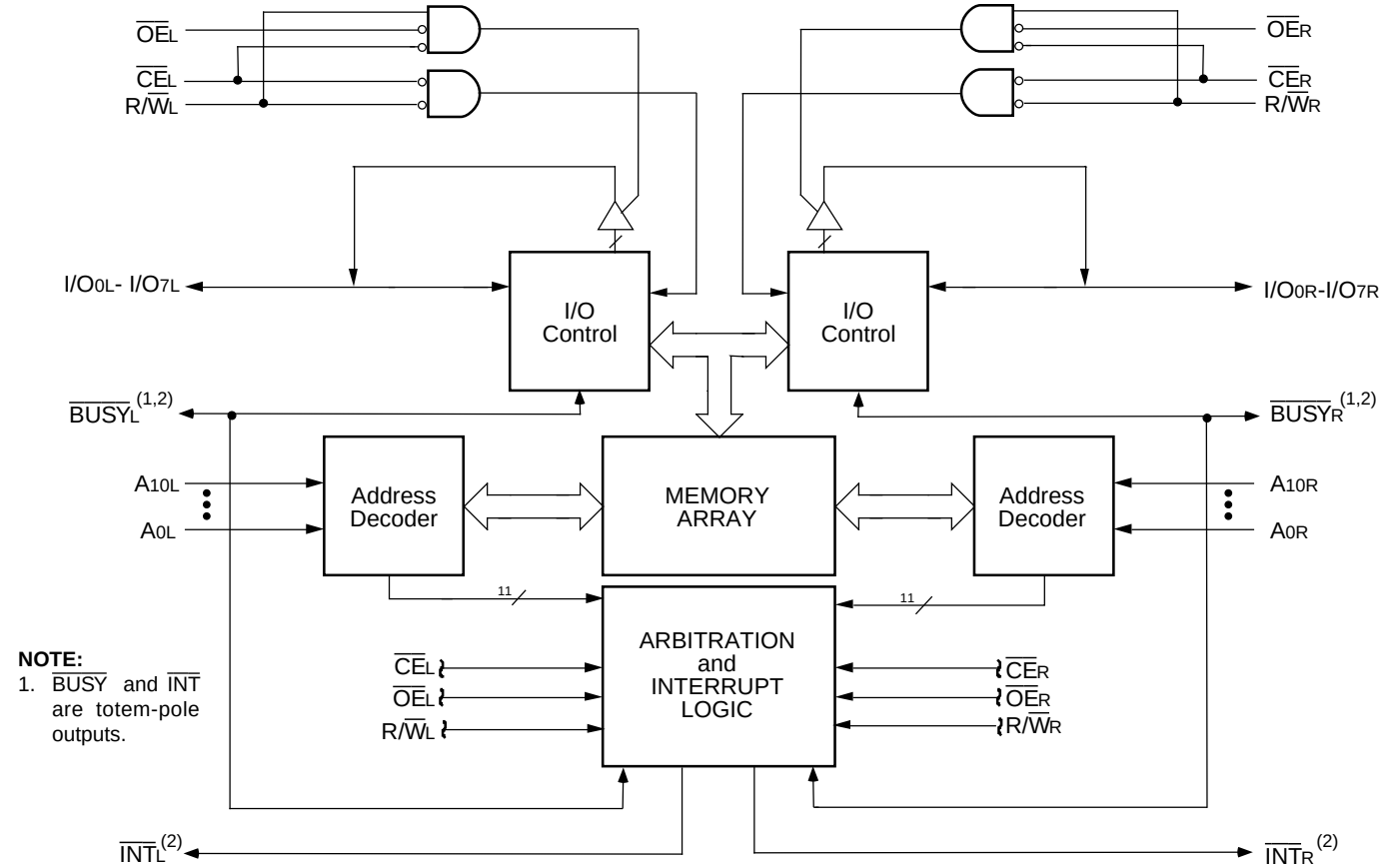
The IDT71V321 is a high-speed 2K x 8 Dual-Port Static RAMs with internal interrupt logic for interprocessor communications. The IDT71V321 is designed to be used as a stand-alone 8-bit Dual-Port RAM.

The device provides two independent ports with separate control, address, and I/O pins that permit independent, asynchronous access for reads or writes to any location in memory. An automatic power down feature, controlled by $\overline{CE}$, permits the on chip circuitry of each port to enter a very low standby power mode.

Fabricated using IDT's CMOS high-performance technology, these devices typically operate on only 250mW of power. Low-power (L) versions offer battery backup data retention capability, with each Dual-Port typically consuming 200µW from a 2V battery.

The IDT71V321 devices are packaged in a 52-pin PLCC and a 64-pin TQFP (thin plastic quad flatpack).

FUNCTIONAL BLOCK DIAGRAM

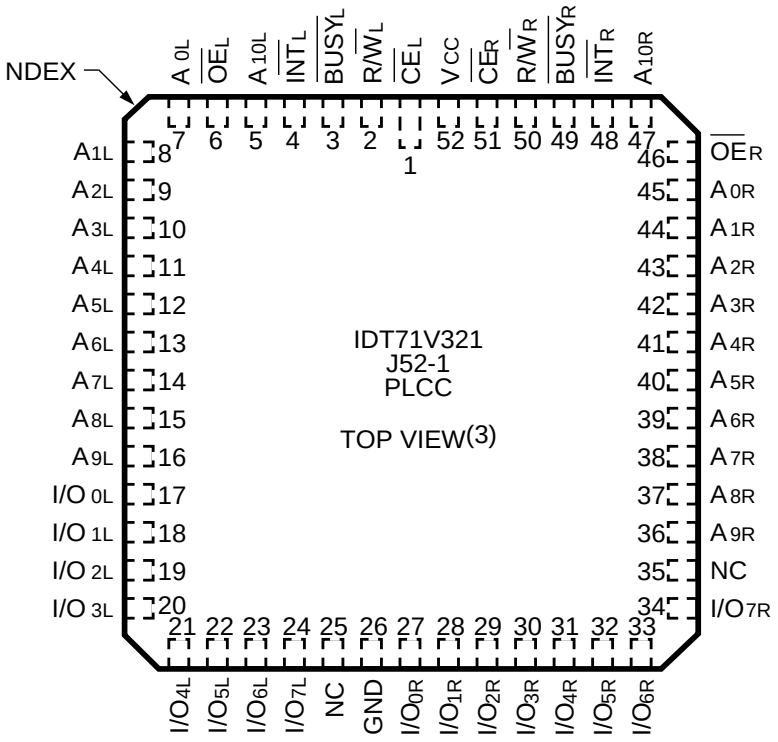


NOTE:
1. $\overline{BUSY}$ and $\overline{INT}$ are totem-pole outputs.

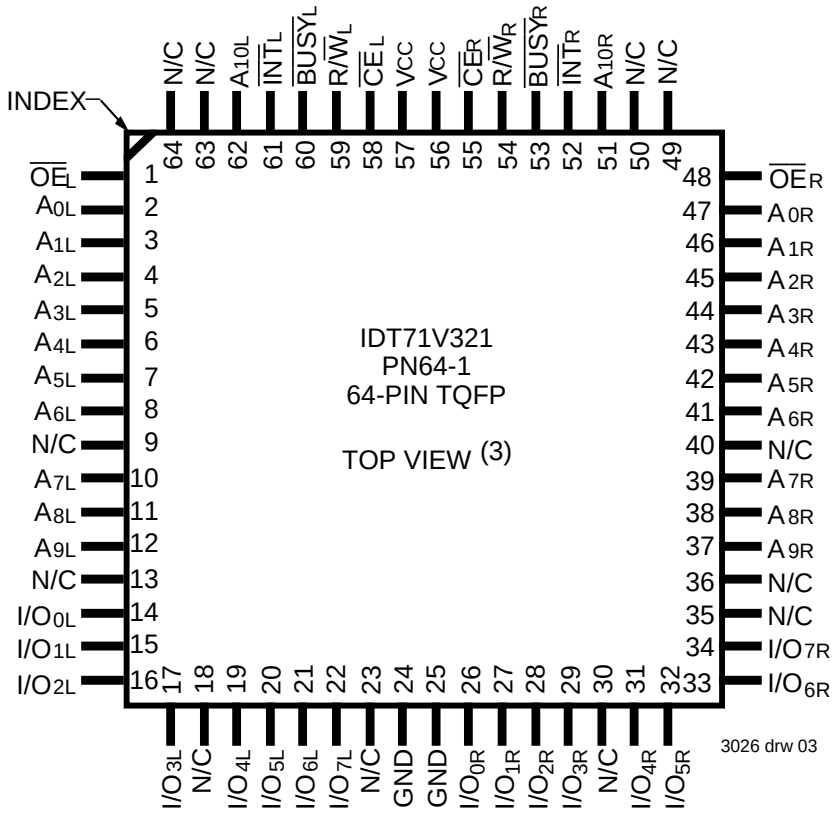
3026 drw 01

COMMERCIAL TEMPERATURE RANGE **OCTOBER 1996**

PIN CONFIGURATIONS [1,2]



3026 drw 02



3026 drw 03

NOTES:
1. All Vcc pins must be connected to the power supply.
2. All GND pins must be connected to the ground supply.
3. This text does not indicate orientation of the actual part-marking.

ABSOLUTE MAXIMUM RATINGS(1)

Symbol	Rating	Commercial	Unit
V_{TERM}(2)	Terminal Voltage with Respect to GND	–0.5 to +4.6	V
T_A	Operating Temperature	0 to +70	°C
T_{BIAS}	Temperature Under Bias	–55 to +125	°C
T_{STG}	Storage Temperature	–55 to +125	°C
I_{OUT}	DC Output Current	50	mA

3026 tbl 01

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. VTERM must not exceed Vcc + 0.5 for more than 25% of the cycle time or 10ns maximum, and is limited to ≤ 20mA for the period of VTERM ≥ Vcc + 0.5V.

RECOMMENDED OPERATING TEMPERATURE AND SUPPLY VOLTAGE

Grade	Ambient Temperature	GND	Vcc
Commercial	0°C to +70°C	0V	3.3V ± 0.3V

3026 tbl 02

RECOMMENDED DC OPERATING CONDITIONS

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage	3.0	3.3	3.6	V
GND	Supply Voltage	0	0	0	V
V_{IH}	Input High Voltage	2.0	—	Vcc+0.3	V
V_{IL}	Input Low Voltage	–0.3(1)	—	0.8	V

3026 tbl 03

NOTES:
1. V_{IL} (min.) = -1.5V for pulse width less than 20ns.
2. V_{TERM} must not exceed V_{CC} + 0.5V.

CAPACITANCE(1)

(T_A = +25°C, f = 1.0MHz) TQFP ONLY

Symbol	Parameter	Conditions(2)	Max.	Unit
C_{IN}	Input Capacitance	V_{IN} = 3dV	9	pF
C_{OUT}	Output Capacitance	V_{IN} = 3dV	10	pF

3026 tbl 04

NOTES:
1. This parameter is determined by device characterization but is not production tested.
2. 3dv references the interpolated capacitance when the input and output signals switch from 0V to 3V or from 3V to 0V.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Conditions	IDT71V321S		IDT71V321L		Unit
			Min.	Max.	Min.	Max.	
$\|I_{LI}\|$	Input Leakage Current(1)	V_{CC} = 3.6V V_{IN} = 0V to V_{CC}	—	10	—	5	µA
$\|I_{LO}\|$	Output Leakage Current	$\overline{CE}$ = V_{IH}, V_{OUT} = 0V to V_{CC} V_{CC} = 3.6V	—	10	—	5	µA
V_{OL}	Output Low Voltage (I/O_0-I/O_7)	I_{OL} = 4mA	—	0.4	—	0.4	V
V_{OH}	Output High Voltage	I_{OH} = -4mA	2.4	—	2.4	—	V

3026 tbl 05

NOTE:
1. At Vcc ≤ 2.0V input leakages are undefined.

DC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE[1] (V_{CC} = 3.3V ± 0.3V)

Symbol	Parameter	Test Condition	Version		71V321X25 Typ.[2]	71V321X25 Max.	71V321X35 Typ.[2]	71V321X35 Max.	71V321X55 Typ.[2]	71V321X55 Max.	Unit
I_{CC}	Dynamic Operating Current (Both Ports Active)	$\overline{CE}$ = V_{IL}, Outputs Open $\overline{SEM}$ = V_{IH} f = f_{MAX}[3]	COM'L.	S L	75 75	150 120	75 75	145 115	75 75	135 105	mA
I_{SB1}	Standby Current (Both Ports — TTL Level Inputs)	$\overline{CE}_R$ = $\overline{CE}_L$ = V_{IH} $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH} f = f_{MAX}[3]	COM'L.	S L	20 20	50 35	20 20	50 35	20 20	50 35	mA
I_{SB2}	Standby Current (One Port — TTL Level Inputs)	$\overline{CE}_{"A"}$ = V_{IL} and $\overline{CE}_{"B"}$ = V_{IH}[5] Active Port Outputs Open, f = f_{MAX}[3] $\overline{SEM}_R$ = $\overline{SEM}_L$ = V_{IH}	COM'L.	S L	30 30	105 75	30 30	100 70	30 30	90 60	mA
I_{SB3}	Full Standby Current (Both Ports — All CMOS Level Inputs)	Both Ports $\overline{CE}_L$ and $\overline{CE}_R \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V, f = 0[4] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V	COM'L.	S L	1.0 0.2	5.0 3.0	1.0 0.2	5.0 3.0	1.0 0.2	5.0 3.0	mA
I_{SB4}	Full Standby Current (One Port — All CMOS Level Inputs)	$\overline{CE}_{"A"} \leq$ 0.2V and $\overline{CE}_{"B"} \geq V_{CC}$ - 0.2V[5] $\overline{SEM}_R$ = $\overline{SEM}_L \geq V_{CC}$ - 0.2V $V_{IN} \geq V_{CC}$ - 0.2V or $V_{IN} \leq$ 0.2V Active Port Outputs Open f = f_{MAX}[3]	COM'L.	S L	30 30	90 75	30 30	85 70	30 30	75 60	mA

NOTES: 3026 tbl 06

1. "X" in part numbers indicates power rating (S or L).
2. V_{CC} = 3.3V, T_A = +25°C, and are not production tested. I_{CCDC} = 70mA (Typ.)
3. At f = f_{MAX}, address and control lines (except Output Enable) are cycling at the maximum frequency read cycle of 1 / t_{RC}, and using "AC Test Conditions" of input levels of GND to 3V.
4. f = 0 means no address or control lines change.
5. Port "A" may be either left or right port. Port "B" is the opposite from port "A".

DATA RETENTION CHARACTERISTICS (L Version Only)

Symbol	Parameter	Test Conditions		71V321L Min.	71V321L Typ.[1]	71V321L Max.	Unit
VDR	VCC for Data Retention			2.0	—	0	V
ICCDR	Data Retention Current	VCC = 2.0V, $\overline{CE} \geq$ VCC - 0.2V	COM'L.	—	100	1500	µA
tCDR[3]	Chip Deselect to Data Retention Time	VIN ≥ VCC - 0.2V or VIN≤ 0.2V		0	—	—	ns
tR[3]	Operation Recovery Time			tRC[2]	—	—	ns

NOTES: 3026 tbl 07

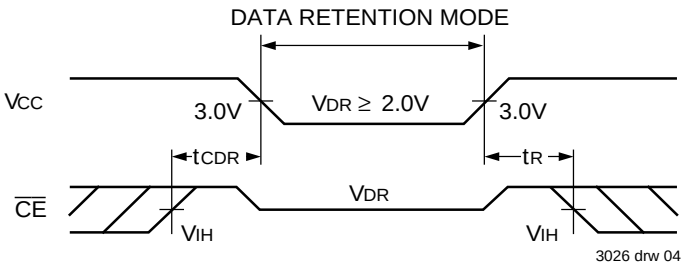
1. V_{CC} = 2V, T_A = +25°C, and is not production tested.
2. t_{RC} = Read Cycle Time.
3. This parameter is guaranteed by device characterization but not production tested.

AC TEST CONDITIONS

Input Pulse Levels	GND to 3.0V
Input Rise/Fall Times	5ns
Input Timing Reference Levels	1.5V
Output Reference Levels	1.5V
Output Load	Figures 1and 2

3026 tbl 08

DATA RETENTION WAVEFORM



3026 drw 04

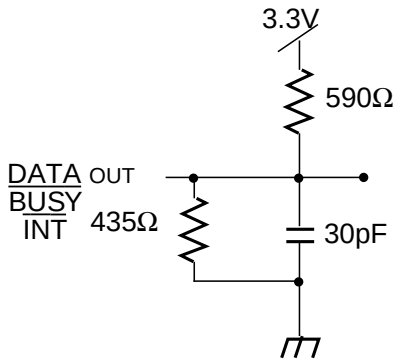
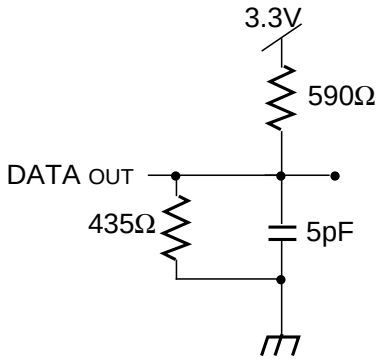


Figure 1. AC Output Test Load



3026 drw 05

Figure 2. Output Test Load (For tHZ, tLZ, twz and tow)

* Including scope and jig.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(3)

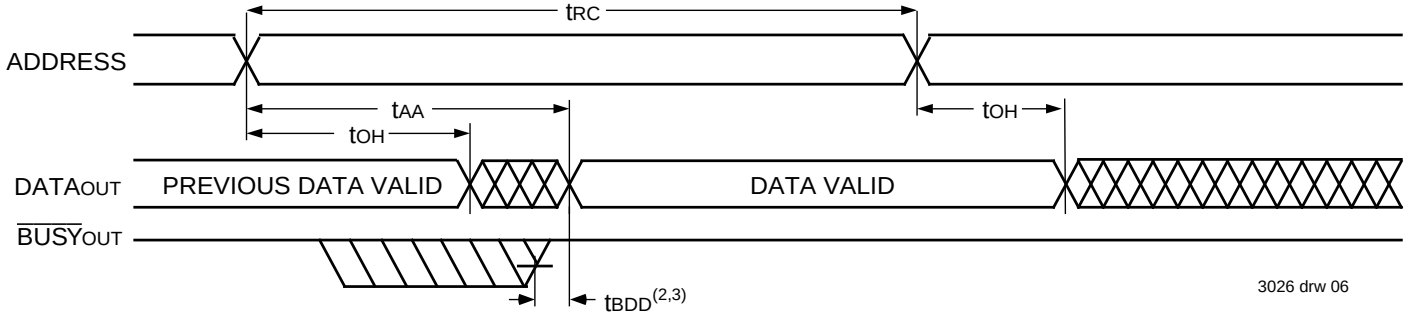
Symbol	Parameter	71V321X25 Min.	71V321X25 Max.	71V321X35 Min.	71V321X35 Max.	71V321X55 Min.	71V321X55 Max.	Unit
READ CYCLE								
tRC	Read Cycle Time	25	—	35	—	55	—	ns
tAA	Address Access Time	—	25	—	35	—	55	ns
tACE	Chip Enable Access Time	—	25	—	35	—	55	ns
tAOE	Output Enable Access Time	—	12	—	20	—	25	ns
tOH	Output Hold from Address Change	3	—	3	—	3	—	ns
tLZ	Output Low-Z Time(1, 2)	0	—	0	—	0	—	ns
tHZ	Output High-Z Time(1, 2)	—	12	—	15	—	30	ns
tPU	Chip Enable to Power Up Time(2)	0	—	0	—	0	—	ns
tPD	Chip Disable to Power Down Time(2)	—	50	—	50	—	50	ns

NOTES:

3026 tbl 09

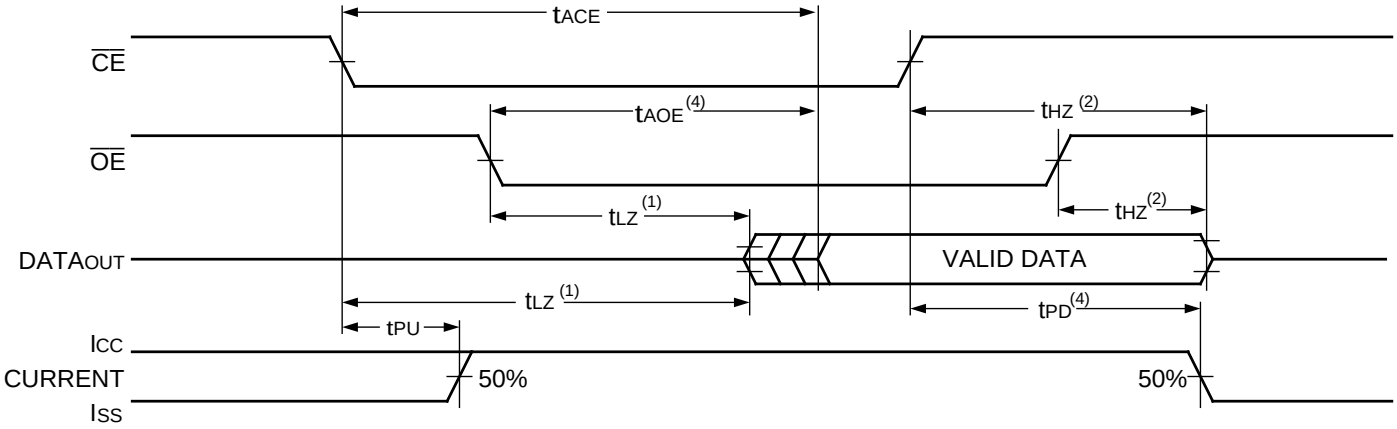
1. Transition is measured ±200mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF READ CYCLE NO. 1, EITHER SIDE(1)



NOTES:
1. R/$\overline{W}$ = VIH, $\overline{CE}$ = VIL, and is $\overline{OE}$ = VIL. Address is valid prior to the coincidental with $\overline{CE}$ transition Low.
2. tBDD delay is required only in case where the opposite is port is completing a write operation to same the address location. For simultanious read operations $\overline{BUSY}$ has no relationship to valid output data.
3. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

TIMING WAVEFORM OF READ CYCLE NO. 2, EITHER SIDE(3)



NOTES:
1. Timing depends on which signal is asserted last, $\overline{OE}$ or $\overline{CE}$.
2. Timing depends on which signal is deaserted first, $\overline{OE}$ or $\overline{CE}$.
3. R/$\overline{W}$ = VIH, and the address is valid prior to other coincidental with $\overline{CE}$ transition Low.
4. Start of valid data depends on which timing becomes effective last tAOE, tACE, tAA, and tBDD.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE(4)

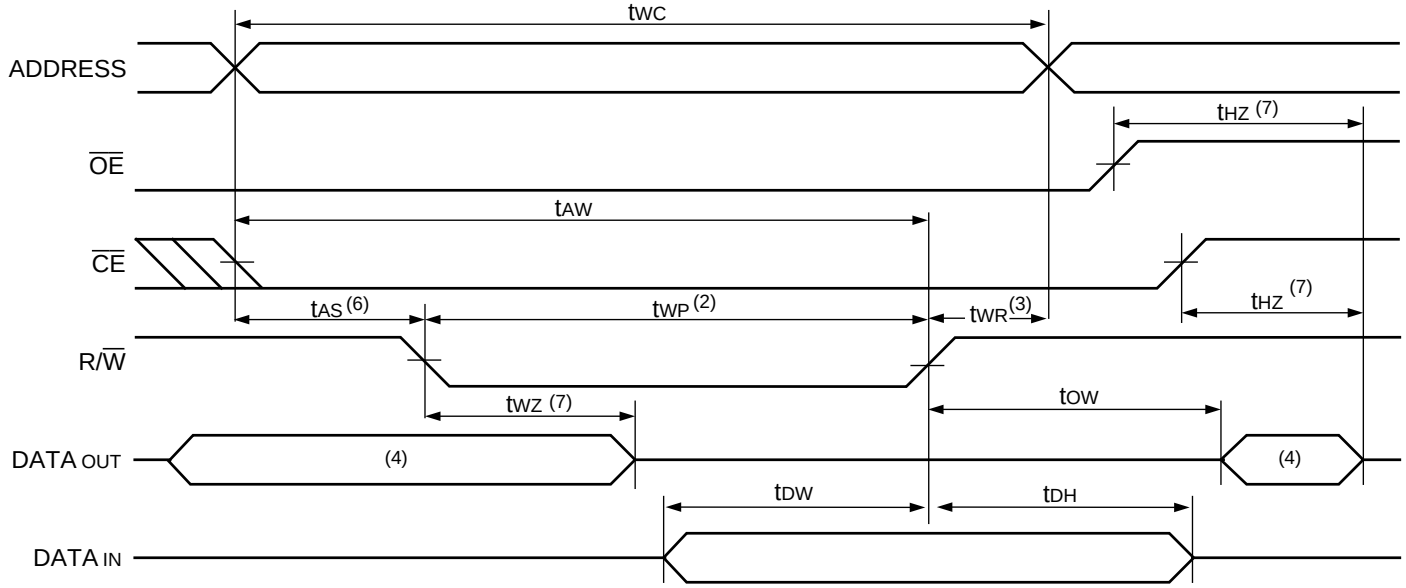
Symbol	Parameter	71V321X25		71V321X35		71V321X55		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
WRITE CYCLE								
t_{WC}	Write Cycle Time	25	—	35	—	55	—	ns
t_{EW}	Chip Enable to End-of-Write	20	—	30	—	40	—	ns
t_{AW}	Address Valid to End-of-Write	20	—	30	—	40	—	ns
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WP}	Write Pulse Width	20	—	30	—	40	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{DW}	Data Valid to End-of-Write	12	—	20	—	20	—	ns
t_{HZ}	Output High-Z Time(1, 2)	—	12	—	15	—	30	ns
t_{DH}	Data Hold Time(3)	0	—	0	—	0	—	ns
t_{WZ}	Write Enable to Output in High-Z(1, 2)	—	15	—	15	—	30	ns
t_{OW}	Output Active from End-of-Write(1, 2)	0	—	0	—	0	—	ns

NOTES:

3026 tbl 10

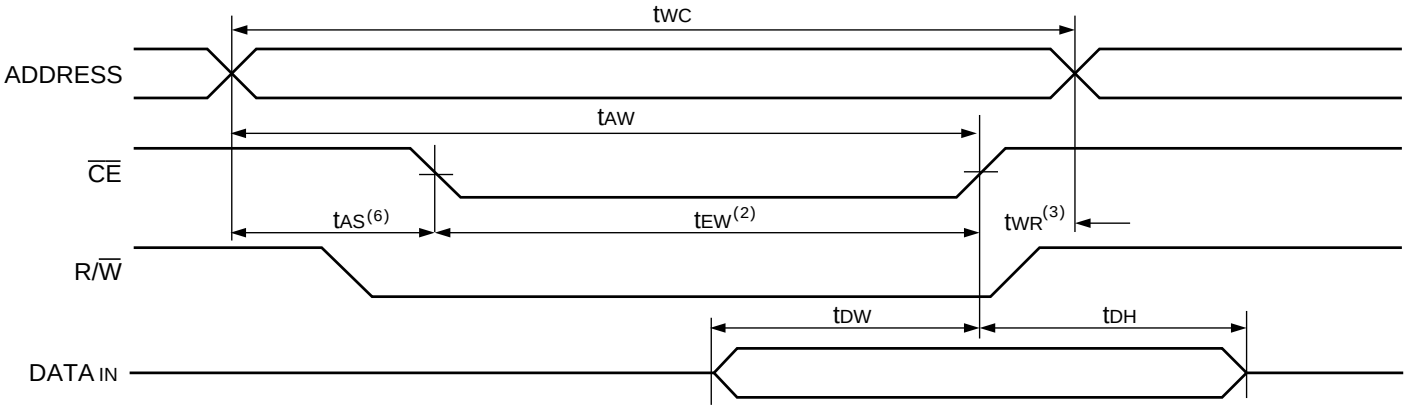
1. Transition is measured ±200mV from Low or High-impedance voltage with Output Test Load (Figure 2).
2. This parameter is guaranteed by device characterization, but is not production tested.
3. The specification for t_{DH} must be met by the device supplying write data to the RAM under all operating conditions. Although t_{DH} and t_{OW} values will vary over voltage and temperature, the actual t_{DH} will always be smaller than the actual t_{OW}.
4. "X" in part numbers indicates power rating (S or L).

TIMING WAVEFORM OF WRITE CYCLE NO. 1,(R/$\overline{W}$ CONTROLLED TIMING) (1,5,8)



3026 drw 08

TIMING WAVEFORM OF WRITE CYCLE NO. 2, $\overline{CE}$ CONTROLLED TIMING(1,5)



3026 drw 09

NOTES:
1. R/$\overline{W}$ or $\overline{CE}$ must be High during all address transitions.
2. A write occurs during the overlap (t_{EW} or t_{WP}) of $\overline{CE}$ = V_{IL} and R/$\overline{W}$= V_{IL}.
3. t_{WR} is measured from the earlier of $\overline{CE}$ or R/$\overline{W}$ going High to the end of the write cycle.
4. During this period, the I/O pins are in the output state and input signals must not be applied.
5. If the $\overline{CE}$ Low transition occurs simultaneously with or after the R/$\overline{W}$ Low transition, the outputs remain in the High-impedance state.
6. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
7. This parameter is determined be device characterization, but is not production tested. Transition is measured +/- 500mV from steady state with the Output Test Load (Figure 2).
8. If $\overline{OE}$ is Low during a R/$\overline{W}$ controlled write cycle, the write pulse width must be the larger of t_{WP} or (t_{WZ} + t_{DW}) to allow the I/O drivers to turn off data to be placed on the bus for the required t_{DW}. If $\overline{OE}$ is High during a R/$\overline{W}$ controlled write cycle, this requirement does not apply and the write pulse can be as short as the specified t_{WP}.

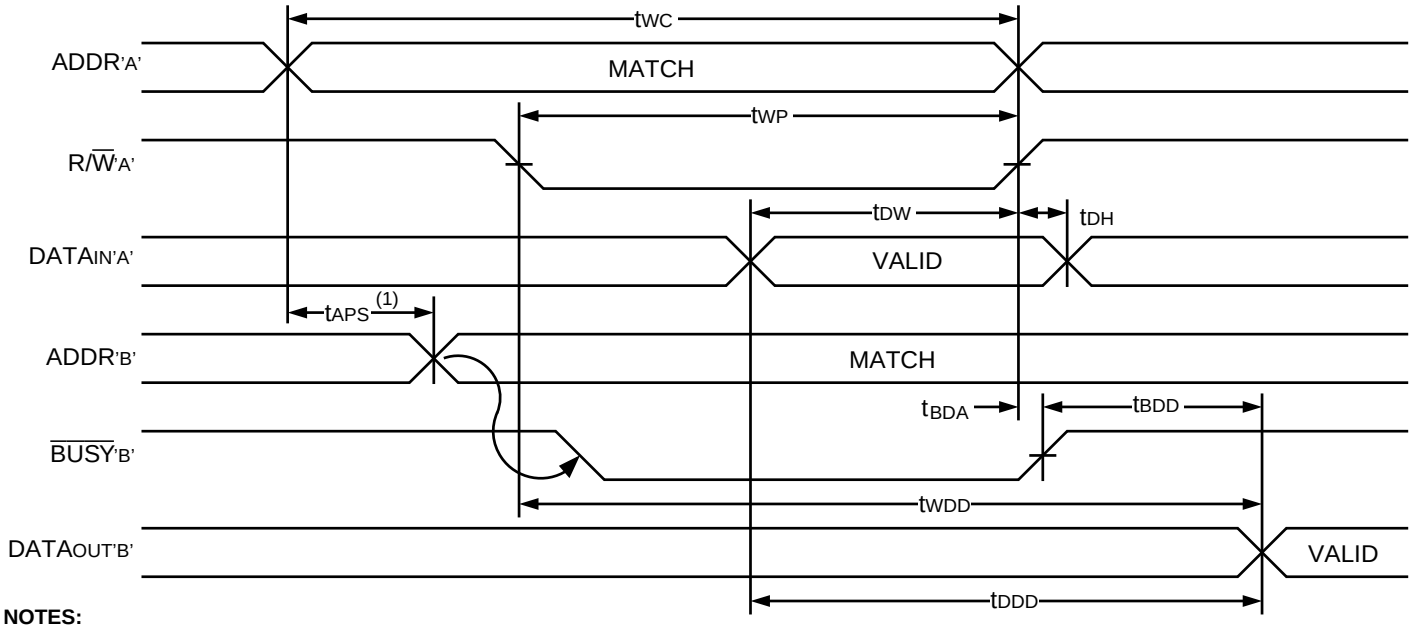
AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(6)

Symbol	Parameter	71V321X25 Min.	71V321X25 Max.	71V321X35 Min.	71V321X35 Max.	71V321X55 Min.	71V321X55 Max.	Unit
BUSY TIMING (M/$\overline{S}$ = V_{IH})								
t_{BAA}	$\overline{BUSY}$ Access Time from Address Match	—	20	—	20	—	30	ns
t_{BDA}	$\overline{BUSY}$ Disable Time from Address Not Matched	—	20	—	20	—	30	ns
t_{BAC}	$\overline{BUSY}$ Access Time from Chip Enable Low	—	20	—	20	—	30	ns
t_{BDC}	$\overline{BUSY}$ Disable Time from Chip Enable High	—	20	—	20	—	30	ns
t_{APS}	Arbitration Priority Set-up Time(2)	5	—	5	—	5	—	ns
t_{BDD}	$\overline{BUSY}$ Disable to Valid Data(3)	—	30	—	30	—	45	ns
t_{WDD}	Write Pulse to Delay Data(1)	—	50	—	60	—	80	ns
t_{DDD}	Write Pulse to Delay Data(1)	—	35	—	45	—	65	ns

NOTES:
3026 tbl 11

1. Port-to-port delay through RAM cells from writing port to reading port, refer to "Timing Waveform of Write with Port-to-Port Read and $\overline{BUSY}$".
2. To ensure that the earlier of the two ports wins.
3. t_{BDD} is a calculated parameter and is the greater of 0, $t_{WDD} - t_{WP}$ (actual), or $t_{DDD} - t_{DW}$ (actual).
4. To ensure that the write cycle is inhibited on port "B" during contention on port "A".
5. To ensure that a write cycle is completed on port "B" after contention on port "A".
6. "X" in part numbers indicates power rating (S or L).

TIMING WAVE FORM OF WRITE WITH PORT-TO-PORT READ WITH $\overline{BUSY}$(1,2,3)

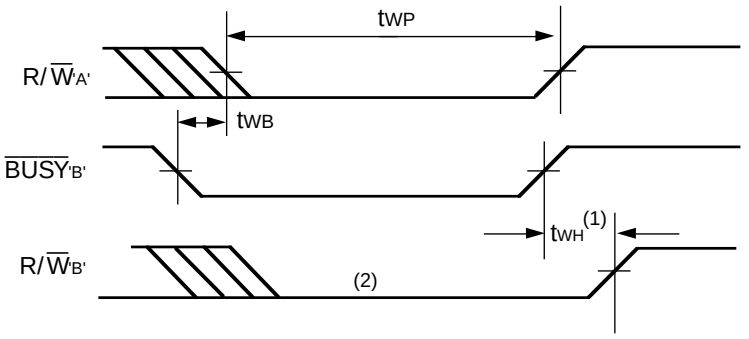


NOTES:

1. To ensure that the earlier of the two ports wins.
2. $\overline{CE}_L = \overline{CE}_R = V_{IL}$
3. $\overline{OE} = V_{IL}$ for the reading port.
4. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port 'B' is opposite from port 'A'.

3026 drw 10

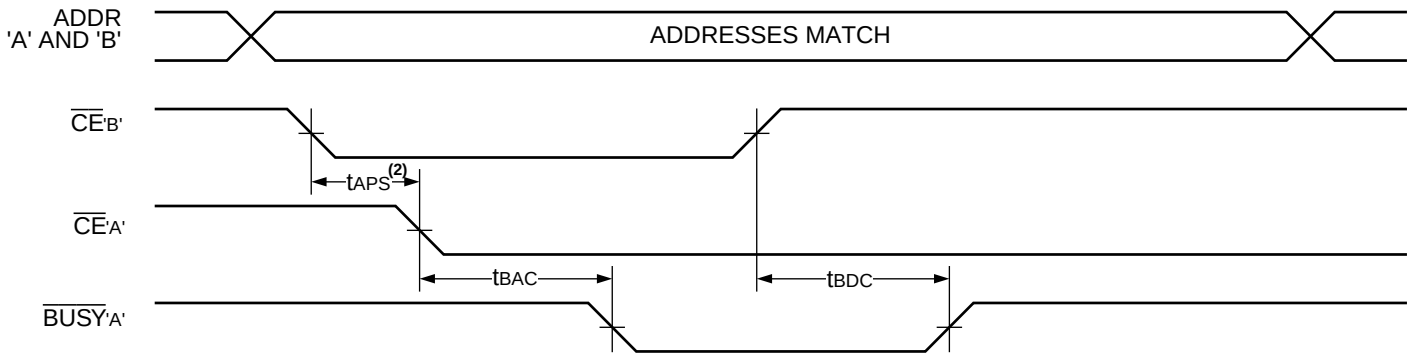
TIMING WAVEFORM OF WRITE WITH $\overline{BUSY}$ (3)



3026 drw 11

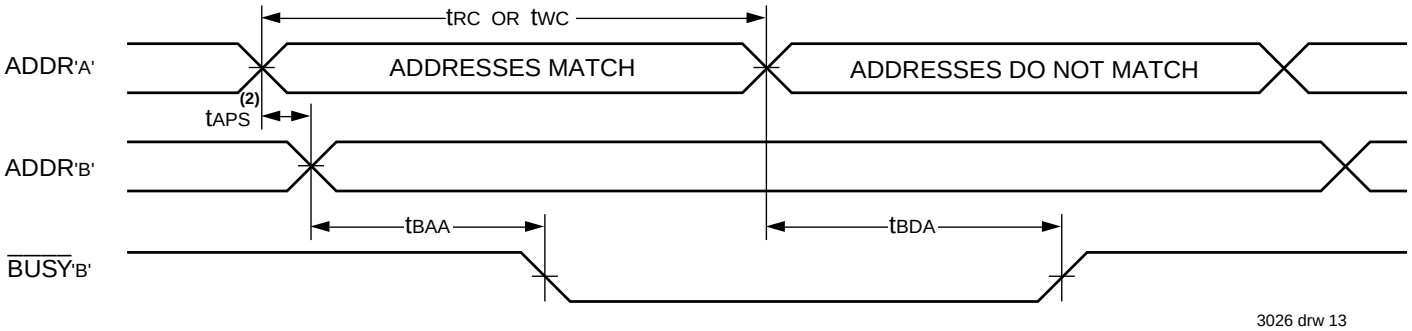
NOTES:
1. tWH must be met for $\overline{BUSY}$.
2. $\overline{BUSY}$ is asserted on port 'B' blocking R/$\overline{W}$B', until $\overline{BUSY}$'B' goes High.
3. All timing is the same for the left and right ports. Port 'A' may be either the left or right port. Port 'B' is opposite from port 'A'.

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY $\overline{CE}$ TIMING (1)



3026 drw 12

TIMING WAVEFORM OF BUSY ARBITRATION CONTROLLED BY ADDRESS MATCH TIMING (1)



3026 drw 13

NOTES:
1. All timing is the same for left and right ports. Port 'A' may be either left or right port. Port 'B' is the opposite from port 'A'.
2. If tAPS is not satisified, the $\overline{BUSY}$ will be asserted on one side or the other, but there is no guarantee on which side $\overline{BUSY}$ will be asserted.

AC ELECTRICAL CHARACTERISTICS OVER THE OPERATING TEMPERATURE AND SUPPLY VOLTAGE RANGE(1)

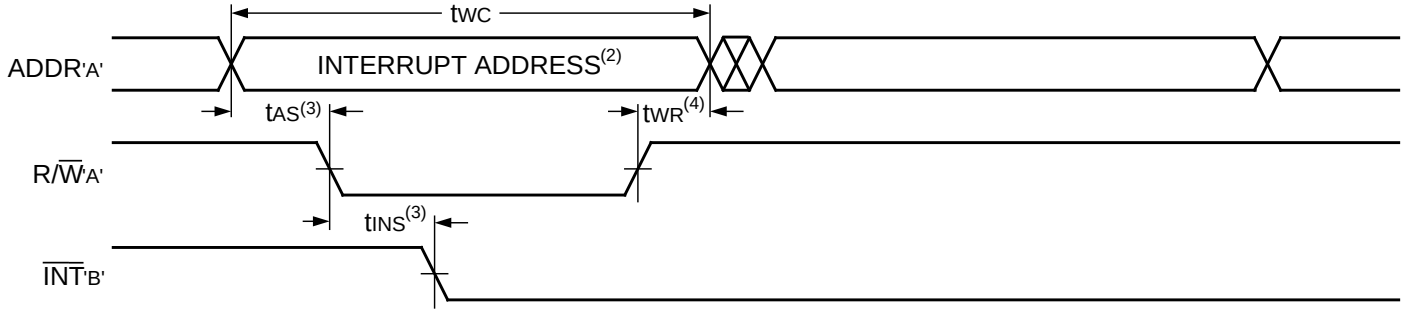
Symbol	Parameter	71V321X25 Min.	71V321X25 Max.	71V321X35 Min.	71V321X35 Max.	71V321X55 Min.	71V321X55 Max.	Unit
INTERRUPT TIMING								
t_{AS}	Address Set-up Time	0	—	0	—	0	—	ns
t_{WR}	Write Recovery Time	0	—	0	—	0	—	ns
t_{INS}	Interrupt Set Time	—	25	—	25	—	45	ns
t_{INR}	Interrupt Reset Time	—	25	—	25	—	45	ns

NOTE:
1. "X" in part numbers indicates power rating (S or L).

3026 tbl 12

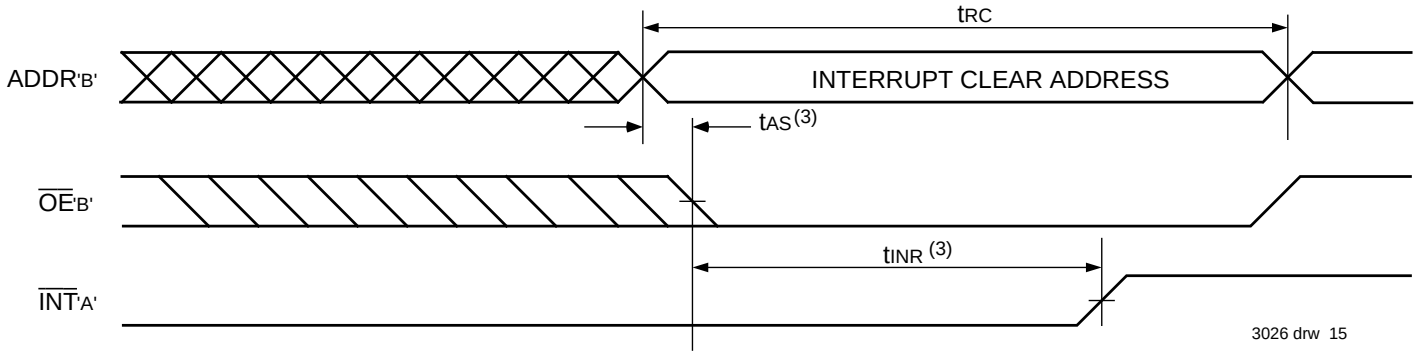
TIMING WAVEFORM OF INTERRUPT MODE

$\overline{INT}$ SETS



3026 drw 14

$\overline{INT}$ CLEARS



3026 drw 15

NOTES:.
1. All timing is the same for left and right ports. Port 'A' may be either left or right port. Port 'B' is the opposite from port 'A'.
2. See Interrupt Truth Table.
3. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is asserted last.
4. Timing depends on which enable signal ($\overline{CE}$ or R/$\overline{W}$) is de-asserted first.

TRUTH TABLES

TABLE I — NON-CONTENTION READ/WRITE CONTROL(4)

Left or Right Port(1)				
R/$\overline{W}$	$\overline{CE}$	$\overline{OE}$	D_{0-7}	Function
X	H	X	Z	Port Disabled and in Power-Down Mode, I_{SB2} or I_{SB4}
X	H	X	Z	$\overline{CE}_R = \overline{CE}_L = V_{IH}$, Power-Down Mode, I_{SB1} or I_{SB3}
L	L	X	$DATA_{IN}$	Data on Port Written Into Memory(2)
H	L	L	$DATA_{OUT}$	Data in Memory Output on Port(3)
H	L	H	Z	High-impedance Outputs

3026 tbl 13

NOTES:
1. $A_{0L} - A_{10L} \neq A_{0R} - A_{10R}$.
2. If $\overline{BUSY} = V_{IL}$, data is not written.
3. If $\overline{BUSY} = V_{IL}$, data may not be valid, see t_{WDD} and t_{DDD} timing.
4. 'H' = V_{IH}, 'L' = V_{IL}, 'X' = DON'T CARE, 'Z' = High-impedance.

TABLE II — INTERRUPT FLAG(1,4)

Left Port					Right Port					
R/$\overline{W}_L$	$\overline{CE}_L$	$\overline{OE}_L$	$A_{10L} - A_{0L}$	$\overline{INT}_L$	R/$\overline{W}_R$	$\overline{CE}_R$	$\overline{OE}_R$	$A_{10L} - A_{0R}$	$\overline{INT}_R$	Function
L	L	X	7FF	X	X	X	X	X	L(2)	Set Right $\overline{INT}_R$ Flag
X	X	X	X	X	X	L	L	7FF	H(3)	Reset Right $\overline{INT}_R$ Flag
X	X	X	X	L(3)	L	L	X	7FE	X	Set Left $\overline{INT}_L$ Flag
X	L	L	7FE	H(2)	X	X	X	X	X	Reset Left $\overline{INT}_L$ Flag

3026 tbl 14

NOTES:
1. Assumes $\overline{BUSY}_L = \overline{BUSY}_R = V_{IH}$
2. If $\overline{BUSY}_L = V_{IL}$, then No Change.
3. If $\overline{BUSY}_R = V_{IL}$, then No Change.
4. 'H' = HIGH, 'L' = LOW, 'X' = DON'T CARE.

TABLE III — ADDRESS BUSY ARBITRATION

Inputs			Outputs		
$\overline{CE}_L$	$\overline{CE}_R$	A_{0L}-A_{10L} A_{0R}-A_{10R}	$\overline{BUSY}_L$(1)	$\overline{BUSY}_R$(1)	Function
X	X	NO MATCH	H	H	Normal
H	X	MATCH	H	H	Normal
X	H	MATCH	H	H	Normal
L	L	MATCH	(2)	(2)	Write Inhibit(3)

3026 tbl 15

NOTES:
1. Pins $\overline{BUSY}_L$ and $\overline{BUSY}_R$ are both outputs for IDT71V321. $\overline{BUSY}_X$ outputs on the IDT71V321 are push-pull, not open-drain outputs.
2. 'L' if the inputs to the opposite port were stable prior to the address and enable inputs of this port. 'H' if the inputs to the opposite port became stable after the address and enable inputs of this port. If t_{APS} is not met, either $\overline{BUSY}_L$ or $\overline{BUSY}_R$ = Low will result. $\overline{BUSY}_L$ and $\overline{BUSY}_R$ outputs can not be low simultaneously.

FUNCTIONAL DESCRIPTION

The IDT71V321 provides two ports with separate control, address and I/O pins that permit independent access for reads or writes to any location in memory. The IDT71V321 has an automatic power down feature controlled by $\overline{CE}$. The $\overline{CE}$ controls on-chip power down circuitry that permits the respective port to go into a standby mode when not selected ($\overline{CE}$ = V_{IH}). When a port is enabled, access to the entire memory array is permitted.

INTERRUPTS

If the user chooses to use the interrupt function, a memory location (mail box or message center) is assigned to each port. The left port interrupt flag ($\overline{INT}_L$) is asserted when the right port writes to memory location 7FE (HEX), where a write is defined as the $\overline{CE}$ = R/$\overline{W}$ = V_{IL} per the Truth Table. The left port clears the interrupt by access address location 7FE access when $\overline{CE}_R$ = $\overline{OE}_R$ = V_{IL}, R/$\overline{W}$ is a "don't care". Likewise, the right port interrupt flag ($\overline{INT}_R$) is asserted when the left port writes to memory location 7FF (HEX) and to clear the interrupt flag ($\overline{INT}_R$), the right port must access the memory location 7FF. The message (8 bits) at 7FE or 7FF is user-defined, since it is an addressable SRAM location. If the interrupt function is not used, address locations 7FE and 7FF are not used as mail boxes, but as part of the random access memory. Refer to Truth Table for the interrupt operation.

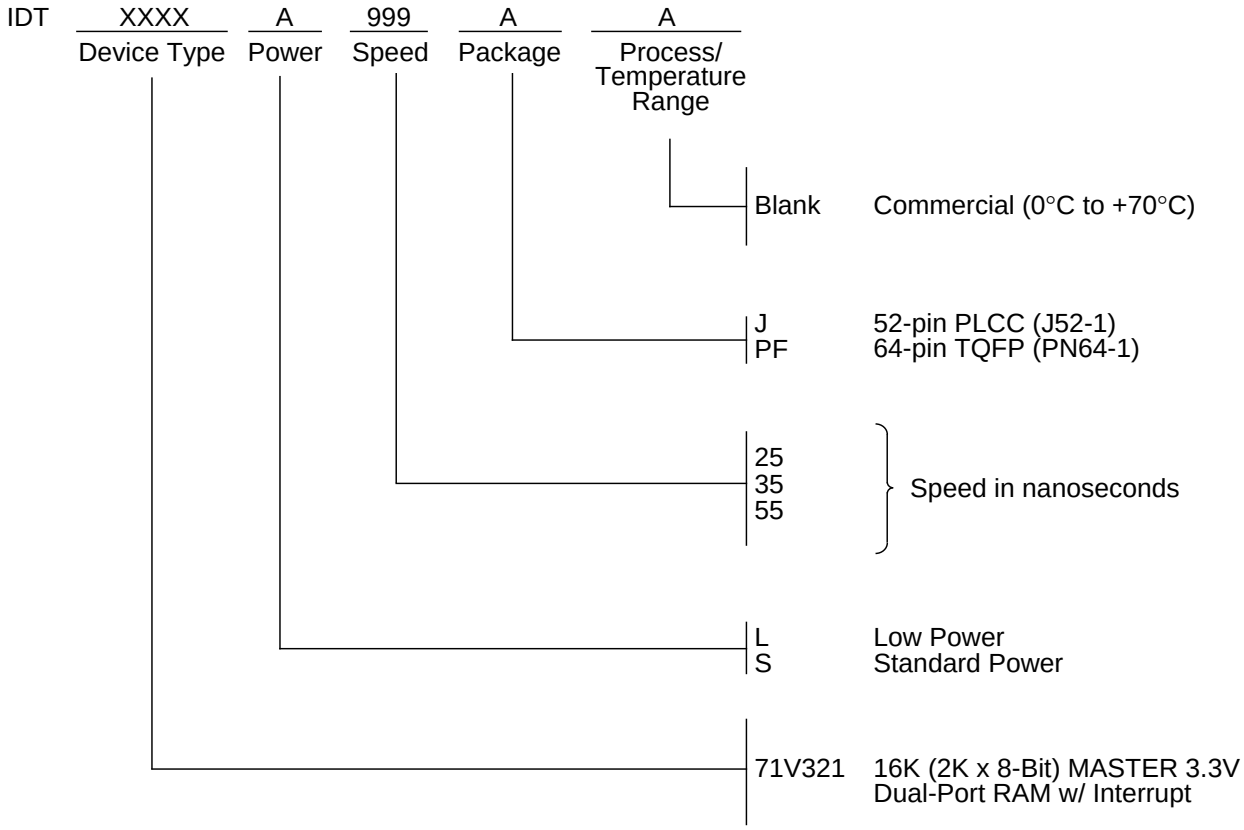
BUSY LOGIC

Busy Logic provides a hardware indication that both ports of the RAM have accessed the same location at the same time. It also allows one of the two accesses to proceed and signals the other side that the RAM is “Busy”. The Busy pin can then be used to stall the access until the operation on the other side is completed. If a write operation has been attempted from the side that receives a busy indication, the write signal is gated internally to prevent the write from proceeding.

The use of busy logic is not required or desirable for all applications. In some cases it may be useful to logically OR the busy outputs together and use any busy indication as an interrupt source to flag the event of an illegal or illogical operation.

The Busy outputs on the IDT71V321 RAM are totem-pole type outputs and do not require pull-up resistors to operate. If these RAMs are being expanded in depth, then the Busy indication for the resulting array does not require the use of an external AND gate.

ORDERING INFORMATION



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