

TC74HCT74AP, TC74HCT74AF, TC74HCT74AFN

DUAL D-TYPE FLIP FLOP WITH PRESET AND CLEAR

The TC74HCT74A is a high speed CMOS D FLIP FLOP fabricated with silicon gate C²MOS technology.

It achieves the high speed operation similar to equivalent LSTTL while maintaining the CMOS low power dissipation.

This device may be used as a level converter for interfacing TTL or NMOS to High Speed CMOS. The inputs are compatible with TTL, NMOS and CMOS output voltage levels.

The signal level applied to the D INPUT is transferred to Q OUTPUT during the positive going transition of the CLOCK pulse.

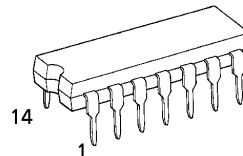
CLEAR and **PRESET** are independent of the CLOCK and are accomplished by setting the appropriate input to an "L" level.

All inputs are equipped with protection circuits against static discharge or transient excess voltage.

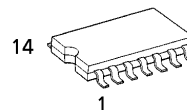
FEATURES :

- High Speed..... $f_{MAX} = 53\text{MHz}$ (typ.)
at $V_{CC} = 5\text{V}$
- Low Power Dissipation..... $I_{CC} = 2\mu\text{A}$ (Max.) at $T_a = 25^\circ\text{C}$
- Compatible with TTL outputs... $V_{IH} = 2\text{V}$ (Min.)
 $V_{IL} = 0.8\text{V}$ (Max.)
- Wide Interfacing ability.....LSTTL, NMOS, CMOS
- Output Drive Capability.....10 LSTTL Loads
- Symmetrical Output Impedance... $|I_{OH}| = I_{OL} = 4\text{mA}$ (Min.)
- Balanced Propagation Delays... $t_{pLH} \approx t_{pHL}$
- Pin and Function Compatible with 74LS74

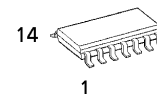
(Note) The JEDEC SOP (FN) is not available in Japan.



P (DIP14-P-300-2.54)
Weight : 0.96g (Typ.)

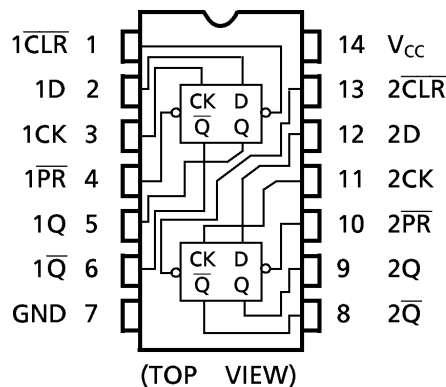


F (SOP14-P-300-1.27)
Weight : 0.18g (Typ.)



FN (SOL14-P-150-1.27)
Weight : 0.12g (Typ.)

PIN ASSIGNMENT

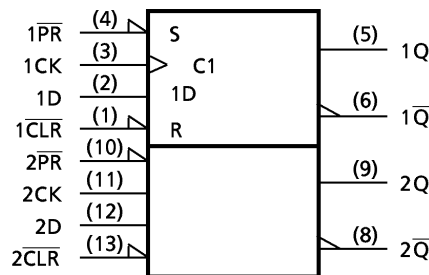


TRUTH TABLE

INPUTS				OUTPUTS		FUNCTION
CLR	PR	D	CK	Q	Q̄	
L	H	X	X	L	H	CLEAR
H	L	X	X	H	L	PRESET
L	L	X	X	H	H	—
H	H	L	┌	L	H	—
H	H	H	┌	H	L	—
H	H	X	└	Q _n	Q̄ _n	NO CHANGE

X : Don't Care

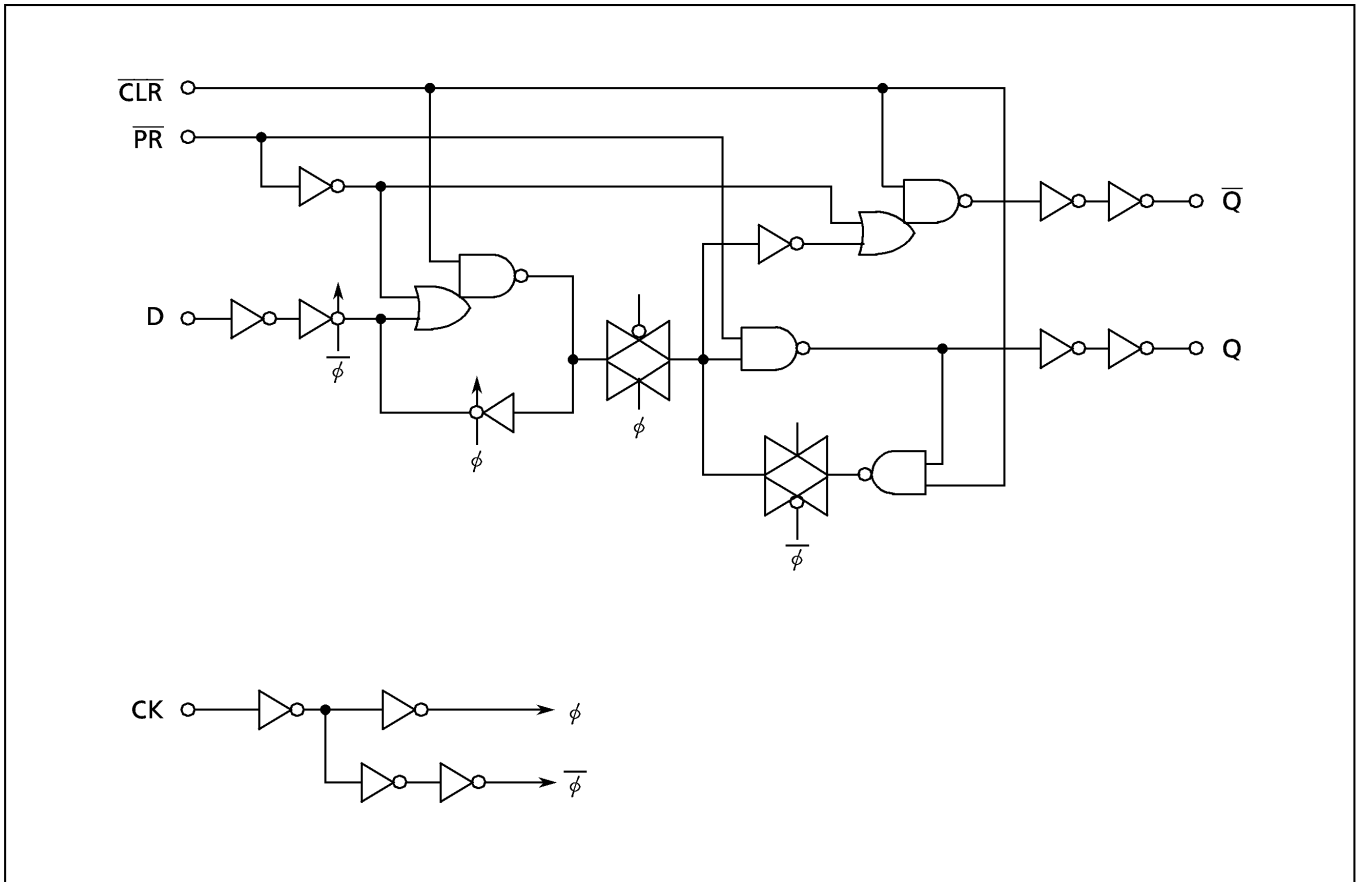
IEC LOGIC SYMBOL



980508EBA2

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SYSTEM DIAGRAM



980508EBA2'

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ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage Range	V_{CC}	-0.5~7	V
DC Input Voltage	V_{IN}	-0.5~ $V_{CC} + 0.5$	V
DC Output Voltage	V_{OUT}	-0.5~ $V_{CC} + 0.5$	V
Input Diode Current	I_{IK}	±20	mA
Output Diode Current	I_{OK}	±20	mA
DC Output Current	I_{OUT}	±25	mA
DC V_{CC} / Ground Current	I_{CC}	±50	mA
Power Dissipation	P_D	500 (DIP)* / 180 (SOP)	mW
Storage Temperature	T_{stg}	-65~150	°C

*500mW in the range of $T_a = -40^{\circ}\text{C} \sim 65^{\circ}\text{C}$. From $T_a = 65^{\circ}\text{C}$ to 85°C a derating factor of $-10\text{mW}/^{\circ}\text{C}$ shall be applied until 300mW.

RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	VALUE	UNIT
Supply Voltage	V_{CC}	4.5~5.5	V
Input Voltage	V_{IN}	0~ V_{CC}	V
Output Voltage	V_{OUT}	0~ V_{CC}	V
Operating Temperature	T_{opr}	-40~85	°C
Input Rise and Fall Time	t_r, t_f	0~500	ns

DC ELECTRICAL CHARACTERISTICS

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	$T_a = 25^{\circ}\text{C}$			$T_a = -40 \sim 85^{\circ}\text{C}$		UNIT	
				MIN.	TYP.	MAX.	MIN.	MAX.		
High - Level Input Voltage	V_{IH}		4.5 ┆ 5.5	2.0	—	—	2.0	—	V	
Low - Level Input Voltage	V_{IL}		4.5 ┆ 5.5	—	—	0.8	—	0.8	V	
High - Level Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OH} = -20 \mu\text{A}$	4.5	4.4	4.5	—	4.4	—	V
			$I_{OH} = -4 \text{ mA}$	4.5	4.18	4.31	—	4.13	—	
Low - Level Output Voltage	V_{OL}	$V_{IN} = V_{IH}$ or V_{IL}	$I_{OL} = 20 \mu\text{A}$	4.5	—	0.0	0.1	—	0.1	V
			$I_{OL} = 4 \text{ mA}$	4.5	—	0.17	0.26	—	0.33	
Input Leakage Current	I_{IN}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	±0.1	—	±1.0	μA	
Quiescent Supply Current	I_{CC}	$V_{IN} = V_{CC}$ or GND	5.5	—	—	2.0	—	20.0		
		I_C	PER INPUT: $V_{IN} = 0.5\text{V}$ or 2.4V OTHER INPUT: V_{CC} or GND	5.5	—	—	2.0	—	2.9	mA

TIMING REQUIREMENTS (Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C		Ta = -40~85°C	UNIT
				TYP.	LIMIT	LIMIT	
Minimum Pulse Width (CK)	$t_{W(L)}$ $t_{W(H)}$		4.5	—	15	19	ns
			5.5	—	14	17	
Minimum Pulse Width ($\overline{\text{CLR}}$, $\overline{\text{PR}}$)	$t_{W(L)}$		4.5	—	15	19	
			5.5	—	14	17	
Minimum Set-up Time	t_s		4.5	—	15	19	
			5.5	—	14	17	
Minimum Hold Time	t_h		4.5	—	0	0	
			5.5	—	0	0	
Minimum Removal Time ($\overline{\text{CLR}}$, $\overline{\text{PR}}$)	t_{rem}		4.5	—	5	5	
			5.5	—	5	5	
Clock Frequency	f		4.5	—	27	22	MHz
			5.5	—	30	24	

AC ELECTRICAL CHARACTERISTICS ($C_L = 15\text{pF}$, $V_{CC} = 5\text{V}$, Ta = 25°C, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	MIN.	TYP.	MAX.	UNIT
Output Transition Time	t_{TLH} t_{THL}		—	6	12	ns
Propagation Delay Time (CK-Q, \overline{Q})	t_{pLH} t_{pHL}		—	17	28	
Propagation Delay Time ($\overline{\text{CLR}}$, $\overline{\text{PR}}$ -Q, \overline{Q})	t_{pLH} t_{pHL}		—	15	25	
Maximum Clock Frequency	f_{MAX}		29	53	—	MHz

AC ELECTRICAL CHARACTERISTICS ($C_L = 50\text{pF}$, Input $t_r = t_f = 6\text{ns}$)

PARAMETER	SYMBOL	TEST CONDITION	V_{CC} (V)	Ta = 25°C			Ta = -40~85°C		UNIT
				MIN.	TYP.	MAX.	MIN.	MAX.	
Output Transition Time	t_{TLH} t_{THL}		4.5	—	8	15	—	19	ns
			5.5	—	7	13	—	16	
Propagation Delay Time (CK-Q, Q)	t_{pLH} t_{pHL}		4.5	—	21	33	—	41	
			5.5	—	19	30	—	37	
Propagation Delay Time ($\overline{\text{CLR}}$, $\overline{\text{PR}}$ -Q, Q)	t_{pLH} t_{pHL}		4.5	—	18	30	—	38	
			5.5	—	15	27	—	35	
Maximum Clock Frequency	f_{MAX}		4.5	27	48	—	22	—	MHz
			5.5	30	53	—	24	—	
Input Capacitance	C_{IN}			—	5	10	—	10	pF
Power Dissipation Capacitance	C_{PD}	(1)		—	32	—	—	—	

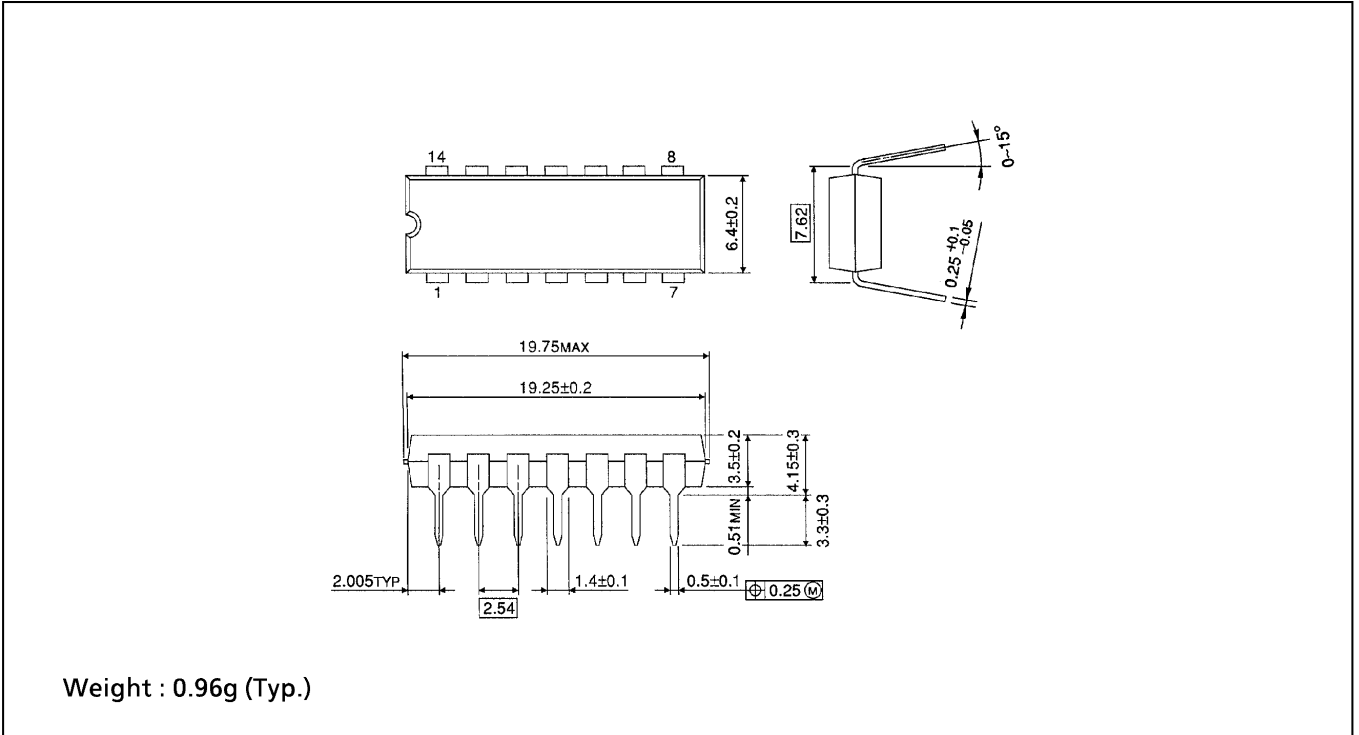
Note (1) C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load.

Average operating current can be obtained by the equation:

$$I_{CC}(\text{opr}) = C_{PD} \cdot V_{CC} \cdot f_{IN} + I_{CC}/2 \text{ (per F/F)}$$

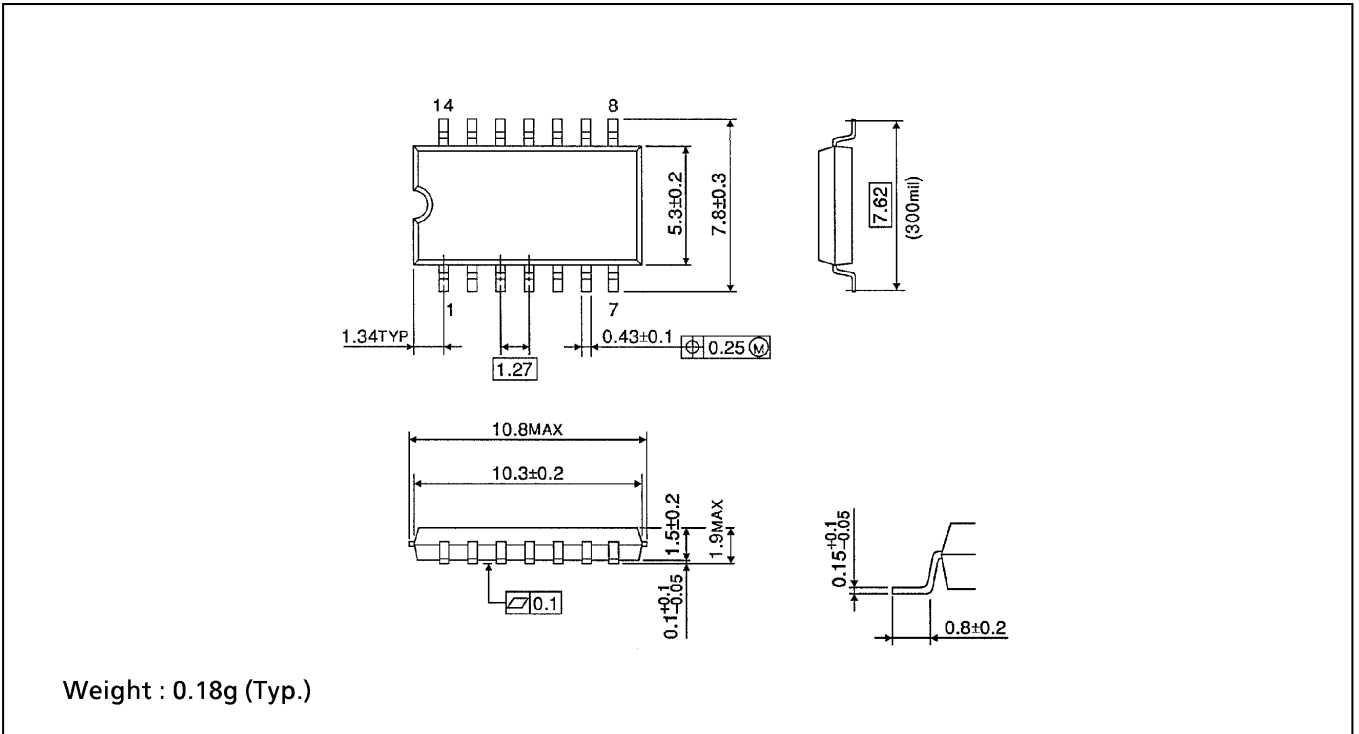
DIP 14PIN OUTLINE DRAWING (DIP14-P-300-2.54)

Unit in mm



SOP 14PIN (200mil BODY) OUTLINE DRAWING (SOP14-P-300-1.27)

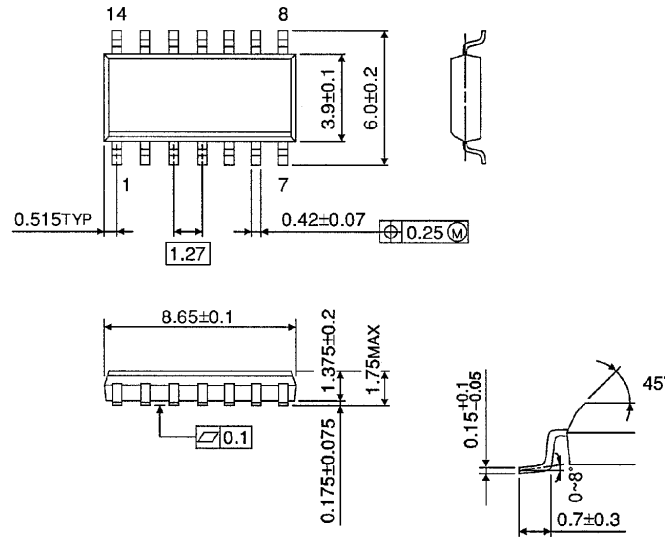
Unit in mm



SOP 14PIN (150mil BODY) OUTLINE DRAWING (SOL14-P-150 -1.27)

Unit in mm

(Note) This package is not available in Japan.



Weight : 0.12g (Typ.)