SONY

CXD2464R

Timing Generator for LCD Panels
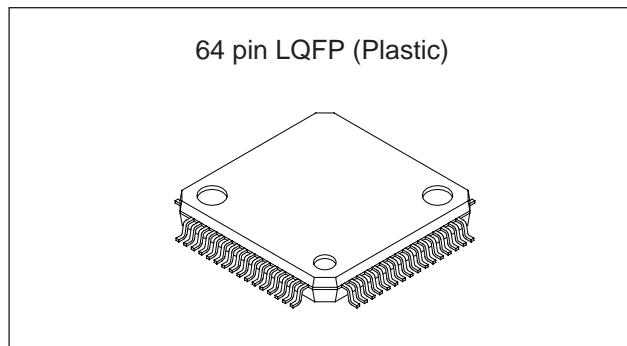
Description

The CXD2464R is a timing signal generator for driving the LCX026, LCX016 and LCX012BL LCD panels. This chip has a built-in serial interface circuit which supports various XGA, SVGA and VGA signals, and (double speed) NTSC and PAL signals through external control from a microcomputer, etc.

Features

• Generates the LCX026/LCX016/LCX012BL drive pulse.
• Supports various SVGA (horizontal scanning frequency: 35 to 54kHz, vertical scanning frequency: 56 to 86Hz) and VGA (horizontal scanning frequency: 31 to 38kHz, vertical scanning frequency: 59 to 75Hz) signals.
• Supports simple (skip scan) display of XGA signals (1024 × 768 dots, horizontal scanning frequency: 57kHz, vertical scanning frequency: 71Hz or less, clock frequency: 62.5MHz or less).
• Supports simple (skip scan) display of SVGA signals (800 × 600 dots).
• Supports Macintosh16 signals (LCX016)
• Supports PC-98 signals (640 × 400 dots, horizontal scanning frequency: 24 to 38kHz, vertical scanning frequency: 56 to 86Hz).
• Supports NTSC and PAL signals
• Line double-speed display realized with a built-in double-speed controller (clock frequency: 33.3MHz or less)
  (Line memory μPD485505: NEC)
• Allows control of sample-and-hold position of CXA2112R sample-and-hold driver.
• Supports up/down inversion and/or right/left inversion.
• Supports line inversion and field inversion
• AC drive of LCD panels during no signal

Note) Supported signals vary according to LCD panel.

64 pin LQFP (Plastic)

Applications

LCD projectors, etc.

Structure

Silicon gate CMOS IC

Absolute Maximum Ratings (Ta = 25°C, V_{SS} = 0V)

• Supply voltage V_{DD} V_{SS} – 0.5 to +7.0   V
• Input voltage V_I V_{SS} – 0.5 to V_{DD} + 0.5   V
• Output voltage V_O V_{SS} – 0.5 to V_{DD} + 0.5   V
• Operating temperature
                    Topr   –20 to +75   °C
• Storage temperature
   Tstg   –55 to +150   °C

Recommended Operating Conditions

• Supply voltage V_{DD} 4.5 to 5.5   V
• Operating temperature
                    Topr   –20 to +75   °C

E98327-PS

Block Diagram

Note) CLP2 and FLDO pulses share the same pins.

Pin Description

Pin No.	Symbol	I/O	Description	Input pin for open status
1	HSYNC	I	Horizontal sync signal input pin	—
2	VSYNC	I	Vertical sync signal input pin	—
3	TST0	—	Test pin (Connect to GND.)	—
4	TST1	—	Test pin (Connect to V_{DD}.)	—
5	TST2	—	Test pin (Not connected.)	—
6	TST3	—	Test pin (Connect to GND.)	—
7	TST4	—	Test pin (Not connected.)	—
8	$V_{SS}0$	—	GND	—
9	TST5	—	Test pin (Connect to GND.)	—
10	TST6	—	Test pin (Connect to V_{DD}.)	—
11	TST7	—	Test pin (Not connected.)	—
12	TST8	—	Test pin (Not connected.)	—
13	TST9	—	Test pin (Not connected.)	—
14	TST10	—	Test pin (Not connected.)	—
15	TST11	—	Test pin (Not connected.)	—
16	TST12	—	Test pin (Connect to GND.)	—
17	CKI2	I	Clock 2 input pin (for scan converter)	—
18	TST13	I	Test pin (Not connected.)	—
19	XCLR	I	System clear pin (Set to L: SVGA (VESA 72Hz))	H
20	MODE3	O	Mode switching pin 3 output	—
21	MODE2	O	Mode switching pin 2 output	—
22	MODE1	O	Mode switching pin 1 output	—
23	$V_{SS}1$	—	GND	—
24	$V_{DD}0$	—	V_{DD}	—
25	RGT	O	Right/left inversion discrimination signal output (H output: Normal, L output: Reverse)	—
26	XRGT	O	Right/left inversion discrimination signal output (H output: Reverse, L output: Normal)	—
27	HST	O	HST pulse output	—
28	HCK1	O	HCK 1 pulse output	—
29	HCK2	O	HCK 2 pulse output	—
30	BLK	O	BLK pulse output	—
31	CLR	O	CLR pulse output	—
32	ENB	O	ENB pulse output	—
33	VCK	O	VCK pulse output	—

Pin No.	Symbol	I/O	Description	Input pin for open status
34	VST	O	VST pulse output	—
35	TST14	—	Test pin (Not connected.)	—
36	PCG	O	PCG pulse output	—
37	DWN	O	Up/down inversion discrimination signal output (H output: Down, L output: Up)	—
38	HD	O	HD pulse output	—
39	CLP1	O	Pedestal clamp pulse 1 output	—
40	Vss2	—	GND	—
41	CLP2/FLDO	O	Pedestal clamp pulse 2 output/FLDO pulse output	—
42	PRG	O	Precharge signal pulse output	—
43	FRP	O	AC drive inversion timing output	—
44	XFRP	O	AC drive inversion timing output (reverse polarity of FRP)	—
45	SHPA	O	External sample-and-hold driver control signal (for CXA2112R)	—
46	SHPB	O	External sample-and-hold driver control signal (for CXA2112R)	—
47	SHPC	O	External sample-and-hold driver control signal (for CXA2112R)	—
48	SHPD	O	External sample-and-hold driver control signal (for CXA2112R)	—
49	INV	O	External sample-and-hold driver control signal (for CXA2112R)	—
50	XVS	O	Auxiliary pulse output for CXD2449Q	—
51	XHS	O	Auxiliary pulse output for CXD2449Q	—
52	IRACT	O	Auxiliary pulse output for scan converter	—
53	ORACT	O	Auxiliary pulse output for scan converter	—
54	RSTR	O	Reset read output (for high-speed line buffer)	—
55	Vss3	—	GND	—
56	VDD1	—	VDD	—
57	RCK	O	Read clock output (for high-speed line buffer)	—
58	RSTW	O	Reset write output (for high-speed line buffer)	—
59	WCK	O	Write clock output (for high-speed line buffer)	—
60	SCTR	I	Chip select input pin (serial transfer block)	—
61	SCLK	I	Serial clock input pin (serial transfer block)	—
62	SDAT	I	Serial data input pin (serial transfer block)	—
63	HDN	O	Phase comparator pulse output	—
64	CKI1	I	Clock 1 input pin	—

* H: Pull up, L: Pull down

Electrical Characteristics

1. DC characteristics

(V_{DD} = 5.0 ± 0.5V, V_{SS} = 0V, Topr = −20 to +75°C)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit	Applicable pins
Supply voltage	V_{DD}		4.5	5.0	5.5	V	
Input, output voltages	V_I, Vo		V_{SS}		V_{DD}	V	
Input voltage 1	V_{IH}	CMOS input	0.7V_{DD}			V	XCLR CKI1, CKI2
	V_{IL}				0.3V_{DD}		
Input voltage 2	Vt+	TTL Schmitt trigger input	2.2			V	HSYNC VSYNC SCTR, SCLK SDAT
	Vt−				0.8		
	Vt+ − Vt−			0.4			
Output voltage 1	V_{OH}	I_{OH} = −2mA	V_{DD} − 0.8			V	*1
	V_{OL}	I_{OL} = 4mA			0.4		
Output voltage 2	V_{OH}	I_{OH} = −4mA	V_{DD} − 0.8			V	*2
	V_{OL}	I_{OL} = 8mA			0.4		
Input leak current	I_I	*3	−10		10	µA	*4
	I_{IL}	*5	−40	−100	−240		XCLR
Output leak current	Ioz	*6	−40		40	µA	*7
Current consumption	I_{DD}	*8			56	mA	At a 30pF load

*1 INV, SHPA, SHPB, SHPC, SHPD, MODE1, MODE2, MODE3, HD, HDN, CLR, ENB, PRG, PCG, CLP1, CLP2/FLDO, VST, BLK, FRP, XFRP, VCK, DWN, RGT, XRGT, IRACT, ORACT, XHS, XVS

*2 RSTR, RSTW, RCK, WCK, HCK1, HCK2, HST

*3 Normal input pins (V_{IN} = V_{SS} or V_{DD})

*4 HSYNC, VSYNC, SCLK, SDAT, SCTR, CKI1, CKI2

*5 Pins with pull-up resistors (V_{IN} = V_{SS})

*6 At high impedance (V_{IN} = V_{SS} or V_{DD})

*7 SHPA, SHPC

*8 fclk = 62.5MHz, V_{DD} = 5.0V

2. AC characteristics

(V$_{DD}$ = 5.0 ± 0.5V, V$_{SS}$ = 0V, Topr = −20 to +75°C)

Item	Symbol	Applicable pins		Min.	Typ.	Max.	Conditions	Unit
Clock input cycle		CKI1, 2	XGA, Mac16	16.0				ns
			SVGA	20.0				
			VGA	30.0				
Output rise time	tr	All outputs				20	CL = 30pF	
Output fall time	tf	All outputs				20	CL = 30pF	
Cross-point time difference	Δt	HCK1, 2		−10		10	CL = 30pF	
Output rise delay time	tpr	All outputs				15	CL = 30pF	
Output fall delay time	tpf	All outputs				15	CL = 30pF	
HCK1 Duty	t$_H$/(t$_H$ + t$_L$)	HCK1		48		52	CL = 30pF	%
HCK2 Duty	t$_L$/(t$_H$ + t$_L$)	HCK2		48		52	CL = 30pF	

Note) The minimum value for the clock input cycle (CKI1) when using the built-in double-speed controller is 30.0ns.

3. Serial transfer AC characteristics

(V$_{DD}$ = 5.0 ± 0.5V, Vss = 0V, Topr =−20 to +75°C)

Symbol	Item	Min.	Typ.	Max.
ts0	SCTR setup time with respect to rise of SCLK	4Tns		
ts1	SDAT setup time with respect to rise of SCLK	2Tns		
th0	SCTR hold time with respect to rise of SCLK	4Tns		
th1	SDAT hold time with respect to rise of SCLK	2Tns		
tw1L	SCLK L level pulse width	2Tns		
tw1H	SCLK H level pulse width	2Tns		
tw2		5Tns		
tw3		5Tns		

T: Master clock cycle (ns)

Note) Consider the frequency at free run (no signal). When the above characteristic specification is not satisfied at free run, operating guarantee is not performed as serial transfer.

4. External clock input AC characteristics

(V$_{DD}$ = 5.0 ± 0.5V, Vss = 0V, Topr = −20 to +75°C)
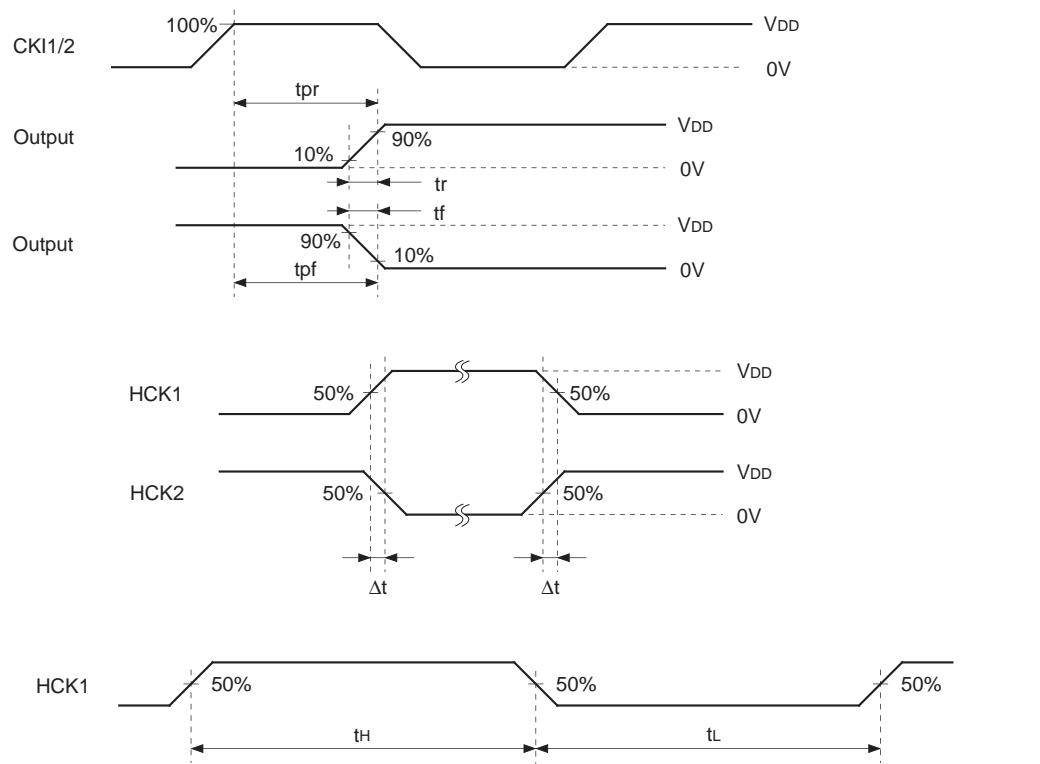
Symbol	Item	Min.	Typ.	Max.
ts0	HSYNC setup time with respect to rise of CKI1/2	2ns		
th0	HSYNC hold time with respect to rise of CKI1/2	6ns		
twL	CKI1/2 L level pulse width	6ns	T/2ns	
twH	CKI1/2 H level pulse width	6ns	T/2ns	

T: Master clock cycle (ns)

Note) During external clock input, set serial data HR to L. The pulse synchronized with the horizontal sync signal is generated by detecting the front edge of horizontal sync signal and then resetting internal PLL counter.
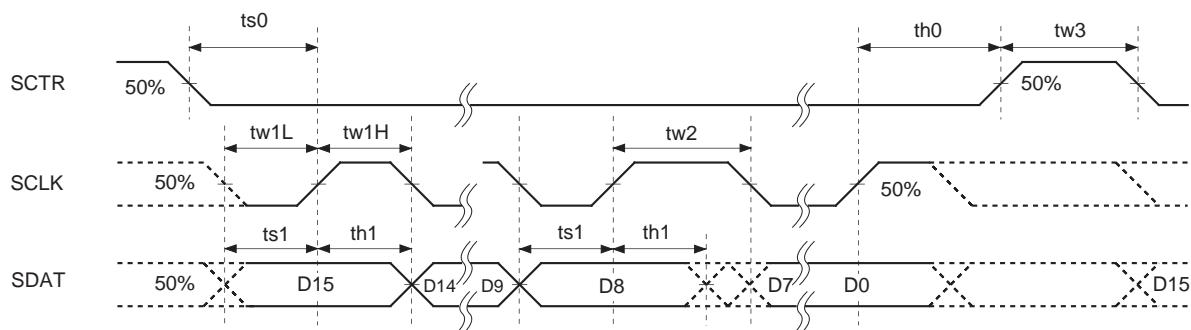
5. Timing definitions

AC characteristics
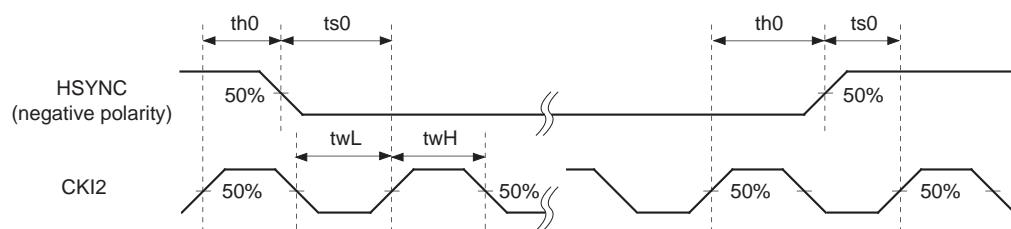
Note) HCK2 is the reverse phase of HCK1.

Serial transfer AC characteristics

Note) See "Serial transfer timing" for the timing relationship between D15 to D0 and each pulse.
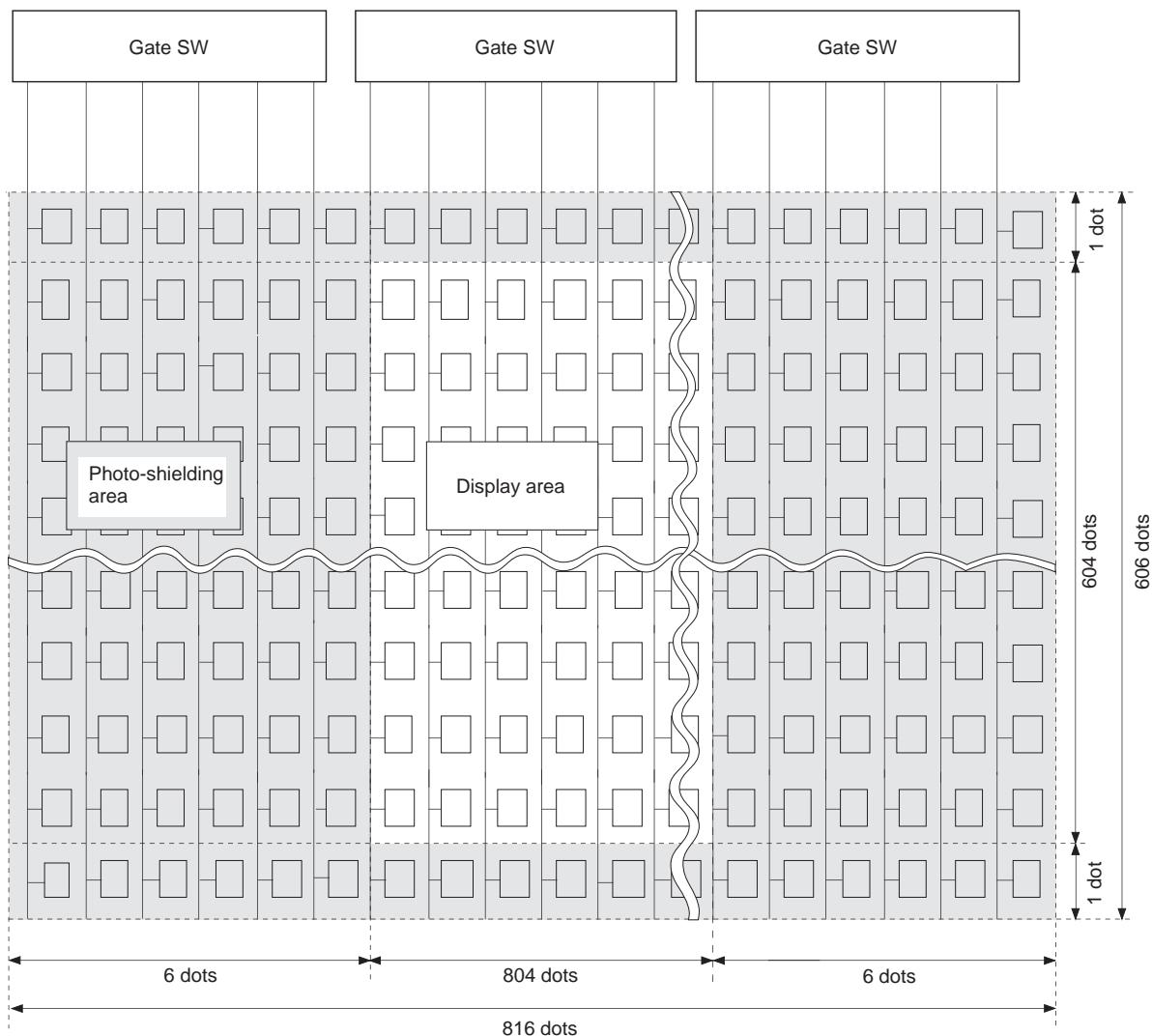
External clock input AC characteristics

Pixel Arrangement

The LCD panels supported by the CXD2464R are the LCX026, the LCX016 and the LCX012BL. The pixel arrangement is a square arrangement for both panels. The shaded region in the diagram is not displayed, however, for the LCX026 and the LCX016, since the CXD2464R has a built-in display area variable circuit, the display area dots varies according to the mode[*1] to match the various signal protocols.

LCX026 pixel arrangement
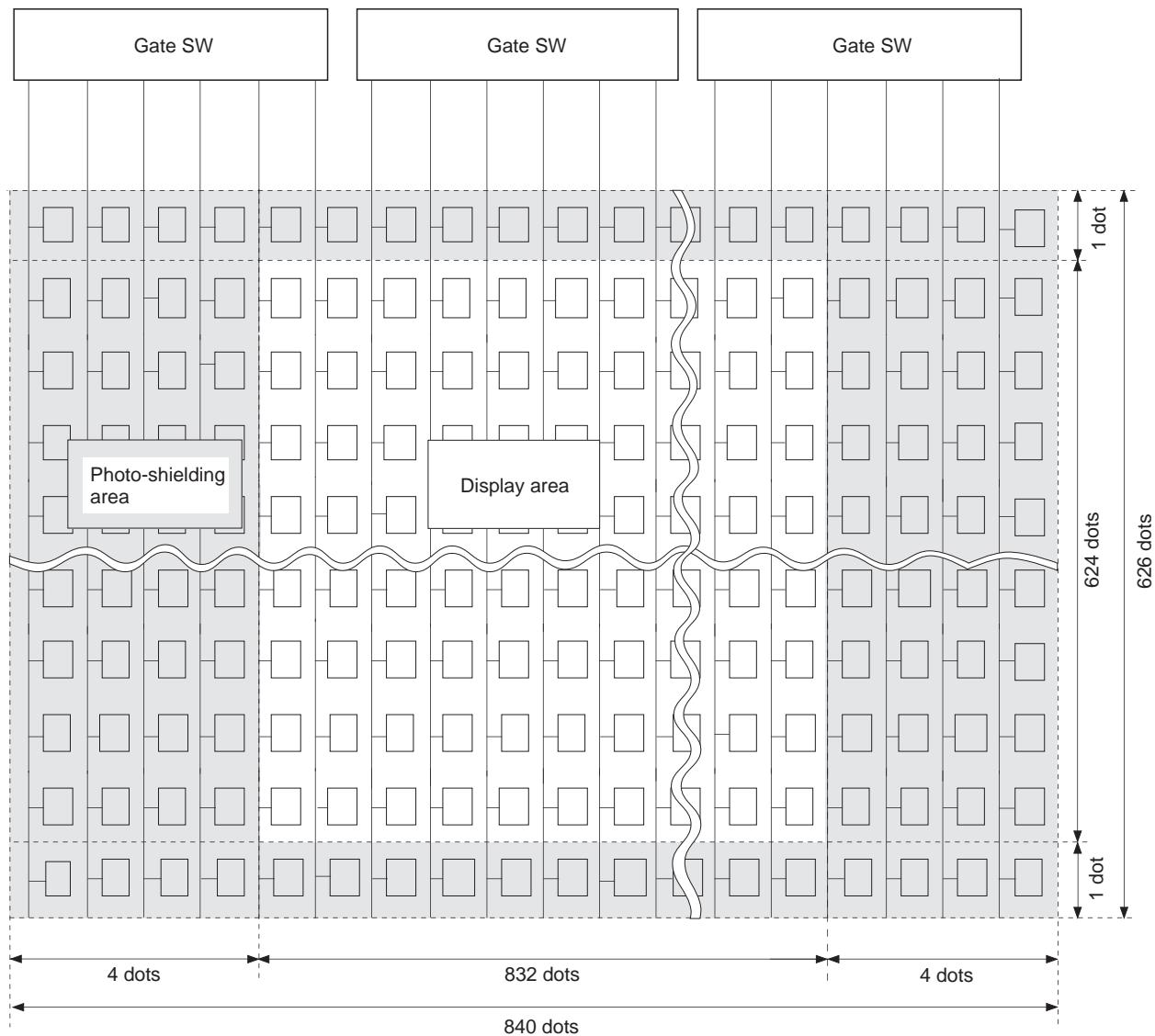
MODE1	MODE2	MODE3	Display mode	Number of horizontal display dots	Number of vertical display dots	Number of display dots
L	L	—	SVGA	804	604	485,616
L	H	L	PAL	762	572	435,864
L	H	H	VGA/NTSC	644	484	311,696
H	L	L	PC-98	644	404	260,176

—: don't care   Unit: dot
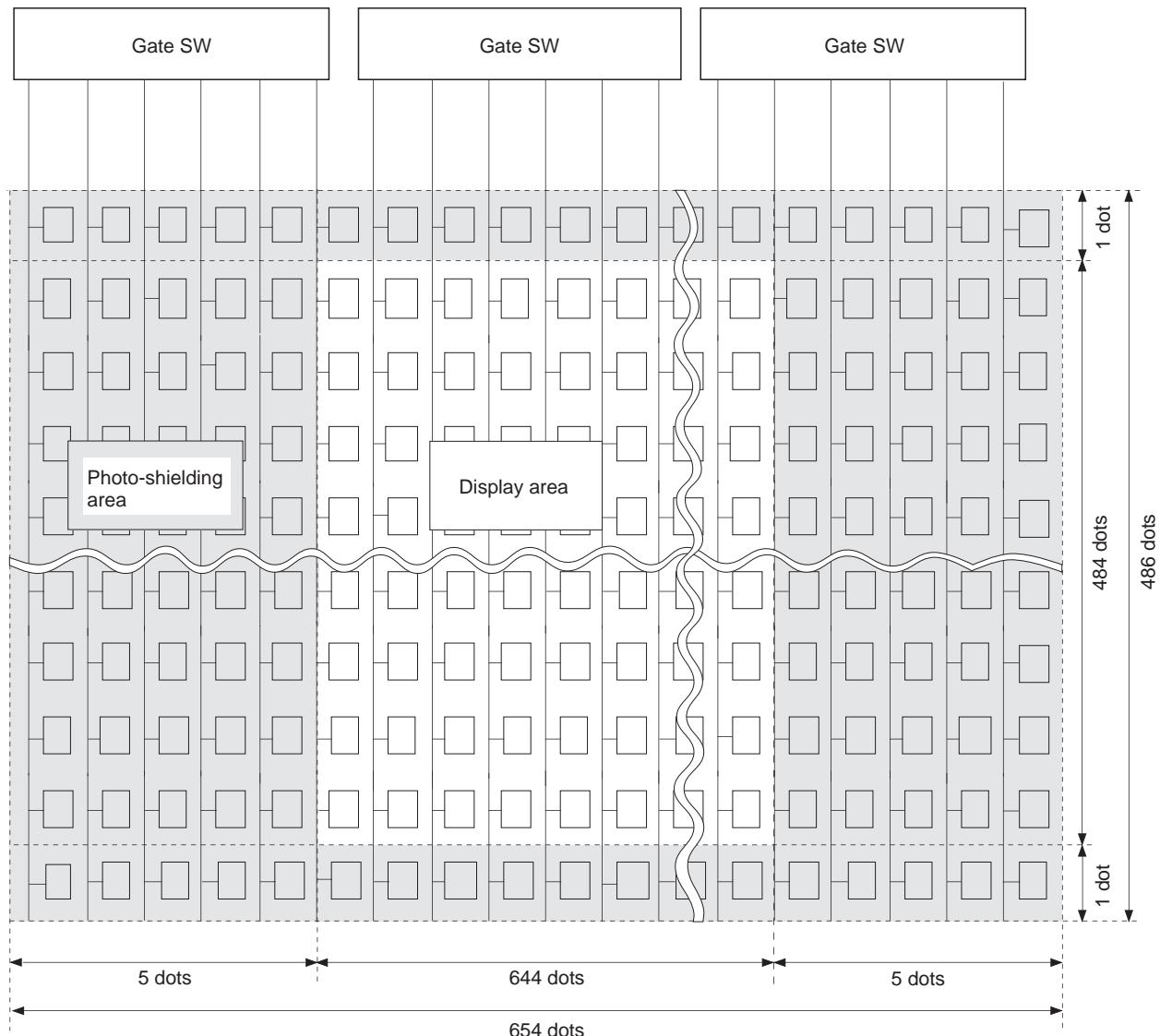
[*1] See the description of serial data specifications for details.

LCX016 pixel arrangement

MODE1	MODE2	MODE3	Display mode	Number of horizontal display dots	Number of vertical display dots	Number of display dots
L	L	L	Macintosh16	832	624	519,168
L	L	H	SVGA	800	600	480,000
L	H	L	PAL	762	572	435,864
L	H	H	VGA/NTSC	640	480	307,200
H	L	L	PC-98	640	400	256,000
H	L	H	WIDE	832	480	399,360

Unit: dot

LCX012BL pixel arrangement

Number of horizontal display dots	Number of vertical display dots	Number of display dots
644	484	311,696

Unit: dot

Input Signal Protocol

1. Horizontal sync signal

    a) A standard signal (HSYNC) should be input for the following display modes.

        LCX026   : SVGA (800 × 600), VGA/NTSC (640 × 480), PC-98 (640 × 400), PAL (762 × 572)

        LCX016   : Macintosh16 (832 × 624), SVGA (800 × 600), VGA/NTSC (640 × 480), PC-98 (640 × 400),

                    PAL (762 × 572), WIDE (832 × 480)

        LCX012BL : VGA/NTSC/PAL (640 × 480), PC-98 (640 × 400)

        However, since the CXD2464R requires a double speed signal as input during NTSC/PAL double-speed display when not using the built-in double-speed controller, a simply double-speeded, 1/2 cycle, 1/2 width horizontal sync signal (HSYNC) should be input at that time.

    b) The input sync signal polarity is not fixed, and is set by the serial data (HPOL).
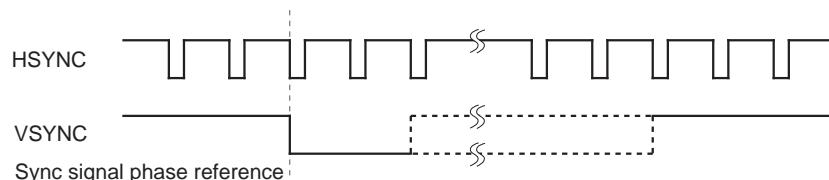
2. Vertical sync signal

    a) A sync-separated, normal-speed VSYNC should be input as the vertical sync signal.
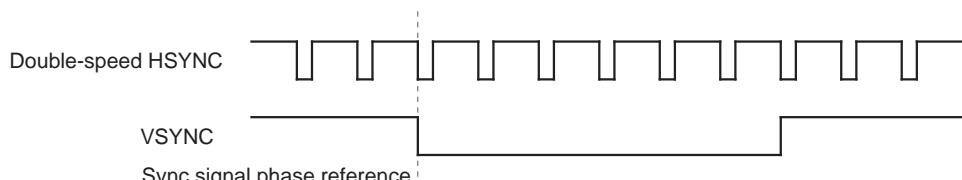
    b) The input sync signal polarity is not fixed, and is set by the serial data (VPOL).

    c) The phase relationship between HSYNC and VSYNC is specified as follows for the CXD2464R.
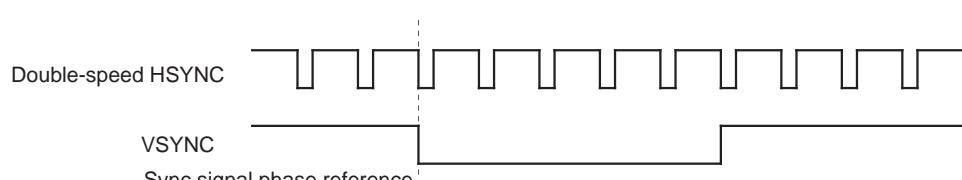
(1) SVGA, VGA, PC-98 (LCX026)/Macintosh16, SVGA, VGA, PC-98 (LCX016)/VGA, PC-98 (LCX012BL)
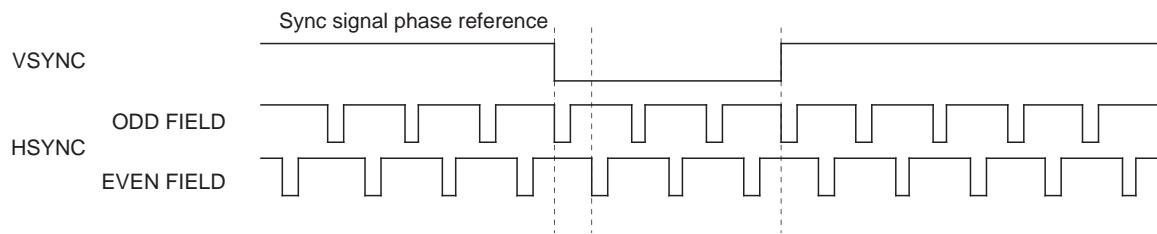
(2) Double-speed NTSC (LCX026/LCX016/LCX012BL)
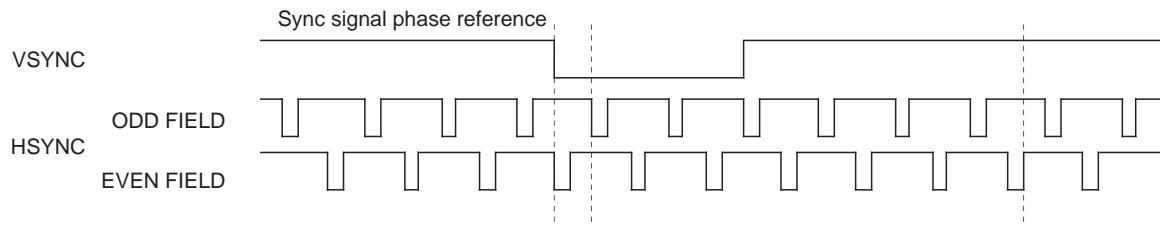
(3) Double-speed PAL (LCX026/LCX016/LCX012BL)

(4) NTSC (LCX026/LCX016/LCX012BL)

Sync signal phase reference

VSYNC

ODD FIELD

HSYNC

EVEN FIELD

(5) PAL (LCX026/LCX016/LCX012BL)

Sync signal phase reference

VSYNC

ODD FIELD

HSYNC

EVEN FIELD

Note) (2) and (3) show the timing when supporting input of double-speed signals

(4) and (5) show the timing when using the built-in double-speed controller (CXD2464R) and a line memory (µPD485505: NEC)

Description of Operation

Sync signal input

The HSYNC and VSYNC input pins support separate SYNC only. When using a composite SYNC input, use a separate IC for sync separation, etc.

Clock input

(1) CKI1 pin

CKI1 is the clock input pin from an external PLL IC. A 1/N frequency divider output for PLL IC is output from the HDN pin. HDN polarity at this time is set by serial data HDNPOL.

(2) CKI2 pin

CKI2 is a clock input pin when using a scan converter that operates with synchronous input signals and asynchronous clock in the system. Since two types of clocks are input in this case, the circuit that basically operates with the respective clocks of CKI1 and CKI2 is asynchronous. For details, refer to the explanation of pulse setting for the scan converter in this specification (starting on page 37).

AC driving of LCD panels for no signal

The following measures have been adopted to allow AC driving of LCD panels even when there is no signal.

Horizontal direction pulse

The PLL is set to free running status. Therefore, the frequency of the horizontal direction pulse is dependent on the PLL free running frequency.

Vertical direction pulse

The number of lines is counted by an internal counter (AUX-VD COUNTER) and the vertical direction pulses (VST, FRP) are output at a specified cycle. For the CXD2464R, no signal (free running) status is judged if there is no VSYNC input for longer than the following periods (free running detection timing).

Mode	V cycle for no signal	Free running detection
Double-speed NTSC	263H	468H
Double-speed PAL	313H	
Other	650H	900H

Note) The double-speed NTSC and PAL modes are the modes when using the built-in double-speed controller.

XCLR pin

The CXD2464R should be forcibly reset during power on in order to initialize the serial transfer block and other internal circuits.
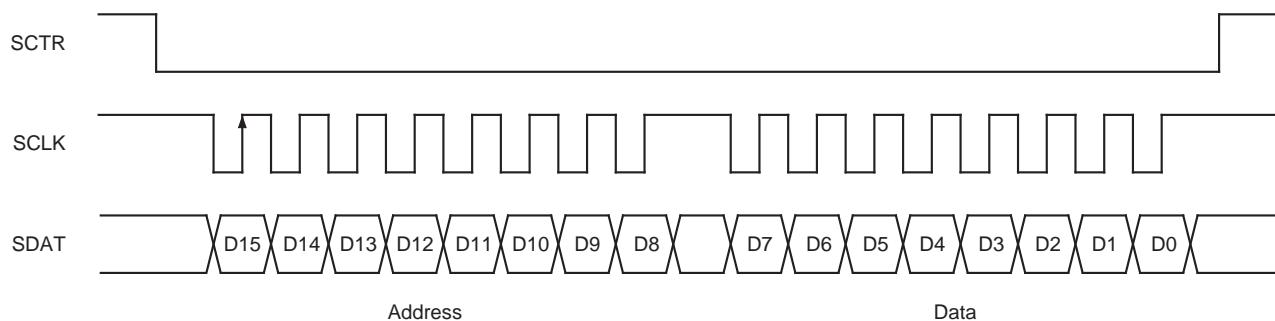
Serial transfer operation

1. Control method

The CXD2464R operation timing is controlled by serial data.

The control data is comprised of an 8-bit address and 8-bit data, and the individual data is loaded at the rise of SCLK. This load operation starts from the fall of SCTR and is completed at the next rise of SCTR.

Serial transfer timing

2. Control data

When using the CXD2464R, set the control data corresponding to each signal source according to the formats in the table below.

Address								Data								Function
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0	
0	0	0	0	0	0	0	0	—	—	—	—	—	PLLP10	PLLP9	PLLP8	(A) PLL frequency division ratio (1/N)
0	0	0	0	0	0	0	1	PLLP7	PLLP6	PLLP5	PLLP4	PLLP3	PLLP2	PLLP1	PLLP0	
0	0	0	0	0	0	1	0	HP7	HP6	HP5	HP4	HP3	HP2	HP1	HP0	(B) H-POSITION
0	0	0	0	0	0	1	1	VP7	VP6	VP5	VP4	VP3	VP2	VP1	VP0	(C) V-POSITION
0	0	0	0	0	1	0	0	—	—	—	—	HSTP3	HSTP2	HSTP1	HSTP0	(D) HST-POSITION
0	0	0	0	0	1	0	1	—	—	—	PCGP4	PCGP3	PCGP2	PCGP1	PCGP0	(E) PCG-POSITION
0	0	0	0	0	1	1	0	—	—	—	PRGP4	PRGP3	PRGP2	PRGP1	PRGP0	(E) PRG-POSITION
0	0	0	0	0	1	1	1	—	—	—	—	—	—	CLPP1	CLPP0	(F) CLP-POSITION
0	0	0	0	1	0	0	0	—	—	—	INV	SHP3	SHP2	SHP1	SHP0	(G) S/H control for CXD2112R
0	0	0	0	1	0	0	1	—	—	CKTST0	FLD	FRP1	FRP0	CKTST1	RCK	(H) Mode settings
0	0	0	0	1	0	1	0	—	—	VPOL	HPOL	HDNPOL	CLPPOL	PCGPOL	PRGPOL	
0	0	0	0	1	0	1	1	—	—	—	MBKB	MBKA	MBK2	MBK1	MBK0	
0	0	0	0	1	1	0	0	—	—	MODE021	MODEB	MODEA	MODE3	MODE2	MODE1	
0	0	0	0	1	1	0	1	VGAV	HR	DWN	RGT	HST	PCG	DSP	PC98	
0	0	0	1	0	0	0	0	—	—	—	SLLAP	—	IRD10	IRD9	IRD8	(I) IRACT fall position
0	0	0	1	0	0	0	1	IRD7	IRD6	IRD5	IRD4	IRD3	IRD2	IRD1	IRD0	
0	0	0	1	0	0	1	0	—	—	—	—	—	IRU10	IRU9	IRU8	(I) IRACT rise position
0	0	0	1	0	0	1	1	IRU7	IRU6	IRU5	IRU4	IRU3	IRU2	IRU1	IRU0	
0	0	0	1	0	1	0	0	ORRS3	ORRS2	ORRS1	ORRS0	—	ORP10	ORP9	ORP8	(J) ORACT reset cycle ORACT frequency
0	0	0	1	0	1	0	1	ORP7	ORP6	ORP5	ORP4	ORP3	ORP2	ORP1	ORP0	
0	0	0	1	0	1	1	0	—	—	—	—	—	ORD10	ORD9	ORD8	(K) ORACT fall position
0	0	0	1	0	1	1	1	ORD7	ORD6	ORD5	ORD4	ORD3	ORD2	ORD1	ORD0	
0	0	0	1	1	0	0	0	—	—	—	—	—	ORU10	ORU9	ORU8	(K) ORACT rise position
0	0	0	1	1	0	0	1	ORU7	ORU6	ORU5	ORU4	ORU3	ORU2	ORU1	ORU0	
0	0	0	1	1	0	1	0	—	—	—	—	—	HPRS10	HPRS9	HPRS8	(L) H position counter reset position
0	0	0	1	1	0	1	1	HPRS7	HPRS6	HPRS5	HPRS4	HPRS3	HPRS2	HPRS1	HPRS0	
0	0	0	1	1	1	0	0	—	—	—	—	—	—	—	PRE	(M) Preset
Settings other than those above are invalid																—

Note) PLLP0, HP0, VP0, HSTP0, PCGP0, PRGP0, CLPP0, SHP0, IRD0, IRU0, ORRS0, ORP0, ORD0, ORU0, HPRS0: LSB

Each control data is described in detail below. (A) to (M)

(A) PLLP10, 9, 8, 7, 6, 5, 4, 3, 2, 1, 0

These bits set the frequency division ratio (master clock) of the internal 1/N frequency divider for the PLL. The data is 11 bits and the frequency division ratio can be set up to 2048. The actual frequency division ratio should be set as follows.

Number of clk for the horizontal period − 2 = Actual number of dots set

Examples of settings for major modes are shown below.

Examples using the LCX026

1) SVGA (800 × 600)
PLLP setting value = 1040 (horizontal period) − 2 → 1038 (HLLLLLLHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	L	L	L	L	L	L	H	H	H	L

* VESA SVGA72

2) VGA (640 × 480)
PLLP setting value = 832 (horizontal period) − 2 → 830 (LHHLLHHHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	L	L	H	H	H	H	H	L

* VESA VGA72

3) PC-98 (640 × 400)
PLLP setting value = 848 (horizontal period) − 2 → 846 (LHHLHLLHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	L	H	L	L	H	H	H	L

4) NTSC (640 × 480)
PLLP setting value = 1560 (horizontal period) − 2 → 1558 (HHLLLLHLHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	H	L	L	L	L	H	L	H	H	L

5) PAL (762 × 572)
PLLP setting value = 1880 (horizontal period) − 2 → 1878 (HHHLHLHLHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	H	H	L	H	L	H	L	H	H	L

Examples using the LCX016

1) Macintosh16 (832 × 624)

PLLP setting value = 1152 (horizontal period) – 2 → 1150 (HLLLHHHHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	L	L	L	H	H	H	H	H	H	L

2) SVGA (800 × 600)

PLLP setting value = 1040 (horizontal period) – 2 → 1038 (HLLLLLLHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	L	L	L	L	L	L	H	H	H	L

* VESA SVGA72

3) VGA (640 × 480)

PLLP setting value = 832 (horizontal period) – 2 → 830 (LHHLLHHHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	L	L	H	H	H	H	H	L

* VESA VGA72

4) PC-98 (640 × 400)

PLLP setting value = 848 (horizontal period) – 2 → 846 (LHHLHLLHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	L	H	L	L	H	H	H	L

5) NTSC WIDE (832 × 480)

PLLP setting value = 1014 (horizontal period) – 2 → 1012 (LHHHHHHLHLL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	H	H	H	H	L	H	L	L

6) NTSC (640 × 480)

PLLP setting value = 1560 (horizontal period) – 2 → 1558 (HHLLLLHLHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	H	L	L	L	L	H	L	H	H	L

7) PAL (762 × 572)

PLLP setting value = 1880 (horizontal period) – 2 → 1878 (HHHLHLHLHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	H	H	L	H	L	H	L	H	H	L

Examples using the LCX012BL

1) VGA (640 × 480)

PLLP setting value = 896 (horizontal period) − 2 → 894 (LHHLHHHHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	L	H	H	H	H	H	H	L

* VESA VGA72

2) PC-98 (640 × 400)

PLLP setting value = 848 (horizontal period) − 2 → 846 (LHHLHLLHHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	L	H	H	L	H	L	L	H	H	H	L
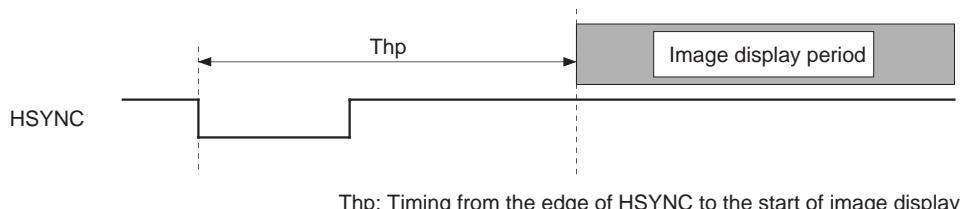
3) NTSC, PAL (640 × 480)

PLLP setting value = 1560 (horizontal period) − 2 → 1558 (HHLLLLHLHHL: LSB)

PLLP	10	9	8	7	6	5	4	3	2	1	0
Setting data	H	H	L	L	L	L	H	L	H	H	L

(B) HP7, 6, 5, 4, 3, 2, 1, 0

These bits set the horizontal display start position. The minimum adjustment width is 1 dot, and adjustment of up to 256 clk with 8 bits is possible using the front edge of HSYNC as the reference.

Thp: Timing from the edge of HSYNC to the start of image display

Minimum and maximum Thp setting values for each mode

LCX026

HP	7	6	5	4	3	2	1	0	800×600	762×572	640×480	640×400
Min.	H	H	H	H	H	H	H	H	161 clk	115 clk		
Max.	L	L	L	L	L	L	L	L	416 clk	370 clk		

LCX016

HP	7	6	5	4	3	2	1	0	832×624	800×600	762×572	640×480	640×400	832×480
Min.	H	H	H	H	H	H	H	H	185 clk	155 clk	109 clk			
Max.	L	L	L	L	L	L	L	L	440 clk	410 clk	364 clk			

LCX012BL

HP	7	6	5	4	3	2	1	0	644×484
Min.	H	H	H	H	H	H	H	H	112 clk
Max.	L	L	L	L	L	L	L	L	367 clk
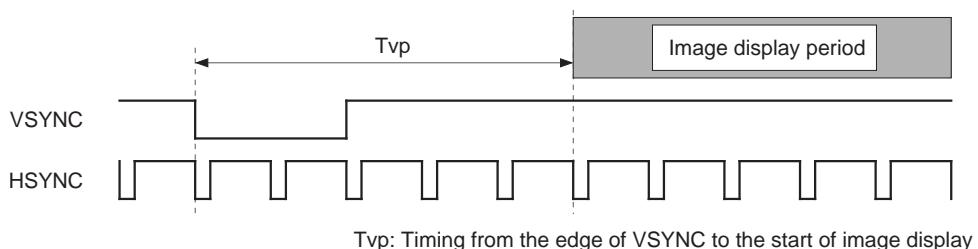
(C) VP7, 6, 5, 4, 3, 2, 1, 0

These bits set the vertical display start position. The minimum adjustment width is 1H, and adjustment of up to 256H with 8 bits is possible using the following references.

Progressive signal input → Front edge of VSYNC

Interlace signal input → First 1H of VSYNC

Here, the interlace signal input indicates NTSC or PAL display (using the built-in double-speed controller). In this case, the image is raised or lowered by two lines on the panel side with respect to a 1H adjustment.
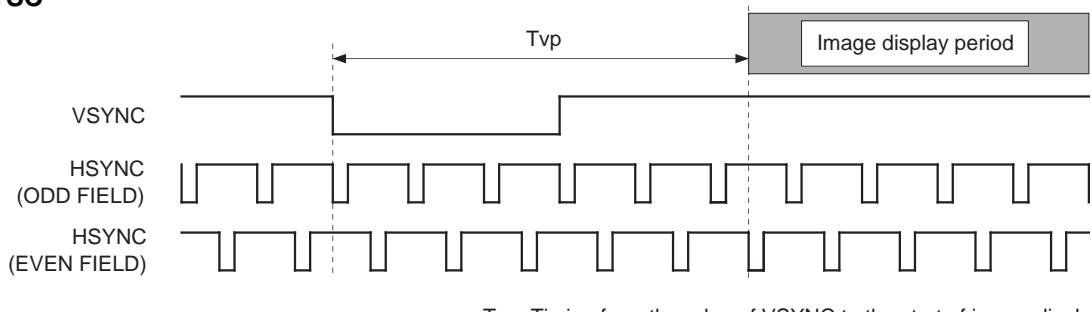
(1) Progressive

Tvp: Timing from the edge of VSYNC to the start of image display

Minimum and maximum Tvp setting values

LCX026

VP	7	6	5	4	3	2	1	0	
Min.	L	L	L	L	L	L	L	L	9H
Max.	H	H	H	H	H	H	H	H	264H

LCX016/LCX012BL

VP	7	6	5	4	3	2	1	0	
Min.	L	L	L	L	L	L	L	L	7H
Max.	H	H	H	H	H	H	H	H	262H

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(2) Interlace

(a) NTSC

Tvp: Timing from the edge of VSYNC to the start of image display
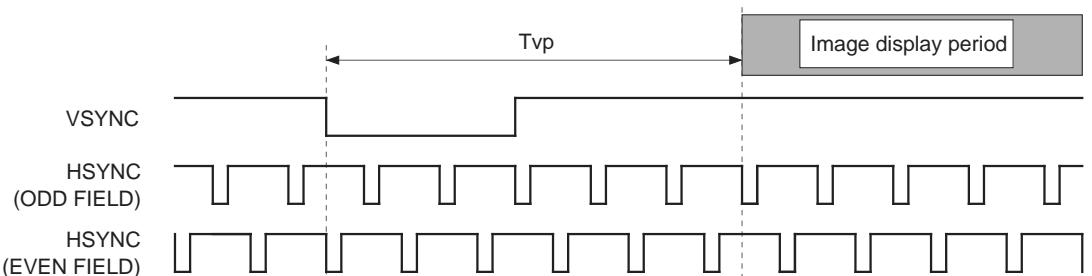
Minimum and maximum Tvp setting values

LCX026

VP	7	6	5	4	3	2	1	0	
Min.	L	L	L	L	L	L	L	L	5.5H
Max.	H	H	H	H	H	H	H	H	260.5H

LCX016/LCX012BL

VP	7	6	5	4	3	2	1	0	
Min.	L	L	L	L	L	L	L	L	4.5H
Max.	H	H	H	H	H	H	H	H	259.5H

(b) PAL

Tvp: Timing from the edge of VSYNC to the start of image display

Minimum and maximum Tvp setting values

LCX026
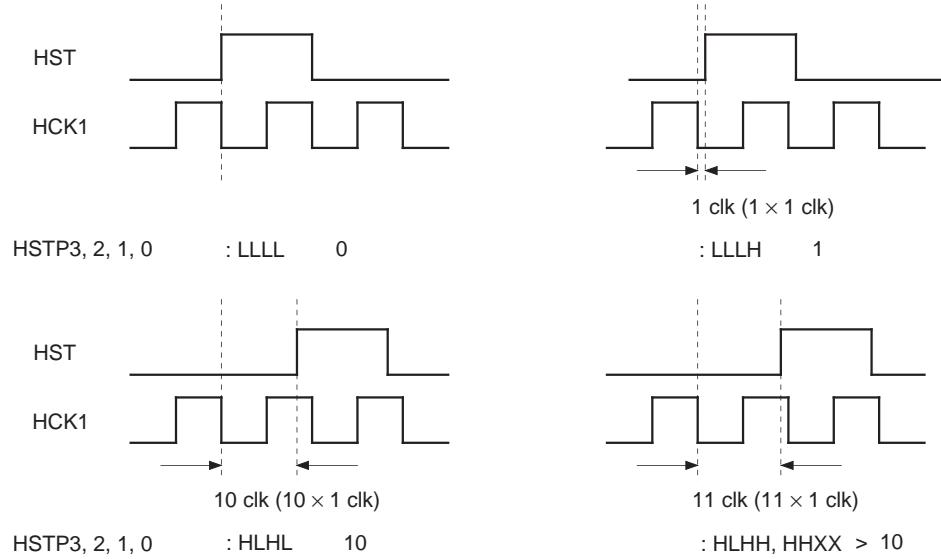
VP	7	6	5	4	3	2	1	0	
Min.	L	L	L	L	L	L	L	L	5.5H
Max.	H	H	H	H	H	H	H	H	260.5H

LCX016/LCX012BL

VP	7	6	5	4	3	2	1	0	
Min.	L	L	L	L	L	L	L	L	4.5H
Max.	H	H	H	H	H	H	H	H	259.5H

(D) HSTP3, 2, 1, 0

These bits control the HST phase relative to HCK, and correct the delay between HST and HCK that occurs within the panel. The phase of 12 position (in 1 clk increments) can be controlled with 4 bits.

HST

HCK1

HSTP3, 2, 1, 0   : LLLL   0

1 clk (1 × 1 clk)

HST

HCK1

HSTP3, 2, 1, 0   : LLLH   1

HST

HCK1

10 clk (10 × 1 clk)

HSTP3, 2, 1, 0   : HLHL   10

HST

HCK1

11 clk (11 × 1 clk)

: HLHH, HHXX > 10

Notes)
1. When setting to the LCX012BL mode, the phases of HST and HCK1, 2 are as shown above regardless of RGT.
2. In the LCX026 and LCX016 modes, when set to the SVGA mode and RGT: L or to a mode other than the SVGA mode and RGT: H, the phase relationship between HST and HCK1, 2 is as shown above.
3. The polarity of HCK1, 2 is reversed when set to panel mode switching, panel display area switching and right/left inversion modes other than as described in notes 1 and 2 above.

(E) PCGP4, 3, 2, 1, 0/PRGP4, 3, 2, 1, 0

These bits set the width of PCG and PRG pulses to 32 positions with 5 bits in 4 clk units.

The rise positions of PCG and PRG pulses are determined by serial data HP (see (B)), modes 1, 2 and 3 (see (H-7)) and PCG (see (H-12)) position. The pulse widths of PCG and PRG can be arbitrarily set within the above range using the rise positions for the reference.

When setting PCGP4, 3, 2, 1, 0 = n (decimal), the panel width at that time is calculated by:

$$(n + 1) \times 4 \ (\text{clk})$$

When setting PCGP4 to 0, the pulse fall position changes relative to the pulse rise position.
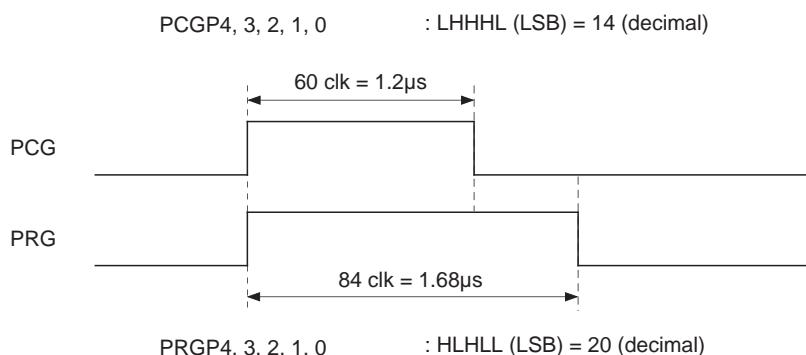
This applies similarly to PRGP4 to 0.

For example, when setting PCGP4, 3, 2, 1, 0: HLLHH = 19 (decimal), the panel width becomes:

$$(19 + 1) \times 4 = 80 \ \text{clk}$$

Since the optimum values for pulse width of PCG and PRG pulses vary according to the LCD panel used, set while also referring to the panel specifications.

Example) MCK: 50MHz (1 clk = 20ns)

PCGP4, 3, 2, 1, 0   : LHHHL (LSB) = 14 (decimal)

60 clk = 1.2μs

PCG

PRG

84 clk = 1.68μs

PRGP4, 3, 2, 1, 0   : HLHLL (LSB) = 20 (decimal)
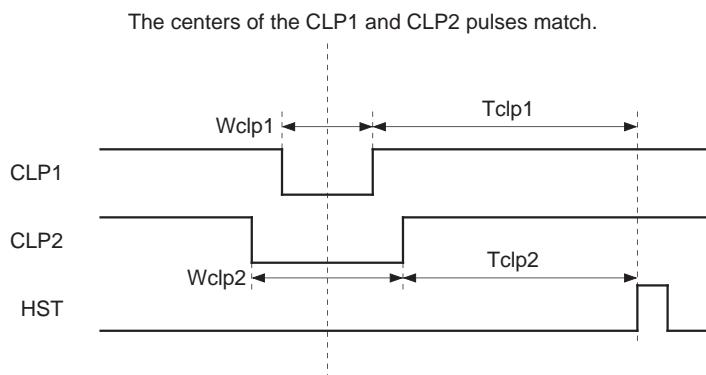
Notes) PCGPOL and PRGPOL are both assumed to be "H".

Polarity is reversed when PCGPOL and PRGPOL are each "L".

(F) CLPP1, 0

These bits adjust the clamp pulse output timing. The timing can be set to 4 positions with 2 bits.

The centers of the CLP1 and CLP2 pulses match.

XGA (LCX026), Macintosh16 (LCX016)

CLPP1	CLPP0	Tclp1	Tclp2	Wclp1	Wclp2	HP Limit (CLP1)	HP Limit (CLP2)
L	L	46 clk	23 clk	69 clk	115 clk	HHHHHHHH (255): LSB	HHHHHHHH (255): LSB
L	H	69 clk	46 clk	69 clk	115 clk		
H	L	92 clk	69 clk	69 clk	115 clk		HHHHLLHH (243): LSB
H	H	115 clk	92 clk	69 clk	115 clk	HHHHLLHH (243): LSB	HHLHHHLL (220): LSB

SVGA (LCX026, LCX016)

CLPP1	CLPP0	Tclp1	Tclp2	Wclp1	Wclp2	HP Limit (CLP1)	HP Limit (CLP2)
L	L	38 clk	19 clk	58 clk	96 clk	HHHHHHHH (255): LSB	HHHHHHHH (255): LSB
L	H	57 clk	38 clk	58 clk	96 clk		
H	L	76 clk	57 clk	58 clk	96 clk		HHHHLHHL (246): LSB
H	H	95 clk	76 clk	58 clk	96 clk	HHHHLHHL (246): LSB	HHHLLLHH (227): LSB

VGA/NTSC, PAL, PC-98 (LCX026, LCX012BL), VGA/NTSC, PAL, PC-98, WIDE (LCX016)

CLPP1	CLPP0	Tclp1	Tclp2	Wclp1	Wclp2	HP Limit (CLP1)	HP Limit (CLP2)
L	L	26 clk	13 clk	38 clk	64 clk	HHHHHHHH (255): LSB	HHHHHHHH (255): LSB
L	H	39 clk	26 clk	38 clk	64 clk		
H	L	52 clk	39 clk	38 clk	64 clk		HHHHHLLL (248): LSB
H	H	65 clk	52 clk	38 clk	64 clk	HHHHHLLL (248): LSB	HHHLHLHH (235): LSB

Note) When CLPP1, 0 is set to HL or HH, the pulses may not be output due to the internal logic depending on the HP serial data setting value. HP Limit is the upper limit for the serial data HP that allows output of CLP1 and 2 pulses when setting each mode.
HSTP is LLHH (LSB) (serial data).

(G) INV, SHP3, 2, 1, 0

This IC allows control of the sample-and-hold position of the CXA2112R sample-and-hold driver by setting serial data in place of not having a sample-and-hold pulse output.
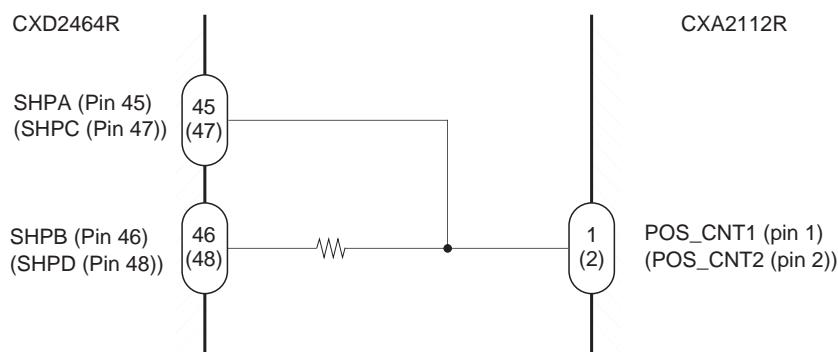
INV set by serial data is output from the INV pin (Pin 49). Connect this INV to INV_CNT (Pin 52) of the CXA2112R.

In addition, data set with SHP3, 2, 1, 0 is reflected in the SHPA, SHPB, SHPC and SHPD output pins (pins 45, 46, 47 and 48) as shown in the table below.

Setting	Output				Setting	Output			
SHP3, 2, 1, 0	SHPA	SHPB	SHPC	SHPD	SHP3, 2, 1, 0	SHPA	SHPB	SHPC	SHPD
LLLL	L	L	L	L	HLLL	L	L	Z	L
LLLH	H	H	L	L	HLLH	H	H	Z	L
LLHL	Z	L	L	L	HLHL	Z	L	Z	L
LLHH	Z	H	L	L	HLHH	Z	H	Z	L
LHLL	L	L	H	H	HHLL	L	L	Z	H
LHLH	L	H	H	H	HHLH	L	H	Z	H
LHHL	Z	L	H	H	HHHL	Z	L	Z	H
LHHH	Z	H	H	H	HHHH	Z	H	Z	H

* Z: High Impedance State

The sample-and-hold position of the CXA2112R can be set by connecting SHPA to SHPD as shown in the diagram below. Refer to the specification of the CXA2112R for further details.

(H) Mode settings

Mode	Mode description	
FLD	FLD pulse output switching (H: FLD, L: CLP2)	H-1
FRP1	FRP polarity inversion cycle switching (H: 1F, L: 2F)	H-2
FRP0	FRP polarity inversion cycle switching (H: 1H, L: F)	
CKTEST0, 1	Test setting (Set to H.)	H-3
RCK	Clock output setting (H: CLK STOP, L: CLK OUT)	H-4
VPOL	Input VSYNC polarity switching (H: Positive, L: Negative)	H-5
HPOL	Input HSYNC polarity switching (H: Positive, L: Negative)	
HDNPOL	HDN pulse output polarity switching (H: Positive, L: Negative)	
CLPPOL	CLP pulse output polarity switching (H: Positive, L: Negative)	
PCGPOL	PCG pulse output polarity switching (H: Positive, L: Negative)	
PRGPOL	PRG pulse output polarity switching (H: Positive, L: Negative)	
MBKB	Skip scan interval switching	H-6
MBKA		
MBK2	Skip scan (FRP) timing switching (H: Main, L: Sub)	
MBK1	Skip scan mode switching (H/H: No skip scan, H/L: 6, 4 skip scan, L/H: 5, 4 skip scan, L/L: 6, 7 skip scan)	
MBK0		
MODE021	Test setting (Set to L.)	H-7
MODEB	Panel mode switching (H/H: LCX026 mode, L/H: LCX016 mode, L/L: LCX012BL mode)	
MODEA		
MODE3	Panel display area switching	
MODE2		
MODE1		
VGAV	Input signal attribute switching (H: Data, L: AV)	H-8
HR	External reset switching (H: No reset, L: Reset)	H-9
DWN	Up/down inversion discrimination signal input (H: Down, L: Up)	H-10
RGT	Right/left inversion discrimination signal input (H: Normal, L: Reverse)	
HST	HST width switching (H: 12 dots wide, L: 24 dots wide)	H-11
PCG	PCG width switching (H: Main, L: Sub)	H-12
DSP	Double-speed mode switching (H: Normal, L: Double-speed)	H-13
PC98	PC-98 (400 line) display switching (H: No display, L: Display)	H-14
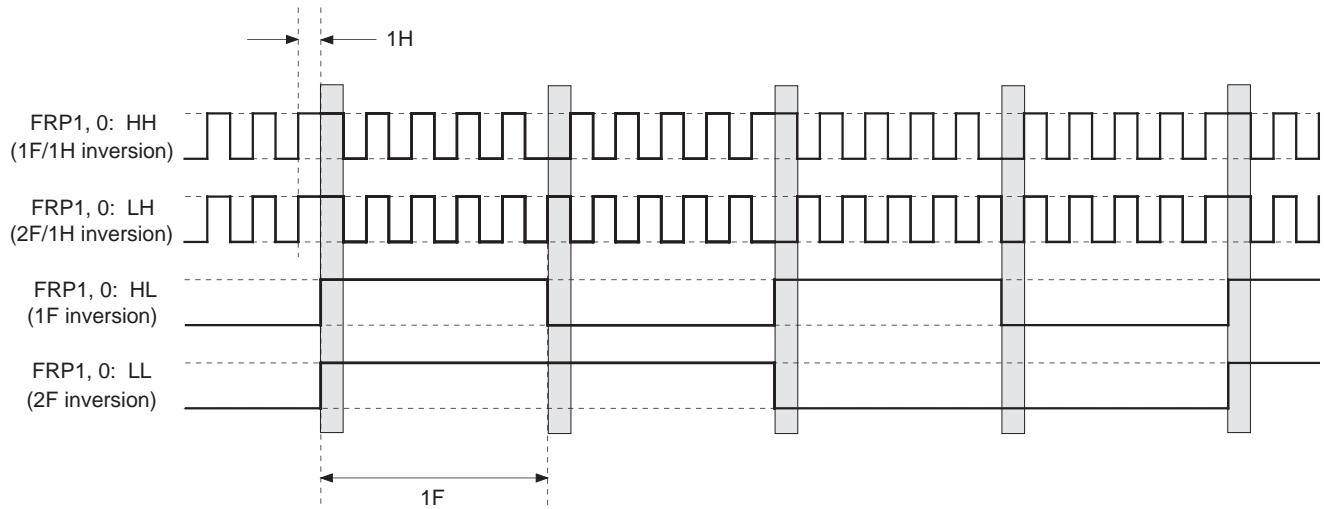
(H-1) FLD

This bit switches the outputs of field identification pulse FLDO and clamp pulse CLP2. The FLDO pulse when FLD is H and the CLP2 pulse when FLD is L are output from Pin 41 (CLP2/FLDO).

Refer to the timing chart for details.

(H-2) FRP1, 0

These bits are the data for switching the LCD AC conversion signal cycle. FRP1, 0 should normally be set to HH.

(H-3) CKTST0, 1

These bits set testing. CKTST0, 1 should normally be set to H.

Note) If these bits are set to L, pulses may not be output normally.
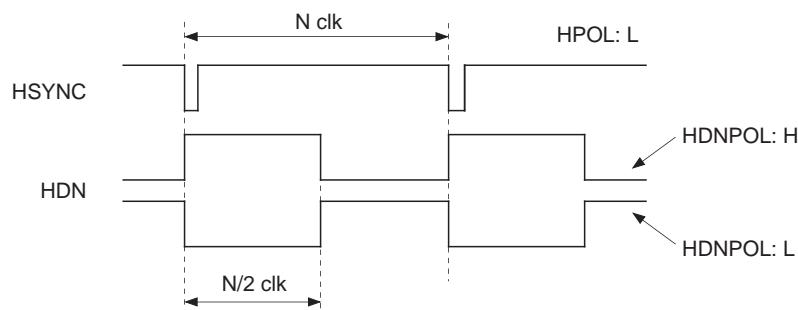
(H-4) RCK

This bit sets testing. RCK should normally be set to H.

(H-5) VPOL, HPOL, HDNPOL, CLPPOL, PCGPOL, PRGPOL

These bits are the data for switching input or output signal polarity. Set these bits according to the explanation below.

(1)   VPOL and HPOL are the data for switching the input vertical and horizontal sync signal polarity. Since signal processing is performed with the sync signal polarity fixed to positive by the internal logic, the data must be switched according to the polarity of the input sync signal.

Therefore, individually set VPOL and HPOL to H when the polarity of the input sync signal is positive, and to L when the polarity is negative.

(2)   The HDN pulse (H return pulse) is the 1/N frequency divider output pulse for the PLL IC. The width of the HDN pulse is calculated according to the setting of PLLP10 to 0 for the value of frequency division N, and that value is N/2. HDNPOL is the data for setting the output polarity of this HDN pulse, and the relationship between its setting and pulse polarity is shown in the diagram below.

(3)   CLPPOL sets the output polarity of clamp pulses CLP1 and CLP2. When CLPPOL is H, both CLP1 and CLP2 have positive polarity, and when CLPPOL is L, both CLP1 and CLP2 have negative polarity.
See the Timing Charts for details.

(4)   PCGPOL and PRGPOL set the output polarity for the PCG and PRG pulses, respectively. When PCGPOL is H, the polarity of the PCG pulse is positive, and when PCGPOL is L, polarity is negative. This applies similarly to the relationship between PRGPOL and PRG pulses.
See the Timing Charts for details.

(H-6) MBK2, 1, 0, B, A
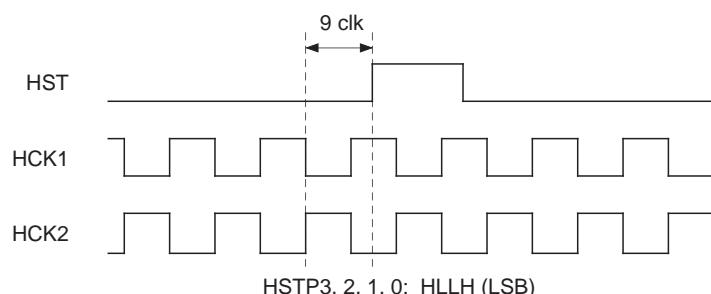
These bits set the skip-scan-related mode timings. These timings enable XGA (scanning line conversion from 768 to 598 vertical lines by 5, 4 skip scan) display for the LCX026, XGA (scanning line conversion from 768 to 615 vertical lines by 6, 4 skip scan) display for the LCX016, and SVGA (scanning line conversion from 600 to 480 vertical lines by 6, 4 skip scan) and double-speed PAL (scanning line conversion from 575 to 480 vertical lines by 6, 7 skip scan) display for the LCX012BL. However, for XGA and SVGA display, the horizontal direction is supported by external signal processing.

Note) Supported input signals (XGA, SVGA) differ for each panel. Use the XGA skip scan display of the LCX026 in the XGA mode, the XGA skip scan display of the LCX016 in the Macintosh16 mode, and the SVGA skip scan display of the LCX012BL in the VGA or SVGA mode. At that time, the display area other than the image display area is written by the blanking level of the video signal according to the mode.
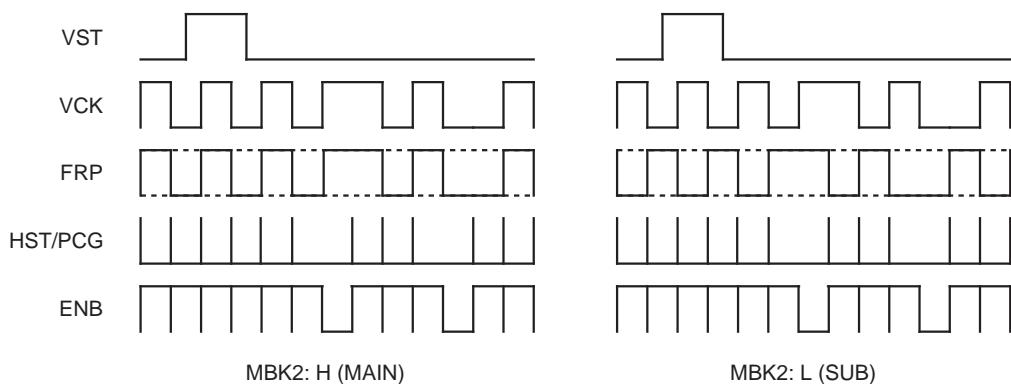
Setting during LCX026 panel driving

When the input signal is XGA (1024 × 768), set the operation of the CXD2464R to the XGA mode of the LCX026, and set the serial data HSTP to HSTP3/2/1/0: HLLH (LSB).
See the Timing Charts for details.
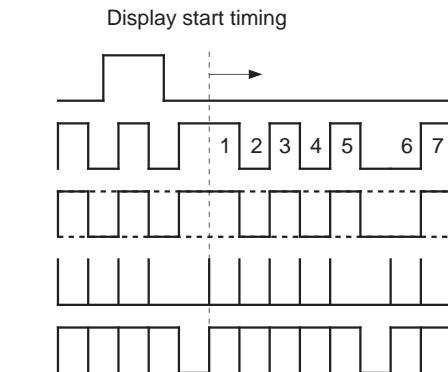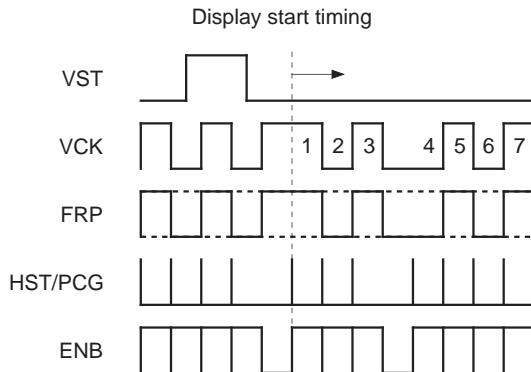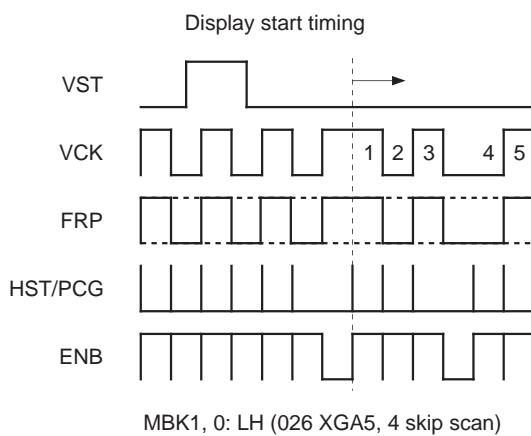
(1) MBK2
This bit sets the FRP-related skip scan timing.

(2) MBK1, 0

These bits set the skip scan mode. Select the XGA, SVGA or double-speed PAL skip scan mode.

MBK1, 0	Skip scan mode
LL	6, 7 skip scan
LH	5, 4 skip scan
HL	6, 4 skip scan
HH	No skip scan

MBK1, 0: LH (026 XGA5, 4 skip scan)

MBK1, 0: HL (016 XGA, 012BL SVGA6, 4 skip scan)

ODD/EVEN FIELD
MBK1, 0: LL (012BL double-speed, PAL6, 7 skip scan)
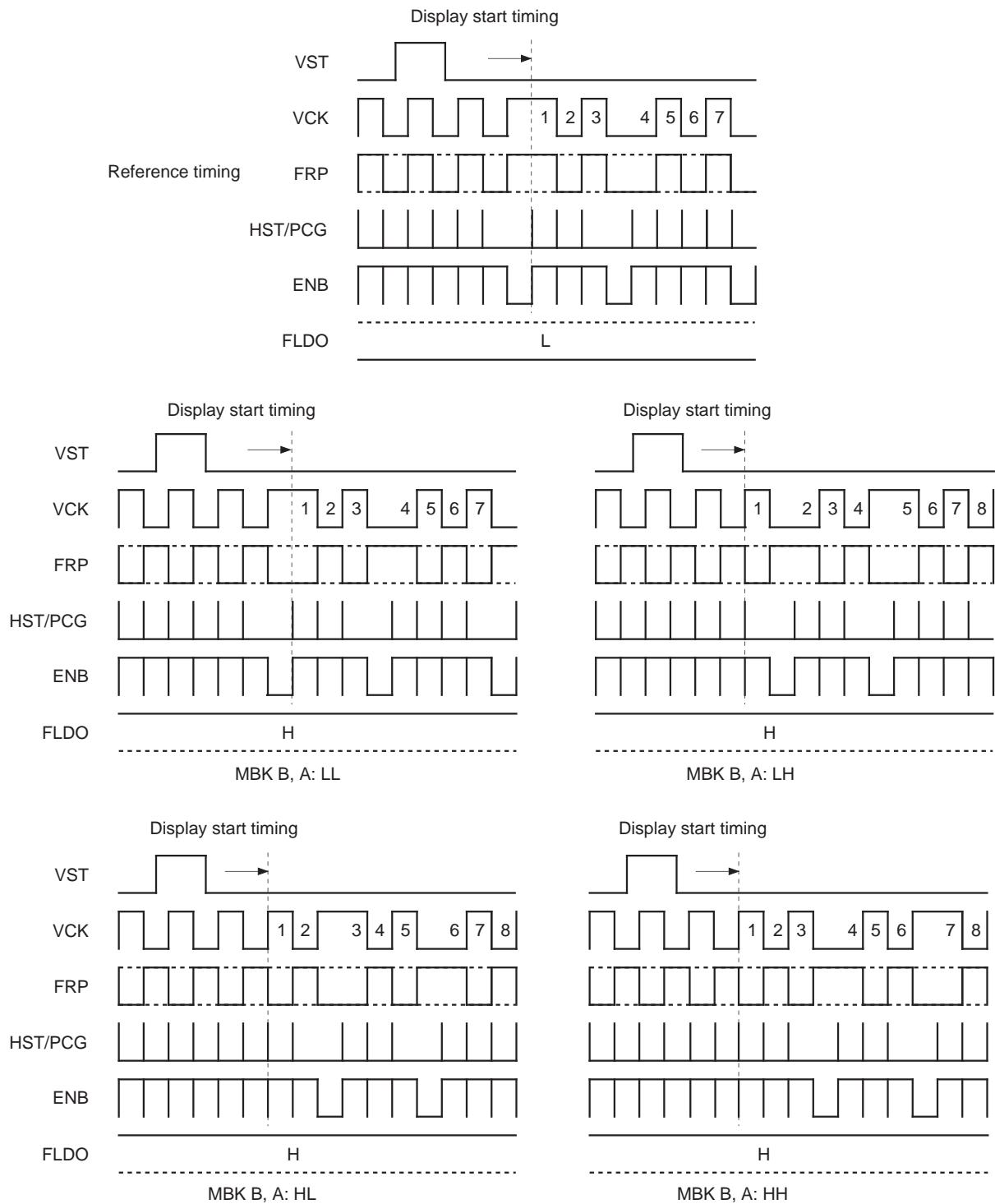
Note) MBK2: H and MBKB, A: LL.

(3) MBK B, A

These bits change skip scan timing for each field (interlace) or for each V cycle (progressive). These bits determine the skip scan timing for the next 1V period using the skip scan timing when the field identification pulse (FLDO) is L as the reference. The optimal skip scan position can be set by setting a skip scan interval of 0 to 3H.

Although the charts below show 5, 4 skip scan timing, but the timing is the same for 6, 4 and 6, 7 skip scan.

Display start timing

Reference timing: VST, VCK, FRP, HST/PCG, ENB, FLDO (L)

MBK B, A: LL

MBK B, A: LH

MBK B, A: HL

MBK B, A: HH

Note) MBK2: H, MBK1, 0: LH

(H-7) MODE021

These bits are a test mode. MODE021 should normally be set to L.

(1) MODE B, A

These bits switch each timing according to the mode. Operation shifts to LCX026 mode when MBKB, A is HH, to LCX016 mode when LH, and to LCX012BL mode when LL. Be sure to set this data when using the CXD2464R in these modes.

MODE B, A	Panel
LL	LCX012BL
LH	LCX016
HH	LCX026

(2) MODE3, 2, 1

These bits switch the panel display area. However, since the panel display area cannot be switched for the LCX012BL, VGA/NTSC mode should be set when using the LCX012BL.

In addition, set to the XGA mode during XGA skip scan display using the LCX026, and to the Macintosh16 mode during XGA skip scan display using the LCX016.

When using the LCX026

MODE	1	2	3
XGA (804×604)	L	L	L
SVGA (804×604)	L	L	H
PAL (762×572)	L	H	L
VGA/NTSC (644×484)	L	H	H
PC-98 (644×404)	H	L	L

* XGA skip scan display

When using the LCX016

MODE	1	2	3
Macintosh16 (832×624)	L	L	L
SVGA (800×600)	L	L	H
PAL (762×572)	L	H	L
VGA/NTSC (640×480)	L	H	H
PC-98 (640×400)	H	L	L
WIDE (832×480)	H	L	H

When using the LCX012BL

MODE	1	2	3
VGA/NTSC (644×484)	L	H	H

* Also supports PAL display.

(H-8) VGAV

This bit switches the CXD2464R according to the attributes of the input signal. The CXD2464R supports input of data signals when VGAV is set to H, and input of interlaced video signals when set to L. Only the double-speed NTSC, PAL and WIDE (LCX016 only) modes are supported, when using the built-in double-speed controller. Set VGAV to L during input of these signals.

(H-9) HR

This bit controls the input horizontal sync signal (HSYNC)-based PLL counter reset operation, and supports external clock input. (Reset operation is allowed when HR is L.)
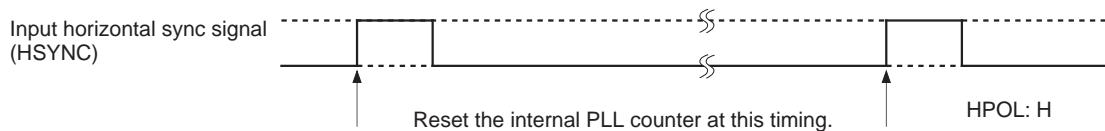
Resetting the internal PLL counter at the front edge of the input HSYNC generates an output pulse synchronized to HSYNC.

This function should be used with systems which do not use a PLL.

In addition, set the PLL frequency division ratio (1/N) resulting from the use of this mode according to:

Number of clk for the horizontal period – 2 = Actual number of clk set

(see page 16).

Reset the internal PLL counter at this timing.   HPOL: H

Note) Since H-POSITION specifications described in this data sheet are not satisfied due to the configuration of the internal logic, the screen center must be adjusted each time.

(H-10) DWN, RGT

These bits set the up/down and right/left inversion discrimination data. These settings allow display to be performed in accordance with each display system.

See the Timing Charts for details.
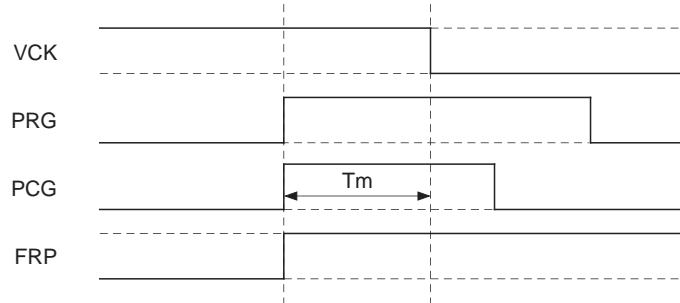
(H-11) HST

This bit adjusts the HST width. HST should normally be set to H.

(H-12) PCG

This bit adjusts the rise (fall) position (pulse starting timing) of the PCG pulse using VCK as a reference. This is linked with PRG and FRP.

Timing at that time. PCG should normally be set to H.

Note) PCGPOL: H, PRGPOL: H

Tm value for each mode

MODE	PCG = H	PCG = L
	Tm	Tm
XGA, Macintosh16	57 clk	46 clk
SVGA	48 clk	38 clk
PAL	32 clk	26 clk
VGA/NTSC		
PC-98		
WIDE		

(H-13) DSP
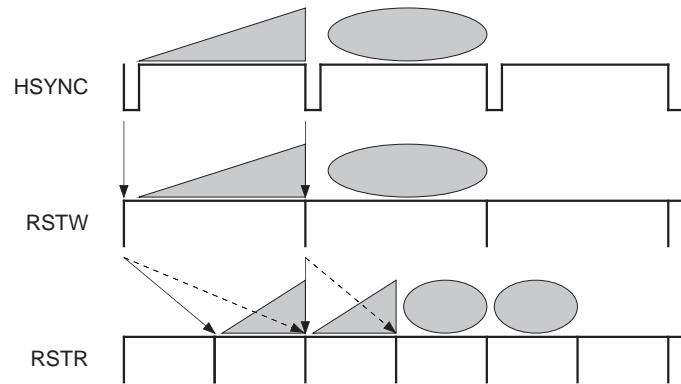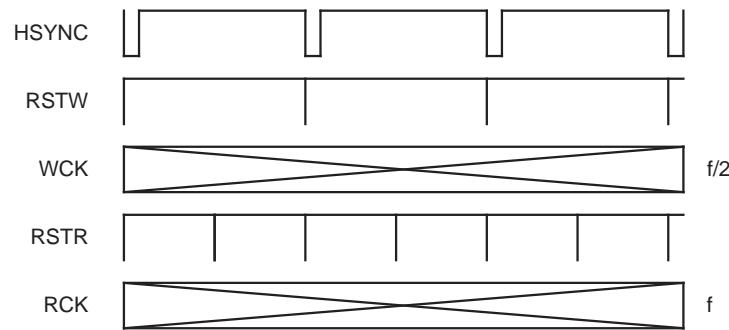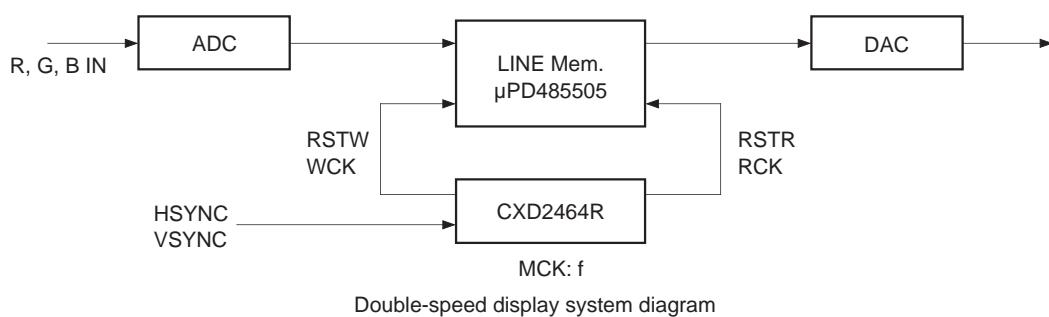
This bit performs the double-speed display mode switching settings. Operation shifts to double-speed display mode when DSP is L. However, DSP should be set H for other modes.

This function is only supported when the built-in double-speed controller is used. This controller is designed to use the µPD485505 (NEC/high-speed line buffer) as the system line memory IC, and generates the double-speed processing pulses RSTW (reset write), WCK (write clock), RSTR (reset read) and RCK (read clock).

The operation of the µPD485505 is as follows. Write operation is started at the RSTW timing, and this memory data is read at double speed at the RSTR timing which is delayed by 1/2H from the RSTW timing. Labeling the master clock frequency (MCK) as f, the write and read clock frequencies at this time are expressed as f/2 and f, respectively.

However, the master clock should have a frequency of 33.3MHz or less when using this mode.

See the IC specifications for a detailed description of µPD485505 operation.

Double-speed display system diagram

Double-speed display timing

Note) See the Timing Charts for details.
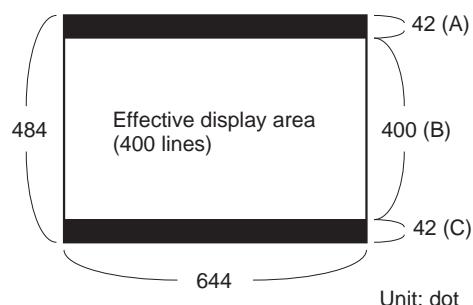
(H-14) PC-98

This bit switches the PC-98 (400-vertical line) display mode. Operation shifts to PC-98 mode when PC98 is L. However, since this function supports the LCX012BL, PC98 is normally (modes other than LCX012BL/PC-98 mode) set H.
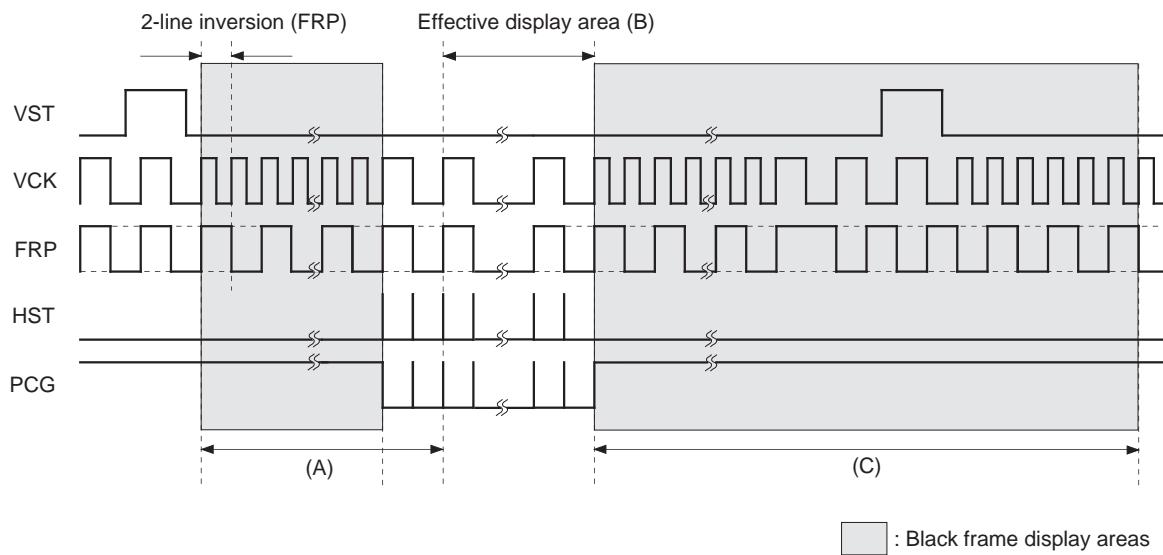
This function is used to display PC-98 (640 × 400) images in the display area of the LCX012BL (644 × 484). The upper and lower 42 lines outside of the display area are black display during this mode.

The vertical high-speed scanning and precharge black writing methods have been introduced as methods for writing these black areas. VCK is shifted to double-speed operation to realize vertical double-speed transfer and enable black display within the limited V blanking. Also, the black level during this period is determined by the PSIG (LCX012BL) level and written at the PCG (LCX012BL) timing.

At this time, HST is masked, limiting the video signal input.

LCX012BL panel

PC-98/400-line display timing

Note) FRP is inverted every two lines during double-speed scanning.
See the Timing Charts for details.

(I) to (L) Scan converter pulse settings

The following settings are not required when not using the scan converter or digital signal driver CXD2449Q.
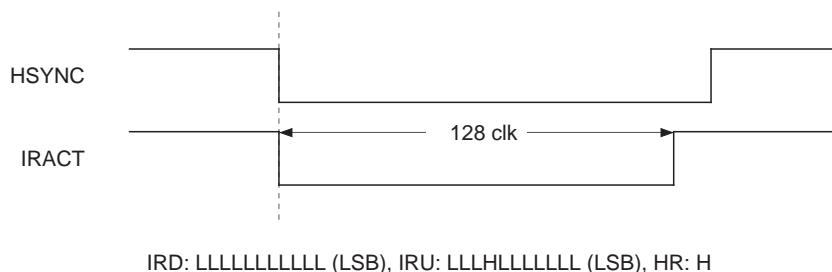
(I-1) SLLAP
SLLAP is used when converting the number of pixels using the scan converter, when the clock differs between input signals and output signals, etc.

SLLAP should be L during the normal operating mode.

SLLAP should be H when operating with CKI1 synchronized only with input signals of the internal circuits of the IC, serial interface, PLL counter and phase comparator, and other components are operated with CKI2.
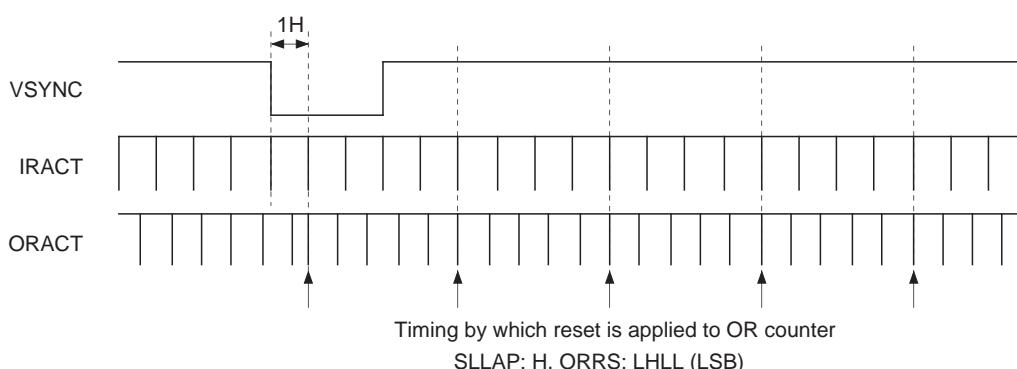
(I-2) IRD10 to 0, IRU10 to 0
IRACT is an output pulse in sync with input HSYNC at an arbitrary position and width. Set the pulse fall position for IRD10 (MSB) to IRD0 (LSB), and the pulse rise position for IRU10 (MSB) to IRU0 (LSB). The setting range is from 0 to N − 1. In addition, do not set IRD and IRU to the same value.

IRD: LLLLLLLLLLL (LSB), IRU: LLLHLLLLLLL (LSB), HR: H

(J-1) ORRS3, 2, 1, 0
When SLLAP is set L, ORACT pulse is completely identical to IRACT pulse when serial data SLLAP is L, and when SLLAP is set H, this is generated from a dedicated counter (loop counter similar to the PLL counter, and referred to as an OR counter) that operates by CKI2, an asynchronous clock that is independent from the input signal. In addition, pulses for LCD panel driving are also generated at this time based on the output of this counter, enabling the LCD panel to be driven with a horizontal cycle and clock that differ from the input signal.

The above OR counter applies a reset with VSYNC and a fixed cycle input HSYNC in order to be in sync with input HSYNC. ORRS3, 2, 1, 0 perform this reset by HSYNC every H seconds or a cycle is set. When ORRS3, 2, 1, 0 (LSB) are set to LLLL, reset is applied for 16H cycles, and at the set number of cycles when set to other settings. Reset can be applied from 1H to a maximum of 16H cycles.

Timing by which reset is applied to OR counter
SLLAP: H, ORRS: LHLL (LSB)

(J-2) ORP10 to 0

ORP sets the number of frequency divisions of the OR counter described above. Similar to PLLP10 to 0, up to 2048 divisions can be set with 11 bits of data. Set the actual number of frequency divisions M as follows:

$\qquad$ M − 2 = actual number of clk set

(K) ORD10 to 0, ORU10 to 0
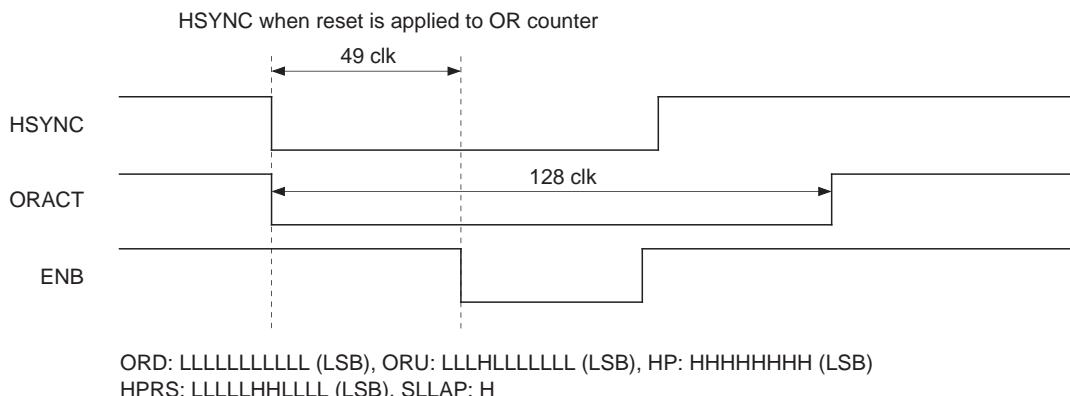
ORACT pulses can be output at an arbitrary position and width of the OR counter operated by clock CKI2 that is asynchronous with input HSYNC when serial data SLLAP is set H.

Set the pulse fall position for ORD10 (MSB) to ORD0 (LSB), and the pulse rise position for ORU10 (MSB) to ORU0 (LSB). The setting range is from 0 to M − 1. In addition, similar to IRACT, do not set ORD and ORU to the same value.

As previously mentioned, when serial data SLLAP is L, ORACT pulses are identical to IRACT pulses regardless of the settings for serial data ORU and ORD.

(L) HPRS10 to 0

Although the counter (H position counter) that generates horizontal display pulses is normally reset based on the PLL counter, when serial data SLLAP is H, reset can be applied to the horizontal direction display counter at an arbitrary position according to an 11-bit setting HPRS based on the OR counter. Consequently, the horizontal display starting position can be varied over a wide range. Setting of serial data HP7 to 0 becomes valid at this time.

ORD: LLLLLLLLLLL (LSB), ORU: LLLHLLLLLLL (LSB), HP: HHHHHHHH (LSB)
HPRS: LLLLLHHLLLL (LSB), SLLAP: H

(M) PRE

This bit sets preset.

Internal preset is reflected in the output when PRE is set L, and serial data settings are reflected in the output when PRE is set H. When the power is turned on, all internal systems are reset, and serial data PRE is set L. Namely, the CXD2464R is in the preset setting status. Always make sure to make all necessary settings before canceling this status (by setting PRE H). If serial data PRE is set H before making all required serial settings, all serial data that has not been set is set L.

When serial settings have been changed when PRE is set H, those settings are immediately reflected in the output.

After XCLR (system reset) Pin 19 is set L to reset the system, serial data PRE is set L and the CXD2464R enters preset setting status even after the power has been turned on. Make all required settings similar to when turning on the power after XCLR has been set H.

The preset setting is VESA SVGA72 (horizontal frequency: 48.08kHz, vertical frequency: 72.19Hz, dot clock: 50.00MHz). Detailed setting values are as shown below.

```
    Address              Data
MSB          LSB
  0 0 0 0 0 0 0 0    PLLP10 to 8: HLL (LSB)
  0 0 0 0 0 0 0 1    PLLP7 to 0: LLLLHHHL (LSB)
  0 0 0 0 0 0 1 0    HP7 to 0: HHHLHLLH (LSB)
  0 0 0 0 0 0 1 1    VP7 to 0: LLLHLLHL (LSB)
  0 0 0 0 0 1 0 0    HSTP3 to 0: LLLH (LSB)
  0 0 0 0 0 1 0 1    PCGP4 to 0: LHHHL (LSB)
  0 0 0 0 0 1 1 0    PRGP4 to 0: HLHLL (LSB)
  0 0 0 0 0 1 1 1    CLPP1 to 0: LL (LSB)
  0 0 0 0 1 0 0 0    INV: L,   SHP3 to 0: LLLL (LSB)
  0 0 0 0 1 0 0 1    FLD: L,   FRP1 to 0: HH (LSB),   CKTST: H,   RCK: H
  0 0 0 0 1 0 1 0    VPOL: H,   HPOL: H,   HDNPOL: H,   CLPPOL: H,   PCGPOL: H,   PRGPOL: H
  0 0 0 0 1 0 1 1    MBKB, A: LL,   MBK2, 1, 0: HHH
  0 0 0 0 1 1 0 0    MODE021: L,   MODEB, A: HH,   MODE3, 2, 1: HLL
  0 0 0 0 1 1 0 1    VGAV: H,   HR: L,   DWN: H,   RGT: H,   HST: H,   PCG: H,   DSP: H,   PC98: H
  0 0 0 1 0 0 0 0    SLLAP: L,   IRD10 to 8: LLL (LSB)
  0 0 0 1 0 0 0 1    IRD7 to 0: LLLLLLLL (LSB)
  0 0 0 1 0 0 1 0    IRU10 to 8: LLL (LSB)
  0 0 0 1 0 0 1 1    IRU7 to 0: HLLLLLLL (LSB)
  0 0 0 1 0 1 0 0    ORRS3 to 0: LLLH (LSB),   ORP10 to 8: LHH (LSB)
  0 0 0 1 0 1 0 1    ORP7 to 0: HHHLLHHL (LSB)
  0 0 0 1 0 1 1 0    ORD10 to 8: LLL (LSB)
  0 0 0 1 0 1 1 1    ORD7 to 0: LLLLLLLL (LSB)
  0 0 0 1 1 0 0 0    ORU10 to 8: LLL (LSB)
  0 0 0 1 1 0 0 1    ORU7 to 0: HLLLLLLL (LSB)
  0 0 0 1 1 0 1 0    HPRS10 to 8: LLL (LSB)
  0 0 0 1 1 0 1 1    HPRS7 to 0: LLLLLLLL (LSB)
  0 0 0 1 1 1 0 0    PRE: L
```
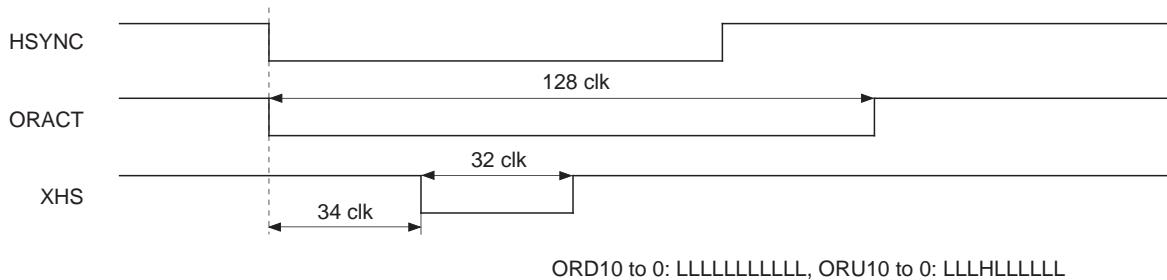
XHS and XVS Pulses

Introduction

XHS and XVS pulses are pulses for digital signal driver CXD2449Q sync signal input. XHS and XVS do not support systems using the built-in double-speed controller. Use the double-speed scan converter (CXD2428Q) with the CXD2449Q during NTSC or PAL double-speed display.
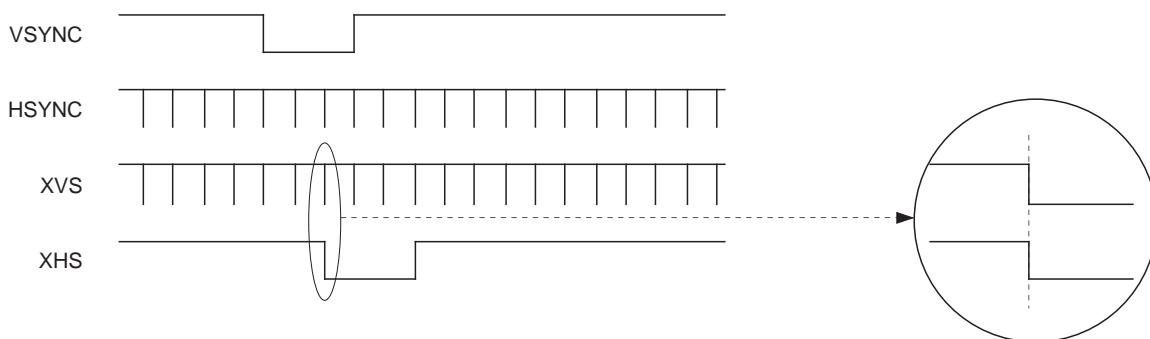
XHS pulses

XHS pulses are output with negative polarity in 32 clock widths 34 clocks after the fall of the IRACT pulse when serial data SLLAP is L. Similarly, XHS pulses are output with negative polarity in 32 clock widths 34 clocks after the fall of the ORACT pulse when serial data SLLAP is H. Therefore, in order to output XHS pulses correctly, respectively set serial data IRD10 to 0 and IRU10 to 0 when serial data SLLAP is L, and ORD10 to 0 and ORU10 to 0 when serial data SLLAP is H.

ORD10 to 0: LLLLLLLLLLL, ORU10 to 0: LLLHLLLLLL
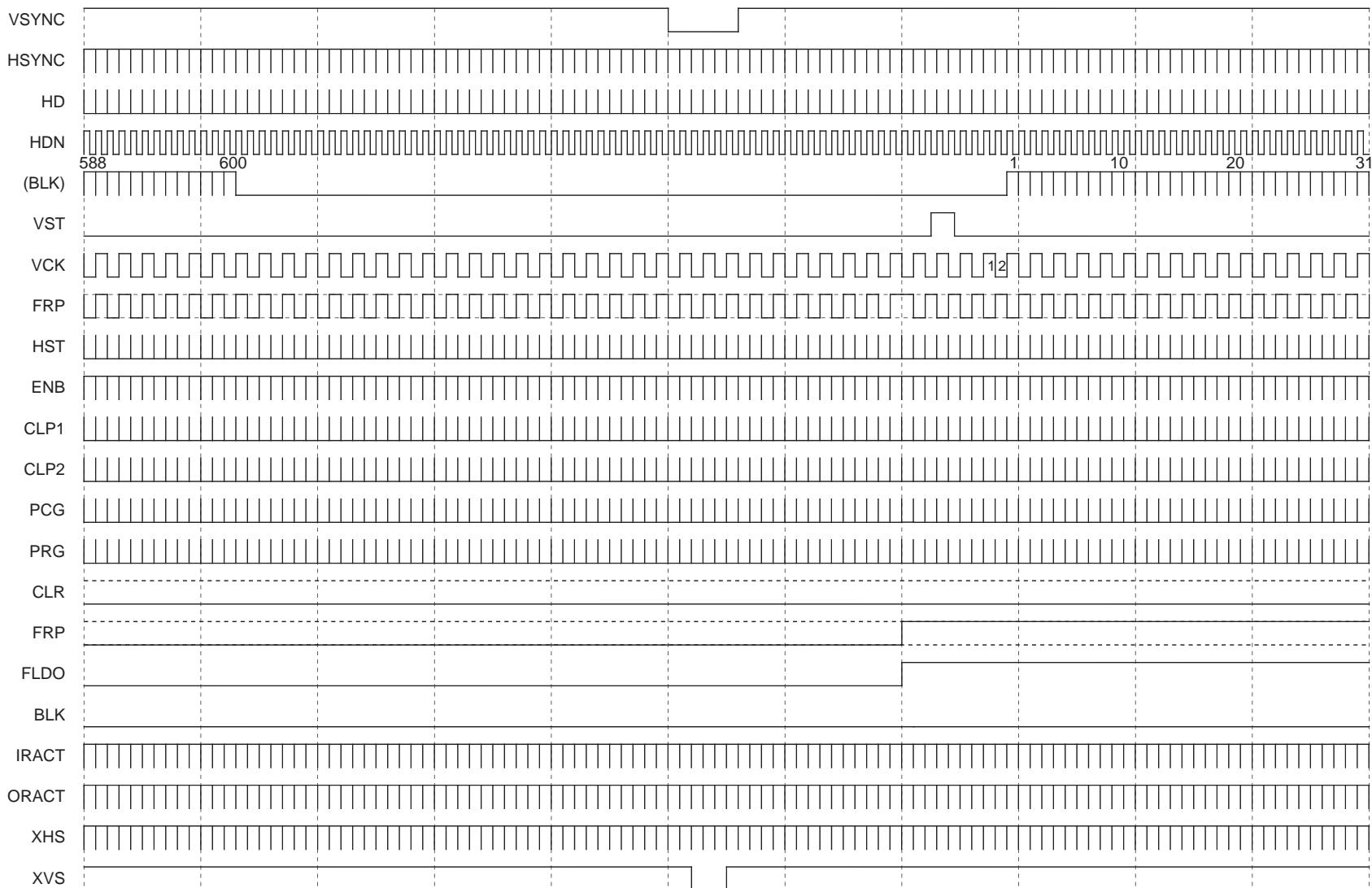
XVS pulses

XVS pulses are output with negative polarity in 3H widths 2H after the vertical sync signal. The phase relationship between XHS and XVS pulses at this time is as shown in the diagram below.

Note) XHS and XVS pulses output ENB and BLK pulses (negative polarity), respectively, for the sake of convenience when using the built-in double-speed controller.

LCX026 SVGA 800 × 600

MODE3/2/1 : H/L/L   MODE B/A : H/H   MODE021 : L   DWN : H   VP : LLLHLLHL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : H
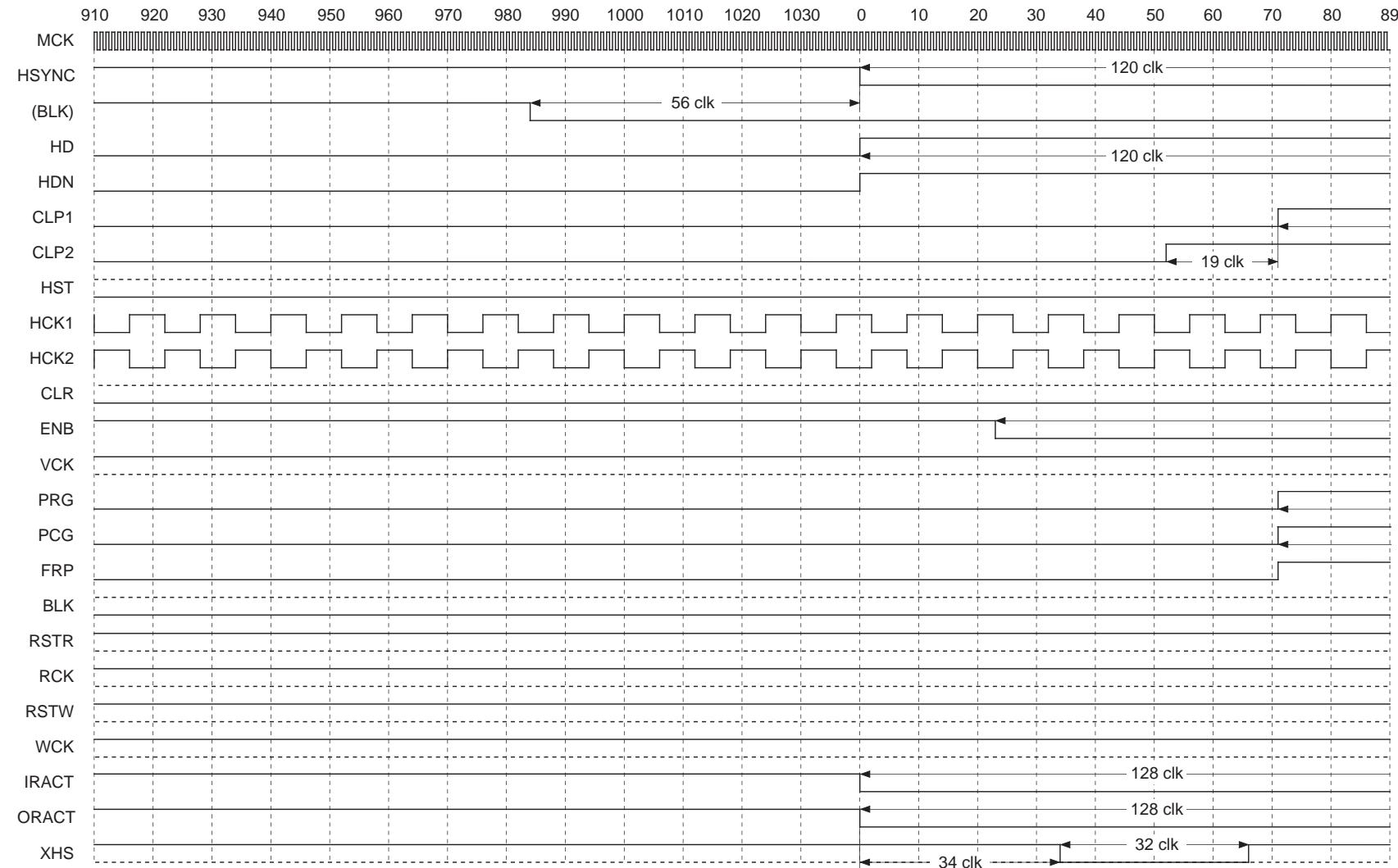

Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP and FLDO polarity are not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX026 SVGA_1 800 × 600

Note) When RGT is Low, HCK1 and 2 are inversed.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

SONY

CXD2464R

LCX026 SVGA_2 800 × 600

RGT : H   PLLP : HLLLLLLHHHL (LSB)   HP : HHHLHLLL (LSB)   HSTP : LLHH (LSB)   PCGP : LHHHL (LSB)   PRGP : HLHLL (LSB)

CLPP : LL (LSB)   HPOL : L   HDNPOL : H   CLPPOL : H   PCGPOL : H   PRGPOL : H   HR : H   HST : H   PCG : H   DSP : H

Loop Counter : 1040 clk
MCK f : 50.00MHz (20.00ns)

Note) When RGT is Low, HCK1 and 2 are inversed.
       The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

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CXD2464R

LCX026　VGA　640 × 480

MODE3/2/1 : H/H/L　MODE B/A : H/H　MODE021 : L　DWN : H　VP : LLLHLHLL (LSB)　MBK2/1/0/B/A : H/H/H/L/L　FRP1/0 : H/H　VPOL : L　VGAV : H　PC98 : H
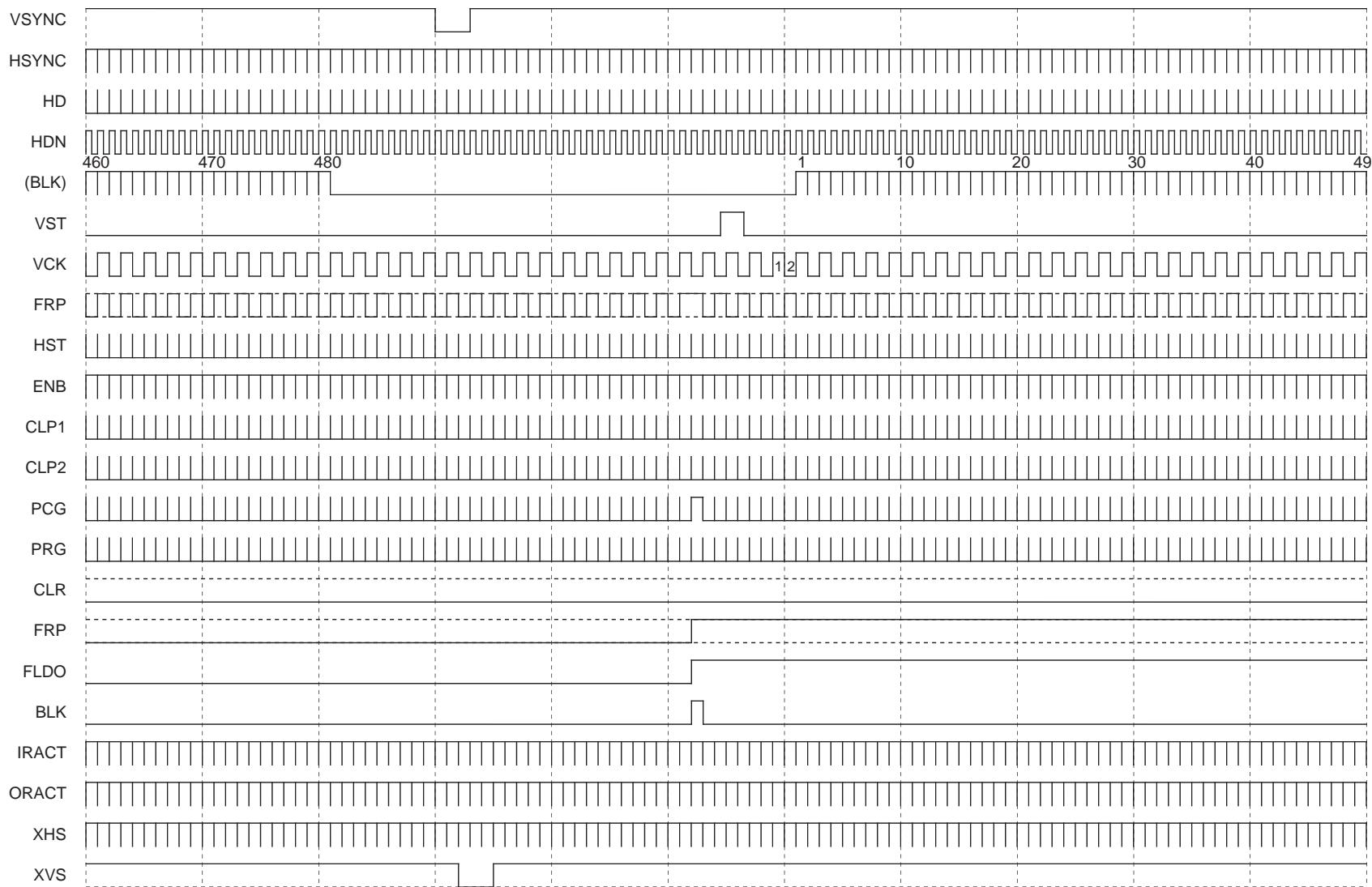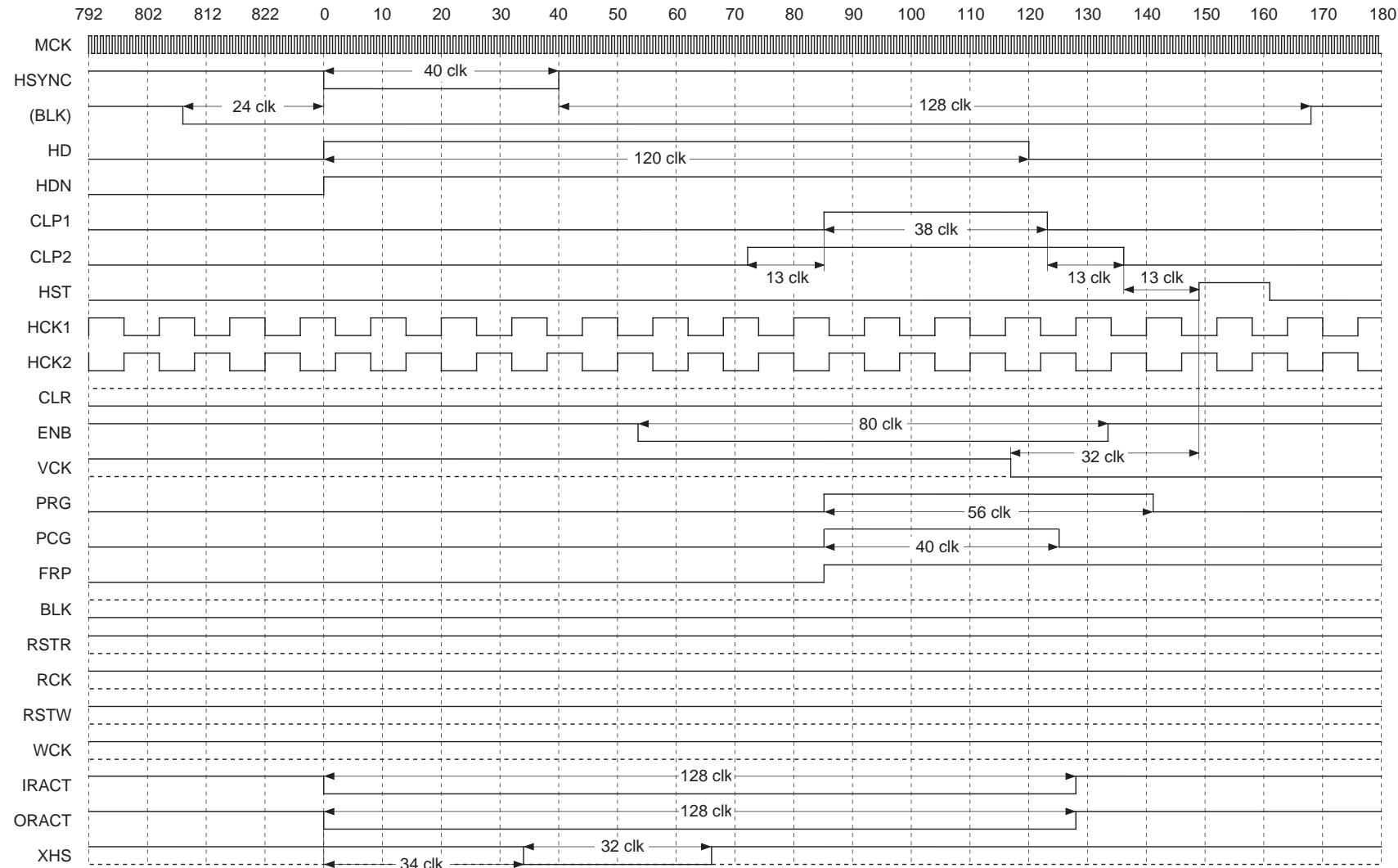
Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP and FLDO polarity are not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX026   VGA   640 × 480

RGT : H   PLLP : LHHLLHHHHHL (LSB)   HP : HHLLHLHL (LSB)   HSTP : LLHH (LSB)   PCGP : LHLLH (LSB)   PRGP : LHHLH (LSB)
CLPP : LL (LSB)   HPOL : L   HDNPOL : H   CLPPOL : H   PCGPOL : H   PRGPOL : H   HR : H   HST : H   PCG : H   DSP : H

Loop Counter : 832 clk
MCK f : 31.50MHz (31.75ns)

Signals (top scale): 792 802 812 822 0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170 180

MCK

HSYNC — 40 clk

(BLK) — 24 clk — 128 clk

HD — 120 clk

HDN

CLP1 — 38 clk

CLP2 — 13 clk   13 clk   13 clk

HST

HCK1

HCK2

CLR

ENB — 80 clk

VCK — 32 clk

PRG — 56 clk

PCG — 40 clk

FRP

BLK

RSTR

RCK

RSTW

WCK

IRACT — 128 clk

ORACT — 128 clk

XHS — 34 clk   32 clk
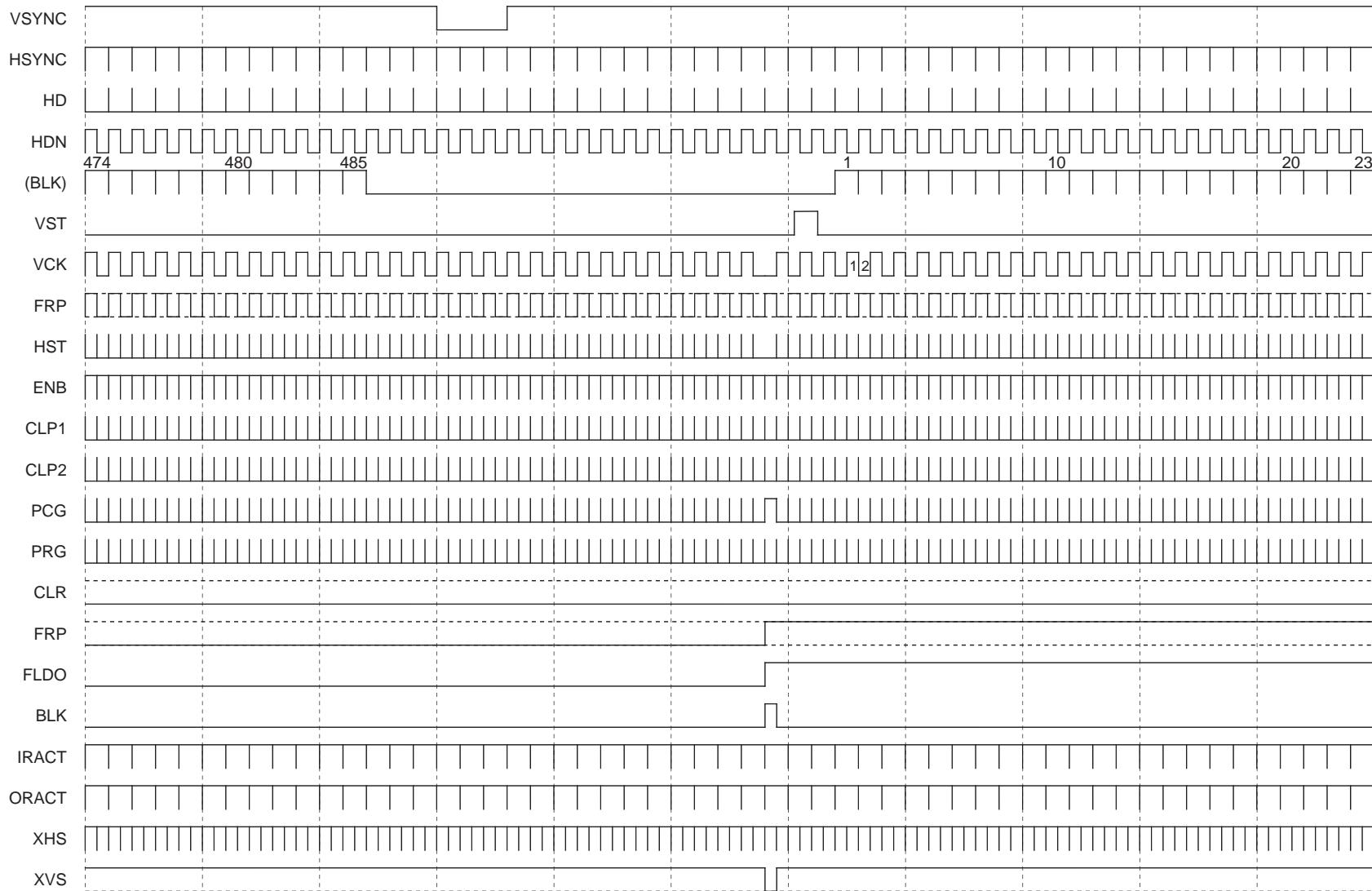
Note) When RGT is Low, HCK1 and 2 are inversed.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX026   NTSC (ODD)   640 × 480

MODE3/2/1 : H/H/L   MODE B/A : H/H   MODE021 : L   DWN : H   VP : LLLLHHLL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : L   PC98 : H
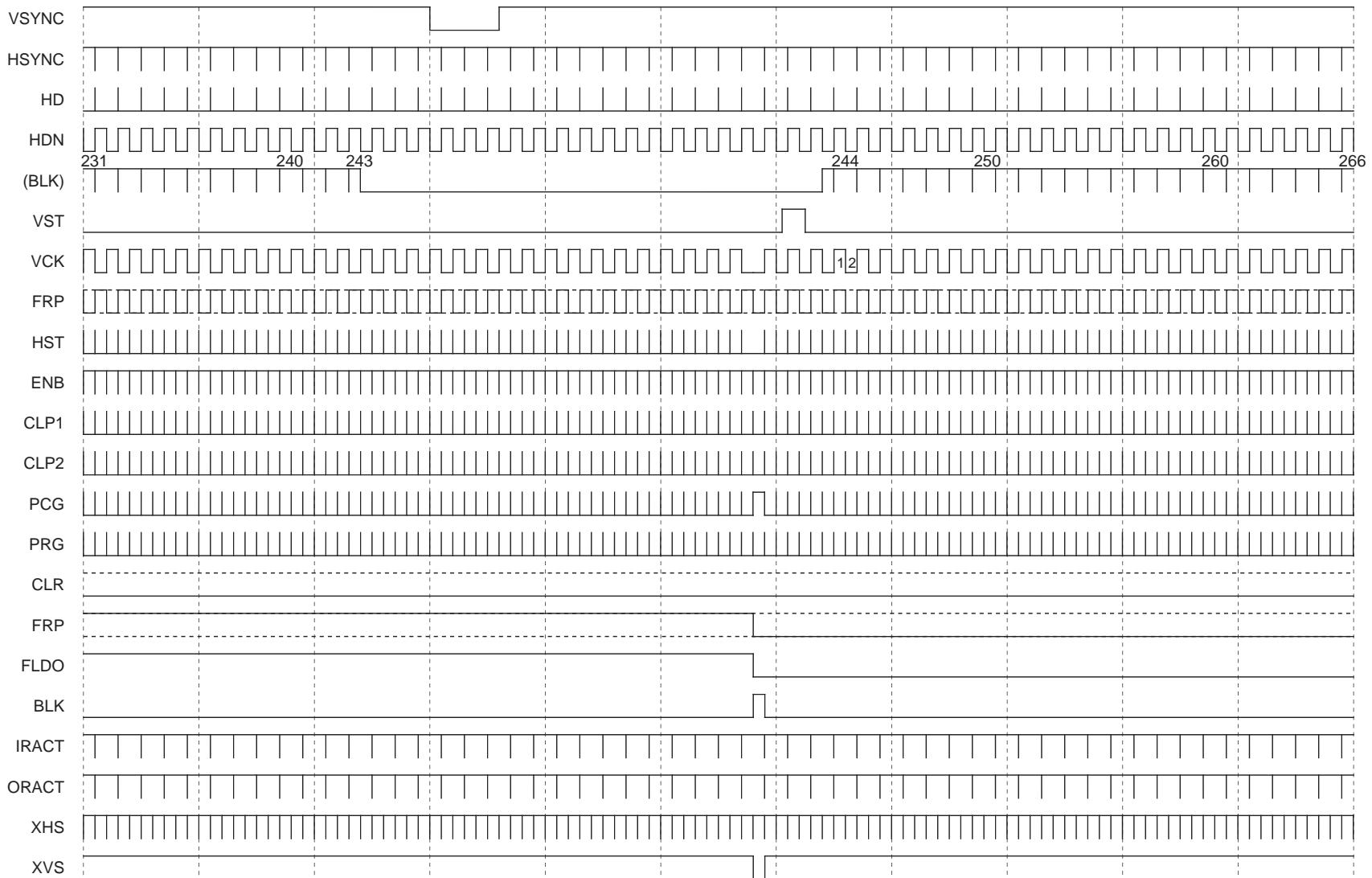

Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP polarity is not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX026　NTSC (EVEN)　640 × 480

MODE3/2/1 : H/H/L　MODE B/A : H/H　MODE021 : L　DWN : H　VP : LLLLHHLL (LSB)　MBK2/1/0/B/A : H/H/H/L/L　FRP1/0 : H/H　VPOL : L　VGAV : L　PC98 : H

VSYNC

HSYNC

HD

HDN

(BLK)

VST

VCK

FRP

HST

ENB

CLP1

CLP2

PCG

PRG

CLR

FRP

FLDO

BLK

IRACT

ORACT

XHS

XVS

231　　240　243　　　　　　　　　　　　244　　250　　　　260　　266

1 2

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Note) When DWN is Low, VST is inversed.
　　　The 1H and 1V cycle FRP polarity is not specified.
　　　The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
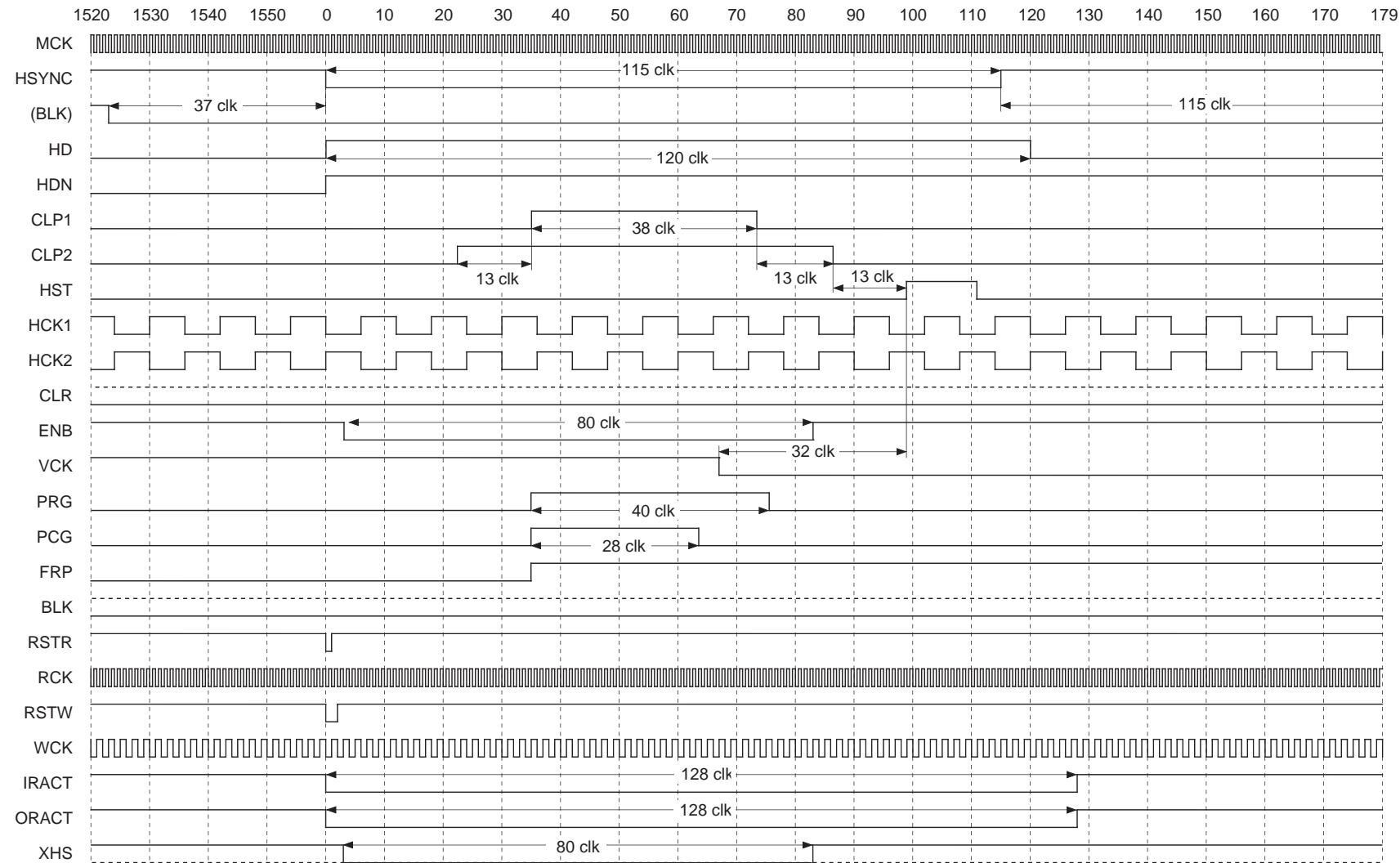
RGT : H   PLLP : HHLLLLHLHHL (LSB)   HP : HHHHHHLL (LSB)   HSTP : LLHH (LSB)   PCGP : LLHHL (LSB)   PRGP : LHLLH (LSB)
CLPP : LL (LSB)   HPOL : L   HDNPOL : H   CLPPOL : H   PCGPOL : H   PRGPOL : H   HR : H   HST : H   PCG : H   DSP : L

Loop Counter : 1560 clk
MCK f : 24.54MHz (40.75ns)

SONY

| | 1520 | 1530 | 1540 | 1550 | 0 | 10 | 20 | 30 | 40 | 50 | 60 | 70 | 80 | 90 | 100 | 110 | 120 | 130 | 140 | 150 | 160 | 170 | 179 |

MCK

HSYNC — 115 clk

(BLK) — 37 clk — 115 clk

HD — 120 clk

HDN

CLP1 — 38 clk

CLP2 — 13 clk — 13 clk — 13 clk

HST

HCK1

HCK2

CLR

ENB — 80 clk — 32 clk

VCK

PRG — 40 clk

PCG — 28 clk

FRP

BLK

RSTR

RCK

RSTW

WCK

IRACT — 128 clk

ORACT — 128 clk

XHS — 80 clk

Note) When RGT is Low, HCK1 and 2 are inversed.
       The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

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CXD2464R
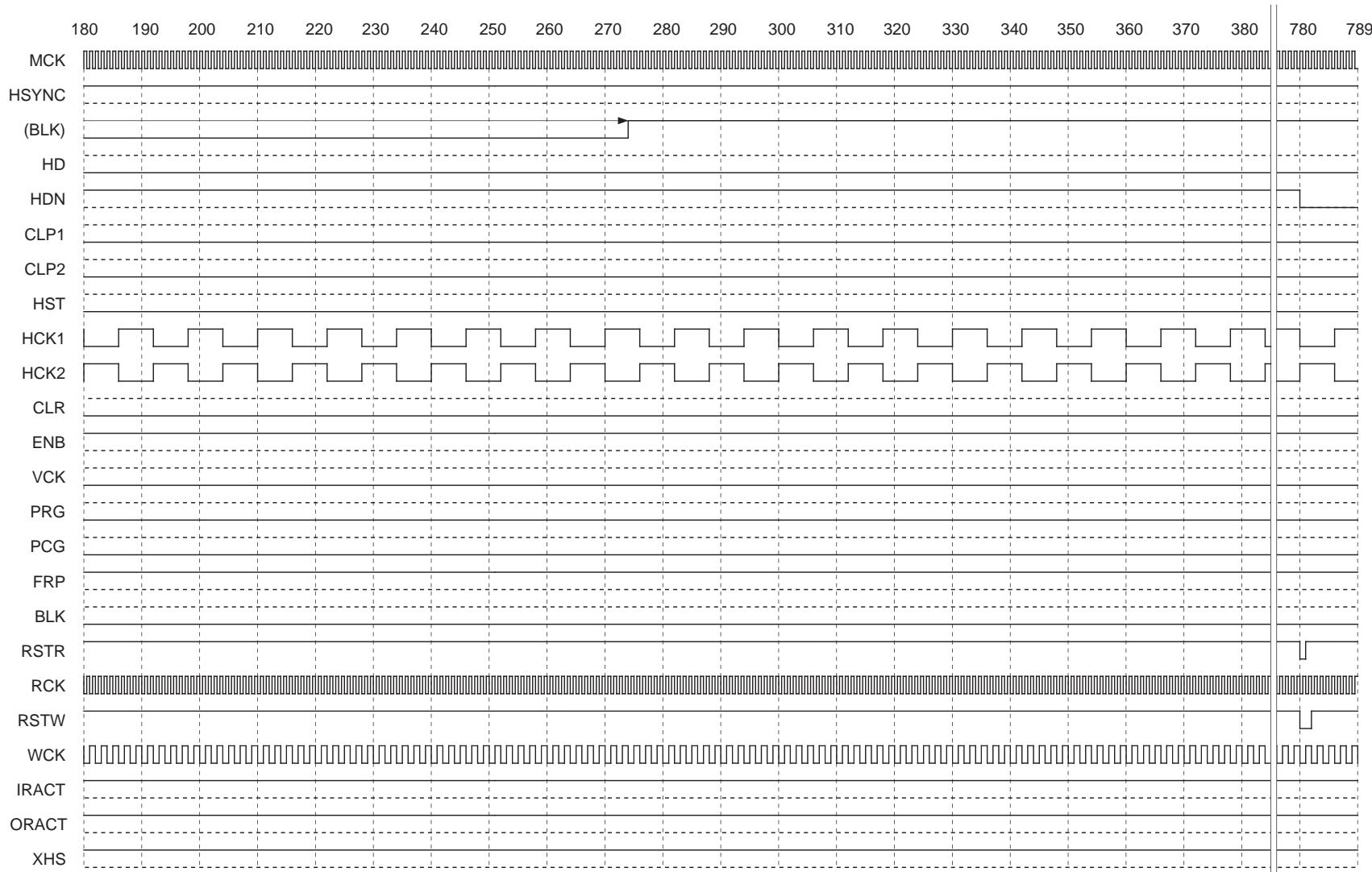
LCX026 NTSC_2 640 × 480

RGT : H PLLP : HHLLLLHLHHL (LSB) HP : HHHHHHLL (LSB) HSTP : LLLH (LSB) PCGP : LLHHL (LSB) PRGP : LHLLH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : L

Loop Counter : 1560 clk
MCK f : 24.54MHz (40.75ns)

180 190 200 210 220 230 240 250 260 270 280 290 300 310 320 330 340 350 360 370 380 780 789

MCK
HSYNC
(BLK)
HD
HDN
CLP1
CLP2
HST
HCK1
HCK2
CLR
ENB
VCK
PRG
PCG
FRP
BLK
RSTR
RCK
RSTW
WCK
IRACT
ORACT
XHS
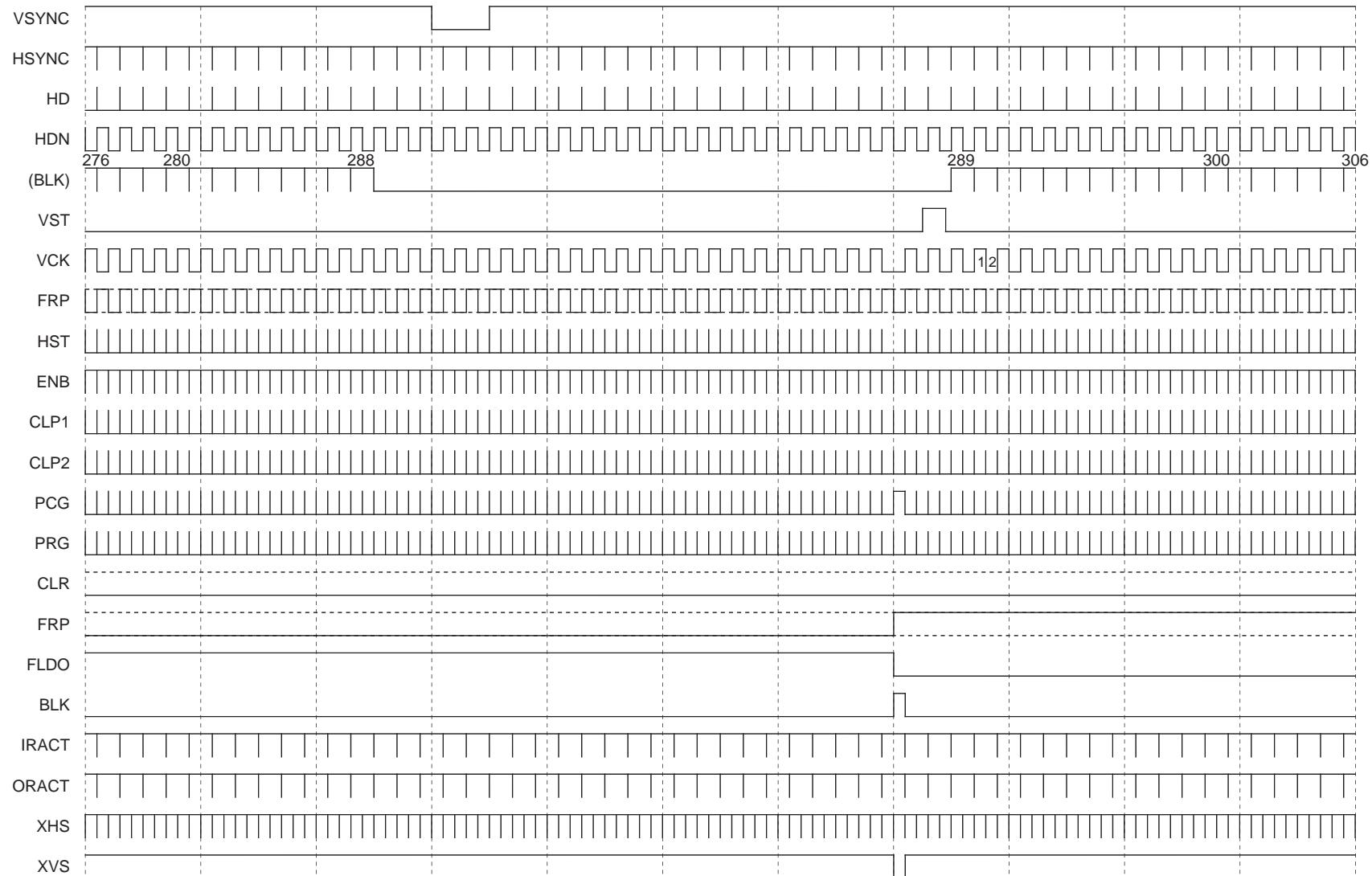
Note) When RGT is Low, HCK1 and 2 are inversed.
     The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX026   PAL (ODD)   762 × 572

MODE3/2/1 : L/H/L   MODE B/A : H/H   MODE021 : L   DWN : H   VP : LLLHLLHL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : L   PC98 : H
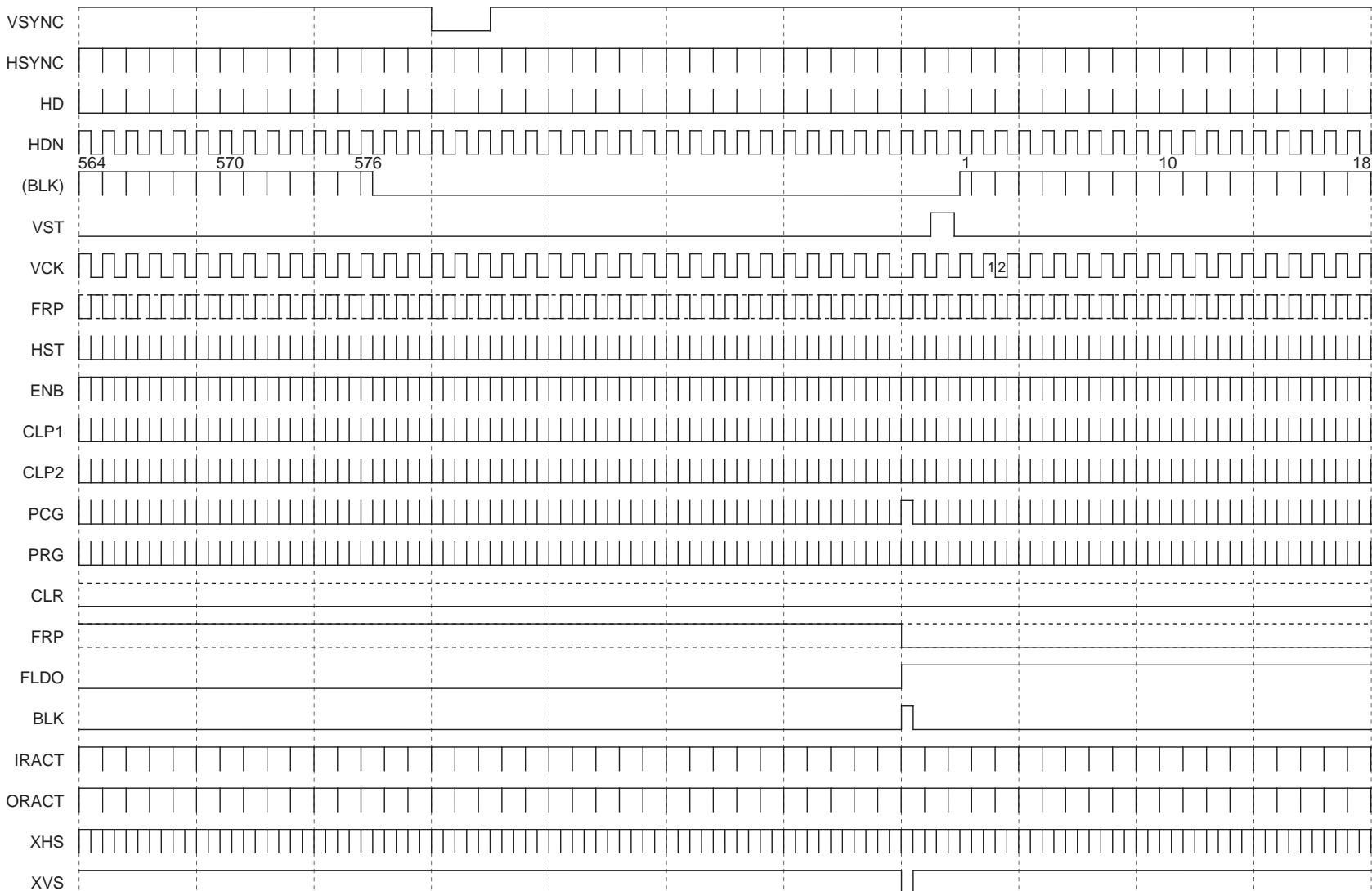
Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP polarity is not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX026   PAL (EVEN)   762 × 572

MODE3/2/1 : L/H/L   MODE B/A : H/H   MODE021 : L   DWN : H   VP : LLLHLLHL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : L   PC98 : H

VSYNC
HSYNC
HD
HDN
564   570   576   1   10   18
(BLK)
VST
VCK   1 2
FRP
HST
ENB
CLP1
CLP2
PCG
PRG
CLR
FRP
FLDO
BLK
IRACT
ORACT
XHS
XVS

Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP polarity is not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

SONY
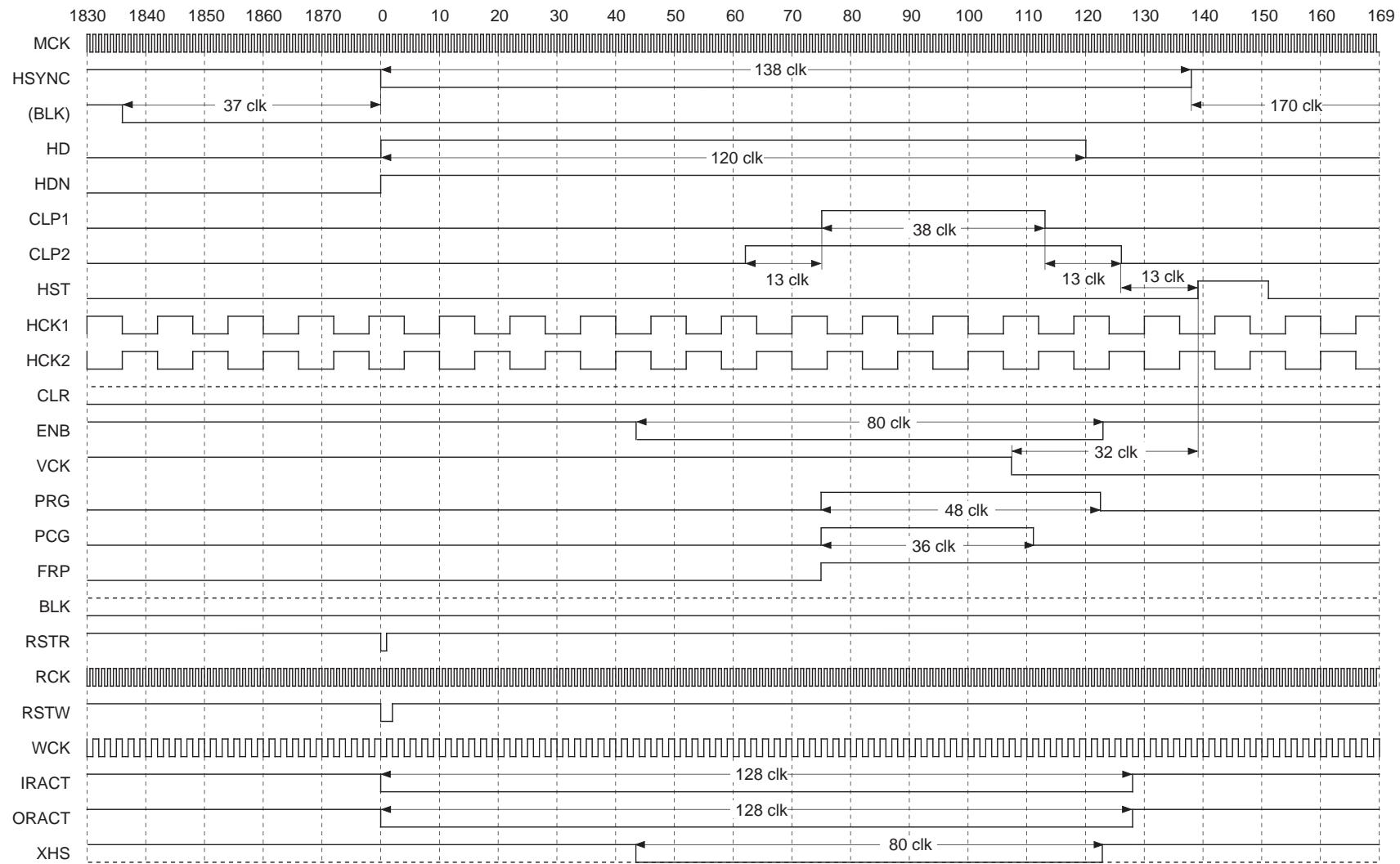
LCX026 PAL_1 762 × 572

RGT : H   PLLP : HHHLHLHLHHL (LSB)   HP : HHLHLHLL (LSB)   HSTP : LLHH (LSB)   PCGP : LHLLL (LSB)   PRGP : LHLHH (LSB)

CLPP : LL (LSB)   HPOL : L   HDNPOL : H   CLPPOL : H   PCGPOL : H   PRGPOL : H   HR : H   HST : H   PCG : H   DSP : L

Loop Counter : 1880 clk
MCK f : 29.38MHz (34.04ns)
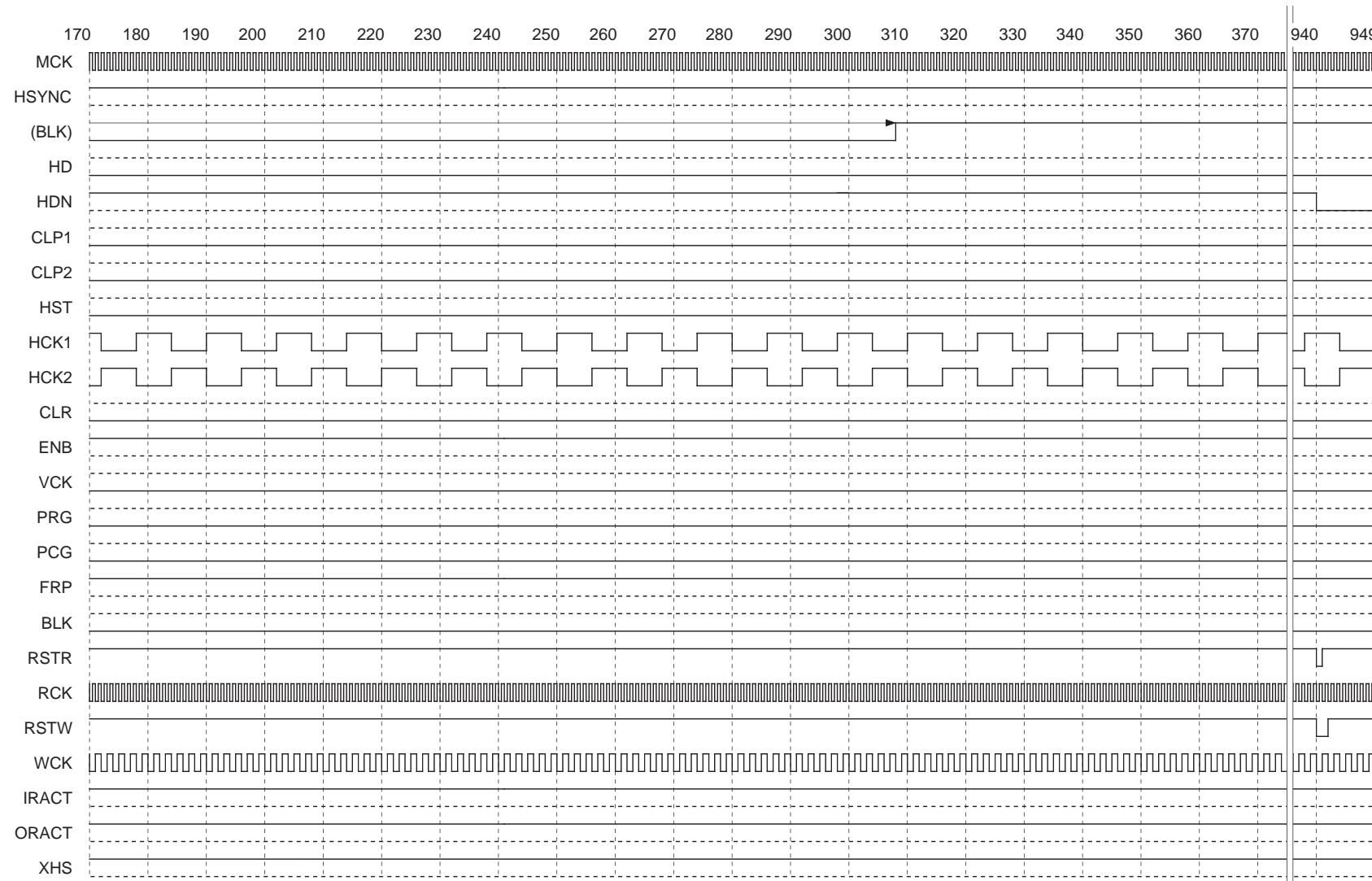
Note) When RGT is Low, HCK1 and 2 are inversed.
      The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX026 PAL_2 762 × 572

RGT : H PLLP : HHHLHLHLHHL (LSB) HP : HHLHLHLL (LSB) HSTP : LLLH (LSB) PCGP : LHLLL (LSB) PRGP : LHLHH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : L

Loop Counter : 1880 clk
MCK f : 29.38MHz (34.04ns)

170 180 190 200 210 220 230 240 250 260 270 280 290 300 310 320 330 340 350 360 370 940 949

MCK
HSYNC
(BLK)
HD
HDN
CLP1
CLP2
HST
HCK1
HCK2
CLR
ENB
VCK
PRG
PCG
FRP
BLK
RSTR
RCK
RSTW
WCK
IRACT
ORACT
XHS

Note) When RGT is Low, HCK1 and 2 are inversed.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

SONY

CXD2464R

LCX026   PC98   640 × 400

MODE3/2/1 : L/L/H   MODE B/A : H/H   MODE021 : L   DWN : H   VP : LLLHLHHL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : H
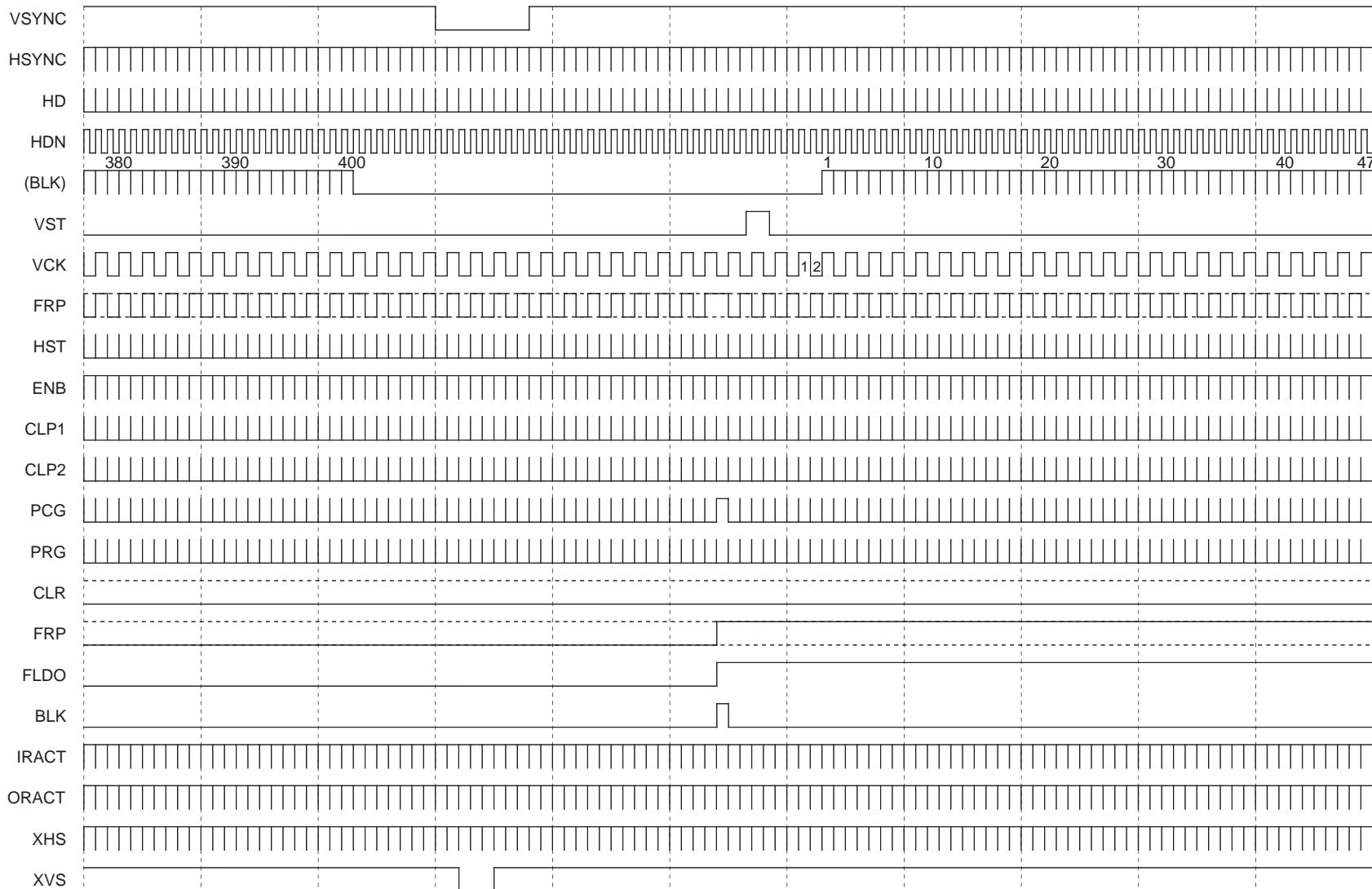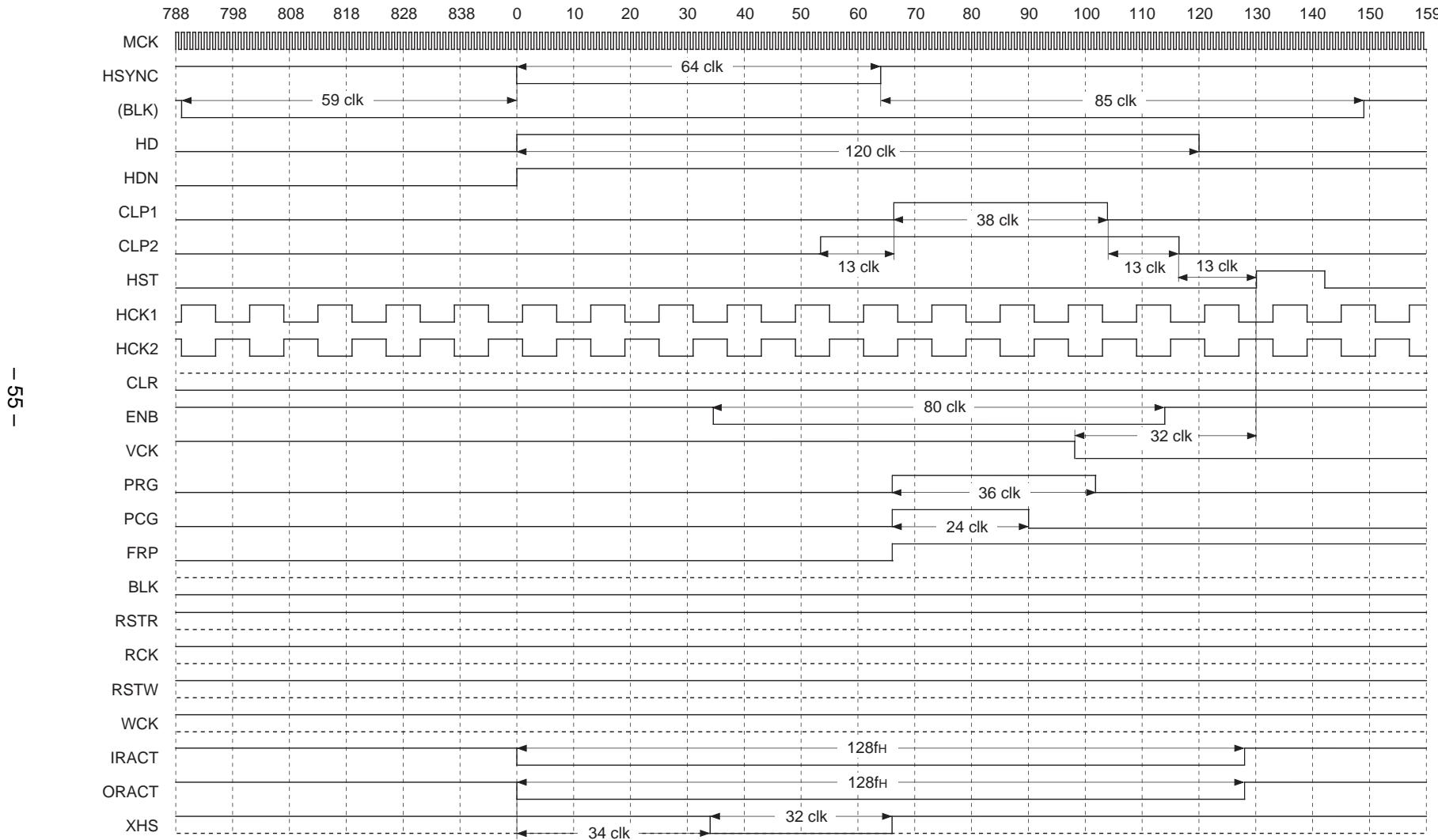
Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP and FLDO polarity are not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX026 PC98 640 × 400

RGT : H PLLP : LHHLHLLHHHL (LSB) HP : HHLHHHLH (LSB) HSTP : LLHH (LSB) PCGP : LLHLH (LSB) PRGP : LHLLH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : H

Loop Counter : 848 clk
MCK f : 21.05MHz (47.50ns)

Note) When RGT is Low, HCK1 and 2 are inversed.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

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CXD2464R
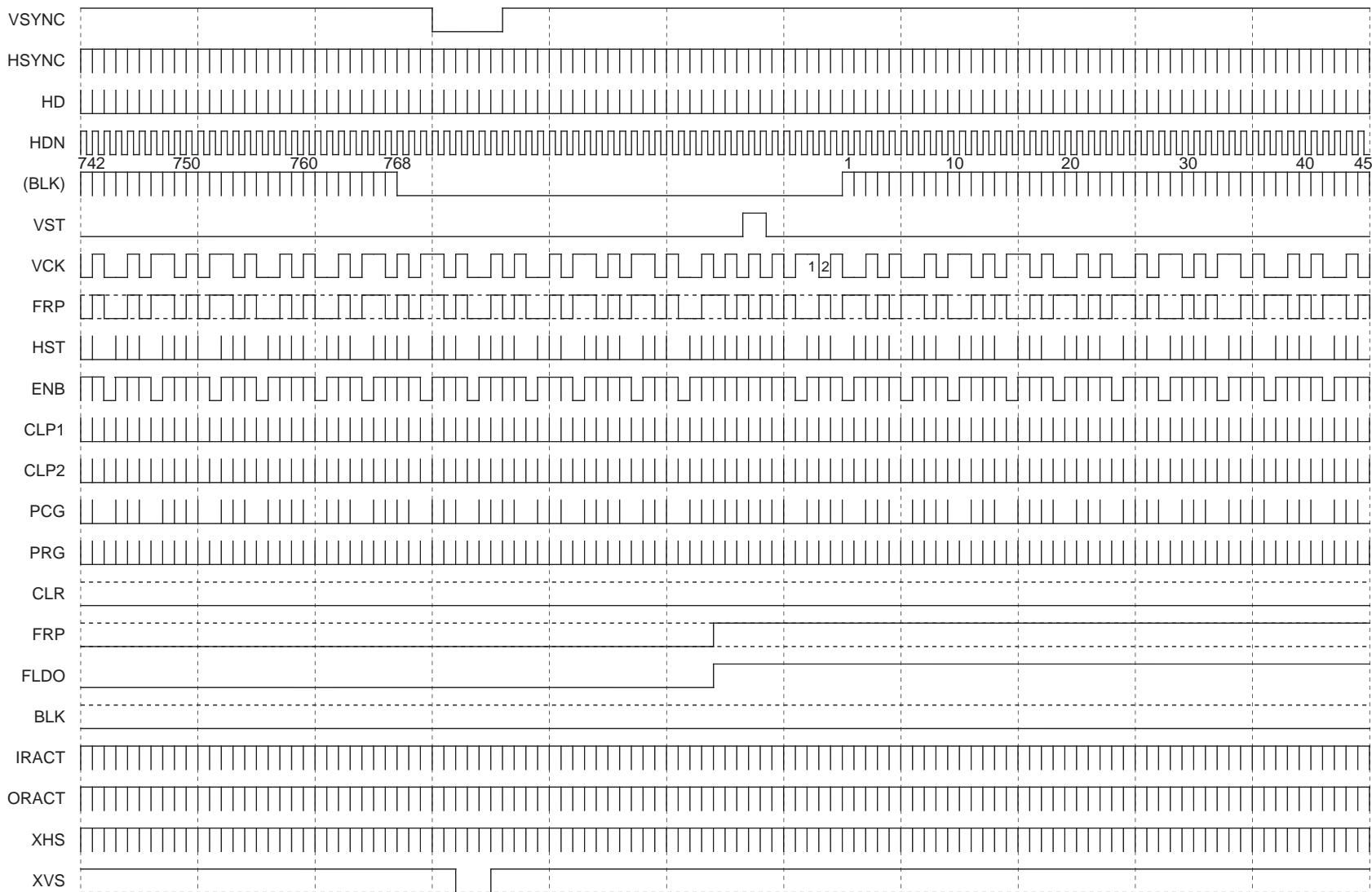
LCX026 XGA 1024 × 768

MODE3/2/1 : L/L/L   MODE B/A : H/H   MODE021 : L   DWN : H   VP : LLLHLHHL (LSB)   MBK2/1/0/B/A : H/L/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : H
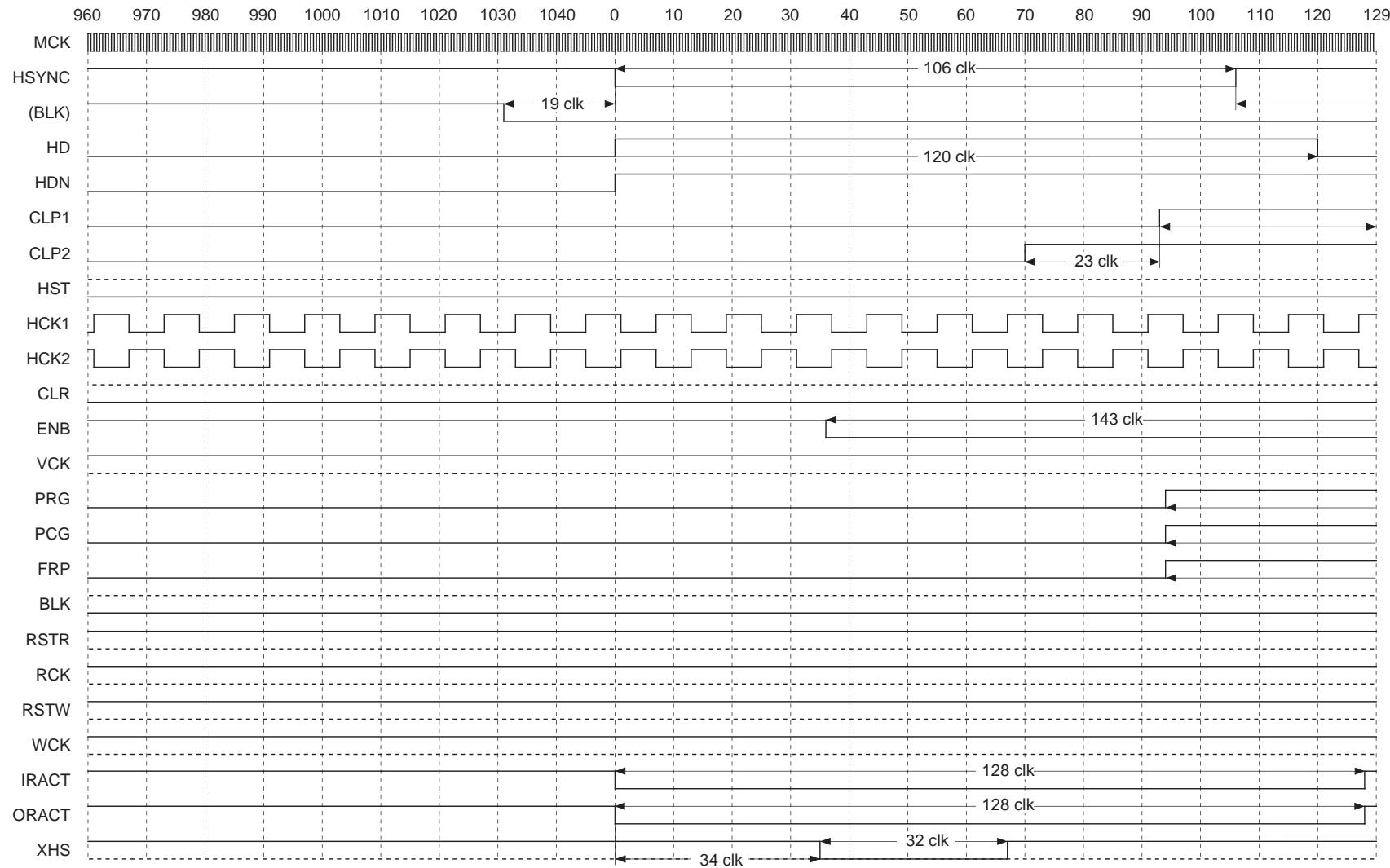
|	
VSYNC	
HSYNC	
HD	
HDN	
(BLK)	742 750 760 768 ... 1 10 20 30 40 45
VST	
VCK	1 2
FRP	
HST	
ENB	
CLP1	
CLP2	
PCG	
PRG	
CLR	
FRP	
FLDO	
BLK	
IRACT	
ORACT	
XHS	
XVS	

Note) When DWN is Low, VST is inversed.
      The 1H and 1V cycle FRP and FLDO polarity are not specified.
      The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX026 XGA_1 1024 × 768

RGT : H PLLP : HLLLLLHHLLL (LSB) HP : HHLHHLHH (LSB) HSTP : HLLH (LSB) PCGP : LHHHH (LSB) PRGP : HLHLH (LSB)

CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : H

Loop Counter : 1050 clk

MCK f : 52.81MHz (18.94ns)

MCK

HSYNC

(BLK) 19 clk

HD 120 clk

HDN

CLP1

CLP2 23 clk

HST

HCK1

HCK2

CLR

ENB 143 clk

VCK

PRG

PCG

FRP

BLK

RSTR

RCK

RSTW

WCK

IRACT 128 clk

ORACT 128 clk

XHS 32 clk 34 clk

HSYNC 106 clk
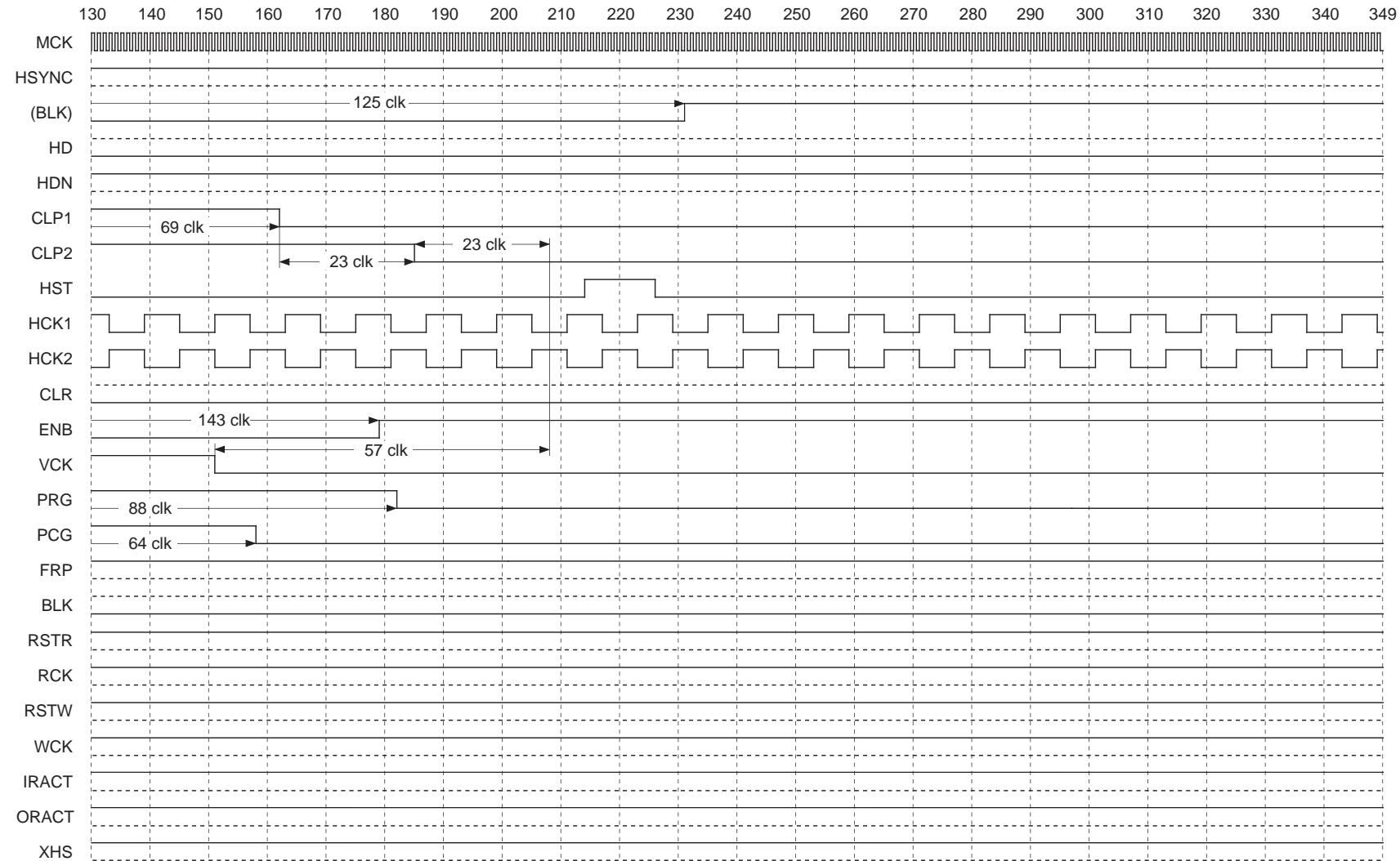
Note) When RGT is Low, HCK1 and 2 are inversed.

　　　The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX026 XGA_2 1024 × 768

RGT : H PLLP : HLLLLLHHLLL (LSB) HP : HHLHHLHH (LSB) HSTP : HLLH (LSB) PCGP : LHHHH (LSB) PRGP : HLHLH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : H

Loop Counter : 1050 clk
MCK f : 52.81MHz (18.94ns)

Note) When RGT is Low, HCK1 and 2 are inversed.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 Macintosh16_1 832 × 624

MODE3/2/1 : L/L/L   MODE B/A : L/H   MODE021 : L   DWN : H   VP : LLHLLLHH (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : H
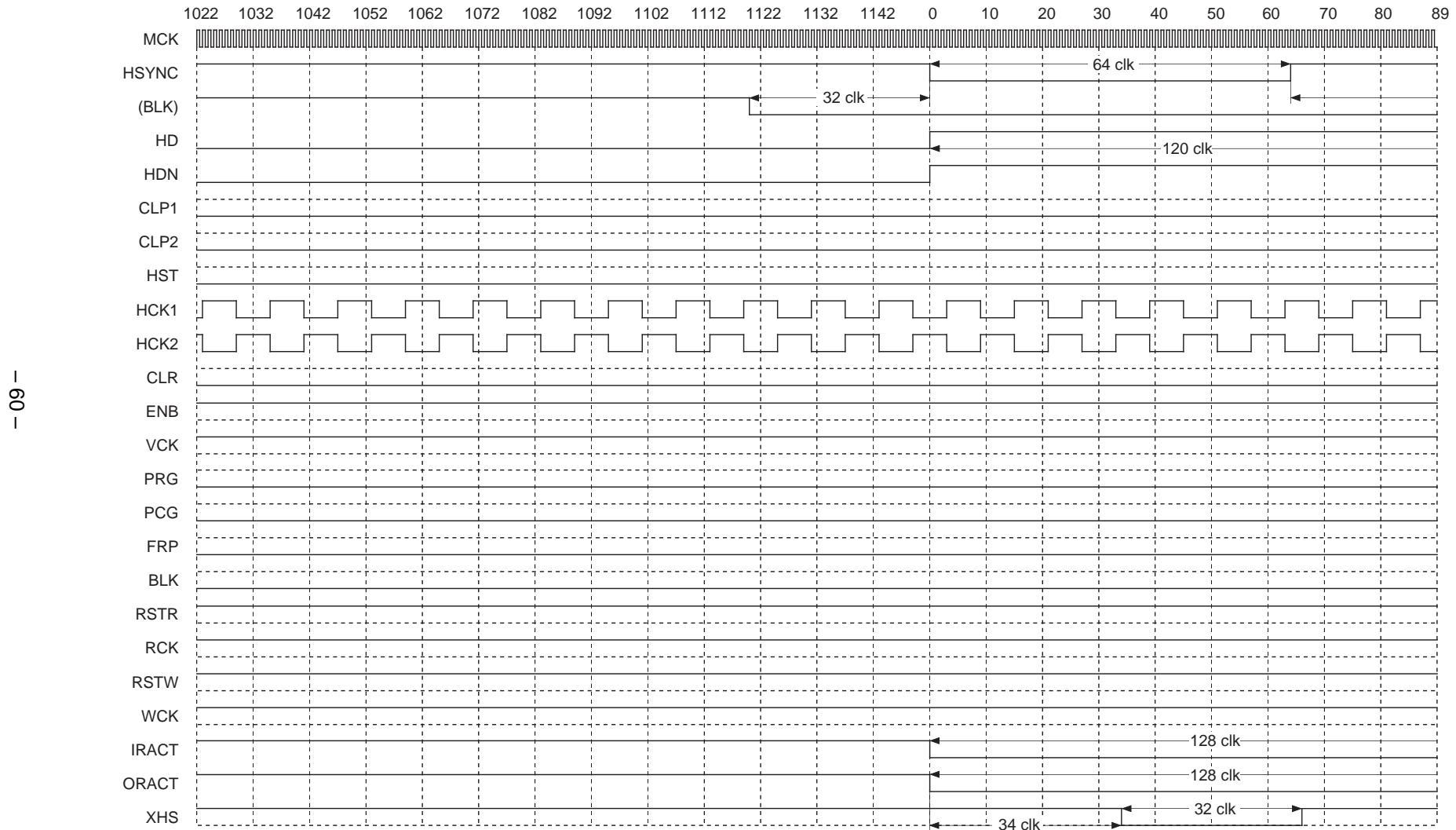

Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP and FLDO polarity are not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 Macintosh16_1 832 × 624

RGT : H PLLP : HLLLHHHHHHL (LSB) HP : LHHLLHHH (LSB) HSTP : LLLH (LSB) PCGP : HLLLL (LSB) PRGP : HLHHH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : H

Loop Counter : 1152 clk
MCK f : 57.28MHz (17.46ns)

1022 1032 1042 1052 1062 1072 1082 1092 1102 1112 1122 1132 1142 0 10 20 30 40 50 60 70 80 89

MCK

HSYNC — 64 clk

(BLK) — 32 clk

HD — 120 clk

HDN

CLP1

CLP2

HST

HCK1

HCK2

CLR

ENB

VCK

PRG

PCG

FRP

BLK

RSTR

RCK

RSTW

WCK

IRACT — 128 clk

ORACT — 128 clk

XHS — 32 clk — 34 clk

Note) When RGT is Low, HCK1 and 2 are inversed.
    The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

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CXD2464R
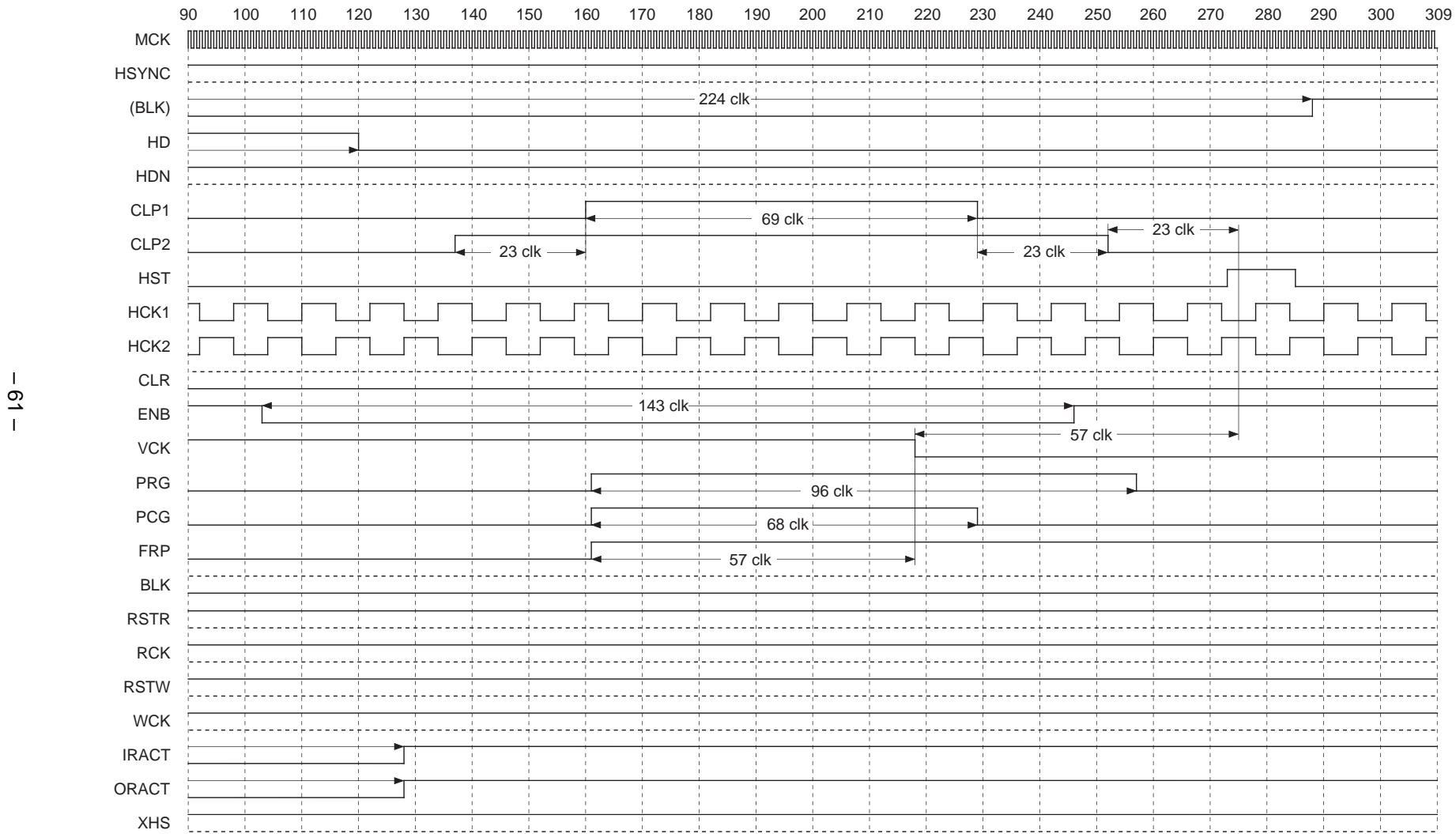
LCX016 Macintosh16_2 832 × 624

RGT : H PLLP : HLLLHHHHHHL (LSB) HP : LHHLLHHH (LSB) HSTP : LLLH (LSB) PCGP : HLLLL (LSB) PRGP : HLHHH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : H
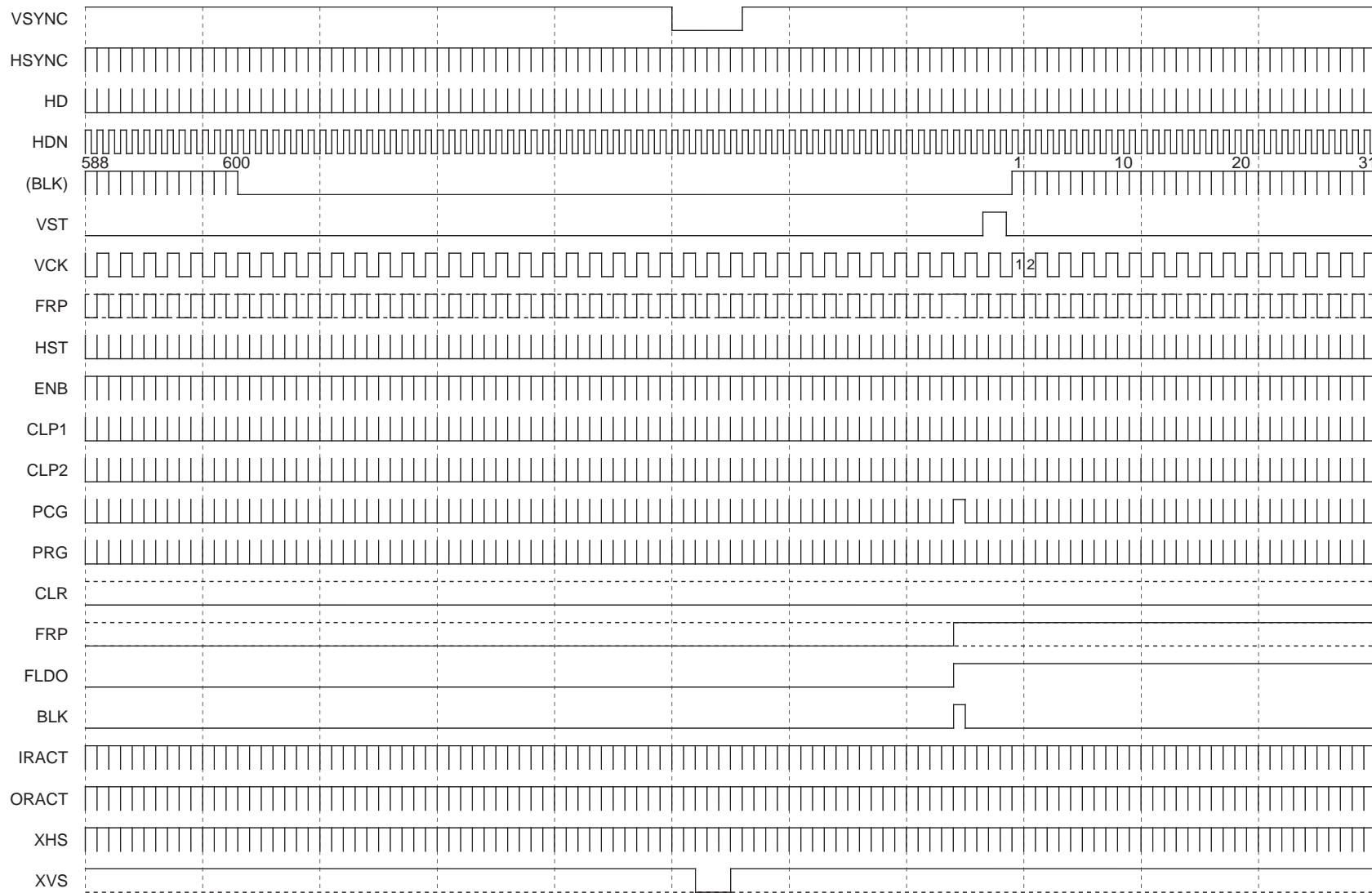
Loop Counter : 1152 clk
MCK f : 57.28MHz (17.46ns)

Note) When RGT is Low, HCK1 and 2 are inversed.
       The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 SVGA 800 × 600

MODE3/2/1 : H/L/L   MODE B/A : L/H   MODE021 : L   DWN : H   VP : LLHLLHHL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : H

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Signal timing chart with the following rows:

VSYNC, HSYNC, HD, HDN, (BLK), VST, VCK, FRP, HST, ENB, CLP1, CLP2, PCG, PRG, CLR, FRP, FLDO, BLK, IRACT, ORACT, XHS, XVS

HDN row markers: 588, 600, ... 1, 10, 20, 31

VCK markers: 1 2
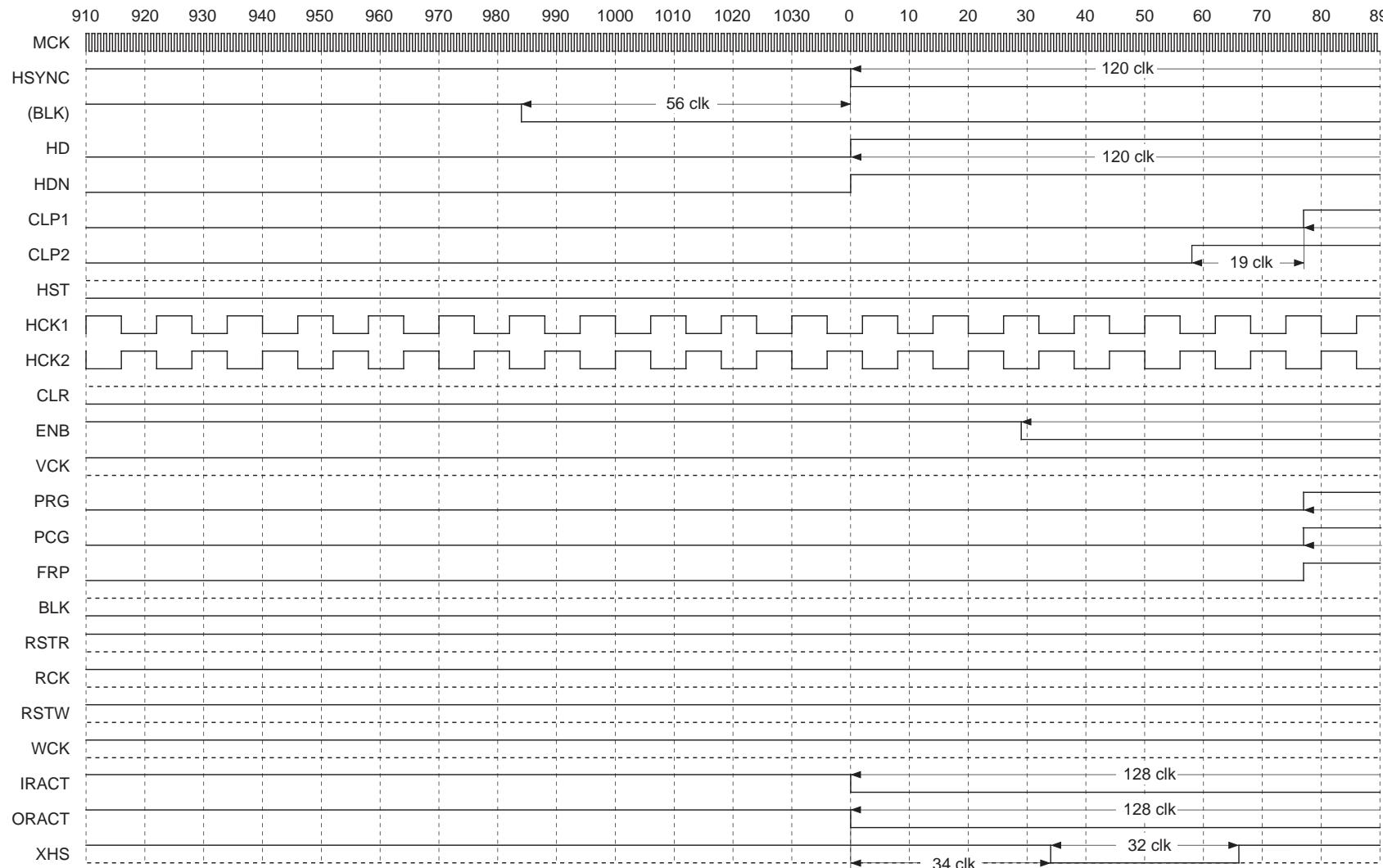
Note) When DWN is Low, VST is inversed.
       The 1H and 1V cycle FRP and FLDO polarity are not specified.
       The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 SVGA_1 800 × 600

RGT : H PLLP : HLLLHHHHHHL (LSB) HP : HHHLLLHL (LSB) HSTP : LLLH (LSB) PCGP : LHHHL (LSB) PRGP : HLHLL (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : H

Loop Counter : 1040 clk
MCK f : 50.00MHz (20.00ns)
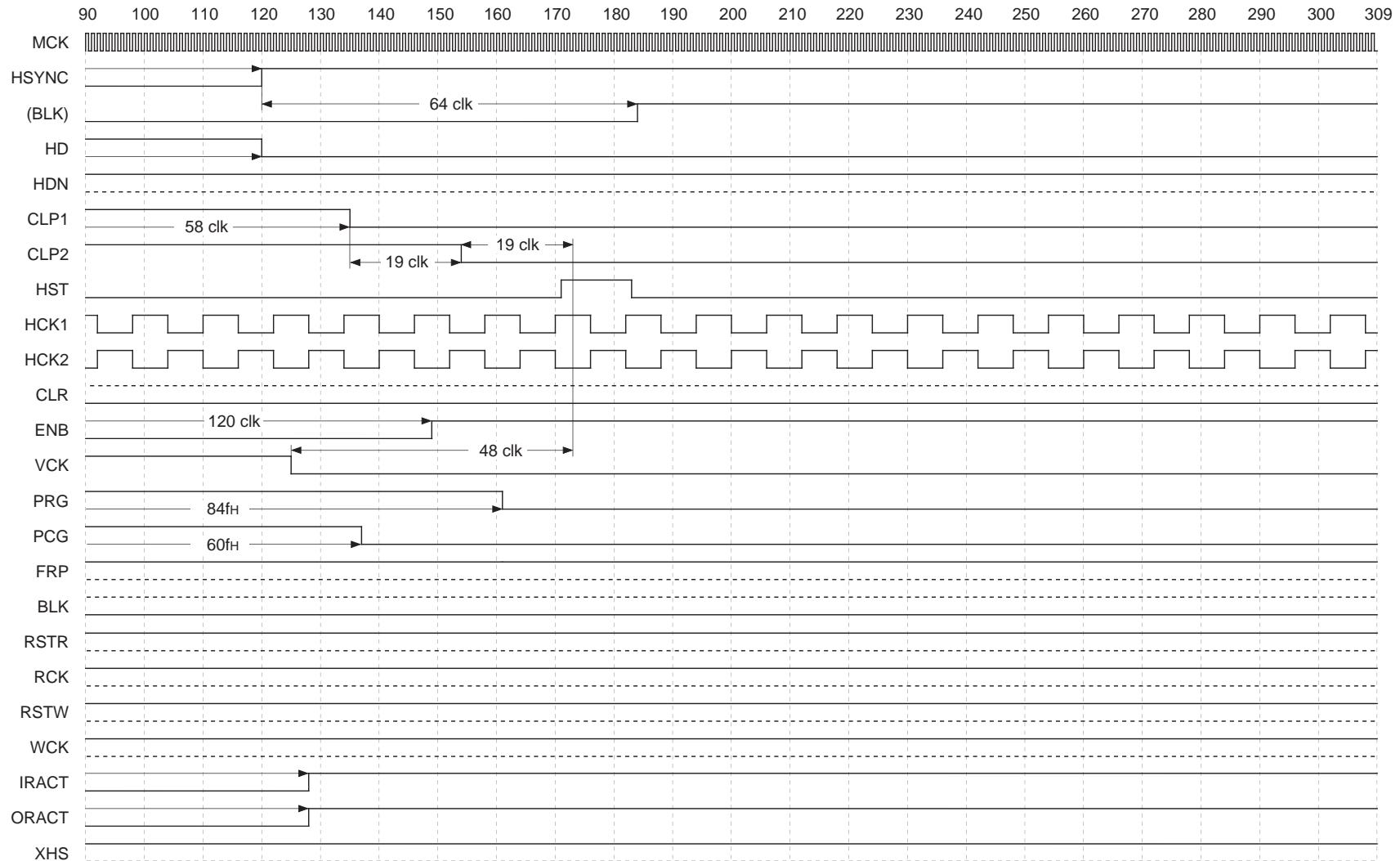
Note) When RGT is Low, HCK1 and 2 are inversed.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016　SVGA_2　800 × 600

RGT : H   PLLP : HLLLHHHHHHL (LSB)   HP : HHHLLLHL (LSB)   HSTP : LLLH (LSB)   PCGP : LHHHL (LSB)   PRGP : HLHLL (LSB)
CLPP : LL (LSB)   HPOL : L   HDNPOL : H   CLPPOL : H   PCGPOL : H   PRGPOL : H   HR : H   HST : H   PCG : H   DSP : H

Loop Counter : 1040 clk
MCK f : 50.00MHz (20.00ns)
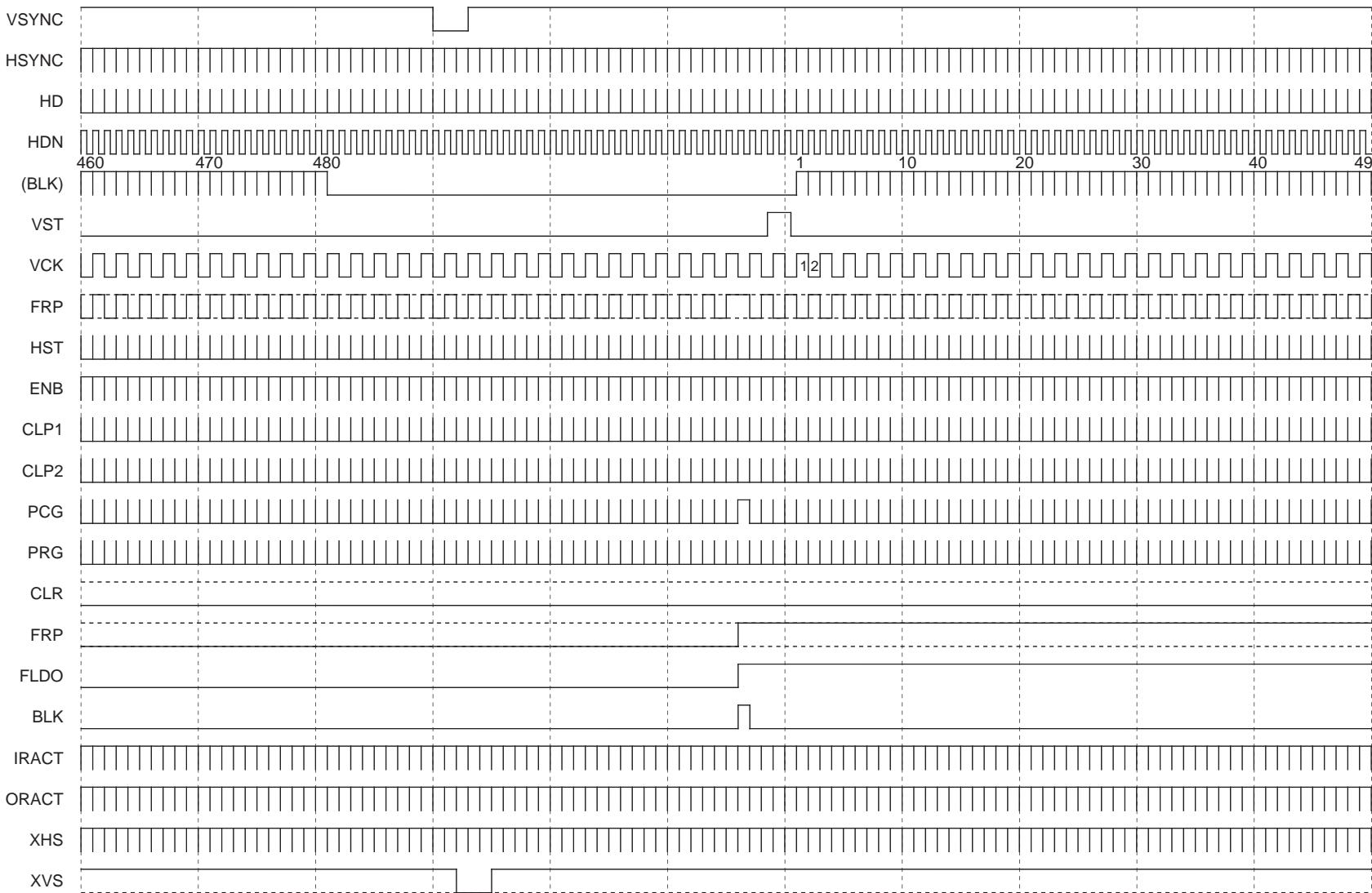
Note) When RGT is Low, HCK1 and 2 are inversed.
　　　 The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016   VGA   640 × 480

MODE3/2/1 : H/H/L   MODE B/A : L/H   MODE021 : L   DWN : H   VP : LLLHHLLL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : H


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CXD2464R

Note) When DWN is Low, VST is inversed.
       The 1H and 1V cycle FRP and FLDO polarity are not specified.
       The fifith row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016   VGA   640 × 480

RGT : H   PLLP : LHHLLHHHHHL (LSB)   HP : HHLLLHLL (LSB)   HSTP : LLLH (LSB)   PCGP : LHLLH (LSB)   PRGP : LHHLH (LSB)
CLPP : LL (LSB)   HPOL : L   HDNPOL : H   CLPPOL : H   PCGPOL : H   PRGPOL : H   HR : H   HST : H   PCG : H   DSP : H

Loop Counter : 832 clk
MCK f : 31.50MHz (31.75ns)

Note) When RGT is Low, HCK1 and 2 are inversed.
      The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

– 66 –
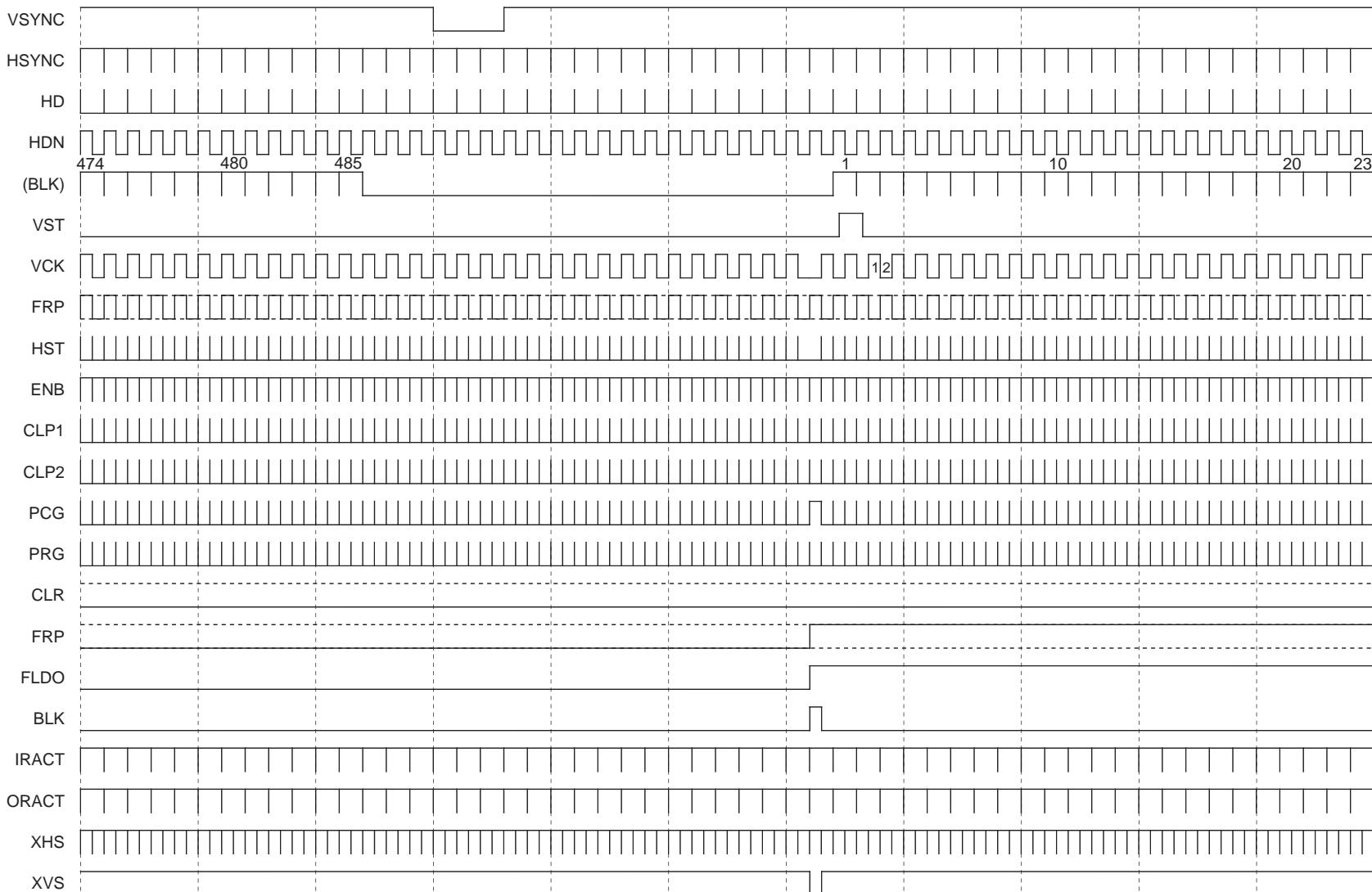
LCX016 NTSC (ODD) 640 × 480

MODE3/2/1 : H/H/L MODE B/A : L/H MODE021 : L DWN : H VP : LLLLHHHL (LSB) MBK2/1/0/B/A : H/H/H/L/L FRP1/0 : H/H VPOL : L VGAV : L PC98 : H
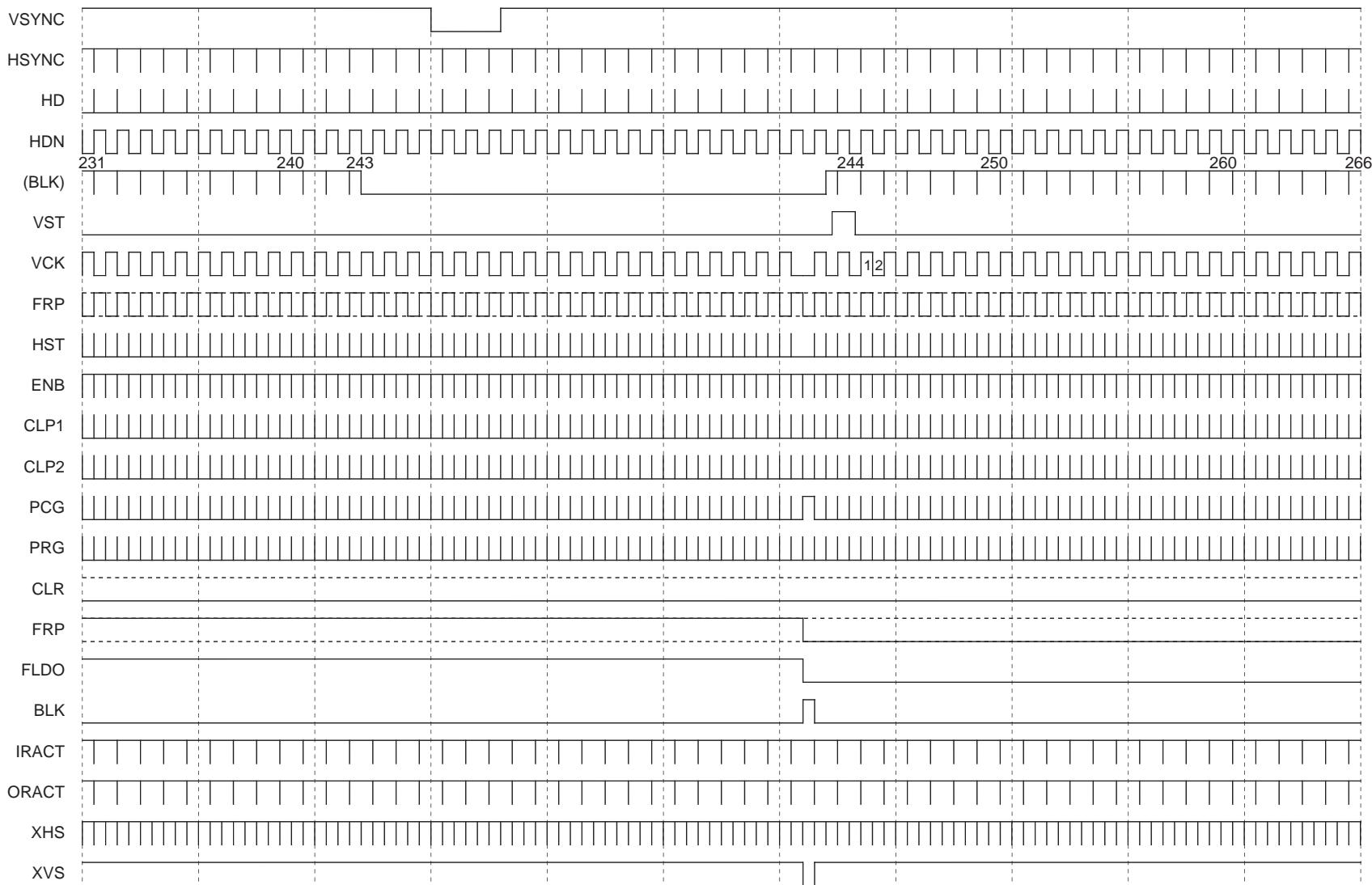
Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP polarity is not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 NTSC (EVEN) 640 × 480

MODE3/2/1 : H/H/L   MODE B/A : L/H   MODE021 : L   DWN : H   VP : LLLLHHHL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : L   PC98 : H
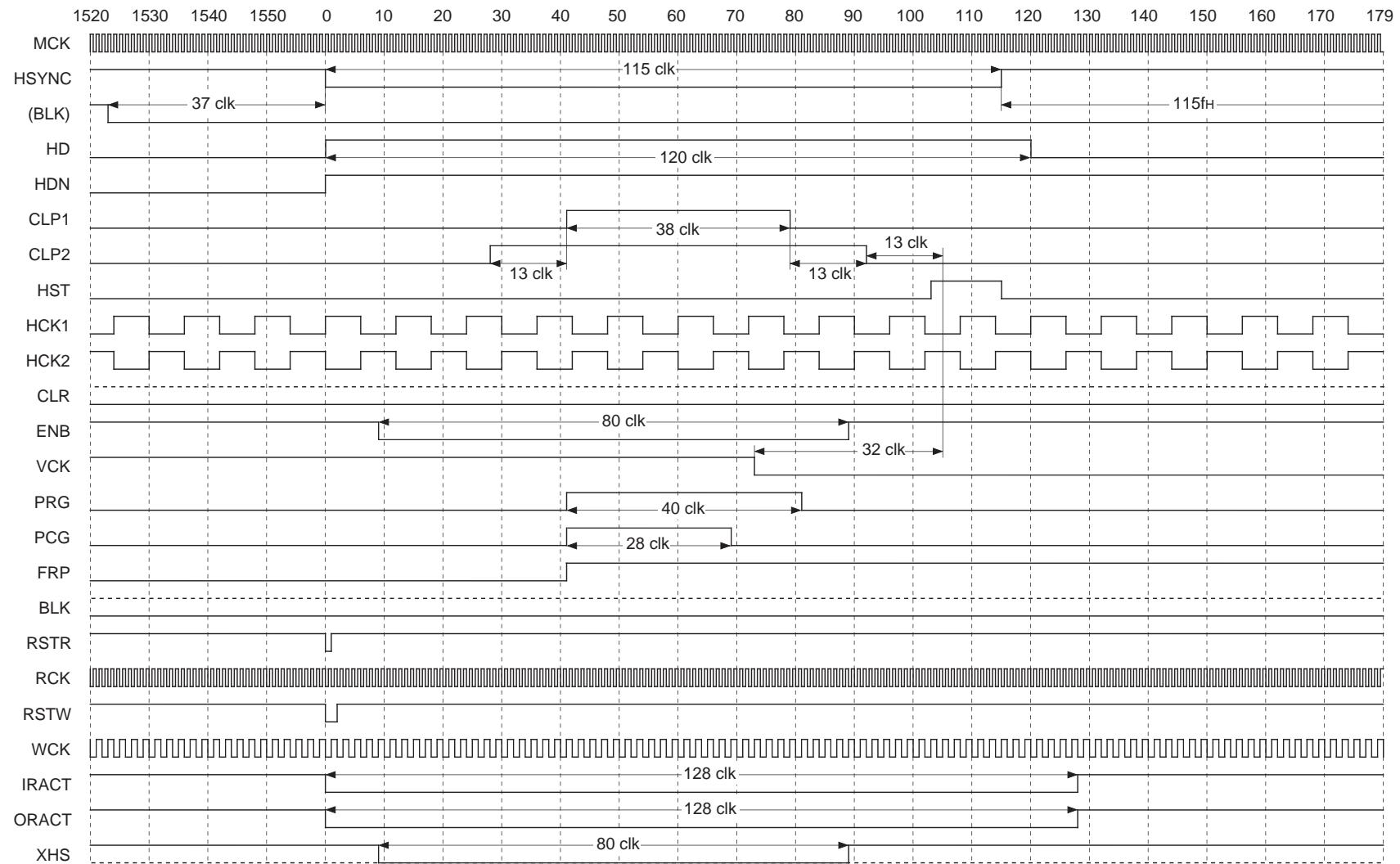
Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP polarity is not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 NTSC_1 640 × 480

RGT : H   PLLP : HHLLLLHLHHL (LSB)   HP : HHHHLHHL (LSB)   HSTP : LLLH (LSB)   PCGP : LLHHL (LSB)   PRGP : LHLLH (LSB)

CLPP : LL (LSB)   HPOL : L   HDNPOL : H   CLPPOL : H   PCGPOL : H   PRGPOL : H   HR : H   HST : H   PCG : H   DSP : L

Loop Counter : 1560 clk
MCK f : 24.54MHz (40.75ns)

SONY

1520 1530 1540 1550 0 10 20 30 40 50 60 70 80 90 100 110 120 130 140 150 160 170 179

MCK

HSYNC — 115 clk

(BLK) — 37 clk — 115fн

HD — 120 clk

HDN

CLP1 — 38 clk

CLP2 — 13 clk — 13 clk — 13 clk

HST

HCK1

HCK2

CLR

ENB — 80 clk

VCK — 32 clk

PRG — 40 clk

PCG — 28 clk

FRP

BLK

RSTR

RCK

RSTW

WCK

IRACT — 128 clk

ORACT — 128 clk

XHS — 80 clk

Note) When RGT is Low, HCK1 and 2 are inversed.
    The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

CXD2464R
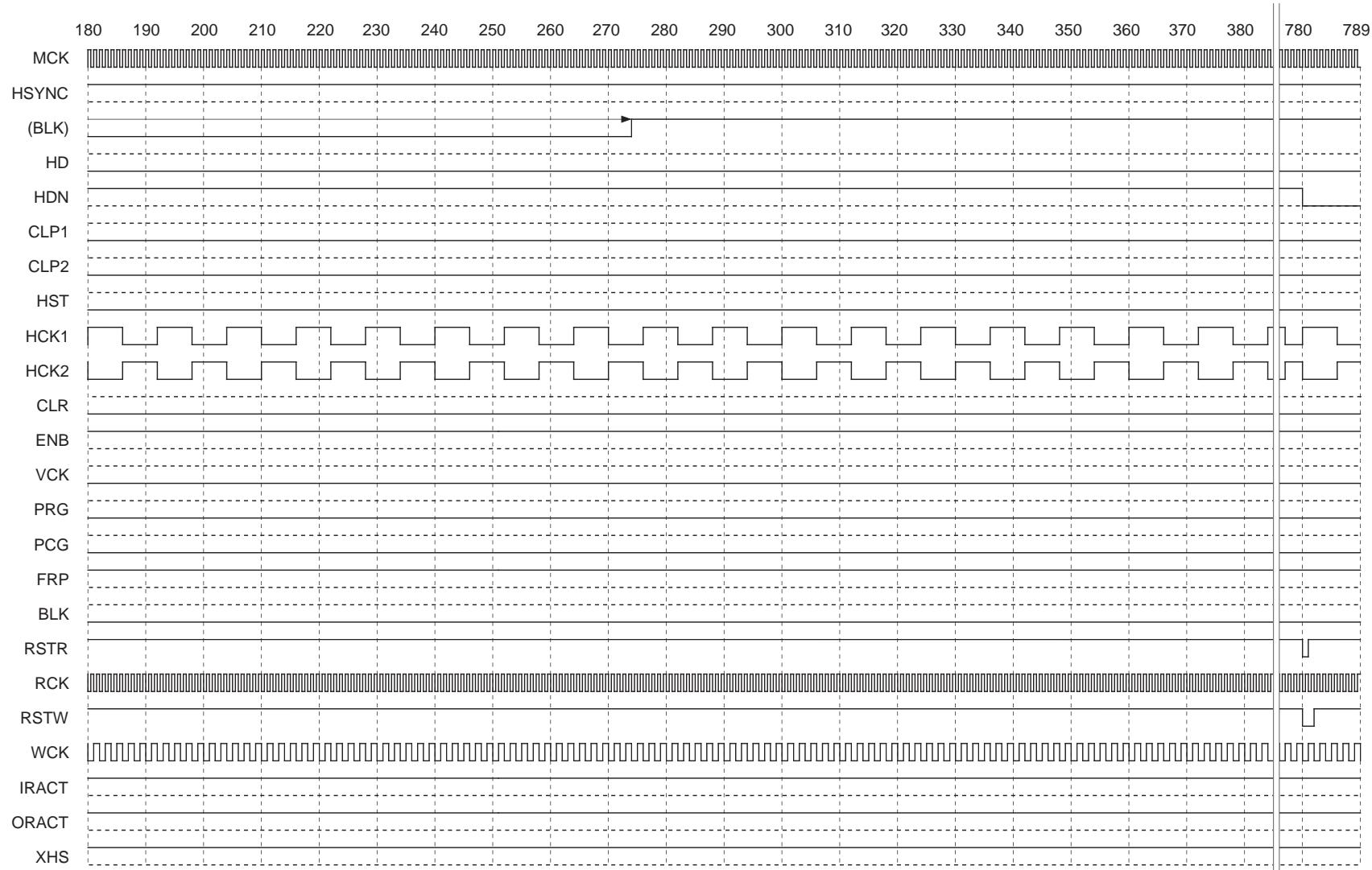
LCX016 NTSC_2 640 × 480

RGT : H PLLP : HHLLLLHLHHL (LSB) HP : HHHHLHHL (LSB) HSTP : LLLH (LSB) PCGP : LLHHL (LSB) PRGP : LHLLH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : L

Loop Counter : 1560 clk
MCK f : 24.54MHz (40.75ns)

Note) When RGT is Low, HCK1 and 2 are inversed.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

SONY

CXD2464R

LCX016 PAL (ODD) 762 × 572

MODE3/2/1 : L/H/L MODE B/A : L/H MODE021 : L DWN : H VP : LLLHLLHH (LSB) MBK2/1/0/B/A : H/H/H/L/L FRP1/0 : H/H VPOL : L VGAV : L PC98 : H
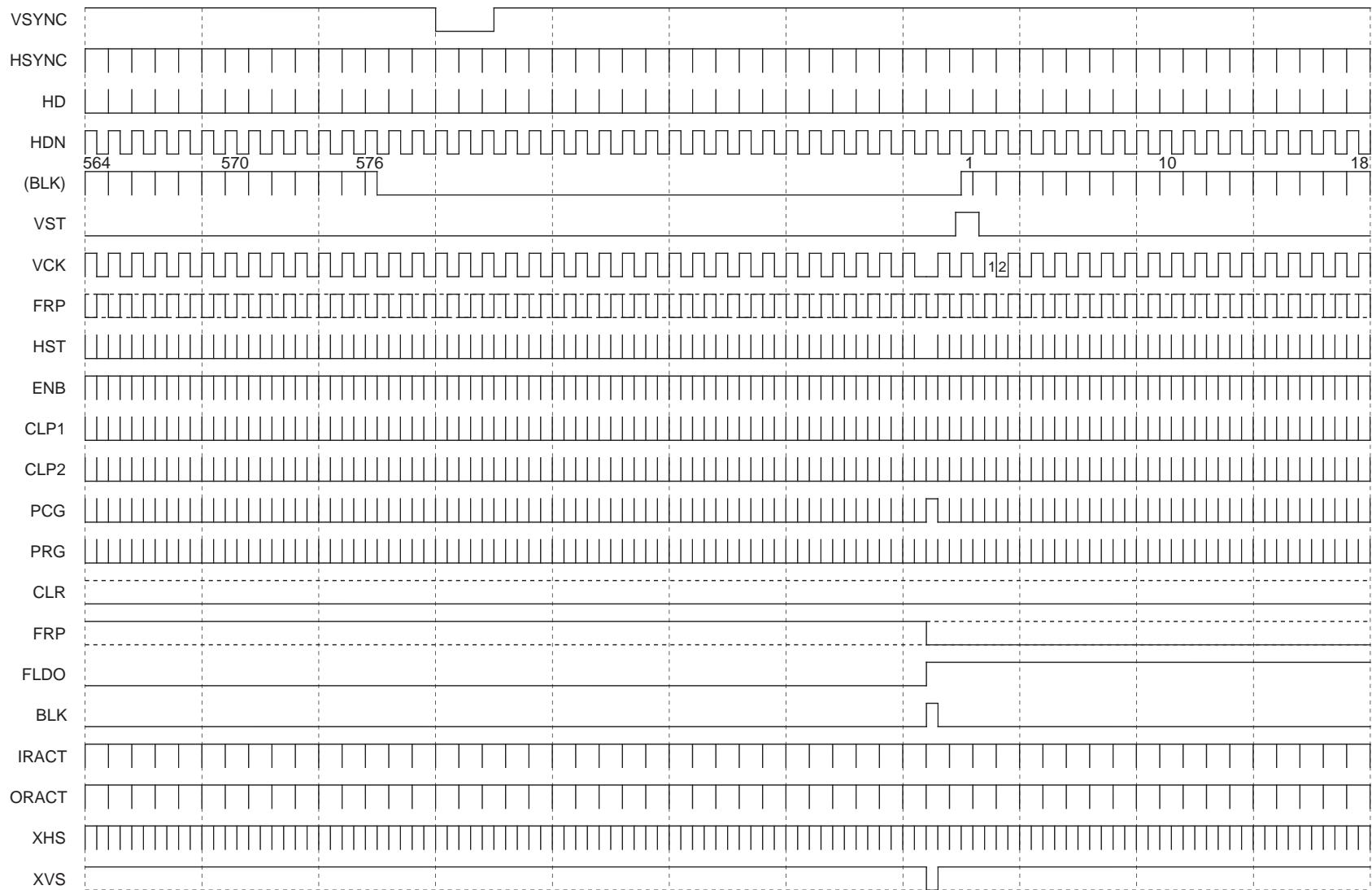

Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP polarity is not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016   PAL (EVEN)   762 × 572

MODE3/2/1 : L/H/L   MODE B/A : L/H   MODE021 : L   DWN : H   VP : LLLHLLHH (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : L   PC98 : H
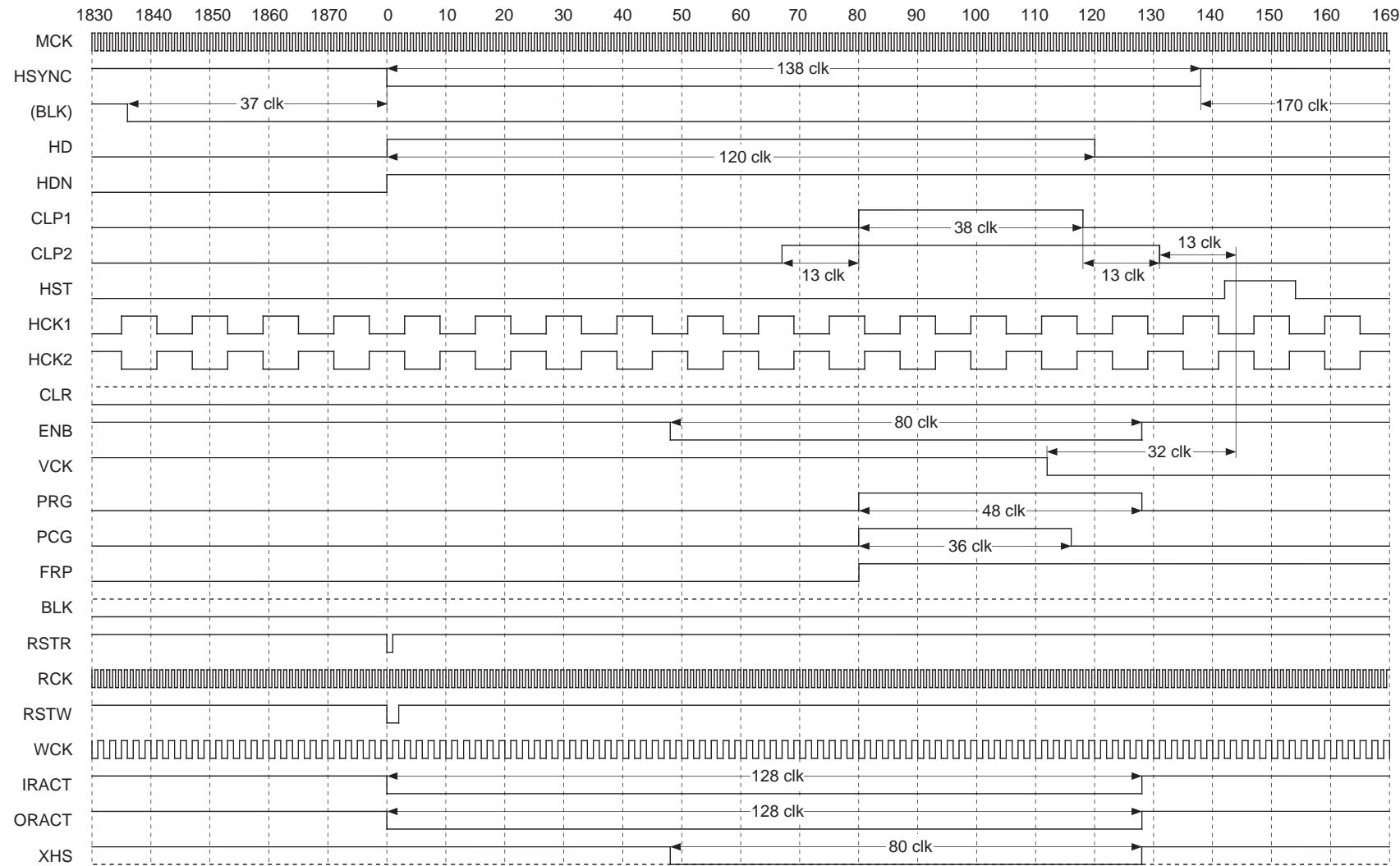
Note) When DWN is Low, VST is inversed.
　　　The 1H and 1V cycle FRP polarity is not specified.
　　　The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 PAL_1 762 × 572

RGT : H PLLP : HHHLHLHLHHL (LSB) HP : HHLLHHHH (LSB) HSTP : LLLH (LSB) PCGP : LHLLL (LSB) PRGP : LHLHH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : L

Loop Counter : 1880 clk
MCK f : 29.38MHz (34.04ns)

Note) When RGT is Low, HCK1 and 2 are inversed.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

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CXD2464R
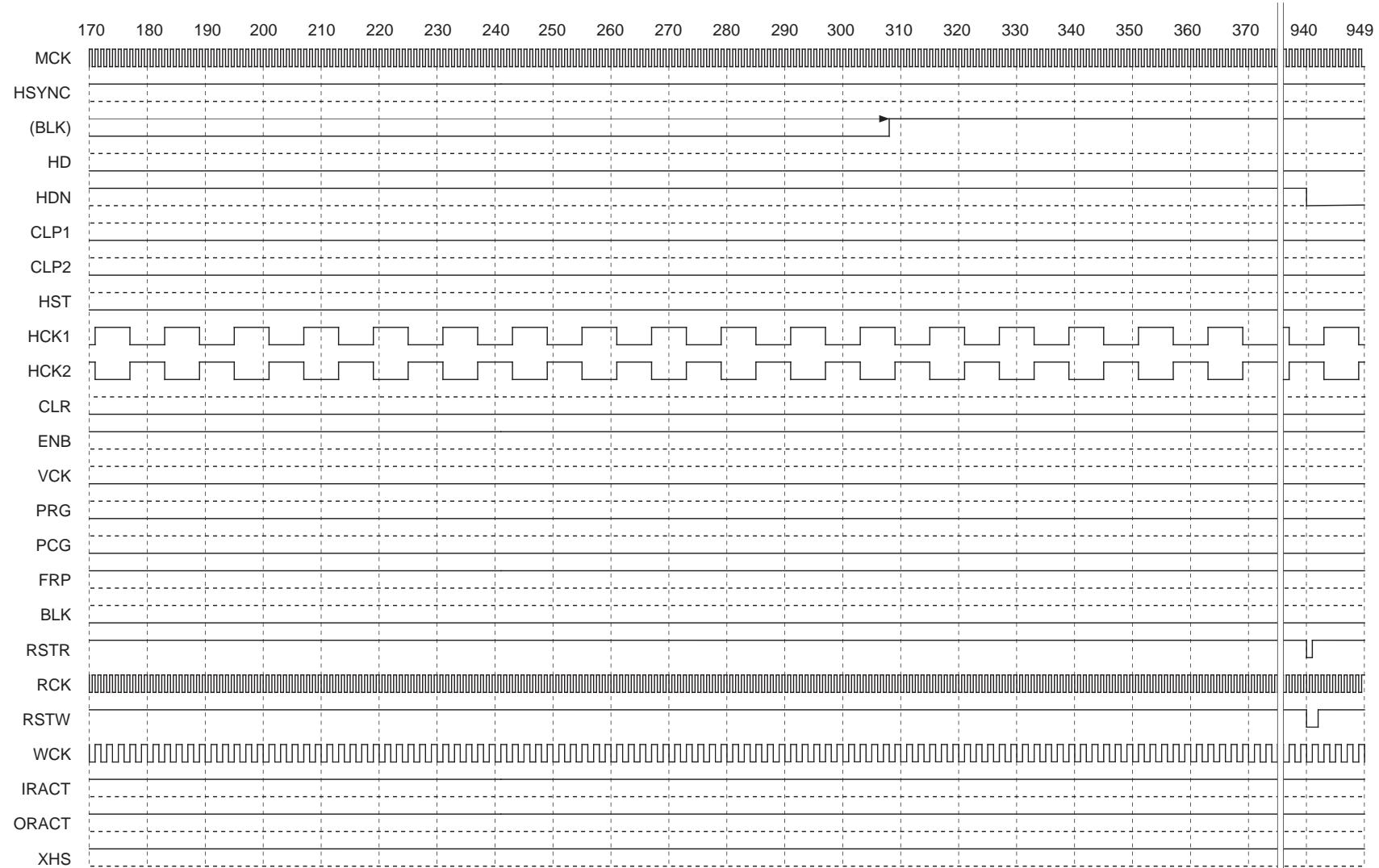
LCX016 PAL_2 762 × 572

RGT : H   PLLP : HHHLHLHLHHL (LSB)   HP : HHLLHHHH (LSB)   HSTP : LLLH (LSB)   PCGP : LHLLL (LSB)   PRGP : LHLHH (LSB)
CLPP : LL (LSB)   HPOL : L   HDNPOL : H   CLPPOL : H   PCGPOL : H   PRGPOL : H   HR : H   HST : H   PCG : H   DSP : L

Loop Counter : 1880 clk
MCK f : 29.38MHz (34.04ns)

Note) When RGT is Low, HCK1 and 2 are inversed.
       The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 NTSC_WIDE 832 × 480

MODE3/2/1 : H/L/H   MODE B/A : L/H   MODE021 : L   DWN : H   VP : LLLHHLLL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : H


Signal labels (top to bottom): VSYNC, HSYNC, HD, HDN, (BLK), VST, VCK, FRP, HST, ENB, CLP1, CLP2, PCG, PRG, CLR, FRP, FLDO, BLK, IRACT, ORACT, XHS, XVS

454 460 470 480 1 10 20 30 49

1 2

Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP and FLDO polarity are not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

RGT : H　PLLP : LHHLLHHHHHL (LSB)　HP : HHLLHHHL (LSB)　HSTP : LLLH (LSB)　PCGP : LHLLH (LSB)　PRGP : LHHLH (LSB)
CLPP : LL (LSB)　HPOL : L　HDNPOL : H　CLPPOL : H　PCGPOL : H　PRGPOL : H　HR : H　HST : H　PCG : H　DSP : H

Loop Counter : 1014 clk
MCK f : 31.90MHz (31.35ns)
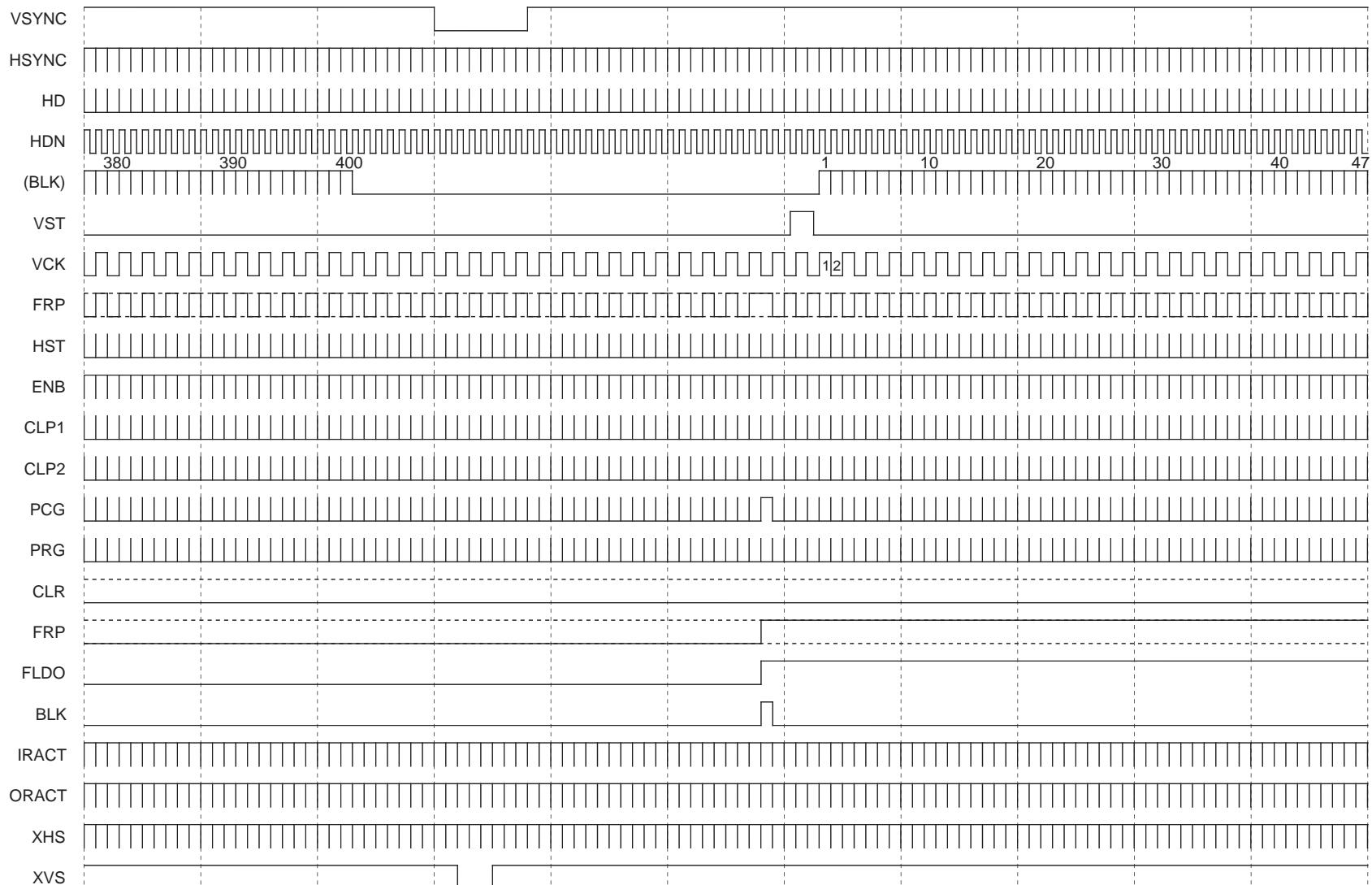
SONY

974　984　994　1004　0　10　20　30　40　50　60　70　80　90　100　110　120　130　140　150　160　170　180

MCK

HSYNC　79 clk

(BLK)　24 clk　79 clk

HD　120 clk

HDN

CLP1　38 clk

CLP2　13 clk　13 clk　13 clk　13 clk

HST

HCK1

HCK2

CLR

ENB　80 clk　32 clk

VCK

PRG　56 clk

PCG　40 clk

FRP

BLK

RSTR

RCK

RSTW

WCK

IRACT　128 clk

ORACT　128 clk

XHS　34 clk　32 clk

Note) When RGT is Low, HCK1 and 2 are inversed.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

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CXD2464R

LCX016 PC98 640 × 400

MODE3/2/1 : L/L/H   MODE B/A : L/H   MODE021 : L   DWN : H   VP : LLLHHLHL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : H
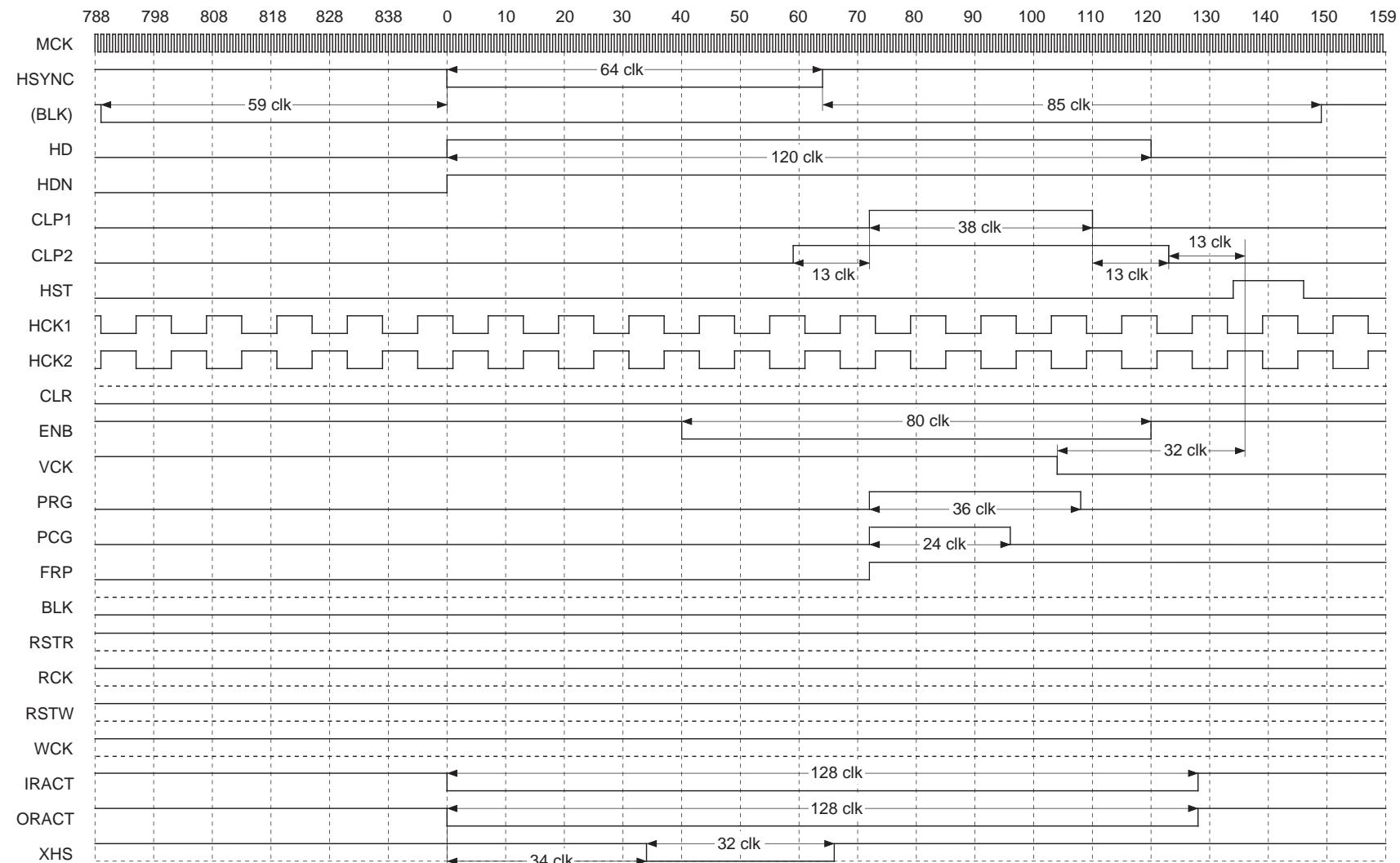
VSYNC

HSYNC

HD

HDN

(BLK)

VST

VCK

FRP

HST

ENB

CLP1

CLP2

PCG

PRG

CLR

FRP

FLDO

BLK

IRACT

ORACT

XHS

XVS

Note) When DWN is Low, VST is inversed.
       The 1H and 1V cycle FRP and FLDO polarity are not specified.
       The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

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LCX016 PC98 640 × 400

RGT : H   PLLP : LHHLHLLHHHL (LSB)   HP : HHLHLHHH (LSB)   HSTP : LLLH (LSB)   PCGP : LLHLH (LSB)   PRGP : LHLLH (LSB)

CLPP : LL (LSB)   HPOL : L   HDNPOL : H   CLPPOL : H   PCGPOL : H   PRGPOL : H   HR : H   HST : H   PCG : H   DSP : H

Loop Counter : 848 clk
MCK f : 21.05MHz (47.50ns)

Note) When RGT is Low, HCK1 and 2 are inversed.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

SONY

CXD2464R
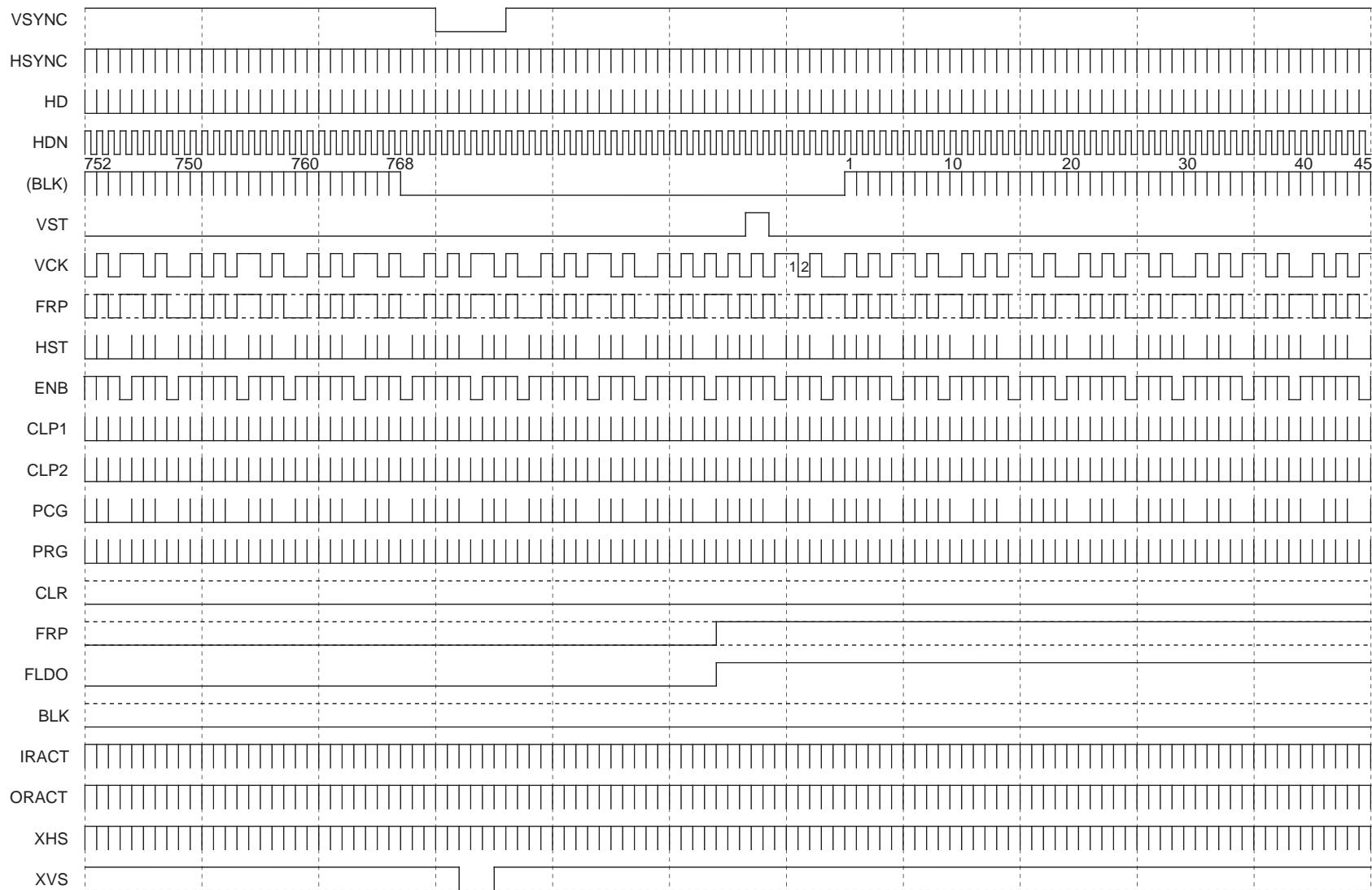
LCX016   XGA   1024 × 768

MODE3/2/1 : L/L/L   MODE B/A : L/H   MODE021 : L   DWN : H   VP : LLLHLHHL (LSB)   MBK2/1/0/B/A : H/H/L/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : H
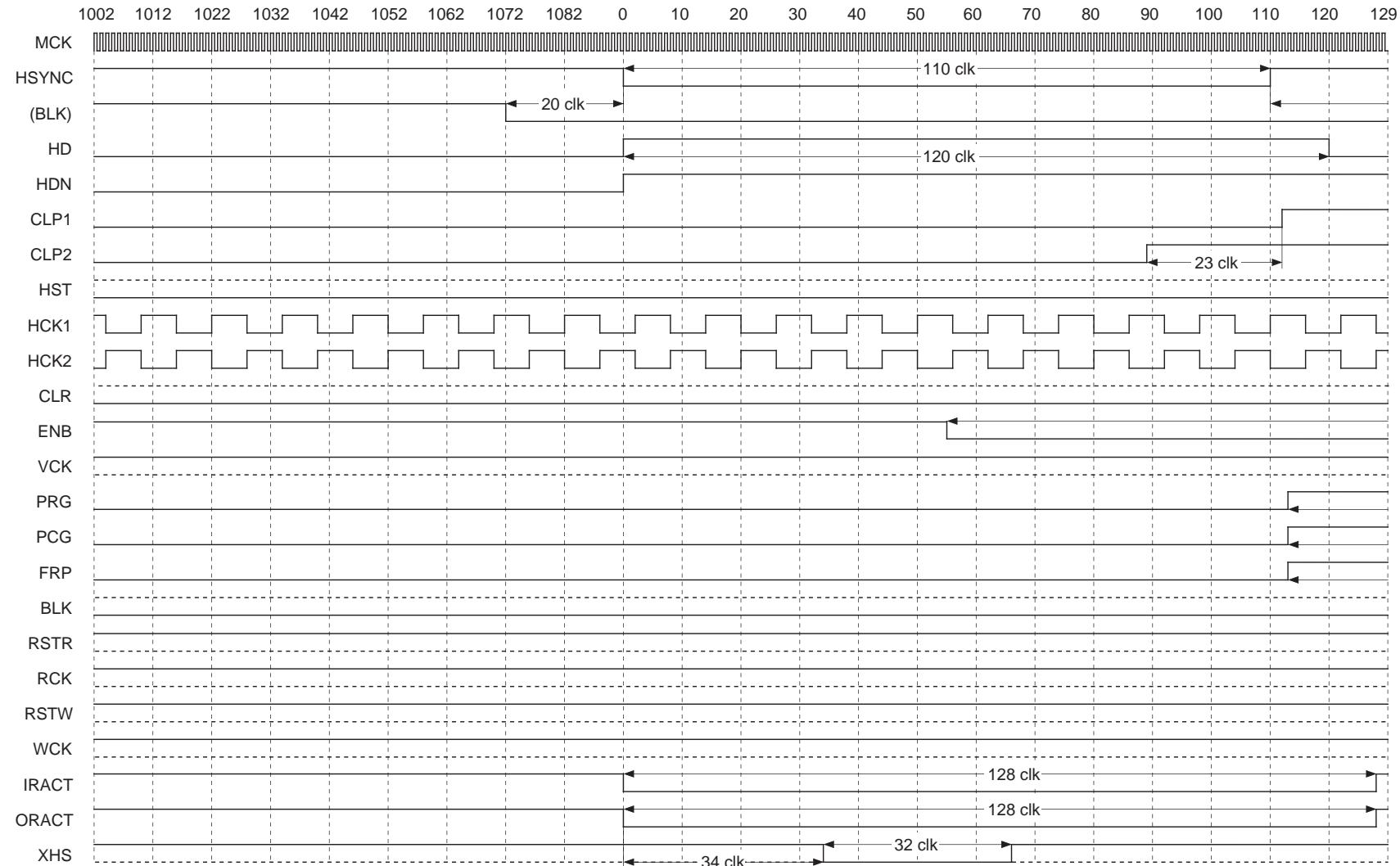
Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP and FLDO polarity are not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX016 XGA_1 1024 × 768

RGT : H   PLLP : HLLLHLLLLHL (LSB)   HP : HHLLHLLL (LSB)   HSTP : LLLH (LSB)   PCGP : LHHHH (LSB)   PRGP : HLHLH (LSB)
CLPP : LL (LSB)   HPOL : L   HDNPOL : H   CLPPOL : H   PCGPOL : H   PRGPOL : H   HR : H   HST : H   PCG : H   DSP : H

Loop Counter : 1092 clk
MCK f : 52.81MHz (18.94ns)

Note) When RGT is Low, HCK1 and 2 are inversed.
      The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

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CXD2464R
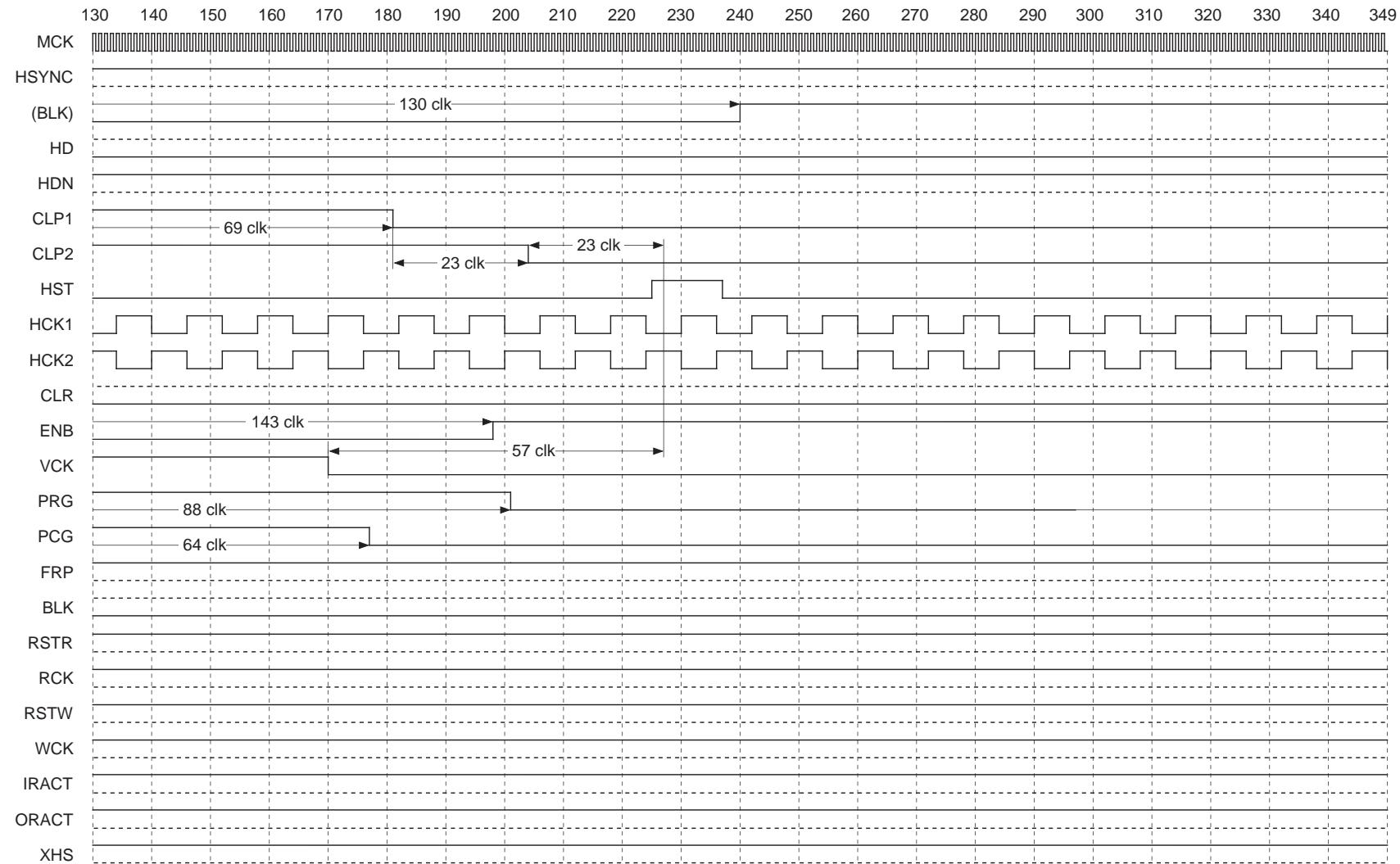
LCX016　XGA_2　1024 × 768

RGT : H　PLLP : HLLLHLLLLHL (LSB)　HP : HHLLHLLL (LSB)　HSTP : LLLH (LSB)　PCGP : LHHHH (LSB)　PRGP : HLHLH (LSB)
CLPP : LL (LSB)　HPOL : L　HDNPOL : H　CLPPOL : H　PCGPOL : H　PRGPOL : H　HR : H　HST : H　PCG : H　DSP : H

Loop Counter : 1092 clk
MCK f : 52.81MHz (18.94ns)

Note) When RGT is Low, HCK1 and 2 are inversed.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL VGA 640 × 480

MODE3/2/1 : H/H/L   MODE B/A : L/L   MODE021 : L   DWN : H   VP : LLLHLHHL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : H

VSYNC
HSYNC
HD
HDN
460   470   480   1   10   20   30   40   49
(BLK)
VST
VCK   1 2
FRP
HST
ENB
CLP1
CLP2
PCG
PRG
CLR
FRP
FLDO
BLK
IRACT
ORACT
XHS
XVS

Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP and FLDO polarity are not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
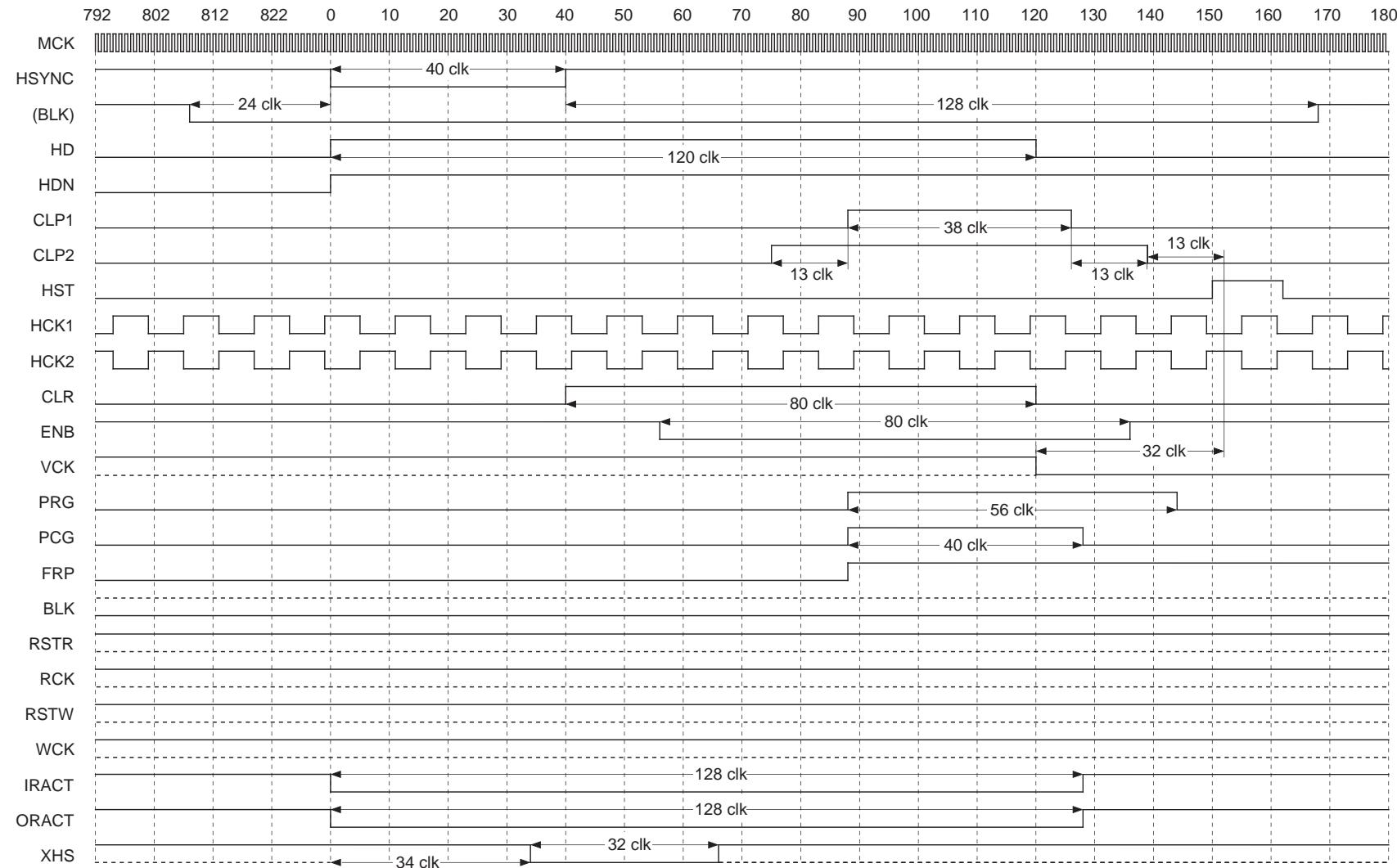
LCX012BL VGA 640 × 480

RGT : H PLLP : LHHLLHHHHHL (LSB) HP : HHLLLHHH (LSB) HSTP : LLLH (LSB) PCGP : LHLLH (LSB) PRGP : LHHLH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : H

Loop Counter : 832 clk
MCK f : 31.50MHz (31.75ns)

Note) When RGT is Low, HCK1 and 2 have the same polarity.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

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SONY

CXD2464R
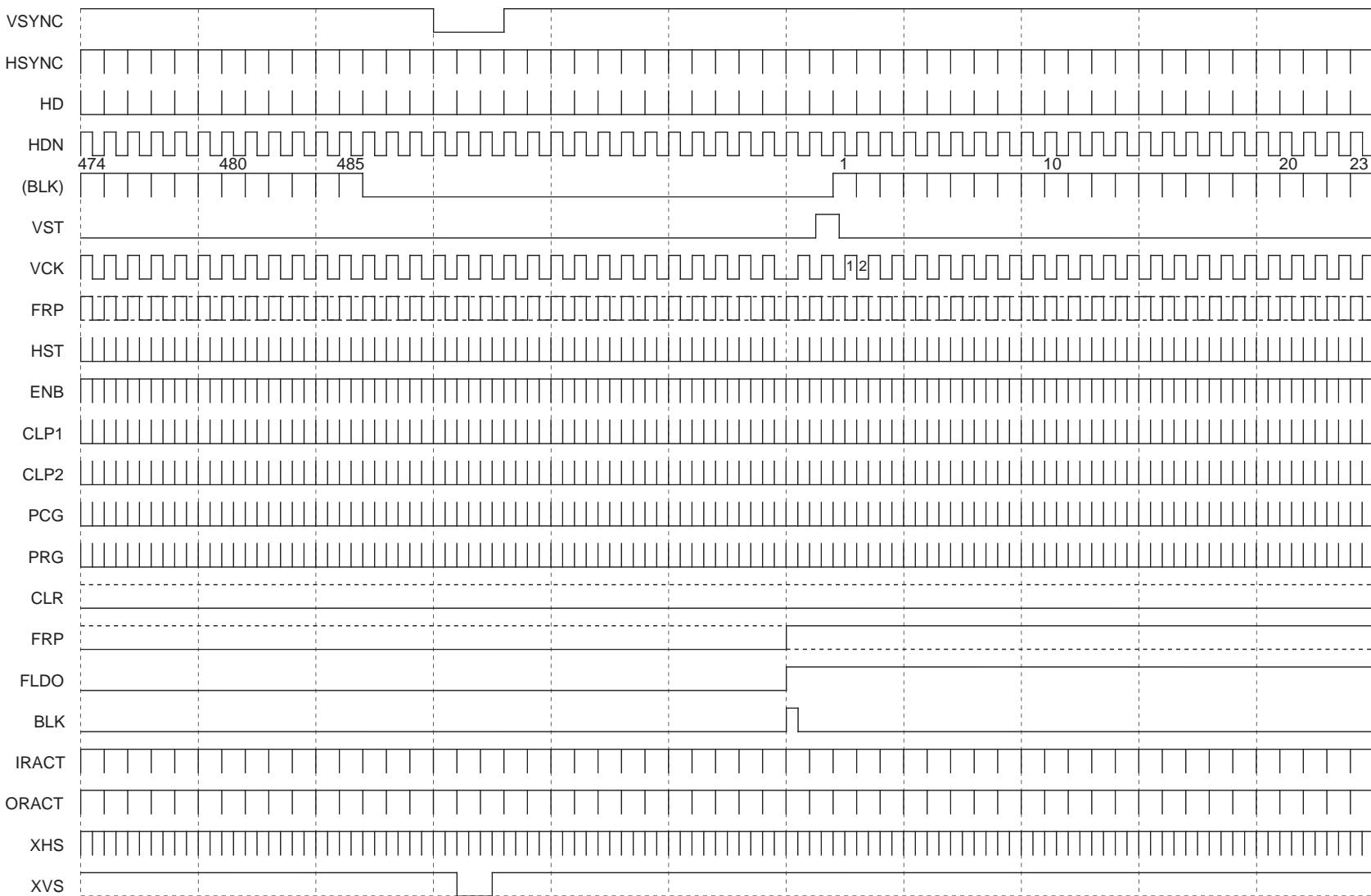
LCX012BL NTSC (ODD) 640 × 480

MODE3/2/1 : H/H/L MODE B/A : L/L MODE021 : L DWN : H VP : LLLLHHLH (LSB) MBK2/1/0/B/A : H/H/H/L/L FRP1/0 : H/H VPOL : L VGAV : L PC98 : H
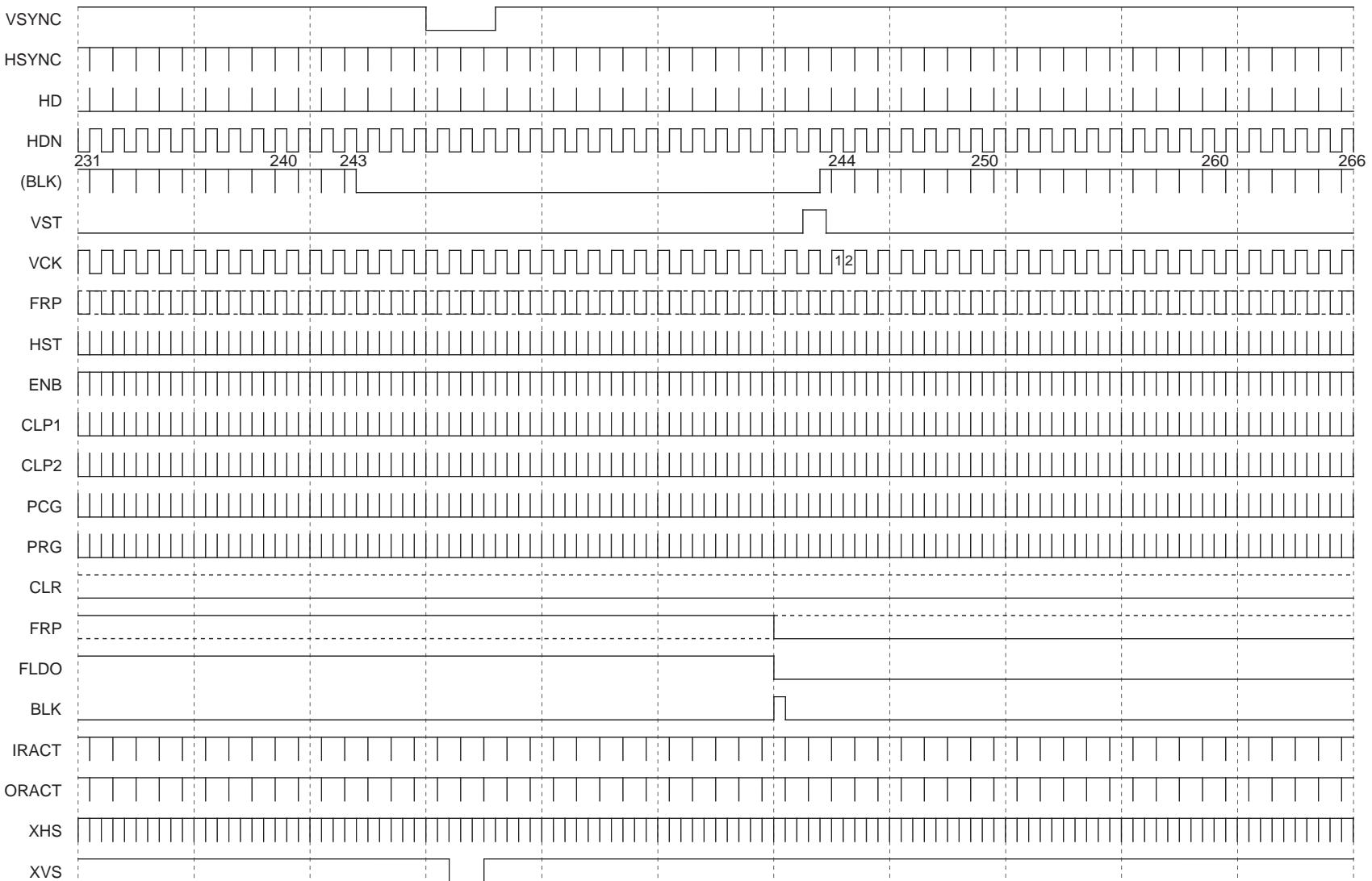
Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP polarity is not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL   NTSC (EVEN)   640 × 480

MODE3/2/1 : H/H/L   MODE B/A : L/L   MODE021 : L   DWN : H   VP : LLLLHHLH (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : L   PC98 : H
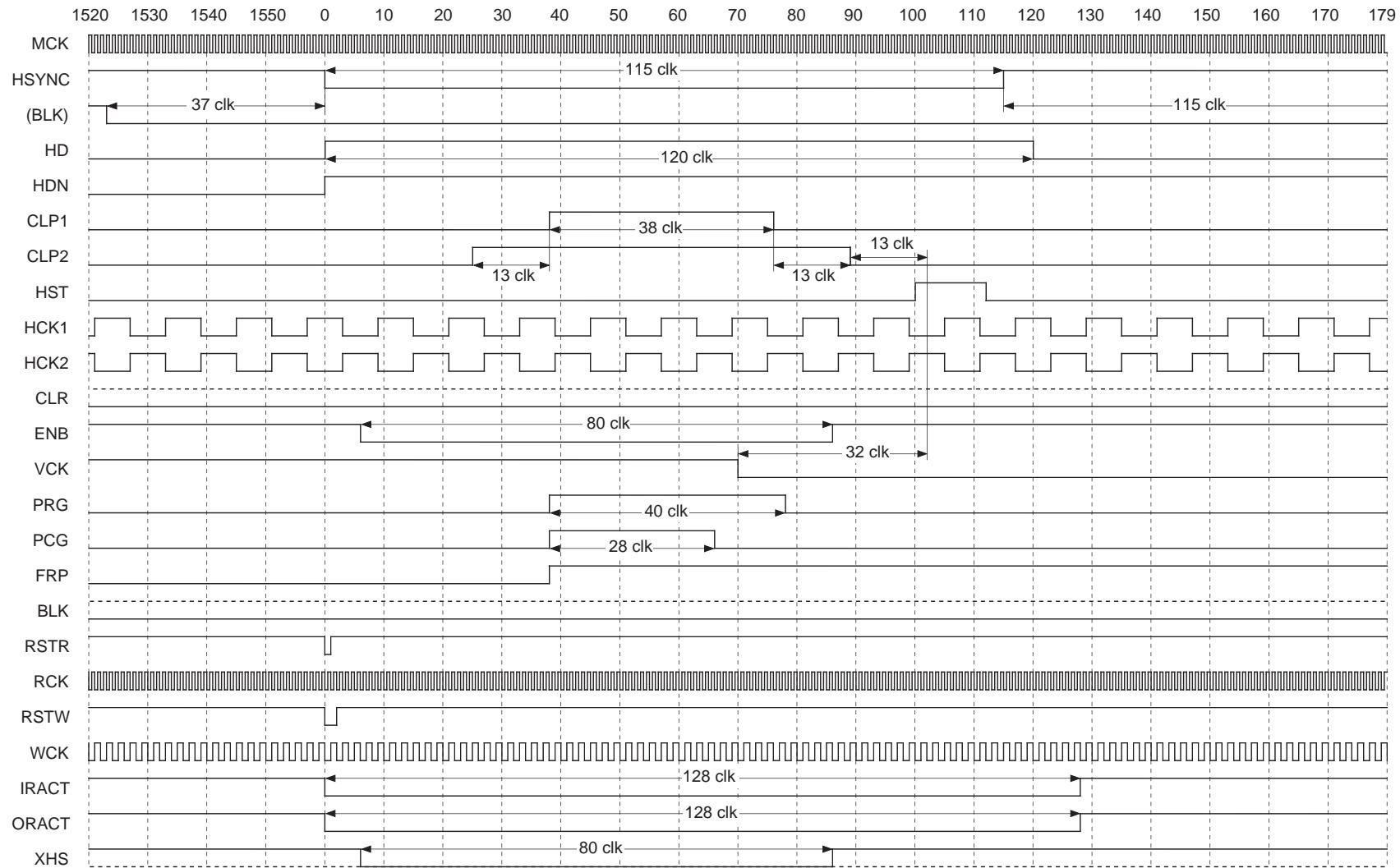

Note) When DWN is Low, VST is inversed.
       The 1H and 1V cycle FRP polarity is not specified.
       The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL NTSC_1 640 × 480

RGT : H PLLP : HHLLLLHLHHL (LSB) HP : HHHHHLLH (LSB) HSTP : LLLH (LSB) PCGP : LLHHL (LSB) PRGP : LHLLH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : L

Loop Counter : 1560 clk
MCK f : 24.54MHz (40.75ns)
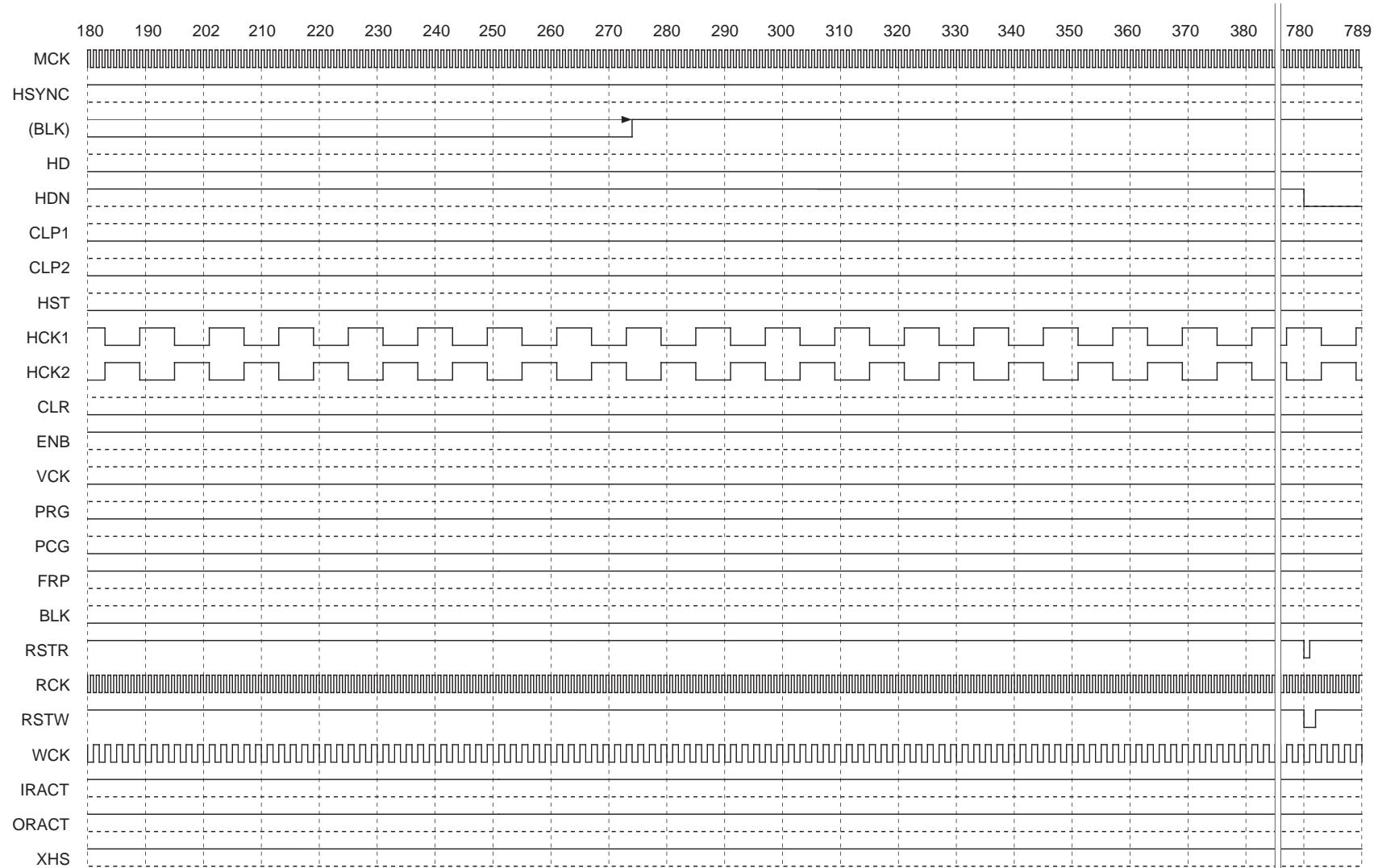
Note) When RGT is Low, HCK1 and 2 have the same polarity.
        The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL   NTSC_2   640 × 480

RGT : H   PLLP : HHLLLLHLHHL (LSB)   HP : HHHHHLLH (LSB)   HSTP : LLLH (LSB)   PCGP : LLHHL (LSB)   PRGP : LHLLH (LSB)

CLPP : LL (LSB)   HPOL : L   HDNPOL : H   CLPPOL : H   PCGPOL : H   PRGPOL : H   HR : H   HST : H   PCG : H   DSP : L

Loop Counter : 1560 clk
MCK f : 24.54MHz (40.75ns)

SONY

| 180 | 190 | 202 | 210 | 220 | 230 | 240 | 250 | 260 | 270 | 280 | 290 | 300 | 310 | 320 | 330 | 340 | 350 | 360 | 370 | 380 | 780 | 789 |

MCK
HSYNC
(BLK)
HD
HDN
CLP1
CLP2
HST
HCK1
HCK2
CLR
ENB
VCK
PRG
PCG
FRP
BLK
RSTR
RCK
RSTW
WCK
IRACT
ORACT
XHS

Note) When RGT is Low, HCK1 and 2 have the same polarity.
         The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

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CXD2464R
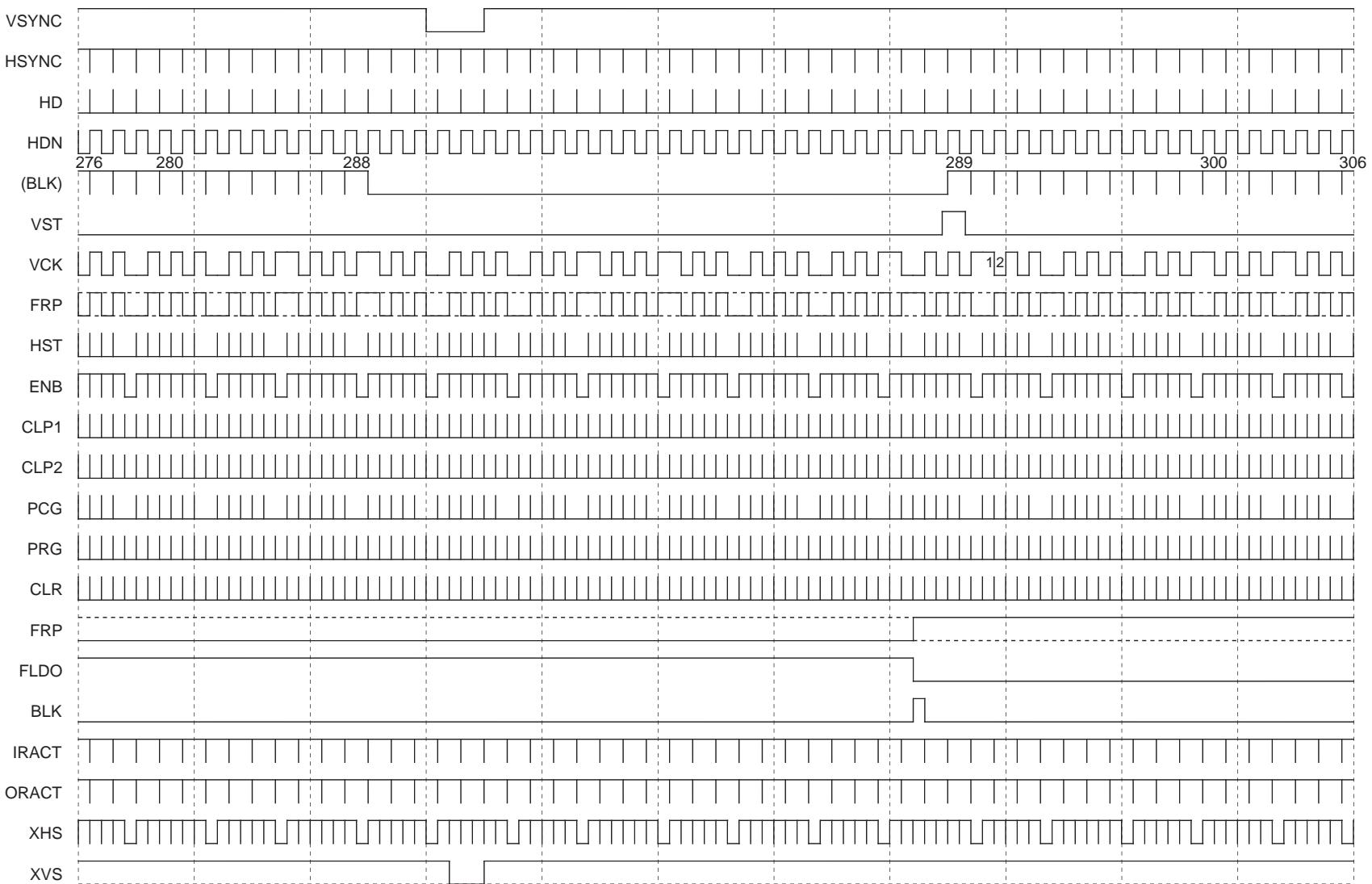
LCX012BL   PAL (ODD)   640 × 480

MODE3/2/1 : H/H/L   MODE B/A : L/L   MODE021 : L   DWN : H   VP : LLLHLLHL (LSB)   MBK2/1/0/B/A : H/L/L/L/L   FRP1/0 : H/H   VPOL : L   VGAV : L   PC98 : H
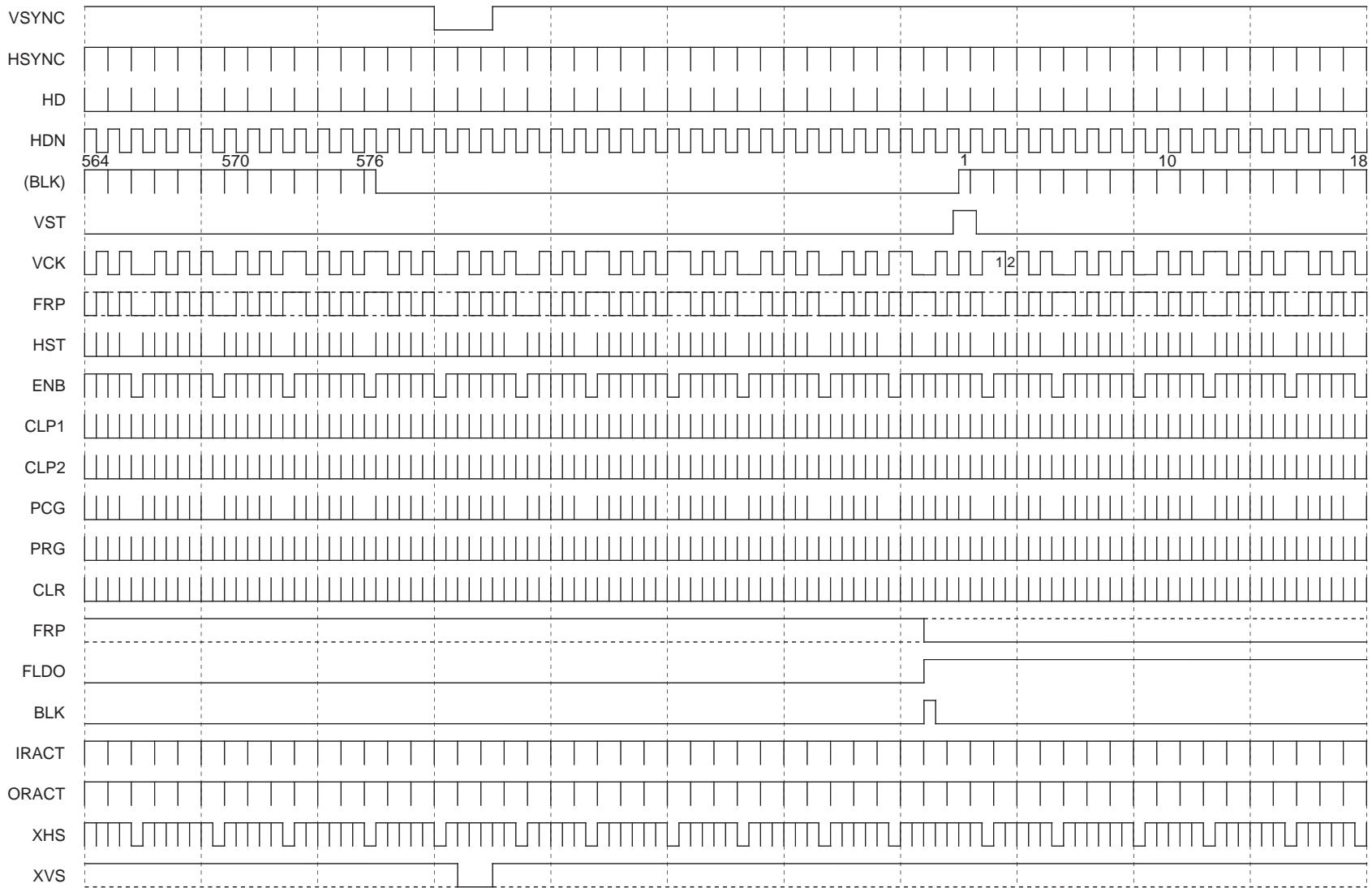

Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP polarity is not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL   PAL (EVEN)   640 × 480

MODE3/2/1 : H/H/L   MODE B/A : L/L   MODE021 : L   DWN : H   VP : LLLHLLHL (LSB)   MBK2/1/0/B/A : H/L/L/L/L   FRP1/0 : H/H   VPOL : L   VGAV : L   PC98 : H
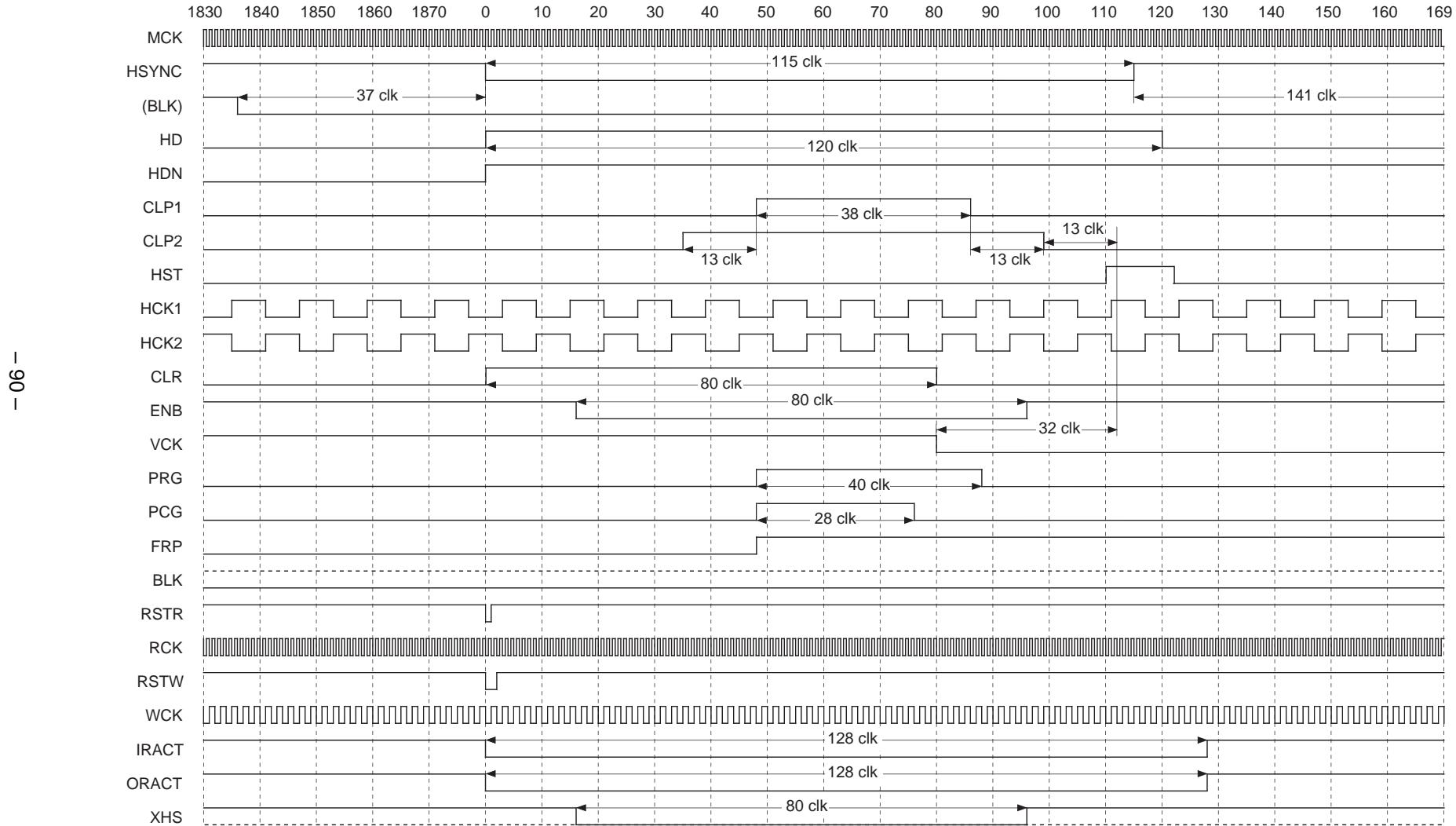

Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP polarity is not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL PAL_1 640 × 480

RGT : H PLLP : HHLLLLHLHHL (LSB) HP : HHHLHHHH (LSB) HSTP : LLLH (LSB) PCGP : LLHHL (LSB) PRGP : LHLLH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : L

Loop Counter : 1560 clk
MCK f : 24.38MHz (41.02ns)
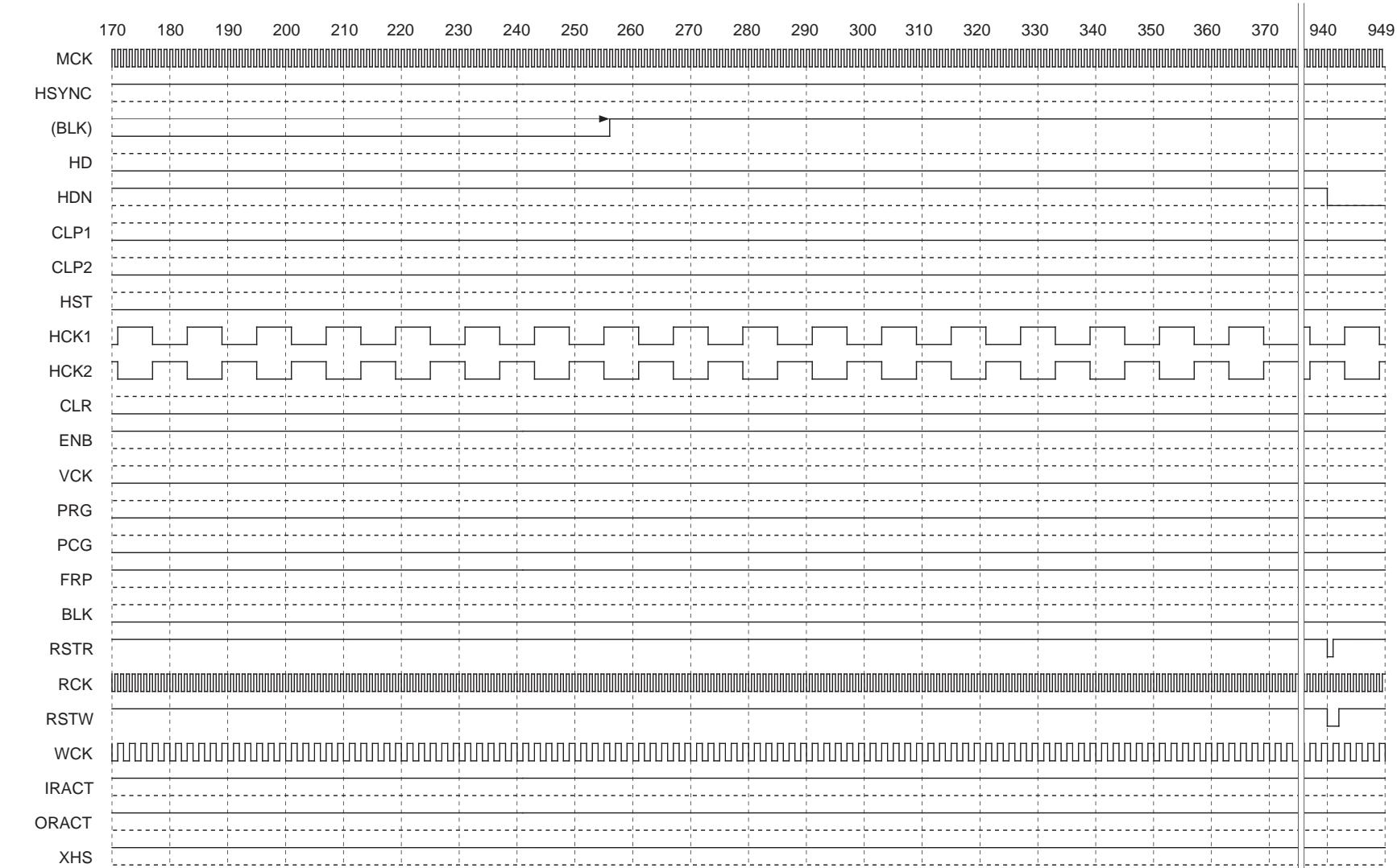
— 90 —

Note) When RGT is Low, HCK1 and 2 have the same polarity.
       The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL PAL_2 640 × 480

RGT : H PLLP : HHLLLLHLHHL (LSB) HP : HHHLHHHH (LSB) HSTP : LLLH (LSB) PCGP : LLHHL (LSB) PRGP : LHLLH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : L

Loop Counter : 1560 clk
MCK f : 21.38MHz (41.02ns)
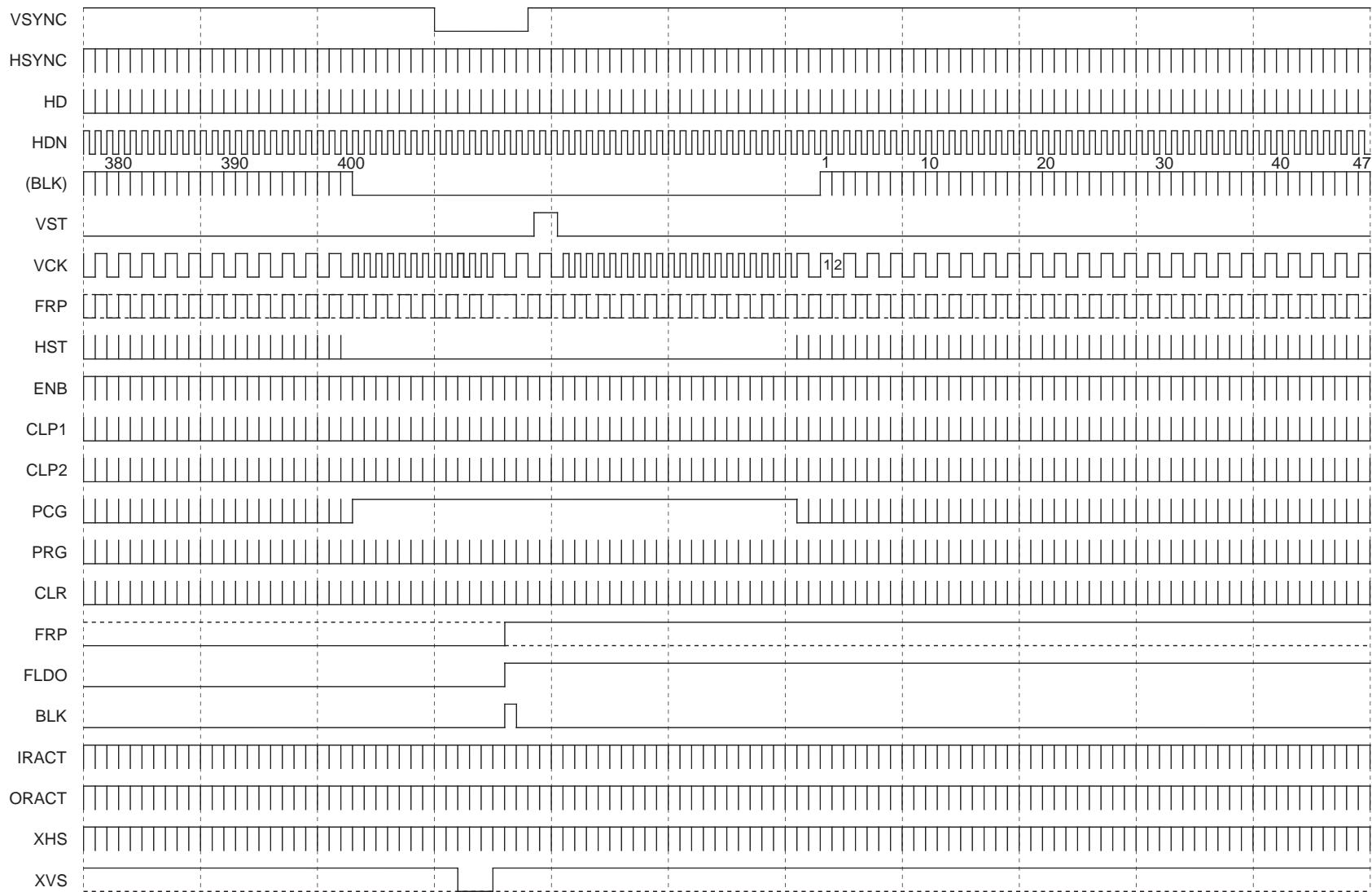
Note) When RGT is Low, HCK1 and 2 have the same polarity.
         The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL PC98 640 × 400

MODE3/2/1 : H/H/L   MODE B/A : L/L   MODE021 : L   DWN : H   VP : LLLLLHLL (LSB)   MBK2/1/0/B/A : H/H/H/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : L


Note) When DWN is Low, VST is inversed.
      The 1H and 1V cycle FRP and FLDO polarity are not specified.
      The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
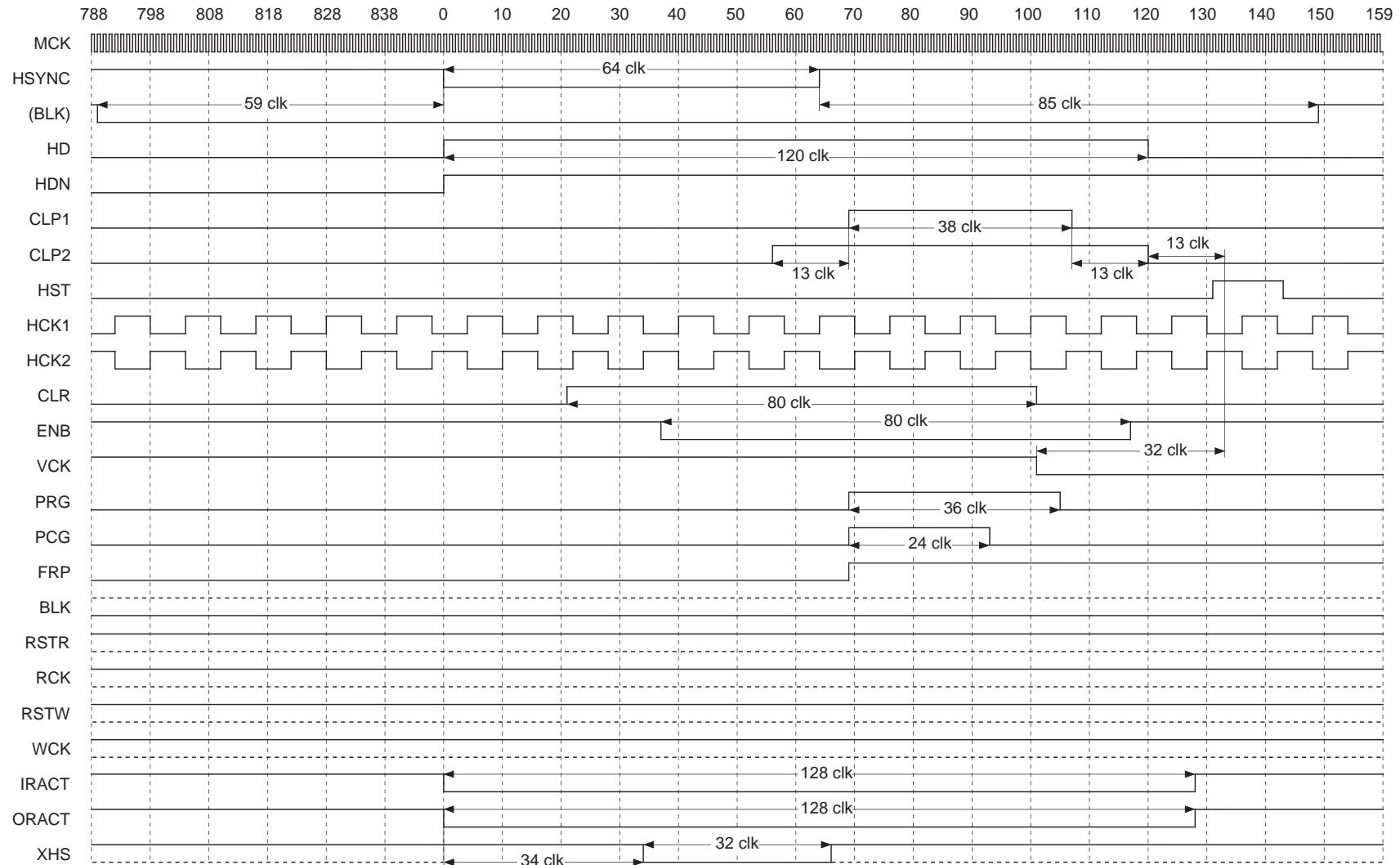
LCX012BL PC98 640 × 400

RGT : H PLLP : LHHLHLLHHHL (LSB) HP : HHLHHLHH (LSB) HSTP : LLLH (LSB) PCGP : LLHLH (LSB) PRGP : LHLLH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : H

Loop Counter : 848 clk
MCK f : 21.05MHz (47.50ns)

| 788 | 798 | 808 | 818 | 828 | 838 | 0 | 10 | 20 | 30 | 40 | 50 | 60 | 70 | 80 | 90 | 100 | 110 | 120 | 130 | 140 | 150 | 159 |

MCK

HSYNC — 64 clk

(BLK) — 59 clk — 85 clk

HD — 120 clk

HDN

CLP1 — 38 clk

CLP2 — 13 clk / 13 clk / 13 clk

HST

HCK1

HCK2

CLR — 80 clk

ENB — 80 clk

VCK — 32 clk

PRG — 36 clk

PCG — 24 clk

FRP

BLK

RSTR

RCK

RSTW

WCK

IRACT — 128 clk

ORACT — 128 clk

XHS — 32 clk — 34 clk
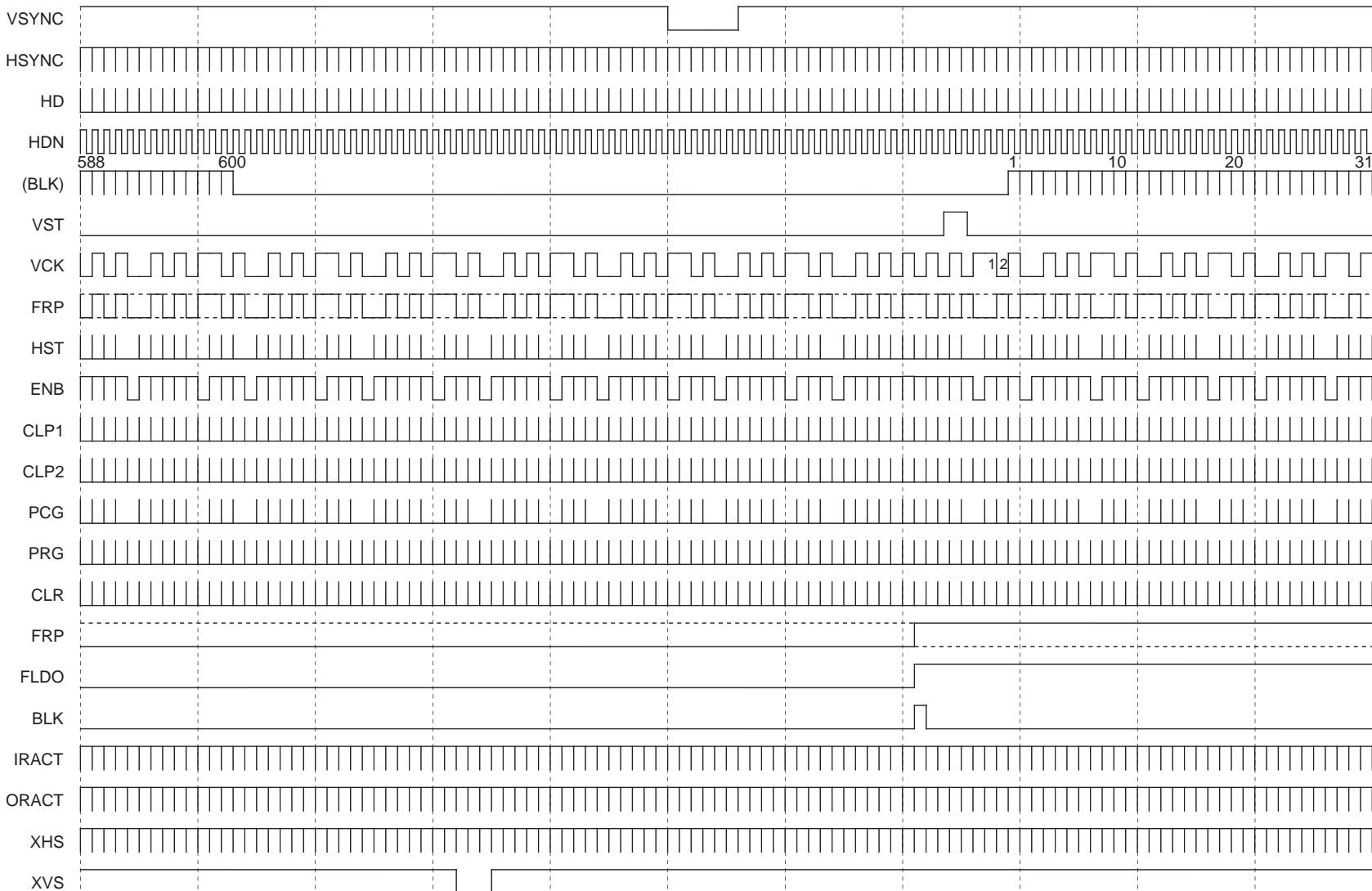
Note) When RGT is Low, HCK1 and 2 have the same polarity.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

LCX012BL SVGA 640 × 480

MODE3/2/1 : H/H/L   MODE B/A : L/L   MODE021 : L   DWN : H   VP : LLLHLLHH (LSB)   MBK2/1/0/B/A : H/H/L/L/L   FRP1/0 : H/H   VPOL : L   VGAV : H   PC98 : H


Note) When DWN is Low, VST is inversed.
The 1H and 1V cycle FRP and FLDO polarity are not specified.
The fifth row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.
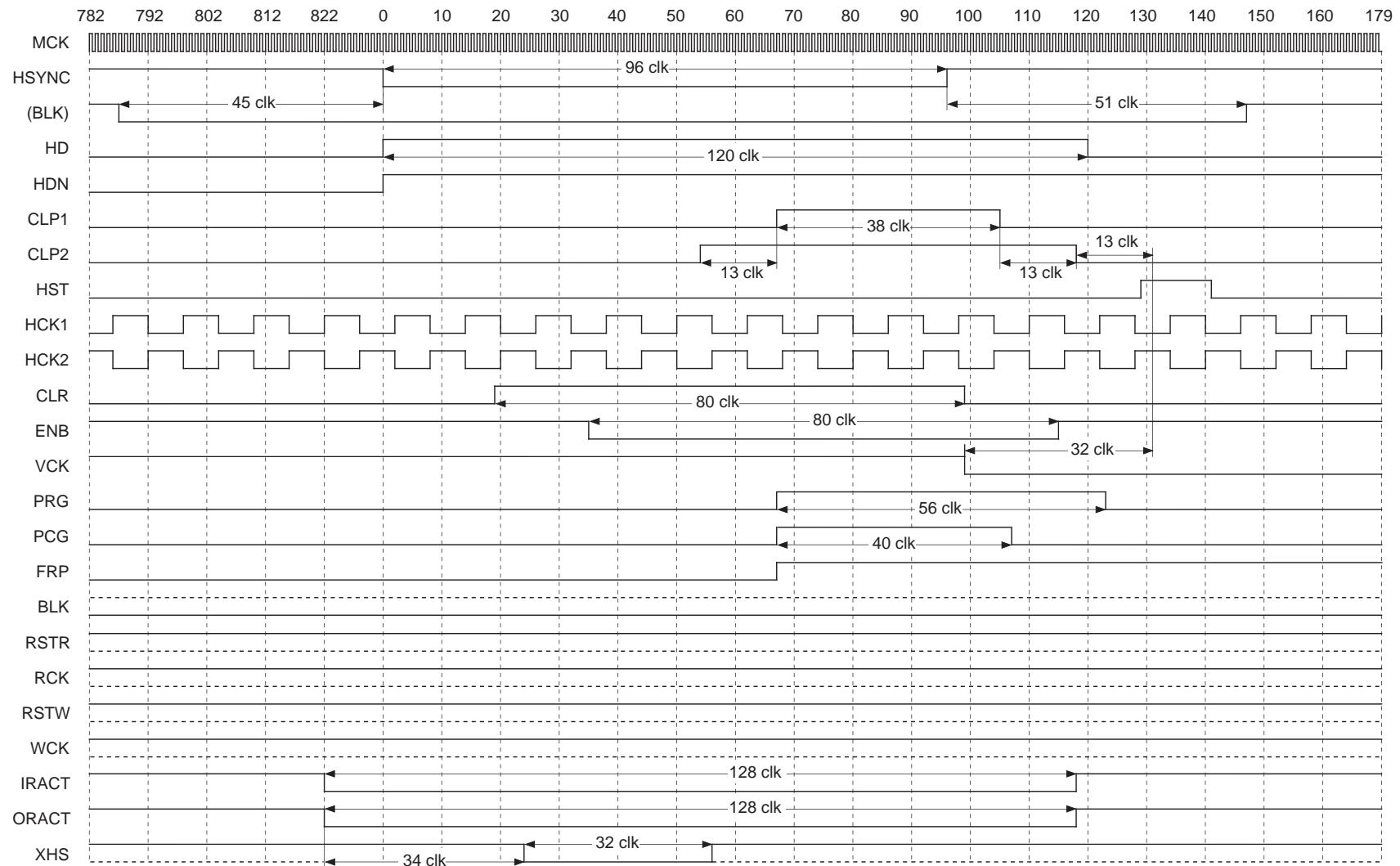
LCX012BL SVGA 640 × 480

RGT : H PLLP : LHHLLHHHHHL (LSB) HP : HHLHHHLL (LSB) HSTP : LLLH (LSB) PCGP : LHLLH (LSB) PRGP : LHHLH (LSB)
CLPP : LL (LSB) HPOL : L HDNPOL : H CLPPOL : H PCGPOL : H PRGPOL : H HR : H HST : H PCG : H DSP : H

Loop Counter : 832 clk
MCK f : 40.00MHz (25.00ns)
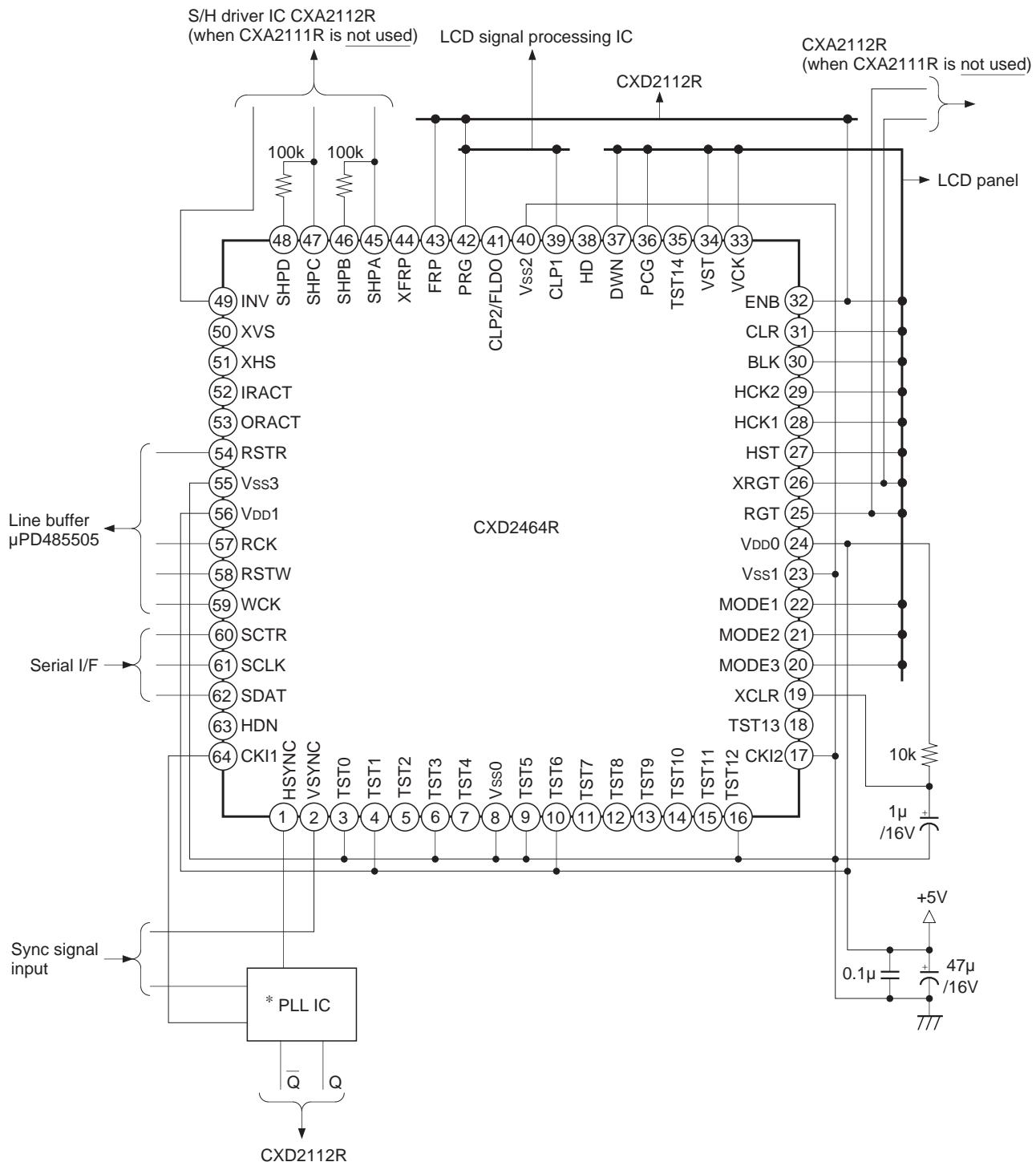
| 782 | 792 | 802 | 812 | 822 | 0 | 10 | 20 | 30 | 40 | 50 | 60 | 70 | 80 | 90 | 100 | 110 | 120 | 130 | 140 | 150 | 160 | 179 |

MCK

HSYNC — 96 clk

(BLK) — 45 clk — 51 clk

HD — 120 clk

HDN

CLP1 — 38 clk

CLP2 — 13 clk / 13 clk / 13 clk

HST

HCK1

HCK2

CLR — 80 clk / 80 clk

ENB

VCK — 32 clk

PRG — 56 clk

PCG — 40 clk

FRP

BLK

RSTR

RCK

RSTW

WCK

IRACT — 128 clk

ORACT — 128 clk

XHS — 34 clk / 32 clk

Note) When RGT is Low, HCK1 and 2 have the same polarity.
The third row of the timing chart (BLK) is a pulse indicated as a reference and is not a pulse output from pins.

Application Circuit
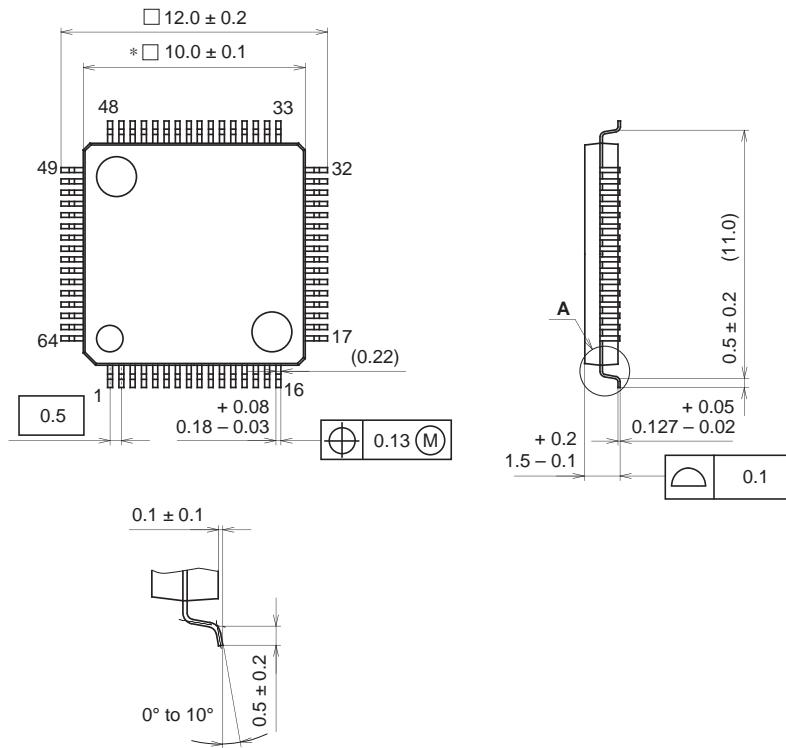
* PLL IC: Sony CXA3106Q (built-in phase comparator, frequency divider) is recommended.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Package Outline   Unit: mm

64PIN LQFP (PLASTIC)

□ 12.0 ± 0.2

∗ □ 10.0 ± 0.1

48   33
49   32
64   17
(0.22)
1   16

0.5

0.18 +0.08 −0.03

⊕ | 0.13 Ⓜ

A

0.5 ± 0.2

(11.0)

0.127 +0.05 −0.02

1.5 +0.2 −0.1

⌒ | 0.1

0.1 ± 0.1

0° to 10°   0.5 ± 0.2

DETAIL **A**

NOTE: Dimension "∗" does not include mold protrusion.

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER/PALLADIUM PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	0.3g

SONY CODE	LQFP-64P-L01
EIAJ CODE	LQFP064-P-1010
JEDEC CODE	———