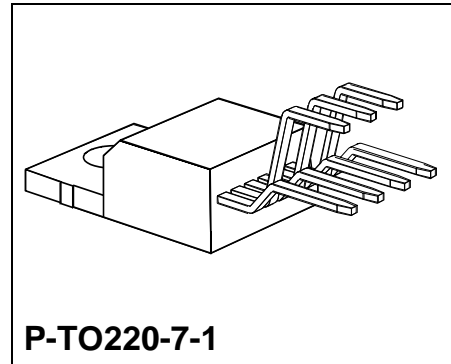


### Overview

#### Features

- Drives motors up to 2 A
- Integrated free-wheeling diodes 2.5 A
- Short-circuit proof to ground
- Overtemperature protection
- Low saturation voltages through bootstrap
- Wide temperature range
- Suitable for applications in automotive engineering



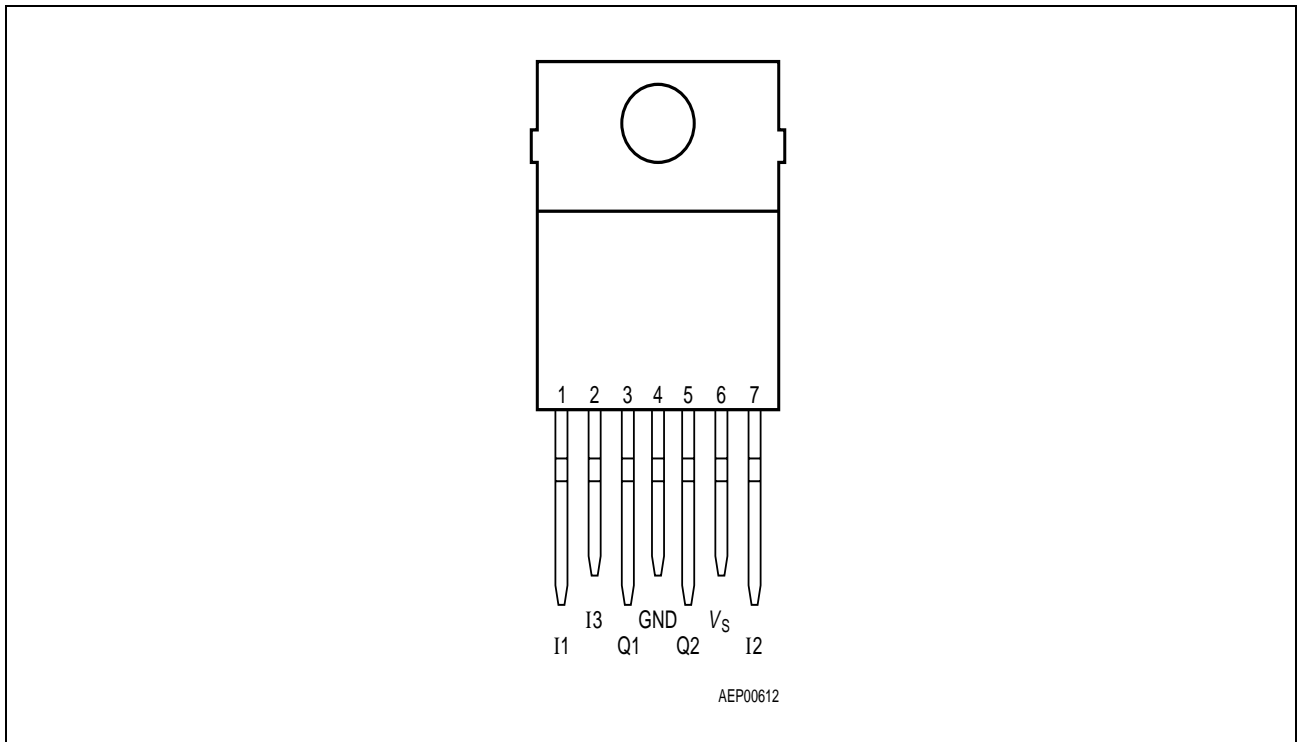
Type	Ordering Code	Package
TLE 4202 B	Q67000-A8225	P-TO220-7-1

#### Description

The two power comparators can switch magnets, motors or other loads either by being separated from each other or by being combined to a full-bridge circuit. The IC is designed for application in motor vehicles. It can be applied at package temperatures between  $-40\text{ }^{\circ}\text{C}$  and  $130\text{ }^{\circ}\text{C}$ .

The IC contains two amplifiers featuring a typical open-loop voltage gain of 80 dB at 500 Hz.

The input stages are PNP differential amplifiers thus resulting in a common-mode input voltage range from 0 V to approx. the value of  $V_S$  and in a maximum input differential voltage of  $V_S$ . To obtain low saturation voltages at the sink circuit, the drive circuit of the sink transistor is connected to the supply voltage. An SOA protective circuit protects the IC against ground short-circuits. At chip temperatures above approx.  $160\text{ }^{\circ}\text{C}$  the source transistors are turned off.



**Figure 1 Pin Configuration (top view)**

## Pin Definitions and Functions

Pin No.	Symbol	Function
1	I1	<b>Input 1</b> Non-inverting input 1, to be connected to pin 2 and pin 3 according to general rules
2	I3	<b>Inverting input 3</b> Inverting inputs of the two comparators; internally connected to reference voltage across 50 kΩ (typ. 1.7 V)
3	Q1	<b>Output Q1</b> Push-pull output B DC-short-circuit proof to ground. Integrated free-wheel diodes to ground and to supply voltage
4	GND	<b>Ground</b>
5	Q2	<b>Output Q2</b> , see pin 3
6	V <sub>s</sub>	<b>Supply voltage</b> Has to be blocked to ground with a ceramic capacitor of at least 100 nF directly at the pins of the ICs
7	I2	<b>Input 2</b> Non-inverting input 2; see pin 1

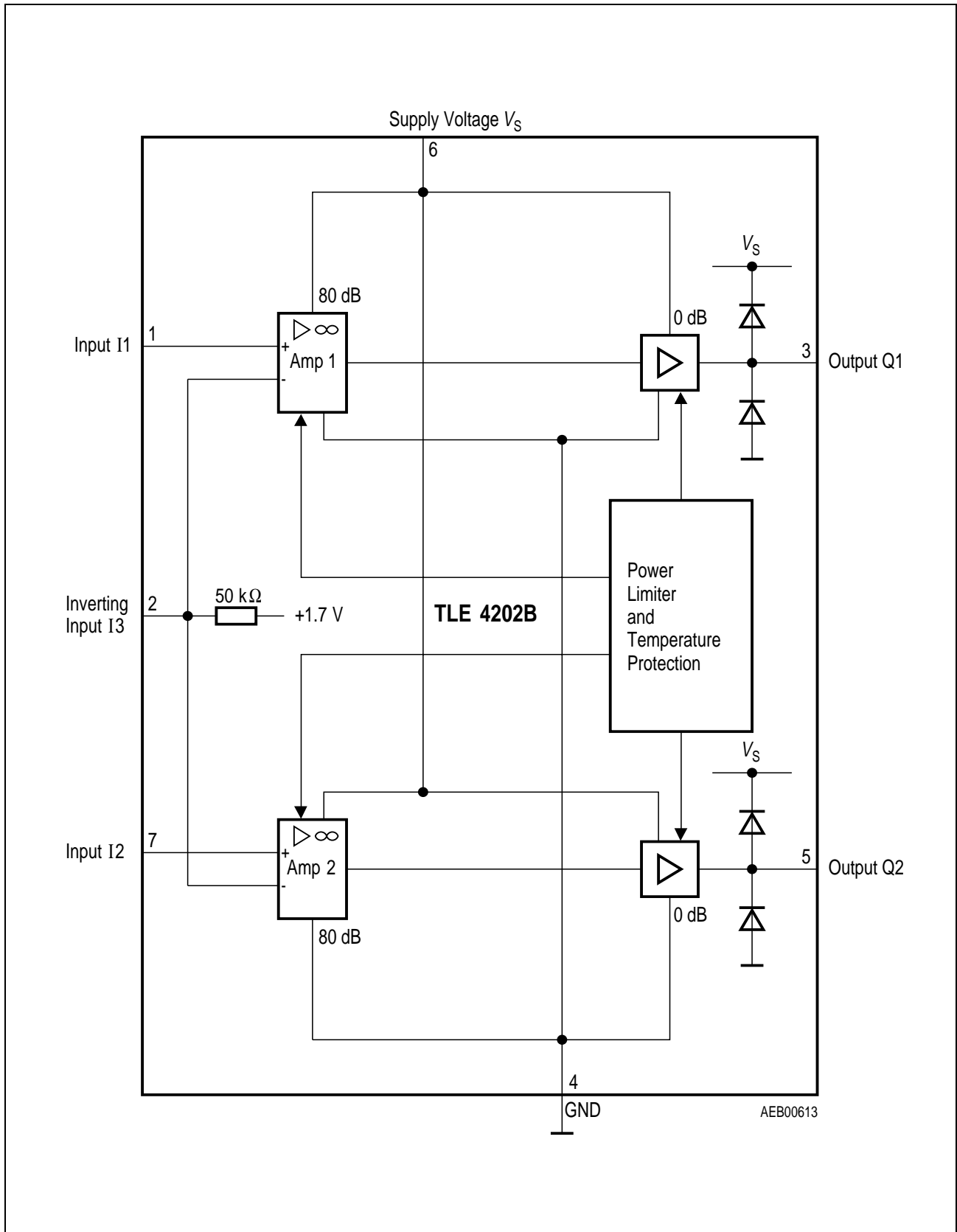


Figure 2 Block Diagram

## Absolute Maximum Ratings

$T_C = -40$  to  $130$  °C

Parameter	Symbol	Limit Values		Unit
		min.	max.	
Supply voltage	$V_S$	–	40	V
Output current of sink transistors $T_C \leq 85$ °C	$I_Q$	–	2.5	A
Output current of source transistors internally limited	$I_Q$	–	–	–
Diode peak currents to + $V_S$	$I_{F+}$	–	2.5	A
to ground	$I_{F-}$	–	2.5	A
Voltage at pins I1, I2, I3	$V_{1,2,7}$	– 0.3	$V_S$	V
Voltage at pins Q1, Q2 <sup>1)</sup>	$V_{3,5}$	–	–	V
Junction temperature	$T_j$	–	150	°C
Storage temperature	$T_{stg}$	– 55	125	°C

## Operating Range

Supply voltage	$V_S$	3.5	17	V
Case temperature during operation $R_L \geq 6 \Omega$ , $V_S = 7 \dots 16$ V	$T_C$	– 40	–	°C
$R_L \geq 9 \Omega$ , $V_S = 16$ V		–	130	°C
Voltage amplification (at negative feedback with external connection)	$V_V$	30	–	dB
Thermal resistance system - case	$R_{th SC}$	–	4	K/W

<sup>1)</sup> The output voltages are kept within a permissible range by free-wheel diodes

Outputs Q1 and Q2 short-circuit proof to ground

$R_L$ : Resistance between output 1 and output 2

## Characteristics

$V_S = 13\text{ V}; T_j = 25\text{ °C}$

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

## General Data

Quiescent current	$I_S$	–	15	25	mA	$S = 1$	1
Open-loop gain	$G_{VO}$	50	80	–	dB	$f = 500\text{ Hz}$ $V_S \leq 7\text{ V} \leq 16\text{ V}$ $T_C = -40\text{ °C to } 110\text{ °C}$	1

## Input Characteristics

Input current (pins I1, I2)	$I_{I1,7}$	–	1	3	$\mu\text{A}$	$V_{I1,12} = 0$	2
Input current	$I_{I2}$	–	35	70	$\mu\text{A}$	$V_{I2} = 0; V_{I1,7} = V_S$	1
	$-I_{I2}$	–	230	300	$\mu\text{A}$	$V_{I2} \leq V_S; V_{I1,7} = 0\text{ V}$	–
Input resistance	$R_{I1,7}$	1	5	–	$\text{M}\Omega$	$f$	1
Input reference voltage	$V_{I2}$	1.4	1.7	2	V	$= 1\text{ kHz}$	1
Input offset voltage	$V_{I0}$	–20	–	20	mV	$I_2 = 0; V_{I1,7} = 0\text{ V}$	3
						–	

## Characteristics (cont'd)

$V_S = 13\text{ V}$ ;  $T_j = 25\text{ °C}$

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

## Output Characteristics

Saturation voltages							
Source operation	$V_{\text{Sato}}$	–	0.9	1	V	$I_Q = -0.3\text{ A}$ ; $S1 = 1$	2
measured to $V_S$	$V_{\text{Sato}}$	–	1.2	1.6	V	$I_Q = -1.0\text{ A}$ ; $S1 = 1$	2
	$V_{\text{Sato}}$	–	1.5	2.1	V	$I_Q = -2\text{ A}$ ; $S1 = 1$	2
Sink operation	$V_{\text{Satu}}$	–	0.25	0.4	V	$I_Q = 0.3\text{ A}$ ; $S1 = 2$	2
			0.5	0.75	V	$I_Q = 1\text{ A}$ ; $S1 = 2$	2
	$V_{\text{Satu}}$	–	1	1.3	V	$I_Q = 2\text{ A}$ ; $S1 = 2$	2
Short-circuit current	$I_{\text{SC}}$	–	1.25	1.6	A	$V_Q = 0\text{ V}$	2
Diode forward voltage to + $V_S$	$V_{F+}$	–	1	1.3	V	$I_F = I_Q = 1\text{ A}$	2
to ground	$V_{F-}$	–	0.9	1.2	V	$I_F = I_Q = 1\text{ A}$	2
Slew rate falling edge	$SR$	–	6	–	V/ $\mu\text{s}$	–	1
Slew rate rising edge	$SR$	–	6	–	V/ $\mu\text{s}$	–	1

## Switching Times

Rise time of $V_Q$	$t_r$	–	1.5	–	$\mu\text{s}$	–	1
Fall time of $V_Q$	$t_f$	–	1.5	–	$\mu\text{s}$	–	1
Switch-ON delay	$t_{\text{ON}}$	–	3	–	$\mu\text{s}$	–	1
Switch-OFF delay	$t_{\text{OFF}}$	–	1.5	–	$\mu\text{s}$	–	1
Quiescent current	$I_S$	–	15	30	mA	$S = 1$	1

## Characteristics

$V_S \leq 7 \text{ V to } 17 \text{ V}; T_C = -40 \text{ to } 110 \text{ }^\circ\text{C}$

Parameter	Symbol	Limit Values			Unit	Test Condition	Test Circuit
		min.	typ.	max.			

## Saturation Voltage

Source operation measured to $V_S$	$V_{\text{Sato}}$	–	0.9	1.2	V	$I_Q = -0.3 \text{ A}; S = 1$	2
	$V_{\text{Sato}}$	–	1.2	1.8	V	$I_Q = -1 \text{ A}; S = 1$	2
	$V_{\text{Sato}}$	–	1.5	2.4	V	$I_Q = -2 \text{ A}; S = 1$	2
Sink operation	$V_{\text{Satu}}$	–	0.25	0.60	V	$I_Q = 0.3 \text{ A}; S1 = 2$	2
	$V_{\text{Satu}}$	–	0.5	1.1	V	$I_Q = 1 \text{ A}; S1 = 2$	2
	$V_{\text{Satu}}$	–	1.2	2	V	$I_Q = 2 \text{ A}; S1 = 2$	2
Short-circuit current	$-I_{\text{SC}}$	–	–	3.5	V	$V_Q = 0 \text{ V}$ $T_C = 25 \text{ }^\circ\text{C to } 110 \text{ }^\circ\text{C}$	–



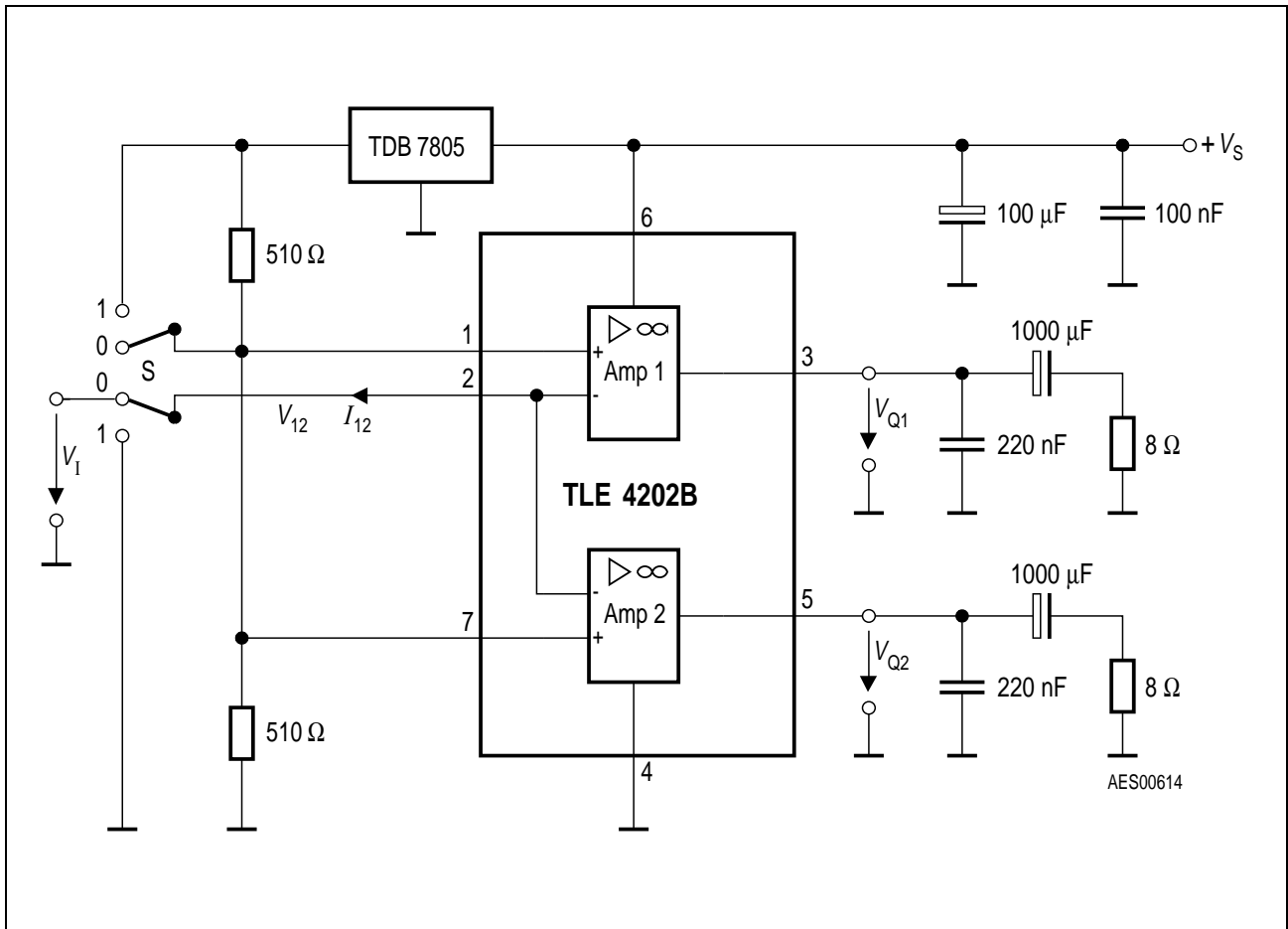


Figure 3 Test Circuit 1

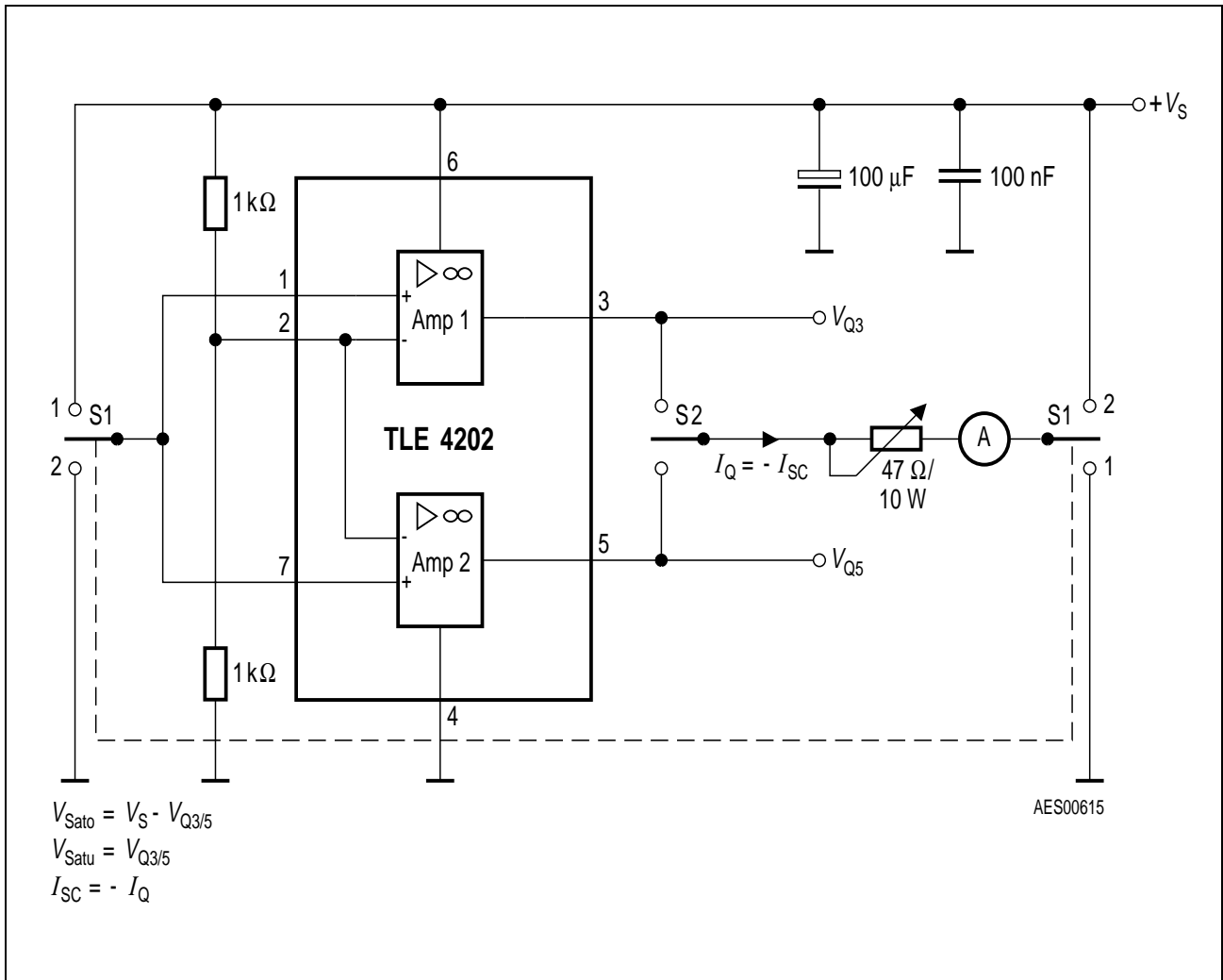


Figure 4 Test Circuit 2

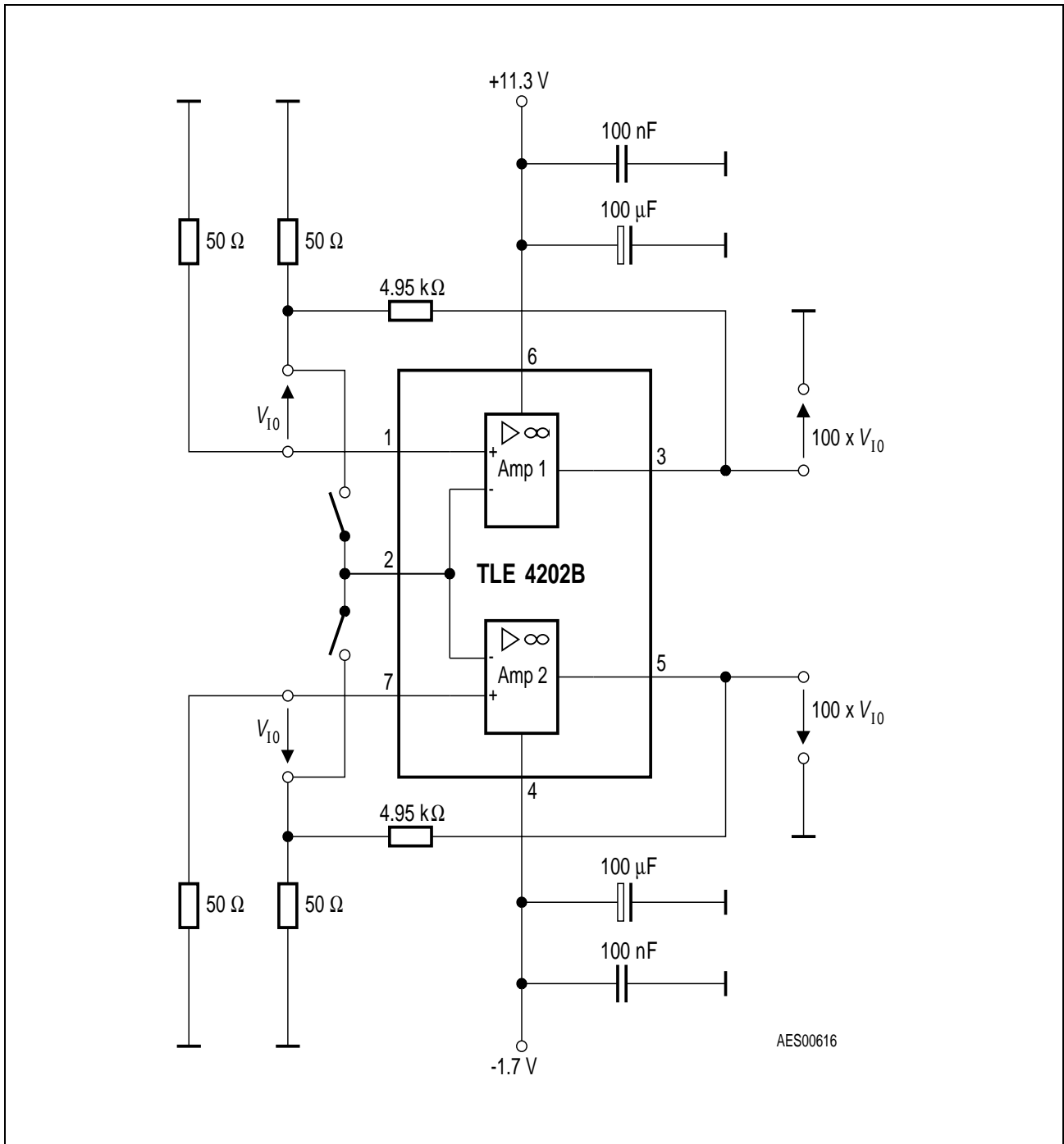


Figure 5 Test Circuit 3

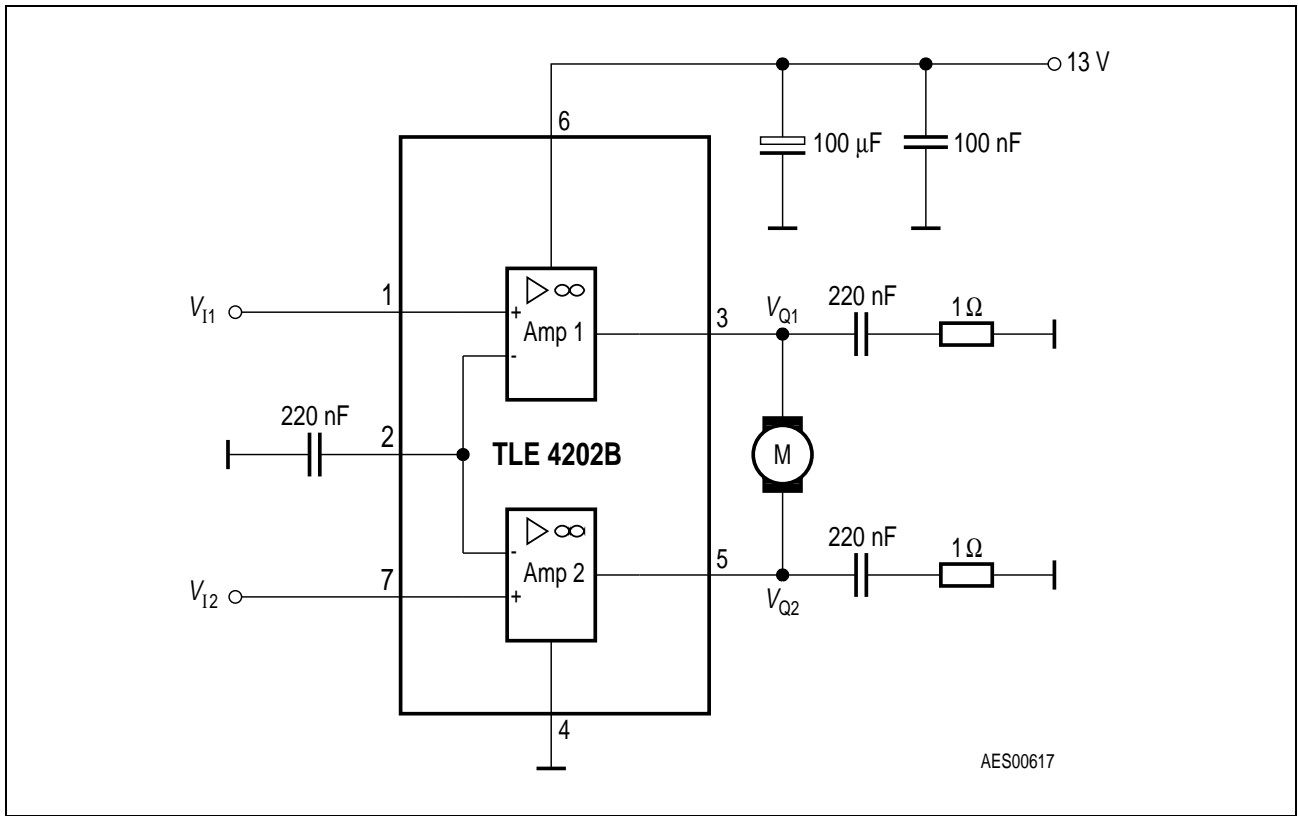


Figure 6 Application Circuit

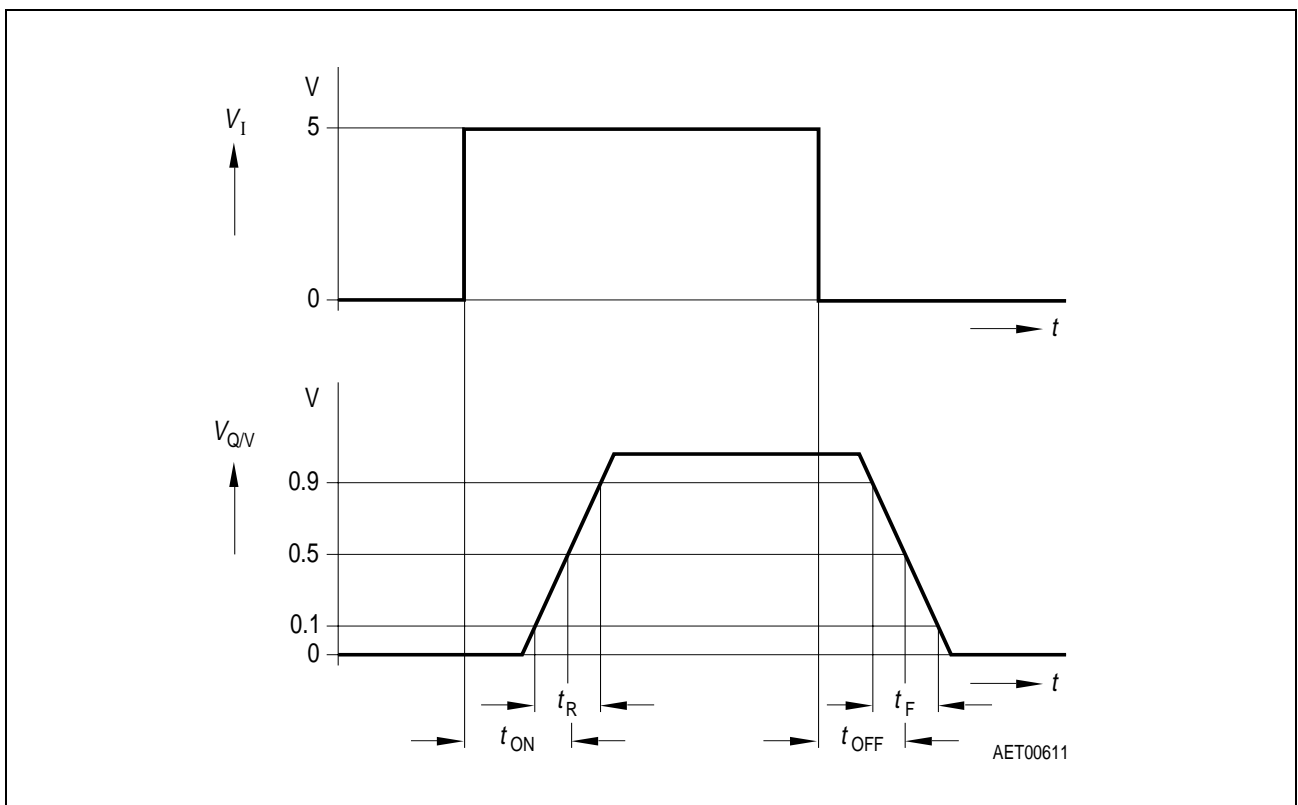
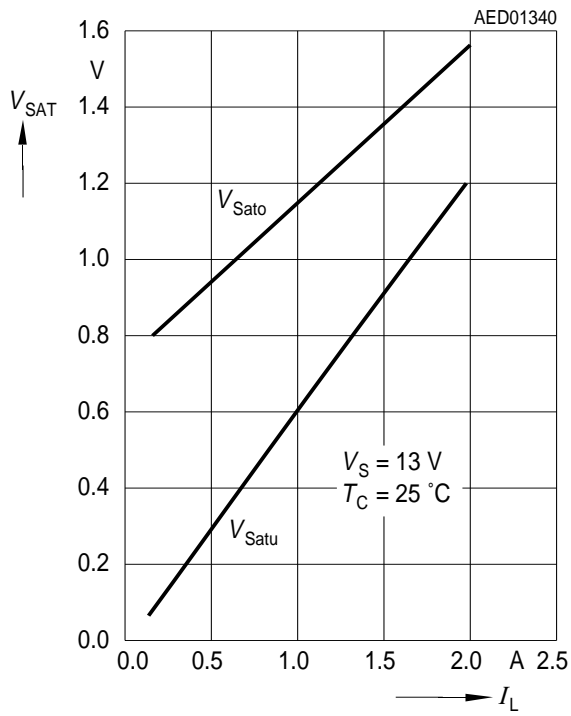
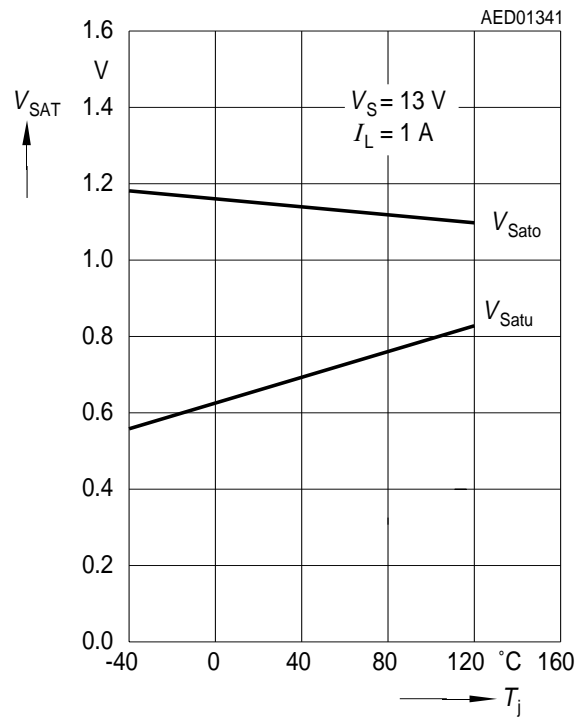


Figure 7 Diagrams

### Saturation Voltage versus Output Current



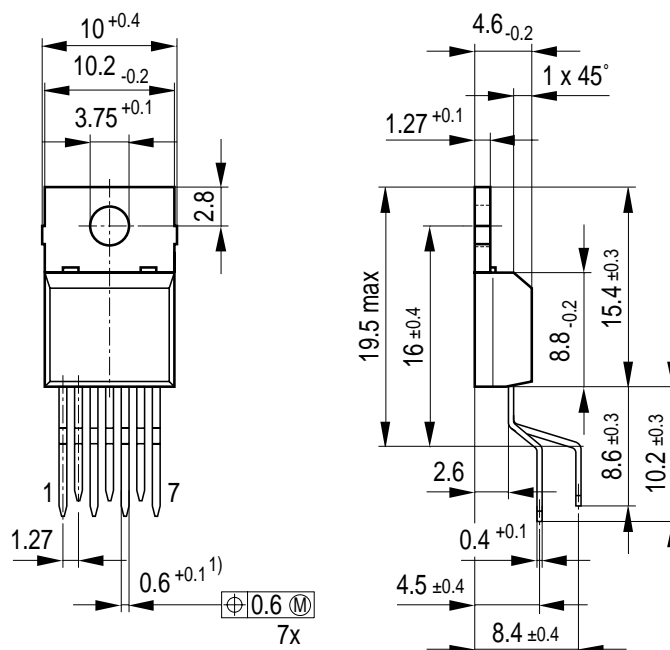
### Saturation Voltage versus Temperature



Package Outlines

**P-TO220-7-1**

(Plastic Transistor Single Outline)



1) 0.75<sup>-0.15</sup> at dam bar (max 1.8 from body)

1) 0.75<sup>-0.15</sup> im Dichtstegbereich (max 1.8 vom Körper)

GPT05108

**Sorts of Packing**

Package outlines for tubes, trays etc. are contained in our Data Book "Package Information".

Dimensions in mm