



# MX23L4100

## 4M-BIT MASK ROM (8/16 BIT OUTPUT)

### FEATURES

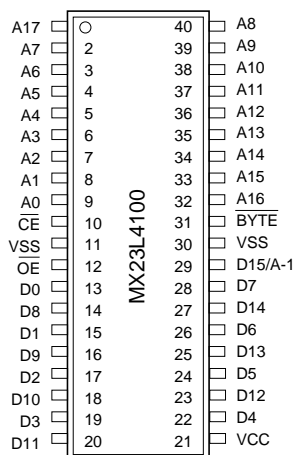
- Bit organization
  - 512K x 8 (byte mode)
  - 256K x 16 (word mode)
- Fast access time
  - Random access: 100ns
- Current
  - Operating: 30mA
  - Standby: 20uA
- Supply voltage
  - 3.3V±10%
- Package
  - 40 pin SOP (500 mil)
  - 40 pin PDIP (600 mil)

### ORDER INFORMATION

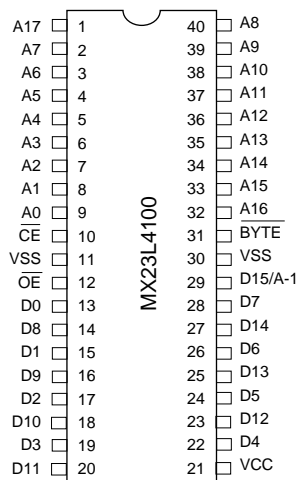
Part No.	Access Time	Package
MX23L4100MC-10	100ns	40 pin SOP
MX23L4100MC-12	120ns	40 pin SOP
MX23L4100MC-15	150ns	40 pin SOP
MX23L4100PC-10	100ns	40 pin PDIP
MX23L4100PC-12	120ns	40 pin PDIP
MX23L4100PC-15	150ns	40 pin PDIP

### PIN CONFIGURATION

#### 40 SOP



#### 40 PDIP

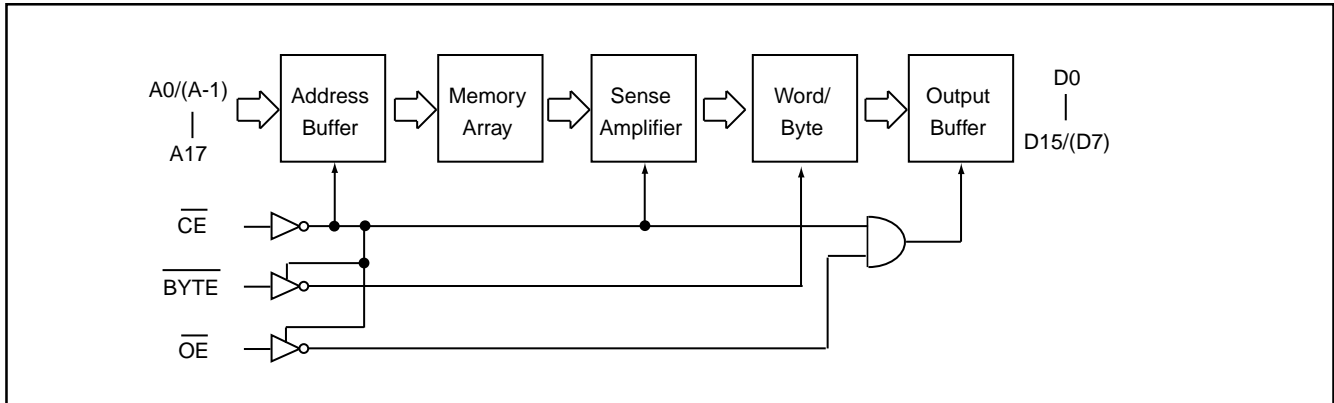


### PIN DESCRIPTION

Symbol	Pin Function
A0~A17	Address Inputs
D0~D14	Data Outputs
$\overline{CE}$	Chip Enable Input
$\overline{OE}$	Output Enable Input
Byte	Word/ Byte Mode Selection
VCC	Power Supply Pin
VSS	Ground Pin
NC	No Connection

### MODE SELECTION

$\overline{CE}$	$\overline{OE}$	Byte	D15/A-1	D0~D7	D8~D15	Mode	Power
H	X	X	X	High Z	High Z	-	Stand-by
L	H	X	X	High Z	High Z	-	Active
L	L	H	Output	D0~D7	D8~D15	Word	Active
L	L	L	Input	D0~D7	High Z	Byte	Active

**BLOCK DIAGRAM**

**ABSOLUTE MAXIMUM RATINGS**

Item	Symbol	Ratings
Voltage on any Pin Relative to VSS	VIN	-0.8V to VCC+2.0V (Note)
Ambient Operating Temperature	Topr	0°C to 70°C
Storage Temperature	Tstg	-65°C to 125°C

Note: Minimum DC voltage on input or I/O pins is -0.5V. During voltage transitions, inputs may undershoot VSS to -0.8V for periods of up to 20ns. Maximum DC voltage on input or I/O pins is VCC+0.5V. During voltage transitions, input may overshoot VCC to VCC+2.0V for periods of up to 20ns.

**DC CHARACTERISTICS** (Ta = 0°C ~ 70°C, VCC = 3.3V±10%)

Item	Symbol	MIN.	MAX.	Conditions
Output High Voltage	VOH	2.4V	-	IOH = -0.4mA
Output Low Voltage	VOL	-	0.4V	IOL = 1.6mA
Input High Voltage	VIH	2.2V	VCC+0.3V	
Input Low Voltage	VIL	-0.3V	0.8V	
Input Leakage Current	ILI	-	5uA	0V, VCC
Output Leakage Current	ILO	-	5uA	0V, VCC
Operating Current (CE toggle)	ICC1	-	30mA	tRC=100ns, all output open
Standby Current (TTL)	ISTB1	-	1mA	CE = VIH
Standby Current (CMOS)	ISTB2	-	20uA	CE > VCC - 0.2V
Input Capacitance	CIN	-	10pF	Ta = 25°C, f = 1MHZ
Output Capacitance	COUT	-	10pF	Ta = 25°C, f = 1MHZ

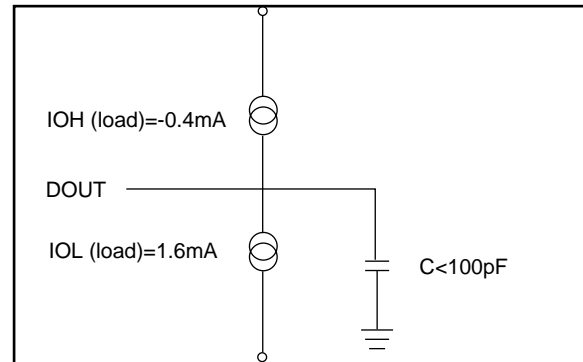
## AC CHARACTERISTICS (Ta = 0°C ~ 70°C, VCC = 3.3V±10%)

Item	Symbol	23L4100-10		23L4100-12		23L4100-15	
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.
Read Cycle Time	tRC	100ns	-	120ns	-	150ns	-
Address Access Time	tAA	-	100ns	-	120ns	-	150ns
Chip Enable Access Time	tACE	-	100ns	-	120ns	-	150ns
Output Enable Time	tOE	-	50ns	-	60ns	-	70ns
Output Hold After Address	tOH	-	0ns	-	0ns	-	0ns
Output High Z Delay	tHZ	-	20ns	-	20ns	-	20ns

Note: Output high-impedance delay (tHZ) is measured from OE or CE going high, and this parameter guaranteed by design over the full voltage and temperature operating range - not tested.

### AC Test Conditions

Input Pulse Levels	0.4V~2.4V
Input Rise and Fall Times	10ns
Input Timing Level	1.4V
Output Timing Level	1.4V
Output Load	See Figure



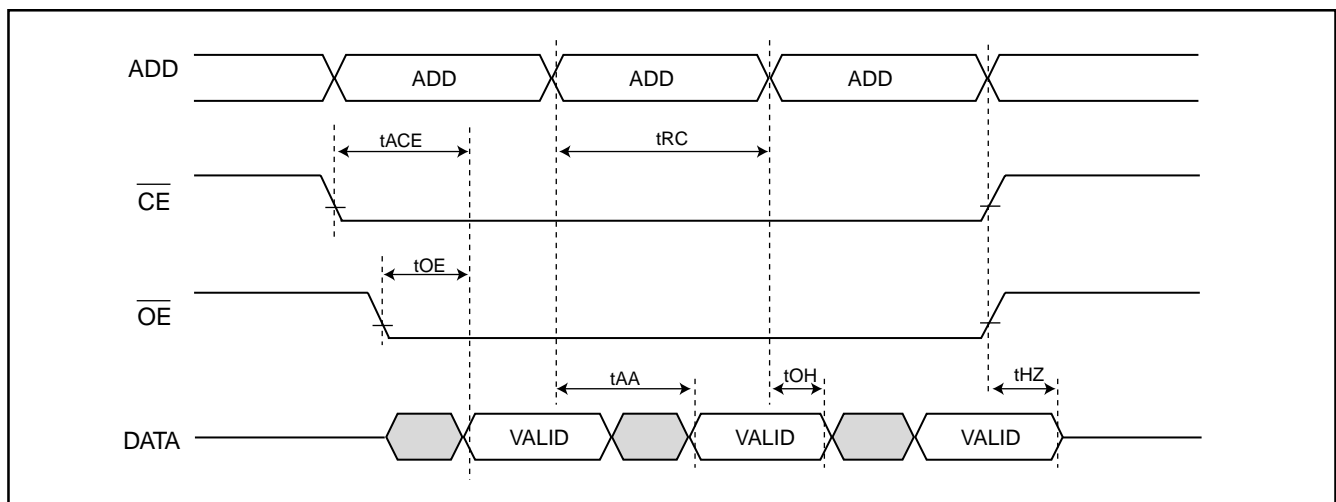
Note: No output loading is present in tester load board.

Active loading is used and under software programming control.

Output loading capacitance includes load board's and all stray capacitance.

### TIMING DIAGRAM

#### ACCESS TIMING



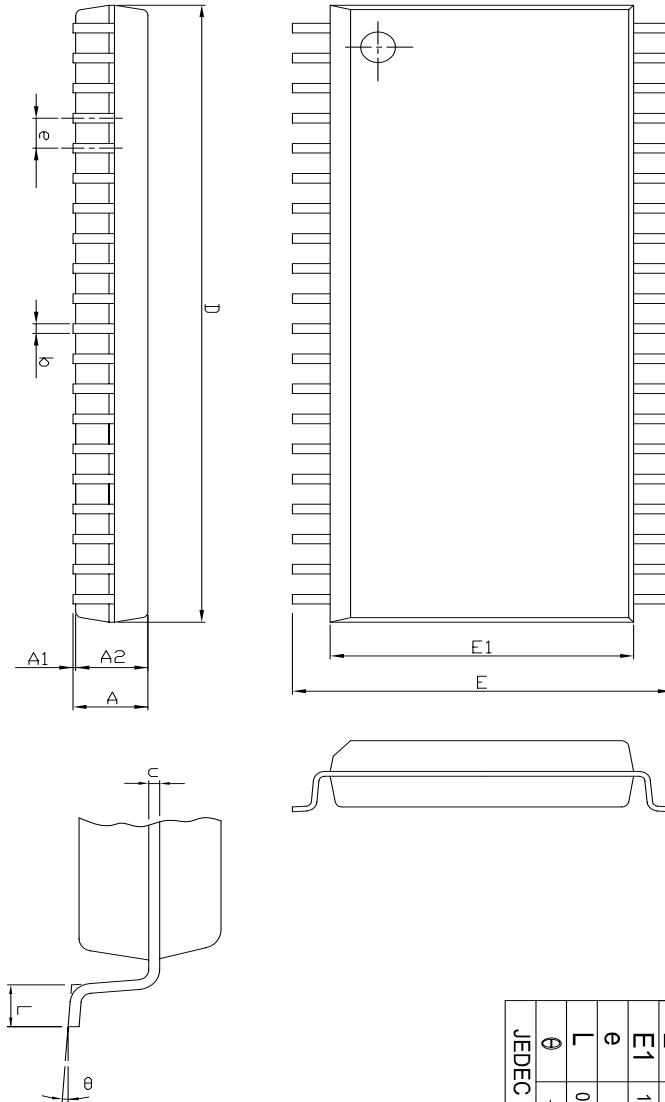
## PACKAGE INFORMATION

### 40-PIN PLASTIC DIP (600 mil)

UNIT SYMBOL	INCH(BASE)	MM(REF.)
A	0.155±0.008	3.937±0.203
A1	0.025±0.005	0.635±0.127
B	0.018 (REF.)	0.457 (REF.)
B1	0.050 (REF.)	1.270 (REF.)
C	0.010 (REF.)	0.254 (REF.)
D	2.05±0.005	52.07±0.127
E	0.600±0.005	15.240±0.127
E1	0.550±0.005	13.970±0.127
e1	0.100(REF.)	2.540 (REF.)
eA	0.650±0.030	16.510±0.762
L	0.13	3.30
Q1	0.0725±0.005	1.8415±0.127
S	0.075±0.005	1.0905±0.127

旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO.	
		61110-0202.4	
TITLE			
PACKAGE OUTLINE FOR			
PDP 40L (600 MIL)			
DRAWN	APPROVED	DATE	UNIT
C.L.Chang	Leo Lee	05-02-01	
TOLERANCE		REVISION	
X ±.	XX ±0.1	4	
.XXX±.002			

## 40-PIN PLASTIC SOP



Symbol	Dimension in mm (Base)			Dimension in inch (Ref.)		
	Min	Nom	Max	Min	Nom	Max
A	—	—	3.00	—	—	0.118
A1	0.10	—	—	0.004	—	—
A2	2.57	2.69	2.82	0.101	0.106	0.111
b	0.41REF			0.016 REF		
c	0.20 REF			0.008 REF		
D	25.93	26.06	26.19	1.021	1.026	1.031
E	13.87	14.12	14.38	0.546	0.556	0.566
E1	11.18	11.30	11.43	0.440	0.445	0.450
e	1.27 REF			0.050 REF		
L	0.58	0.79	0.99	0.023	0.031	0.039
θ	—	5°	—	—	5°	—

JEDEC

<b>MIIIC</b> 旺宏電子股份有限公司 Macronix International Co., Ltd.		DWG. NO. 6110-0206.1	
TITLE PACKAGE OUTLINE FOR SOP 40L (450 MIL)		TOLERANCE .X ±. .XX ±.01 .XXX±.002	
DRAWN C.L.Chiang	APPROVED Dennis Chang	DATE 05-03-01	UNIT INCH
REVISION 1		ROUGHNESS	



**REVISION HISTORY**

<b>REVISION</b>	<b>DESCRIPTION</b>	<b>PAGE</b>	<b>DATE</b>
1.3	AC CHARACTERISTICS tOH 10ns-->0ns	P3	FEB/01/1999
1.4	Modify Package Information	P4~5	JUL/16/2001



**MX23L4100**

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