

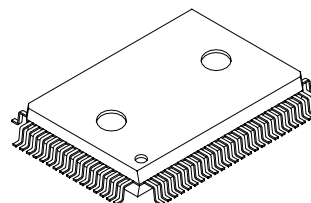
CMOS 8-bit Single Chip Microcomputer

Description

The CXP84120/84124 is a CMOS 8-bit single chip micro-computer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, remote control reception circuit and other servo systems besides the basic configurations of 8-bit CPU, ROM, RAM, and I/O port.

The CXP84120/84124 also provides a power-on reset function and a sleep/stop function that enables lower power consumption.

80 pin QFP (Plastic)



Features

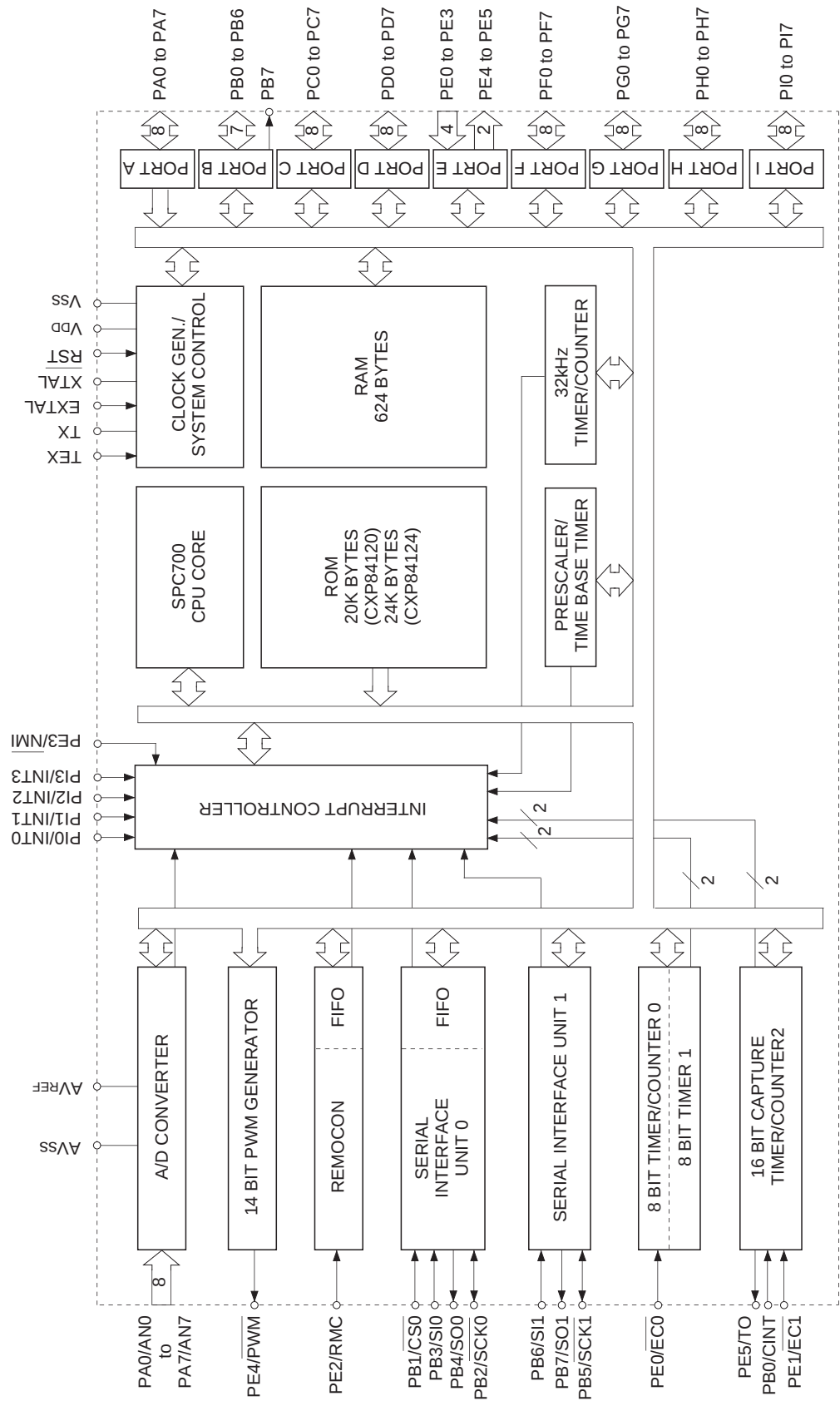
- Wide-range instruction system (213 instructions) to cover various types of data
 - 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle
 - 400ns at 10MHz operation
 - 122μs at 32kHz operation
- Incorporated ROM capacity
 - 20K bytes (CXP84120)
 - 24K bytes (CXP84124)
- Incorporated RAM capacity
 - 624 bytes
- Peripheral functions
 - A/D converter
 - 8 bits, 8 channels, successive approximation method (Conversion time of 32μs/10MHz)
 - Serial interface
 - SIO with 8-bit, 8-stage FIFO incorporated for data use (Auto transfer for 1 to 8 bytes), 1 channel
 - 8-bit standard SIO, 1 channel
 - Timer
 - 8-bit timer
 - 8-bit timer/counter
 - 19-bit time base timer
 - 16-bit capture timer/counter
 - 32kHz timer/counter
 - Remote control reception circuit
 - Incorporated noise elimination circuit
 - Incorporated 8-bit, 6-stage FIFO for measurement data
 - PWM output
 - 14 bits, 1 channel
- Interruption
 - 14 factors, 15 vectors, multi-interruption possible
- Standby mode
 - Sleep/stop
- Package
 - 80-pin plastic QFP
- Piggyback/evaluation chip
 - CXP84100 80-pin ceramic QFP

Structure

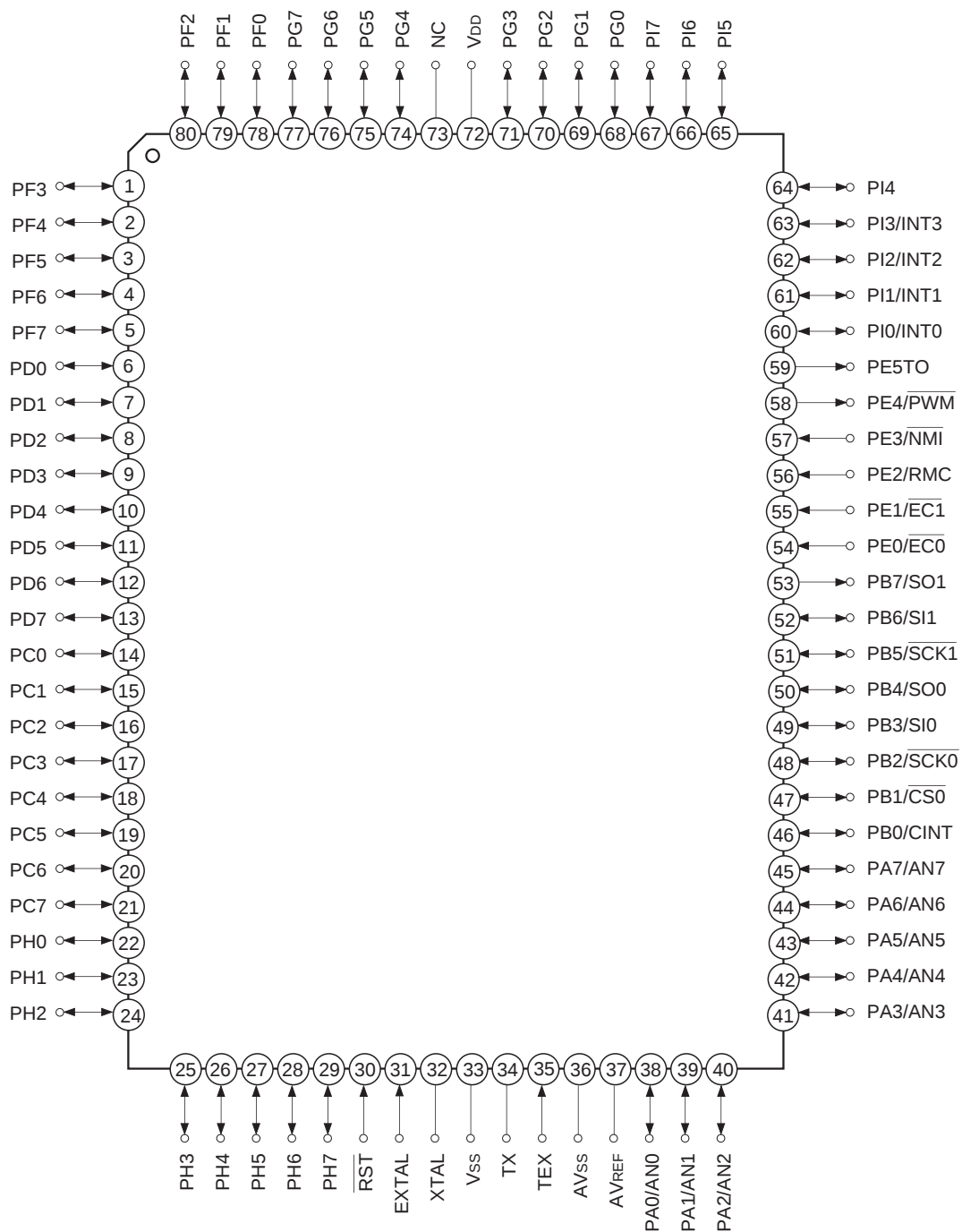
Silicon gate CMOS IC

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Block Diagram



Pin Assignment (Top View)



Note) NC (Pin 73) must be connected to V_{DD}.

Pin Description

Symbol	I/O	Description	
PA0/AN0 to PA7/AN7	I/O/Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bit. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Analog inputs to A/D converter. (8 pins)
PB0/CINT	I/O/Input	(Port B) 7-bit I/O port in which I/O can be set in a unit of single bit. Also, an uppermost bit (PB7) exclusively for output. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External capture input to 16-bit timer/counter.
PB1/ $\overline{\text{CS0}}$	I/O/Input		Chip select input for serial interface (CH0).
PB2/ $\overline{\text{SCK0}}$	I/O/I/O		Serial clock I/O (CH0).
PB3/SI0	I/O/Input		Serial data input (CH0).
PB4/SO0	I/O/Output		Serial data output (CH0).
PB5/ $\overline{\text{SCK1}}$	I/O/I/O		Serial clock I/O (CH1).
PB6/SI1	I/O/Input		Serial data input (CH1).
PB7/SO1	Output/Output		Serial data output (CH1).
PC0 to PC7	I/O	(Port C) 8-bit I/O port. I/O can be set in a unit of single bit. Capable of driving 12mA sink current. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PD0 to PD7	I/O	(Port D) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PE0/ $\overline{\text{EC0}}$	Input/Input	(Port E) 6-bit port. Lower 4 bits are for inputs; upper 2 bits are for outputs. (6 pins)	External event inputs for timer/counter. (2 pins)
PE1/ $\overline{\text{EC1}}$	Input/Input		
PE2/RMC	Input/Input		Remote control reception circuit input.
PE3/ $\overline{\text{NMI}}$	Input/Input		Non-maskable interruption request input.
PE4/ $\overline{\text{PWM}}$	Output/Output		14-bit PWM output.
PE5/TO/ADJ	Output/Output/ Output		Rectangular wave output for 16-bit timer/counter. Output for 32kHz oscillation frequency division.
PF0 to PF7	I/O	(Port F) 8-bit I/O port. I/O can be set in a unit of single bit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	

Symbol	I/O	Description	
PG0 to PG7	I/O	(Port G) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PH0 to PH7	I/O	(Port H) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	
PI0/INT0 to PI3/INT3	I/O/Input	(Port I) 8-bit I/O ports. I/O can be set in a unit of single bit. Incorporation of pull-up resistor can be set through the software in a unit of 4 bits. (8 pins)	External interruption request inputs.
PI4 to PI7	I/O		
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock generation circuit. Connect a 32kHz crystal oscillator between TEX and TX. For usage as event input, connect clock oscillation source to TEX, and open TX.	
TX	Output		
$\overline{\text{RST}}$	Input	Low-level active, system reset.	
NC		NC. Under normal operating conditions, connect to V _{DD} .	
AV _{REF}	Input	Reference voltage input for A/D converter.	
AV _{SS}		A/D converter GND.	
V _{DD}		Positive power supply.	
V _{SS}		GND	

Input/Output Circuit Formats for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A Pull-up resistance "0" when reset Port A data Port A direction "0" when reset Data bus RD (Port A) Port A input selection "0" when reset Input multiplexer A/D converter * Pull-up transistors approx. 10kΩ	Hi-Z
PB0/CINT PB1/CS0 PB3/SI0 PB6/SI1 4 pins	Port B Pull-up resistance "0" when reset Port B data Port B direction "0" when reset Data bus RD (Port B) CINT CS0 SI0 SI1 Schmitt input * Pull-up transistors approx. 10kΩ	Hi-Z
PB2/SCK0 PB5/SCK1 2 pins	Port B Pull-up resistance "0" when reset SCK OUT Output enable Port B output selection "0" when reset Port B data Port B direction "0" when reset Data bus RD (Port B) Schmitt input SCK in * Pull-up transistors approx. 10kΩ	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 1 pin	Port B Pull-up resistance SO Output enable Port B output selection "0" when reset Port B data Port B direction "0" when reset Data bus RD (Port B) * Pull-up transistors approx. 10kΩ	Hi-Z
PB7/SO1 1 pin	Port B SO Output enable Port B output selection "1" when reset Port B data Data bus RD (Port B) * Pull-up transistors approx. 10kΩ	High level
PC0 to PC7 8 pins	Port C Pull-up resistance "0" when reset Port C data Port C direction "0" when reset Data bus RD (Port C) *1 Large current drive of 12mA possible *2 Pull-up transistors approx. 10kΩ	Hi-Z
PE0/EC0 PE1/EC1 PE2/RMC PE3/NMI 4 pins	Port E Schmitt input IP EC0 EC1 RMC/NMI Data bus RD (Port E)	Hi-Z

Pin	Circuit format	When reset
PE4/PWM 1 pin		High level
PE5/TO/ADJ 1 pin	* ADJ signals are frequency division outputs for 32kHz oscillation frequency adjustment. ADJ2K provides usage as buzzer output.	High level
PD0 to PD7 PF0 to PF7 PG0 to PG7 PH0 to PH7 PI4 to PI7 36 pins	* Pull-up transistors approx. 10kΩ	Hi-Z

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Absolute Maximum Ratings

(V_{SS} = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V _{DD}	−0.3 to +7.0	V	
	AV _{SS}	−0.3 to +0.3	V	
Input voltage	V _{IN}	−0.3 to +7.0* ¹	V	
Output voltage	V _{OUT}	−0.3 to +7.0* ¹	V	
High level output current	I _{OH}	−5	mA	Output per pin
High level total output current	ΣI _{OH}	−50	mA	Total for all output pins
Low level output current	I _{OL}	15	mA	Value per pin, excluding large current outputs
	I _{OLC}	20	mA	Value per pin* ² for large current outputs
Low level total output current	ΣI _{OL}	100	mA	Total for all output pins
Operating temperature	T _{opr}	−20 to +75	°C	
Storage temperature	T _{stg}	−55 to +150	°C	
Allowable power dissipation	P _D	600	mW	

*¹ V_{IN} and V_{OUT} must not exceed V_{DD} + 0.3V.*² The large current drive transistor is the N-ch transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions

(V_{SS} = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V _{DD}	4.5	5.5	V	High-speed mode guaranteed operation range* ¹
		3.5	5.5		Low-speed mode guaranteed operation range* ¹
		2.7	5.5		Guaranteed operation range with TEX clock
		2.5	5.5		Guaranteed data hold range during stop
High level input voltage	V _{IH}	0.7V _{DD}	V _{DD}	V	* ²
	V _{IHS}	0.8V _{DD}	V _{DD}	V	Hysteresis input* ³
	V _{IHEX}	V _{DD} − 0.4	V _{DD} + 0.3	V	EXTAL* ⁴
Low level input voltage	V _{IL}	0	0.3V _{DD}	V	* ²
	V _{ILS}	0	0.2V _{DD}	V	Hysteresis input* ³
	V _{ILEX}	−0.3	0.4	V	EXTAL* ⁴
Operating temperature	T _{opr}	−20	+75	°C	

*¹ High-speed mode is 1/2 frequency division clock selection; low-speed mode is 1/16 frequency division clock selection.*² Value for each pin of normal input ports (PA, PB3, PB4, PB6, PC, PD, PF to PH, PI4 to PI7).*³ Value of the following pins: RST, CINT, CS0, SCK0, SCK1, EC0, EC1, RMC, NMI, INT0, INT1, INT2, INT3.*⁴ Specifies only during external clock input.

Electrical Characteristics

DC Characteristics

(Ta = -20 to +75°C, Vss = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output voltage	V _{OH}	PA to PD, PE4, PE5, PF to PI	V _{DD} = 4.5V, I _{OH} = −0.5mA	4.0			V
			V _{DD} = 4.5V, I _{OH} = −1.2mA	3.5			V
Low level output voltage	V _{OL}		V _{DD} = 4.5V, I _{OL} = 1.8mA			0.4	V
			V _{DD} = 4.5V, I _{OL} = 3.6mA			0.6	V
		PC	V _{DD} = 4.5V, I _{OL} = 12.0mA			1.5	V
Input current	I _{IHE}	EXTAL	V _{DD} = 5.5V, V _{IH} = 5.5V	0.5		40	μA
	I _{IIE}		V _{DD} = 5.5V, V _{IL} = 0.4V	−0.5		−40	μA
	I _{IHT}	TEX	V _{DD} = 5.5V, V _{IH} = 5.5V	0.1		10	μA
	I _{ILT}		V _{DD} = 5.5V, V _{IL} = 0.4V	−0.1		−10	μA
	I _{ILR}	$\overline{\text{RST}}^{*1}$		−1.5		−400	μA
	I _{IL}	PA to PD ^{*2} , PF to PI ^{*2}				−2.0	mA
			V _{DD} = 4.5V, V _{IL} = 4.0V	−10			μA
I/O leakage current	I _{IZ}	$\overline{\text{PE0}}$ to PE3, $\overline{\text{RST}}^{*1}$	V _{DD} = 5.5V, V _I = 0, 5.5V			±10	μA
Power supply current ^{*3}	I _{DD1}	V _{DD}	High-speed mode operation (1/2 frequency division clock)		18	40	mA
			V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)				
	I _{DD2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		35	100	μA
	I _{DDS1}		Sleep mode		1.1	8	mA
			V _{DD} = 5.5V, 10MHz crystal oscillation (C ₁ = C ₂ = 15pF)				
	I _{DDS2}		V _{DD} = 3V, 32kHz crystal oscillation (C ₁ = C ₂ = 47pF)		9	30	μA
	I _{DDS3}		Stop mode				10
V _{DD} = 5.5V, termination of 10MHz and 32kHz crystal oscillation							
Input capacity	C _{IN}	Pins other than PB7, PE4, PE5, AV _{REF} , AV _{SS} , V _{DD} , V _{SS}	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1 $\overline{\text{RST}}$ specifies the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*2 Pins PA to PD, and PF to PI specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected. (Excludes output PB7)

*3 When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f _c	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t _{XL} , t _{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	t _{CR} , t _{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive			200	ns
Event count input clock pulse width	t _{EH} , t _{EL}	$\overline{\text{EC0}}$ EC1	Fig. 3	t _{sys} + 50* ¹			ns
Event count input clock rise time, fall time	t _{ER} , t _{EF}	$\overline{\text{EC0}}$ EC1	Fig. 3			20	ms
System clock frequency	f _c	TEX TX	VDD = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input clock input pulse width	t _{TL} , t _{TH}	TEX	Fig. 3	10			μs
Event count input clock rise time, fall time	t _{TR} , t _{TF}	TEX	Fig. 3			20	ms

*¹ t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t_{sys} [ns] = 2000/f_c (upper two bits = "00"), 4000/f_c (upper two bits = "01"), 16000/f_c (upper two bits = "11")

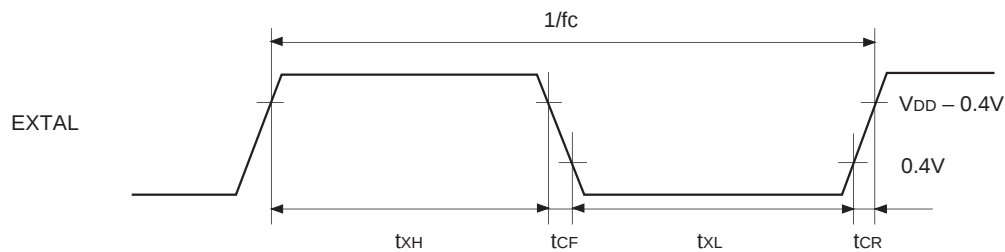


Fig. 1. Clock timing

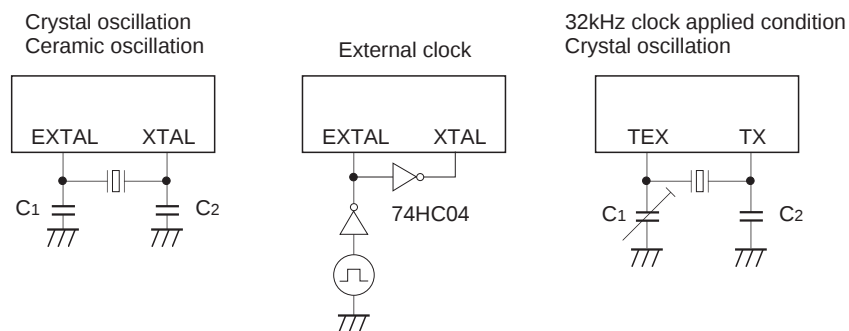


Fig. 2. Clock applied conditions

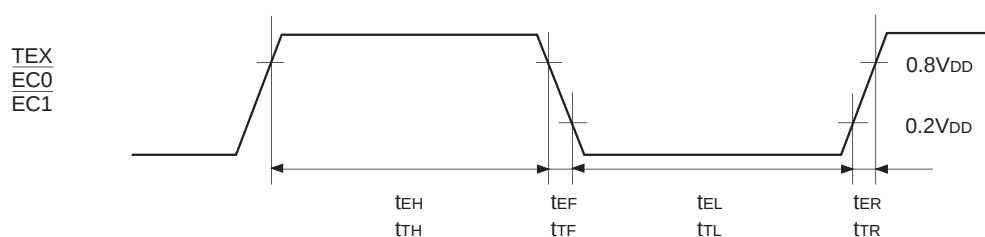


Fig. 3. Event count clock timing

(2) Serial transfer (CH0)

(Ta = -20 to +75°C, VDD = 4.5 to 5.5V, VSS = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{CS0}} \downarrow \rightarrow \overline{\text{SCK0}}$ delay time	t_{DCSK}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \overline{\text{SCK0}}$ float delay time	t_{DCSKF}	$\overline{\text{SCK0}}$	Chip select transfer mode ($\overline{\text{SCK0}}$ = output mode)		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{DCSO}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}} \uparrow \rightarrow \text{SO0}$ float delay time	t_{DCSOF}	SO0	Chip select transfer mode		$t_{\text{sys}} + 200$	ns
$\overline{\text{CS0}}$ High level width	t_{WHCS}	$\overline{\text{CS0}}$	Chip select transfer mode	$t_{\text{sys}} + 200$		ns
$\overline{\text{SCK0}}$ cycle time	t_{KCY}	$\overline{\text{SCK0}}$	Input mode	$2t_{\text{sys}} + 200$		ns
			Output mode	$16000/f_c$		ns
$\overline{\text{SCK0}}$ High, Low level width	$t_{\text{KH}},$ t_{KL}	$\overline{\text{SCK0}}$	Input mode	$t_{\text{sys}} + 100$		ns
			Output mode	$8000/f_c - 50$		ns
SI0 input setup time (for $\overline{\text{SCK0}} \uparrow$)	t_{SIK}	SI0	$\overline{\text{SCK0}}$ input mode	100		ns
			$\overline{\text{SCK0}}$ output mode	200		ns
SI0 input hold time (for $\overline{\text{SCK0}} \uparrow$)	t_{KSI}	SI0	$\overline{\text{SCK0}}$ input mode	$t_{\text{sys}} + 200$		ns
			$\overline{\text{SCK0}}$ output mode	100		ns
$\overline{\text{SCK0}} \downarrow \rightarrow \text{SO0}$ delay time	t_{KSO}	SO0	$\overline{\text{SCK0}}$ input mode		$t_{\text{sys}} + 200$	ns
			$\overline{\text{SCK0}}$ output mode		100	ns

Note 1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t_{sys} [ns] = 2000/ f_c (upper two bits = "00"), 4000/ f_c (upper two bits = "01"), 16000/ f_c (upper two bits = "11")

Note 2) The load condition for the $\overline{\text{SCK0}}$ output mode, SO0 output delay time is 50pF + 1TTL.

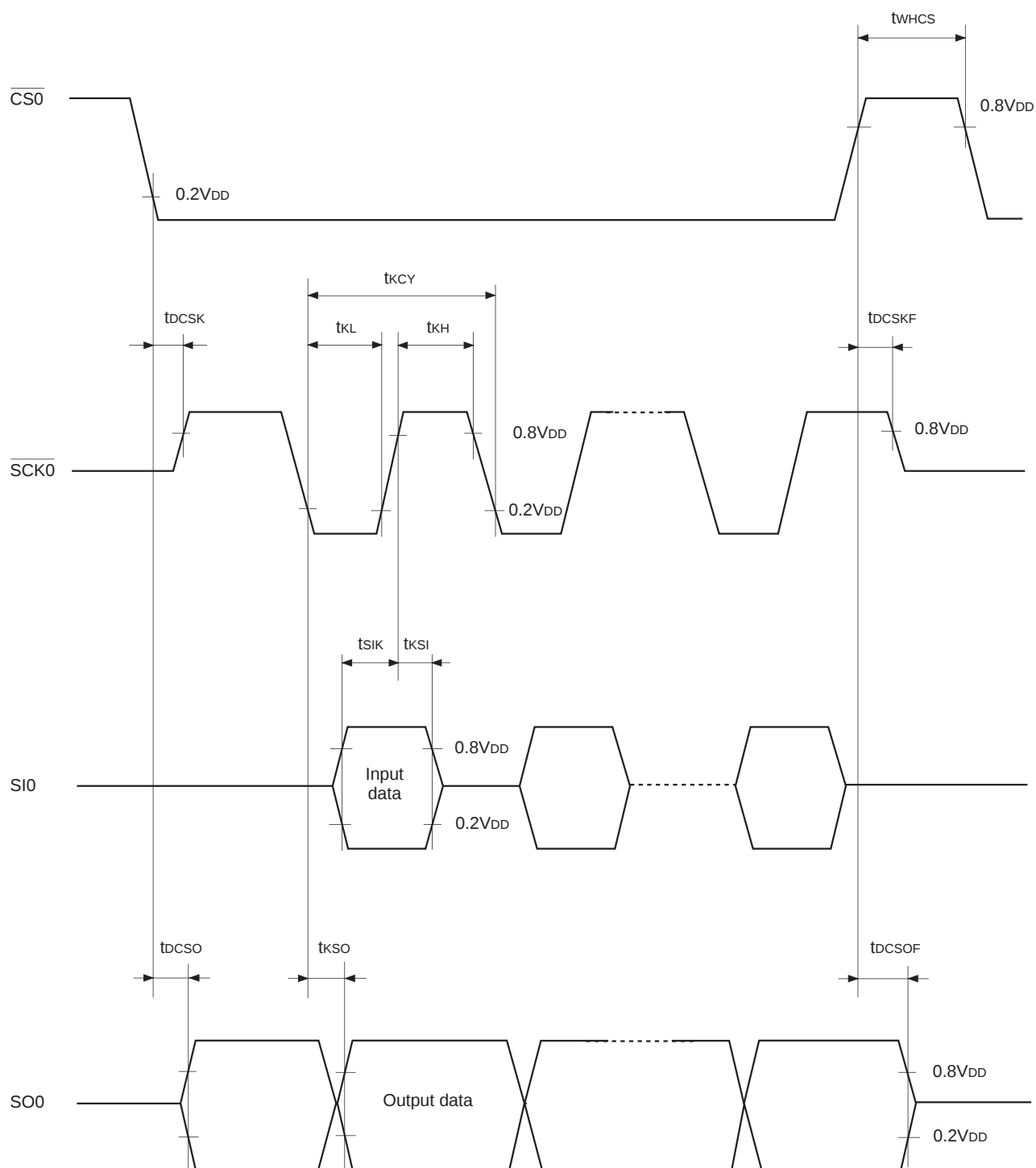
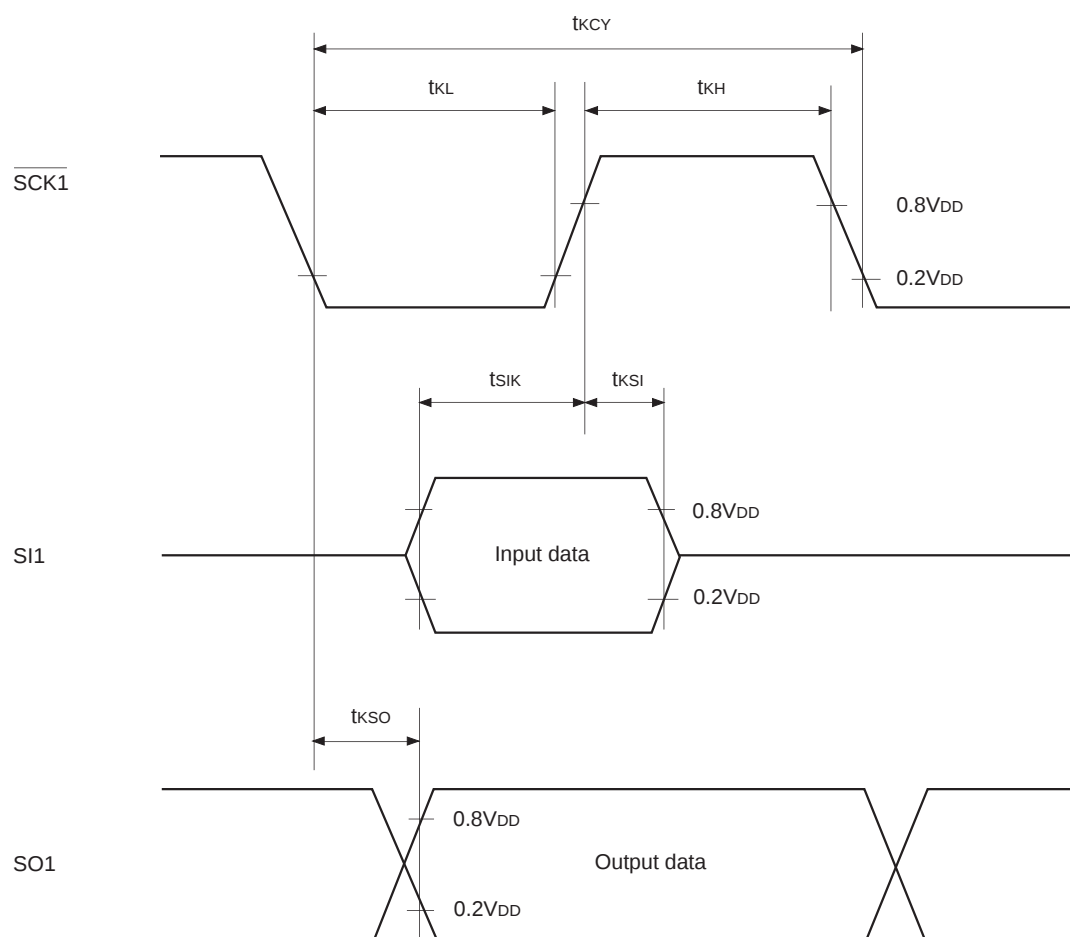


Fig. 4. Serial transfer CH0 timing

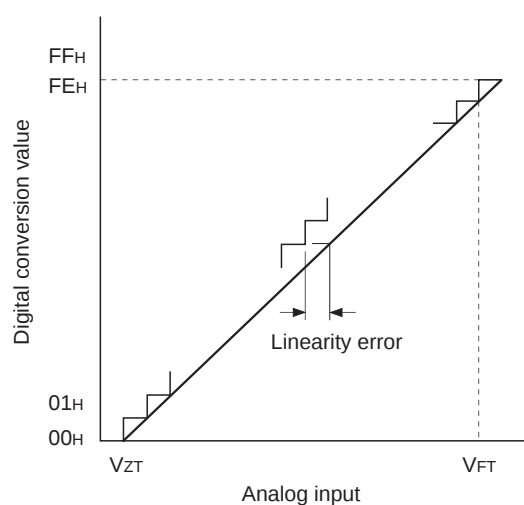
Serial transfer (CH1)(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, V_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{\text{SCK1}}$ cycle time	t_{KCY}	$\overline{\text{SCK1}}$	Input mode	1000		ns
			Output mode	16000/fc		ns
$\overline{\text{SCK1}}$ High, Low level width	$t_{\text{KH}},$ t_{KL}	$\overline{\text{SCK1}}$	Input mode	400		ns
			Output mode	8000/fc - 50		ns
SI1 input setup time (for $\overline{\text{SCK1}} \uparrow$)	t_{SIK}	SI1	$\overline{\text{SCK1}}$ input mode	100		ns
			$\overline{\text{SCK1}}$ output mode	200		ns
SI1 input hold time (for $\overline{\text{SCK1}} \uparrow$)	t_{KSI}	SI1	$\overline{\text{SCK1}}$ input mode	200		ns
			$\overline{\text{SCK1}}$ output mode	100		ns
$\overline{\text{SCK1}} \downarrow \rightarrow \text{SO1}$ delay time	t_{KSO}	SO1	$\overline{\text{SCK1}}$ input mode		200	ns
			$\overline{\text{SCK1}}$ output mode		100	ns

Note) The load condition for the $\overline{\text{SCK1}}$ output mode, SO1 output delay time is 50pF + 1TTL.**Fig. 5. Serial transfer CH1 timing**

(3) A/D converter characteristics(Ta = -20 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to AV_{DD}, V_{SS} = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V _{DD} = 5.0V V _{SS} = AV _{SS} = 0V			±5	LSB
Zero transition voltage	V _{ZT} *1			-10	70	150	mV
Full-scale transition voltage	V _{FT} *2			4930	5050	5120	mV
Conversion time	t _{CONV}			160/f _{ADC} *3			μs
Sampling time	t _{SAMP}			12/f _{ADC} *3			μs
Reference input voltage	V _{REF}	AV _{REF}		V _{DD} - 0.5		V _{DD}	V
Analog input voltage	V _{IAN}	AN0 to AN7		0		AV _{REF}	V
AV _{REF} current	I _{REF}	AV _{REF}	Operation mode		0.6	1.0	mA
	I _{REFS}		Sleep mode Stop mode 32kHz operation mode			10	μA



*1 V_{ZT} : Value at which the digital conversion value changes from 00_H to 01_H and vice versa.

*2 V_{FT} : Value at which the digital conversion value changes from FE_H to FF_H and vice versa.

*3 f_{ADC} indicates the below values due to ADC operation clock selection.

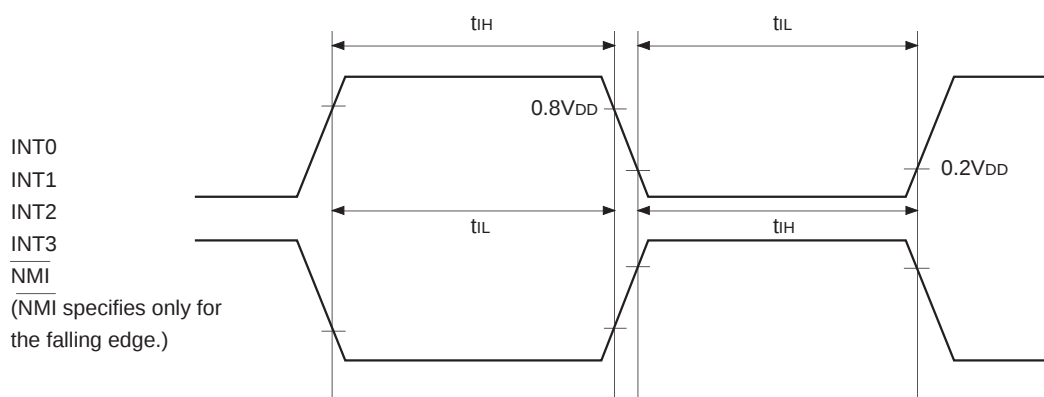
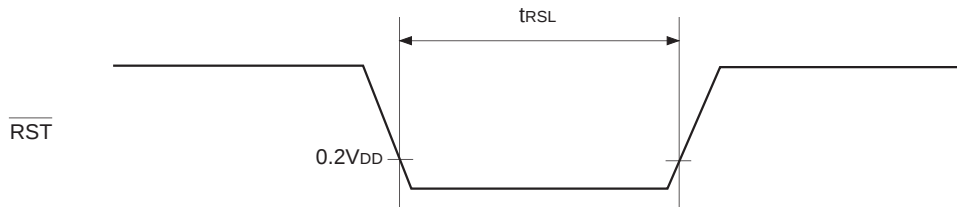
During PS2 selection, f_{ADC} = f_c/2

During PS1 selection, f_{ADC} = f_c

Fig. 6. Definition of A/D converter terms

(4) Interruption, reset input ($T_a = -20$ to $+75^\circ\text{C}$, $V_{DD} = 4.5$ to 5.5V , $V_{SS} = 0\text{V}$ reference)

Item	Symbol	Pins	Condition	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 INT3 $\overline{\text{NMI}}$ PJ0 to PJ7		1		μs
Reset input Low level width	t_{RSL}	$\overline{\text{RST}}$		$8/f_c$		μs

**Fig 7. Interruption input timing****Fig. 8. $\overline{\text{RST}}$ input timing**

Appendix

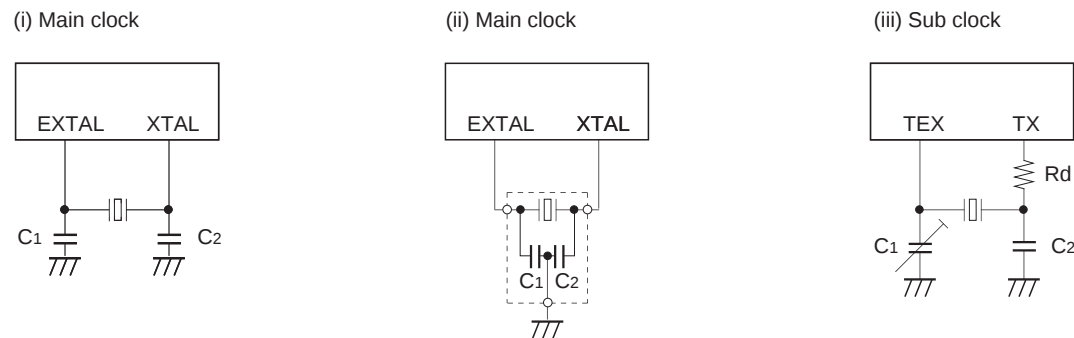


Fig. 9. SPC700 series recommended oscillation circuit

Manufacturer	Model	fc (MHz)	C ₁ (pF)	C ₂ (pF)	Circuit example	
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	(i)	
	CSA8.00MG	8.00				
	CSA10.0MT	10.00				
	CST4.19MGW*	4.19			(ii)	
	CST8.00MTW*	8.00				
	CST10.00MTW*	10.00				
RIVER ELETEC CORPORATION	HC-49/U03	4.19	15	15	(i)	
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27		(i)
		8.00				
		10.00				

Those marked with an asterisk (*) signify types with built-in ground capacitance (C1, C2).

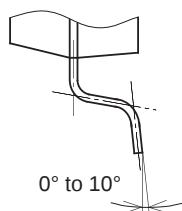
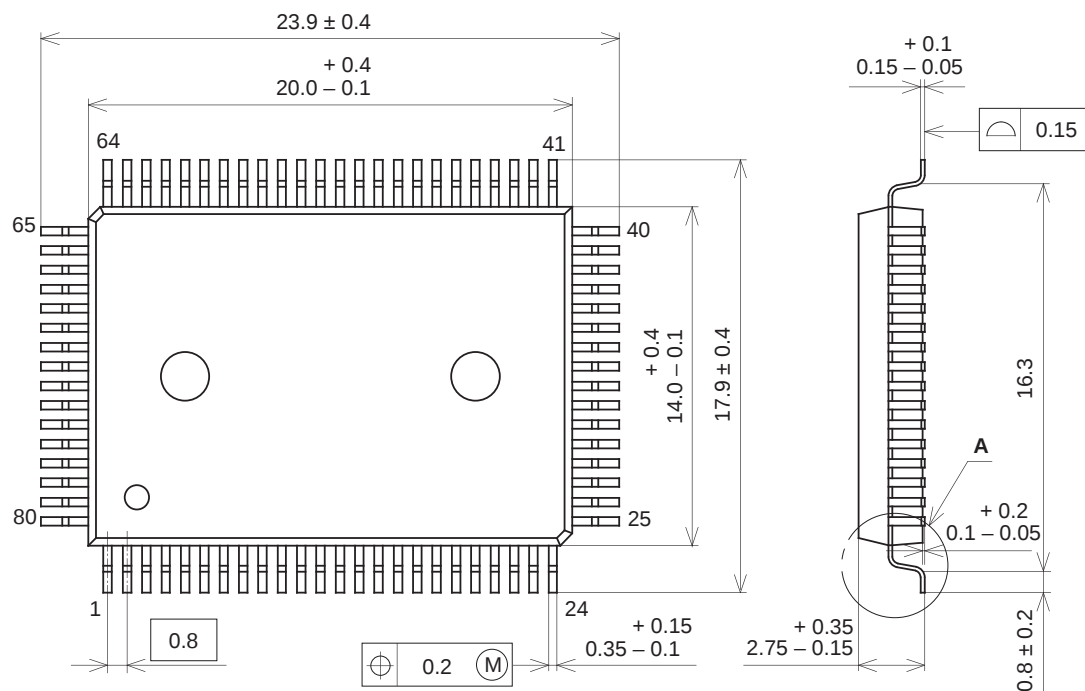
Mask option table

Item	Content	
Reset pin pull-up resistance	Non-existent	Existent

Package Outline

Unit: mm

80PIN QFP (PLASTIC)



DETAIL A

PACKAGE STRUCTURE

SONY CODE	QFP-80P-L01
EIAJ CODE	QFP080-P-1420
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.6g