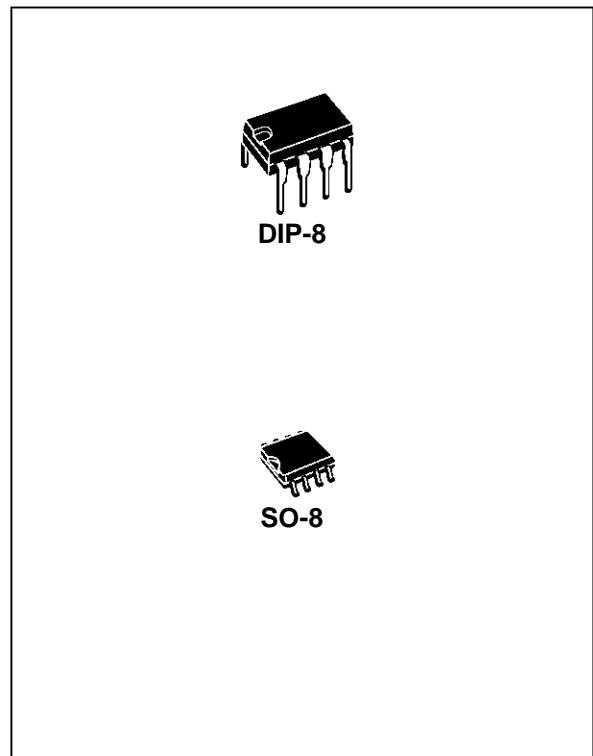


**DC-DC CONVERTER FROM 5V TO 12V, 0.03A  
FOR FLASH MEMORY PROGRAMMING SUPPLY**

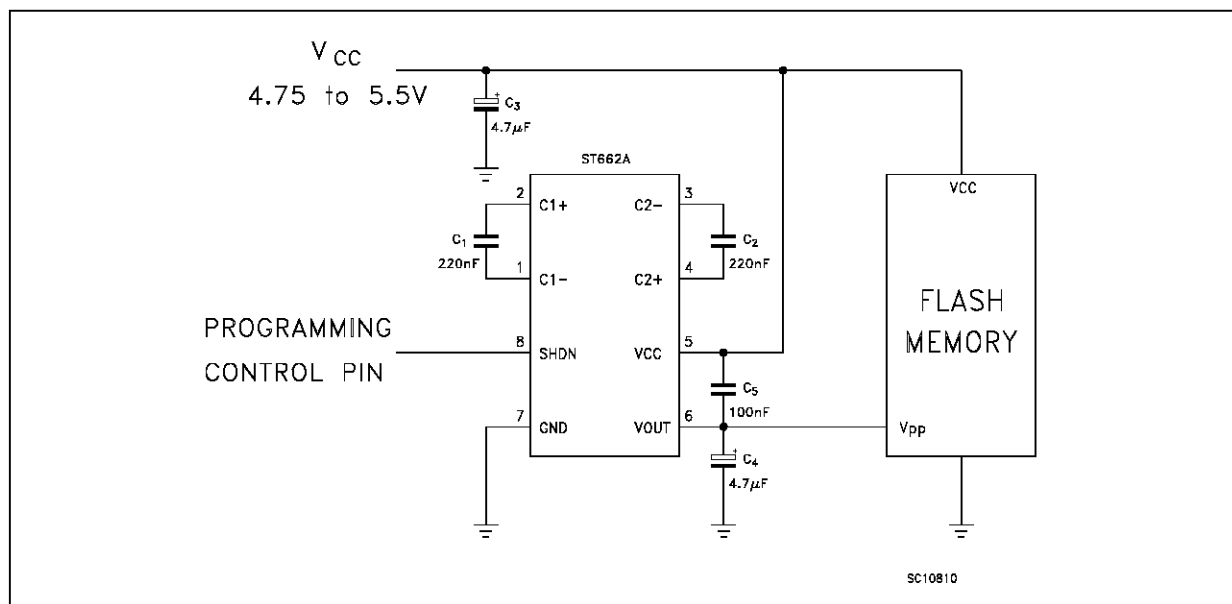
- OUTPUT VOLTAGE:  $12V \pm 5\%$
- SUPPLY VOLTAGE RANGE: 4.5V TO 5.5V
- GUARANTEED OUTPUT CURRENT UP TO 30mA
- VERY LOW QUIESCENT CURRENT:  $100\mu A$
- LOGIC CONTROLLED ELECTRONIC SHUTDOWN:  $1\mu A$
- JUST CAPACITORS NEEDED (NO INDUCTOR)

**DESCRIPTION**

The ST662A is a regulated charge pump DC-DC converter. It provides  $12V \pm 5\%$  output voltage to program byte-wide flash memory, and can supply 30mA output current from input as low as 4.75V  
A logic controlled shut down pin that interfaces directly with microprocessor reduces the supply current to only  $1\mu A$



**TYPICAL APPLICATION CIRCUIT**



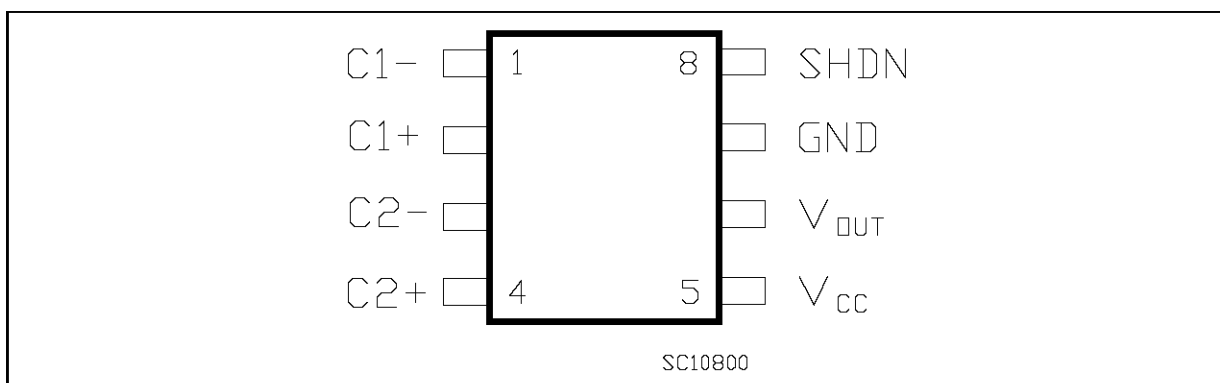
# ST662A

## ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
$V_{CC}$	DC Input Voltage to GND	-0.3 to 6	V
SHDN	Shutdown Voltage	-0.3 to $V_{CC}+0.3$	V
$I_o$	Output Current Continuous	50	mA
$P_{tot}$	Power Dissipation	500	mW
$T_{op}$	Operating Ambient Temperature Range (for <b>AC SERIES</b> ) (for <b>AB SERIES</b> )	0 to 70 - 40 to 85	°C °C
$T_{stg}$	Storage Temperature Range	- 40 to 150	°C

Absolute Maximum Rating are those values beyond which damage to the device may occur. Functional operation under these condition is not implied.

## CONNECTION DIAGRAM AND (top view)



## PIN CONNECTIONS

Pin No	Symbol	Name and Function
1	C1-	Negative Terminal For The First Charge Pump Capacitor
2	C1+	Positive Terminal For The First Charge Pump Capacitor
3	C2-	Negative Terminal For The Second Charge Pump Capacitor
4	C2+	Positive Terminal For The Second Charge Pump Capacitor
5	$V_{CC}$	Supply Voltage
6	$V_{OUT}$	12V Output Voltage $V_{OUT} = V_{CC}$ When in Sshutdown Mode
7	GND	Ground
8	SHDN	Active High C-MOS logic level Shutdown Input. SHDN is internally pulled up to $V_{CC}$ . Connect to GND for Normal Operation. In Shutdown mode the charge pumps are turned off and $V_{OUT} = V_{CC}$

## ORDERING NUMBERS

Type	DIP-8	SO-8 (*)
ST662AB	ST662ABN	ST662ABD
ST662AC	ST662ACN	ST662ACD

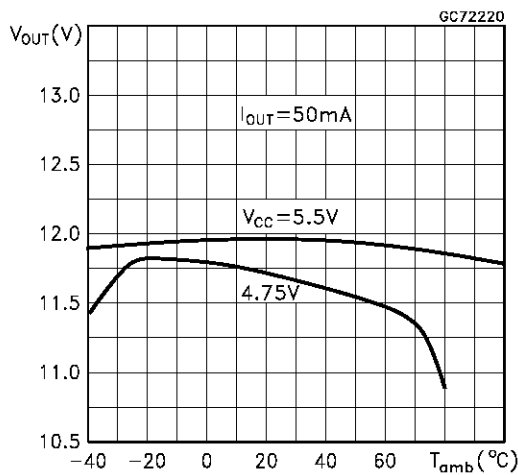
(\*) AVAILABLE IN TAPE AND REEL WITH "-TR" SUFFIX

**ELECTRICAL CHARACTERISTICS** (Refer to the test circuits,  $V_{CC} = 4.5V$  to  $5.5V$   $T_a = T_{min}$  to  $T_{max}$  unless otherwise specified. Typical Value are referred at  $T_a = 25^\circ C$ )

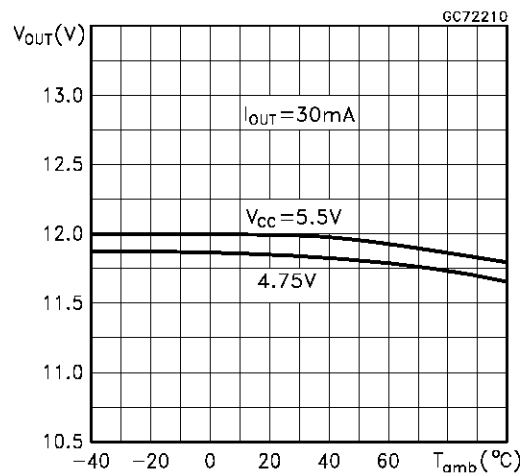
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_o$	Output Voltage	$I_o = 0\text{ mA to }20\text{ mA}$	11.4	12	12.6	V
$V_o$	Output Voltage	$I_o = 0\text{ mA to }30\text{ mA } V_{CC} = 4.75\text{ to }5.5\text{ V}$	11.4	12	12.6	V
$I_{Q1}$	Quiescent Current	No Load, $V_{SHDN} = 0$		100	500	$\mu A$
$I_{Q2}$	Shutdown Current	No Load, $V_{SHDN} = V_{CC}$		1	10	$\mu A$
$I_{SH}$	Shutdown Pin Current	$V_{SHDN} = 0V, V_{CC} = 5V$ $V_{SHDN} = V_{CC} = 5V$	-50	-12 0	-5	$\mu A$ $\mu A$
$V_{il}$	Shutdown Input Low Threshold				0.4	V
$V_{ih}$	Shutdown Input High Threshold		2.4			V
$f_o$	Oscillator Frequency	$V_{CC} = 5V, I_o = 30\text{ mA}$		400		KHz
$\eta$	Power Efficiency	$V_{CC} = 5V, I_o = 30\text{ mA}$		72		%
$R_{sw}$	$V_{CC} - V_{OUT}$ Switch Impedance	$V_{SHDN} = V_{CC} = 5V, I_o = 100\ \mu A$		1	2	K $\Omega$

Do not overload or short the Output to Ground. If the above conditions are observed, the device may be damaged.

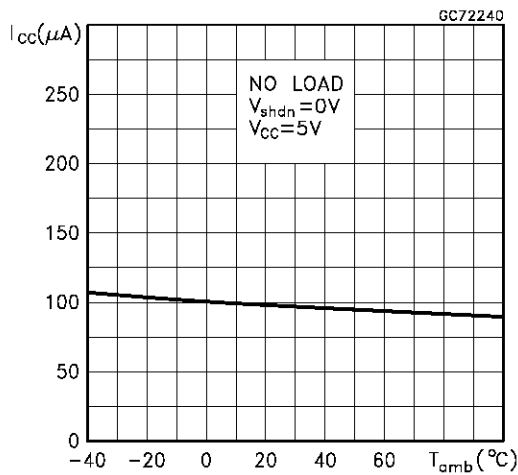
Output Voltage vs Temperature



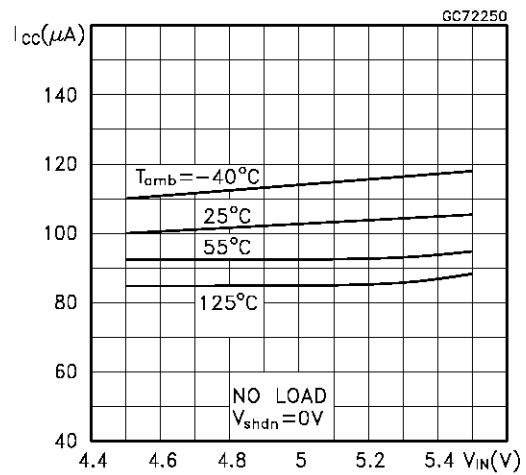
Output Voltage vs Temperature



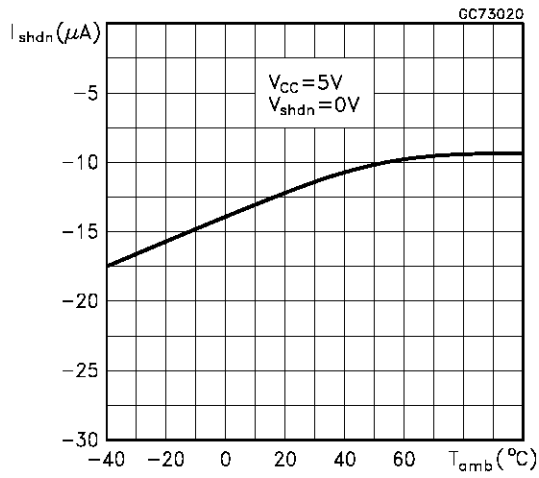
Supply Current vs Temperature



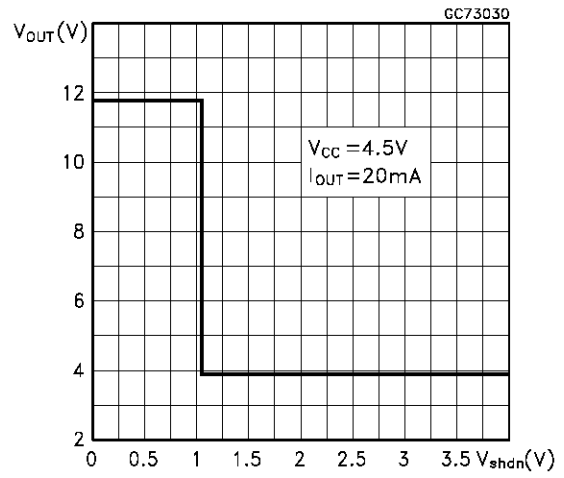
Supply Current vs Supply Voltage



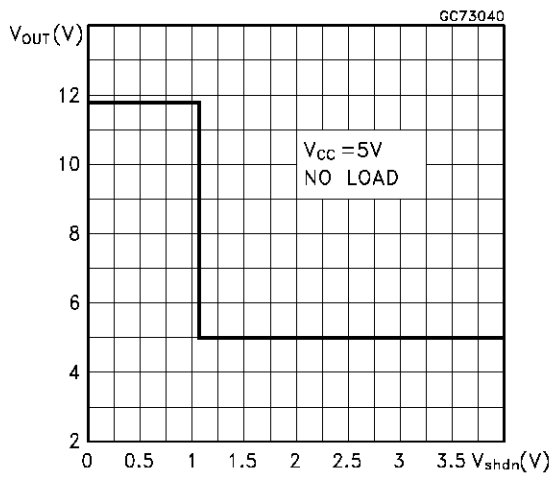
SHDN Pin Current vs Temperature



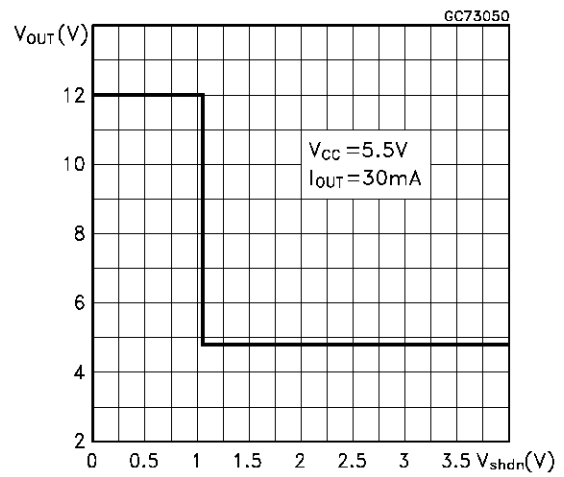
Output Voltage vs Shutdown Input Voltage



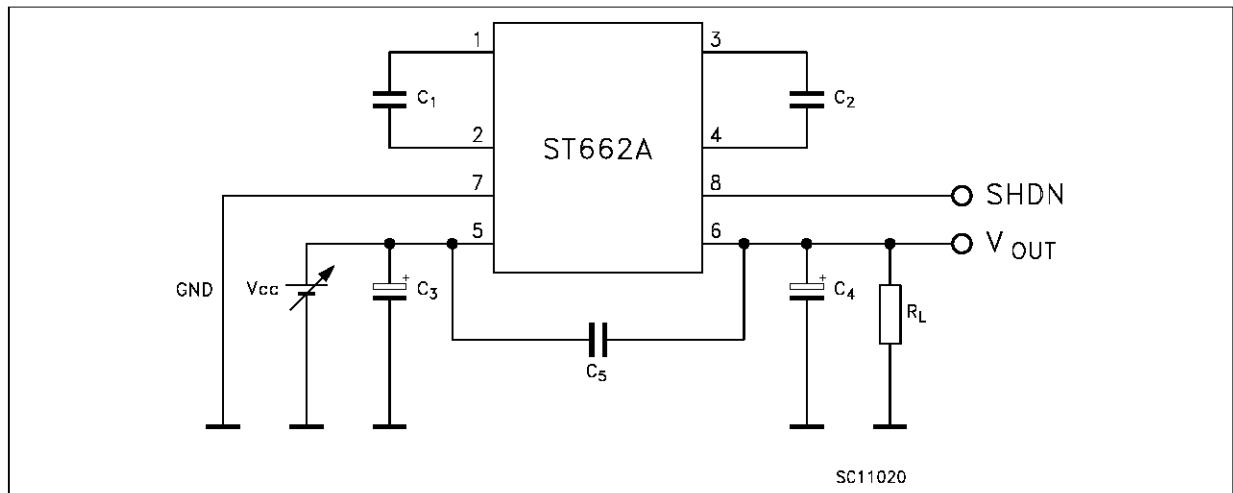
Output Voltage vs Shutdown Input Voltage



Output Voltage vs Shutdown Input Voltage



Test Circuit



**DESCRIPTION**

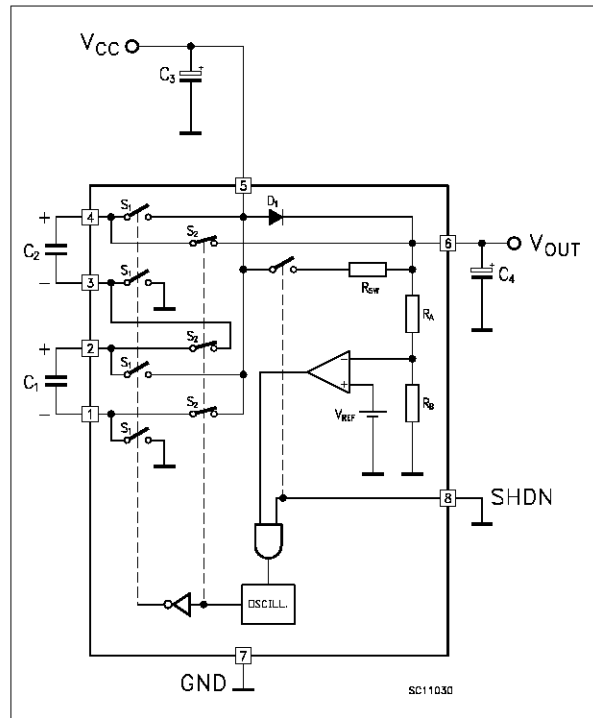
The ST662 is an IC developed to provide a 12V regulated output 30mA from voltage input as low as 4.75 without any inductors. It is useful for a wide range of applications and its performances makes it ideal for flash memory programming supply.

An evaluation kit is provided to facilitate the application. This include a single-side demo board designed for surface-mount components. The operating principle of ST662 (see fig. 1) is to charge C1 and C2 capacitor by closing the S1 switch (while S2 is opened) at the V<sub>CC</sub> voltage. After S1 will be opened and S2 closed so that C1 and C2 capacitors are placed in series one to each other, and both are in series with V<sub>in</sub>. The sum of VC1 and VC2 and V<sub>in</sub> is applied to the capacitor C4. This works as voltage tripler. An amplifier error checks the output voltage and blocks the oscillator if the output voltage is greater than 12V.

The shutdown pin is internally pulled to V<sub>CC</sub>. When it is held low the output voltage rises to +12V. Fig.2 shows the transition time of the shut down pin when the VSHDN goes from 5V to 0V. Input logic levels of this input are CMOS compatible.

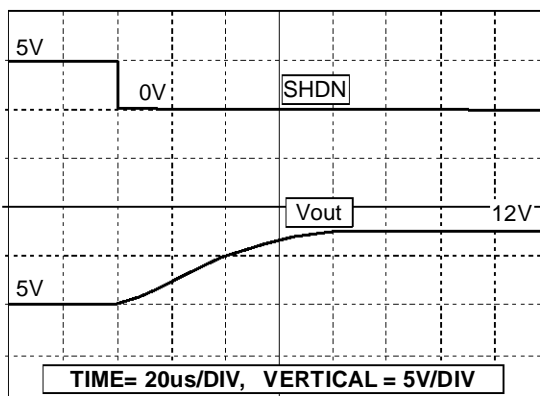
Applying a logic high at this input, the V<sub>OUT</sub> oscillator will be blocked and the V<sub>OUT</sub> will reach the V<sub>IN</sub> value by D1. In this condition I<sub>CC</sub> will be

**Figure 1: Operating Principle Circuit**



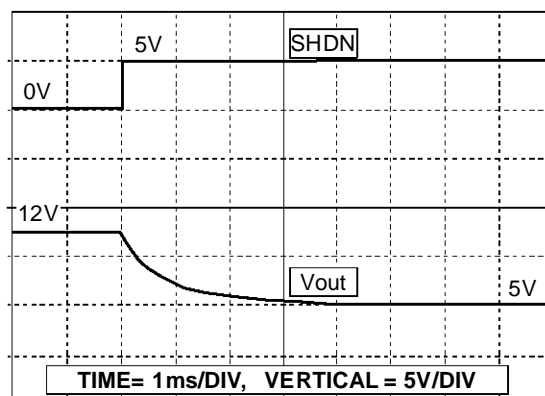
low as 1μA. The fig.3 shows the transition time of the shut down pin when the VSHDN goes from 0V to 5V.

**Figure 2: Exiting Shutdown**



NOTE: V<sub>CC</sub> = 5V, I<sub>OUT</sub> = 200μA

**Figure 3: Entering Shutdown**



NOTE: V<sub>CC</sub> = 5V, I<sub>OUT</sub> = 200μA

**APPLICATION CIRCUIT**

Based on fast charge/discharge of capacitors, this circuit involves high di/dt values limited only by  $R_{on}$  of switches. This implies a critical layout design due to the need to minimize inductive paths and place capacitors as close as possible to the device.

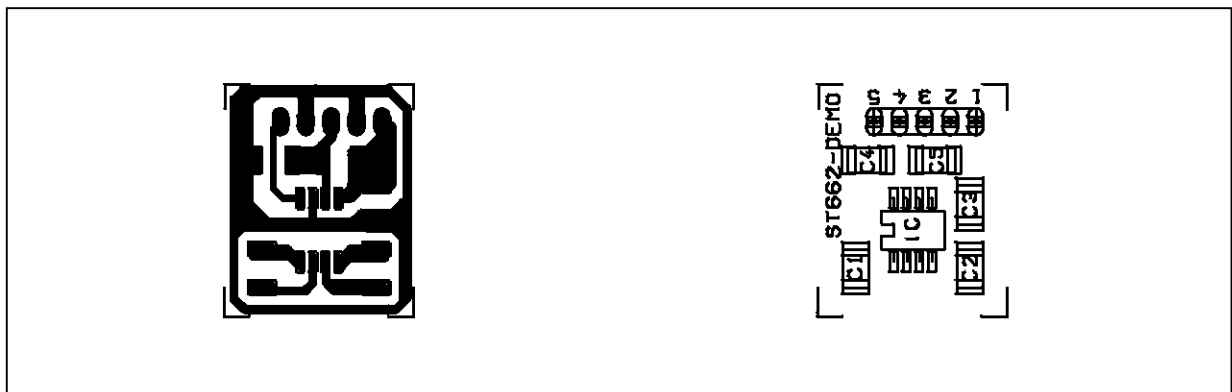
A good layout design is strongly recommended for noise reason. For best performance, use very short connections to the capacitors and the values shown in table 1.

C3 and C4 must have low ESR in order to minimize the output ripple. Their values can be reduced to  $2\mu\text{F}$  and  $1\mu\text{F}$ , respectively, when using ceramic capacitors, but must be of  $10\mu\text{F}$  or larger if aluminium electrolytic are chosen.

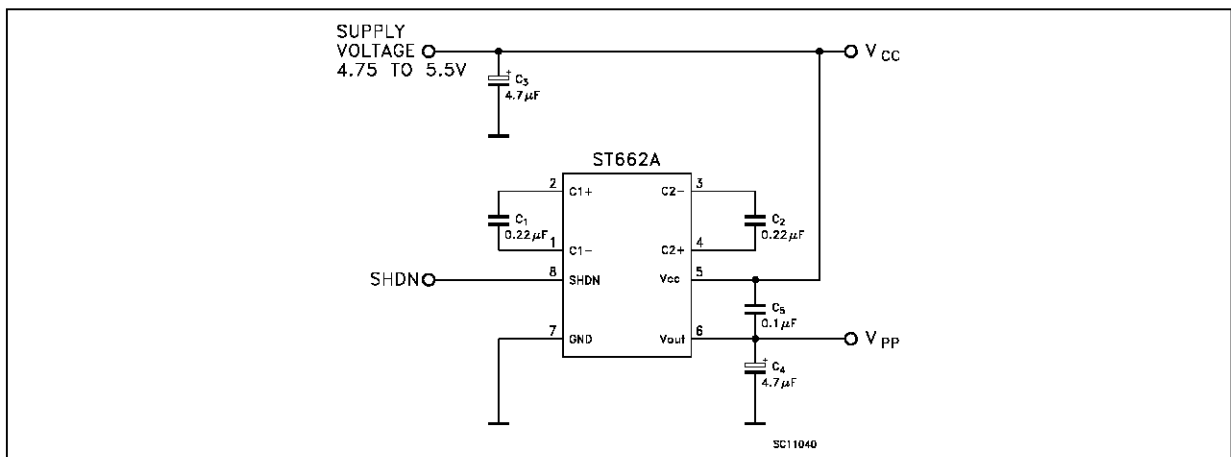
C5 must be placed as close to the device as possible and could be omitted if very low output noise performance are not required.

Fig 4 and Fig 5 show, respectively, our EVALUATION kit layout and the relatively electrical schematic.

**Figure 4:** KIT Lay-out



**Figure 5:** Electrical Schematic

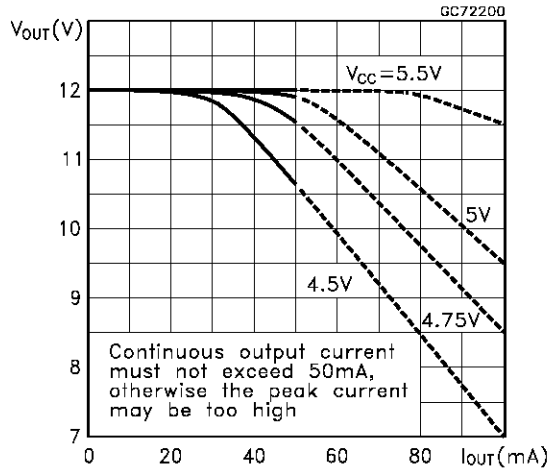


**Table 1:** List of Components

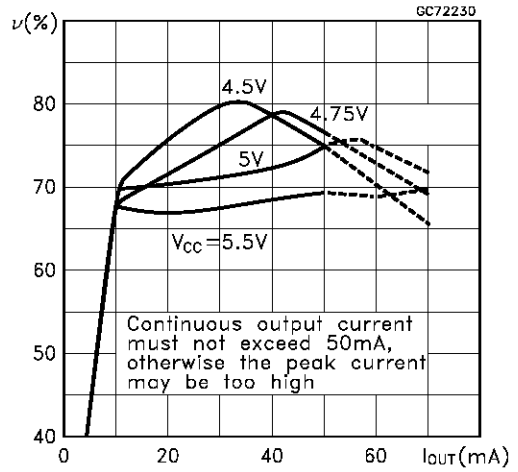
CAPACITOR	TYPE	VALUE ( $\mu\text{F}$ )
Charge Pump C1	Ceramic	0.22
Charge Pump C2	Ceramic	0.22
Input C3	Electrolytic Tantalum	4.7
Output C4	Electrolytic Tantalum	4.7
Decoupling C5	Ceramic	0.1

**ST662A OUTPUT PERFORMANCE**

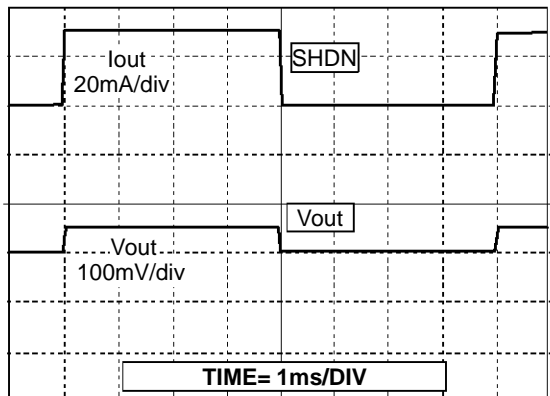
Output Voltage vs Output Current



Efficiency vs Output Current

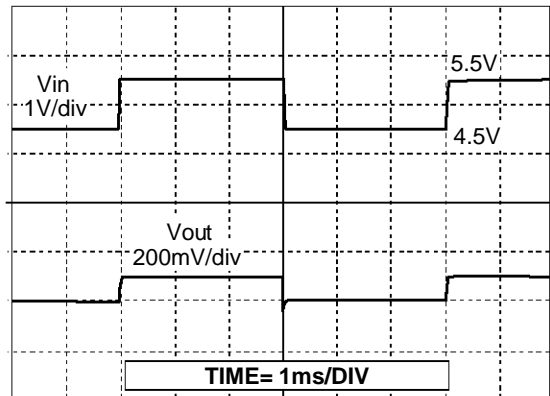


Load Transient Response



NOTE:  $V_{cc} = 5V$ ,  $I_{out} = 0$  to 30mA

Line Transient Response



NOTE:  $V_{cc} = 4.5$  to 5.5V,  $I_{out} = 30mA$

**HOW TO INCREASE OUTPUT CURRENT OR OUTPUT VOLTAGE CAPABILITY**

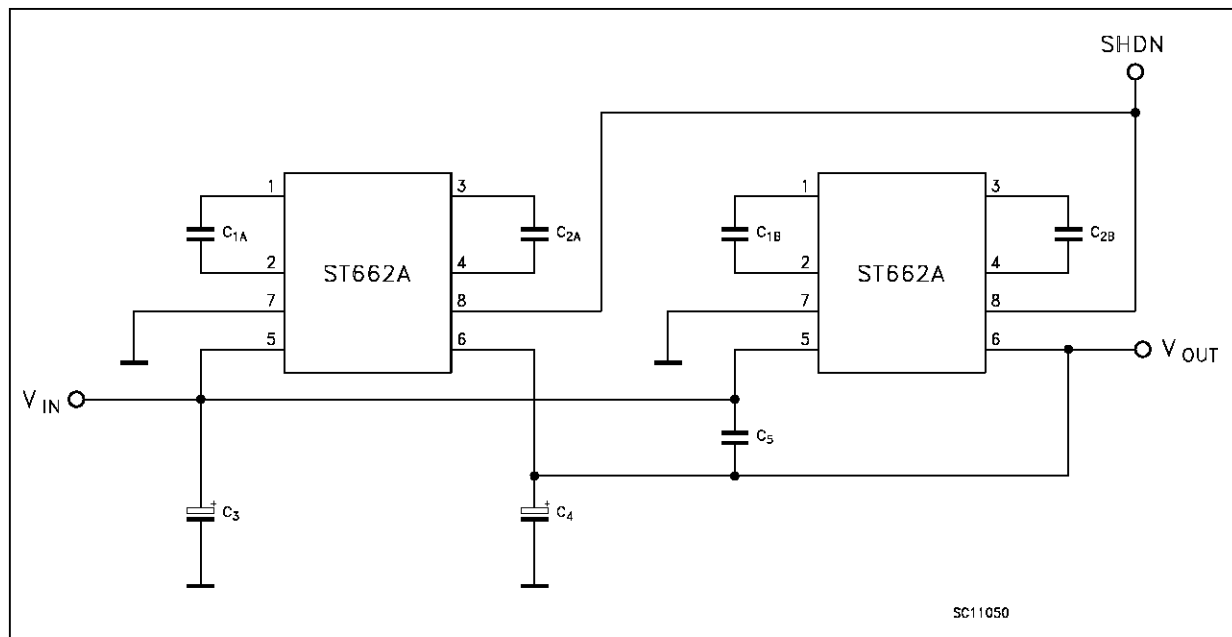
Current capability is limited by  $R_{on}$  of internal switches. It is possible to increase it connecting in parallel two or more ST662A devices; each one of them can supply 30mA. The figure 6 shows the electric schematic. The capacitors C3, C4 and C5 must be placed very close to the ICs on the board. If this is not possible, you can place two

different capacitors, each of them of half value, very close to the respective integrated circuit.

Fig. 8 show the Output Current capability of the proposed circuit.

If an output voltage greater than 12V is required, it's possible to realize the circuit of the following diagram (figure 7). The relevant Output Current capability is shown in figure 9 in which is shown the output voltage vs load current.

**Figure 6:** Application Circuit for Two ST662A in Parallel



**Table 2:** List of Components

CAPACITOR	TYPE	VALUE (μF)
C1A	Ceramic	0.22
C2A	Ceramic	0.22
C1B	Ceramic	0.22
C2B	Ceramic	0.22
C3	Electrolytic Tantalum	10
C4	Electrolytic Tantalum	10
C5	Ceramic	0.22



Figure 7: Application Circuit for Output Voltage greater than 12V

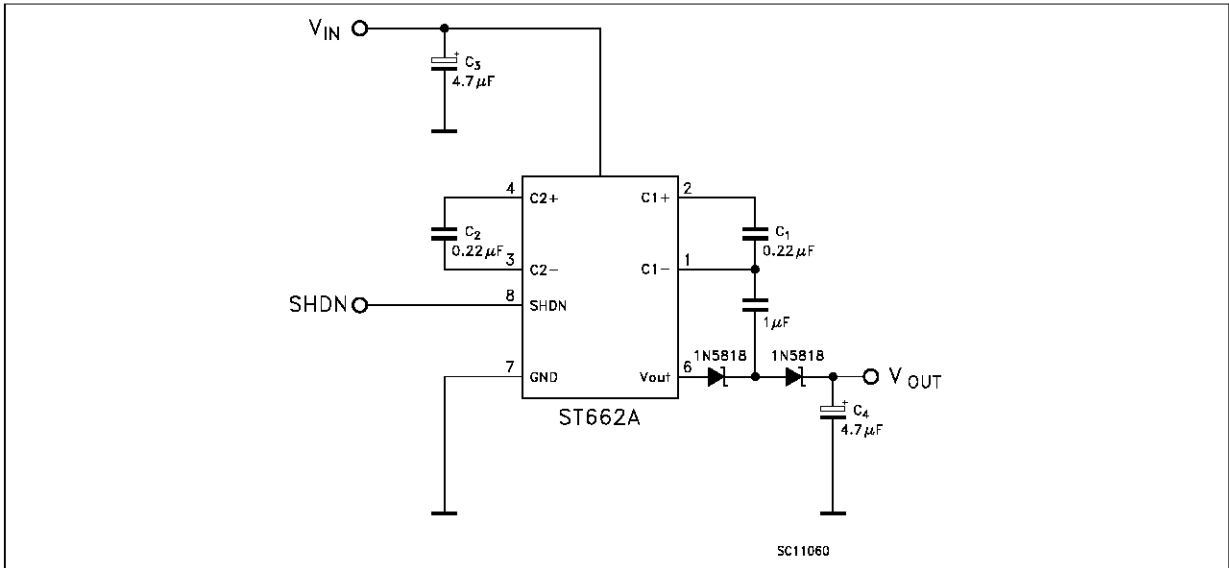


Figure 8: Output Voltage for the Application with Two Device in Parallel

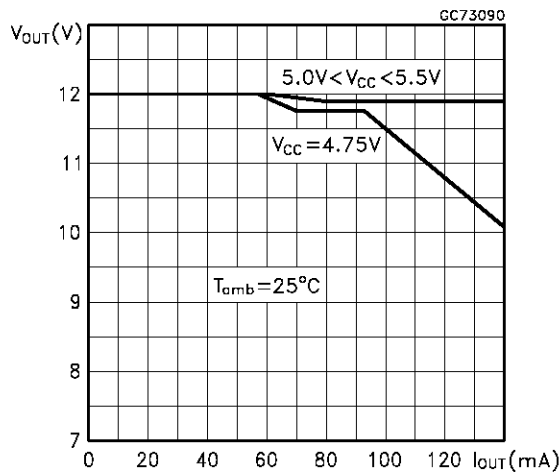
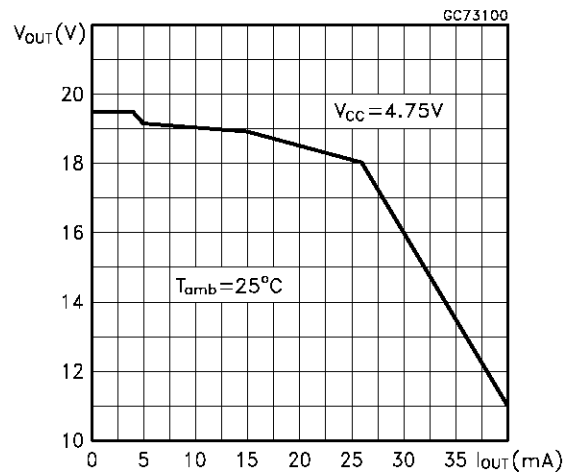
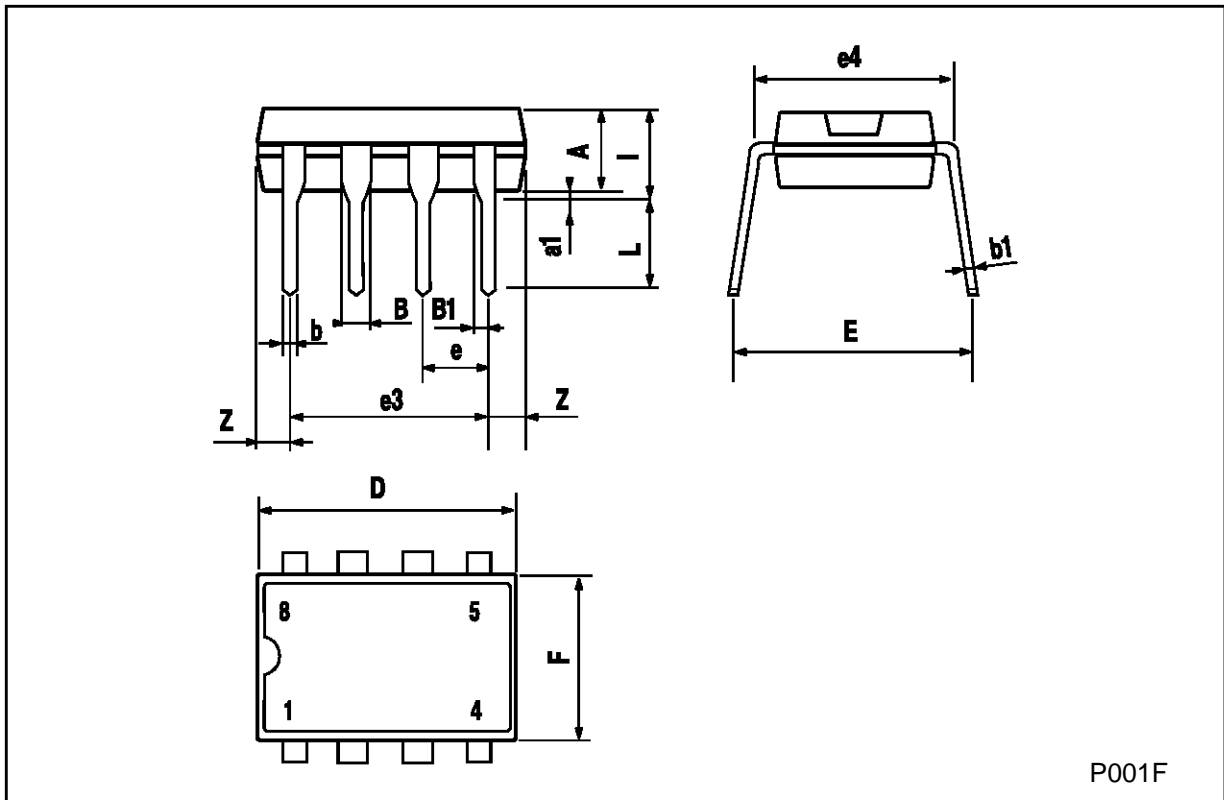


Figure 9: Output Voltage for Application with Output Voltage greater than 12V



**Plastic DIP-8 MECHANICAL DATA**

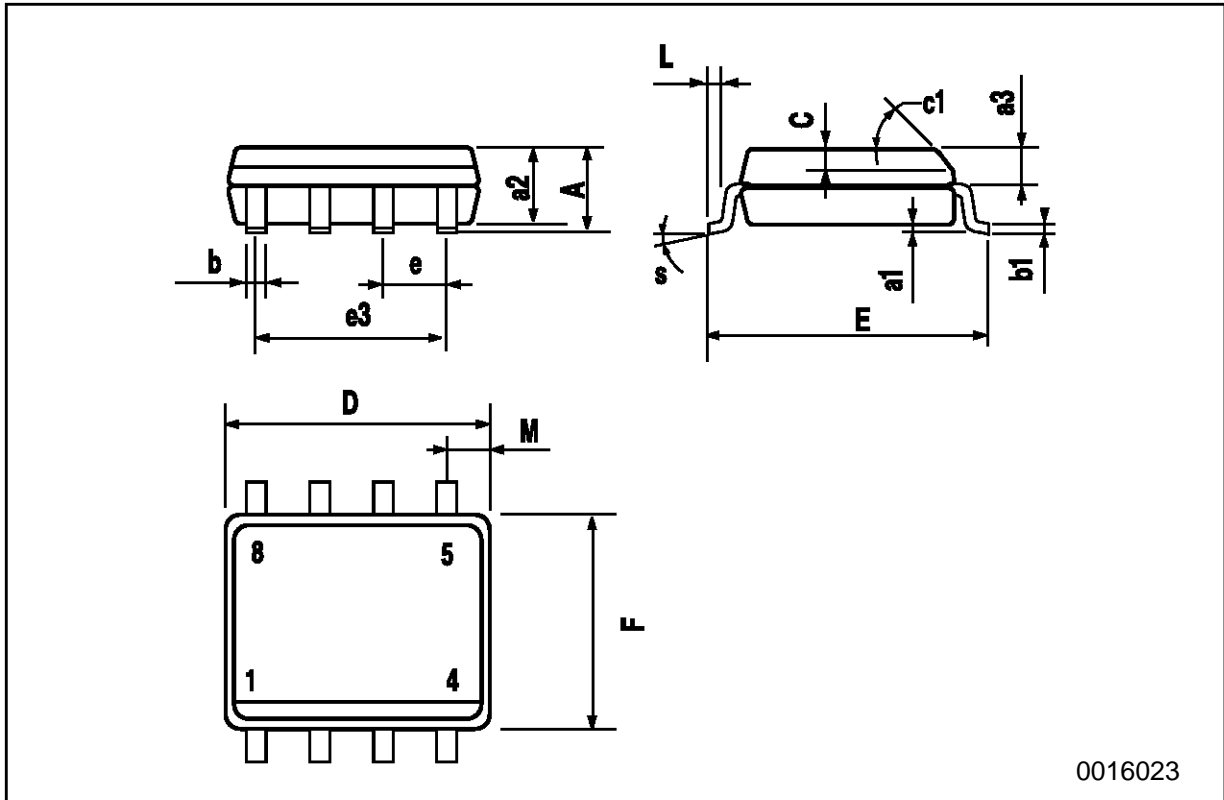
DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A		3.3			0.130	
a1	0.7			0.028		
B	1.39		1.65	0.055		0.065
B1	0.91		1.04	0.036		0.041
b		0.5			0.020	
b1	0.38		0.5	0.015		0.020
D			9.8			0.386
E		8.8			0.346	
e		2.54			0.100	
e3		7.62			0.300	
e4		7.62			0.300	
F			7.1			0.280
I			4.8			0.189
L		3.3			0.130	
Z	0.44		1.6	0.017		0.063



P001F

**SO-8 MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.75			0.068
a1	0.1		0.25	0.003		0.009
a2			1.65			0.064
a3	0.65		0.85	0.025		0.033
b	0.35		0.48	0.013		0.018
b1	0.19		0.25	0.007		0.010
C	0.25		0.5	0.010		0.019
c1	45 (typ.)					
D	4.8		5.0	0.188		0.196
E	5.8		6.2	0.228		0.244
e		1.27			0.050	
e3		3.81			0.150	
F	3.8		4.0	0.14		0.157
L	0.4		1.27	0.015		0.050
M			0.6			0.023
S	8 (max.)					



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