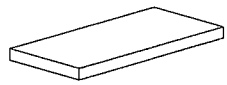
PRELIMINARY

16-CHARACTER 3-LINE DOT MATRIX LCD CONTROLLER DRIVER

■ GENERAL DESCRIPTION

The NJU6464 is a Dot Matrix LCD controller driver for 16-character 3-line with icon display in single chip.
It contains voltage converter and regulator, bleeder resistance, CR oscillator, microprocessor interface circuits, instruction decoder controller, character generator ROM/RAM, high voltage operation common and segment drivers.
The voltage converter generates high voltage(about 8V) from the supply voltage(3V) and the generated high voltage is regulated by the regulator. The bias level of LCD driving voltage is generated by high value of bleeder resistance and the buffer amplifier converts its impedance. The 16th gray scale contrast control function
is incorporated for its adjustment. Therefore, simple power supply circuit and easy contrast adjustment are available.
The complete CR oscillator is incorporated, therefore no external components for oscillation circuit are required.
The microprocessor interface circuits which operate by 1MHz, can be selected serial, 4 or 8 bits interface.
The character generator ROM consists of 10,080 bits stores 252 kinds of character Font. Each 160 bits CG RAM and Icon display RAM can store 4 kinds of special character displayed on the dot matrix display area or 152 kinds of Icon on the Icon display area.
The 29-common (24 for character, 4 for icon and 1 for static) and 83-segment (80 for character, 2 for icon and 1 for static) drivers operating up to 10.0V drives 16-character 3-line with 152 Icon and static segment LCD display.

■ PACKAGE OUTLINE



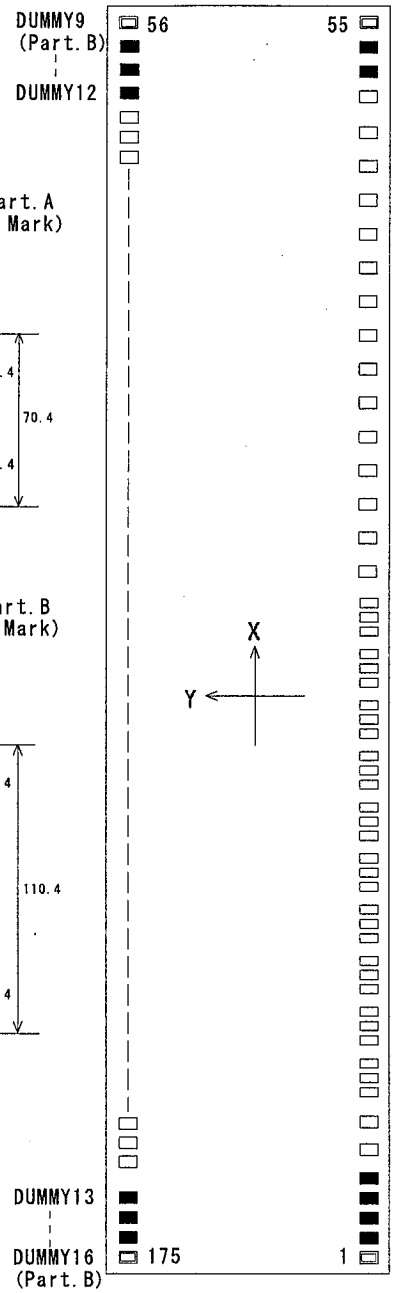
NJU6464CH

■ FEATURES

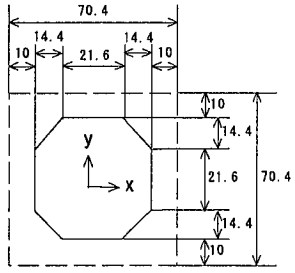
- 16-character 3-line Dot Matrix LCD Controller Driver
- Maximum 152 Icon Display
- Serial, 4 or 8 Bits parallel Direct Interface with Microprocessor
- Display Data RAM - 48 x 8 bits : Maximum 16-character 3-line Display
- Character Generator ROM - 10,080 bits : 252 Characters for 5 x 8 Dots
- Character Generator RAM - 32 x 5 bits : 4 Patterns(5 x 8 Dots)
- Icon Display RAM - 32 x 5 bits : Maximum 152 Icon
- High Voltage LCD Driver : 29-common / 83-segment
- Duty and Bias Ratio : 1/28 duty and 1/6.3 bias
- Useful Instruction Set : Clear Display, Return Home, Display ON/OFF Cont, Cursor ON/OFF Cont, Display Blink, Cursor Shift, Character Shift
- Common and Segment driver Location order Select Function(Mode A/Mode B)
- Power On Initialization / Hardware Reset
- Voltage Converter and Bleeder Resistance on-chip
- Voltage regulator on-chip
- Software contrast control
- Oscillation Circuit on-chip
- Low Power Consumption
- Operating Voltage --- 2.4 to 3.3 V (Except LCD Driving Voltage)
- Package Outline --- Bumped Chip
- C-MOS Technology

Feb. 1999
Ver. 0

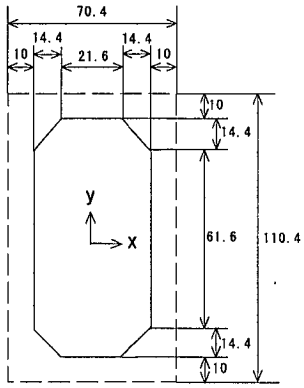
■ PAD LOCATION



Enlarged Figure of Part. A
(Alignment Mark)



Enlarged Figure of Part. B
(Alignment Mark)



Chip Size :9.89 X 1.99 mm
Chip Center : X=0um, Y=0um

Pad Size
No. 2～54、57～174
: 50um X 90um
Bump Size
No. 2～54、57～174
: 63um X 103um

Bump Heigt : 25umTYP.
Bump Material: Au

■ PAD COORDINATES CHIP SIZE 9.89 mm x 1.99 mm (CHIP CENTER X=0 μm, Y=0 μm)

PAD No.	PAD NAME		X=(μm)	Y=(μm)
	Mode A	Mode B		
1	DUMMY1	DUMMY1	-4790	-837
2	DUMMY2	DUMMY2	-4695	-837
3	DUMMY3	DUMMY3	-4615	-837
4	DUMMY4	DUMMY4	-4535	-837
5	DUMMY5	DUMMY5	-4455	-837
6	OSC1	OSC1	-4168	-837
7	OSC2	OSC2	-4008	-837
8	V5 (L)	V5 (L)	-3845	-837
9	V5 (C)	V5 (C)	-3720	-837
10	V5 (R)	V5 (R)	-3595	-837
11	VSS (L)	VSS (L)	-3333	-837
12	VSS (C)	VSS (C)	-3208	-837
13	VSS (R)	VSS (R)	-3083	-837
14	V5OUT (L)	V5OUT (L)	-2911	-837
15	V5OUT (C)	V5OUT (C)	-2786	-837
16	V5OUT (R)	V5OUT (R)	-2661	-837
17	C2⁻ (L)	C2⁻ (L)	-2396	-837
18	C2⁻ (C)	C2⁻ (C)	-2271	-837
19	C2⁻ (R)	C2⁻ (R)	-2146	-837
20	C2⁺ (L)	C2⁺ (L)	-1884	-837
21	C2⁺ (C)	C2⁺ (C)	-1759	-837
22	C2⁺ (R)	C2⁺ (R)	-1634	-837
23	C1⁻ (L)	C1⁻ (L)	-1372	-837
24	C1⁻ (C)	C1⁻ (C)	-1247	-837
25	C1⁻ (R)	C1⁻ (R)	-1122	-837
26	C1⁺ (L)	C1⁺ (L)	-860	-837
27	C1⁺ (C)	C1⁺ (C)	-735	-837
28	C1⁺ (R)	C1⁺ (R)	-610	-837
29	VDD (L)	VDD (L)	-438	-837
30	VDD (C)	VDD (C)	-313	-837
31	VDD (R)	VDD (R)	-188	-837
32	VR (L)	VR (L)	-17	-837
33	VR (C)	VR (C)	108	-837
34	VR (R)	VR (R)	233	-837
35	VREG (L)	VREG (L)	664	-837
36	VREG (C)	VREG (C)	789	-837
37	VREG (R)	VREG (R)	914	-837
38	TEST	TEST	1120	-837
39	SEL	SEL	1462	-837
40	RESET	RESET	1636	-837
41	P/S	P/S	1927	-837
42	RS	RS	2095	-837
43	R/W	R/W	2386	-837
44	E/SCL	E/SCL	2554	-837
45	DB0	DB0	2824	-837
46	DB1	DB1	3049	-837
47	DB2	DB2	3291	-837
48	DB3	DB3	3516	-837
49	DB4	DB4	3757	-837
50	DB5	DB5	3982	-837

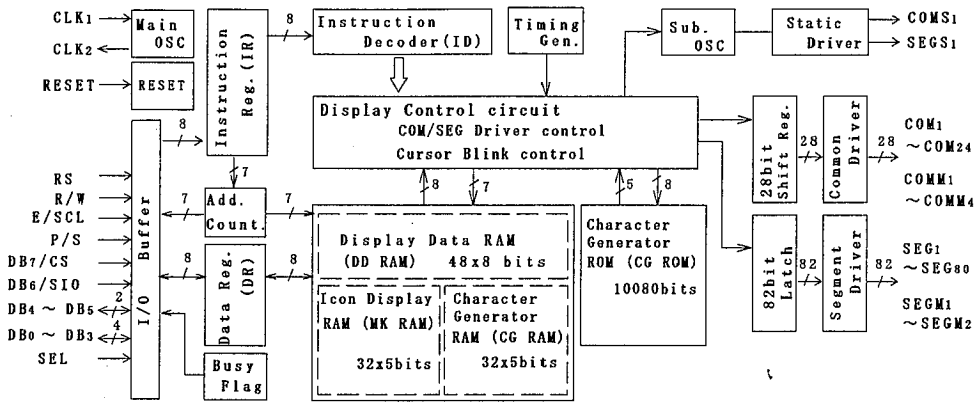
PAD No.	PAD NAME		X=(μm)	Y=(μm)
	Mode A	Mode B		
51	DB6/SIO	DB6/SIO	4224	-837
52	DB7/CS	DB7/CS	4449	-837
53	DUMMY6	DUMMY6	4610	-837
54	DUMMY7	DUMMY7	4690	-837
55	DUMMY8	DUMMY8	4788	-837
56	DUMMY9	DUMMY9	4808	847
57	DUMMY10	DUMMY10	4698	847
58	DUMMY11	DUMMY11	4618	847
59	DUMMY12	DUMMY12	4538	847
60	SEGS1	SEGS1	4458	847
61	COM9	COM9	4378	847
62	COM10	COM10	4298	847
63	COM11	COM11	4218	847
64	COM12	COM12	4138	847
65	COM13	COM13	4058	847
66	COM14	COM14	3978	847
67	COM15	COM15	3898	847
68	COM16	COM16	3818	847
69	SEGM1	SEGM2	3738	847
70	SEG1	SEG80	3658	847
71	SEG2	SEG79	3578	847
72	SEG3	SEG78	3498	847
73	SEG4	SEG77	3418	847
74	SEG5	SEG76	3338	847
75	SEG6	SEG75	3258	847
76	SEG7	SEG74	3178	847
77	SEG8	SEG73	3098	847
78	SEG9	SEG72	3018	847
79	SEG10	SEG71	2938	847
80	SEG11	SEG70	2858	847
81	SEG12	SEG69	2778	847
82	SEG13	SEG68	2698	847
83	SEG14	SEG67	2618	847
84	SEG15	SEG66	2538	847
85	SEG16	SEG65	2458	847
86	SEG17	SEG64	2378	847
87	SEG18	SEG63	2298	847
88	SEG19	SEG62	2218	847
89	SEG20	SEG61	2138	847
90	SEG21	SEG60	2058	847
91	SEG22	SEG59	1978	847
92	SEG23	SEG58	1898	847
93	SEG24	SEG57	1818	847
94	SEG25	SEG56	1738	847
95	SEG26	SEG55	1658	847
96	SEG27	SEG54	1578	847
97	SEG28	SEG53	1498	847
98	SEG29	SEG52	1418	847
99	SEG30	SEG51	1338	847
100	SEG31	SEG50	1258	847

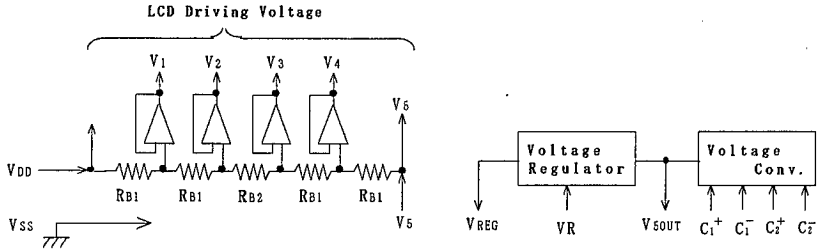
PAD No.	PAD NAME		X=(μm)	Y=(μm)
	Mode A	Mode B		
101	SEG_{32}	SEG_{49}	1178	847
102	SEG_{33}	SEG_{48}	1098	847
103	SEG_{34}	SEG_{47}	1018	847
104	SEG_{35}	SEG_{46}	938	847
105	SEG_{36}	SEG_{45}	858	847
106	SEG_{37}	SEG_{44}	778	847
107	SEG_{38}	SEG_{43}	698	847
108	SEG_{39}	SEG_{42}	618	847
109	SEG_{40}	SEG_{41}	538	847
110	SEG_{41}	SEG_{40}	458	847
111	SEG_{42}	SEG_{39}	378	847
112	SEG_{43}	SEG_{38}	298	847
113	SEG_{44}	SEG_{37}	218	847
114	SEG_{45}	SEG_{36}	138	847
115	SEG_{46}	SEG_{35}	58	847
116	SEG_{47}	SEG_{34}	-22	847
117	SEG_{48}	SEG_{33}	-102	847
118	SEG_{49}	SEG_{32}	-182	847
119	SEG_{50}	SEG_{31}	-262	847
120	SEG_{51}	SEG_{30}	-342	847
121	SEG_{52}	SEG_{29}	-422	847
122	SEG_{53}	SEG_{28}	-502	847
123	SEG_{54}	SEG_{27}	-582	847
124	SEG_{55}	SEG_{26}	-662	847
125	SEG_{56}	SEG_{25}	-742	847
126	SEG_{57}	SEG_{24}	-822	847
127	SEG_{58}	SEG_{23}	-902	847
128	SEG_{59}	SEG_{22}	-982	847
129	SEG_{60}	SEG_{21}	-1062	847
130	SEG_{61}	SEG_{20}	-1142	847
131	SEG_{62}	SEG_{19}	-1222	847
132	SEG_{63}	SEG_{18}	-1302	847
133	SEG_{64}	SEG_{17}	-1382	847
134	SEG_{65}	SEG_{16}	-1462	847
135	SEG_{66}	SEG_{15}	-1542	847
136	SEG_{67}	SEG_{14}	-1622	847
137	SEG_{68}	SEG_{13}	-1702	847
138	SEG_{69}	SEG_{12}	-1782	847
139	SEG_{70}	SEG_{11}	-1862	847
140	SEG_{71}	SEG_{10}	-1942	847
141	SEG_{72}	SEG_{9}	-2022	847
142	SEG_{73}	SEG_{8}	-2102	847
143	SEG_{74}	SEG_{7}	-2182	847
144	SEG_{75}	SEG_{6}	-2262	847
145	SEG_{76}	SEG_{5}	-2342	847
146	SEG_{77}	SEG_{4}	-2422	847
147	SEG_{78}	SEG_{3}	-2502	847
148	SEG_{79}	SEG_{2}	-2582	847
149	SEG_{80}	SEG_{1}	-2662	847
150	$SEGM_{2}$	$SEGM_{1}$	-2742	847

PAD No.	PAD NAME		X=(μm)	Y=(μm)
	Mode A	Mode B		
151	COM_{24}	COM_{24}	-2822	847
152	COM_{23}	COM_{23}	-2902	847
153	COM_{22}	COM_{22}	-2982	847
154	COM_{21}	COM_{21}	-3062	847
155	COM_{20}	COM_{20}	-3142	847
156	COM_{19}	COM_{19}	-3222	847
157	COM_{18}	COM_{18}	-3302	847
158	COM_{17}	COM_{17}	-3382	847
159	COM_{8}	COM_{8}	-3462	847
160	COM_{7}	COM_{7}	-3542	847
161	COM_{6}	COM_{6}	-3622	847
162	COM_{5}	COM_{5}	-3702	847
163	COM_{4}	COM_{4}	-3782	847
164	COM_{3}	COM_{3}	-3862	847
165	COM_{2}	COM_{2}	-3942	847
166	COM_{1}	COM_{1}	-4022	847
167	$COMM_{4}$	$COMM_{4}$	-4102	847
168	$COMM_{3}$	$COMM_{3}$	-4182	847
169	$COMM_{2}$	$COMM_{2}$	-4262	847
170	$COMM_{1}$	$COMM_{1}$	-4342	847
171	$COMS_{1}$	$COMS_{1}$	-4422	847
172	$DUMMY_{13}$	$DUMMY_{13}$	-4502	847
173	$DUMMY_{14}$	$DUMMY_{14}$	-4582	847
174	$DUMMY_{15}$	$DUMMY_{15}$	-4662	847
175	$DUMMY_{16}$	$DUMMY_{16}$	-4808	847

Note : Mode A:SEL="L", Mode B:SEL="H"

■ BLOCK DIAGRAM





■ TERMINAL DESCRIPTION

PAD No	SYMBOL	I/O	FUNCTION
29, 30, 31 10, 11, 12	V_{DD}, V_{SS}	—	Power Source V_{DD} : +3V , V_{SS} : 0V
8, 9, 10	V_5	—	LCD driving voltage
6	OSC_1	I	System clock input terminal This terminal should be open for internal clock operation.
7	OSC_2	O	System clock output terminal This terminal can use for clock frequency monitoring.
41	P/S	I	Parallel or serial interface selection terminal "0":Serial interface "1":Parallel interface
42	RS	I	Register selection signal input terminal "0":Instruction register (writing) Busy flag, address counter (reading) "1":Data register (writing / reading)
43	R/W	I	Read / Write selection signal input terminal "0":Write "1": Read
44	E	I	Read / Write activation signal input in parallel mode
	SCL	I	Sift clock input in serial mode
52	DB_7	I/O	3-state data bus for MSB to transfer the Data between MPU and NJU6464 in parallel mode . DB_7 is also used for the Busy Flag reading.
	CS	I	Chip select signal input in serial mode
51	DB_6	I/O	3-state data bus for bit 6 to transfer the Data between MPU and NJU6464 in parallel mode
	SIO	I/O	Serial Data I/O in serial mode
49, 50	DB_4, DB_5	I/O	3-state data bus for bit 4 and 5 to transfer the Data between MPU and NJU6464 in parallel mode . In serial mode, these terminals are not used and should be open.
45～48	DB_0～DB_3	I/O	3-state data bus for lower 4 bits to transfer the Data between MPU and NJU6464 in parallel mode In serial and 4-bit parallel mode, these terminals are not used and should be open.
61～68 151～166	COM_1～COM_{24}	O	LCD common driving signal output terminals
167～170	$COMM_1$～$COMM_4$	O	Icon common driving signal output terminals
171	$COMS_1$	O	Static driving common signal output terminal When power down mode, V_{DD} or V_{SS} level are output.
70～149	SEG_1～SEG_{80}	O	LCD segment driving signal output terminals
69, 150	$SEGM_1$, $SEGM_2$	O	Icon segment driving signal output terminals
60	$SEGS_1$	O	Static driving segment signal output terminal When power down mode, V_{DD} or V_{SS} level are output.

PAD No	SYMBOL	I/O	FUNCTION
17～28	C_1^+, C_1^- C_2^+, C_2^-	I/O	Step up voltage capacitor connecting terminals In case of tripler operation, connect the capacitor between C_1^+ and C_1^-, C_2^+ and C_2^-. In case of doubler operation, connect the capacitor between C_2^+ and C_2^-, connect C_2^+ to C_1^+, and C_1^- should be open.
14, 15, 16	V_{5OUT}	O	Step up voltage output terminal
35, 36, 37	V_{REG}	O	Voltage regulator output terminal Connect the resistor between this terminal and VR Terminal.
32, 33, 34	VR	I	Reference voltage for voltage regulator input terminal Connect the resistor between this terminal and V_{DD} terminal.
40	$\overline{RESET}$	I	Reset Terminal. When the "L" level input over than 1.2ms to this terminal, the system will be reset (at f_{OSC} 145KHz).
39	SEL	I	Common and Segment driver location order select terminal "0":Mode A location (See the PAD COORDINATES) "1":Mode B location (See the PAD COORDINATES)
38	TEST	I	Maker Testing Terminal (Pull down) This terminal should be connected to V_{SS} or open.
2～5	$DUMMY_2$ ～$DUMMY_5$	—	Dummy terminal These terminals are electrically open.
53, 54	$DUMMY_6$, $DUMMY_7$		
57～59	$DUMMY_{10}$ ～$DUMMY_{12}$		
172～174	$DUMMY_{13}$ ～$DUMMY_{15}$		
1 55 56 175	$DUMMY_1$ $DUMMY_8$ $DUMMY_9$ $DUMMY_{16}$	—	Dummy terminal These terminals are electrically open and an alignment pattern is placed beside each terminals.

■ FUNCTIONAL DESCRIPTION

(1)Description for each block

(1-1)Register

The NJU6464 incorporates two 8-bit registers, an Instruction Register(IR) and a Data Register (DR). The Register(IR) stores instruction codes such as "Clear Display" and "Cursor Shift" or address data for Display Data RAM(DD RAM), Character Generator RAM(CG RAM) and Icon Display RAM (MK RAM).
The MPU can write the instruction code and address data to the Register(IR), but it cannot read out from the Register(IR).
The Register(DR) is a temporary stored register, the data stored in the Register(DR) is written into the DD RAM, CG RAM or MK RAM and read out from the DD RAM, CG RAM or MK RAM.
The data in the Register(DR) written by the MPU is transferred automatically to the DD RAM, CG RAM or MK RAM by internal operation.
When the address data for the DD RAM, CG RAM or MK RAM is written into the Register(IR), the addressed data in the DD RAM, CG RAM or MK RAM is transferred to the Register(DR).
By the MPU read out the data in the Register(DR), the data transmitting process is performed completely.
After reading the data in the Register(DR) by the MPU, the next address data in the DD RAM, CG RAM or MK RAM is transferred automatically to the Register(DR) to provide for the next MPU reading.
These two registers are selected by the selection signal RS as shown below.
Table 1. shows register operation controlled by RS and R/W signals.

Table 1. Register Operation

RS	R/W	Selected Register	Operation
0	0	IR	Write
0	1		Read busy flag(DB_7) and address counter (DB_0~DB_6)
1	0	DR	Write (Register(DR) to DD RAM, CG RAM or MK RAM)
1	1		Read (DD RAM, CG RAM or MK RAM to Register(DR)

(1-2)Busy Flag (BF)

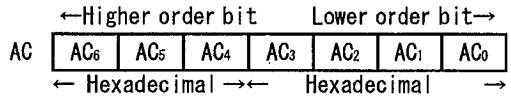
When the internal circuits are in the operation mode, the busy flag(BF) is "1", and any instruction reading is inhibited.
The busy flag(BF) is output at DB_7 when RS="0" and R/W="1" as shown in Table 1.
The next instruction should be written after the busy flag(BF) goes to "0".

(1-3)Address Counter (AC)

The address counter(AC) addresses the DD RAM, CG RAM or MK RAM.
When the address setting instruction is written into the Register(IR), the address information is transferred from Register(IR) to the Counter(AC). The selection of either the DD RAM, CG RAM or MK RAM is also determined by this instruction.
After writing (or reading) the display data to (or from) the DD RAM, CG RAM or MK RAM, the Counter(AC) increments (or decrements) automatically.
The address data in the Counter(AC) is output from DB_6 ~ DB_0 when RS="0" and R/W="1" as shown in Table 1.

(1-4) Display Data RAM (DD RAM)

The display data RAM (DD RAM) consists of 48 x 8 bits stores up to 48-character display data represented in 8-bit code.
The DD RAM address data set in the address counter (AC) is represented in Hexadecimal.



(Example) DD RAM address " 08 "

0	0	0	1	0	0	0
←	0	→←		8		→

・3-line Display

The relation between DD RAM address and display position on the LCD is shown below.

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	←Display Position
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	←DD RAM Address (Hexadecimal)
2nd Line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
3rd Line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	

When the display shift is performed, the DD RAM address changes as follows:

(Left Shift Display)

(00) ←	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	00
(10) ←	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	10
(20) ←	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	20

(Right Shift Display)

0F	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	→ (0F)
1F	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	→ (1F)
2F	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	→ (2F)

Note : The left and right shift performs only in same line, the display data do not change to other line.

(1-5) Character Generator ROM (CG ROM)

The Character Generator ROM (CG ROM) generates 5 x 8 dots character pattern represented in 8-bit character code.
The storage capacity is up to 252 kinds of 5 x 8 dots character pattern (available address is $(04)_H$ through $(FF)_H$).
The correspondence between character code and standard character pattern of NJU6464 is shown in Table 2-1.
User-defined character patterns (Custom Font) are also available by mask option.

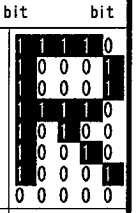
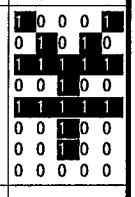
Table 2-1. CG ROM Character Pattern (ROM version -02)

Lower 4bit (Hexadecimal) \ Upper 4bit (Hexadecimal)	0	1	2	3	4	5	6	7	8	9	A	B	C	D	E	F
0	CG RAM (01)															
1	(02)															
2	(03)															
3	(04)															
4																
5																
6																
7																
8																
9																
A																
B																
C																
D																
E																
F																

(1-6) Character Generator RAM (CG RAM)

The character generator RAM (CG RAM) can store any kind of character pattern in 5 x 8 dots written by the user program to display user's original character pattern. The CG RAM can store 4 kinds of character in 5 x 8 dots mode.
To display user's original character pattern stored in the CG RAM, the address data $(00)_H$-$(03)_H$ should be written to the DD RAM as shown in Table 2-1.
Table 3. shows the correspondence among the character pattern, CG RAM address and Data.

Table 3. Correspondence of CG RAM address, DD RAM character code and CG RAM character pattern(5 x 7 dots)

Character Code (DD RAM Data)	CG RAM Address		Character Pattern (CG RAM Data)
7 6 5 4 3 2 1 0 ← → Upperbit Lower bit	7 6 5 4 3 2 1 0 ← → Upperbit Lower bit		← 4 3 2 1 0 → Upper bit Lower bit
0 0 0 0 0 0 0 0	0 1 0 0 0	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	 Character Pattern Example(1) ←Cursor Position
0 0 0 0 0 0 0 1	0 1 0 0 1	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	 Character Pattern Example(2) ←Cursor Position
		0 0 0 0 0 1	
. . .	. . .	. . .	. . .
0 0 0 0 0 0 1 1	0 1 0 1 1	1 0 0 1 0 1 1 1 0 1 1 1	

Notes : 1. Character code bit 0, 1 correspond to the CG RAM address bit 3, 4 (2bits:4 patterns).
2. CG RAM address 0 to 2 designate character pattern line position. The 8th line is the cursor position and the display is performed by logical OR with cursor. Therefore, in case of the cursor display, the 8th line should be "0". If there is "1" in the 8th line, the bit "1" is always displayed on the cursor position regardless of cursor existence.
3. Character pattern row position correspond to the CG RAM data bits 0 to 4 are shown above.
4. CG RAM character patterns are selected when character code bits 2 to 7 are all "0" and these are addressed by character code bits 0 and 1.
5. "1" for CG RAM data corresponds to display ON and "0" to display OFF.

(1-7) Icon Display RAM (MK RAM)

The NJU6464 can display maximum 152 Icons.
The Icon Display can be controlled by writing the Data in MK RAM corresponds to the Icon.
The relation between MK RAM address and Icon Display position is shown below:

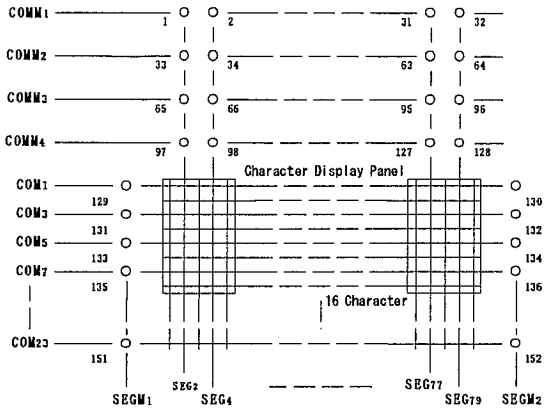


Table 4. Correspondence among Icon Position, MK RAM Address and Data

MK RAM Address	Bits for Icon Display Position								
	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	
60_H	*	*	*	1	2	3	4	129	COMM1 Line and Both besides of 1st Line (COM1, 3, 5, 7)
61_H	*	*	*	5	6	7	8	130	
:	:								
67_H	*	*	*	29	30	31	32	136	
68_H	*	*	*	33	34	35	36	137	COMM2 Line and Both besides of 2nd Line (COM9, 11, 13, 15)
69_H	*	*	*	37	38	39	40	138	
:	:								
$6F_H$	*	*	*	61	62	63	64	144	
70_H	*	*	*	65	66	67	68	145	COMM3 Line and Both besides of 3rd Line (COM17, 19, 21, 23)
71_H	*	*	*	69	70	71	72	146	
:	:								
77_H	*	*	*	93	94	95	96	152	
78_H	*	*	*	97	98	99	100	*	COMM4 Line
79_H	*	*	*	101	102	103	104	*	
:	:								
$7F_H$	*	*	*	125	126	127	128	*	

*:Don't care

Notes: 1. When the Icon display function using, the system should be initialized by the software initialization because the MK RAM is not initialized by the power turning on and hardware reset.
2. The cross-points between $SEGM_1$, $SEGM_2$ and some of common $COMM_1$ through $COMM_4$, even common likes as COM_2, COM_4...COM_{24}, are always off because of the corresponding RAM does not exist as shown above.
3. In the table 4, the bits D_5 to D_7 mentioned by * are invalid, therefore both of "0" or "1" can be written but these are no meaning.

(1-8)Timing Generator

The timing generator generates a timing signals for the DD RAM, CG RAM and MK RAM and other internal circuits.
RAM read timing for the display and internal operation timing for MPU access are separately generated, so that they may not interfere with each other.
Therefore, when the data write to the DD RAM for example, there will be no undesirable influence, such as flickering, in areas other than the display area.

(1-9)LCD Driver

LCD Driver consists of 29-common driver and 83-segment driver.
The character pattern data are latched to the addressed Segment-register respectively. This latched data controls display driver to output LCD driving waveform.

(1-10)Cursor Blinking Control Circuit

This circuits controls cursor On/Off and the cursor position character blinks.
The cursor or blinks appear in the digit residing at the DD RAM address set in the address counter (AC).
When the address counter is $(28)_H$, a cursor position is shown as follows:

	AC_6	AC_5	AC_4	AC_3	AC_2	AC_1	AC_0
AC	0	0	0	1	0	0	0

3-Line display

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	←Display position
1st Line	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	←DD RAM address (Hexadecimal)
2nd Line	10	11	12	13	14	15	16	17	18	19	1A	1B	1C	1D	1E	1F	
3rd Line	20	21	22	23	24	25	26	27	28	29	2A	2B	2C	2D	2E	2F	

Cursor position

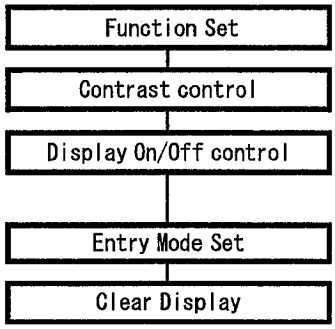
Note : The cursor or blinks also appear when the address counter (AC) selects the CG RAM or the MK RAM. But the displayed cursor and blink are meaningless.
If the AC storing the CG or MK RAM address data, the cursor and blink are displayed in the meaningless position.

(2)Power on Initialization by internal circuits

(2-1)Initialization By Internal Reset Circuits

The NJU6464 is automatically initialized by internal power on initialization circuits when the power is turned on. In the internal power on initialization, following instructions are executed. During the Internal power on initialization, the busy flag (BF) is "1" and this status is kept 7 ms (fosc=145kHz) after V_{DD} rises to 2.4V.

Initialization flow is shown below:



DL=1 :8-bit long interface data
PD=1 :Power down off

Setting $(00)_H$ to the contrast control register

D = 0 :Display Off
C = 0 :Cursor Off
B = 0 :Cursor Blink Off

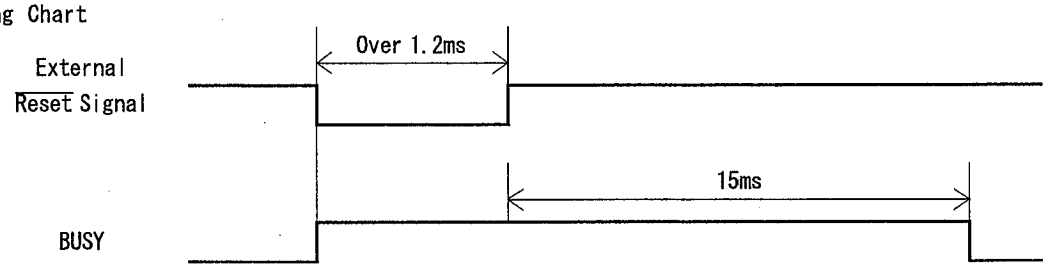
I/D=1 :Increment by 1
S = 0 :No Shift

Note : If the condition of power supply rise time described in the Electrical Characteristics is not satisfied, the internal Power On Initialization Circuits will not operated and initialization will not performed.
In this case the initialization by MPU software is required.

(2-2)Initialization By Hardware

The NJU6464 incorporates $\overline{RESET}$ terminal to initialize the all system. When the "L" level input over 1.2ms to the $\overline{RESET}$ terminal, reset sequence is executed. In this time, busy signal output during 15 ms (fosc=145kHz) after $\overline{RESET}$ terminal goes to "H".

・Timing Chart



(3)Instructions

The NJU6464 incorporates two registers, an Instruction Register (IR) and a Data Register(DR). These two registers store control information temporarily to allow interface between NJU6464 and MPU or peripheral ICs operating different cycles. The operation of NJU6464 is determined by this control signal from MPU. The control information includes register selection signals (RS), read/write signals (R/W) and data bus signals (DB_0 to DB_7).
Table 5. shows each instruction and its operating time.

Note : The execution time mentioned in Table 5. based on fcp or fosc=145kHz.
If the oscillation frequency is changed, the execution time is also changed.

Table 4. Table of Instructions

INSTRUCTIONS	CODE RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	DESCRIPTION	Execute Time
Maker Testing	0	0	0	0	0	0	0	0	0	0	All "0" code is using for maker testing.	—
Clear Display	0	0	0	0	0	0	0	0	0	1	Display clear and sets RAM address $(00)_H$ in AC.	14.13ms
Return Home	0	0	0	0	0	0	0	0	1	*	Sets RAM address $(00)_H$ in AC and returns display being shifted original position. RAM contents remain unchanged.	600μs
Entry Mode Set	0	0	0	0	0	0	0	1	I/D	S	Sets cursor move direction and specifies shift of display are performed in data read/write. I/D=1:Increment, I/D=0:Decremen S=1:Accompanies display shift	0μs
Display ON/OFF Control	0	0	0	0	0	0	1	D	C	B	Sets of display On/Off(D), cursor On/Off(C) and blink of cursor position character(B).	0μs
Cursor or Display Shift	0	0	0	0	0	1	S/C	R/L	*	*	Moves cursor & shifts display without changing RAM contents S/C=1 : Display shift S/C=0 : Cursor shift R/L=1 : Shift to the right R/L=0 : Shift to the left	cursor: 600μs display: 0μs
Function Set	0	0	0	0	1	DL	*	*	*	PD	Sets interface data length(DL) and power down mode(PD).	PD=0: 0μs PD=1: 200μs
Contrast control	0	0	0	1	*	*	←—	Cc		—→	Sets data to Contrast Control Register.	0μs
Set RAM Address	0	0	1	←—			A_R			—→	Sets RAM address. After this instruction, the data is transferred to/from RAM.	600μs
Read Busy Flag & AC contents	0	1	BF	←—			AC			—→	Reads busy flag and AC content BF=1 : Internally operating BF=0 : Can accept instruction	0μs
Write Data to RAM	1	0	←—			Write Data		(DD RAM)		—→	Writes data into RAM.	600μs
	1	0	*	*	*	←—		(CG RAM)		—→		
	1	0	*	*	*	←—		(MK RAM)		—→		
Read Data from RAM	1	1	←—			Read Data		(DD RAM)		—→	Reads data from RAM.	600μs
	1	1	*	*	*	←—		(CG RAM)		—→		
	1	1	*	*	*	←—		(MK RAM)		—→		
Explanation of Abbreviation	DD RAM : Display data RAM, CG RAM : Character generator RAM, MK RAM : Icon display RAM, A_R : RAM address (both of DD, CG and MK RAM) AC : Address counter used for both of DD, CG and MK RAM											

*:Don't care

NOTE1 fosc=145KHz. Change frequency, change execute time too.

(3-1)Description of each instructions

(a)Maker Testing

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	0

All "0" code in 4-bit length is using for device testing mode (only for maker).
Therefore, please avoid all "0" input or no meaning Enable signal input at data "0".
(Especially please check the output condition of Enable signal when the power turns on.)

(b)Clear Display

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	0	1

Clear display instruction is executed when the code "1" is written into DB_0.
When this instruction is executed, the space code $(20)_H$ is written into every DD RAM address, the DD RAM address $(00)_H$ is set into the address counter and entry mode is set increment.
If the cursor or blink are displayed, they are returned to the left end of the 1st line on the LCD.
The S of entry mode does not change.

Note: The character pattern for character code $(20)_H$ must be blank code in the user-defined character pattern(Custom font).

(c)Return Home

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	0	1	*

* =Don't Care

Return home instruction is executed when the code "1" is written into DB_1. When this instruction is executed, the DD RAM address $(00)_H$ is set into the address counter. Display is returned its original position if it is shifted, the cursor or blink are returned to the left end of the 1st line in the LCD if the cursor or blink are on the display.
The DD RAM contents do not change.

(d) Entry Mode Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	0	1	I/D	S

Entry mode set instruction which sets the cursor moving direction and display shift On/Off, is executed when the code "1" is written into DB_2 and the codes of (I/D) and (S) are written into DB_1(I/D) and DB_0(S), as shown below.
(I/D) sets the address increment or decrement, and the (S) sets the entire display shift in the DD RAM writing.

I/D	Function
1	Address increment: The address of the DD RAM or CG RAM increment (+1) when the read/write, and the cursor or blink move to the right.
0	Address decrement: The address of the DD RAM or CG RAM decrement (−1) when the read/write, and the cursor or blink move to the left.

S	Function
1	Entire display shift. The shift direction is determined by I/D.: shift to the left at I/D=1 and shift to the right at the I/D=0. The shift is operated only for the character, so that it looks as if the cursor stands still and the display moves. The display does not shift when reading from the DD RAM and writing/reading into/from CG RAM.
0	The display does not shift.

(e)Display ON/OFF Control

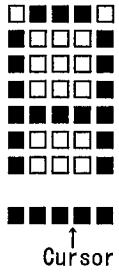
	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	0	0	0	0	1	D	C	B

Display On/Off control instruction which controls the whole display On/Off, the cursor On/Off and the cursor position character blink, is executed when the code "1" is written into DB_3 and the codes of (D), (C) and (B) are written into DB_2(D), DB_1(C) and DB_0(B), as shown below.

D	Function
1	Display On.
0	Display Off. In this mode, the display data remains in the DD RAM so that it is retrieved immediately on the display when the D change to 1.

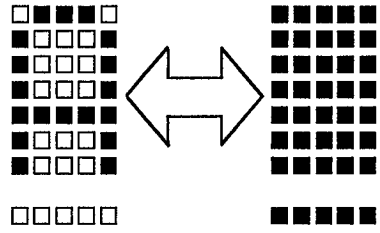
C	Function
1	Cursor On. The cursor is displayed by 5 dots on the 8th line.
0	Cursor Off. Even if the display data write, the I/D etc does not change.

B	Function
1	The cursor position character is blinking. Blinking rate is 600ms at f_{osc}=145kHz. The cursor and the blink can be displayed simultaneously.
0	The character does not blink.



Character Font 5 x 8 dots

(1)Cursor display example



Alternating display

(2)Blink display example

(f)Cursor/Display Shift

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	0	1	S/C	R/L	*	*	* =Don't Care

The Cursor/Display shift instruction shifts the cursor position or display to the right or left without writing or reading display data. This function is used to correct or search the display. The cursor moves to the 2nd line when it passes the 16th digit of the 1st line. Notice that the every 1st to 3rd line displays shift at the same time. When the displayed data are shifted repeatedly, each line moves only horizontally.
The 2nd and 3rd line display does not shift into the 1st and 2nd line.
The contents of address counter(AC) does not change by operation of the display shift only.
This instruction is executed when the code "1" is written into DB_4 and the codes of (S/C)and (R/L) are written into DB_3(S/C) and DB_2(R/L), as shown below.

S/C	R/L	Function
0	0	Shifts the cursor position to the left ((AC) is decremented by 1)
0	1	Shifts the cursor position to the right ((AC) is incremented by 1)
1	0	Shifts the entire display to the left and the cursor follows it.
1	1	Shifts the entire display to the right and the cursor follows it.

(g)Function Set

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	0	1	DL	*	*	*	PD	* =Don't Care

Function set instruction which sets the interface data length and powerdown mode, is executed, when the code "1" is written into DB_5 and the code of (DL) and (PD) is written into DB_4 (DL) and DB_0 (PD), as shown below. In the serial interface operation, the DL is not cared. When the powerdown mode is set, the display is off automatically (D=0). Afterward, when the powerdown mode is reset, the display is off continuously. The display is appeared by the display on (D="1") instruction.

Note : This function set instruction must be performed at the head of the program prior to all other existing instructions(except Busy flag/Address read). This function set instruction can not be executed afterwards unless the interface data length change.

DL	Function
1	Set the interface data length of 8-bit (using from DB_7 to DB_0) in the parallel operation only
0	Set the interface data length of 4-bit (using from DB_7 to DB_4) in the parallel operation only the data must be sent or received twice in this mode.

PD	Function
1	Power down mode off (Normal operation)
0	Power down mode on (The display goes to off automatically.)

(h) Contrast Control

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	0	0	0	1	*	*	C_3	C_2	C_1	C_0	* =Don't Care

Contrast Control instruction which adjusts the contrast of the LCD, is executed when the code "1" is written into DB_6 and the codes of C_3 to C_0 are written into DB_3 to DB_0 as shown below.
The contrast of LCD can be adjusted one of 16 voltage stage by setting this 4-bit register.
See (5-1) to realize "how to adjust the Contrast of LCD".
Set the binary code "0000" when contrast adjustment is unused.

contrast	C_3	C_2	C_1	C_0
low	0	0	0	0
	:	:	:	:
	:	:	:	:
high	1	1	1	1

(i) Set RAM Address

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	0	1	A_6	A_5	A_4	A_3	A_2	A_1	A_0
				←Higher order bit				Lower order bit→		

The RAM address set instruction is executed when the code "1" is written into DB_7 and the address is written into DB_6 to DB_0 as shown above.
The address data (DB_6 to DB_0) is written into the address counter (AC) by this instruction. After this instruction execution, the data writing/reading is performed into/from the addressed RAM.
The RAM includes DD RAM, CG RAM and MK RAM, and these RAMs are shared by address as shown below.

			RAM address
DD RAM	1st Line	:	from $(00)_H$ to $(0F)_H$
DD RAM	2nd Line	:	from $(10)_H$ to $(1F)_H$
DD RAM	3rd Line	:	from $(20)_H$ to $(2F)_H$
CG RAM	4characters	:	from $(40)_H$ to $(5F)_H$
MK RAM	152icon	:	from $(60)_H$ to $(7F)_H$

(j) Read Busy Flag & AC contents

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	0	1	BF	A_6	A_5	A_4	A_3	A_2	A_1	A_0
				←Higher order bit				Lower order bit→		

This instruction reads out the internal status of the NJU6464. When this instruction is executed, the busy flag (BF) stored in DB_7 and the address counter (AC) contents stored in DB_6 to DB_0 are read out.
The (BF)="1" indicates that internal operation is in progress. The next instruction is inhibited when (BF)="1". Check the (BF) status before the next write operation.

(k)Write Data to RAM

Write Data to RAM instruction is executed when the code "1" is written into (RS) and code "0" is written into (R/W).
By the execution of this instruction, the binary 8-bit data (A_7 to A_0) are written into the DD RAM, and the binary 5-bit data (A_4 to A_0) are written into the CG or MK RAM. The selection of RAM is determined by the previous instruction. After this instruction execution, the address increment(+1) or decrement(-1) is performed automatically according to the entry mode set.
And the display shift is also executed according to the previous entry mode set.

·Write Data to DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
			←Higher order bit						Lower order bit→	

·Write Data to CG or MK RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	0	*	*	*	D_4	D_3	D_2	D_1	D_0
						←Higher order bit			Lower order bit→	

(l)Read Data from MK RAM

Read Data from RAM instruction is executed when the code "1" is written into (RS) and (R/W).
By the execution of this instruction, the binary 8-bit data (D_7 to D_0) are read out from the DD RAM, the binary 5-bit data (D_4 to D_0) are read out from the CG or MK RAM. The selection of RAM is determined by previous instruction. Before executing this instruction, RAM address set must be executed, otherwise the read out data are invalidated.
When this instruction is serially executed, the next address data is normally read from the second read.
The RAM address set instruction is not required if the cursor shift instruction is executed just beforehand (only DD RAM reading). The cursor shift instruction has same function as the DD RAM address set, so that after reading the DD RAM, the address increment or decrement is executed automatically according to the entry mode.
But display shift does not operate regardless of the entry mode.

Note : The address counter(AC) is automatically incremented or decremented by 1 after write instruction to either of the DD RAM, CG RAM or DD RAM. Even if the read instruction is executed after this write instruction, the addressed data can not be read out correctly.
For a correct data read out, either the address set instruction or cursor shift instruction (only with DD RAM) must be implemented just before this instruction or from the second time read out instruction execution if the read out instruction is executed 2 times consecutively.

·Read Data from DD RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0
Code	1	1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0
			←Higher order bit						Lower order bit→	

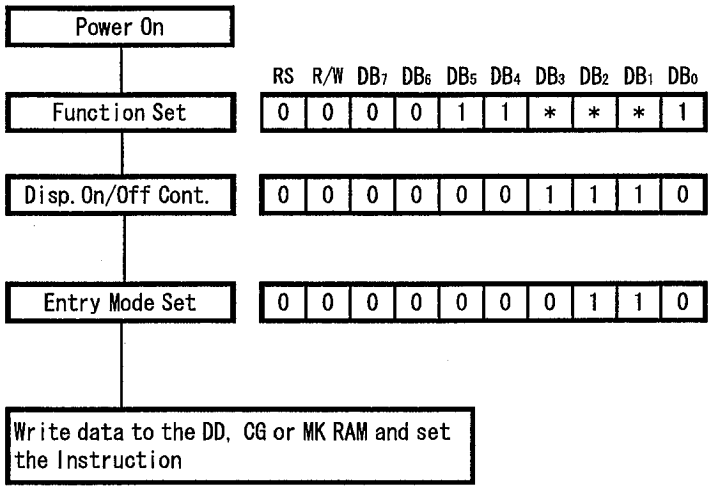
·Read Data from CG or MK RAM

	RS	R/W	DB_7	DB_6	DB_5	DB_4	DB_3	DB_2	DB_1	DB_0	
Code	1	1	*	*	*	D_4	D_3	D_2	D_1	D_0	* =Don't Care
						←Higher order bit			Lower order bit→		

(3-2) Initialization using the internal reset circuits

(a) 8-bit operation (Using internal reset circuits).

The Function set, Display On/Off Control and Entry Set Instruction must be executed before the data input, as shown below.



Initialized.
No display appears.

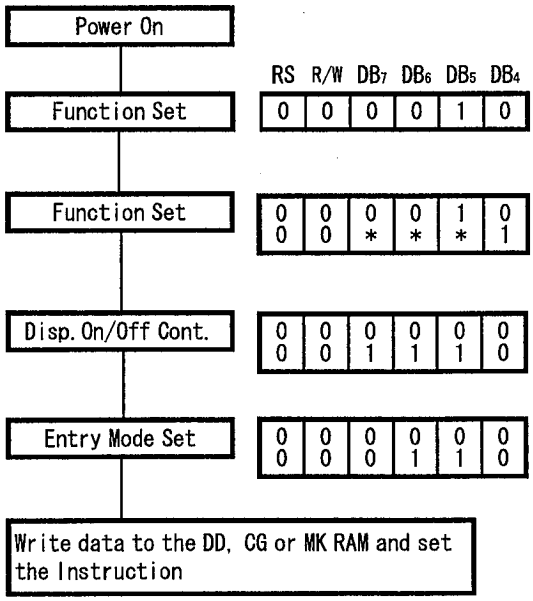
Set the 8-bit operation and Power down mode off.

Turns on display and cursor.
Entire display is in space mode set by the initialization.

Example for set address increment and cursor right shift when the data write to the DD, CG or MK RAM.

(b) 4-bit operation (Using internal reset circuits).

In the 4-bit operation, the function set must be performed by the user programming.
When the power is turned on, 8-bit operation is selected automatically, therefore the first input is performed under 8-bit operation. In this operation, full instruction can not input because of terminals DB_0 to DB_3 are no connection. Therefore, same instruction must be rewritten on the RS, R/W and DB_7 to DB_4, as shown below. Since one operation is completed by the two accesses in the 4-bit operation mode, rewrite is required to set the instruction code in full.



Initialized.
No display appears.

Set the 4-bit operation.
This step is executed in 8-bit mode set by the initialization.

Set the 4-bit operation, Power down mode off, 5 x 8 dots Font.
The 4-bit operation starts from this step.

Turn on display and cursor.
Entire display is in space mode set by the initialization.

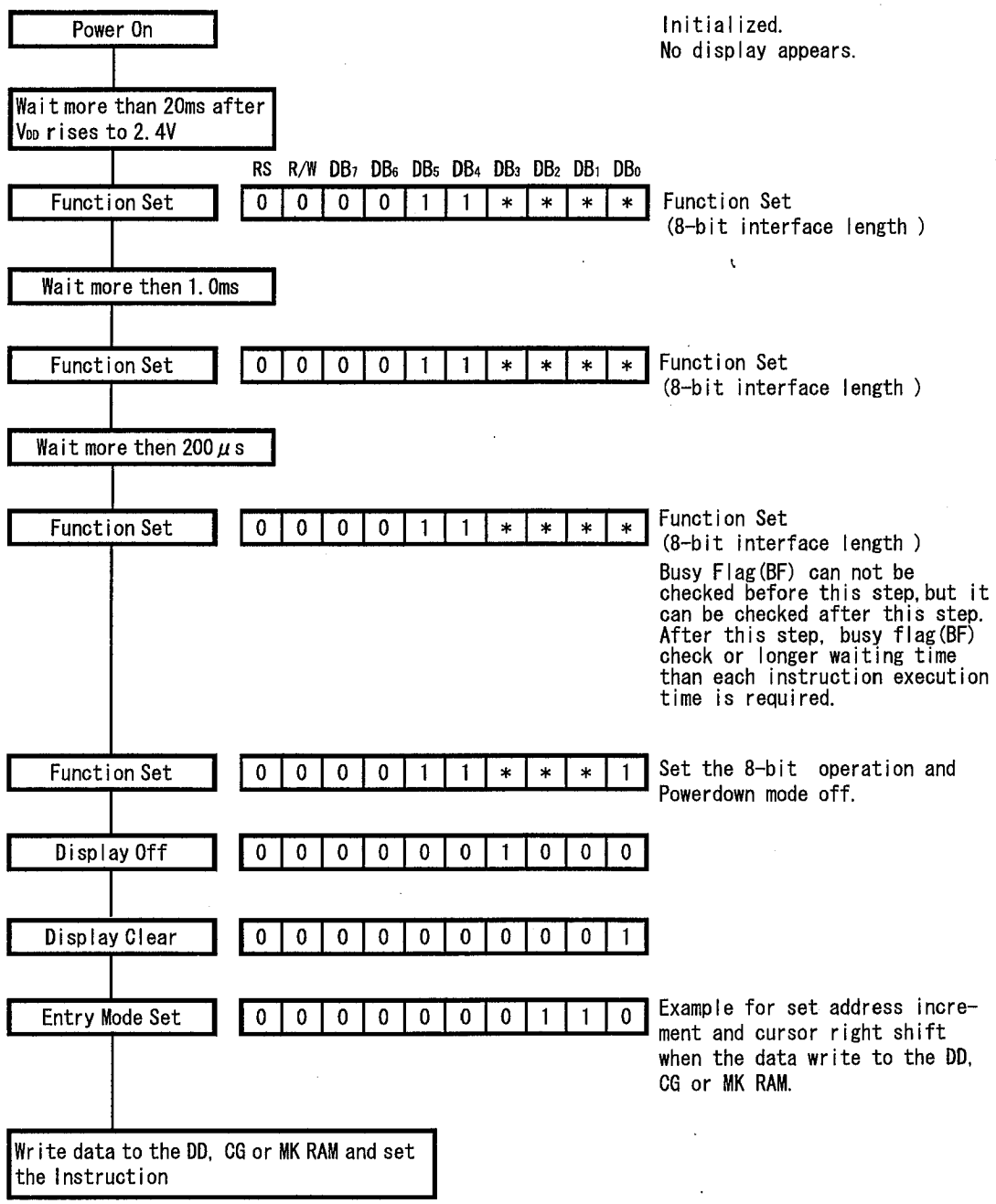
Example for set address increment and cursor right shift when the data write to the DD RAM or CG RAM.

Note : When the Icon display function using, the system should be initialized by software initialization.

(3-3) Initialization by instruction

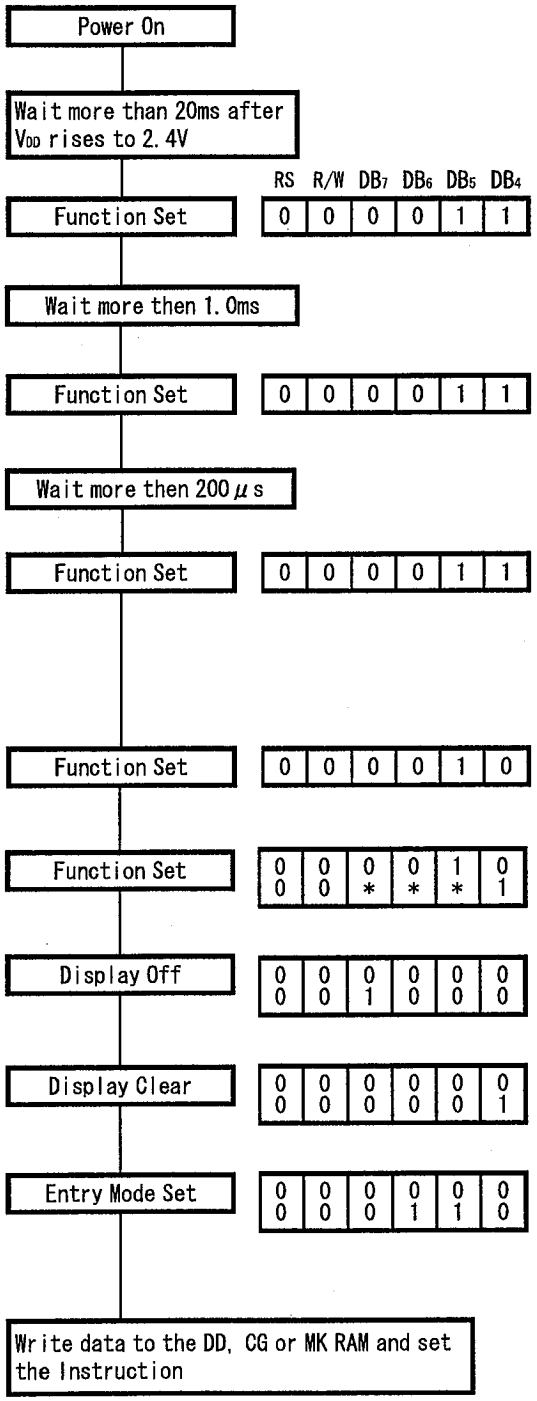
If the power supply conditions for the correct operation of the internal reset circuits are not met, the NJU6464 must be initialized by the instruction.

(a) Initialization by Instruction in 8-bit interface length.



Note : When the Icon display function using, the system should be initialized by software initialization.

(b) Initialization by Instruction in 4-bit interface length



Note : When the Icon display function using, the system should be initialized by software initialization.

(4)Powerdown Function

NJU6464 incorporates the powerdown mode to decrease the operating current.
The powerdown mode can be set/reset by the function set instruction.
In the powerdown mode, all the character display (16-character 3-line) and icon display turn off and only the static display area operates automatically.
The status of internal circuits at the powerdown mode is shown below :

- Main oscillator stops operation and sub oscillator for the static display starts operations.
- Voltage converter, voltage regulator and buffer amplifier for the bleeder resistance stop the operation.
- The contents of DD RAM, CG RAM and MK RAM are kept.

(5)LCD display

(5-1)Power Supply for LCD Driving

NJU6464 incorporates Voltage converter (tripler or doubler) to generate the LCD driving high voltage, Voltage regulator to adjust the LCD driving voltage, Bleeder resistance and buffer amplifier.

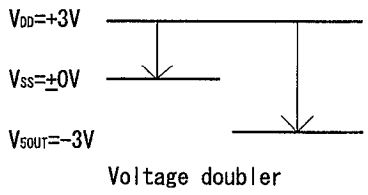
(a)Voltage converter

- Voltage tripler

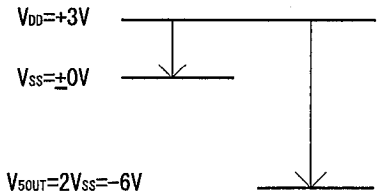
By connecting the capacitor between C_1^+ and C_1^-, C_2^+ and C_2^-, V_{SS} and V_{5OUT} respectively, two times negative voltage of $V_{DD}-V_{SS}$ output from V_{5OUT}.

- Voltage doubler

By connecting the capacitor between C_2^+ and C_2^-, V_{SS} and V_{5OUT} respectively, and connecting the C_1^+ terminal to C_2^+ terminal, and C_1^- terminal being open, negative voltage of $V_{DD}-V_{SS}$ output from V_{5OUT}.



Voltage doubler

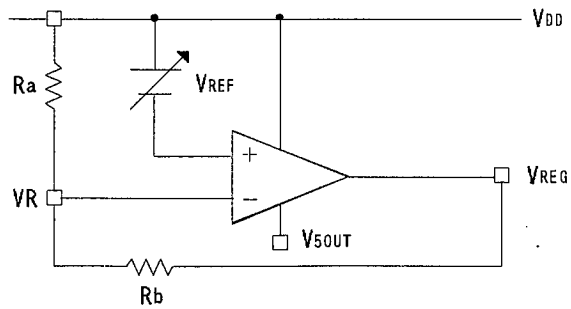


Voltage tripler

(b)Voltage Regulator

Voltage Regulator incorporates a non-inverting OP-AMP which supplied V_{DD} and V_{5OUT}, and a reference voltage source.
By setting the VR level by connecting R_a and R_b, the regulator which amplifies V_{REF} output the LCD driving voltage to the V_{REG} terminal.
Therefore, the LCD operating voltage can be output between V_{DD} and V_{REG} by setting V_{REF} and the external resistances R_a and R_b.

$$V_{REG} = (1+R_b/R_a) \cdot V_{REF} \quad \text{where,} \quad V_{DD} = 0V \quad \text{and} \quad |V_{REG}| < |V_{5OUT}|$$

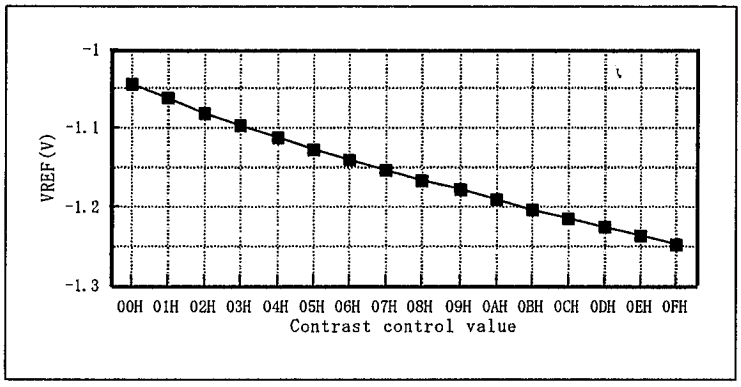


The contrast control function performs V_{REF} value adjustment from 1st step to 16th step by a step setting when the 4-bit data write into the contrast control register by the instruction.

Note : Set the contrast control register to $(00)_H$ when the contrast control function is unused.
Use variable resistances to the external resistances R_a, R_b and a thermistor if need due to the voltage reference V_{REF} is changed by the lot and operating temperature.
Take care the Noise input on the V_R terminal because of it designed in high impedance.
Short wiring or sealed wiring are required to avoid the noise input, if necessary.

[The Voltage Reference VREF characteristics]

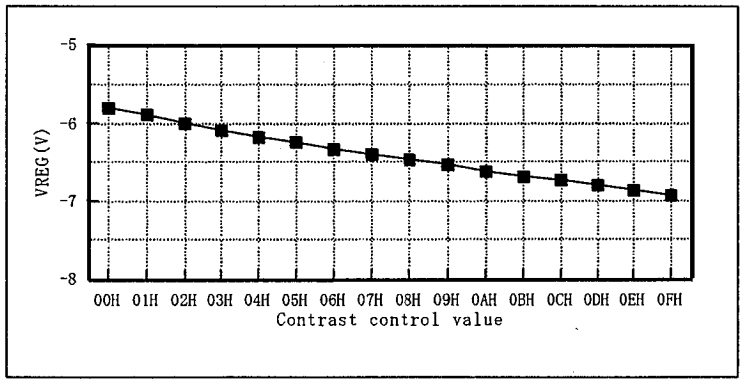
Supply Voltage : V_{DD}= 0V, V_{SS}= -3V Temperature : 25°C



[The LCD Operating Voltage V_{REG} characteristics]

Supply Voltage : V_{DD}= 0V, V_{SS}= -3V Voltage Tripler Output : V_{5OUT}= -9V
External Resistances : R_a = 180K Ω, R_b = 820K Ω Temperature : 25°C

Used Equation : $V_{REG}(xx)_H = (1 + 820k\,\Omega / 180k\,\Omega) \cdot V_{REF}(xx)_H$



(c)Bleeder Resistance

Each LCD driving voltage (V_1, V_2, V_3, V_4) is generated by the high impedance bleeder resistance buffered by voltage follower OP-AMP to get a enough display characteristics with low operating current.

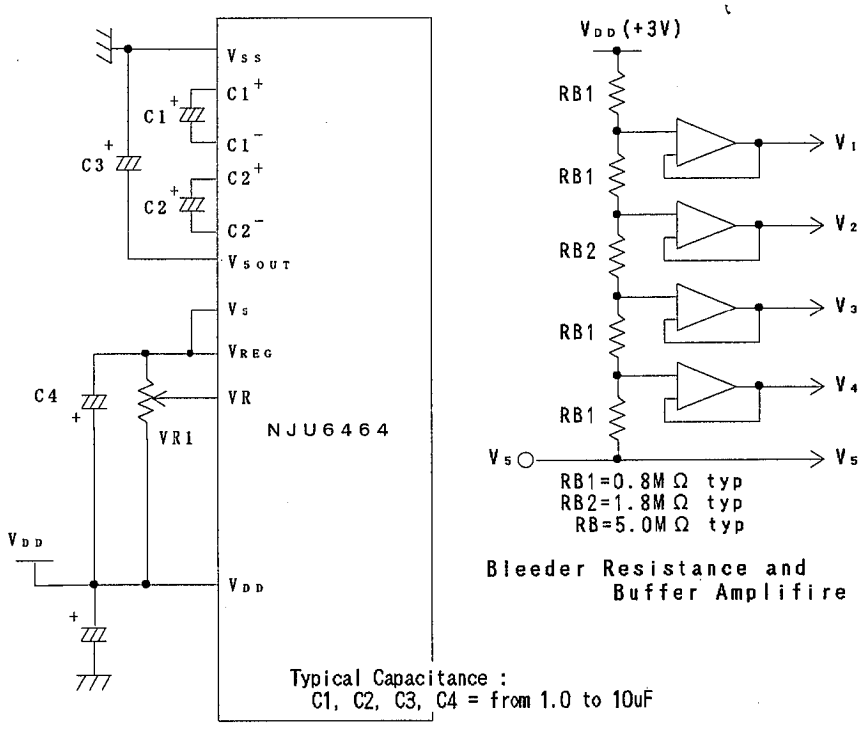
The bleeder resistance is set 1/6.3 bias suitable for 1/28 duty ratio and 5MΩ resistance in total.

The capacitor connected between V_5 and V_{DD} is needed for stabilizing V_5. The determination of the each capacitance of C_1, C_2 and C_3 generating for LCD operating voltage, is required to operate with the LCD panel actually. The capacitance for the typical application is shown below :

LCD Driving Voltage vs Duty Ratio

Power supply	Duty Ratio	1/28
	Bias	1/6.3
V_{LCD}		$V_{DD} - V_5$

V_{LCD} is the maximum amplitude for LCD driving voltage.



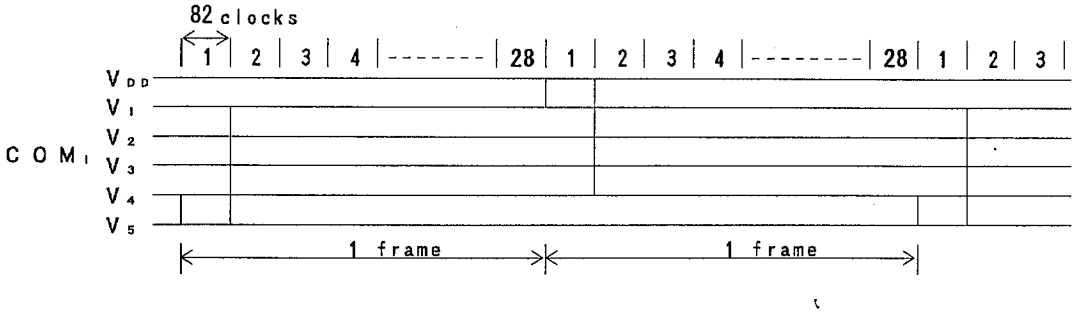
Typical application for LCD operating voltage generation

Note 1 : Take care the Noise input on the V_R terminal as designed in high impedance. Short wiring or sealed wiring are required to avoid the noise input, if necessary.

(5-2) Relation between oscillation frequency and LCD frame frequency

As the NJU6464 incorporate oscillation capacitor and resistor for CR oscillation, 145kHz oscillation is available without any external components.
The LCD frame frequency example mentioned below is based on 145kHz oscillation. (1clock =6.90 μ s)

1/28 duty ratio



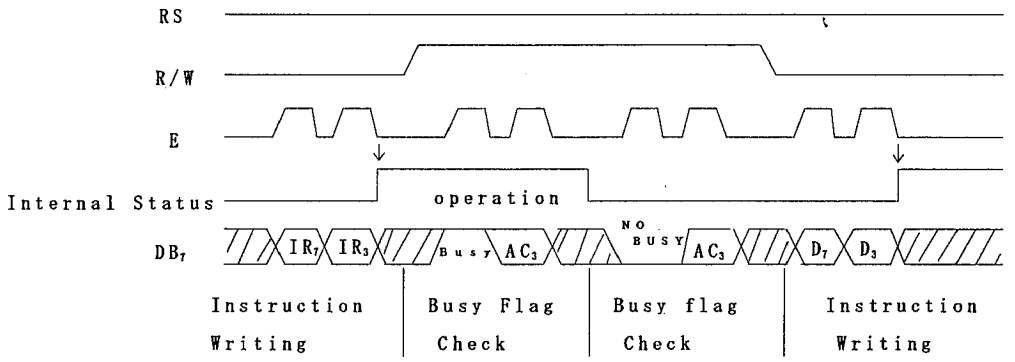
1 frame = 6.90(μ s) x 82 x 28 = 15.84(ms)
Frame frequency = 1 / 15.84(ms) = 63.1(Hz)

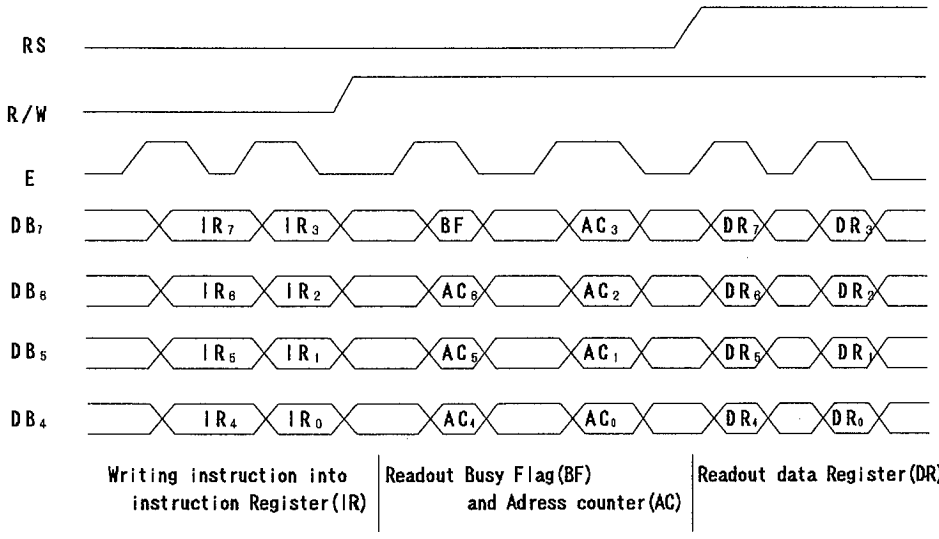
(6) Interface with MPU

Interface circuits of NJU6464 can be connected to serial or 4/8-bit parallel.
NJU6464 can be interfaced with both of 4/8-bit MPU and the two-time 4-bit or one-time 8-bit data transfer is available.

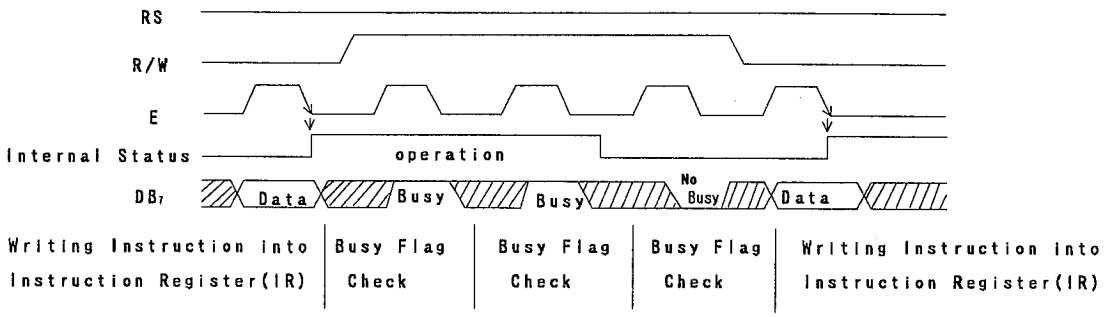
(6-1) 4-bit MPU interface

When the interface length is 4-bit, the data transfer is performed by 4 lines connected to DB_4 to DB_7 (DB_0 to DB_3 are not used). The data transfer with the MPU is completed by the two time 4-bit data transfer.
The data transfer is executed in the sequence of upper 4-bit (the data DB_4 to DB_7 at 8-bit length) and lower 4-bit (the data DB_0 to DB_3 at 8-bit length).
The busy flag check can be executed after two-time 4-bit data transfer (1 instruction execution by two-time transfer). In this case, the data of busy flag and address counter contents are also output twice.





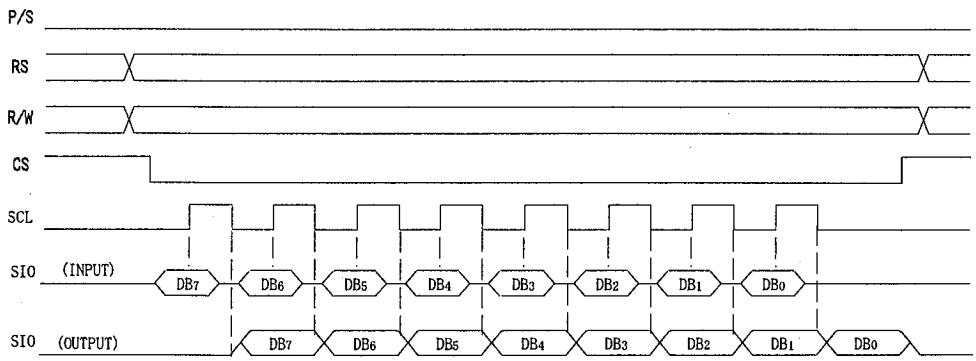
(6-2) 8-bit MPU interface



(6-3) Serial interface

Serial interface circuit is activated when the P/S terminal is set to "L" level then the chip select terminal (CS) goes to "L" level. The data input/output is MSB first like as the order of DB_7, DB_6 ···· DB_0.
The input data is entered into the shift register synchronized at the rise edge of the serial clock SCL. The shift register converted to parallel data at the CS rise edge input.
In case of entering over than 8-bit data, valid data is last 8-bit data.
The output data is exited from the shift register synchronized at the fall edge of the serial clock SCL.
The time chart for the serial interface is shown below.

Note : The level ("L" or "H") of RS and R/W terminals should be set before CS terminal goes to "L" level.



■ ABSOLUTE MAXIMUM RATINGS

(Ta=25°C)

PARAMETER	SYMBOL	RATINGS	UNIT	NOTE
Supply Voltage	V_{DD}	-0.3～+7.0	V	
Input Voltage	V_{IN}	-0.3～V_{DD}+0.3	V	
Operating Temperature	Topr	-30～+80	°C	
Storage Temperature	Tstg	-55～+125	°C	

Note 1 : If the LSI are used on condition above the absolute maximum ratings, the LSI may be destroyed. Using the LSI within electrical characteristics is strongly recommended for normal operation. Use beyond the electric characteristics conditions will cause mal function and poor reliability.
Note 2 : Decoupling capacitor should be connected between V_{DD} and V_{SS} due to the stabilized operation for the Voltage converter.
Note 3 : All voltage values are specified as V_{SS} = 0V
Note 4 : The relation : $V_{DD} > V_{SS}$, $V_{DD} > V_{SS} \geqq V_{5OUT}$, V_{SS}=0V must be maintained.

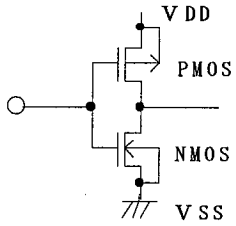
■ ELECTRICAL CHARACTERISTICS

(V_{DD} =2.4～3.3V、Ta=-20～+75°C)

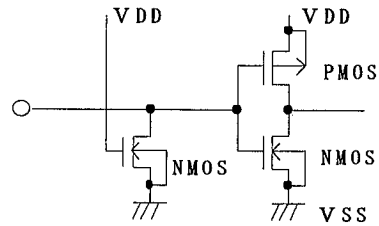
PARAMETER		SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Operationg Voltage		V_{DD}		2.4	3.0	3.3	V	
Input Voltage		V_{IH}		0.8V_{DD}	—	V_{DD}	V	4
		V_{IL}		V_{SS}	—	0.2V_{DD}	V	5
Output Voltage		V_{OH}	$-I_{OH}$=0.205mA、V_{DD}=3V	2.0	—	—	V	6
		V_{OL}	I_{OL}=1.6mA、V_{DD}=3V	—	—	0.5	V	
Driver On-resist. (COM)		R_{COM}	$\pm I_d$=1μA (All com term.)	—	—	20	kΩ	9
Driver On-resist. (SEG)		R_{SEG}	$\pm I_d$=1μA (All seg term.)	—	—	30	kΩ	
Input Leakage Current		I_{LI}	V_{IN}=0 or V_{DD}	-1	—	1	μA	7
Pull-up MOS Current		$-I_P$	V_{DD}=3V, (All DB terminals)	10	25	50	μA	
Operating Current		I_{DD1}	V_{DD}=3V f_{OSC}=Internal Osc. V_5=-5V, during display	—	250	290	μA	8
		I_{DD2}	V_{DD}=3V f_{OSC}=Internal Osc. dyuring access, T_{CYCE}=5μs	—	—	500	μA	
		I_{DD3}	V_{DD}=3V, f_{OSC}=Internal Osc. during power down mode	—	—	20	μA	
Voltage Converter (Tripler)	Output Voltage	V_{5OUT}	V_{DD}=3V, Ta=25°C, I_{OUT}=100μA	-4.6	-4.8	—	V	
	Voltage Efficiency	V_{ef}	R_L=∞	90.0	95.0	—	%	
Voltage Regulator	Reference Voltage	V_{REF}	Contrast Control $(00)_H$ Ta=25°C	-1.3	-1.0	-0.7	V	
	Output Voltage	V_{REG}	R_L=∞, V_{5OUT}=-10V, R_{RV}=1MΩ Contrast Control $((00)_H$	-10	—	-1.8		
Bleeder resistance		R_B	V_{DD}-V_5=3V	—	5.0	—	MΩ	
Oscillation Frequency		f_{OSC}	V_{DD}=3V, Ta=25°C	110	145	180	kHz	
LCD Driving Voltage		V_{LCD}	V_{LCD}=V_{DD}-V_5	V_{DD}-5.0	—	V_{DD}-10.0	V	10

Note 5 : Input/Output structure except LCD driver are shown below:

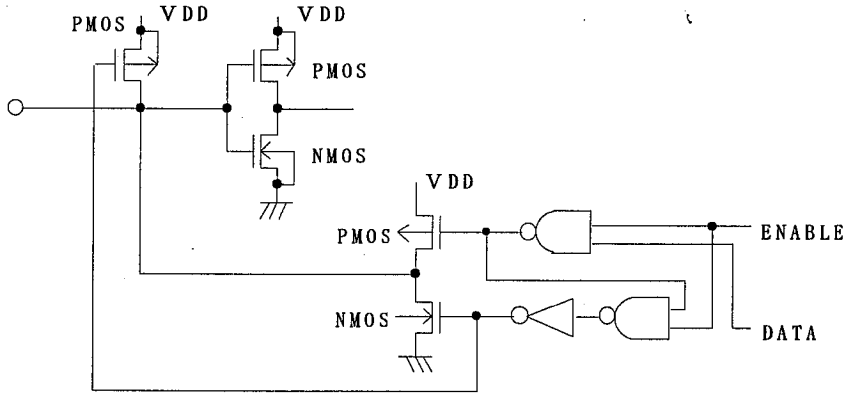
·Input Terminal Structure
E/SCL, RS, R/W, P/S, SEL, $\overline{\text{RESET}}$ Terminals



TEST Terminal (Pull-Down MOS)

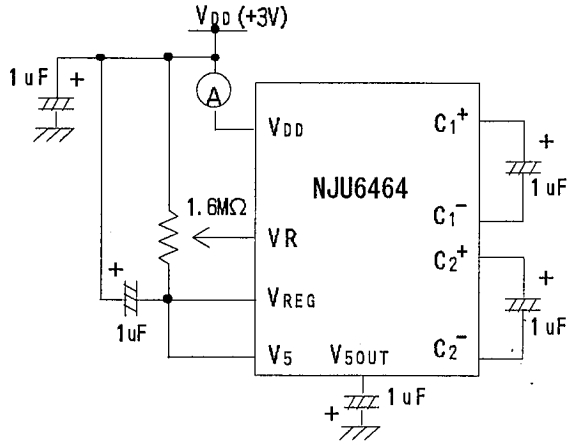


·Input/Output Terminal Structure
DB_0 to DB_7 Terminals



Note 6 : Apply to the Output and Input/Output Terminals.
Note 7 : Except pull-up resistance current and output driver current.
Note 8 : Except Input/output current but including the current flow on bleeder resistance.
If the input level is medium, current consumption will increase due to the penetration current. Therefore, the input level must be fixed to "H" or "L".

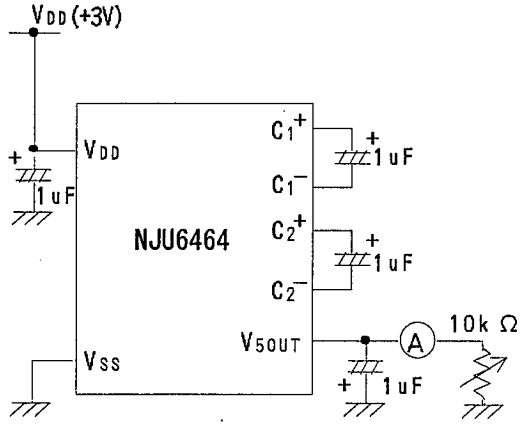
· Operating Current Measurement Circuit



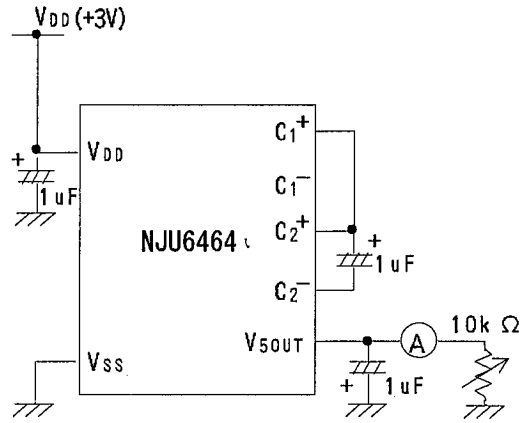
Note 9 : R_{COM} and R_{SEG} are the resistance values between power supply terminals (V_{DD}, V_{5OUT}) and each common terminal (COM_1 to COM_{24}, $COMMK_1$ to $COMMK_4$) and supply voltage (V_{DD}, V_{5OUT}) and each segment terminal (SEG_1 to SEG_{80}, $SEGM_1$ and $SEGM_2$) respectively, and measured when the current I_d is flown on every common and segment terminals at a same time.

Note 10: Apply to the output voltage from each COM and SEG are less than ±0.15V against the LCD driving constant voltage (V_{DD}, V_{5OUT}) at no load condition.

Voltage Tripler Measurement Circuit

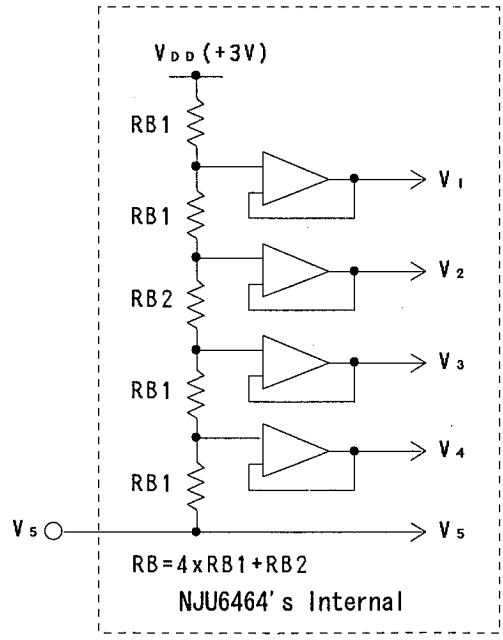


Voltage Doubler Measurement Circuit



Voltage Tripler/Doubler
Operation Clock Frequency = 10kHz

Bleeder Resistance
and Buffer Amplifier



・Bus timing characteristics (V_{DD} = 2.4～3.3V, V_{SS} = 0V, Ta =-20 ～ +75℃)

Write operation (Write from MPU to NJU6464)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Enable cycle time		t_{CYCE}	1	—	fig. 1	μs
Enable pulse width	"1" level	PW_{EH}	400	—		ns
Enable rise time, fall time		t_{Er}, t_{Ef}	—	20		
Set up time	RS, R/W, E	t_{AS}	200	—		
Address hold time		t_{AH}	200	—		
Data set up time		t_{DSW}	200	—		
Data hold Time		t_H	200	—		

Timing Characteristics (Write operation)

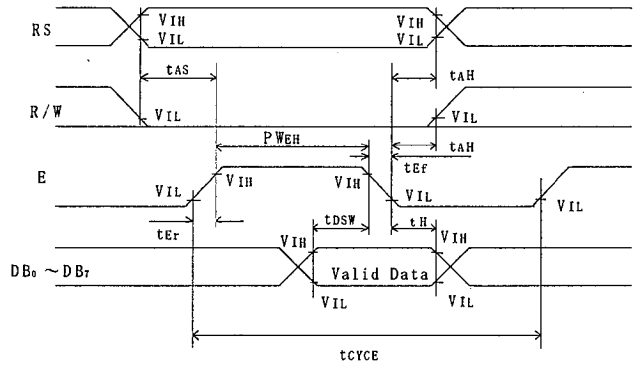


fig. 1

Read operation (Read from NJU6464 to MPU)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Enable cycle time		t_{CYCE}	1	—	fig. 2	μs
Enable pulse width	"1" level	PW_{EH}	600	—		ns
Enable rise time, fall time		t_{Er}, t_{Ef}	—	20		
Set up time	RS, R/W, E	t_{AS}	200	—		
Address hold time		t_{AH}	200	—		
Data delay time		t_{DDR}	—	500		
Data hold time		t_{DHR}	0	—		

Timing Characteristics (Read operation)

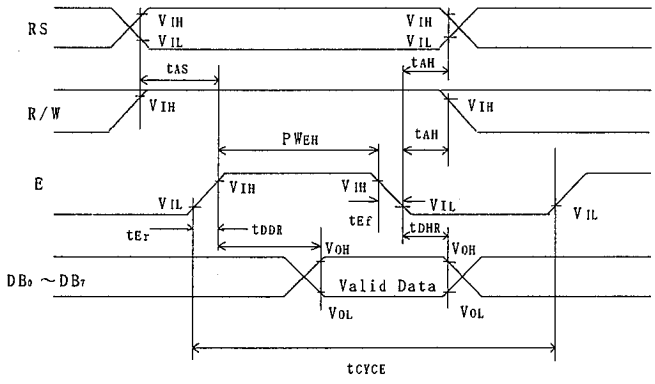


fig. 2

・Serial Interface Sequence

(V_{DD} = 2.4 ~ 3.3V , V_{SS} =0V, Ta =-20 ~ +75°C)

PARAMETER		SYMBOL	MIN.	MAX.	CONDITION	UNIT
Serial clock cycle time		t_{CYCE}	1	—	fig.3	μs
Serial clock width	"1" level	t_{SCH}	300	—		ns
	"0" level	t_{SCL}	700	—		
Serial clock rise and fall Time		t_{SCr}, t_{SCf}	—	20		
Chip select pulse width		PW_{CS}	500	—		
Chip select set up time		t_{CSU}	200	—		
Chip select hold time		t_{CH}	200	—		
Chip Select rise and fall Time		t_{CSr}, t_{CSf}	—	20		
Set up time	RS, R/W - CS	t_{AS}	200	—		
Address hold time	CS - RS, R/W	t_{AH}	200	—		
Serial input data set up time		t_{SISU}	200	—		
Serial input data hold time		t_{SIH}	200	—		
Serial output data delay time		t_{SOD}	—	700		
Serial output data hold time		t_{SOH}	0	—		

Load Condition of DB_0 to DB_7 : CL=100pF

Serial Interface

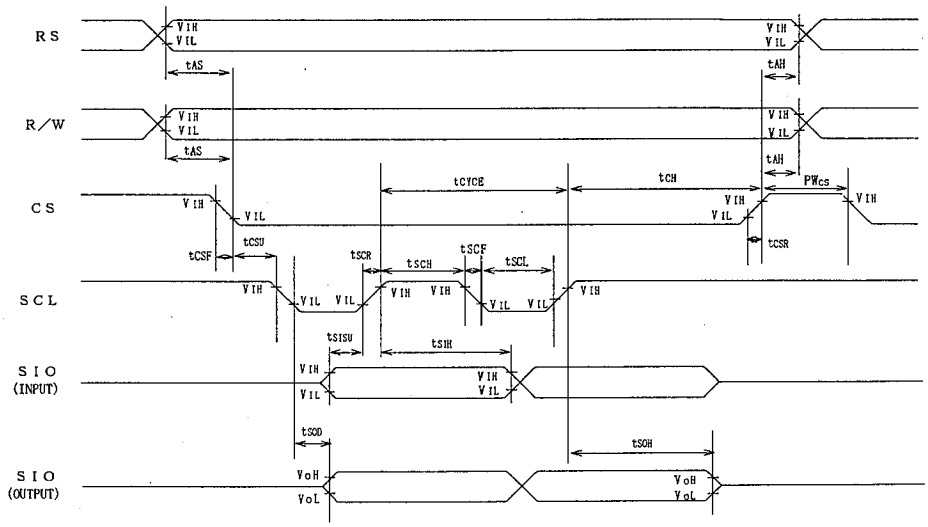
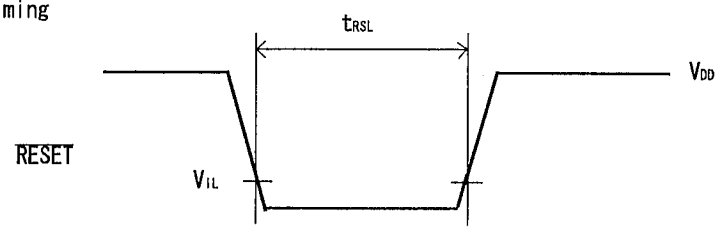


fig. 3

・The Input Condition when using the Hardware Reset Circuit

Input timing



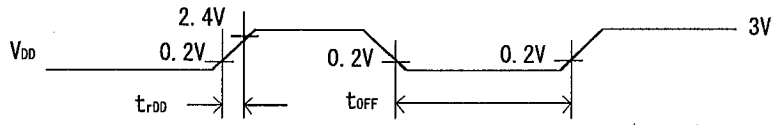
PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Reset input "0" level width	t_{RSL}	f_{OSC}=145kHz	1.2	—	ms

・Power Supply Condition when using the internal initialization circuit

(Ta = -20 ～ +75°C)

PARAMETER	SYMBOL	CONDITION	MIN	MAX	UNIT
Power supply rise time	t_{rDD}	—	0.1	5	ms
Power supply OFF time	t_{OFF}	—	1	—	ms

Since the internal initialization circuits will not operate normally unless the above conditions are met, in such a case initialize by instruction. (Refer to initialization by the instruction)

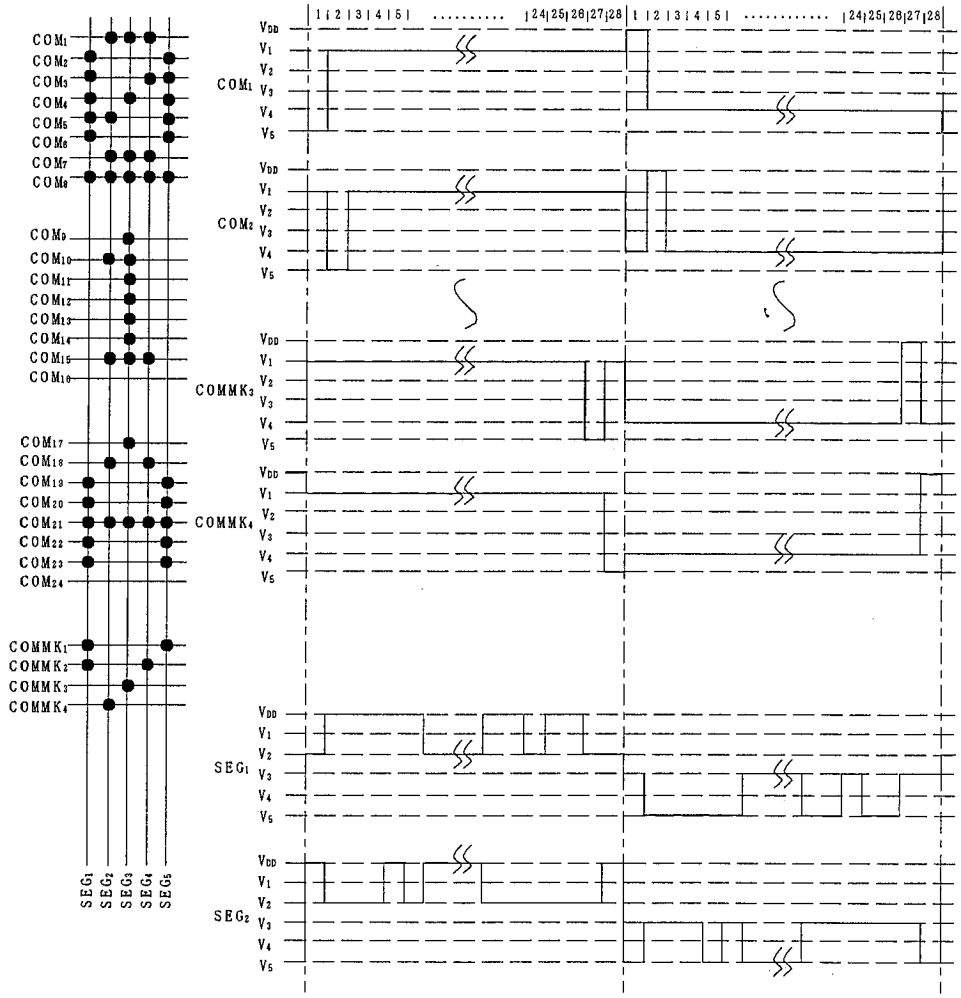


$0.1ms \leqq t_{rDD} \leqq 5ms$ $\quad t_{OFF} \geqq 1ms$

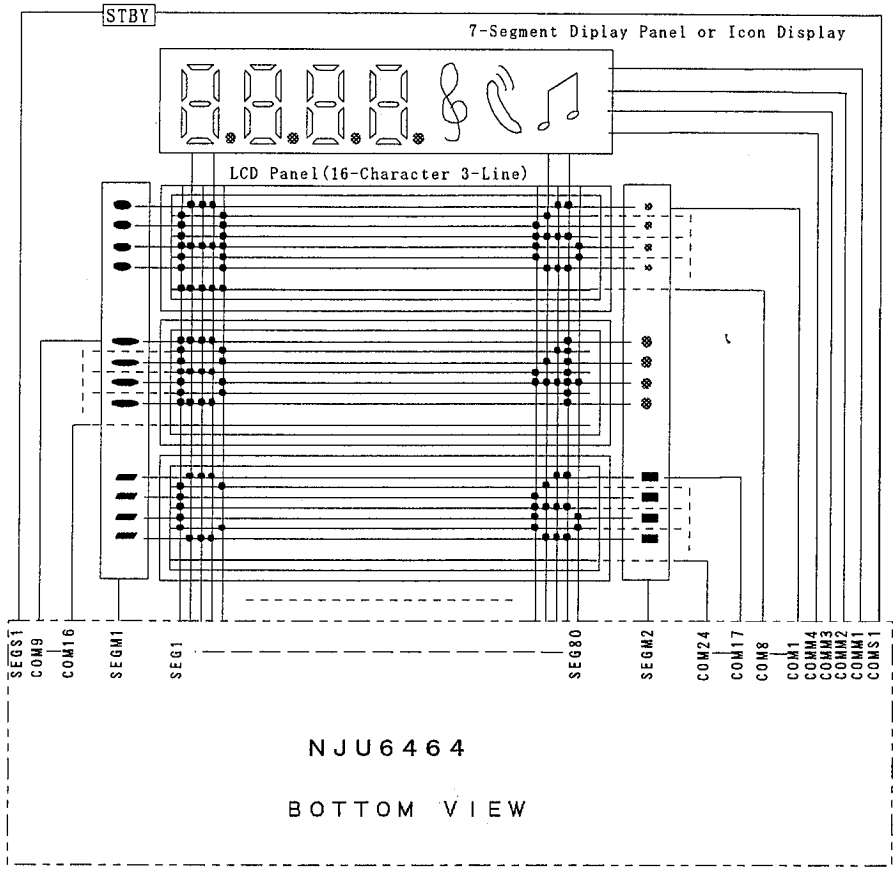
t_{OFF} specifies the power off time in a short period off or cyclical on/off.

■ LCD DRIVING WAVE FORM

1/28 Duty Driving

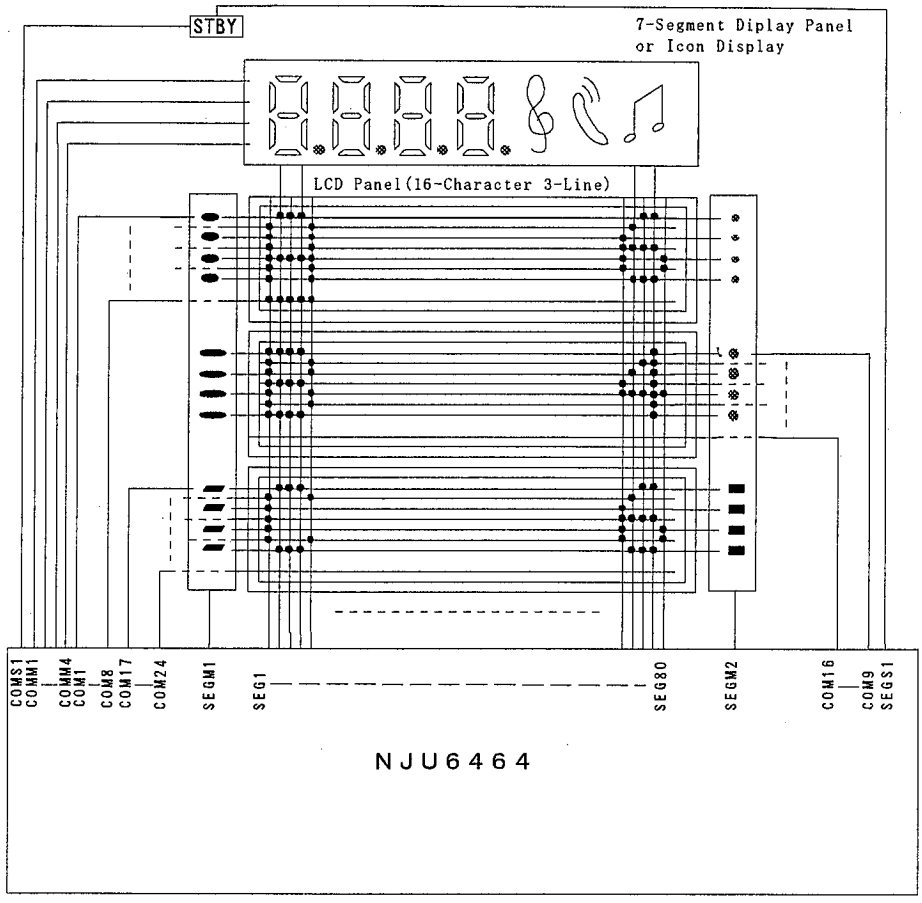


■ APPLICATION CIRCUITS (1)



16-character 3-line Display Example
(The terminal description is "Mode A".)

■ APPLICATION CIRCUITS (2)



16-character 3-line Display Example
(The terminal description is "Mode B".)

MEMO